Electron transport in semiconducting nanowires and quantum dots

by

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Abstract

Single electrons confined in electrostatic quantum dots are a promising platform for realizing spin based quantum information processing. In this scheme, the spin of each electron is encoded as a qubit, and can be manipulated and measured by modulating the gate voltages defining each dot. Since each qubit is realized in a single quantum dot, one could imagine scaling up this system by placing many quantum dots together in a tightly packed array. To be truly scalable each qubit must exhibit minimal variation, such that their behavior is consistent across the entire device. Transport through these quantum dots must therefore be explored in detail, to determine the source of these variations and design strategies to combat their effects.

In this thesis a study of the transport properties of InAs nanowires and Si quantum dots is presented. In both systems the close proximity of the conduction electrons to defect-prone surfaces or interfaces causes them to be very sensitive to the physical properties of these regions. Through cryogenic transport measurements, and the development of relevant physical models, the effects of surface states, oxide charge traps, and interface defects are explored. In general these defects possess a finite charge, which modifies the electrostatic potential and alters electron transport. These additional changes to the electrostatic potential are detrimental for spin based quantum information processing, which requires precise control of this potential. In addition, the severity of each of these effects can be different in each device, leading to variation which limits scalability. By studying these effects we aim to better understand their properties and origins, such that they can be mitigated.

Static defects, such as surface states, are found to be a dominant source of scattering that limits mobility. In InAs nanowires, we find that these effects can be removed through growth of an epitaxial shell that physically separates the nanowire surface from the conducting core. Dynamic defects on the other hand, lead to charge noise that shifts the potential causing instability. This noise originates from charge traps in close proximity to the conduction channel. For nanowires, the native oxide that forms at the surface is a likely location for these traps to occur. Through removal of this oxide and replacement with a defect free dielectric shell, greatly improved stability is observed. To test the viability of these fabrication techniques, nanowires treated with the most promising surface processes are used to fabricate top-gated nanowire field effect transistors. These devices are used to realize electrostatically defined double quantum dots, which show well controlled transport properties and minimal charge noise.

In Si, electron transport is studied in a pair of capacitively coupled metal-oxide-semiconductor quantum dots. Here, the capacitive coupling is used implement charge sensing, such that

the electrostatic potential of one dot can be measured down to the single electron regime. The pair of dots is also used to implement a novel memristive system which demonstrates current hysteresis. This shows the versatility of this system and its capability to control individual electrons, similar to the requirements needed to implement spin based quantum information processing.

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Dedication

To my parents who taught me to use my mind, to follow my heart

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Chapter 1

Introduction

Chapter contributions: Simulations were performed using The R Project for Statistical Computing with scripts written by Gregory Holloway.

1.1 Introduction

Electron transport in solids plays a major role in our lives as it is the building block for a vast section of our current technology known as electronics. For many years, the flow of electrons in these systems was well described by classical physics in terms of voltage differences leading to current flow. As technology advances, the size of these systems has shrunk towards the atomic scale, leading to the breakdown of classical physics and the emergence of quantum phenomena. While these effects may need to be mitigated to preserve the classical operation of these devices, they also provide the potential for new technologies based on quantum behavior. This requires a thorough understanding of the underlying physics such that progress can be made from observing these effects to actively controlling them.

The overarching physical description of these small scale effects is quantum mechanics. While quantum mechanics is generally accepted as the correct description of the universe, it's effects are often counterintuitive. One major difficulty with understanding quantum mechanics is that our macroscopic view of the world is inherently classical. In classical mechanics objects react to forces to move in fixed trajectories. In contrast, in quantum mechanics an object's behavior is probabilistic allowing it to be in two states at once, or take multiple paths through a system. Electrons which are often pictured as particles of

matter moving through a circuit, can quantum mechanically behave as waves. This leads to interesting effects, such as an electron being able to interfere with itself, or tunneling through barriers that would classically be impassable. Observing these effects on individual electrons is difficult, and requires properly designing systems where these properties will dominate.

Electron transport itself can act as a probe of the environment seen by the electron. This transport can be measured as a macroscopic current, providing a means to observe quantum effects. For example, current through microscopic objects can change dramatically as the wave-like nature of the electron is confined. This can result in quantization of the electron's energy, yielding steps or peaks in the current [1]. Other quantum properties of the electron, such as it's intrinsic spin, can also effect transport[2, 3]. Semiconductors provide an ideal platform for studying these effects as the number of electrons in the material can be controlled through doping, or electrostatic gating. However, even when electrons are confined in the range of 20-100 nm, the separation of these energy levels is quite small, on the order of a few meV. This requires that all other energies in the system be lower than this value for these effects to be visible. Thermal energy blurs out quantum behavior at room temperature. This can be overcome by using cryostats to cool samples down to temperatures in the range of 25 mK - 4 K. With all of these requirements in place quantum effects can be observed and studied.

One goal of understanding quantum phenomena is to exploit these effects to realize new and more powerful technologies. The quantum computer is one such device, which combines the binary architecture of modern computing science with the properties of quantum mechanics to implement a new type of computation. In a classical computer, information is stored in classical bits which can be either a 0 or 1. Whereas in a quantum computer, the quantum bit or qubits are encoded quantum mechanically such that they can be in a superposition of the 0 and 1 states simultaneously. For N qubits, the computer can be in 2^N states at once, allowing each state to be operated on simultaneously. This can provide an exponential speed up for finding solutions to certain problems when compared to a classical computer. Theoretical work has developed several algorithms which are predicted to have more efficient solutions with a quantum computer, and include factoring of large numbers [4], and database search[5]. Quantum computers also provide a more natural platform for simulating quantum systems, such as quantum magnets [6], or quantum chemistry [7].

While several implementations of small scale prototypes have been demonstrated, a fully universal scalable computer has not been realized. Systems, like NMR, have been shown to exhibit fully universal control, but suffer from poor scalability [8]. One promising avenue for scalability is solid state systems, where many small devices with the desired electronic properties can be packed into a small space, analogous to modern computer chips. In

particular, the realization of electrostatically defined quantum dots can be used to confine and manipulate individual electrons. The electron's spin can then be encoded as a qubit, providing a robust platform for implementing spin-based quantum information processing. In theory the electron's charge could be used to encode a qubit, but the state would be numerous nearby charges leading to fast decoherence. The study of electron transport in semiconducting structures as potential candidates for quantum information processing platforms is the goal of this thesis.

1.2 Outline of the thesis

The rest of this chapter is focused on a discussion of the fundamentals of charge transport in nanowires and quantum dots. This theoretical description of transport provides the background information necessary to better understand the rest of the thesis. Chapter 2 presents a study of mobility in InAs nanowires. The temperature dependence of the mobility value is used to determine that ionized impurity scattering from surface states is the primary mechanism limiting mobility in these nanowires. The mobility of core/shell nanowires is also measured, and shows reduced scattering rates indicating that the addition of an epitaxial shell can remove some of the surface states. The presence of cystalline defects in the nanowire, such as stacking faults, is found to further lower the mobility. In chapter 3, the effect of charge noise on electron transport in InAs nanowires is studied. Abrupt jumps in conductance between two values are observed, and attributed to changes in the occupation of single electron charge traps near the nanowire. A model of the dynamics of these traps as a function of temperature and gate voltage is presented. The model shows good agreement with experimental data, and provides an estimate of the trap location relative to the surface of the nanowire. Chapter 4 looks at the occupation of transverse subbands in a nanowire as a function of an applied axial magnetic field. These subbands provide channels for electron transport, and thus directly affect the conductance of the nanowire. We present a model of magnetoconductance based on the subband occupation of a cylindrical wire. Experimental conductance is measured as a function of magnetic field and gate voltage, and the model is fitted to the data to extract the subband occupation, as well as an estimate of the electrostatic potential in the nanowire. The focus of chapter 5 is to test the effect of different surface passivation techniques on various transport properties of InAs nanowires. The ultimate goal being to determine which process gives the cleanest, most stable device suitable for implementing quantum information processing. The surface processes include wet etching of the nanowire oxide, formation of a self assembled monolayer, growth of a thermal oxide, and deposition of a dielectric shell. After fabrication and

measurement, each process was characterized based on its mobility, subthreshold swing, charge noise, and gate hysteresis. The most promising combination of techniques was then used to fabricate a top-gated nanowire device in a novel entrenched geometry capable of forming an electrostatic double quantum dot. The device showed unambiguous transport signatures of a double quantum dot, with minimal charge noise confirming the effectiveness of the surface processing.

Chapter 6 looks at Si metal-oxide-semiconductor quantum dots. We move away from III-V's, which are nuclear spin abundant, to group IV (Si), which can be isotopically purified (^{28}Si) to have no nuclear spins, and thus realize a magnetic "vacuum". This is attractive for spin based quantum information processing, since the low density of nuclear spins should improve electron spin coherence times. Here, transport through a pair of capacitively coupled quantum dots is studied to extract basic properties of each quantum dot. Next, one dot is employed as a charge sensor and used to measure the charge of the other dot down to the single electron regime where spin-based quantum information processing can be performed. The charge sensing not only reveals the electron number, but can also be used to probe the potential landscape of the other dot. The pair of dots is also used to implement a novel quantum memristive system, which has potential future applications as ultra dense, low power memory [9, 10]. In this configuration, the transport through one dot shows hysteretic behavior dependent on the charge state of the other dot. Chapter 7 presents conclusions and discusses future work.

1.3 Background

The purpose of this section is to provide a concise overview of the fundamentals of charge transport through 1D and 0D systems, eg. nanowires and quantum dots. We begin with a discussion of transport along semiconducting nanowires showing how the shape of the nanowire and its crystalline structure modify transport. Specific electrostatic potentials are then added to this system to present the ideas of surface accumulation, and confinement in a quantum dot. The dot is then abstracted away from the nanowire system to allow for a more in-depth explanation of the parameters governing transport through a quantum dot. Finally a look at transport through two quantum dots in series is presented as a means to study the spin of the confined electrons.

1.3.1 Nanowire transport

When placed in a solid the electron's wave function is dictated by the electrostatic potential of the material, due to the nuclei, other fixed charges, applied potentials, and the shape of the material. Including the kinetic term, the Hamiltonian can be written as:

$$H = \frac{\hbar^2 p^2}{2m} + V_{nuclei} + V_\alpha \tag{1.1}$$

where $\hbar = h/2\pi$ and h is Planck's constant, p is the momentum, m is the electron mass, V_{nuclei} is the electrostatic potential due to the material's positively charged nuclei, and V_α is the electrostatic potential from all other sources. For a crystalline material such as a semiconducting nanowire, V_{nuclei} is a periodic potential with a minimum at the position of each nucleus. A typical InAs nanowire is roughly 60 nm in diameter, with a lattice constant of ~ 0.6 nm, this suggests that the electron will see roughly 10,000 nuclei in a single nanowire cross-section alone. Trying to keep track of all of these nuclei would be an impossible task, so instead the effective mass approximation is employed. In this approximation, the motion of the electron through the periodic potential of the material can be recast as motion through free-space, but only in certain ranges or bands of energy. The curvature of these bands in momentum space determines the effective mass m^* of the electron in that band, which can be different from the true electron mass. This provides a simple means to capture some of the inherent properties of the host material, with a material specific value that replaces m in equation 1.1. The equation can thus be rewritten as [11]:

$$H = \frac{\hbar^2 p^2}{2m^*} + V_\alpha \tag{1.2}$$

The first case of V_α that will be assumed is a hard wall potential at the edges of the semiconductor material, i.e. the electron is confined inside the material. The hard wall potential is defined as:

$$V(r,\theta,l) = \begin{cases} 0, & \text{if } 0 < l < L \text{ and } r < R \\ \infty, & \text{otherwise} \end{cases} \tag{1.3}$$

where r, θ, and l are cylindrical coordinates for the nanowire with $r = 0$ being the center of the nanowire and $l = 0$ located at one end, R is the radius of the nanowire, and L is the length. By definition, nanowires have a much longer length than radius $L \gg R$. Therefore, it is a common assumption that the electron wavefunction is only confined radially, and in the axial direction the electron is allowed to propagate semi-infinitely. The Hamiltonian is then separated into axial and radial parts, and the electron wavefunction is found by

solving the time-independent Schrödinger equation. Axially, the electrons propagate as plane waves, whereas radial confinement causes the radial wavefunction to take the form of Bessel functions. The electron energy levels are thus quantized in the transverse direction and given by the 1D density of states in the axial direction.

Translating these electron wavefunctions into current measured through the nanowire is achieved using the Landauer approach. In the case of ballistic transport, the current carried by a single 1D channel at zero temperature is given by [12]:

$$I = \int_0^{eV} ev(E) g_{1D}(E) dE = \int_0^{eV} ev(E) \frac{2}{hv(E)} dE = \frac{2e}{h}(eV) \tag{1.4}$$

where V is the bias voltage applied to the nanowire, $v(E)$ is the group velocity, and g_{1D} is the 1D density of states. Thus each 1D channel carries a single quantum of conductance $G_0 = 2e^2/h$. The position of these 1D channels is given by the energy levels for the radial wavefunction. The effects of temperature can be included by smearing out these conductance levels with the Fermi-Dirac distribution.

$$I = \frac{2e}{h} \int_{-\infty}^{\infty} D(E)[f(E - \mu_L) - f(E - \mu_R)] dE \tag{1.5}$$

where $f(E) = [1 + \exp(E/k_B T)]^{-1}$, T is the temperature, E is the energy, $\mu_{L/R}$ are the chemical potentials of the leads, and $D(E)$ is the transmission coefficient of the system. $D(E)$ indicates the ratio of the number of electrons successfully transmitted through the system relative to the number incident electrons. This coefficient can therefore be used to include the effects of scattering. The voltage across the device sets the chemical potentials of the leads through: $V = \mu_L - \mu_R$. Simulated current calculated using equation 1.5 for a bias of 1 mV and a temperature of 20 K is shown in figure 1.1(b). The energies of the subbands are calculated for a cylindrical InAs nanowire with a diameter of 60 nm. For comparison, experimentally measured current through a 65 nm diameter nanowire with a length of 1 μm is shown in figure 1.1(a).

In semiconductors, fixed charge can lead to built in electrostatic potentials which can modify transport. For example, InAs has a surface charge density that causes the conduction band to bend down at the surface. Experimentally, this is a nice feature of the material as it induces an accumulation layer at the surface facilitating ohmic contacts with a variety of metals. This built-in potential also changes the electron wavefunction, and can be understood by adding an additional potential term to equation 1.2. The exact form of the radial potential is unknown, but a commonly used analytic form is: $V(r) = A(1 - (r/R)^{b/2})$ [13], where A and b are coefficients describing the shape of the potential. Since this potential

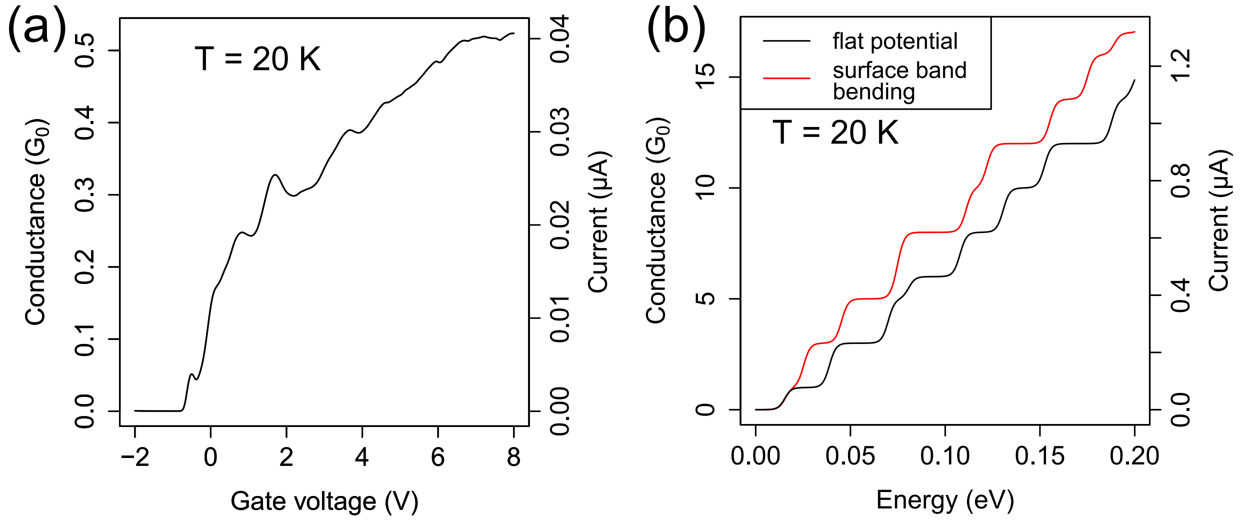

Figure 1.1: Experimental and simulated current through an InAs nanowire at 20 K, with a bias of 1 mV. (a) Current through a 1 μm long nanowire as a function of back gate voltage. The back gate changes the Fermi level inside the nanowire bringing different subbands into the bias window. Step-like features are visible in the conductance, but have a height much less than G_0 due to scattering. (b) Simulated current as a function of Fermi energy through a nanowire with and without surface band bending. The steps in current occur each time a new transverse subband is populated. The two curves show similar behavior, but with different subband energy level structures leading to different step positions.

is purely radial, the Hamiltonian can still be separated into axial and radial parts yielding a similar picture of transport in this system. The main effect of this additional potential is to shift the eigenenergies of the radial Hamiltonian, modifying the subband occupation spectrum. Simulated current for a potential with strong surface band-bending ($A = 0.25$ eV, $b = 9$), and no radial potential ($A = 0$ eV, $b = 0$) are shown in figure 1.1(b).

Variation of the electrostatic potential along the length of the nanowire can lead to effects like scattering, where electrons are reflected back towards their source. To understand this mechanism, the case of a delta function somewhere along the length of the nanowire is considered. This potential is assumed to be radially independent, such that it extends across the entire cross-section of the nanowire. The potential will have the form: $V(l) = g\delta(l - l_1)$, where g is the strength of the barrier, and l_1 is its position along the nanowire length. Since this potential is dependent only on l, the Hamiltonian can still be separated into axial and radial parts. Physically, this means that the potential does not affect the radial states, and only provides a means for the axial states to couple to

one another. Elastic collisions are assumed, such that the energy of the system must be conserved. Therefore, the magnitude of the plane wave's momentum must remain fixed, such that only backscattering can occur. This greatly simplifies the problem as it means we must only consider one dimensional scattering. For potentials with both a radial and axial dependence, the potential can also couple different radial states together leading to interband scattering. To find the transmission through a potential barrier, the transfer matrix is calculated. This matrix acts on the left and right propagating states on the left side of the potential to give the magnitude of the states on the right side of the potential. For a delta function in one dimension this is found to be:

$$M_{b1}(ka) = \frac{1}{ika}\begin{pmatrix} ika+1 & 1 \\ -1 & ika-1 \end{pmatrix} \tag{1.6}$$

where $a = \hbar^2/mg$ and $k = \sqrt{2mE/\hbar^2}$. Given the transfer matrix, the transmission probability is: $T = 1 - |M_{12}/M_{22}|^2$. For a delta function potential this transmission probability is: $T = (ka)^2/(1+(ka)^2)$. This can be directly substituted for $D(E)$ in equation 1.5 since k explicitly depends on the energy. Simulated current as a function of energy for a single subband through a delta function potential is shown in figure 1.2(a). Simulated current through an InAs nanowire with a single delta function potential is shown in figure 1.2(b). The arrows indicate each time a new subband becomes filled. The step for each subband has become significantly rounded by the transmission through the tunnel barrier.

For a more interesting example, a second delta function barrier is added in series with the first barrier. This barrier is located at l_2, and has the potential: $V(l) = g\delta(l - l_2)$. The distance between the two barriers is defined as: $l_{12} = l_2 - l_1$. The total transfer matrix for this system is now the product of three transfer matricies corresponding to transmission through barrier 1 (M_{b1}), propagation through free space over length l_{12} (M_{fs}), and then transmission through barrier 2 (M_{b2}): $M_t = M_{b2} \cdot M_{fs} \cdot M_{b1}$. The transfer matrix for a barrier is already given above, thus the transfer matrix through free space is all that is needed to complete the calculation. The transfer matrix for free space is:

$$M_{fs}(kl_{12}) = \begin{pmatrix} e^{ikl_{12}} & 0 \\ 0 & e^{-ikl_{12}} \end{pmatrix} \tag{1.7}$$

Solving for transmission through the total system and reevaluating equation 1.5 gives current through the two barriers. Figure 1.3(a) shows current for a single subband, which shows markedly different behavior than what was seen for a single barrier. Here, the conductance shows an array of peaks with amplitudes approaching G_0. Each of these peaks corresponds to a discrete energy level formed between the two barriers, due to confinement of electrons in the axial direction. For the limit of $g \to \infty$ the energy of these

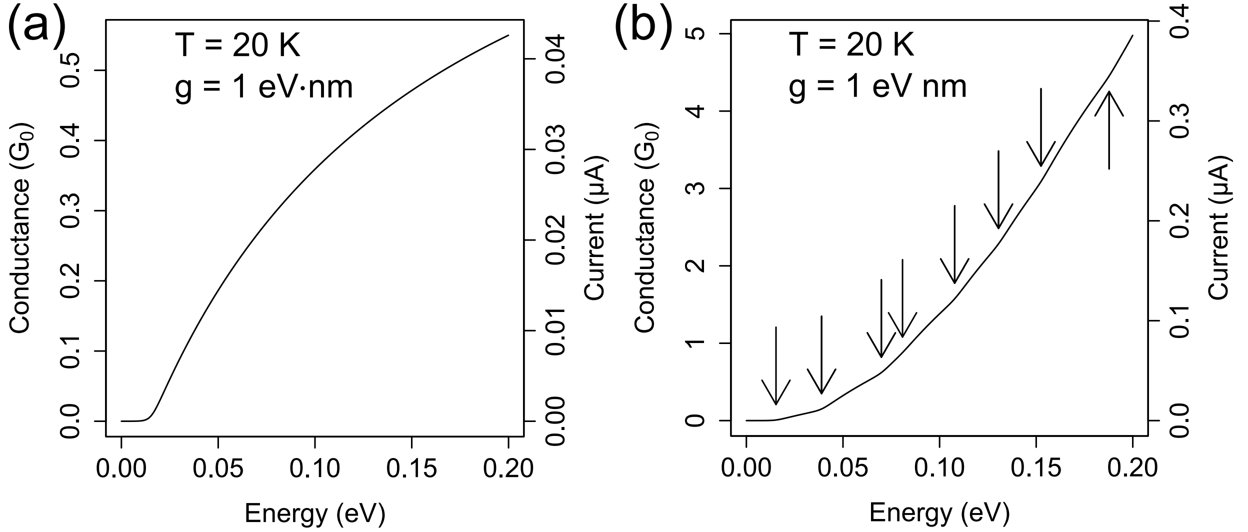

Figure 1.2: (a) Simulated current as a function of energy, at 20 K, for a single subband through a single delta function potential barrier with $g = 1$ eV nm, and a bias of 1 mV. The current through the barrier increases as the energy increases, and approaches G_0V for large energy. (b) Simulated current through a nanowire with no surface band-bending at 20 K. Arrows indicate the energy of each radial subband. The energy of the barrier is large compared to the separation of the subbands causing each step to become rounded.

states approaches $E = (\hbar n\pi)^2/2ml_{12}^2$. The region of space where the electron is confined in all three directions is called a quantum dot, and is characterized by a fully discretized energy spectrum. In this case electron-electron interactions are neglected such that the energy level spectrum is dictated solely by the orbital energies of the dot. Interestingly, the transmission through these energy levels at low energy is higher than that of the single barrier. This is due to resonant tunneling through the discrete set of energy levels created between the two barriers.

1.3.2 Quantum dot transport

A quantum dot is a region of space confined in all three spatial directions. As was shown above, this geometry can be achieved by adding two barriers in series along the length of a nanowire. Several methods can be used to realize these barriers including: inclusion of different bandgap materials during growth, etching to constrict the nanowires, and electrostatic gating. In this thesis the barriers are formed using electrostatic gating, due

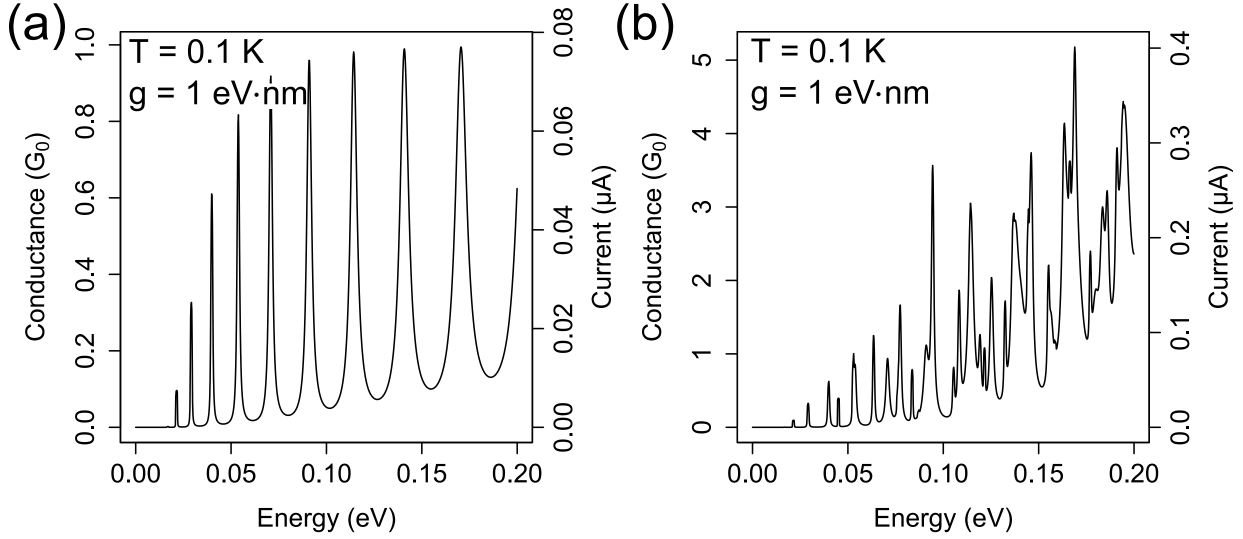

Figure 1.3: (a) Simulated current as a function of energy, at 1 K, through two delta function potentials each with $g = 1$ eV nm, and bias of 1 mV. The current shows sharp peaks due to resonant tunneling through discrete energy levels formed between the two barriers. At each peak the current is higher than the current seen through a single barrier at the same energy despite both systems having the same g value.(b) Simulation of current in a nanowire with the same double delta function potential as (a). The mixture of the radial energy spectrum and the discrete energy levels between the barriers still leads to peaks in current, but the spacing between peaks is more complicated.

to the increased tunability of the barriers, but the transport through any implementation would behave similarly. For the discussion of quantum dot transport we will focus on a simpler model of a quantum dot connected to semi-infinite leads. This way the physics of the dot is decoupled from other transport effects making them easier to understand, and the discussion is generalized such that they apply to other quantum dot systems such as those defined in 2D materials.

Since an electron in a dot is confined in all three spatial directions, the orbital energy spectrum of the electron is a set of discrete energy levels, whose spacing is dictated by the dimensions of the dot. These energy levels are the solutions to the familiar "electron in a 3D box problem" studied in undergraduate quantum mechanics courses and take the form:

$$E_{orb} = \frac{\hbar^2\pi^2}{2m^*}(\frac{n_x}{L_x} + \frac{n_y}{L_y} + \frac{n_z}{L_z})^2. \tag{1.8}$$

where, m^* is the electron effective mass, $n_{x,y,z}$ are the quantum numbers for each spatial

directions, and $L_{x,y,z}$ are the lengths of each side of the box. In addition to these orbital energies there is a Coulomb repulsion energy, which also effects how electrons are added to a quantum dot. This energy is due to the Coulomb repulsion between electrons, and creates an energy cost to add more electrons to a dot. This charging energy is determined by the capacitance of the dot through: $E_C = e^2/C$, where C is the dot capacitance. In many experimental quantum dots the Coulomb repulsion energy tends to dominate over the orbital energy, particularly when many electrons are present on the dot.

To calculate the current through the quantum dot, equation 1.5 is used by changing $D(E)$ to reflect the discrete energy spectrum of a quantum dot.

$$D(E) = \sum_N \gamma_0 h \delta(\mu(N)) \tag{1.9}$$

where the sum is over the N discrete states $\mu(N)$ in the quantum dot, $\delta(\mu(N))$ is a delta function centered at $\mu(N)$, and γ_0 is the total tunneling rate through the dot. The tunnel rate can be written in terms of the tunneling rates through the left and right barriers as: $\gamma_0 = \gamma_L\gamma_R/(\gamma_L + \gamma_R)$. For this form of $D(E)$, it is assumed that the tunnel rate is constant for each energy level. The factor of two at the beginning of equation 1.5 is also dropped since spin degeneracy in the quantum dot is broken by the Pauli exclusion principle. Current through the dot is thus given by:

$$I = e\gamma_0 \sum_N f(\mu(N) - \mu_L) - f(\mu(N) - \mu_R) \tag{1.10}$$

At this point the model for current through a quantum dot has two parameters that can be controlled in an experiment: the bias voltage V_b, and the temperature T. As a function of V_b the current through the dot is characterized by a series of steps in current as new energy levels enter the bias window. Simulated current for this case in shown in figure 1.4, along with an energy level diagram of the dot. A nice addition to this model would be a way to control the energy levels of the quantum dot relative to the bias, such that the number of electrons on the dot could be controlled. This is achieved experimentally by placing an electrostatic gate near the dot, which capacitively couples to the energy levels providing a means of tuning the electron number. Theoretically the gate voltage can be understood by looking at the chemical potential of the dot in the constant interaction model [14]:

$$\mu(N) = U(N) - U(N-1) = E_N + \frac{(N - N_0 - 1/2)e^2}{C} - \frac{eC_gV_g}{C} \tag{1.11}$$

where N is the number of electrons in the dot, E_N is the orbital energy of the Nth electron, V_g is the gate voltage, C_g is the gate capacitance, and N_0 is the number of electrons in the

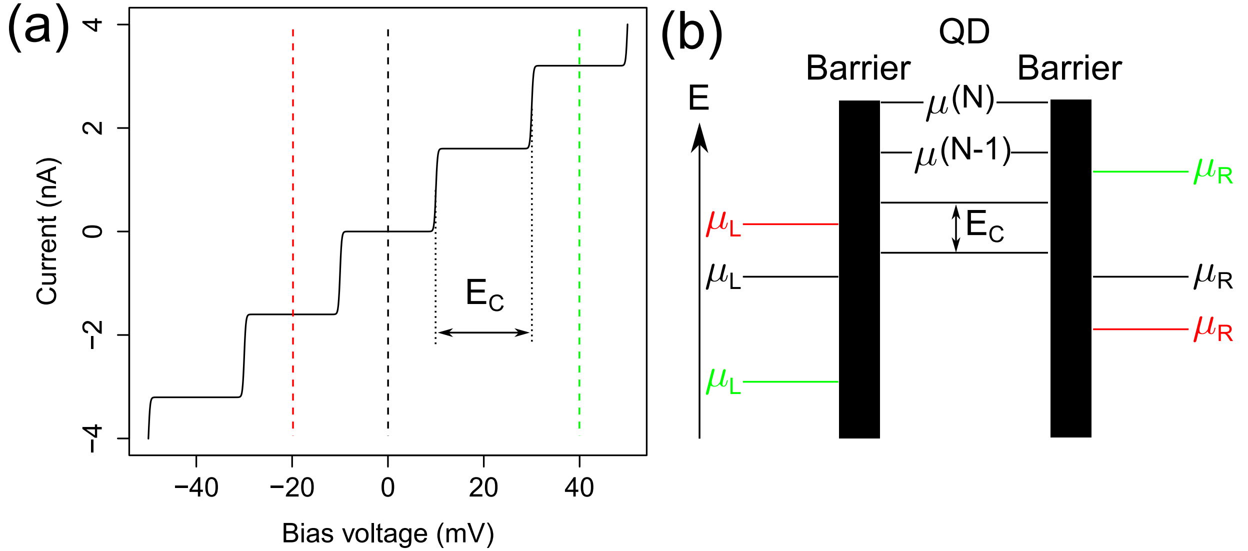

Figure 1.4: (a) Simulated current through a quantum dot as a function of bias voltage at 1 K. The charging energy of this dot is set to $E_C = 10$ meV, and the tunnel rate is $\gamma_0 = 1$ GHz. At zero bias no states fall in the bias window so zero current is observed. As bias is increased above E_C a state will fall in the bias window giving finite current. (b) Energy level diagram of the quantum dot shown in (a). The bias applied to the device sets the chemical potential of each lead. Three different biases are shown in different colors, corresponding to the dashed vertical lines in (a).

dot when $V_g = 0$. The chemical potential of the quantum dot is more useful than the bare energy of the states, since the dot is referenced to leads with chemical potentials μ_L/μ_R. The energy difference between two chemical potentials can also be calculated:

$$\mu(N+1) - \mu(N) = E_{N+1} - E_N + e^2/C \tag{1.12}$$

and gives the difference in orbital energy plus the charging energy as expected. In the case of $e^2/C \gg E_{N+1} - E_N$ the separation between subsequent chemical potentials would be equal and be given solely by the charging energy.

The addition of the gate voltage in equation 1.11 provides a means to change the energy level of the dots relative to the chemical potential of the leads. If gate voltage is swept when a small finite bias is applied to the quantum dot a series of peaks are observed in the current each time a different energy level passes through the bias window. A plot showing simulated current as a function of V_g is shown in figure 1.5(a). In between these current peaks are regions of very low current caused by the Coulomb repulsion. Each low current

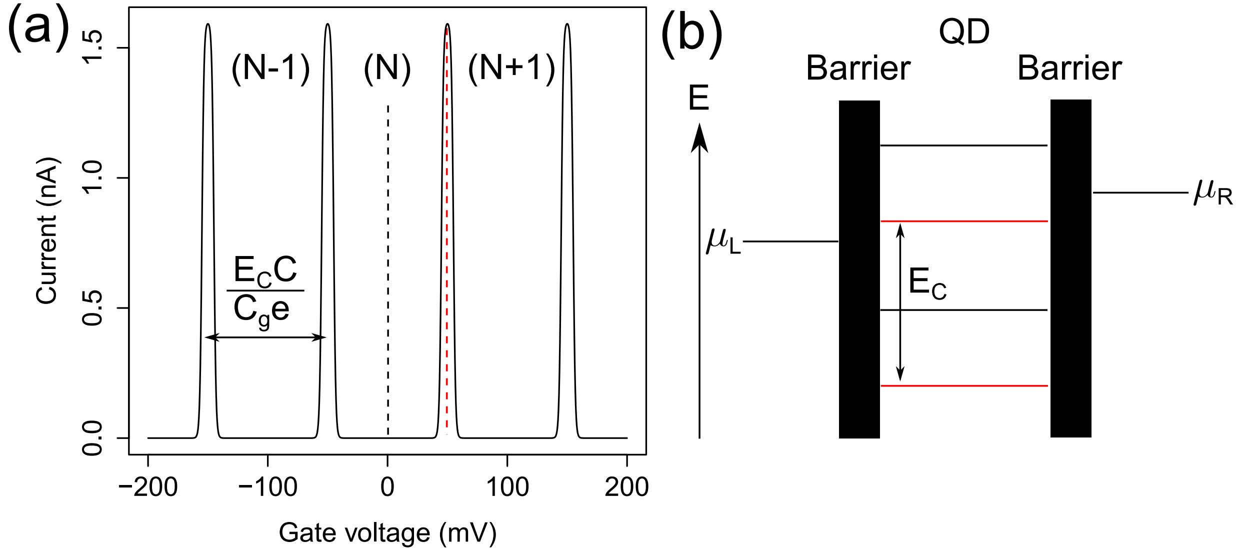

Figure 1.5: (a) Simulated current through a quantum dot as a function of gate voltage at 1 K, with $V_b = 1$ mV. The charging energy of the dot is $E_C = 10$ meV, the tunnel rate is $\gamma_0 = 1$ GHz, and the gate capacitance is $0.1C$. Peaks occur when the chemical potential of the dot falls in the bias window. The low current regions in between each peak correspond to a fixed charge on the dot, as indicated by the numbers in parentheses. (b) Energy level diagram of the dot shown in (a). The two colors of lines in the middle show the chemical potentials in the dot at different gate voltages, corresponding to the vertical dashed lines in (a). At the gate voltage giving the black states no level falls in the bias window giving suppressed current. When the voltage is increased to the point shown by the red lines a state is present in the dot to allow transport between the leads.

region corresponds to a fixed charge on the dot, and is commonly referred to as Coulomb blockade due to this repulsion effect.

Current through the dot can now be calculated as a function of both V_b and V_g. Similar to V_g, it is found that blockade extends over a small portion of V_b, leading to diamond shaped regions of blockaded current. These Coulomb diamonds are shown in figure 1.6. The horizontal and vertical dimensions of each diamond are determined by C and C_g. The annotations in figure 1.6(a) show how these capacitances relate to the dimensions. The slope of the edges of the diamonds is dictated by the capacitance between the dot and each of the leads. These capacitances $C_{L,R}$ for the left and right leads respectively are part of the total capacitance of the dot $C = C_g + C_L + C_R$. If $C_L = C_R$ the slopes are symmetric, and the bias applied to the device drops equally across both tunnel barriers, see figure

1.6(b). As one of these capacitances grows relative to the other it means that more of the bias is being dropped on one side of the dot, as shown in figure 1.6(d). This changes how the energy levels in the dot fall in the bias window, altering the Coulomb diamond pattern. The annotations in figure 1.6(c) show how these capacitances are analytically related to each slope. The number of electrons on the quantum dot can be estimated by identifying the zero electron state, where current is no longer observed through the dot, and then counting the number of Coulomb diamonds from that point.

1.3.3 Double quantum dot transport

Transport through a single quantum dot is now extended to the case of two quantum dots in series. This situation can be pictured as two discrete sets of energy levels in series between two thermally populated reservoirs. When a finite bias is applied across the two dots, current can flow when an energy level from each dot is in the bias window, and the energy levels are positioned such that electrons can flow from high to low energy. An energy level diagram of two dots in various energy configurations is shown in figure 1.7. A metallic gate is placed next to each dot to control its chemical potential, identical to the single dot case.

Current through the double dot could be found using a similar formalism as that of the single dot. Therefore, the focus of this section is the electrostatics of the two dots to show how the charge states of the two dots are modulated, and where unblockaded current can be expected. As a starting point it is assumed that there is no coupling between the two dots, such that the charge state and gate of one dot do not affect the chemical potential of the other dot. This means that each gate can act independently to change the charge state of its dot. These couplings are controlled by a gate capacitance $C_{g1,g2}$ for each gate respectively. For very small bias, current will only be non-zero when a charge state in both dots is aligned with the leads. Current as a function of both gates is then a square array of points, as shown in figure 1.8(a). The dashed lines in figure 1.8(a) indicate the areas of fixed charge on both dots. This type of plot is commonly called a stability diagram since it shows stable regions of charge for each gate. Notice how as a function of one gate, equally spaced regions of fixed charge are observed in each dot, analogous to the situation of transport through a single dot shown in figure1.5(a).

When a capacitive coupling between the two dots is turned on, the number of charges on one dot will affect the chemical potential of the other dot. In this case, the points of non-zero current in the stability diagram split into two points, and the regions fixed charge become skewed into hexagonal shaped regions. The two current points are known as triple

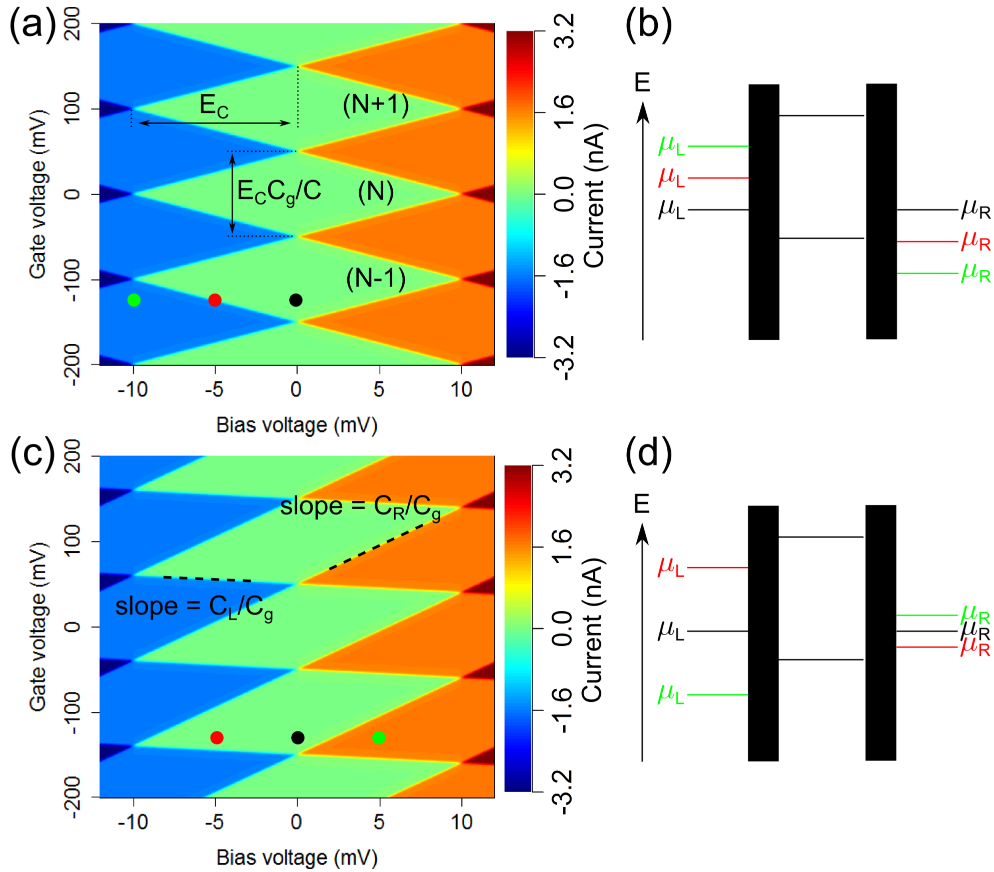

Figure 1.6: (a,c) Current as a function of bias voltage and gate voltage showing Coulomb diamond structure characteristic of transport through a quantum dot. The green diamonds of zero current contain a fixed number of charges on the dot indicated by the numbers in parentheses. (a) The capacitance between the dot and the two leads is equal giving diamonds symmetric about zero bias. (c) The capacitance to the left lead is 9 times larger than that of the right lead, giving skewed diamonds. The slopes of the edges of the diamond are shown next to each black dashed line. (b,d) energy level diagrams for the two dots shown in (a,c). The three different colored chemical potentials correspond to the points in the Coulomb diamond marked by the colored circles in (a,c). (b) The symmetric lead capacitances cause the chemical potentials of the leads to move equally on each side of the dot. (d) The capacitance to the left lead is larger, causing it to move more than the right, and giving asymmetric bias current.

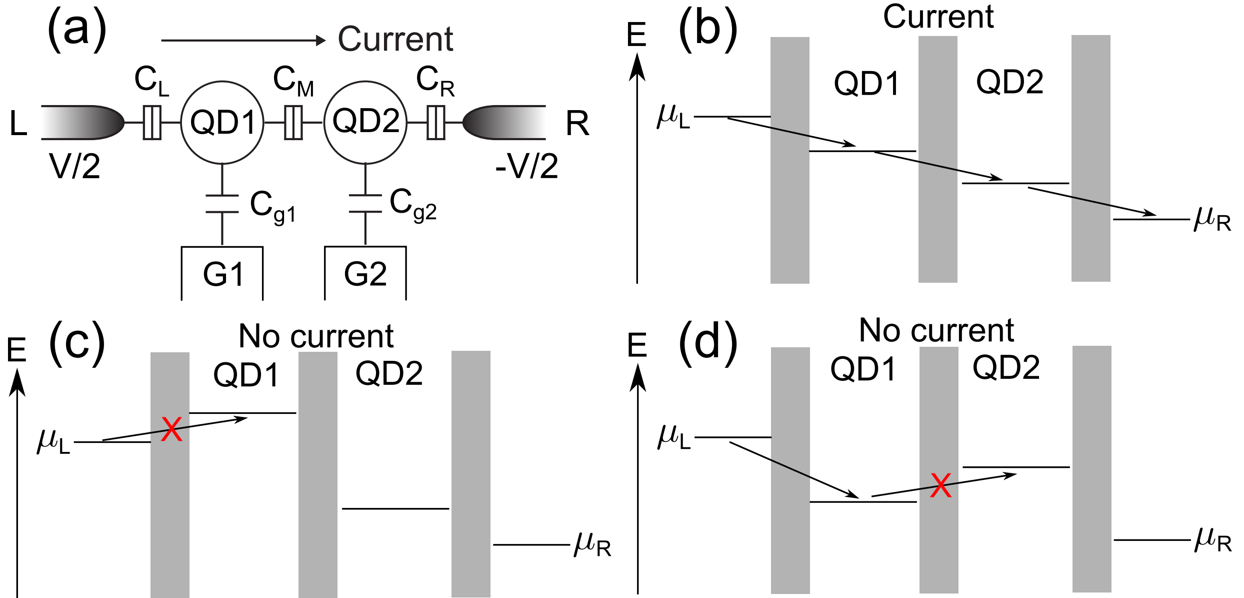

Figure 1.7: (a) Schematic of a double quantum dot between two leads. In this model, the tunnel barrier between each dot and its adjacent lead is represented by a resistor and capacitor in parallel. Only the value of the capacitance of each barrier is shown in the schematic. Each dot is also capacitively coupled to an electrostatic gate. (b-d) Energy level diagram of a double quantum dot in various charge configurations. (b) The chemical potentials of both dots are within the bias window, and positioned to allow electrons to tunnel from one to the other giving current through the double dot. (c,d) Two charge configurations where transport through the dot is blocked giving no current. The red x's show the charge transition which is not allowed.

points, with each point corresponding to a different ordering of the electrons entering and exiting the two dots. Despite the regions of fixed charge becoming skewed, the location of the triple points still falls on a square array as shown in figure 1.8(b). If the interdot capacitance C_m is increased far enough the two dots effectively merge into a single dot leading to a stability diagram with parallel diagonal lines, see figure 1.8(c). Each of these lines of finite current are the Coulomb blockade peaks of the single dot.

In real systems the chemical potential of a dot can also be affected by the gate of the other dot, i.e. there is some coupling between dot 1 and gate 2. This cross capacitance $C_{x1,x2}$ can also be included in the electrostatic model and causes a shift between the location of adjacent triple dots. Therefore the points no longer fall on a square array, a stability diagram with non-zero cross capacitance and interdot capacitance is shown in figure 1.9(a).

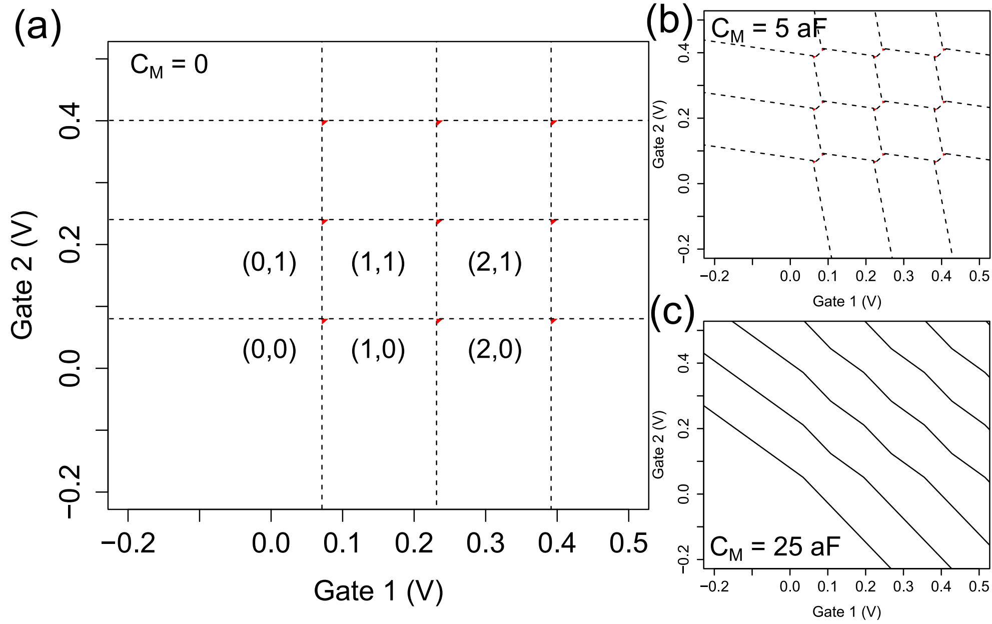

Figure 1.8: Double quantum dot stability diagrams as a function of the two gate voltages with different interdot capacitance C_M. Dashed lines show regions of fixed charge on the two dots indicated by the numbers in parentheses. Current flow through the two dots is shown by the red points where two or more lines intersect. (a) For $C_M = 0$ the stability diagram is an array of squares, where changing a gate voltage changes the number of electrons on that dot without affecting the charge of the other dot. (b) At intermediate C_M the two dots are coupled giving a honeycomb structure to the stability diagram. The single points of current at the verticies in (a) have now split into two triple points. (c) When C_M is further increased the stability diagram begins to look like a set of diagonal parallel lines indicating that the two dots have merged into one larger dot.

Up until now the case of small bias has been assumed in the double dot system, such that unblockaded current is only observed at the triple points. When a finite bias is applied, each triple point grows into a triangularly shaped region of non-zero current typically called a bias triangle. A stability diagram with non-zero bias is shown in figure 1.9(b). The size of each triangle grows linearly with the applied bias, and change direction if the sign of the bias is flipped. Figure 1.10 shows two bias triangle as well as schematics of the double dot energy levels to show how the positions of these levels determine the extents of the bias triangles. In short, each vertex of the triangle corresponds to a different combination of the energy levels being aligned to the left and right leads. The shape of each bias

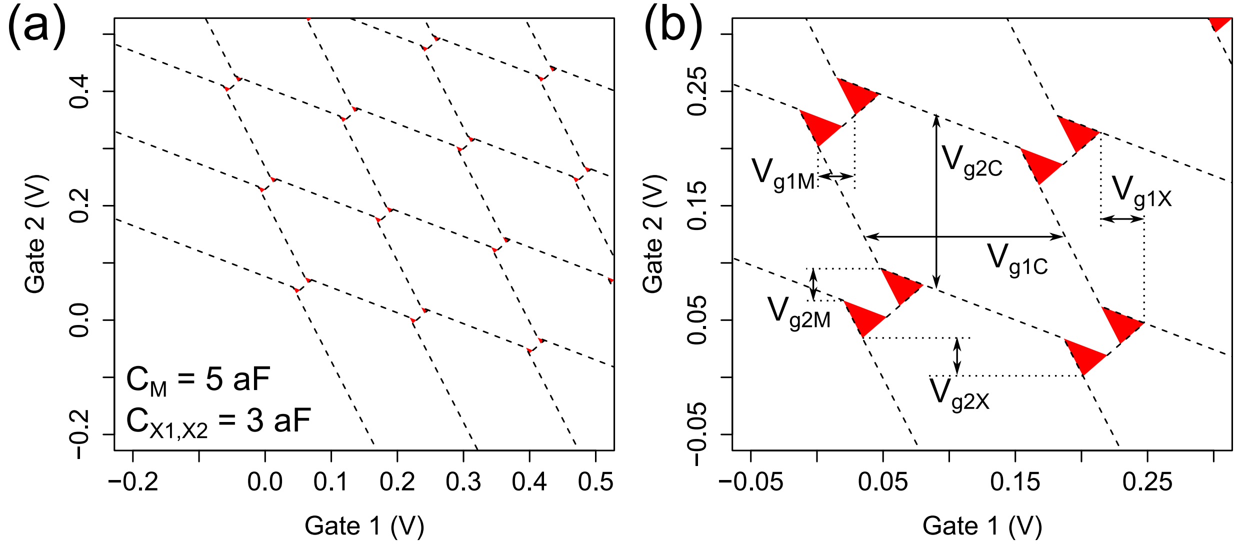

Figure 1.9: Stability diagram for a double quantum dot with finite cross capacitance between the gates and dots. The main effect of this cross capacitance on the stability diagram is to skew the location of each pair of triple points relative to the other pairs. (a) Large area of the stability diagram showing the skewed behavior. (b) Zoom-in of a smaller portion of a stability diagram with 10 mV of bias showing bias triangle of non-zero current. Annotations label the critical dimensions of this stability diagram that can be used to extract the capacitances.

triangle is thus determined by the coupling between the gates and the chemical potentials of each dot, which is explained in the previous paragraphs. The analytic equation for each of these couplings is given in reference [15]. The dimensions of the stability diagram labeled in figures 1.9,1.10 can thus be related to the various capacitances. The following equations relate the two set of parameters together, and can be extracted from the chemical potentials by choosing specific values for the number of electrons in each dot and solving for the corresponding changes in gate voltage.

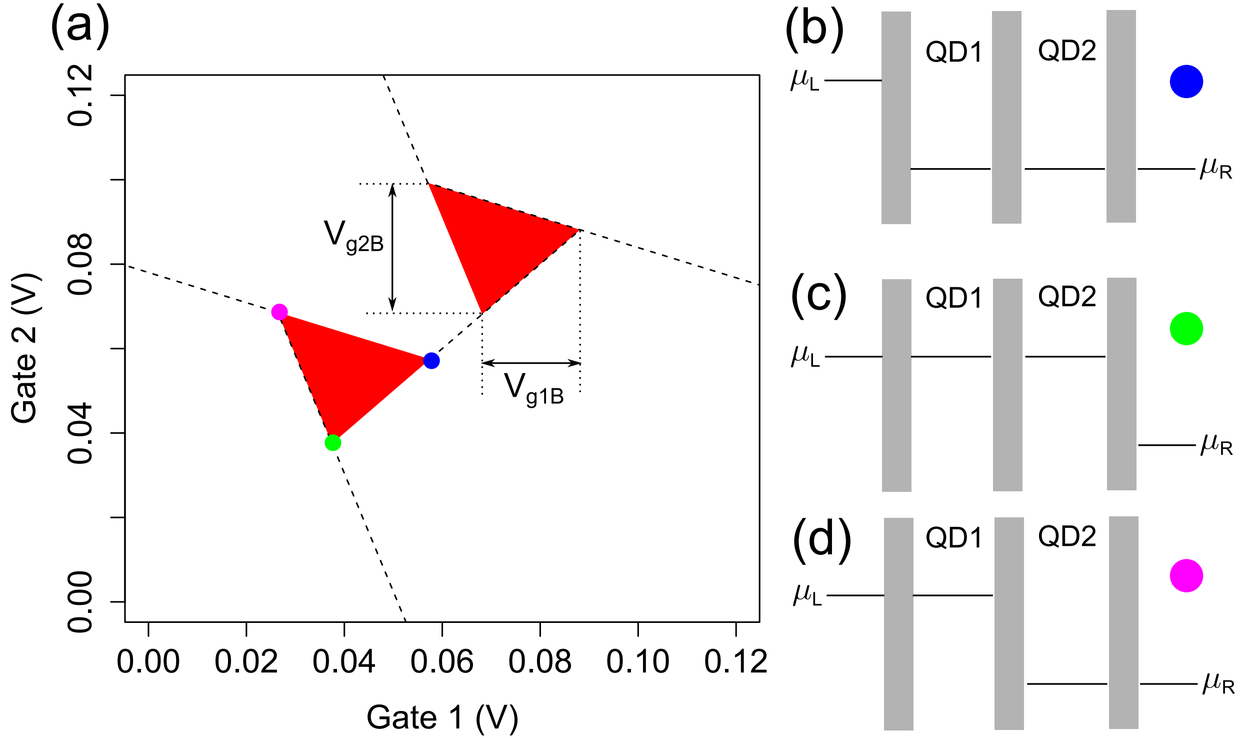

Figure 1.10: (a) Triple points of a double dot at finite bias showing bias triangles. The labeled dimensions of the triangles will be used to extract the capacitances of the double dots. (b-d) Energy level diagram of a double dot at finite bias showing the positions of the chemical potentials of each dot at the verticies of the bias triangles. The colored circles correspond to the circles in (a) and show which diagram matches to which vertex.

$$V_{g1(2)C} = eC_{1(2)}/C_{T1(2)} \tag{1.13}$$
$$V_{g1(2)M} = eC_M/C_{T1(2)} \tag{1.14}$$
$$V_{g1(2)B} = V_b(C_1C_2 - C_M^2)/C_{T1(2)} \tag{1.15}$$
$$V_{g1(2)X} = eC_{g1(2)X}/C_U \tag{1.16}$$
$$C_{T1(2)} = C_{g1(2)}C_{2(1)} + C_{g2(1)X}C_M \tag{1.17}$$
$$C_U = C_{g1X}C_{g2X} - C_{g1}C_{g2} \tag{1.18}$$

In addition to the electrostatics of the system, the electrons' spin can also effect transport through a double dot [2, 3]. If the second dot is filled with a single electron, transport

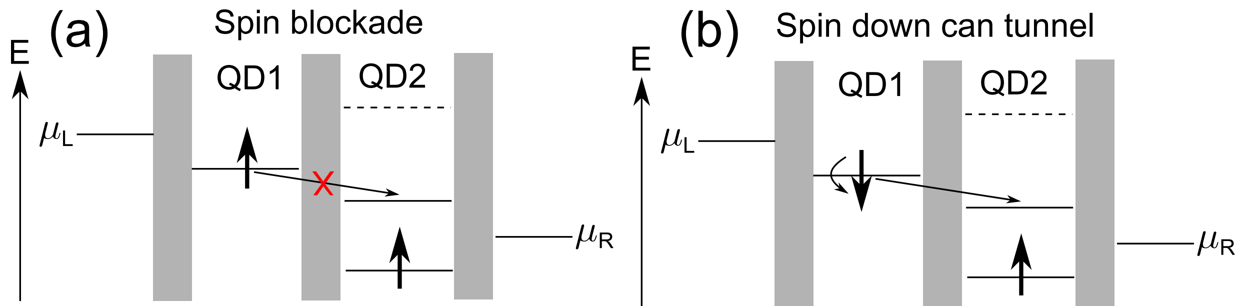

Figure 1.11: Energy level diagram of a double quantum dot including the effects of electron spin. The spin up electron in the right dot is fixed, since this state sits below the bias window. (a) The spin up electron in the left dot is unable to tunnel into the second quantum dot due to the Pauli exclusion principle. (b) If the left electron spin can be rotated to the spin down position it can tunnel into the second dot and out of the system giving a brief jump in current. However, another spin up electron is likely to enter the first dot from the left lead returning the system to a blockaded state.

that should be electrostatically allowed can become blockaded due to the Pauli exclusion principle. This prevents electrons from occupying the same state, and adds to the addition energy of the second quantum dot and can block transport. A schematic of this situation referred to as spin blockade is shown in figure 1.11. In this case the electron in the right dot is spin up. Since there is a random distribution of electron spins in the leads there is an equal probability of spin up or spin down electron entering the left dot. If the electron is spin down, then the two electrons have different spin and can both occupy the right dot with no problem. Once the new electron has tunneled to the right dot it can then exit the system. The problem occurs when a spin up electron enters the left dot. The triplet state formed by the two spin up electrons has a much higher energy and prevents the new electron from tunneling from the left to right dot. Since the electron doesn't have anywhere else to tunnel it remains fixed in the left dot, blocking current leading to spin blockade. Interestingly, this provides a simple means of measuring the spin of the left electron, since spin is directly coupled to transport in this system. One could use this a preliminary testbed for spin based quantum information processing by looking at various means of manipulating the electron spin. For example one could prepare the blockade state, and then apply an electromagnetic pulse designed to rotate the left electron's spin. If the pulse is successful a small jump in current would be observed when the now unblockaded electron tunneled to the right dot and out of the system. This spin blockade based measurement scheme is a fundamental building block for other more robust spin readout schemes.

Chapter 2

Temperature-dependent electron mobility in InAs nanowires

Chapter contributions: Devices were fabricated by Yipu Song. Cryogenic measurements and data analysis were performed by Gregory Holloway and Yipu Song. Numerical simulations were carried out by Nupur Gupta.

2.1 Introduction

Semiconductor nanowires grown by the vapour-liquid-solid (VLS) method [16, 17, 18, 19, 20] are the subject of active study, with many potential applications ranging from nanoscale circuits [21] and gas sensors [22] to high-efficiency solar cells [23, 24, 25, 26]. In particular, InAs nanowires form Ohmic contacts easily[27], and can be grown with low structural defect densities [18], giving rise to high electron mobilities [28], though still low compared to high-quality bulk InAs [29]. The quasi-one-dimensional nature of electron transport at low temperatures [30] together with a spin-orbit coupling ~ 40 times larger than GaAs makes InAs an attractive material for the development of spintronic devices such as electron spin qubits in gate-defined quantum dots [31, 32, 33]. Although transport in InAs nanowires is well-studied [34], the detailed role played by surface states and the surface potential [35, 36, 37, 38] with regard to the electron mobility is not well understood.

This chapter focuses on temperature dependent electron mobility measurements on InAs and InAs/$In_{0.8}Al_{0.2}As$ core/shell nanowire field-effect transistors (FETs) that each

show a characteristic temperature dependence across a wide range of nanowire diameters. For pure InAs nanowires, mobility peaks in the range $3,000-20,000$ cm^{2}V^{-1}s^{-1} near 40 K, with a positive slope at lower temperatures and a negative slope at higher temperatures. Conversely, core/shell nanowires show increasing mobility with decreasing temperature. For comparison, mobilities seen in GaAs high electron mobility transistors often exceed 10^6 cm^{2}V^{-1}s^{-1} [39], suggesting that carrier electrons in these nanowires experience numerous scattering events. In both types of nanowires, the temperature dependence at high temperature seems consistent with that of acoustic phonon scattering, but the experimental mobility is 2-3 orders of magnitude lower than expected [40]. A similar argument excludes optical phonon scattering as a dominant mechanism in this temperature range (it might dominate at even higher temperatures). We expect this to remain true even in quasi-one-dimensional systems, where phonon scattering is moderately enhanced due to a larger available phase space for scattering [41]. Furthermore, the experimental results are obtained on nanowires with low stacking fault densities, which we confirm for measured devices by using transmission electron microscopy. This excludes stacking faults from explaining this qualitative temperature dependence of mobility. On the other hand, the nanowire geometry suggests that a surface scattering mechanism should be dominant. Surface states are known to be present at densities $\sim 10^{11} - 10^{12}$ cm^{-2} eV^{-1} and to act as electron donors. We argue that a sufficient density of these positively charged surface states should be more effective at scattering electrons than surface roughness (charge neutral defects), and therefore limit the mobility. Our numerical simulations show that surface charges at the known densities will indeed lead to scattering rates that produce mobilities of the correct order. We find that the decrease in mobility with temperature above ~ 50 K can be explained by an increase in the number of ionized surface states, presumably due to thermal activation. Consistent with this picture, chemical treatment of the nanowire surface is seen to have a strong effect on the temperature-dependent mobility. Surface roughness scattering, on the other hand, should produce a weaker temperature dependence than what we observe [42]. The difference in the temperature dependence of mobility between the bare and core/shell nanowires is attributed to a decrease in the ionized impurity scattering rate due to the expitaxial shell. These results underscore the need for tailored surface passivation techniques [43, 44] to reduce the density of surface scatterers and smooth the local electronic potential, leading to increased carrier mobility and more ideal devices for a wide range of quantum transport, nanoscale circuitry and optoelectronics applications.

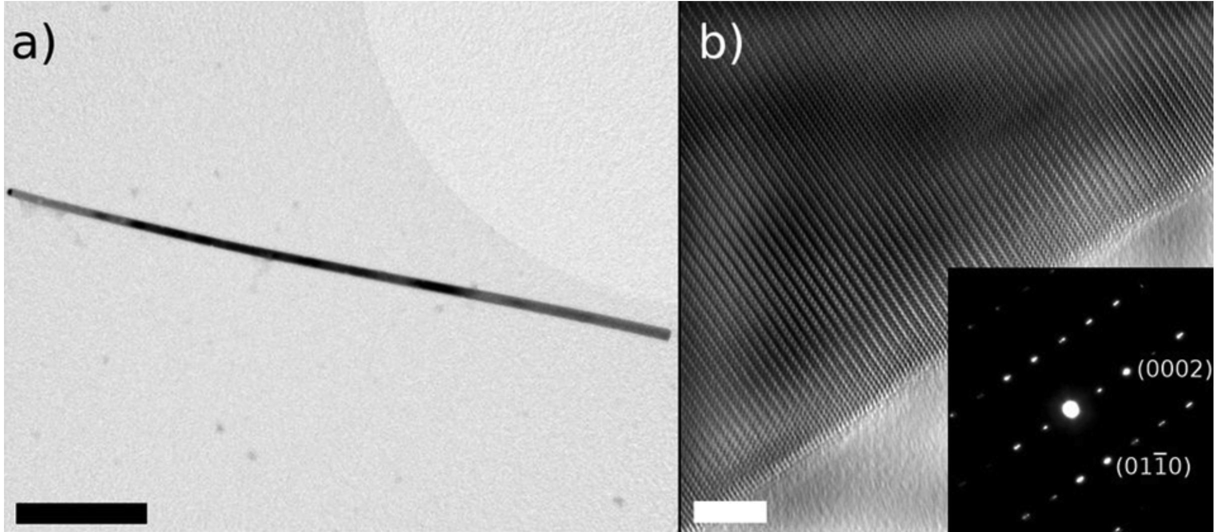

Figure 2.1: (a) Low and (b) high magnification bright-field TEM images of an InAs nanowire grown by GS-MBE at 0.5 μm/hr. Scale bars are 500 nm in (a) and 5 nm in (b). The inset in (b) shows selected area diffraction pattern along the $[2\bar{1}\bar{1}0]$ zone axis indicating pure wurtzite crystal structure. A majority of wires grown under these conditions had low stacking fault densities $< 1\ \mu\text{m}^{-1}$.

2.2 Nanowire growth by gas-source MBE

InAs nanowires were grown in a gas source molecular beam epitaxy (GS-MBE) system using Au seed particles.[1] A 1 nm Au film is heated to form nanoparticles on a GaAs (111)B substrate. For nanowire growth, In atoms were supplied as monomers from an effusion cell, and As_2 dimers were supplied from an AsH_3 gas cracker operating at 950°C. Nanowire growth proceeded at a substrate temperature of 420°C, an In impingement rate of 0.5 μm/hr, and a V/III flux ratio of 4. The nanowires grew in random orientations with respect to the GaAs (111)B substrate, possibly due to the large lattice mismatch strain between InAs and GaAs. Transmission electron microscopy (TEM) analysis, shown in 2.1a, indicated a Au nanoparticle at the end of each nanowire (darker contrast at the left end), consistent with the VLS process [2]. Most nanowires had a rod-shaped morphology

[1]Nanowires are grown by Chris Haapamaki in Ray LaPierre's group at the Centre for Emerging Device Technologies at McMaster University, Hamilton, Ontario, Canada. Technical assistance with the MBE was provided by Sharam Tavakoli

[2]FIB operation and TEM images presented in this chapter were performed by Julia Huang and Fred Pearson at the Canadian Centre for Electron Microscopy, McMaster University, Hamilton, Ontario, Canada

with negligible tapering and a diameter ($\sim 20-80$ nm) that was roughly equal to the Au nanoparticle diameter at the top of each nanowire, indicating minimal sidewall deposition.

For core/shell nanowires, the same parameters were used to grow the InAs core at a substrate temperature of 420°C. While still in the MBE system, a small flux of Al atoms is then turned on to facilitate radial growth of the undoped $In_{0.8}Al_{0.2}As$ shell [44].The nanowires were characterized using transmission electron microscopy (TEM). As-grown nanowires were sonicated and suspended in ethanol, dispersed onto TEM grids with holey carbon films, and imaged with a JEOL 2010F TEM with an accelerating voltage of 200 kV. Low-magnification TEM images of typical nanowires reveal that the nanowires have an inner core and an outer shell structure. In general, the nanowires had a core diameter of 20-50 nm and a shell that was 12-15 nm thick, independent of core diameter. The chemical composition of the nanowires was analyzed by energy-dispersive x-ray spectroscopy (EDS). As shown in figure 2.2(a), the EDS line scan analysis along the radial direction shows In and As in the core region and In, As and Al in the shell region. High-resolution TEM (HRTEM) image of a representative unetched nanowire in figure 2.2(b) clearly shows lattice fringes of a single-crystal nanowire along the $[2\bar{1}\bar{1}0]$ zone axis. Both core and shell exhibit wurtzite crystal structure, evidenced by ABAB... stacking, and confirmed by selected area diffraction. HRTEM and electron diffraction data are both consistent with a dislocation-free core/shell interface for these nanowires. However, at higher Al concentrations, dislocations due to relaxation of the core/shell interface are observed [44].

A common occurrence in III-V nanowires is the existence of stacking faults whereby the crystal structure alternates between zincblende and wurtzite, or exhibits twinning, along the nanowire length. Joyce et al. [19] and Dick et al. [20] have shown that growth parameters in metalorganic chemical vapour deposition (MOCVD) have profound effects on the InAs nanowire crystal phase. Zincblende, wurtzite, or mixed zincblende/wurtzite nanowires were formed by simply tuning the temperature and V/III ratio. We have found that for GS-MBE grown InAs nanowires, stacking faults can be nearly eliminated and pure wurtzite structures can be realized at sufficiently low growth rate $\sim 0.5\mu$m/hr. At higher growth rates, but otherwise identical growth conditions, the InAs nanowires exhibited a much larger fraction of stacking faults on average. For example, TEM analysis of InAs nanowires grown at a rate of 1 μm hr^{-1} exhibited an average linear density of stacking faults ≈ 1 μm^{-1}. Similar to GaAs nanowires [45, 46, 19], the density of faults diminished dramatically when the growth rate was reduced. Selected area electron diffraction for a typical nanowire (inset of figure 2.1(b)) confirms the pure wurtzite crystal structure and the absence of stacking faults.

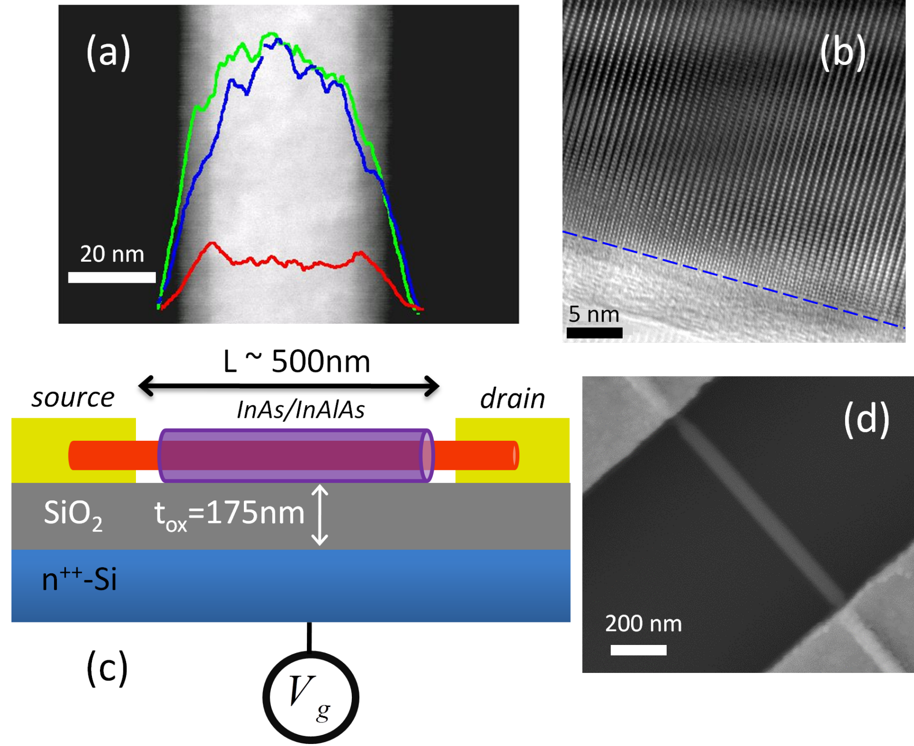

Figure 2.2: (a) High-angle annular dark field image of InAs - $In_{0.8}Al_{0.2}As$ core/shell nanowire with superimposed energy-dispersive x-ray spectroscopy linescan (Al: red, In: blue, As: green). (b) High-resolution TEM image taken along the $[2\bar{1}\bar{1}0]$ zone axis, showing an absence of dislocations in the shell, consistent with previous reports [44]. The dashed line indicates the nanowire surface. (c) Schematic cross-section of the FET device. (d) SEM image of device 3. The etching profile of the nanowire is seen near the metal contact at the upper left.

2.3 Mobility in field-effect transistors

Field-effect transistors (FETs) were fabricated by mechanically depositing as-grown nanowires on a 175 nm thick SiO_2 layer above a n^+-Si substrate that functions as a backgate, and writing source/drain contacts for selected wires using electron-beam lithography (schematic of device layout is shown in figure2.2). This was followed by an ammonium sulfide etching and chemical passivation process to remove the native oxide and prevent regrowth [27] prior to evaporation of Ni/Au contacts. Core/shell nanowires followed a similar procedure,

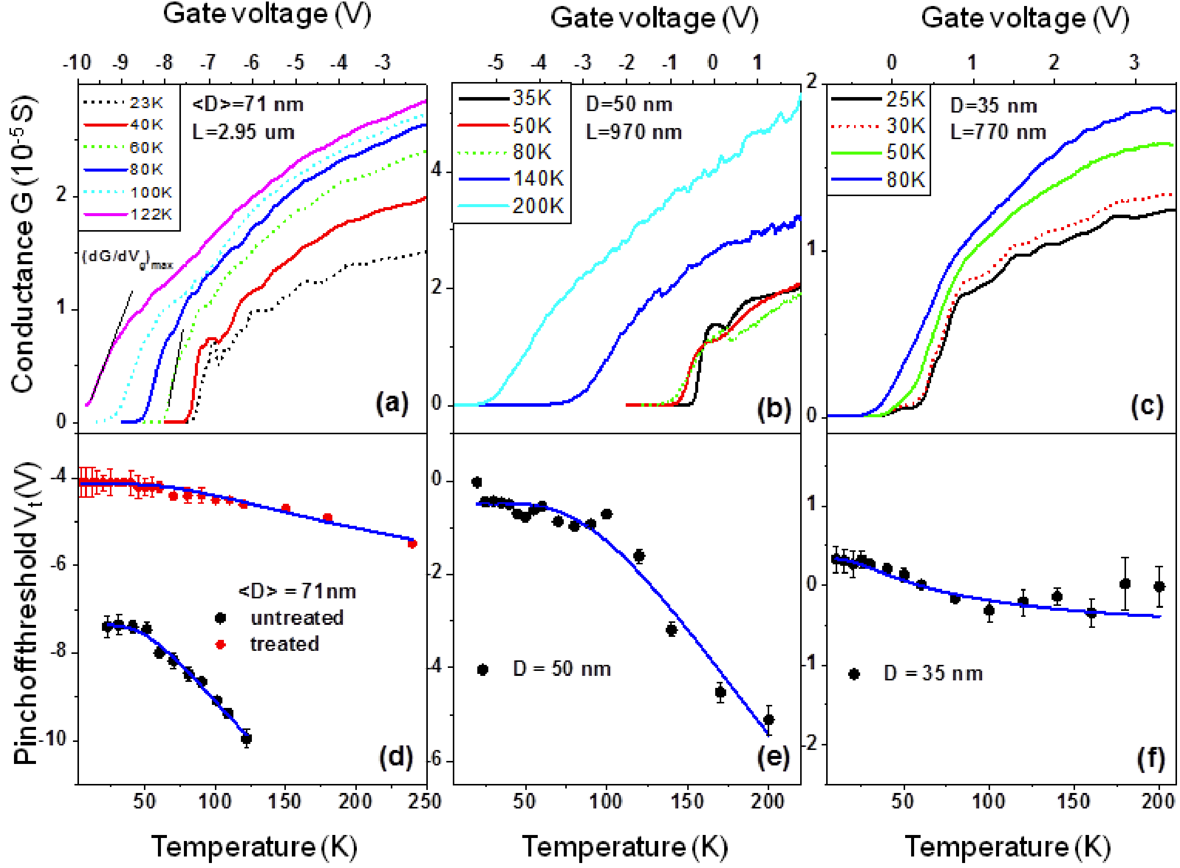

Figure 2.3: (a-c) Conductance versus backgate voltage for devices $1-3$ at selected temperatures. D is the nanowire diameter and L the FET channel length (device 1 is tapered with an average nanowire diameter $\langle D \rangle = 71$ nm). The tangent lines drawn on the $T = 122$ K and $T = 60$ K traces in (a) indicate the maximum slopes corresponding to peak field-effect mobility. The pinchoff threshold voltage is defined as the intercept between this tangent line and the $G = 0$ axis. (d-f) The pinchoff threshold voltages versus temperature extracted from the conductance measurements. In (d), data are shown for device 1 before and after an ammonium sulfide treatment was applied to the FET channel (the data in (a) correspond to the untreated case). The empirical fits in (d-f) are of the form $V_t = V_0 + V_1 e^{-E_a/kT}$, as described in the text.

but with the inclusion of a 10 s etch in citric acid prior to the ammonium sulfide etch to

remove the shell material. FETs made with core/shell nanowires were also annealed at 120 °C for five minutes to promote diffusion of the Ni into the nanowire contact area[47]. Both processes yielded devices with contact resistances that are negligible compared to the channel resistance [27]. Channel lengths ranged from 0.4-3 μm. Transport measurements were carried out in He vapour in an Oxford continuous flow cryostat from 4 K to room temperature. Bias and gate voltages were applied using a high resolution home-built voltage source, and a DL Instruments current preamplifier was used to measure DC current at a noise floor of $\sim$ 0.5 pA/$\sqrt{Hz}$. All devices tested at room temperature displayed fully Ohmic I-V characteristics, with resistances typically in the range of $5 - 200$ kΩ. Gate sweeps were performed at a rate between 3 mV/s (lower temperatures) and 10 mV/s (higher temperatures). Earlier work reported that a sweep rate of 7 mV/s led to very small hysteresis [34]. Under these conditions, we observe a shift with respect to gate voltage of less than 50 mV upon changing sweep direction, and no observable change in the shape of the conductance curve. Note that FET devices with channel lengths greater than $\sim$ 200 nm are known to be in the diffusive transport regime [48].

The gate capacitance per unit length was calculated using the expression [49, 28, 43]

$$C'_g = 2\pi\epsilon_0\epsilon_r/\cosh^{-1}\left(\frac{R+t_{ox}}{R}\right) \tag{2.1}$$

where R is the nanowire radius, ϵ_0 is the electric constant, $\epsilon_r = 3.9$ is the relative dielectric constant and t_{ox} the thickness of the SiO_2 layer, respectively. The equation above assumes that the nanowire is embedded in SiO_2; to compensate for the fact that the nanowire actually sits atop the SiO_2 and is surrounded by vacuum ($\epsilon_r = 1$), it was shown by Wunnicke [49] that a modified dielectric constant $\epsilon'_r = 2.25$ can be taken. Our numerical simulations, comparing the pinchoff threshold voltages of the FET device calculated with and without SiO_2 embedding, confirmed that this is a suitable correction factor. The capacitances based on equation 2.1 are listed in table 2.1.

2.4 Results

2.4.1 Bare InAs nanowires

Here we will focus on three representative devices, denoted 1, 2 and 3 with nanowire diameters $D = 71$, 50 and 35 nm, respectively. The nanowires in devices 2 and 3 were untapered, whereas the nanowire in device 1 was tapered, with diameter linearly varying from 53 nm to 90 nm across the FET channel (average diameter $\langle D \rangle = 71$ nm). Subsequent

device #	Nanowire material	D (nm)	L (μm)	C'_g (aF$\cdot\mu$m^{-1})
1	bare InAs	71	2.95	50.76
2	bare InAs	50	0.97	45.21
3	bare InAs	35	0.77	40.52
4	core/shell	54	0.47	46.34
5	core/shell	49	0.47	44.92
6	core/shell	25	0.94	36.81

Table 2.1: Diameters (D) and channel lengths (L), measured by AFM and TEM, and calculated capacitance per unit length (C'_g) for the six main FET devices investigated. For core/shell nanowires, the core diameter is listed. Uncertainties in diameter are ± 2 nm (for tapered device 1, D is the average diameter).

to transport measurements, the channel of device 1 was subjected to an ammonium sulfide etching and passivation treatment similar to that carried out just before contacting. Its temperature dependent mobility was then remeasured, but likely after the native oxide had partially or fully regrown due to a time delay of several days. TEM analysis was carried out on several devices after transport studies were complete to check for the presence of stacking fault defects. Devices 1 and 3 were found to have zero and one fault, respectively, whereas a fourth device ($D = 55$ nm) with low mobility was found to have an atypically large fault density (see section 2.6 below). TEM analysis was not performed on device 2.

Figure 2.3(a-c) shows conductance $G = I_{sd}/V_{sd}$, where I_{sd} and V_{sd} are the source-drain current and bias, respectively, versus backgate voltage V_g for devices 1, 2 and 3 at selected temperatures. The bias is set to $V_{sd} = 1$ mV (similar results are obtained at higher bias). For all three devices, the maximum transconductance $\left(\frac{dI_{sd}}{dV_g}\right)_{max}$ is seen to decrease as temperature is raised above $\sim 30 - 50$ K. Figures 2.3(d-f) show the pinchoff threshold voltages V_t corresponding to the data in figures 2.3(a-c), where V_t is defined as the intercept between the maximum slope tangent line and the $G = 0$ axis. V_t typically shifts toward more positive gate voltages as temperature decreases, and saturates below ~ 50 K. All temperature sweeps reported here were from low to high temperature. We fit the pinchoff threshold data to an empirical function based on thermal activation $V_t = V_0 + V_1 e^{-E_a/kT}$, where k is the Boltzmann constant, typically yielding an $E_a \sim 5{-}30$ meV. Smaller diameter nanowires typically have smaller E_a, such as device 3 in figure 2.3(f), with $E_a \approx 5$ meV. Note that for device 1 in figure 2.3(d) we also plot the V_t measured after the chemical treatment was applied to the FET channel. V_t shifted considerably to more positive gate voltage post-treatment, and also showed a weaker temperature dependence. This suggests that the surface potential and density of conduction electrons in the nanowire are controlled

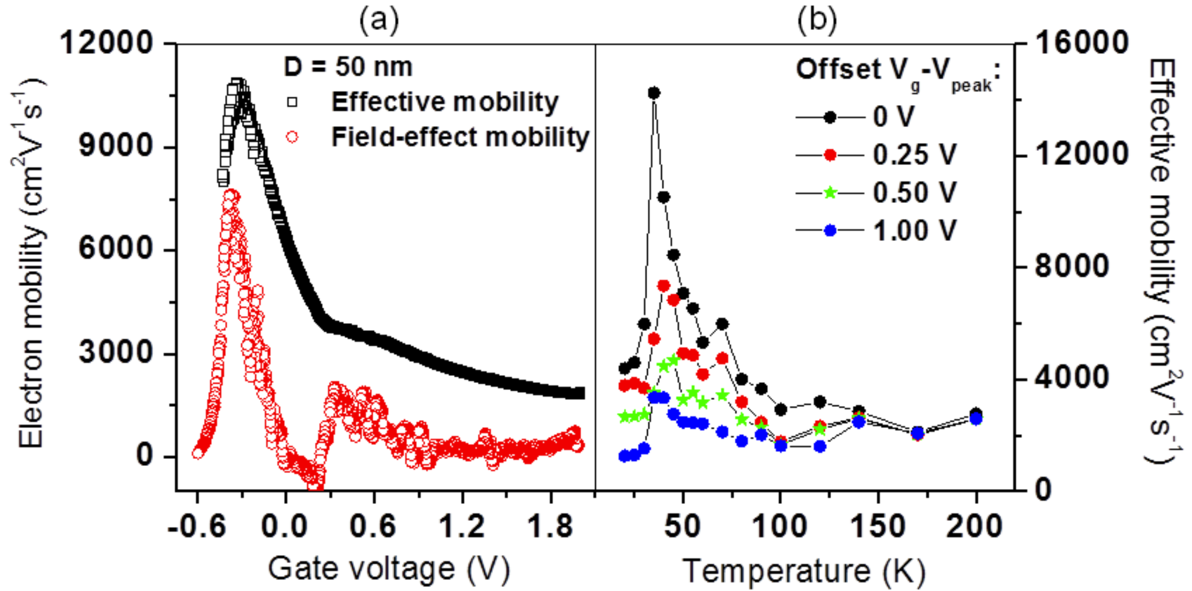

Figure 2.4: (a) Comparison of the field-effect and effective mobilities for device 2 at $T = 40$ K. (b) The temperature dependence of effective mobility for device 2 at different values of gate voltage relative to V_{peak}, the gate voltage at which peak mobility occurs. The values at V_{peak} are shown by black dots, at $V_{peak} + 0.25$ V by red dots, etc. The mobility at $V_{peak} + 0.5$ V (green stars) is near the crossover point between the two slopes seen in the effective mobility in the left panel.

in large part by the surface chemistry [22].

From the measured conductance versus backgate voltage curves, both the field-effect mobility and the effective mobility may be extracted. The field-effect mobility is a lower bound on the effective mobility, and is defined as [28]

$$\mu_{\text{fe}} = q^{-1}\frac{d\sigma}{dn} = \frac{L}{C_g'}\frac{dG}{dV_g}, \tag{2.2}$$

where σ is conductivity, n is the electron concentration, q is electron charge, C_g' is the gate capacitance per unit length and L is the channel length. Equation 2.2 only strictly holds at peak mobility, where $\frac{d\mu_{\text{fe}}}{dn} = 0$. The effective mobility is defined as [28]

$$\mu_{\text{eff}} = \frac{LG}{C_g'(V_g - V_t)}, \tag{2.3}$$

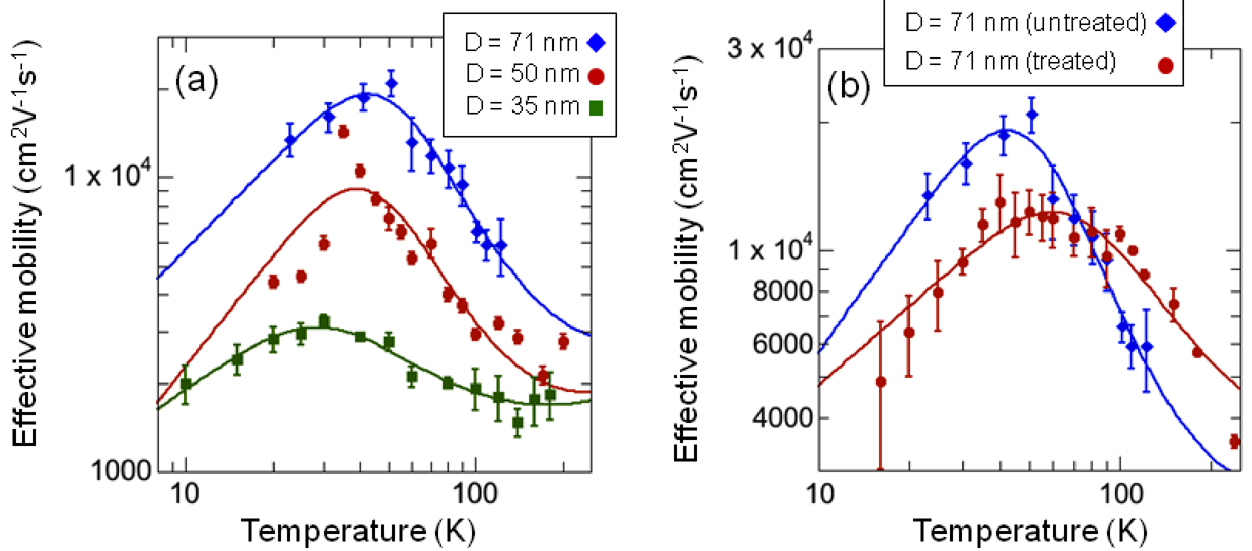

Figure 2.5: (a) Experimental peak effective mobilities versus temperature for devices $1-3$ (diameters 71, 50, and 35 nm, respectively). The empirical fitting function described in the text (solid lines) is given by $\mu = AT^x(1+Be^{-E_a/kT})^{-2}$, where x, A, B and E_a are fitting parameters given in the main text. (b) Comparison of peak effective mobilities versus temperature for device 1 before and after an ammonium sulfide etching and passivation treatment was applied to the FET channel. The fitting function is of the same form. For comparison, the pinchoff threshold voltages before and after treatment are shown in figure 2.3(d).

where V_t is the pinchoff threshold voltage defined previously, and the expression only holds for $V_{sd} << V_g - V_t$. The two measures of mobilities are compared in figure 2.4(a) for device 2 at 40 K. The effective mobility is typically a smoother function of V_g, and $\mu_{\text{eff}} \geq \mu_{\text{fe}}$ for all of our data. Two regimes can be clearly seen in μ_{eff}: the slope $|\frac{d\mu_{\text{eff}}}{dV_g}|$ is larger from $V_g = -0.25V$ to $V_g = +0.25V$ than at more positive gate voltages. In figure 2.4(b) we show the effective mobility versus temperature for device 2 at different values of gate voltage relative to the position of peak effective mobility (V_{peak}). The data shown are for $V_g = V_{peak} + \delta$, where the top curve (black dots) is for $\delta = 0$, and the lower curves (red, green, blue) are for $\delta = 0.25, 0.5, 1.0$ V, respectively. The temperature dependence is most pronounced at peak mobility, but follows a similar trend for points on the high slope region of the effective mobility curve. At large positive gate voltages relative to V_{peak}, the mobil-

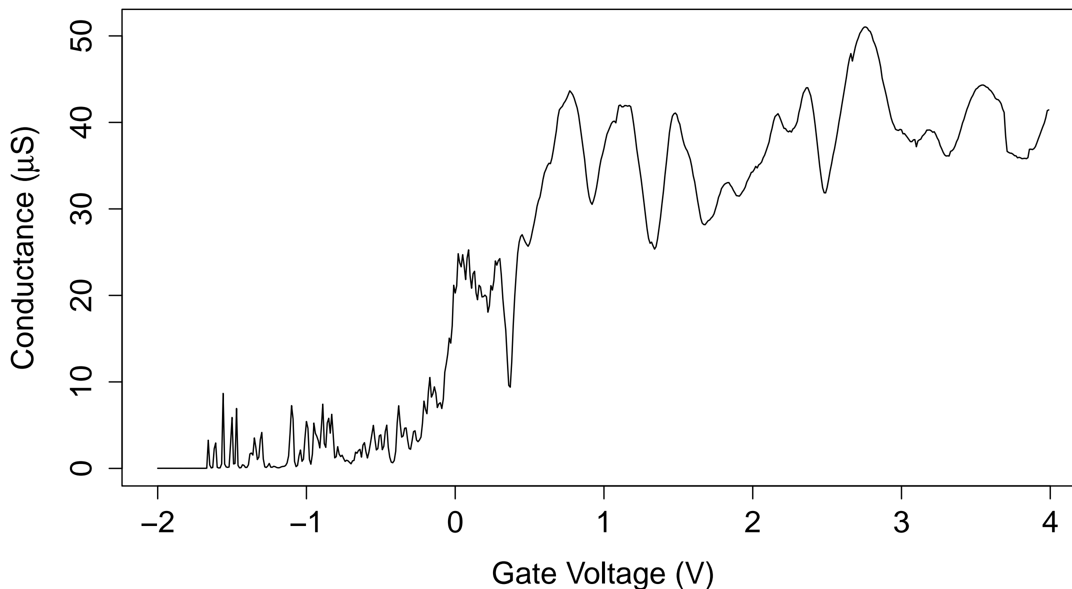

Figure 2.6: Experimental conductance through an InAs nanowire FET with a channel length of 500 nm at 1.4 K. The conductance shows numerous peaks indicating the formation of localized puddles of charge due to potential disorder along the nanowire and electron-electron interactions. The emergence of these peaks makes it difficult to extract an accurate estimate of the mobility at these temperatures.

ity shows little to no dependence on temperature. A possible source of systematic error in mobility is shielding due to Ohmic contacts [50], which can become large for short channel lengths. For our shortest channel length of 770 nm (device 3), the calculated mobility could be overestimated by up to a factor of two in the worst case. A much smaller error should apply to the other devices, in particular, it will be negligible for device 1. This type of error is independent of temperature, and therefore does not affect the qualitative behaviour of mobility. Another concern is the dependence of the measured mobility on the bias voltage. We observe no difference, within statistical error, between mobilities measured at 1 mV and 10 mV bias.

Below 20 K it becomes difficult to properly quantify mobility in these nanowires due to the emergence of Coulomb peaks in the conductance. This is due to the combination

of potential disorder and electron-electron Coulomb interactions which causes the electron density to vary along the nanowire. These variations in the density are analogous to the Coulomb blockade effects discussed in chapter 1, but are due to unintentional potential fluctuations. When these charge localization effects begin to dominate the system, equations 2.2, 2.3 are no longer valid and thus mobility can no longer be accurately extracted from the conductance curve. Figure 2.6 shows an example of experimental data from a bare InAs nanowire at 1.4 K with numerous Coulomb blockade peaks.

Devices 1 and 3 show qualitatively similar behaviour to device 2, as shown in figure 2.5(a). The maximum in mobility at around $T = 50$ K is consistent with previous reports [28, 51]. At a given temperature, the mobility increases with nanowire diameter, as was also reported previously [28]. This is consistent with the mobility being dominated by surface charge scattering, as the overlap of the carrier distribution with the scattering potential becomes much stronger at smaller diameters [52]. Motivated by this hypothesis, the data in figure 2.5 are fit to empirical function of the form $\mu(T) \propto T^x N(T)^{-y}$, where $N(T)$ is the number of surface scatterers. This function does not result from an analytical solution of the surface scattering problem, which is in general too difficult to solve without resorting to numerics [52]. Rather, this function provides a good model for our data and is based on the the following reasoning. For a fixed number of scatterers, the average mobility increases with temperature as T^x, where $x \sim 1$, since the carrier concentration increases with temperature leading to an increase in the Fermi velocity, which reduces the scattering probability [52, 42]. This increase in carrier concentration is also observed experimentally, as seen in figure 2.8 below. On the other hand, an increase in the number of scatterers decreases mobility. In the limit of a low density of scatterers and a high probability of scattering per defect, scattering events can be treated as uncorrelated, and $\mu \propto N^{-1}$ (or equivalently, the scattering rate is proportional to the number of scatterers). However, for scattering from positively charged surface states, there is a high density of scatterers with a low probability of scattering per defect, leading to correlated scattering [53] (see section below). Here, the electron wavefunction remains coherent while interacting with multiple surface charges simultaneously, which leads roughly to $\mu \propto N^{-2}$, since the scattering matrix element is roughly proportional to N, so the transition rate is proportional to N^2. We model $N(T)$ based on the thermal activation of surface donors: $N(T) \propto (1 + Be^{-E_a/kT})$, where B and E_a are free parameters. The fact that similar expressions can be used to model the pinchoff threshold voltages seen in figure 2.3, as well as the carrier concentration in figure 2.8 below, further support our claim that the surface donors are thermally activated.

The data in figure 2.5 are fit to $\mu = AT^x(1 + Be^{-E_a/kT})^{-2}$. For $D = (71, 50, 35)$ nm, the fit parameters (excluding scaling factor A) are the following: $x = (1.0, 1.25, 0.67)$, $B = (13.4, 14.6, 3.0)$, and $E_a = (17.2, 15.1, 8.0)$ meV. We note that the data can be fit

equally well to a functional form $\mu \propto N^{-1}$, albeit with different fit parameters, but we chose the N^{-2} form for consistency with the numerical modeling results in section 2.5. The E_a values suggest thermal ionization of the surface donor states with activation energies in the range $8 - 20$ meV, consistent with the range of E_a values obtained from fitting V_t in figure 2.3. The smaller value of B for the 35 nm diameter nanowire is consistent with the weaker temperature dependence of its pinchoff threshold voltage in figure 2.3(f), indicating a smaller number of thermally activated donor states relative to the larger diameter nanowires. Figure 2.5(b) compares the data for device 1 before and after an ammonium sulfide etching and passivation treatment was applied to the FET channel. The best fit parameters in the latter case are $x = 0.62$, $B = 4.5$, $E_a = 20.2$ meV. After the chemical treatment, the turnover in mobility broadens and shifts to higher temperatures. This is accompanied by a much weaker change in the pinchoff threshold voltage with temperature, shown in figure 2.3(d). The smaller value of fit parameter B after chemical treatment is consistent with the weaker temperature dependence of pinchoff threshold voltage after treatment. We note here that the detailed condition of the nanowire surface post-treatment is not known, and it is likely that the native oxide partially or fully regrew before or during the post-treatment transport measurements. The data are presented only to show that the nanowire transport properties are significantly altered by chemical removal of the oxide followed by unspecified surface chemical processes; these processes evidently incur some change in the nature or density of surface states. The overall reduction in mobility is consistent with previous observations of low mobility in nanowires exposed to wet etching conditions [54, 51].

2.4.2 InAs/$In_{0.8}Al_{0.2}As$ core/shell nanowires

As seen above, changes to the nanowire surface can substantially alter its transport properties. This motivates the study of transport in core/shell nanowires, where the surface of the InAs core is now covered in an epitaxial layer of $In_{0.8}Al_{0.2}As$. Due to the large bandgap of $In_{0.8}Al_{0.2}As$, it is expected that the conduction electrons will remain confined in the core, but will see a different surface potential and structure due to the addition of a shell. In the previous section, it was postulated that scattering from surface states limits mobility in bare InAs nanowires. Therefore, if the mobility behavior of core/shell nanowires is different from that of the bare wires, it would indicate a change in the nature of the scatterers. Figure 2.7 shows the peak effective mobilities of the core/shell InAs/$In_{0.8}Al_{0.2}As$ nanowires across a wide temperature range. The unpassivated devices presented above exhibit a turnover at low temperatures, where mobility rapidly decreases

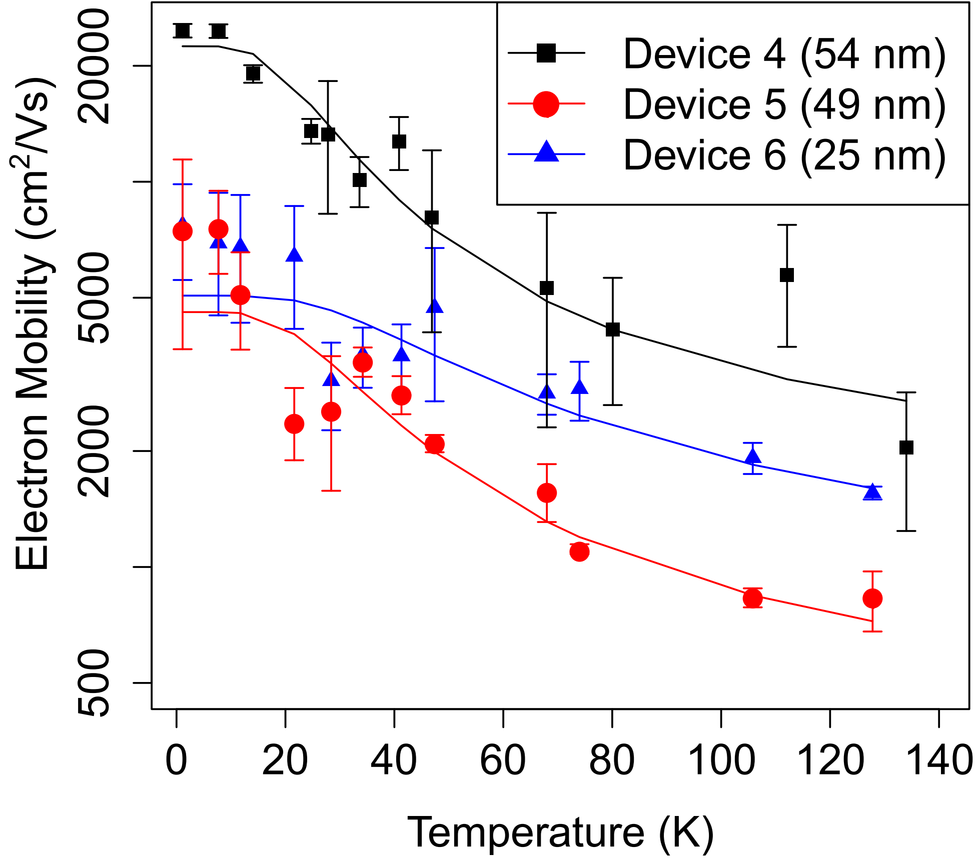

Figure 2.7: (a) Experimental peak effective mobilities versus temperature for devices $4-6$ (diameters 54, 49, and 25 nm, respectively). The fitting function described in the text (solid lines) is given by $\mu = AT^x(1+Be^{-E_a/kT})^{-2}$, where x, A, B and E_a are fitting parameters given in the main text. Unlike the unpassivated nanowires, the core/shell nanowires show mobility that increases with decreasing temperature all the way down to 1 K.

with decreasing temperature. In contrast, the mobilities of the core/shell nanowires increase as temperature is lowered, even down to $T = 1$ K (effective mobility could not be properly measured below 1 K due to the onset of strong Coulomb blockade). We have investigated several more specimens of both nanowire types, and see a similar turnover in mobility only for the unpassivated nanowires. The data in figure 2.7 have been fit to the same equation for mobility as the unpassivated nanowires $\mu = AT^x(1+Be^{-E_a/kT})^{-2}$. With fit parameters $x = (0.01, 0.02, 0.01)$, $B = (3.2, 2.9, 1.8)$, and $E_a = (6.0, 7.0, 9.0)$ meV for devices 4-6 respectively. The values of E_a are close to the lower end of the range

seen for unpassivated nanowires, suggesting that the donors may be of similar origin in the two types of nanowires. However, the lower values of B indicate that the number of thermally activated donor states has been decreased by the epitaxial shell. The diameter dependence of B is also consistent, showing lower values for smaller diameters. The drastic decrease in x reflects the lack of a turnover in mobility at low temperature, indicative of a reduced scattering rate. We note that the highest core/shell nanowire mobility observed was $\approx 25,000$ cm^{2}V^{-1}s^{-1} at 1 K for device 4 (core diameter $\sim$ 54 nm), higher than the peak mobility $\approx 20,000$ cm^{2}V^{-1}s^{-1} at 35 K for the unpassivated device 1 (diameter $\sim$ 70 nm). Mobilities in excess of 20,000 cm^{2}V^{-1}s^{-1} have also been observed with InAs-InP core/shell nanowires [43] at low temperature.

For completeness, we show the estimated carrier electron concentrations at peak mobility for both types of nanowires in figure 2.8. The concentrations are estimated from the ratio of conductivity to effective mobility. The core-shell carrier concentrations are seen to decrease steadily as temperature is lowered, whereas the unpassivated nanowire concentrations show more experimental scatter, but appear to vary less with temperature below 100K. Note that the error bars shown only account for error in the fitting used to extract effective mobility, but there is additional experimental variation in device conductance over the course of measurements due to hysteretic changes in surface state population [55], trapping of electrons in the nanowire oxide [56], etc. The core-shell concentrations fit reasonably well to a simple exponential, $n(T) = Ae^{BT}$, where n is concentration, T is temperature, and A and B are fitting parameters.

2.5 Numerical modeling

We carried out numerical modeling of the nanowire transistor to test whether scattering from charged surface states can account for the magnitude and temperature dependence of the experimental mobilities. The nanowire transistor was simulated using a finite-element method implemented in the COMSOL® multiphysics package. The model consisted of a 1 μm long, 50 nm diameter nanowire atop a 175 nm thick SiO_2 layer with underlying backgate. The layer above the SiO_2 that embeds the nanowire is vacuum, with $\epsilon_r = 1$, and we take $\epsilon_r = 15.15$ for the InAs nanowire. In consideration of the low effective mass of electrons in InAs, we used a self-consistent Poisson-Schrodinger solver [57] to calculate the electrostatic potential and charge distribution in the nanowire so that quantum confinement is properly taken into account. The model assumes that the conduction electron concentration at zero gate voltage is due to a surface density of positively charged donor states, $\sigma_{ss}^{+} \sim 10^{11} - 10^{12}$ cm^{-2}, an input parameter that is allowed to vary with tempera-

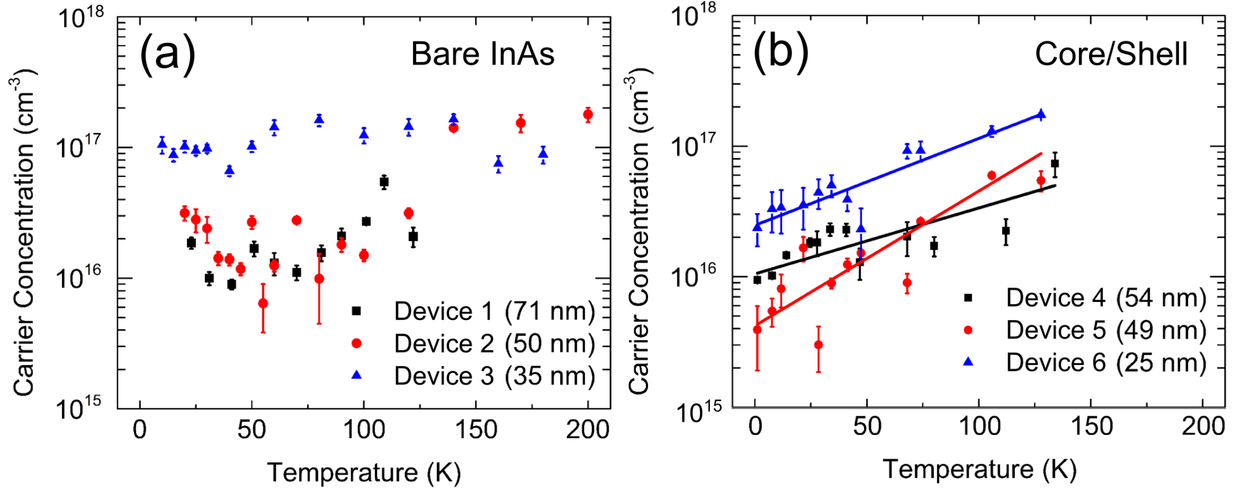

Figure 2.8: Carrier electron concentrations at peak mobility, versus temperature, for bare nanowires (a) and core/shell InAs/$In_{0.8}Al_{0.2}As$ nanowires (b). The estimated nanowire diameters are indicated in the legend. The solid lines in (b) are empirical fits of the form $n(T) = Ae^{BT}$, where n is concentration, T is temperature, and A and B are fitting parameters. The slopes B obtained are 0.012K^{-1},0.024K^{-1}, and 0.015K^{-1} for devices 4, 5, and 6, respectively. The concentrations for the unpassivated nanowires show more scatter, but are largely independent of temperature below 100K.

ture.

Consider a Cartesian coordinate system with z aligned with the nanowire axis and radial coordinates (x, y). The potential $V(x, y, z)$ that is a solution to the Poisson equation is nearly independent of axial coordinate z, so we solve the Schrodinger equation in a two-dimensional cross-section of the nanowire to obtain the radial eigenstates $\psi_i(x, y)$. The electron density in the radial plane, $n_{2d}(x, y)$, is calculated from these solutions as

$$n_{2d}(x,y) = \sum_i n_{2d,i}(x,y) = \sum_i |\psi_i(x,y)|^2 \int_0^\infty f(E-E_i)g(E-E_i)dE \tag{2.4}$$

where $g(E - E_i) = \frac{1}{\pi\hbar}\sqrt{\frac{2m^*}{(E-E_i)}}$ is the one-dimensional (1D) density of states per unit length, $f(E - E_i)$ is the Fermi-Dirac distribution, and E_i and $\psi_i(x, y)$ are the energy and wavefunction of the ith eigenstate, respectively. The summation reduces to

$$n_{2d}(x,y) = \frac{1}{\pi\hbar}\sqrt{2m^* k_B T} \sum_i |\psi_i(x,y)|^2 \times F_{-1/2}\left(\frac{E_F - E_i}{k_B T}\right) \tag{2.5}$$

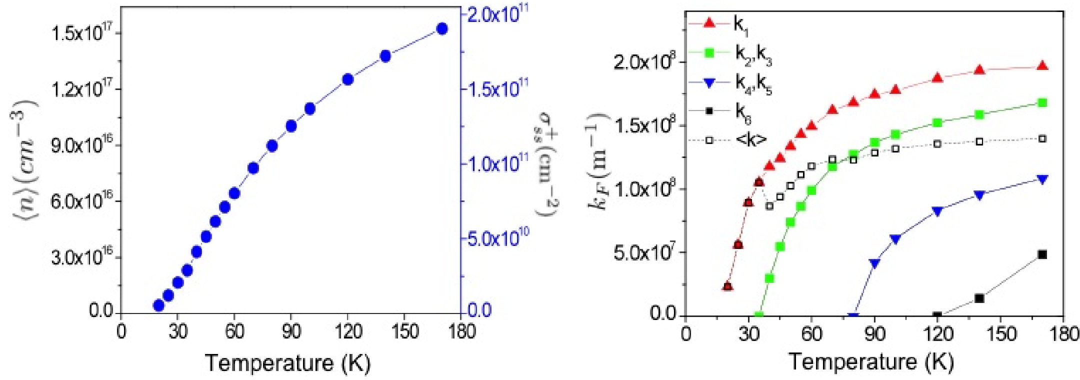

Figure 2.9: (a) The values of surface donor density, $\sigma_{ss}^{+}(T)$, used as inputs for the numerical simulation of a 50 nm diameter nanowire are shown on the right vertical axis. The functional form, described in the text, models a simple thermal activation of donors. The resulting average conduction electron densities, $\langle n(T)\rangle$, are shown on the left axis. The $\sigma_{ss}^{+}(T)$ values were chosen to produce $\langle n(T)\rangle$ at $V_g = 0$ similar in magnitude to the values observed experimentally for device 2 at peak mobility. (b) Fermi wavenumbers $k_1, .., k_6$ of the first six radial subbands calculated from the Schrodinger-Poisson solutions for inputs $\sigma_{ss}^{+}(T)$. $\langle k\rangle$ is the average value over thermal occupation, and is proportional to the average electron velocity.

where E_F is the quasi-Fermi level, F_j is the Fermi-Dirac integral of order j, and $m^* = 0.023$ m_e. The electron concentration in three dimensions is $n(x, y, z) = n_{2d}(x, y)/L$, where L is the nanowire length. The Fermi energy E_F is determined by the net conduction electron concentration at zero gate voltage. Figure 2.9(a) shows the values of $\sigma_{ss}^{+}(T)$ used in the simulations, and the resulting spatial average conduction electron density $\langle n(T)\rangle$. We chose a function $\sigma_{ss}^{+}(T) = \sigma_0 + \sigma_1 e^{-E_a/kT}$ to model the thermal activation of surface donor states, where $\sigma_0 = 1.7 \times 10^9$ cm^{-2}, $\sigma_1 = 9.8 \times 10^{10}$ cm^{-2} and $E_a = 6.7$ meV for the curve in figure 2.9(a). These values were chosen so that the simulated electron density at zero gate voltage would roughly match the experimentally measured carrier density of device 2 at peak mobility. Note that peak mobility occurred at negative gate voltages in the real device, so the actual densities of surface donor states are likely larger than the values used in simulation. The reason for carrying out the simulations at zero gate voltage was to model the behaviour for a radially symmetric wavefunction, unperturbed by the presence of a nonzero gate voltage, for simplicity.

Mobility is calculated using a multi-subband momentum relaxation time approxima-

tion [58]. We define three-dimensional eigenstates $|m,k\rangle = \psi_m(x,y)e^{ikz}/\sqrt{L}$, where m is the radial subband index and k is the axial wavenumber. The transition probability $T^{mn}_{k,k'}$ between the states $|m,k\rangle$, $|n,k'\rangle$ are calculated using Fermi's golden rule:

$$T^{mn}_{k,k'} = \frac{2\pi}{\hbar}|M^{mn}_{k,k'}|^2\delta(E_k - E_{k'}) \tag{2.6}$$

where $M^{mn}_{k,k'}$ is the scattering matrix element $\langle k,m|V_C|k',n\rangle$ resulting from the Coulomb interaction potential V_C of charged surface impurities. In our numerical simulations, V_C is obtained directly from the Poisson solver, and this takes into account both screening and dielectric mismatch effects [59, 60]. In the absence of these effects, V_C would be analytically expressed as a sum over unscreened point-charge potentials. In a cylindrical coordinate system (r,θ,z) where r and z are the radial and axial coordinates,

$$V_C = \sum_i V_{C,i} = \frac{e^2}{4\pi\epsilon_0\epsilon_r}\sum_i \left(r^2 + (D/2)^2 - rD\cos\theta_i + (z-z_i)^2\right)^{-1/2} \tag{2.7}$$

where $V_{C,i}$ is the potential due to a single impurity located at $\mathbf{r}_i = (D/2, \theta_i, z_i)$. With the numerically-derived V_C that includes screening effects, we find that the value of $M^{mn}_{k,k'}$ for a single positively charged surface impurity is on the order of 10^{-2} meV or less. Its smallness is due to the vanishing of $|\psi|^2$ at the surface, the large dielectric constant for InAs, screening effects, and that the scattering potential is attractive. In this case, treating scattering from single impurities independently and incoherently adding their rates can only lead to the observed mobilities if the surface impurity charge densities are unreasonably high, $N \sim 10^{13}$ cm^{-2}. At such densities, the mean separation between scatterers is too small for the picture of uncorrelated scattering to be valid. On the other hand, for a V_C that is the collective potential corresponding to a random distribution of many scatterers over the length of the nanowire, we are able to obtain the observed mobilities at impurity densities $N(T) \sim \sigma^+_{ss}(T)$ (see figure 2.10). This approach justifies the empirical expression $\propto N^{-2}$ used in the previous section to fit the experimental data, since the scattering matrix element M^{mn} now roughly scales with N, rather than being independent of N in the picture of uncorrelated single-defect scattering.

The scattering matrix element is given by

$$M^{mn}_{k,k'} = \int_0^{D/2}\int_0^{2\pi}\int_{-L/2}^{L/2} r\psi_m(r,\theta)V_C\psi^*_n(r,\theta)e^{-i(k-k')z}dz d\theta dr \tag{2.8}$$

where V_C is the total potential corresponding to a set of impurities. The integral in equation 2.8 has no straightforward analytical solution, so is generally solved numerically

[52]. The geometry for simulating correlated scattering is indicated schematically in figure 2.10(a), and the Poisson solution V_C obtained for a random impurity distribution is shown in figure 2.10(b). The relaxation rate in subband m due to scattering into subband n is calculated as

$$1/\tau^{mn}(k) = \sum_{k'} (1 - \cos\phi) T^{mn}_{k,k'} \tag{2.9}$$

where ϕ is the angle of deflection between the incoming wave vector k and the outgoing wave vector k'. The values of k' are given by energy conservation, $E_m + \hbar^2 k^2/2m^* = E_n + \hbar^2 k'^2/2m^* = E_F$. In a 1D geometry, only back scattering events contribute to electron relaxation rates. When the electron concentration permits the occupation of multiple subbands, the relaxation rate in the mth subband is obtained as $1/\tau_m(k) = \sum_n 1/\tau^{mn}(k)$, where k is the initial momentum. At low temperatures, it is valid to only consider the relaxation time for an electron with Fermi wavenumber k_F. Making this approximation, we substitute the Fermi wavenumber in each subband for k. The average relaxation time is given by $\tau = \sum_i \tau_i n_i/n$, where n_i is the population of ith subband, leading to an average electron mobility $\mu = e\tau/m^*$. Figure 2.9(b) shows the Fermi wavenumbers of the first few radial subbands calculated from the Schrodinger-Poisson solutions for input donor densities $\sigma^+_{ss}(T)$. The first excited subband appears near 40 K, producing a dip in the average wavenumber $\langle k_F \rangle$. The sharp drop in Fermi velocity as temperature is lowered below 40 K strongly increases the ionized impurity scattering rate, which causes a drop in mobility.

We performed the scattering calculations in two ways: (i) calculating integrals $M^{mn}_{k,k'}$ for the electron wavefunction and scattering potential over the entire length of the $L = 1$ μm nanowire, and (ii) restricting the problem to a subsection of the nanowire of length $l < L$. Method (ii) is motivated by the fact that the experimentally observed mobilities suggest a mean free path $l_{mf} \sim 100 - 200$ nm or less [61], so that on average, we expect an electron traversing the nanowire to experience several uncorrelated scattering events. In the latter picture, the scattering rate τ^{-1} is calculated from the $T^{mn}_{k,k'}$ for the electron wavefunction restricted to a length l comparable to the mean free path, and the scattering rate for the entire length of nanowire is L/l times this rate. On the other hand, the probability for the electron to be in any one subsection is l/L, so these factors cancel. The only difference between the two cases is that the 1D density of states gl, which appears in the evaluation of equation 2.9, is proportional to the subsection length. Hence, for an electron treated quantum mechanically on a length scale l (but classically on larger length scales), the density of states to scatter into is lower than if the wavefunction were spread across length L, increasing the calculated mobility. Therefore a factor L/l larger density of scatterers is required in calculation (ii) relative to (i) in order to produce the same calculated mobility.

The results of these calculations are shown in figure 2.10: (d) shows the density of scatterers N obtained by calculations (i) and (ii) that reproduce the experimental mobili-

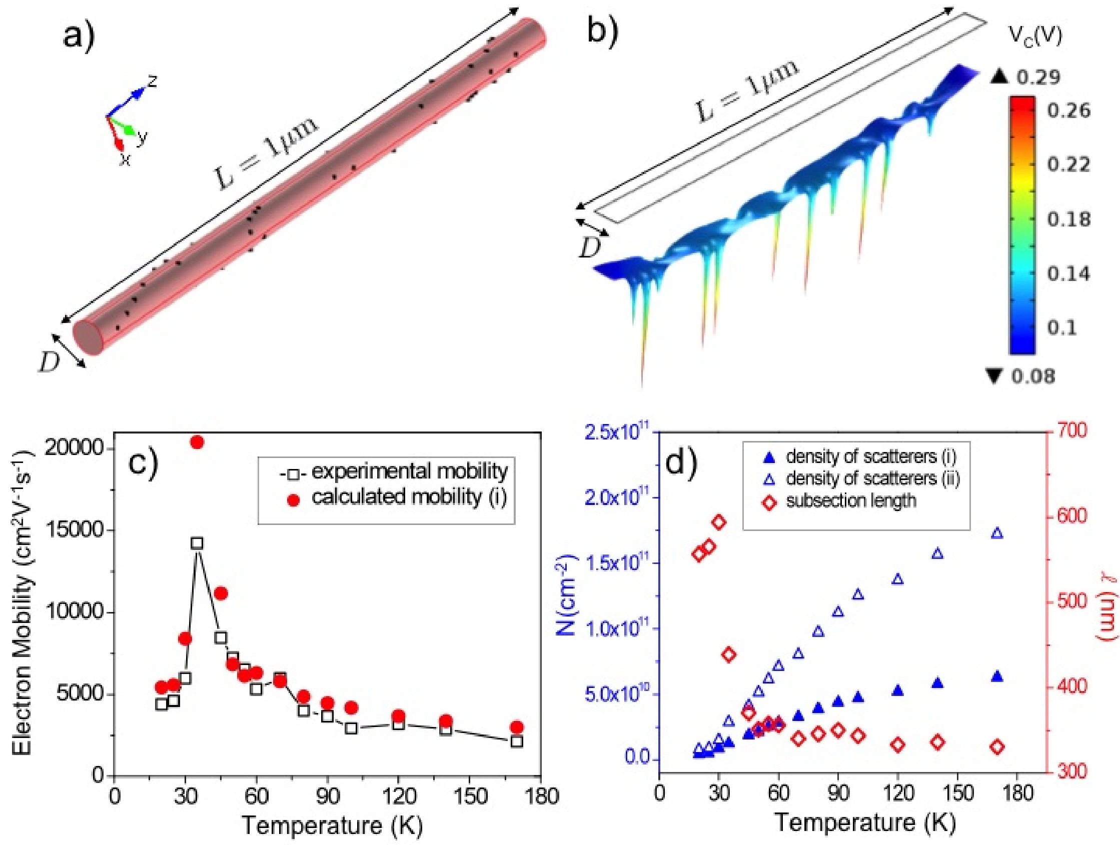

Figure 2.10: (a) Geometry used for calculating scattering from a random distribution of surface charges for a nanowire of total length $L = 1$ μm and diameter D =50 nm. The total scattering rate is obtained by calculating the scattering matrix elements over the entire nanowire in method (i), or by calculating the matrix elements over a subsection of length l and incoherently adding the rates from all L/l sections in method (ii). (b) Poisson potential V_C corresponding to the surface charge distribution in (a), projected onto a plane along the axis of the nanowire. (c) Comparison of the experimental mobilities (device 2) and the mobilities calculated using method (i) (the results using method (ii) are nearly identical). (d) The densities of surface charges $N(T)$ that produce the calculated mobilities in (c) for both methods. The subsection lengths l used in method (ii), loosely identified with mean free path, are shown on the right axis.

ties. In calculation (ii), a variable subsection length l was chosen such that $N(T) \approx \sigma_{ss}^{+}(T)$; these l values are plotted on the right axis. The calculated mobilities from (ii) are shown in

figure 2.10(c) in comparison with the experimental values. A three-fold increase of N over the range 40-150 K is able to explain the observed decrease in mobility with temperature for both calculation methods. Furthermore, the density of scatterers is nearly a perfect match to the assumed ionized surface donor density for method (ii). It is reasonable to expect that the increase of N with temperature results from the thermally activated ionization of surface donor states. Confinement also plays a role in this temperature dependence, since higher radial subbands contribute to a larger electron concentration near the surface, with a corresponding increased scattering rate. However, for a fixed N, this confinement effect is too small to cause a negative slope of the mobility-versus-temperature. We find that interband scattering plays a very limited role, giving at most a correction of order 10% to the scattering rates. As expected, the positive slope of mobility below 40 K follows the behaviour of the average Fermi velocity (figure 2.9b) over the same temperature range, where only the lowest radial subband is occupied. Overall, the simulation results confirm that scattering from charged surface states at expected densities can explain the magnitude and temperature dependence of the experimental mobilities.

2.6 Structural defects and mobility

Finally, we studied the relationship between structure and mobility by performing post-measurement TEM on selected devices; this was motivated by the observation that a fraction of devices displayed significantly lower mobilities than were typical for a given nanowire diameter. A Focused Ion Beam (FIB) was used to remove devices from the substrate, after which they were placed on a holey carbon TEM grid for inspection. Indeed, it was observed that a 55 nm diameter nanowire with low mobility $\sim 1,000$ cm^2/Vs had a high linear density of stacking faults, at least $\sim$(70 nm)$^{-1}$ as shown in figure 2.11. In contrast, the highest mobility device we measured, device 1, had no visible faults along the entire channel length. Device 3 ($D = 35$ nm) was found to have only one visible fault as shown in figure 2.11, and better mobility than the $D = 55$ nm device, despite having a smaller diameter. The magnitude and temperature dependence of mobility appear to be greatly reduced in the $D = 55$ nm device due to the high density of stacking faults. Wurtzite InAs has a $\sim$ 20% larger bandgap than zincblende InAs [62], so that for electrons, stacking faults correspond to potential wells that may be as deep as $\sim$ 70 meV. Since these are planar defects, the reflection coefficient for an incoming plane wave can be a sizable fraction of unity. On the other hand, we cannot obtain theoretical mobilities as low as $\sim 1,000$ cm^2/Vs from a simple 1D model of square well potentials at the linear

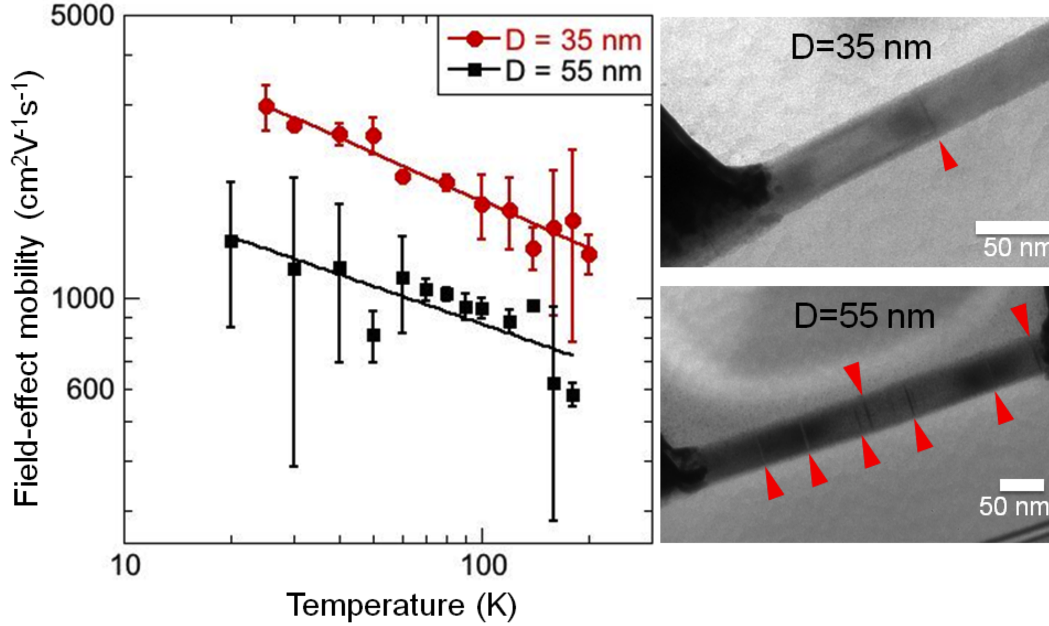

Figure 2.11: Stacking fault density and reduced mobility. Peak field-effect mobilities (left) and post-measurement TEM images (right) for device 3 (D =35 nm) and a low-mobility D =55 nm nanowire FET device. Stacking faults are indicated by the red arrows; at least 7 faults can be seen in the D =55 nm nanowire, compared to only one visible fault in the D =35 nm nanowire. The nanowires are imaged along the $[2\bar{1}\bar{1}0]$ zone axis so that all planar defects will be visible. The solid lines show power law fits to $T^{-0.4}$ and $T^{-0.3}$ for the 35 nm and 55 nm devices, respectively. No faults were observed along the entire channel for device 1 (average diameter 71 nm).

defect density observed here. It is possible that the longer zincblende sections may contain bound states that trap electrons [63], leading to Coulomb scattering. Gap states that trap charges locally can arise at dislocations [64], however, there are no mechanisms within the VLS growth method through which dislocations could form for the bare (111) oriented InAs nanowires studied here. A stacking fault is simply a rotation of the tetrahedral coordination for one monolayer, which leaves the lattice four-fold covalently bonded and free of distortion. Further investigation is required to clarify the origin of the surprisingly low mobilities seen here. Importantly, the low fault densities observed in devices 1 and 3, together with the characteristic mobility temperature dependence in figure 2.5, rules out the possibility of stacking faults being responsible for the turnover in mobility below 50 K.

2.7 Discussion

The numerical modeling explains the temperature dependence of the bare InAs nanowire mobility. As temperature is increased above 40 K, the mobility decreases due to the thermal activation of scatterers. Conversely, as the temperature is lowered from 40 K, the rate of ionized impurity scattering increases due to lowering of the Fermi velocity. While the temperature dependence of core/shell nanowires is similar for higher temperatures, it continues to increase as temperature is lowered. This suggests a possible reduction of ionized impurity scattering for the core/shell geometry. Indeed, the fitting parameters to the analytic equation for mobility seem consistent with a reduced density of scatterer. An interesting possibility is that the primary electron donors in the passivated nanowires may be surface states of the outer shell, rather than the InAs/InAlAs interface. In that case, the InAs/InAlAs interface could have a reduced density of surface states, and the high density of outer shell surface states would be much less effective in scattering conduction electrons in the core.

While the data and modeling in sections 2.4 and 2.5 provide strong evidence for the dominant role of positively charged surface states as scatterers, it is also possible that negatively charged impurities, such as native oxide charge traps [65], might play a role. Negative charges produce stronger scattering potentials [60], so that a relatively small number of impurities could limit the electron mobility. On the other hand, we observe that the pinchoff threshold voltage shifts to more positive values as temperature is reduced, but more positive gate voltages should lead to *higher* occupation of negative traps. Furthermore, if oxide charge traps limited mobility, then we would expect much higher mobilities in the core/shell nanowires where the oxide surface is $12 - 15$ nm away from the core. Somewhat higher mobilities were observed in those nanowires, but only by a factor ~ 1.25. Therefore we suspect that oxide charge traps do not play an important role with regard to mobility in these nanowires. A related concern is the possibility of scattering due to electrostatic fields from trapped charges in the underlying SiO_2 substrate. This cannot be firmly ruled out from the present data. Experiments with FET devices made from nanowires encased in alternate dielectrics (e.g. SiN_x, Al_2O_3) are presented in chapter 5 and show that the dielectric does effect mobility. We also have not considered surface roughness scattering as a dominant mechanism, though certainly it contributes to the scattering rate. The reasoning is two-fold: (1) the temperature dependence above 50 K does not appear to be consistent with surface roughness scattering, which should be weak or even increase with

temperature [66, 42], and (2) surface roughness has been observed to limit the mobility to these values only in the case of thin (sub-10 nm thick) conduction layers [66]. Hence, we only expect surface roughness to be dominant for the accumulation layer, which makes a large contribution to the device conductance only when the device is fully on. Indeed, the temperature dependence of mobility in the fully on state is much weaker, as seen in figure 2.4b. A further argument is that epitaxial core/shell passivation should smooth the roughness and lead to much higher peak mobilities, but this does not appear to be the case. Finally, at low temperatures we must consider the Coulomb interaction between electrons that form 'puddles' in a disordered potential, i.e. charging effects. This might provide an alternate explanation for the mobility drop below 50 K. However, the core/shell nanowires also exhibit coulomb blockade behavior at low temperature, but do not show a decrease in mobility with temperature. This suggests that the Coulomb interaction is an unlikely explanation for the turnover in mobility.

2.8 Conclusion

In conclusion, we have shown evidence to support the hypothesis that ionized impurity scattering by charged surface states dominates the peak electron mobility in InAs nanowires across a wide range of temperatures. For bare nanowires, transport measurements show a ubiquitous turnover in the temperature-dependent mobility below ∼50 K. In contrast, InAs/$In_{0.8}Al_{0.2}As$ core/shell nanowires show an increasing mobility down to low temperature, indicative of a lower rate of ionized impurity scattering. The decrease in mobility with temperature above 50 K can be explained by a thermally activated increase in the number of scatterers. The different temperature dependence below 50 K is attributed to a decrease in the overall surface scattering rate in the core/shell nanowires. The results for pure InAs nanowires provide a benchmark to compare with the transport behaviour of nanowires passivated by chemical means or by alternative epitaxial shells. Additionally, by performing TEM measurements subsequent to transport measurements, we find that stacking faults cannot be responsible for the characteristic mobility temperature dependence, but that nanowires with high stacking fault density appear to have sharply reduced mobilities.

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Holloway, Gregory W., et al. "Electron transport in InAs-InAlAs core-shell nanowires." *Applied Physics Letters* 102.4 (2013): 043115.

Chapter 3

Trapped charge dynamics in InAs nanowires

Chapter contributions: Devices were fabricated by Yipu Song. Cryogenic measurements were performed by Gregory Holloway and Jonathan Baugh. Data analysis was carried out by Gregory Holloway.

3.1 Introduction

InAs nanowires continue to attract much attention as an interesting material for nanoscale circuits [67], spin-dependent quantum transport [31], single electron charge sensing [68, 56] and potentially for realizing topological quantum states [69, 70, 71]. A serious impediment to obtaining clean behaviour in transport devices is the uncontrolled spatial variation of electrostatic potential along the nanowire, evidenced by spontaneous quantum dot formation at low temperatures [18]. These fluctuations may be due to surface defects [55], stacking faults [18], or charged defects in the nanowire or in the native oxide layer [72, 73, 60]. Fluctuations due to charge traps can vary in time due to carrier trapping and detrapping events, leading to the appearance of random telegraph noise (RTN) in the device conductance. The large nanowire surface-to-volume ratio renders nanowire transistors very sensitive to these charge fluctuations [56, 65]. We have observed and studied RTN in a number of InAs field-effect transistor (FET) devices and here show results consistent with the charge traps giving rise to RTN residing in the oxide. Similar results are also seen in core/shell InAs/$In_{0.8}Al_{0.2}As$ nanowires, suggesting that the shell layer does not complete

decouple the nanowire from these oxide traps. However, here we focus on the behavior in bare InAs nanowires. The charge dynamics are consistent with a charge trap model that includes a Coulomb energy barrier [74] in addition to a multiphonon emission barrier [56]. These results confirm that the native oxide is the main source of charge noise in high quality InAs nanowires, and help to shed light on the underlying physics of the trapped charge dynamics.

In order to study the trapped charge behaviour, we employ FET devices in which the global potential of the nanowire channel is adjusted using a backgate. The nominally undoped nanowires are n-type, due to the presence of surface states which act as electron donors [55, 75]. At certain temperatures and at sufficiently slow gate sweep rates, random jumps can be seen in the source-drain conductance (figure 3.1a). These shifts are evidence of the changes in local potential that occur as the charge state of a trap changes by one electron. The trapped electron generates an electric field in the nanowire that produces a potential barrier, and local depletion of carriers, reducing conductance [73, 76, 60]. By setting the gate voltage to be constant near one such step and measuring the DC conductance versus time with sufficiently large bandwidth, RTN can be observed and recorded (figure 3.1b). Occasionally, we have seen multilevel fluctuations reflecting the dynamics of multiple traps [77], but here we focus on single trap behaviour. Guided by the Coulomb barrier model of Schulz [74], we perform experiments in which the modulation of gate voltage and temperature are used to determine the activation energies and place upper bounds on the radial locations of individual charge traps. The capture and emission dynamics we observe are consistent with traps that are charge neutral in the empty state and negatively charged in the filled state, i.e. electron traps.

3.2 Methods

The InAs nanowires used here are grown in a gas source molecular beam epitaxy system using Au seed particles[1] [17]. Nanowires are mechanically deposited onto a 180 nm thick layer of SiO_2 on top of a degenerately doped silicon wafer. Using scanning electron microscopy, we select untapered nanowires with diameters 30-60 nm for contacting. Ni/Au Ohmic contacts are deposited after an etching/passivation step [27], with a typical FET channel length of 1 μm. The sample is then wire-bonded to a chip carrier and cooled

[1] Nanowires are grown by Chris Haapamaki in Ray LaPierre's group at the Centre for Emerging Device Technologies at McMaster University, Hamilton, Ontario, Canada. Technical assistance with the MBE was provided by Sharam Tavakoli

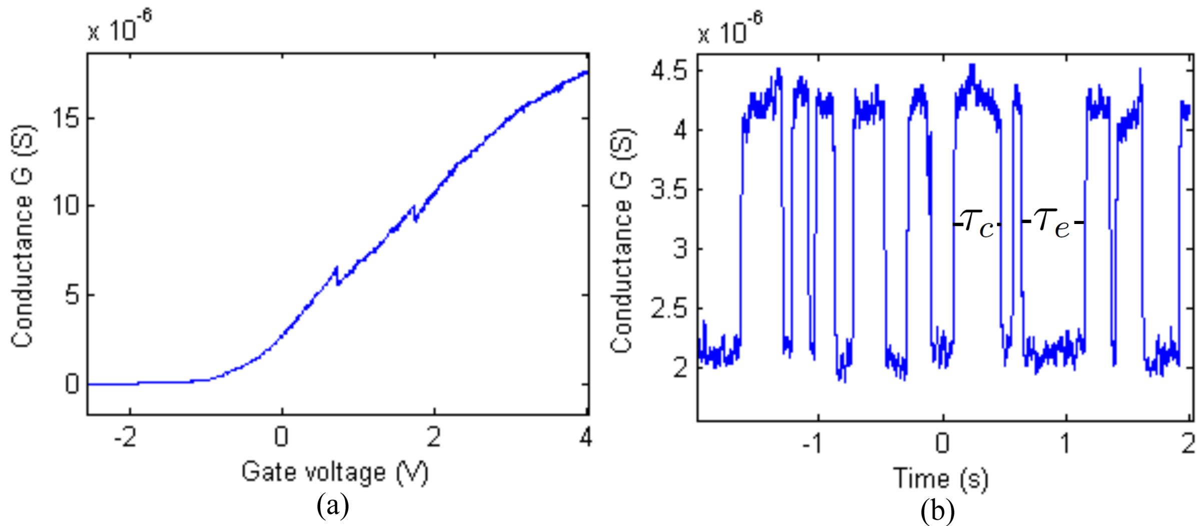

Figure 3.1: (a) Conductance through an InAs nanowire FET as gate voltage is swept from negative to positive values. The two visible jumps are caused by electron capture events in two different charge traps. (b) Random telegraph signal in the FET conductance versus time, showing two-level behaviour. The electron capture and emission times, τ_c and τ_e, correspond to the high and low conductance states, respectively.

in liquid helium vapour, with temperature controllable between 4 and 300 K. Differential conductance at low frequencies ($0.1 - 2$ kHz) is measured with a standard lock-in and current-voltage preamplifier circuit. The lock-in output is measured with a digital oscilloscope, and conductance traces up to 20 s long are recorded. The measurement bandwidth is determined by the filter of the lock-in, and for these experiments was in the range of $0.3 - 3$ kHz.

3.3 Trapped charge dynamics

To study the trap dynamics we measure the average capture and emission times of individual traps. Because RTN is known to follow Poisson statistics [73], these times are obtained by taking an average over many conductance jumps. The capture and emission times can

be described by the Shockley-Read-Hall relations as [74]:

$$\langle \tau_c \rangle = 1/(nC_n) = \left[N_C C_n e^{-(E_C - E_F)/k_B T}\right]^{-1} \tag{3.1}$$

$$\langle \tau_e \rangle = \left[N_C C_n e^{-(E_C - E_T)/k_B T}\right]^{-1}, \tag{3.2}$$

where the average capture time $\langle \tau_c \rangle$ is inversely related to the product of the density of free electrons n and the capture coefficient C_n. The density of electrons can also be expressed through Boltzmann statistics using the energy difference between the conduction band energy E_C and Fermi level E_F, where N_C is the effective density of states in the conduction band, k_B is the Boltzmann constant and T is the temperature. Similarly, the emission time reflects the energy separation between the conduction band and the trap energy level E_T.

The typical conduction electron density in the nanowire is $\sim 10^{17}$–10^{18} cm^{-3}, including a surface accumulation layer, suggesting that the capture time should be short for a trap in the nanowire or on its surface. Experimentally, however, we find that the capture time can often be on the order of seconds or longer. This discrepancy suggests two things: (i) the capture coefficient must be small, indicating a trap located outside the conduction volume (e.g. in the native oxide), and (ii) there is an additional energy barrier that must be overcome to change the trap occupancy. For a trap located in an insulating region adjacent to a semiconductor populated with carriers, there is a Coulomb energy associated with the image charge that is created when an electron transfers from the conduction band to the trap, i.e. the trap may be modeled as a capacitor with a corresponding charging energy. For traps only a few nanometers from the semiconductor surface, this charging energy is typically on the order of 100 meV [74], which leads to a large deviation of capture and emission times from the Shockley-Read-Hall predictions. The results for planar structures are used here, and can be written $\Delta E = (qx_T/T_{ox})(V_G - V_{FB} - \Psi_S)$ [74, 72], where q is the trapped charge, x_T is the trap location relative to the nanowire surface, T_{ox} is the thickness of the gate oxide, V_G is the back gate voltage, V_{FB} is the flat-band voltage, and Ψ_S is the surface potential. Taking into account this Coulomb energy, we replace $E_C - E_F \rightarrow E_C - E_F + \Delta E$ in equation 4.1 and $E_T \rightarrow E_{T0}$ in equation 3.2, where E_{T0} is the energy level of the empty trap. It is also necessary to include an energy E_B in both equations 4.1 and 3.2 to account for a multiphonon emission process [65, 78]. This term is gate voltage independent and is the energy barrier for the simultaneous emission of several optical phonons. This process mediates the transition of the electron-lattice configuration coordinate between the free and bound electron states [79].

The energy barriers for capture and emission can now be written as $E_{cap} = E_C - E_F + \Delta E + E_B$ and $E_{emis} = E_C - E_{T0} + E_B$. The corresponding energy level diagram is shown in figure 3.2a. Trapping occurs when an electron at the Fermi level gains sufficient energy to reach the transition energy level, from which it can enter the trap at energy E_T. Emission

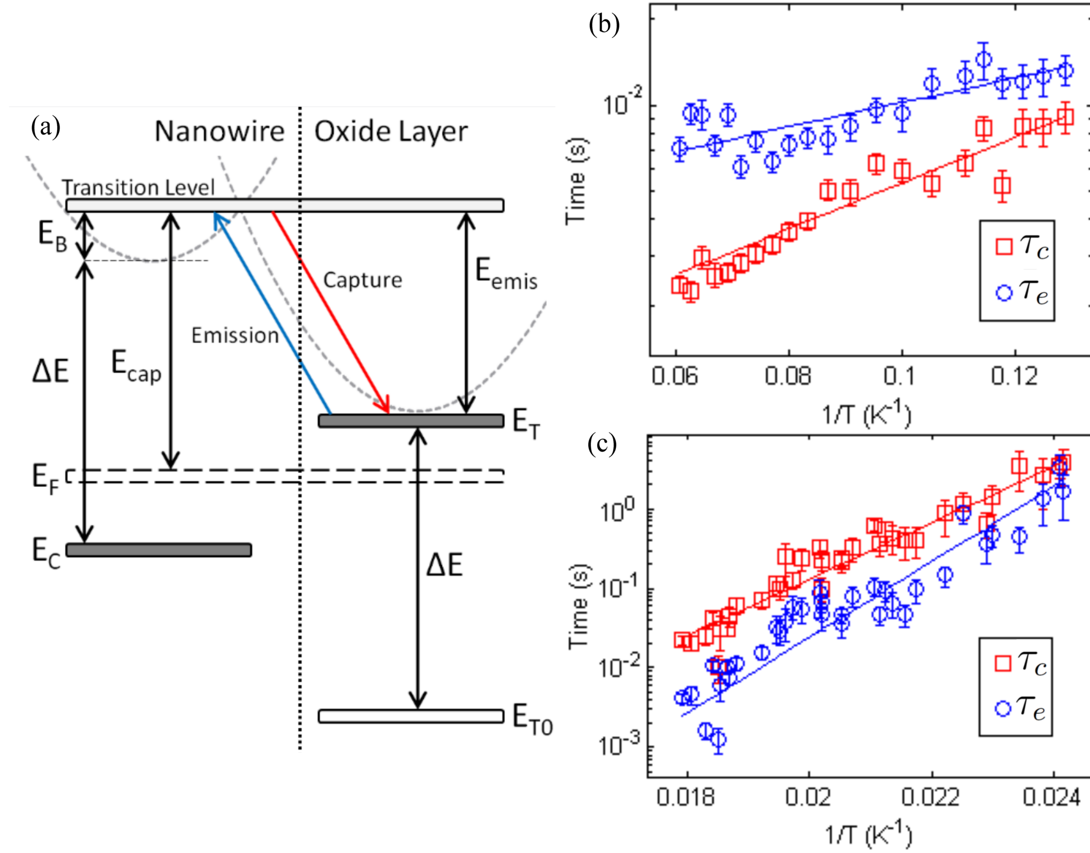

Figure 3.2: (a) Energy level diagram describing a trap model consistent with our data. E_F and E_C are energies of the Fermi level and the conduction band in the nanowire. The vertical dotted line separates the nanowire and its native oxide. The dashed parabolas represent the quadratic dependence of the electron-lattice interaction energy on the configuration coordinate (not shown), which leads to the multiphonon emission barrier [56] of energy E_B. E_T and E_{T0} are the energies of the filled and empty trap states. The upper horizontal line indicates the energy of the transition level that is $\Delta E + E_B$ above the conduction band, where $\Delta E = E_T - E_{T0}$ is the Coulomb energy. E_{cap} and E_{emis} are the energies required for electron capture and emission to occur. E_{cap} varies linearly with ΔE, whereas E_{emis} is independent of ΔE. (b,c) Variation in the average capture and emission times of two different traps in the same FET device, versus $1/T$. The fits (solid lines) described in the text yield the energy barriers associated with capture and emission.

occurs when a trapped electron can overcome the energy barrier E_{emis}. Both processes are thermally activated. Gate-induced changes in ΔE will cause the transition level and E_T to shift together relative to the other levels. The difference between them is constant and equal to E_{emis}. Conversely, E_{cap} depends on the separation between E_F and the transition level and varies linearly with ΔE. Both of these predictions are consistent with the RTN data shown in figure 3.3. The small gate voltage dependence for E_{emis} seen in figure 3.3 can be explained by a weak dependence of $E_C - E_F$ with gate voltage. The energy level diagram in figure 3.2a and the expressions for $\langle \tau_c \rangle$ and $\langle \tau_e \rangle$ are consistent with the data shown in figures 3.2b, 3.2c and 3.3, and correspond to a trap charge state that is neutral when empty and negative when filled [74]. For a positive/neutral charge state, varying the gate voltage should lead to capture and emission times changing at the same rate [74]. This adds support to the identification of these defects as oxide charge traps, as the InAs surface donor-like states are expected to have positive/neutral charge states [55, 60].

By measuring the average capture and emission times versus changes in temperature and gate voltage, the expressions for $\langle \tau_c \rangle$ and $\langle \tau_e \rangle$ allow us to extract information on the trap energetics. The temperature dependence of capture and emission times is fit to $\langle \tau_{c,e} \rangle = \alpha e^{E_{cap,emis}/k_B T}$. From α we obtain $N_C C_n$ for both capture and emission. For each trap studied in detail, these coefficients were equal, within error. Additionally, this fit yields the activation energies of trapping and detrapping $E_{cap} = E_C - E_F + \Delta E + E_B$ and $E_{emis} = E_C - E_{T0} + E_B$. Upon studying a number of traps, a broad range of activation energies is observed. At temperatures from $8 - 18$ K, we find for one trap $E_{cap} = 1.6$ meV and $E_{emis} = 0.9$ meV (figure 3.2b). In the temperature range $40 - 60$ K, we find $E_{cap} = 71$ meV and $E_{emis} = 94$ meV (figure 3.2c) for another trap. In the $40 - 60$ K range, conductance jumps from the first trap are no longer observed within the bandwidth of our measurements. This is understood by considering that conductance fluctuations will occur too rapidly to be resolved when thermal energy is larger than the activation energy. On the other hand, for traps with activation energy much larger than thermal energy, electrons are unable to overcome the energy barrier, and so the charge state will be frozen in. RTN observed at higher temperatures therefore arises predominantly from traps with larger activation energies.

The position of the Fermi level at typically $0 - 0.26$ eV above the conduction band [38], allows us to estimate of the magnitude of ΔE. For the trap corresponding to the data in figure 3.2c, where $E_{cap} = 71$ meV, the expression $E_{cap} = E_C - E_F + \Delta E + E_B$ suggests $\Delta E + E_B$ is roughly in the range $71 - 330$ meV. This is consistent with the expectation $\Delta E \sim 100$ meV noted by Schulz [74]. The gate voltage dependence of the capture and emission times allows us to estimate the radial distance of a trap from the crystalline nanowire surface. From the definition of ΔE there is an explicit dependence on gate voltage V_G. Therefore by fitting the ratio of capture time over emission time to $\langle \tau_c \rangle / \langle \tau_e \rangle = \beta e^{\gamma V_G}$,

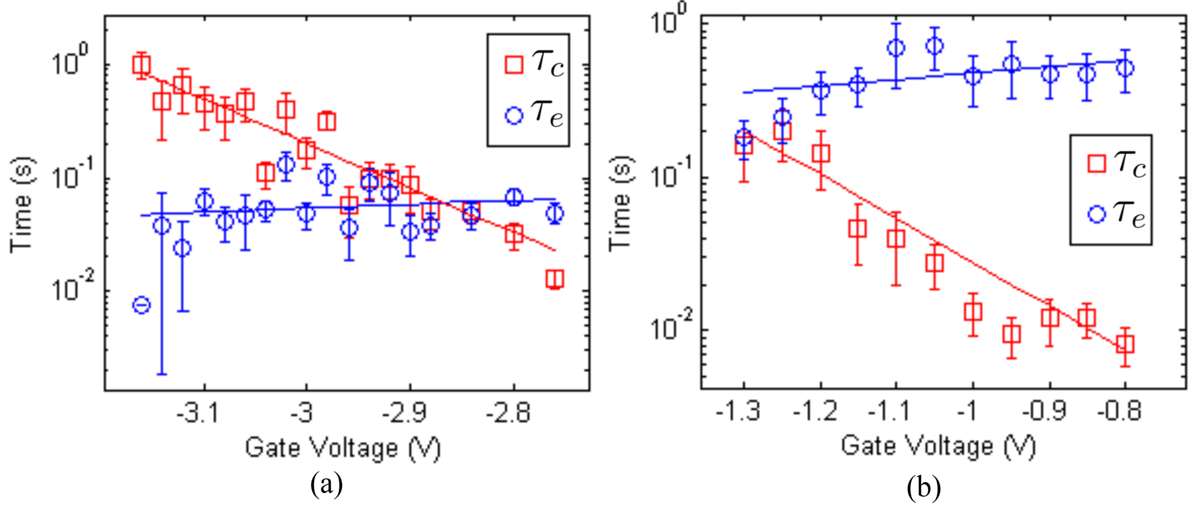

Figure 3.3: (a,b) Average capture and emission times as a function of gate voltage V_G. The weak dependence of the emission time on V_G is consistent with a model of neutral/negative charge traps. The dependence of $\langle\tau_c\rangle/\langle\tau_e\rangle$ on V_G is used to extract an upper bound on the radial distance of the trap relative to the nanowire surface.

we may estimate the separation of the trap from the nanowire surface, $x_T = \gamma T_{ox} k_B T/q$. However, this calculation neglects the dependence of the surface potential Ψ_S on gate voltage, leading to an overestimate for the value of x_T [80], so we treat this estimate of x_T as an upper bound. For the two traps shown in figures 3.3a and 3.3b, $x_T \leq 8.4 \pm 3.2$ nm and 11.8 ± 4.0 nm, respectively, whereas the amorphous oxide layer of the nanowire is known to be approximately $2-5$ nm thick from transmission electron microscopy. For the charge traps that induced the largest conductance jumps in our experiments, we estimate a charge sensitivity [56] $\approx 6 \times 10^{-4}\ e/\sqrt{Hz}$.

3.4 Hysteretic behaviour

Finally, we include data showing hysteretic effects that may arise, at least in part, from changes in the trapped charge population. An initial gate voltage V_i was applied at $T > 150$ K and during cooling to freeze in a particular charge configuration. Conductance curves measured at $T = 50$ K corresponding to three V_i values are shown in figure 3.4a for a 32 $\pm$2

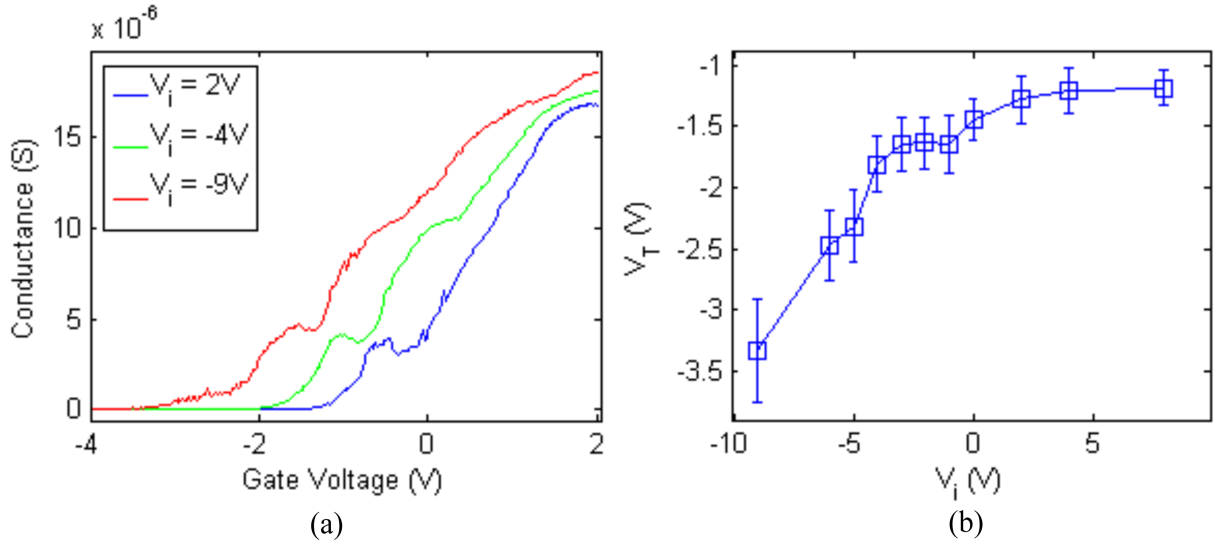

Figure 3.4: (a) Conductance curves for a 32 nm diameter nanowire FET measured at T =50 K, with several initial gate voltages V_i applied during cooldown from $T > 150$ K. When a positive V_i is applied, traps are predominantly filled and pinchoff occurs at a more positive gate voltage. Here 'traps' may refer to other defects beyond native oxide charge traps, such as InAs surface states or SiO_2 charge traps. (b) Change in pinchoff threshold voltage V_T versus V_i. The saturation that occurs at positive V_i suggests most traps are being filled. No saturation was seen for negative voltages down to -9 V, suggesting that only a fraction of traps were depleted.

nm diameter nanowire with channel length 820 nm. As an aside, reproducible plateau-like features can clearly be seen in the conductance. These features could be due to populating quantized radial subbands of the nanowire, or due to resonant scattering from a defect. The conductance curve shifts to more negative voltages as V_i is made more negative. This is consistent with the expectation that as more traps are depleted of electrons, the average conduction volume in the nanowire increases, requiring more negative gate voltage to reach pinchoff. The average slope of the conductance curve also decreases with more negative V_i, indicating a lower effective mobility. This is also consistent with a greater fraction of carrier density near the nanowire surface, which should dominate scattering. In particular, at $V_i = -9$ V we observe a pronounced low-mobility tail just before pinchoff. We cannot assign the shift in conductance exclusively to the nanowire oxide traps, since SiO_2 charge traps and the gate-induced ionization of InAs surface states may also contribute.

3.5 Conclusion

We have shown that an oxide trap model in which electrons must overcome a Coulomb barrier, in addition to a multiphonon emission barrier, to move into a bound state correctly describes sources of RTN in InAs nanowire FET devices. The model was used to extract activation energies and to place upper bounds on the radial locations of several distinct traps. Due to the appreciable density and broad activation energy range of these oxide traps, RTN is commonly observed in nanowire electronics, and hinders the performance and stability of single-electron devices. Our results suggest that oxide removal from the nanowire surface, with proper passivation to prevent regrowth, should lead to the reduction or elimination of RTN, an important obstacle for sensitive experiments at the single electron level. Recent advances in chemical passivation [81] might accomplish this, see chapter 5 for a detailed study of different chemical passivation techniques. Despite the detrimental effects of charge traps, they are useful for assessing the charge sensitivity of nanowire transistors [56].

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Chapter 4

Magnetoconductance signatures of subband structure in semiconductor nanowires

Chapter contributions: Device fabrication, cryogenic measurements, and data analysis were performed by Gregory Holloway.

4.1 Introduction

The study of quantum transport of electrons and holes in semiconductor nanowires is of fundamental interest, and underlies recent developments in nanoscale sensing [22, 56] and potential avenues for quantum information processing [82, 33, 31, 71, 70]. The quasi one-dimensional (1D) geometry of nanowires allows for a wide range of experiments on low dimensional transport, but correct interpretation of results often requires a detailed understanding of the transverse subband structure due to the confining radial electrostatic potential. Precise knowledge of the radial potential, however, is not usually straightforward to determine experimentally. Several recent experiments have shed light on the subband structure in multi-band nanowires. Quantized conductance steps were observed in quasi-ballistic (short channel) InAs nanowire field-effect transistors (FETs) [83, 84], and attributed to the successive occupation of the first few radial subbands. In the presence of a perpendicular magnetic field, these steps split into two due to the Zeeman interaction. The resulting conductance patterns have been observed as a function of magnetic field and

gate voltage [85, 86]. The presence of an axial field produces qualitatively different conductance patterns due to the coupling of orbital angular momentum to magnetic flux. Axial field magnetoconductance studies of InN nanowires [87, 88] and InAs nanowires[30] reveal oscillations caused by the occupation of orbital angular momentum subbands. With strong surface band bending, a cylindrical conducting shell forms below the nanowire surface and the resulting conduction electron energy levels are parabolic in magnetic field [88]. Levels with adjacent angular momentum quantum numbers are shifted from each other by one flux quantum. This gives rise to a flux-periodic, diamond shaped energy level structure, so that varying magnetic field at a fixed chemical potential leads to flux-periodic conductance oscillations as the occupation of orbital states is modulated. These flux-periodic oscillations have been observed in InN nanowires [87, 88], however the precise orbital states contributing to conductance could not be identified. Experiments on GaAs/InAs core-shell nanowires [89, 90], where conductance is predominantly due to the shell, also showed flux periodic oscillations. Importantly, the phase of the oscillations was seen to change by π at certain gate voltages, as would be expected from the diamond-shaped energy level structure of the orbital states. In all of these axial field magnetoconductance experiments, the focus has been on conduction in a thin shell close to the nanowire surface, such that flux-periodic oscillations are expected. In general this is obviously not always the case, as different materials can have varying degrees of band bending such that conduction may not be strongly confined to the surface. For example, nanowires with an epitaxial larger bandgap shell are expected to have reduced surface band bending [91, 43], leading to more uniformly distributed transverse electronic wavefunctions. Even bare InAs nanowires do not show the expected flux-periodic oscillations[30], likely due to reduced surface band bending compared to InN nanowires. These examples reflect the need to model conductance for more general radial potentials to accurately capture the details of the subband energy levels. In this chapter it is found that lower surface confinement alters the shape of the transverse subband energy spectrum and its dependence on magnetic field in a manner characterized by less periodicity, making precise identification of orbital subbands more practical.

Here, we calculate the energy spectra of transverse subbands for various radial potentials, ranging from flat to those with strong surface band bending. We find a quasi-parabolic behavior of these energies with respect to magnetic field, but with large variations in curvature depending on the radial potential and on the radial quantum number. Indeed, the energetic ordering of the subbands depends on the degree of band bending, and the overall pattern of conductance versus magnetic field and gate voltage provides a fingerprint of the underlying radial potential. Although similar treatments have been applied to the studies of InN and GaAs/InAs core/shell nanowires, the wavefunctions in those cases are assumed to be confined in a thin conducting shell, either by the core/shell structure or

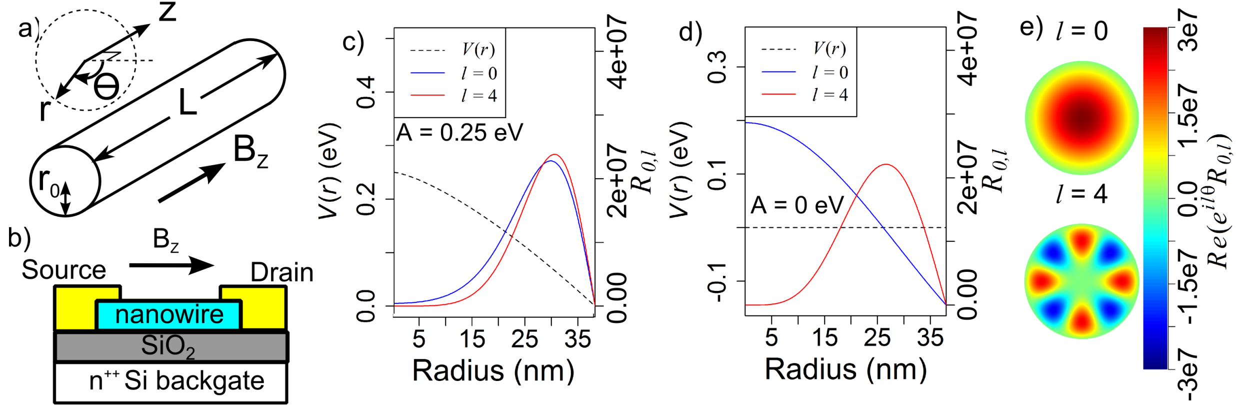

Figure 4.1: (a) The cylindrical nanowire geometry is shown with an axial magnetic field B_z. (b) Schematic of the nanowire FET used to measure magnetoconductance. The two-terminal conductance is measured between the source and drain contacts as a function of B_z and gate voltage. (c,d) Radial wavefunctions $R_{0,0}(r)$ and $R_{0,4}(r)$ normalized by $\int_0^\infty \int_0^{2\pi} |e^{il\theta} R_{n,l}(r)|^2 r dr d\theta = 1$ calculated for a cylindrically symmetric radial potential $V(r)$ defined in the main text with $A = 0.25$ eV, $b = 2.75$ (c) and $A = 0$ eV, $b = 2.75$ (d). $R_{n,l}(r)$ is characterized by the radial and angular quantum numbers n and l, respectively. The effective mass used is for InAs. Strong band bending results in a wavefunction proximate to the nanowire surface for any state with finite angular momentum. (e) Real part of the transverse electron wavefunction for the two states shown in (d).

by a strong surface potential. Here, we consider the more general case of a wavefunction that extends across the nanowire cross-section, enabling the description of devices with low to moderate surface band bending. In addition, we report the results of low temperature conductance measurements on a short-channel InAs nanowire FET as a function of gate voltage and magnetic field. Features are identified in the magnetoconductance that we show are quantitatively consistent with the occupation of a set of radial states. By calculating conduction in the weakly localized regime, we find a consistent description of the overall changes in magnitude of the conductance over a gate voltage range of 6 volts. We suggest that this method of analysis can be applied fruitfully to nanowire devices closer to the ballistic regime than the one investigated here, in order to precisely identify the subbands contributing to transport and to obtain the dominant characteristics of the radial electrostatic potential.

4.2 Model

Consider a nanowire of radius r_0 and length $L > 2r_0$, as shown schematically in figure 4.1a. Assuming cylindrical symmetry, the single particle wavefunction for conduction electrons can be written as the product: $\psi(r, \theta, z) = e^{ikz}e^{il\theta}R_{n,l}(r)$, where (r, θ, z) are cylindrical coordinates, k is the axial wavenumber, and n, l denote the radial and angular quantum numbers, respectively. To model the transverse part of the wavefunction, $e^{il\theta}R_{n,l}(r)$, we take a circular cross-section with a potential $V = \infty$ for $r > r_0$ and $V = V(r)$ for $r \leq r_0$. We choose potentials of a form studied in ref. [13], $V(r) = A(1 - (r/r_0)^{b/2})$, where $A = V(0) - V(r_0)$, $V(r_0)$ is the surface potential, and b dictates the shape of the potential. This potential is taken to be independent of the number of occupied subbands and to remain constant as the chemical potential in the nanowire is varied. In the results of later sections, ~ 10 subbands enter into the description of device conductance. The charge induced in the nanowire when 10 subbands are occupied is an order of magnitude smaller than the total charge corresponding to a typical surface charge density of 10^{12} cm^{-2}[75]. This justifies an approximate treatment of the radial potential as fixed and independent of the carrier density. Since the surface charge density is positive (surface states are donor-like), the conduction band generally bends downward [75], and in this paper we only consider $A \geq 0$. The electronic Hamiltonian with an applied axial magnetic field can be written [13]:

$$\begin{aligned} H = \frac{-\hbar^2}{2m^*}\Bigg[&\frac{1}{r}\frac{\partial}{\partial r} + \frac{\partial^2}{\partial r^2} + \frac{\partial^2}{\partial z^2} \\ &+ \frac{1}{r^2}\frac{\partial^2}{\partial \theta^2} - \frac{1}{r^2}\frac{2}{\hbar}\phi_z L_z - \frac{1}{r^2}\phi_z^2\Bigg] + V(r), \end{aligned} \tag{4.1}$$

where $\phi_z = \Phi/\Phi_0 = \pi B_z r^2/(h/e)$ is the normalized magnetic flux, B_z is the axial magnetic field, L_z is the orbital angular momentum operator and $m^* = 0.023m_e$ (for InAs) where m_e is the electron mass. This Hamiltonian neglects contributions from the spin Zeeman effect and spin-orbit coupling, which break spin degeneracy and split the subband energies (for a more general treatment, see ref. [13]). For a magnetic field of 8 T (the upper limit to field in the experimental section below), the Zeeman energy is ~ 4.2 meV for electrons in InAs, smaller than the typical subband energy separation, which justifies an approximate treatment neglecting the Zeeman effect. Equation 4.1 reduces to the following partial differential equation (PDE) for $R_{n,l}(r)$:

$$ER = \frac{-\hbar^2}{2m^*}[\frac{R'}{r} + R'' - k^2R - \frac{R}{r^2}(l + \phi_z)^2] + RV(r), \tag{4.2}$$

where primes denote derivatives with respect to r, $E = E_{n,l}$ and $R = R_{n,l}(r)$. A 4th-order Runge-Kutta PDE solver [92] numerically calculates $R_{n,l}(r)$ at fixed values of l and ϕ_z. The subband energies $E_{n,l}$ are determined by applying the boundary condition that $R_{n,l}(r_0) = 0$.

4.3 Results

4.3.1 Theory

In this section we calculate magnetoconductance for a cylindrical InAs nanowire FET, assumed to be in the ballistic transport regime, in order to establish a qualitative picture for how the radial potential determines the pattern of conductance versus field and gate voltage. A nanowire radius $r = 38$ nm is chosen that is close to the radius of the nanowire investigated experimentally in the next section. Figure 4.1b shows a schematic of the typical FET geometry; however, in the calculations which follow we assume no breaking of cylindrical symmetry by the back gate, which is approximately justified when the gate oxide thickness is large compared to the nanowire diameter. First is considered the case of strong band bending, taking $A = 0.25$ eV and $b = 2.75$. Figure 4.1c shows that in this case, the electron distribution is mostly independent of l, and is concentrated near the nanowire surface, consistent with the expected accumulation layer. In contrast, figure 4.1d shows that for a flat potential, the $l = 0$ and $l \neq 0$ states have very different spatial distributions. The magnetic field dependence of the subband energies is intuitively understood by imagining that electrons are located near the peak of the wavefunction. The limiting case of strong band bending is a two dimensional electron gas (2DEG) near the surface considered in ref. [87], where the subband energy (in the radial ground state, $n = 0$) is given by: $E_l = \frac{\hbar^2 k_z^2}{2m^*} + \frac{\hbar^2}{2m^* r_{\text{eff}}^2}(l - \phi_z)^2$, and r_{eff} is the electron's average radial position. Figure 4.2a shows that strong band bending in our model also produces $n = 0$ energy bands that are nearly parabolic with respect to the magnetic flux. The curvatures of the energy levels in the $n = 1$ manifold, appearing above 0.19 eV in figure 4.2a, are smaller than those of the radial ground state manifold because the radial expectation value r_{eff} is closer to the nanowire center for $n > 0$.

Assuming quasi-ballistic conditions, electrical conductance may be calculated using the Landauer equation [58], $G = 2e^2/h \sum_m \int \tau_m(E)(df/dE)dE$, where $\tau_m(E)$ is the transmission probability for the mth subband, and $f = f(E,T)$ is the Fermi-Dirac distribution at temperature T. For ballistic transport, $\tau_m(E)$ is a step function of unit height centered at the subband energy $E_m(B_z)$. The resulting conductance in the presence of strong band

bending is shown in figure 4.2b. This gives a series of conductance steps of height $2e^2/h$ occurring when a subband crosses the chemical potential, defined here as $\epsilon = E_F - E_C$, where E_F and E_C are the Fermi energy and conduction band edge, respectively. The rounding of the conductance steps is determined by the temperature in the Fermi-Dirac distribution, which in figure 4.2 we set to $T = 1$ K.

The frequency components of the magnetoconductance oscillations may be analyzed by calculating the Fourier transform with respect to magnetic field at each value of ϵ, as shown in figure 4.2c. The mean value of each conductance trace was subtracted prior to performing the fast Fourier transform (FFT) in order to suppress artifacts from the dc component. In the region below 0.19 eV, where only the radial ground state ($n = 0$) is occupied, the FFT shows a dominant peak at a frequency ~ 0.65 T^{-1}. This peak occurs when the flux enclosed by the average electronic radius is equal to Φ_0. A frequency of 0.65 T^{-1} implies an effective radius $r_{\text{eff}} = 29$ nm, consistent with radial wavefunctions shown in figure 4.1c. The slight increase in frequency of this peak as the chemical potential increases is due to the occupation of states with higher angular momentum that have r_{eff} closer to the nanowire surface. The peaks at double and triple this frequency are harmonics that arise from taking the FFT of a square-like wave, and are unrelated to mesoscopic interference effects. For example, the Altshuler-Aronov-Spivak (AAS) effect for cylindrical shell conduction [93, 94] would produce a peak at twice the fundamental frequency (i.e. corresponding to a flux of $\Phi_0/2$), however this is not included in our model, and we see no evidence for such oscillations in the experiments of the next section. Above 0.19 eV, an additional peak appears at lower frequency, due to the first radial excited state manifold. The effective electronic radius corresponding to this state encloses a smaller flux, resulting in a lower frequency magnetic oscillation.

The effect of decreased band bending is shown in figure 4.2d, where $A = 0$, and larger differences are seen in the curvatures of the energies $E_m(B_z)$ between subbands with the same n but different l values. For $A = 0$, the radial wavefunctions at zero magnetic field are Bessel functions of order l. The transverse wavefunctions for $l = 0$ and $l = 4$ in the radial ground state ($n = 0$) are shown in figure 4.1e. For $l = 0$, the radial wavefunction is concentrated in the center of the nanowire, giving a nearly flat magnetic field dependence of the lowest energy level in figure 4.2d. As $|l|$ is increased, the wavefunction peak moves toward the surface, with successively greater curvature in E_m versus B_z. The flat potential also lowers the energies of radial excitations, reordering the filling of states as the chemical potential is increased in comparison to strong band bending. This is visible in the lower part of figure 4.2d, where the successive subband minima move upwards in energy. This is due to an effective increase in confinement as the quantum number $|l|$ increases, since the

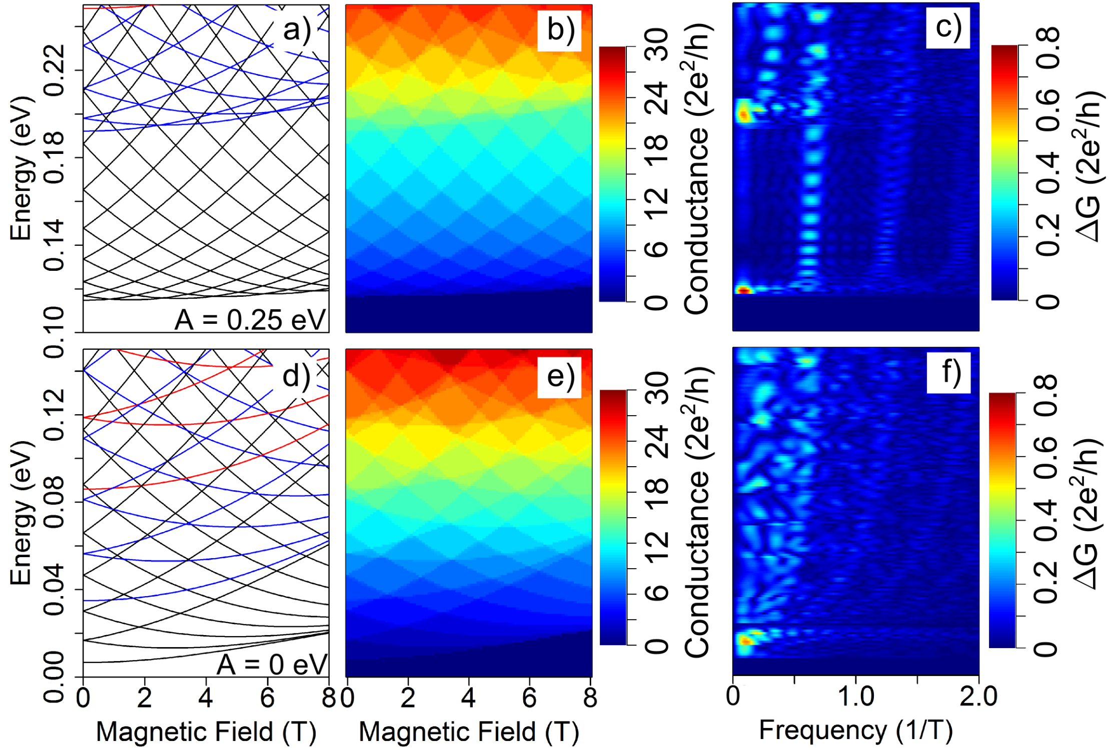

Figure 4.2: (a,d) Calculated energy levels $E_k(B_z)$ in a nanowire with radius $r_0 = 38$ nm, for radial potentials $V(r)$ with $b = 2.75$ and $A = 0.25$ eV (a) and $A = 0$ eV (d). The radial quantum number is distinguished by color, where black denotes $n = 0$, blue $n = 1$, and red $n = 2$. (b,e) Ballistic magnetoconductance calculated from the energies in (a,d) using the Landauer equation. The conductance increases (decreases) stepwise by $2e^2/h$ when a new transverse mode is populated (emptied). The vertical axis is to be identified with the chemical potential in the nanowire, modulated by gate voltage. (c,f) Fast-Fourier transform (FFT) of the conductance in (b,e). The colorscale is labeled ΔG since the FFT peak intensity reflects the amplitude of magnetoconductance oscillations at a particular frequency. The mean of each conductance trace is subtracted prior to the FFT in order to avoid low frequency artifacts.

wavefunction becomes more narrowly peaked. Figure 4.2f shows the FFT of the magnetoconductance for $A = 0$. Rather than distinct peaks, it shows a distribution of frequencies that correspond to a wider distribution of effective electronic radii compared to strong band bending. Generally, the structure of the energy spectrum is not strictly periodic in chemical potential or magnetic field. This ensures that by probing the magnetoconduc-

tance over a sufficiently large range of chemical potential (gate voltage), a fingerprint of the radial electrostatic potential can be obtained, at least in theory. The results in figure 4.2 make it clear that a flatter potential produces a more aperiodic conductance pattern that would allow the corresponding subbands to be more easily identified by comparing theory to experiment. To check for self-consistency, the conversion between gate voltage and chemical potential is straightforward to estimate based on the geometrical capacitance [49] of the gate and the density of carriers in the nanowire.

4.3.2 Experiment

A FET device based on an InAs/$In_{0.8}Al_{0.2}As$ core/shell nanowire, with a nominal Te doping density in the shell of 5×10^{16} cm^{-3}[1], was investigated experimentally. The core radius was estimated from scanning electron microscopy to be $r_0 \approx 38$ nm, and a channel length $L \approx 200$ nm between contacts was fabricated. A 300 nm thick gate dielectric (SiO_2) separated the nanowire from the backgate. The device geometry is shown in figure 4.1b, and the fabrication procedure was described in chapter 2. The chemical potential is controlled by modulating the voltage of the backgate, and an axial magnetic field up to 8 T is applied. As mentioned above, a gate separation much larger than the nanowire diameter is crucial to minimize the breaking of cylindrical symmetry in the nanowire radial potential when a gate voltage is applied. Conductance data shown in figures 4.3a and 4.4a was measured at a lattice temperature of 30 mK, with an estimated electron temperature ≈ 100 mK. Similarly, a temperature of 100 mK was used for the simulations shown in figures 4.3b and 4.4b. At this temperature, the device conductance typically shows additional modulations with field and gate voltage due to electron interaction effects (Coulomb repulsion) and interference effects (e.g. universal conductance fluctuations), the latter being due to a phase coherence length comparable to the channel length. The details of these effects are not amenable to simulation because they depend on device specific, mesoscopic potential fluctuations, making them essentially random in nature. We note here that experiments carried out at higher temperatures, such that the the phase coherence length is suppressed but the subband level spacing is still large compared to thermal energy, could suppress some of the additional conductance modulations seen in figure 4.4a. We first note two caveats in comparing the experimental data to the model described previously. One, we expect the conduction in this device to be in the weakly localized regime, rather than the

[1]Nanowires are grown by Chris Haapamaki in Ray LaPierre's group at the Centre for Emerging Device Technologies at McMaster University, Hamilton, Ontario, Canada. Technical assistance with the MBE was provided by Sharam Tavakoli

quasi-ballistic regime. This is accounted for in the model by calculating conductance using $G = (2e^2/h)N^2L_0^2/(NL_0L + L^2)$, where N is the number of occupied channels, and L_0 is a characteristic length of the order of the mean free path[95]. Note that this expression is derived from the Landauer equation to roughly include the effects of quantum interference, and is only valid in the weakly localized regime where transport is phase coherent and $NL_0 \gtrsim L$. For the case of $NL_0 \gg L$, this equation simplifies to $G = (2e^2/h)NL_0/L$, which is identical to the Landauer equation with a transmission probability of $\tau_m(E) = L_0/L$. We were not able to measure the field effect mobility directly on this device, as the back-gate was not sufficient to pinch off the conductance. From measurements of longer channel devices in the diffusive regime, we find an average elastic mean free path of $\lambda \sim 35 \pm 13$ nm for many nanowires from the same growth batch. Two, the back-gated geometry breaks the cylindrical symmetry of the nanowire and produces, at a finite gate voltage, an asymmetric radial potential. We have not included this effect in the modelling, however a numerical estimate suggests it will not be a dominant effect. Using a finite element model [2] of our device geometry, a difference in surface potential between the top and bottom surfaces of the nanowire is found to be ≈ -6.7 mV per volt of applied gate voltage. At the largest gate voltage, ± 3 V, this yields only $\sim 20\%$ of the typical surface band bending ≈ 100 meV. Note the gate sweep is also centered around $V_g = 0$ in order to minimize this effect.

As described in section 4.3.1 above, positive steps in conductance occur as the chemical potential is increased at a fixed magnetic field. Hence, the derivative of conductance with respect to gate voltage should give a positive value when the chemical potential is equal to the energy of a transverse subband, and be zero elsewhere. In figure 4.3a we plot the derivative of the raw conductance data shown in figure 4.4a. The derivative data is noisy, but shows three plausible parabolic trajectories where the derivative has an average value above the noise floor. We find analytic expressions for these curves by averaging the points in the vicinity of these features and fitting to quadratic functions with least squares fitting. The resulting curves are plotted as the three white lines in figure 4.3a. The parabolic fit describing one subband does not contain enough information to identify the subband, since it can be reproduced by a variety of radial potentials and n, l values. However, several curves can provide sufficient information to assign the subbands. We construct a simple quantitative measure by defining $d_{i,i+1}$ as the energy separation between adjacent subbands at zero magnetic field, and s_i as the linear slope near zero field (calculated from 0 to 2 T). The ratio $d_{i,i+1}/s_j$ is limited to a certain range of values that depend on the A and b parameters describing the radial potential. Examples calculated from the model are shown in figure 4.3b for l values from -1 to -6 and in three radial manifolds,

[2] Finite element method calculations were performed using COMSOL Multiphysics v4.2a.

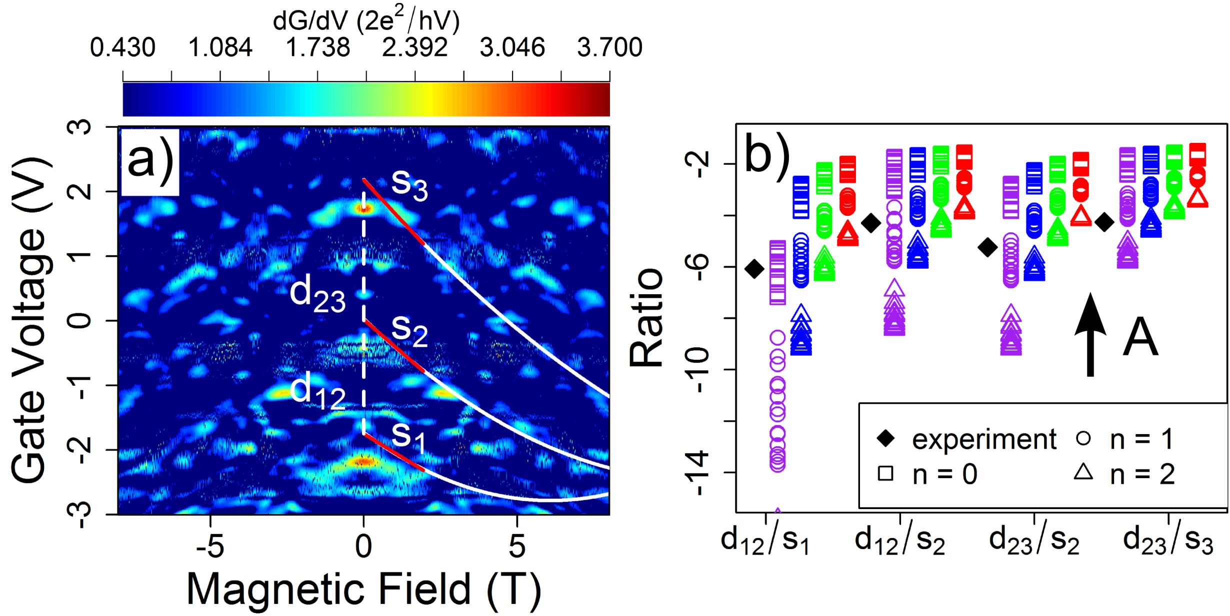

Figure 4.3: (a) Derivative with respect to gate voltage of the experimental conductance of the InAs nanowire FET, where values below 0.43 $\frac{2e^2}{hV}$ have been removed for clarity. White curves are least squares fits to parabolas consistent with transverse subbands. Red lines are linear fits to the parabolas from 0 to 2 T, used for extracting the zero-field slope of each curve. $s_1 - s_3$ indicate the slopes and d_{12}, d_{23} indicate the vertex separations in gate voltage.(b) Ratios $d_{i,i+1}/s_j$ calculated for a range of A and b values, as described in the text. Colors indicate different sets of l values: purple: $l = (-1, -2, -3)$, blue: $l = (-2, -3, -4)$, green: $l = (-3, -4, -5)$, red: $l = (-4, -5, -6)$. These are plotted for three different radial excitation manifolds, $n = 0, 1, 2$. Experimental values (black diamonds) from the fits to the data in (a) show best overall agreement with the $n = 1$, $l = (-1, -2, -3)$ states. The $\uparrow A$ symbol indicates the direction of increasing A values, i.e. stronger band bending.

$n = 0, 1, 2$. Here A is varied from 0 to 0.2 eV, and b from 2 to 9 (however the ratios depend much more strongly on A than b). The magnitude of the ratio $|d_{i,i+1}/s_j|$ decreases as A is increased, i.e. as the surface potential becomes larger. The dependence on b is opposite to this, but much weaker. This provides an unambiguous way to correlate the parabolic features in the experimental data to a model of the radial potential, and in principle to identify the corresponding transverse subbands. Note that these ratios are independent of the energy scale, so that the correspondence between experimental gate voltage and chemical potential is not needed for matching theory to experiment; on the contrary, finding

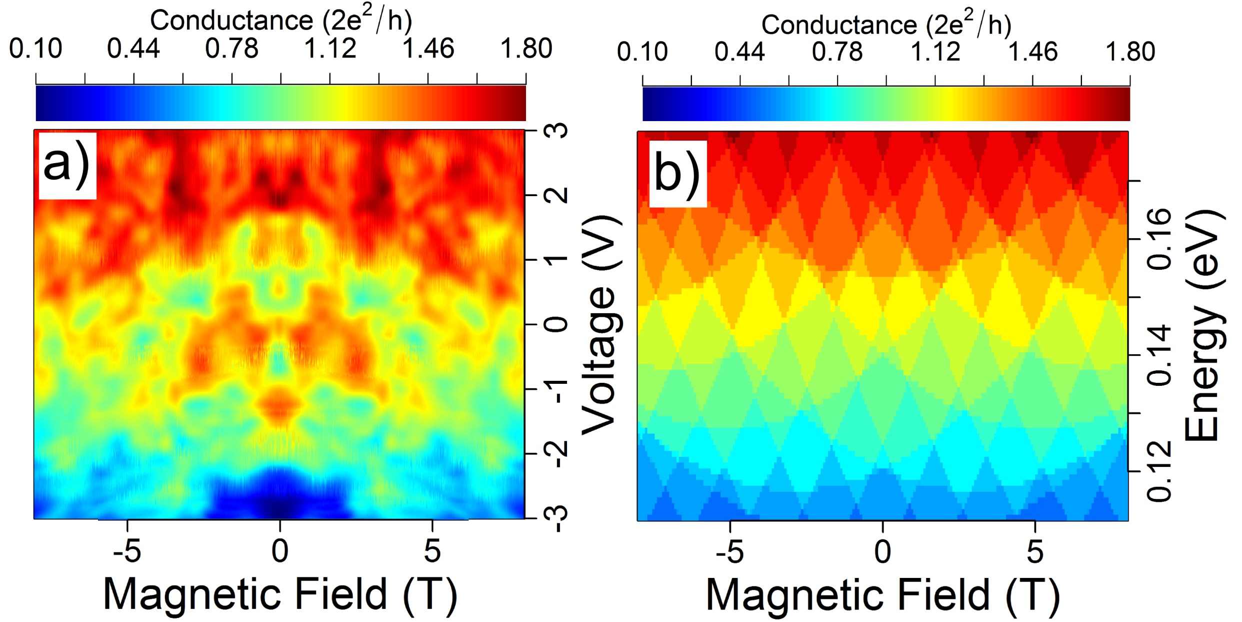

Figure 4.4: (a) Raw experimental magnetconductance of an InAs nanowire FET, the source of the data shown in figure 4.3a. (b) Simulated magnetoconductance for $A = 0.11$ eV and $b = 2.75$, over a range of chemical potential consistent with the experimental data, as described in the text. The relative transmission probability of each subband is crudely estimated by calculating the expectation value of the Coulomb potential due to a surface charge to take into account surface charge scattering. Note that the conductance scales for the two plots are nearly the same.

this match automatically determines the correspondence. Clearly, a stronger assignment can be made when there are more subbands visible in the data. From the data in figure 4.3a we extract the ratios indicated as black diamonds in figure 4.3b. For three out of the four possible ratios, the subbands with $n = 1$, $l =$ -1 to -3 are found to match the data. The average band bending parameter for these three points is $A = 0.11$ eV. We conclude that these are likely candidates to assign to the three parabolic features in the data, however, the data from this device is too sparse and noisy to make an unambiguous assignment.

In figure 4.4b we simulate the conductance for a radial potential with $A = 0.11$ eV and $b = 2.75$, which gives a reasonable match to the experimental conductance in figure 4.4a. This matching suggests that $V_g = 0$ V corresponds to a chemical potential of about 140 meV in this device, and that the gate range of ± 3 V corresponds to an energy shift of

about 70 meV. This can be crudely checked by estimating the gate modulation of carrier density via the expression $\Delta n = \frac{C_g}{\mathcal{A}eL}\Delta V_g$, where n is carrier density and $\mathcal{A}$ is the cross-sectional area. C_g is the geometric gate capacitance which we estimate as 8.6 aF for this device. The gate range of 6 V corresponds to $\Delta n = 3.55 \times 10^{-17}$ cm^{-3}. Alternatively, the dependence of n on chemical potential ϵ can be calculated in the diffusive regime. Here we use an expression for carrier concentration appropriate to a nanowire with transverse subbands: $n(\epsilon) = \frac{\sqrt{2m^* k_B T}}{\hbar \pi \mathcal{A}} \sum_i F_{-1/2}(\frac{\epsilon - E_i}{k_B T})$ [96], where k_B is the Boltzmann constant, $F_{-1/2}$ is the Fermi Dirac integral of order -1/2, and E_i are the subband energies below ϵ. The range of ϵ shown in figure 4.4b corresponds to $\Delta n = 1.28 \times 10^{-17}$ cm^{-3}, which is only 0.36 times the value estimated from gate capacitance. However, these quantities are of the same order, and we have not taken into account gate screening in the short channel device that would lower C_g and reduce $\Delta n/\Delta V_g$. The experimentally observed change in conductance $\Delta G \approx 1.6 \times 2e^2/h$ over the 6V gate range is consistent with reasonable values for the chemical potential and the effective mean free path in a diffusive transport picture. Using 6V$= \Delta V_g = \frac{L^2}{C_g \mu}\Delta G$, we obtain an effective mobility $\mu = 960$ cm^{2}V^{-1}s^{-1}, corresponding to a mean free path $\lambda = 18$ nm when setting $\epsilon = 0.14$ eV. Taking into account gate screening by the contacts and/or mobile charges associated with the oxide or interfaces would decrease C_g, implying larger values for mobility and mean free path.

For transport through many modes in a phase coherent conductor, quantum interference effects can lead to a non-negligible contribution to conductance. If a system is in the weakly localized regime such that $NL_0 \gtrsim L$, the total conductance can be approximated as $G = (2e^2/h)N^2 L_0^2/(NL_0 L + L^2)$ [95]. This approximation requires a 1D system where backscattering is dominant over interband scattering, and that the transmission probabilities of each subband are equal. The nanowire studied here satisfies the first assumption since it is a quasi-1D system, where the large separation in subband energies will strongly suppress interband scattering. This claim is confirmed numerically by calculating the scattering rates between different subbands caused by a perturbing potential. From previous studies of nanowire conduction we have shown that Coulomb scattering dominates at low temperature [96], therefore the scattering rate is calculated using the Coulomb potential of a random assembly of charges at the nanowire surface. When the number of charges is selected to correspond to a surface charge density of 10^{12} cm^{-2}, interband scattering is indeed suppressed by several orders of magnitude compared to back scattering. Additionally, using this method we find that the greatest difference in back scattering rates of all subbands shown in figure 4.4b at k=0 is only 2%, validating the assumption that each subband has the same transmission probability. Simulation of planar defects to mimic the effects of stacking faults yield similar results. Back scattering being dominant over interband scattering is important since it means that even though the electron scatters several

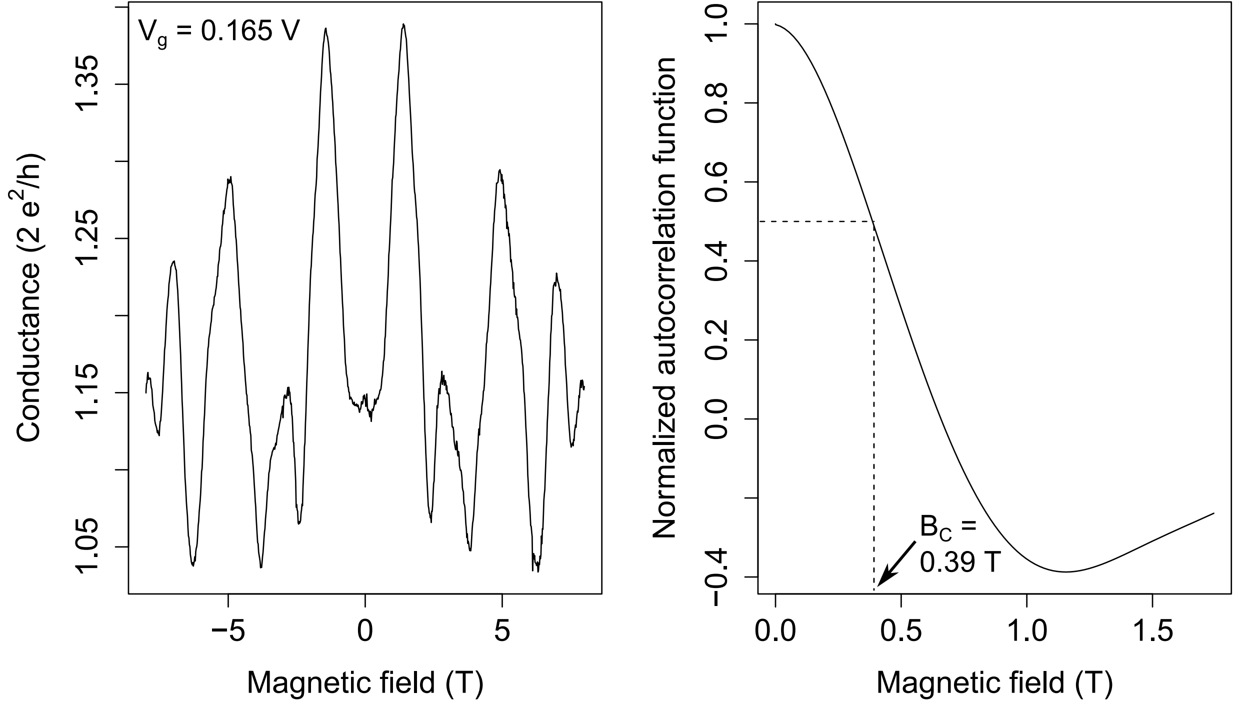

Figure 4.5: (a) A single experimental magnetoconductance trace from figure 4.4a when $V_g = 0.165$. (b) Normalized autocorrelation function of the data shown in (a) calculated using equation 4.3. The dashed lines show the position where the autocorrelation function is half of its maximum value, and the corresponding correlation field B_C. $B_C = 0.39$ T corresponds to $L_\phi = 365$ nm.

times along the nanowire, it generally stays in the same subband. Therefore scattering will lower the overall conductance, but the effects of subband occupation should still be visible in the conductance data. Finally, this device satisfies the weak localization criterion that $NL_0 \gtrsim L$ for the majority of the conductance range, since the simulation shows between 9 and 24 energy levels are occupied and we expect a mean free path of ~ 18 nm. Using the equation for conductance, an excellent match to the experimental conductance range is found for $L_0 = 20$ nm. This agrees well with the 18 nm predicted above, and is close to the lower end of the mean free path range $\lambda \approx 35 \pm 13$ nm obtained from mobility measurements on many nanowires from the same growth batch.

The present model does not include mesoscopic interference effects such as Aharanov-Bohm (AB) and Altshuler-Aronov-Spivak (AAS) oscillations [93, 94] that apply to the case of cylindrical shell conduction. Indeed, a phase coherence length $L_\phi \approx 275$ nm $> L$

is estimated for this device based on an analysis of the autocorrelation function of magnetoconductance fluctuations [88]. The autocorrelation function is calculated from magnetoconductance $G(B)$ at a fixed gate voltage using:[88]

$$F(\Delta B) = \langle \delta G(B + \Delta B) \delta G(B) \rangle \quad (4.3)$$

where $\langle ... \rangle$ denotes an average over all magnetic field points B, and $\delta G(B) = G(B) - \langle G(B) \rangle$. An example of experimental magnetoconductance and the resulting autocorrelation function are shown in figure 4.5. Once the autocorrelation function is calculated the correlation field B_C can be extracted using: $F(B_C) = \frac{1}{2}F(0)$. The phase coherence length can then be found using: $L_\phi = \sqrt{4\pi\Phi_0/B_C}$. With this technique, we obtained similar values of L_ϕ for several other FETs fabricated with nanowires from the same batch. While the AB effect is suppressed by disorder, the AAS effect should survive and exhibit conductance oscillations with a period of $\Phi_0/2$. However, these effects are most clear and strong in the limiting case of shell conduction at a fixed radius, where all electronic states enclose the same flux. Our results suggest intermediate band bending in this device and therefore a distribution of effective radii, which is expected to strongly attenuate AAS oscillations. Also, the AAS effect should produce oscillations whose phase is independent of the chemical potential (gate voltage), and no such gate-independent oscillation is visible in the conductance data.

4.4 Conclusion

This chapter has described a model of magnetoconductance based on the energy spectra of transverse electronic states in a semiconductor nanowire. It extends previous work in this area to examine the contrasting effects of weak and strong surface band bending on the patterns of conductance versus magnetic field and gate voltage. Conductance features from experiments on an InAs nanowire were shown to be consistent with the model, and provide a plausible match to specific subbands, although this assignment is by no means definitive. Interestingly, even though the device is in the weakly localized regime, characterized by multiple scattering events, back scattering is found to dominate over interband scattering such that the picture of subband occupation is still valid. We propose that in a quasi-ballistic system, quantitative analysis of these conductance patterns using a method akin to the $d_{i,i+1}/s_j$ ratios described above will allow unambiguous identification of the subbands participating in transport. It will also determine, to a degree consistent with the quality of the data, the radial potential $V(r)$. Cleaner transport can be achieved either

by using materials with higher mobility, such as InSb [97], using core/shell nanowires with lower defect densities than the one examined here, or by fabricating even shorter channels. There are two caveats to further shortening the channel: it will produce quantization in the axial direction, which complicates the conductance calculation, and it will increase gate screening by the nanowire contacts, which reduces the effectiveness of the gate in modulating the chemical potential. Including Zeeman and spin-orbit effects in the model is straightforward [13], and would improve agreement with experiment at high magnetic fields. It will also provide a method for measuring the subband-specific magnitudes of the g-factor and the spin-orbit coupling, assuming the subband splittings due to these effects are visible. Inclusion of the potential asymmetry due to a backgate geometry in numerical simulations is also straightforward, although we estimate this asymmetry to make only a small correction to the surface potential when the gate oxide is sufficiently thick. Accurate understanding of the radial potential and subband structure has implications for controlling surface scattering and tuning the number of modes participating in transport, leading to a better control of nanowire device properties.

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Chapter 5

Electrical characterization of chemical and dielectric passivation of InAs nanowires

Chapter contributions: Device fabrication, cryogenic measurements, and data analysis were performed by Gregory Holloway.

5.1 Introduction

Semiconducting nanowires offer a promising platform for a number of electronic and optoelectronic applications, including quantum information processing devices such as spin qubits [98, 31], topological qubits [70, 99, 100], and on-demand single photon generation [101, 102]. In particular, realization of spin qubits with fully-electrical control can be achieved in materials with a strong spin-orbit coupling by confining single electrons in electrostatically defined quantum dots [103, 82, 32]. While prototypical devices have demonstrated the fundamentals of this implementation [98, 31, 104, 105, 33], further engineering is desirable to improve the reproducibility (less wire to wire variation), the tunability and stability of the electrostatic potential. Fluctuations in the electrostatic potential are largely due to charge traps located at the nanowire surface or in the native oxide layer [65, 106]. Chemical passivation, in which a layer of atoms or molecules is covalently bonded to the semiconductor surface, is one method to prevent the oxide from forming and to passivate surface states. Sulfur atoms and sulfur-functionalized molecules are effective at passivating

III-V surfaces [107, 108], but tend to decay over a few days or weeks in ambient conditions, making them impractical as a permanent solution [27]. Another method to decouple charge noise in planar structures is to bury the active layer under buffer layers such that the surface is well separated from the active region [109, 110]. This idea has been applied, with some success, to nanowires by growing an epitaxial shell of a larger band-gap III-V material around the nanowire [43, 91]. However, the complex growth kinetics of the shell and multiple side facets limit the number of materials that will grow uniformly around the nanowire. Alternatively, one could deposit a dielectric shell around the nanowire using a conformal deposition technique such as atomic layer deposition (ALD) or plasma enhanced chemical vapor deposition (PECVD). In addition to protecting the nanowire surface from oxidation, these dielectric layers have the advantage of high breakdown voltage and a high dielectric constant, so that metal gates can be deposited directly onto the shell. This provides excellent capacitive coupling for devices such as transistors and gate-defined quantum dots.

While a dielectric shell appears to be a promising solution to this problem, care must be taken to prepare the nanowire surface prior to deposition of the shell to ensure a low defect interface between the two materials. Growth of the nanowire native oxide prior to deposition of the shell is expected to cause degradation of this interface. Here, we attempt to solve this problem by combining chemical passivation with deposition of a dielectric shell to realize a more stable transistor device. We survey a variety of passivation techniques by fabricating field effect transistors (FETs) using InAs nanowires that have undergone different combinations of chemical passivation and dielectric deposition. Cryogenic transport measurements were performed on each set of FETs to quantify their electronic properties and stability. As a practical test of these surface processing techniques, the most promising set of nanowires were used to fabricate a top-gated nanowire transistor, in which an electrostatically defined double quantum dot was successfully realized.

5.2 Experimental Details

Undoped InAs nanowires were grown by vapor-liquid-solid growth from gold seed particles in a gas source molecular beam expitaxy (MBE) system[1]. The GaAs (111)B growth substrate was prepared by depositing a 1 nm thick Au film, and then heating it in situ in the

[1] Nanowires are grown by Chris Haapamaki in Ray LaPierre's group at the Centre for Emerging Device Technologies at McMaster University, Hamilton, Ontario, Canada. Technical assistance with the MBE was provided by Sharam Tavakoli. TEM images presented in this chapter were taken by Paul Kuyanov a member of the same group

MBE to form nanoparticles. For nanowire growth, In atoms were supplied as monomers from an effusion cell, and As_2 dimers were supplied from an AsH_3 gas cracker operating at 950 °C. Nanowire growth was carried out at a substrate temperature of 420 °C, an In impingement rate of 0.5 μm/hr, and a V/III flux ratio of 4. Nanowires typically had a diameter of $\sim$ 20 - 80 nm that was roughly equal to the Au nanoparticle diameter at the top of each nanowire, indicating negligible sidewall deposition. Transmission electron microscopy has shown these nanowires to have minimal stacking faults and a wurtzite crystalline structure [96]. Suppression of stacking faults was achieved by growing nanowires at a low growth rate of $\sim$ 0.5 μm/hr [46].

Chemical passivation and deposition of the dielectric shell were performed on the nanowires while still on the growth substrate, so that all facets of the nanowire were exposed equally. Three surface treatments were implemented: a hydrofluoric acid (HF) dip, octadecanethiol (ODT) passivation [111, 81, 112], and thermal oxide (ThO) growth. In addition to performing each process individually, sequential implementations were carried out. In all cases, the time between subsequent surface treatments and the time prior to deposition of the dielectric was minimized to suppress native oxide regrowth; the average time between the end of treatment and reaching a high vacuum environment in the dielectric deposition chamber was $\sim 3 - 4$ minutes.

The HF dip was a 5 second dip in a buffered oxide etchant (BOE) consisting of a 10:1 mixture of NH_4F and HF. Following etching, the substrate was rinsed for 2 minutes in deionized water. The purpose of the HF etch was to remove the native oxide from the nanowire surface. Of course, without a subsequent passivation step, the oxide will quickly regrow when the nanowires are exposed to air. Hence, the HF dip served mostly as a cleaning step prior to other steps. The molecule ODT was used to passivate the nanowire surface since it consists of a long carbon chain connected to a thiol group which readily bonds to InAs. Under appropriate conditions, these molecules will form a self-assembled monolayer on the nanowire surface, passivating it and preventing oxidation for days or weeks [111, 81, 112]. The deposition of the self assembled monolayer was achieved by placing the nanowire substrate in a 5 mmol/L solution of ODT in isopropyl alcohol (IPA). Once in solution, the container was sealed with Parafilm and heated to 60 °C for 1 hour. Following the deposition, the substrate was rinsed for 30 seconds in clean, room temperature isopropyl alcohol (IPA), and then dried with nitrogen. The effectiveness of this method was confirmed by performing contact angle measurements (using a drop of deionized water) on planar InAs substrates. Samples treated with ODT showed a contact angle of 105 degrees, substantially larger than the contact angle of 55 degrees measured on untreated pieces.

The increase in contact angle shows that a hydrophobic surface was created, consistent with a well-formed ODT layer.

Growth of a thermal oxide was carried out in a rapid thermal annealing system with the growth substrate seated in a graphite susceptor. The oxidation process consisted of a 30 second ramp to 300 °C in nitrogen, followed by a 2 minute period at 300 °C in 5 slpm of oxygen, and finally a 5 min ramp down to room temperature, again in nitrogen. The process was calibrated by oxide growth and measurement on a bulk InAs substrate to grow an oxide $\sim$ 2 nm thick. Following the thermal oxidation process, a representative nanowire was inspected with TEM and showed a uniform oxide with a thickness of 1.8 nm. The motivation for testing this process was to grow a denser, more uniform oxide compared to the native oxide, to possibly reduce the densities of defects and charge traps. Such a thermal oxide has been reported to improve mobilities in nanoribbons [113].

Two different dielectric layers were studied in this work: SiN_x deposited by PECVD and Al_2O_3 deposited by ALD. Both deposition systems were connected to a load lock, allowing the growth substrates to be quickly placed in vacuum, minimizing oxide growth prior to the deposition. The PECVD was carried out at 330 °C in 30 sccm of silane and 900 sccm of nitrogen. A 20 nm thick layer of SiN_x was grown by applying 40 W RF plasma for 65 seconds. ALD took place at 300 °C using a trimethyl aluminum precursor and a pulsed 300 W RF plasma. Each deposition cycle grows 1 Å of material, and was carried out for 200 cycles to produce a 20 nm thick film. Following deposition, the substrates were removed from the system and cooled to room temperature prior to further device processing. A TEM image of a nanowire treated with HF, ODT, and covered in an Al_2O_3 shell is shown in figure 5.1a. The amorphous Al_2O_3 shell has a thickness of $\sim$ 20 nm as expected, and is clearly distinct from the crystalline InAs core.

Once all desired surface treatments and depositions were performed on a set of nanowires, they were transferred to device substrates by dry deposition. Device substrates consisted of a 300 nm thick layer of thermally grown SiO_2 on degenerately doped Si. Deposited nanowires were located relative to pre-patterned alignment markers using SEM, and source drain contacts were written in PMMA resist using electron beam lithography. Patterns were designed to produce contacts that were 1 μm wide with channel lengths of either 500 nm or 1 μm. After pattern development, the devices were etched in buffered oxide etchant (BOE) to remove the shell material in the contact area and ensure ohmic contacts. The duration of the BOE step was dependent on the shell material: nanowires with no shell were etched for 5 seconds, those with an Al_2O_3 shell for 20 seconds, and those with a SiN_x

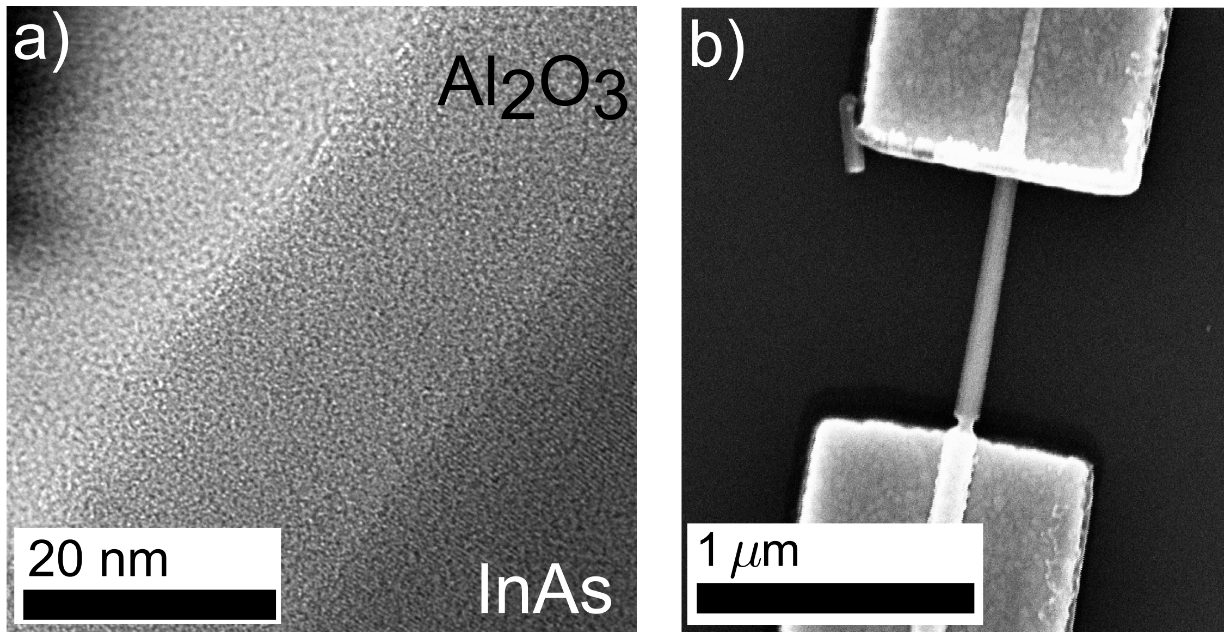

Figure 5.1: (a) TEM image of a nanowire treated with HF, ODT, and covered in an Al_2O_3 shell. The amorphous Al_2O_3 layer is clearly visible around the crystalline InAs core. (b) SEM image of an FET fabricated using a nanowire treated with HF, ODT, and covered in a SiN_x shell. A small section of the shell is unintentionally removed from the channel region near the lower contact, due to lateral etching of the shell material in BOE.

shell for 30 seconds. The etch times were chosen to be 20% longer than the time necessary to remove the same thickness of dielectric from a planar substrate. This helped ensure that the shell was removed from all sides of the nanowire, and had little effect on the nanowire itself, since InAs shows negligible etching in HF. Following the contact etching, the devices were rinsed in deionized water and transferred to a metal evaporation system in less than 3 minutes from leaving the etching solution (pump down time $\sim$ 8 minutes). To remove any oxide that formed during the interim, the devices were exposed to a gentle Ar ion plasma for 10 minutes immediately prior to deposition of 30/50 nm of Ti/Au. We find this ion milling to be crucial to achieving reproducible ohmic contacts. An SEM image of a typical nanowire FET is shown in figure 5.1b.

Current-voltage (I-V) measurement of the FETs was carried out in a pumped liquid helium cryostat with a variable temperature controller, allowing temperatures ranging from room temperature to a base of $\sim$ 1.5 K. DC electrical characterization was performed in

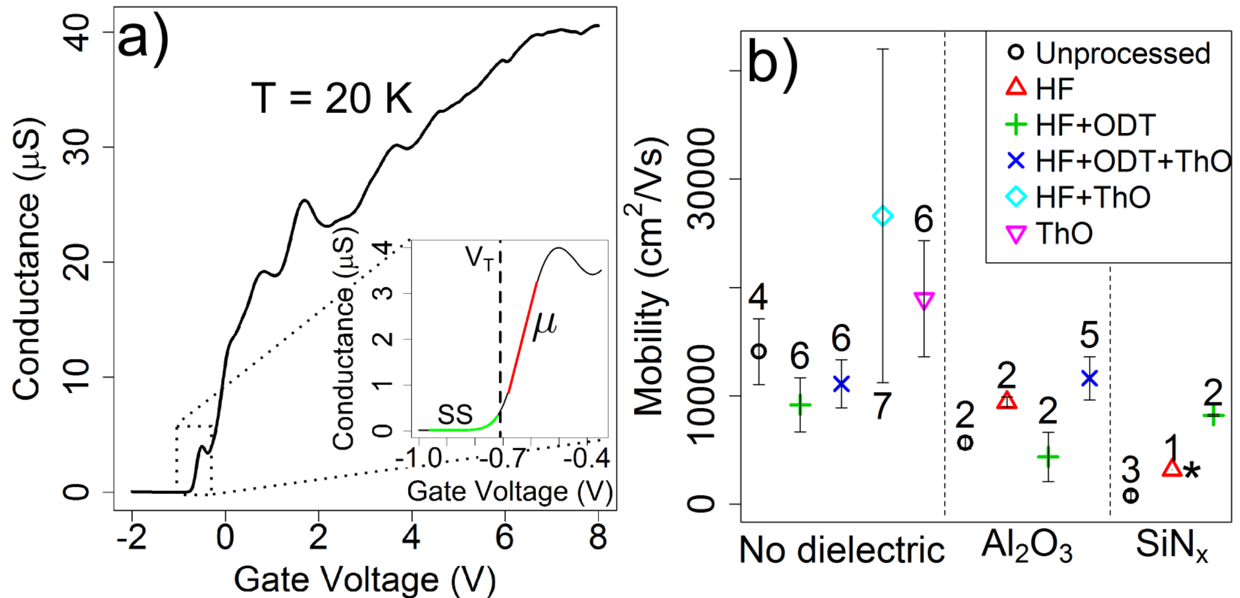

Figure 5.2: (a) Conductance as a function of gate voltage for a representative nanowire FET at 20 K, and a source-drain bias of 1 mV. This was a bare nanowire, with no treatment and no dielectric shell. The inset shows conductance near pinch off, where the black dashed line shows the threshold voltage, and the red and green lines highlight the sections used to extract peak mobility and subthreshold swing, respectively. (b) Average field effect mobility (μ_{fe}) of nanowire FETs that have undergone different surface processing steps. HF denotes hydrofluoric acid, ODT denotes octadecanthiol, and ThO denotes thermal oxide. The details of each process are described in the main text. Each data point corresponds to the field effect mobility averaged over all devices within a particular surface treatment set, and the number above or below the point indicates the total number of devices in each set. Devices are segregated along the x-axis by their dielectric shell, and the processes prior to shell deposition are indicated by corresponding symbols. Error bars reflect the standard error of the mobility values in each set. The lack of an error bar on the set containing only a single data point, and denoted by the asterisk, does not indicate a point with zero uncertainty. Rather, it indicates that there is no distribution of points for this set since it contains only one point.

a two-probe configuration using a home-built voltage source and DL Instruments current-voltage preamplifier. FET conductance was modulated by applying a voltage to the degenerately doped silicon substrate that acted as a global back-gate.

5.3 Results

A typical transconductance curve of a FET measured at 20 K is shown in figure 5.2a (bias voltage = 1 mV). The conductance generally increases with applied gate voltage, but shows a few dips which are absent at higher temperatures and are likely due to electron-electron Coulomb interactions and weak localization of charge. To characterize the nanowire channels, field effect mobility was estimated from the transconductance data using the formula [96]:

$$\mu_{\mathrm{fe}} = \frac{L^2}{C_g}\frac{dG}{dV_g} \tag{5.1}$$

where L is the channel length, G is conductance, and V_g is the gate voltage. The gate capacitance, C_g, is estimated using a finite element model (COMSOL Multiphysics) of the nanowire FET geometry to include the effects of contact screening. If the contact screening is not taken into account, mobility values for shorter channel FETs are found to be significantly lower than those of similar long channel devices. When contact screening is included, the mobility spread between different channel lengths is effectively removed, allowing for a fair comparison between different FET geometries. The effect of the dielectric shell is neglected in these calculations, as our simulations show it only changes the total gate capacitance by $\leq 3\%$. Prior to taking the derivative of the conductance, the data was smoothed using a Gaussian moving average with a standard deviation of 10 mV. Since the calculated mobility varies as a function of gate voltage, the highest extracted value is taken as an estimate of the intrinsic mobility. The inset in figure 5.2a shows conductance near pinch off, where a red line has been fit to the section of the curve with the highest slope, and thus the peak mobility. For this particular device, the peak mobility occurs just above the threshold voltage, but in other devices this is not always the case. This measurement was performed at 20 K, since previous studies have shown that mobility increases at low temperatures, but below 20 K we find that mesoscopic conductance effects become prominent and lead to inaccurate mobility estimates.

At low temperature, it has been suggested that mobility in fault-free InAs nanowires is dominated by ionized impurity scattering from surface sites [96] or surface roughness [34]. A lower value of mobility at 20 K should therefore indicate stronger surface scattering of free electrons. Comparing the mobility estimates across surface processes can therefore give some insight into how each process affects the nanowire surface and/or surface states. Figure ch6fig1bb shows the average peak mobility across several devices for each process;

each point corresponds to a different combination of surface processing steps. FETs are separated along the x-axis by the dielectric shell material, and the symbol for each point denotes the chemical passivation that was carried out prior to shell deposition. One noticeable trend is a decrease in mobility when a dielectric shell is added to the bare nanowire (black circles). This could be due to the formation of defects at the interface between the nanowire's native oxide and the dielectric material. Focusing on nanowires that underwent ODT passivation with no dielectric shell added, we do not see sizeable increases in mobility, as one might expect from removing the native oxide. This could indicate that the ODT layer is ineffective at removing the sources of scattering, the ODT monolayer was incomplete or ill-formed, or it is short-lived such that it decays over the few days between fabrication and measurement. The nanowires with a dielectric shell can provide some insight, since the shell should encase the nanowire and prevent further changes to the nanowire surface. Interestingly, an increase in mobility is generally observed when a surface treatment is performed on the nanowire prior to deposition of the shell. These mobilities never exceed that of the unprocessed bare wires, but are somewhat better than those obtained when depositing dielectric on an unprocessed nanowire.

Further understanding of the nanowire/dielectric interface can be gained by looking at the subthreshold swing. The subthreshold swing is a measure of the change in gate voltage needed to drop the current in a transistor by one decade in the region below the threshold voltage. This part of the conductance curve is highlighted in green in the inset of figure 5.2a. Subthreshold swing was estimated using the formula: $SS = (d\log(I)/dV_g)^{-1}$. Figure 5.3a shows the value of subthreshold swing as a function of temperature for one device. Above 20 K, the subthreshold swing increases roughly linearly as a function of temperature, as predicted by the following equation [114]:

$$SS = ln(10) \times (k_B T/q)(1 + C_t/C_g) \tag{5.2}$$

where k_B is the Boltzmann constant, T is temperature, q is the electron charge, and C_t is the capacitance due to interface traps and should be proportional to the density of these traps. The change in subthreshold swing versus temperature can be used as a measure of the relative density of interface traps. The solid line in figure 5.3a shows the fit of equation 5.2 to the experimental data. The disagreement below 20 K is likely due to localization and Coulomb blockade effects, which dominate the device conductance at low temperatures and lead to deviations from expected subthreshold swing behavior.

To compare the temperature dependence of the subthreshold swing across different pro-

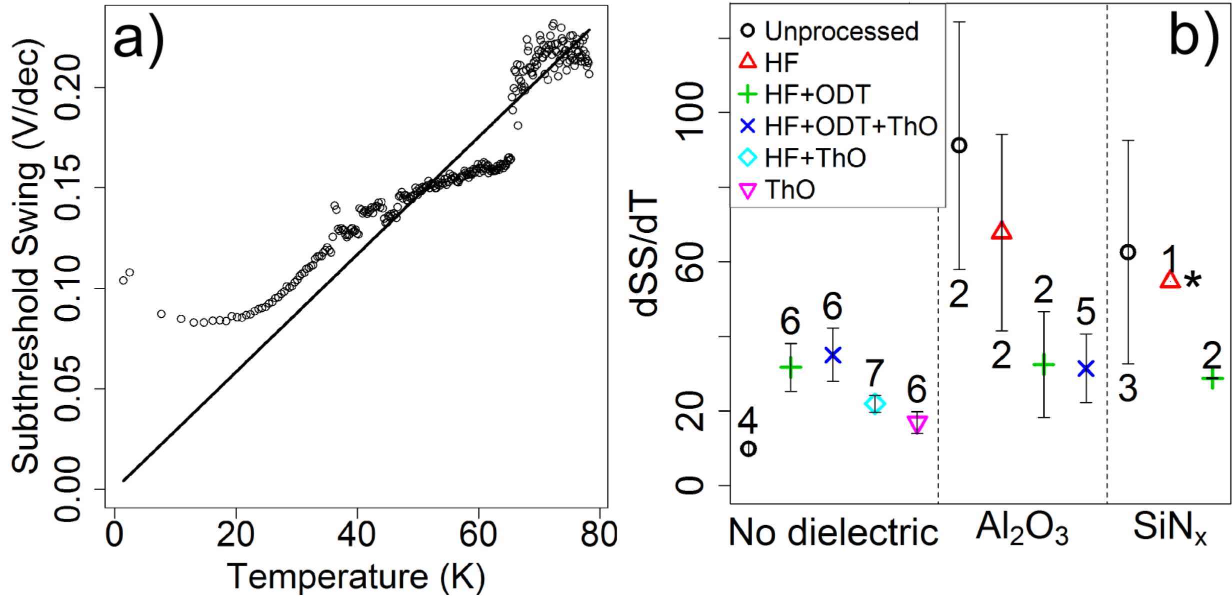

Figure 5.3: (a) Subthreshold swing (SS) as a function of temperature (T) for an InAs nanowire FET (bare nanowire with no surface processing). Each data set shows a roughly linear temperature dependence, indicated by the linear fit (solid line) in the plot. This line is a fit to equation 5.2 to determine C_t. (b) Average dSS/dT value across different surface processing techniques. The plot has the same layout as figure 5.2b. Note that the jumps observed in the data of (a) are due to slow charge fluctuations in a single trap somewhere near the device channel, i.e. random telegraph noise.

cesses, the value of $dSS/dT = (1 + C_t/C_g)$ is extracted for each device, and the average for each process is plotted in figure 5.3b. Higher values in this plot correspond to larger values of C_t, which suggest a larger density of interface traps. The value of dSS/dT for the different processes follows similar trends to the mobility data shown in figure 5.2b. Most notably, when a dielectric shell is added to a bare nanowire, the density of interface traps increases dramatically. However, by passivating the nanowire surface prior to the dielectric deposition, the density of interface traps can be made comparable to the value seen in wires with no dielectric shell. When looking at dSS/dT for nanowires with no dielectric shell, the unprocessed devices have the lowest value, followed by the thermal oxide devices. This suggests that the surface processing, particularly HF and ODT treatments, lead to an increase in the density of interface traps. On the other hand, these same processes appear to be essential in reducing the trap densities when the dielectric shell is added.

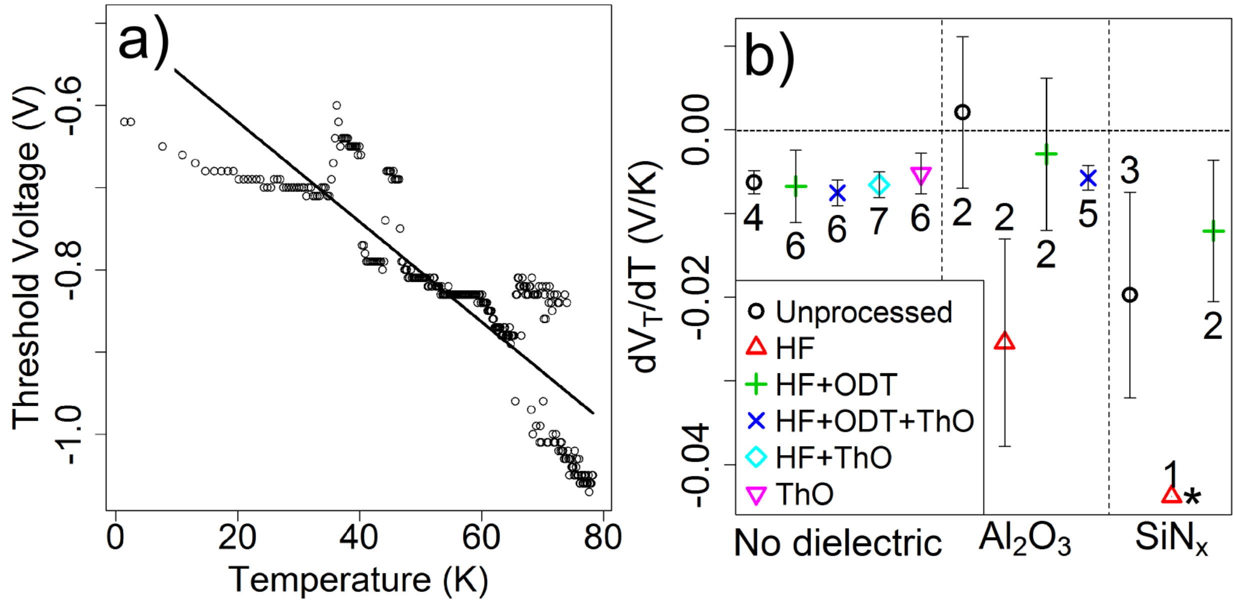

Figure 5.4: (a) Temperature dependence of threshold voltage (V_T) for an InAs nanowire FET (same nanowire as shown in 5.3). Here, the data is fit using a least squares fit whose slope is related to the density of donor-like states in the nanowire. (b) Average dV_T/dT values across different surface processing techniques. Plots have the same layout as figure 5.2b. Note that most points are located near zero indicating a low density of donor-like states, except for the nanowires treated with HF only, which show a much higher negative value of dV_T/dT indicating a higher density of donor-like states. The jumps observed in the data of (a) are due to slow charge fluctuations in a single trap somewhere near the device channel, i.e. random telegraph noise.

The threshold voltage versus temperature is shown for one device in figure 5.4a. Threshold voltage is found to decrease roughly linearly as temperature is increased. This is ascribed to thermal activation of donor-like surface states in the nanowire [55]. As temperature increases and more donor-like states become ionized, a more negative gate voltage is required to deplete the nanowire of carriers. The slope of the threshold voltage versus temperature can therefore be used as a rough indication of the surface density of donor-like states. This value is measured by fitting the temperature dependence of the threshold voltage to a linear fit as shown by the solid line in figure 5.4a. The slopes of these lines are averaged across each process and plotted in figure 5.4b. Here, the nanowires with no dielectric shell show a similar value of dV_T/dT independent of the surface process. When a dielectric shell is added the values of dV_T/dT are more spread out with no obvious trend

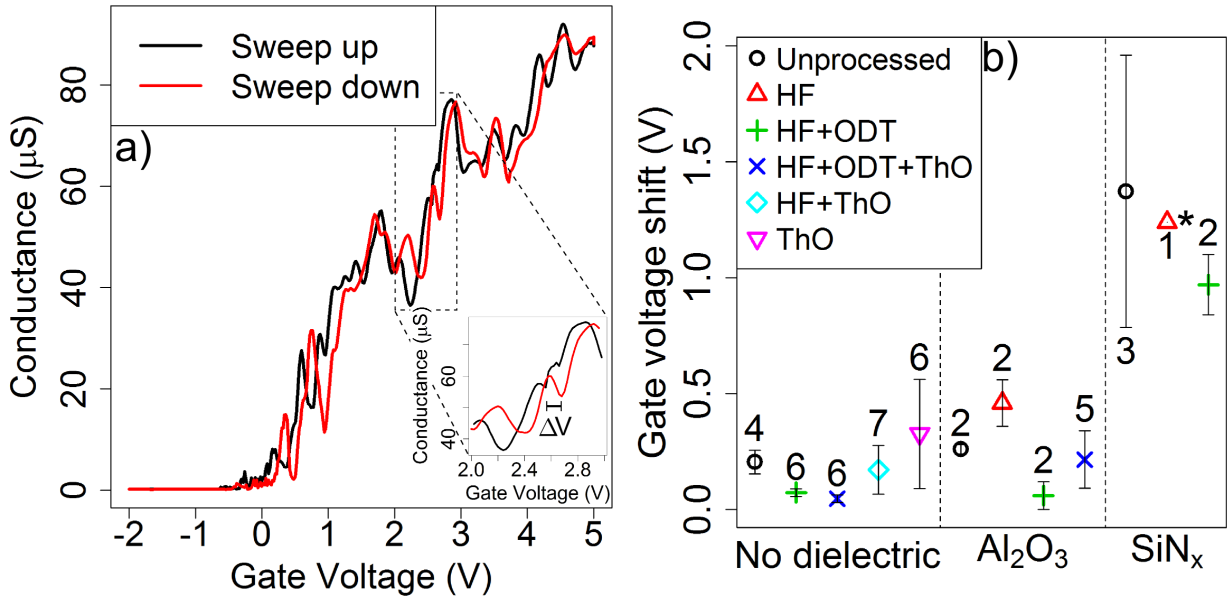

Figure 5.5: (a) Conductance of a FET at 1.4 K measured by sweeping the gate voltage up, waiting for 45 s, and then sweeping back down. This particular nanowire was treated with HF, ODT and had a thermal oxide, but no deposited dielectric. Changes in the trapped charge population cause a hysteretic behavior such that the two curves have a relative gate voltage shift. The inset shows a magnified portion of the conductance curve and the gate voltage shift ΔV. (b) Average gate voltage shift at 1.4 K for different surface processes, following the same layout as figure 5.2b.

apparent. The exception to this is the nanowires treated with only HF prior to the dielectric deposition, which have a much larger value of dV_T/dT. This suggests that the HF etch modifies the surface chemistry leaving an increased density of donor-like states, and may be related to hydrogen passivation.

The density of charge traps in the FET channel can also be estimated by looking at hysteresis of the conductance curve when sweeping the gate voltage in different directions. This hysteresis is due to the gate voltage modulating the occupation of charge traps [55, 106]. Figure 5.5b shows the hysteresis in FET conductance measured at 1.4 K with a gate voltage sweep rate of 90 mV/s. The inset shows a portion of the conductance curve, where the gate voltage shift ΔV is indicated. The shift is expected to be towards more positive gate voltages when first sweep is up (to positive voltages) and the second sweep is down. This is because just prior to the sweep down, the gate voltage is very positive which

fills traps with electrons, and these electrons contribute to an increased negative potential. A more positive gate voltage is then required to cancel out this potential, shifting the conductance curve to more positive values. Figure 5.5 shows that the data agrees with this expectation.

The magnitude of the relative gate voltage shift between the sweep up and sweep down curve, ΔV, is an indicator of the density of charge traps. Note that charge traps are not necessarily in the nanowire or its surface, but could be in the dielectric shell or SiO_2 substrate, as long as they are close enough to affect the electrostatic potential in the nanowire and thus its conductance. The average gate voltage shifts measured at a temperature of 1.4 K for the different surface processes are shown in figure 5.5b. Interestingly, it appears that SiN_x has a higher density of traps than either Al_2O_3 or no dielectric. While the surface passivation techniques may slightly lower the trap density for the nanowires with SiN_x, it is still much higher than in the other devices. This suggests that the SiN_x itself likely contains a high density of traps. Conversely, there is not much difference between gate voltage shifts seen in the nanowires with Al_2O_3 and no dielectric shell, indicating that the Al_2O_3 shell is not a major source of charge traps. In all cases, the ODT appears to reduce the trap density. Among the devices treated with ODT, those with no dielectric shell and with Al_2O_3 shell show less hysteresis than untreated nanowires, indicating that ODT could be removing traps at the nanowire surface.

To test the viability of using these nanowires for realizing quantum devices, FETs were fabricated with local top gates which could be used to form an electrostatically defined double quantum dot. Nanowires treated with a combination of ODT and Al_2O_3 were used for this test, since the results presented above suggested that they showed the best overall characteristics among those devices with a dielectric shell. A schematic of a 5-gated device is shown in figure 5.6a. In this case, a thinner dielectric shell of only 8 nm was used to increase the capacitive coupling between the nanowire and the local top gates. Nanowires were deposited onto substrates that had been pre-patterned with a series of parallel trenches with a width of 70 nm and a depth of 60 nm, made by reactive ion etching of the SiO_2 substrate. Sonicating the substrates for 10 s in acetone following the nanowire deposition increased the number of nanowires in trenches, and simultaneously removed many nanowires not located in trenches (the latter is helpful to prevent stray nanowires from causing breaks or other problems with metal traces connecting the device to bonding pads). Entrenched nanowires were patterned in two electron beam lithography steps to create ohmic source/drain contacts and capacitively coupled top gates, both using Ti/Au metal stacks. Ohmic contacts were made the same way as the previous FETs, using

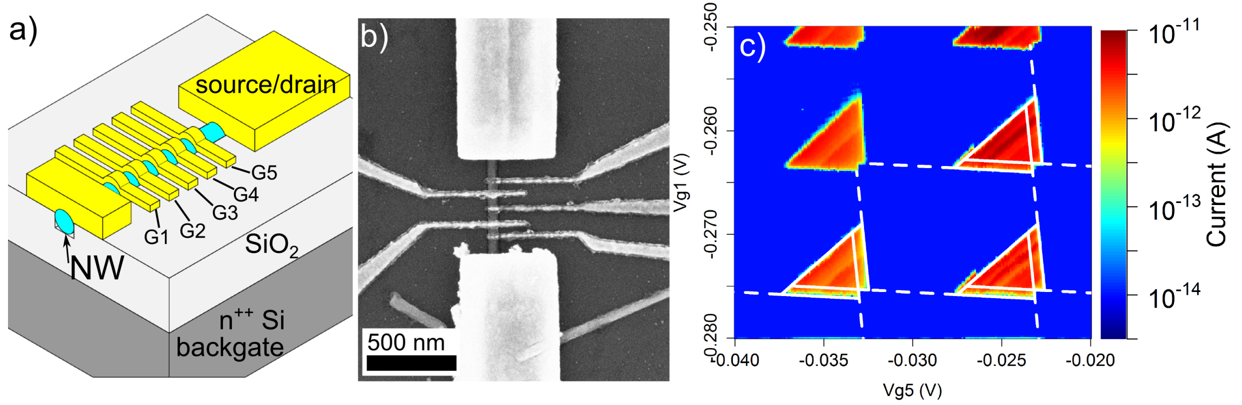

Figure 5.6: (a) Schematic of the entrenched, top-gated nanowire device for making an electrostatically defined double quantum dot. The trench geometry allows the top gates to partially wrap around the nanowire while keeping the height profile relatively flat, allowing for fine gates of the desired width (40 nm) and pitch (80 nm). It also allows for global back-gating to tune the carrier density in the nanowire prior to forming barriers and dots. (b) SEM image of a top-gated nanowire FET with dimensions similar to the device studied here. (c) Charge stability diagram, measured at 25 mK and a bias of 2 mV, showing bias triangles that signify double quantum dot transport. The double dot is formed by defining tunnel barriers with gates 1,3, and 5. Here, the electron number in each dot is modulated by sweeping gates 1 and 5. Regions of low current correspond to fixed charge on the two dots. White dashed lines correspond to the best fit of the data to a simple capacitive model [15]; the charging energies are 4.5 meV and 4.2 meV for the dots near gate 1 and 5, respectively. The corresponding lever arms for gates 1 and 5 are 0.31 and 0.46, respectively. The back gate voltage was +6 V in this example.

a short BOE dip to remove the dielectric shell. An SEM image of a completed top-gated nanowire FET is shown in figure 5.6b.

Our motivations for using the trench geometry are fourfold: (1) the flatter height profile of the top side of the nanowire with respect to the substrate allows for partial wrap-around gating while maintaining relatively fine widths and pitches (here we achieved 40 nm width and 80 nm pitch). In contrast, we find it impossible to achieve a similar width and pitch when the nanowire is not entrenched, due to a less favourable resist profile during the lithography step. (2) Gating is possible from both top and bottom of the nanowire, in

particular we have a global back gate acting from the bottom. This allows for tuning the carrier density to a desired value before using the top gates in depletion mode to form barriers and dots, which in turn allows us to even use nanowires that are normally pinched off at zero back gate voltage. Also, the fact that the nanowire is surrounded on three sides by SiO_2 increases the efficiency of the back gate. (3) The nanowire orientation is predefined by the trench alignment, which is very useful when aligning the device to a magnetic field, for example. (4) As mentioned above, sonication allows for the number of stray nanowires not in trenches to be reduced, which is helpful for the device processing. Potential disadvantages of this geometry include a reduced effective surface area for Ohmic contacting, and the possibility for charge noise due to defects in the etched SiO_2 sidewalls, however neither appears to be serious in the experimental results we present below.

The general strategy for tuning a double quantum dot was to increase the carrier concentration in the nanowire by applying a positive back gate voltage, followed by local depletion due to negative voltages applied to the fine gates to form tunnel barriers. The ability to change the nanowire potential using the global back gate is an important advantage this geometry has over devices which have only local bottom gates [31, 104, 105, 33], giving better overall electrostatic control. Gates 1, 3 and 5 are used to create a double-well potential. Figure 5.6c shows the current measured through a device as a function of the voltages on gates 1 and 5, at a lattice temperature of 25 mK and source-drain bias of 2 mV. This shows the characteristic bias triangles and honeycomb structure of a double quantum dot, which can be fit to a simple capacitive model [15]. The model fit is indicated by the white dashed line, and from it we extract dot charging energies of 4.5 meV and 4.2 meV. Ideally one would use gates 2 and 4 as plunger gates to control the electron number in each dot, however in this particular device, those gates were weakly coupled to the nanowire due to a defect in the lithography. The lever arm relating gate 1 to its adjacent dot, and gate 5 to its adjacent dot, are 0.31 and 0.46, respectively, indicating very good capacitive coupling. The high dielectric constant of the Al_2O_3 combined with the partial wrap-around geometry of the gates allows the double quantum dot to be easily formed and tuned with absolute local gate voltages well below 1 V (however in this example, the back gate voltage was +6 V). The data shown in figure 5.6c was acquired over a time scale of hours, and shows almost no charge noise, reinforcing the results of the FET measurements which suggested this surface treatment would minimize the number of charge traps. Overall, this device geometry along with the ODT and Al_2O_3 surface processing provide a promising pathway for future mesoscopic devices.

5.4 Discussion

Nanowires treated with HF, ODT, and Al_2O_3 were selected as the most promising candidates for realizing electrostatic quantum dots since they showed a consistently lower density of charge traps than nanowires treated with other surface processes. Despite this favorable charge noise behavior, these nanowires had a lower mobility than most other nanowires that were investigated. One possible explanation for this trend is that mobility is likely dominated by scattering from static scattering sites such as ionized impurities at the surface [96], or surface roughness [34]. Importantly, the state of these scatterers need not change with time to affect the mobility, it only matters that they are fixed near the conduction channel to act as scattering sites. This is unlike the dynamic behavior governing the other parameters studied here, where the occupation of charge traps must change to cause the observed effect. For example, gate voltage hysteresis requires traps to change from filled to emptied in order to shift the conductance curve. This suggests that while the HF, ODT, and Al_2O_3 combination is effective at removing defects which can act as dynamic charge traps, it may induce more static defects which can lead to lower mobility. While the removal of charge noise was deemed more important for realizing electrostatic quantum dot devices, other applications may favor a high mobility and would benefit more from one of the other surface treatments. Our results while limited, suggest that the thermal oxide may improve mobility, similar to previous findings on InAs nanoribbons. [113]

One of the motivations for using the dielectric shell was to encase the nanowire so that its electrical properties would remain constant over time and when exposed to ambient conditions. However, we observe that most devices still experience noticeable shifts in threshold voltage after extended periods in a nitrogen atmosphere or air, and this is typically reversible after pumping to a vacuum of ~ 0.1 mTorr for several hours. One possible explanation for this is that during the short HF (BOE) etch prior to Ohmic contacting, some lateral etching occurs so that a section of the nanowire channel adjacent to the contacts has its shell removed or partially etched, as shown near the lower contact in figure 5.1b. This bare region of the channel would be most sensitive to molecular adsorbates. It is also possible that adsorbed molecules on the shell surface transfer charge that affects the nanowire surface potential, however this seems an unlikely mechanism to yield an effect as strong as what is observed. We are exploring alternate techniques for removing the dielectric in the Ohmic regions to prevent this lateral removal of the shell.

The molecule chosen for chemical passivation of the nanowire surface was ODT, since it can provide one of the most stable self assembled monolayers on III-V materials. How-

ever, it can also be difficult to form a perfect monolayer at the surface, and some reports highlight the necessity of removing all oxygen from the system to achieve ideal passivation [81]. Therefore, it may be more practical to use an ammonium polysulfide process [108, 27] to passivate the surface with S atoms. While this S passivation does not last as long as ODT in ambient conditions, it is stable enough to prevent oxidation during a quick transfer to a dielectric deposition chamber, and is a simpler and potentially more reliable process than ODT passivation. While we observed the ODT step to improve the properties of nanowires that had a subsequent dielectric shell, we did not see noticeable improvements (e.g. in mobility) for nanowires with ODT only as compared to unprocessed nanowires. It would be interesting to see if replacing the ODT step with ammonium polysulfide has a noticeable effect on devices with or without a dielectric shell.

5.5 Conclusion

The effects of surface passivation and conformal dielectric deposition on the low temperature electronic properties of InAs nanowire FETs were investigated. It was found that deposition of a dielectric shell on unpassivated nanowires tended to degrade electronic performance, as quantified by mobility, threshold versus temperature, subthreshold swing and gate hysteresis. Al_2O_3, deposited by an ALD process, was found to be superior to PECVD SiN_x. Interestingly, chemical surface passivation prior to dielectric deposition was found to improve electronic performance, in particular nanowires treated with ODT followed by Al_2O_3 were found to have characteristics similar to unprocessed nanowires. This allows us to maintain the desired intrinsic properties of the nanowire, while encasing it in a conformal insulating high-k dielectric. The addition of this shell facilitated a novel entrenched top-gated device geometry which was used to demonstrate a stable, gate-defined double quantum dot. The dielectric shell improves gate control of the electrostatic potential in the nanowire, evidenced by the strong capacitive coupling between local gates and their adjacent dots. The ability to improve electrostatic control while maintaining intrinsic nanowire transport properties improves the viability of these nanowires as a platform for quantum device applications such as spin and topological qubits.

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Chapter 6

Si quantum dots

Chapter contributions: Device fabrication, cryogenic measurements, and data analysis were performed by Gregory Holloway. Theory for the double dot memristor was proposed by Ying Li, Simon C. Benjamin, G. Andrew D. Briggs, and Jan A. Mol at the Department of Materials, University of Oxford.

6.1 Introduction

Semiconductor quantum dot transistors have numerous applications including quantum information processing[115, 32], single electron pumps [116], and the study of topological materials[117, 118]. In many of these systems dots are defined electrostatically, allowing for greater tunability and control of the transport properties. While the GaAs heterostructures were the system of choice for many years [119, 120, 121], recently interest in Si has been growing due its low density of nuclear spins [122, 123, 124]. This absence of nuclear spins allows for improved electron spin coherence a key ingredient for spin-based quantum information processing. In particular, isotopically purified Si has been used to demonstrate electron spin coherence times of 28 ms[124]. Initial progress in spin control in Si was made using individual donor atoms, ion implanted into bulk Si[125, 126, 127, 123, 128]. These donors are ionized and the nuclear and electron spins are controlled using NMR and ESR respectively. More recently, electrostatic quantum dots have been realized in Si using either Si/Ge heterostructures [129, 130, 131] or Si metal-oxide-semiconductor (MOS) structures [132, 124, 133, 3, 134, 135, 136, 137, 138]. While Si/Ge heterostuctures tend to have superior transport properties[139], the material is expensive to produce requiring access to an molecular beam epitaxy system. On the other hand, Si MOS devices can be CMOS

compatible [122, 136, 138] allowing them to be fabricated in the current Si foundries for rapid scalability. Before either system can be scaled up, transport through these quantum dots must be thoroughly studied to understand the relevant transport phenomena. For example, it is currently unclear whether devices can be made to reproducibly reach the single electron regime, a necessary ingredient for spin-based quantum information processing.

Here, we study transport through a pair of capacitively coupled Si MOS quantum dots. This system provides a means to study charge transport through a single quantum dot revealing basic properties like the charging energy and tunneling rates into the dot. The second capacitively coupled dot is then used as a charge sensor to probe the state of the first dot, even when current through the first dot is suppressed. With this charge sensing technique, the electrostatic potential of the first dot is probed down to the single electron regime. Finally, the pair of dots is used to implement a novel quantum memristive system where transport through one dot shows hysteretic behavior dependent on the charge state of the other dot.

6.2 Experimental details

Devices were fabricated using undoped silicon with a thermal oxide of 12 nm. Ion implantation of phosphorus with an energy of 12 keV was performed through a photomask to create degenerately doped source drain contacts. Following implantation the resist mask was stripped, and the chip was annealed at 950 °C in N_2 to remove damage from the implantation process, and to activate the dopants. To prevent shorts between these ion implanted regions and subsequent metal gates, a 6 nm layer of Al_2O_3 was deposited by atomic layer deposition. Gates to define the quantum dots were then fabricated on the substrate using three layers of Al gates. Each gate layer was patterned using electron beam lithography with a PMMA mask, and Al was deposited using an electron beam evaporator with a deposition rate of 1 Å/s. Following liftoff of the excess metal, the devices were exposed to a 25 W O_2 plasma at 150 °C for two minutes to form an oxide layer at the metal surface. This oxide provides an insulating layer between different gate layers, and we find this process results in gate-gate breakdown voltage greater than 4 V. The first gate layer, shown in red in figure 6.1, is a screening layer which controls where subsequent gates will form an accumulation layer at the Si/SiO_2 interface. The screening gates define two horizontal channels with a separation of $\sim$ 140 nm. Layer two, shown in green, are the accumulation gates used to form the conducting channel between the dots and the source/drain contacts, as well as the plunger gates which control the chemical potentials of the dots. The blue layer is deposited last and is used to form tunnel barriers. After all

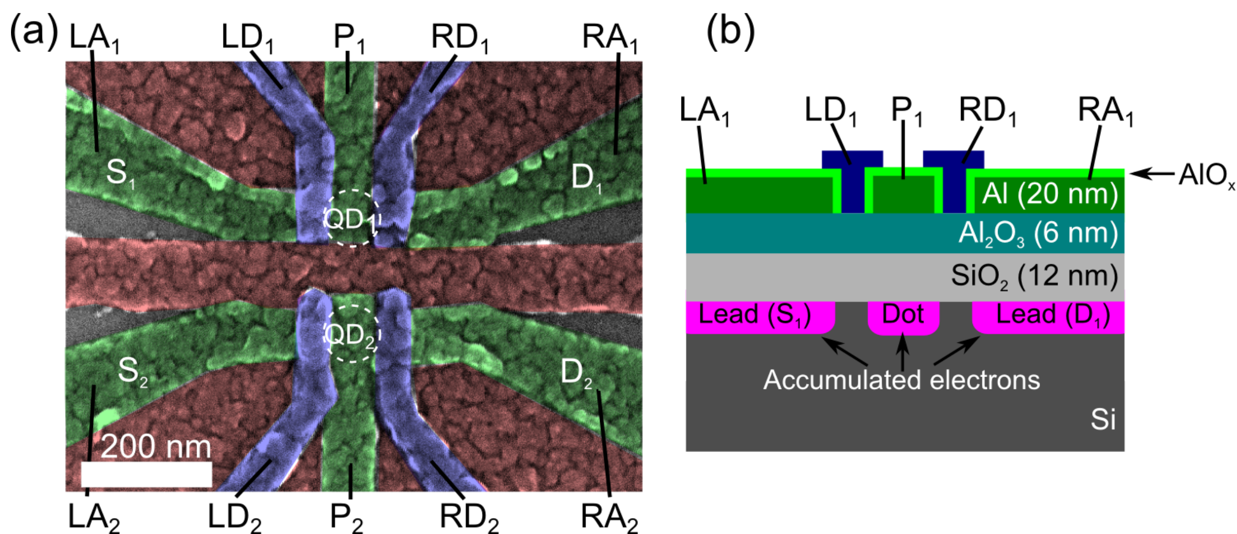

Figure 6.1: (a) False color SEM image showing the different layers of aluminum gates used to define a pair of MOS quantum dots in Si. The approximate location of the dots is shown by the white circular outlines. Transport through each dot occurs horizontally from the source (S) to drain (D) leads connecting each dot to ion implanted regions (not shown). (b) Horizontal cross-section schematic through quantum dot 1 showing the material stack. Dielectric layers separate the gates from the Si substrate, and a thin layer of plasma grown AlO_x isolates each gate layer. Applying a positive voltage to the plunger and accumulation gates (green) creates an accumulation layer of electrons at the Si/SiO_2 interface. Depletion gates (blue) are biased more negatively to create tunnel barriers defining a dot relative to source and drain leads.

gate layers are deposited, the chip is annealed in forming gas at 220 °C for 1 hour, which is found to be critical for obtaining clean and reproducible device characteristics.

Measurements were performed in a dilution fridge with a lattice temperature of 25 mK. DC voltages were applied to the device using a multi-channel custom voltage source based on the Texas Instruments 1220 20-bit digital to analog converter. Current was measured using a DL Instruments current voltage preamplifier. To operate the device the screening gates were grounded, and a voltage of 2.8 V was applied to the accumulation gates ($L/RA_{1/2}$). Voltages on the depletion and plunger gates were modulated to form a dot. The general procedure for this process is to make all three gates comparable to the accumulation gates such that an uninterrupted conducting channel was formed between the source and drain. The depletion gate voltages were then stepped down until Coulomb blockade peaks were observed when sweeping the plunger gates, indicating formation of a

quantum dot.

6.3 Results

6.3.1 Single dot transport

One of the first steps to characterizing this material is to study charge transport through a single quantum dot. Figure 6.2 shows a Coulomb diamond measurement where quantized charge is observed in the quantum dot. A charging energy E_C of 3 meV is extracted from these diamonds, and can be used to estimate the dot size based on its self-capacitance. For a circular disk, the self capacitance is given by $e^2/E_C = C = 8\epsilon_0\epsilon_r r$ where C is the self-capacitance, ϵ_0 is the electric constant, ϵ_r is the dielectric constant of Si, and r is the dot radius. An $E_C = 3$ meV gives a dot radius of 65 nm, consistent with the dimensions of the plunger gate. This indicates that the dot is indeed formed under the plunger gate. The periodic behavior of the diamonds suggests this dot is in the many electron regime, where the energy is dominated by Coulomb repulsion. One may also notice that the edges of the diamonds become more sharp as the gate voltage is made more negative. This is likely due to tunneling boardening of the Coulomb blockade peaks suggesting a tunnel rate energy comparable to the charging energy $\Gamma\hbar \sim E_C$.

To better understand the tunneling rates of each barrier, the current through the system is measured as a function of each depletion gate. The data shown in figure 6.2(b) was collected by sweeping the plunger gate across several Coulomb blockade peaks at each set of depletion gates. The maximum current in each plunger gate sweep was then plotted as a function of the depletion gates. To fit this data we assume that the current is proportional to the total tunnel rate: $I \propto \Gamma_1\Gamma_2/(\Gamma_1 + \Gamma_2)$, and that each tunnel rate is exponentially dependent on the depletion gate voltage:$\Gamma_{1,2} \propto exp(V_{D1,D2})$. The best fit to the data is shown in 6.2c, and shows excellent agreement considering the simplicity of the model.

6.3.2 Charge sensing

While it is useful to study the dot in the many electron regime by measuring its current, it is unfeasible to use this approach down to the single electron regime for this particularly device geometry. This is due to the rapid decrease in current as the dot's plunger gate is made more negative leading to immeasurable currents before the dot is completely emptied. Therefore, it is useful to use a nearby charge sensor to study the state of the dot when

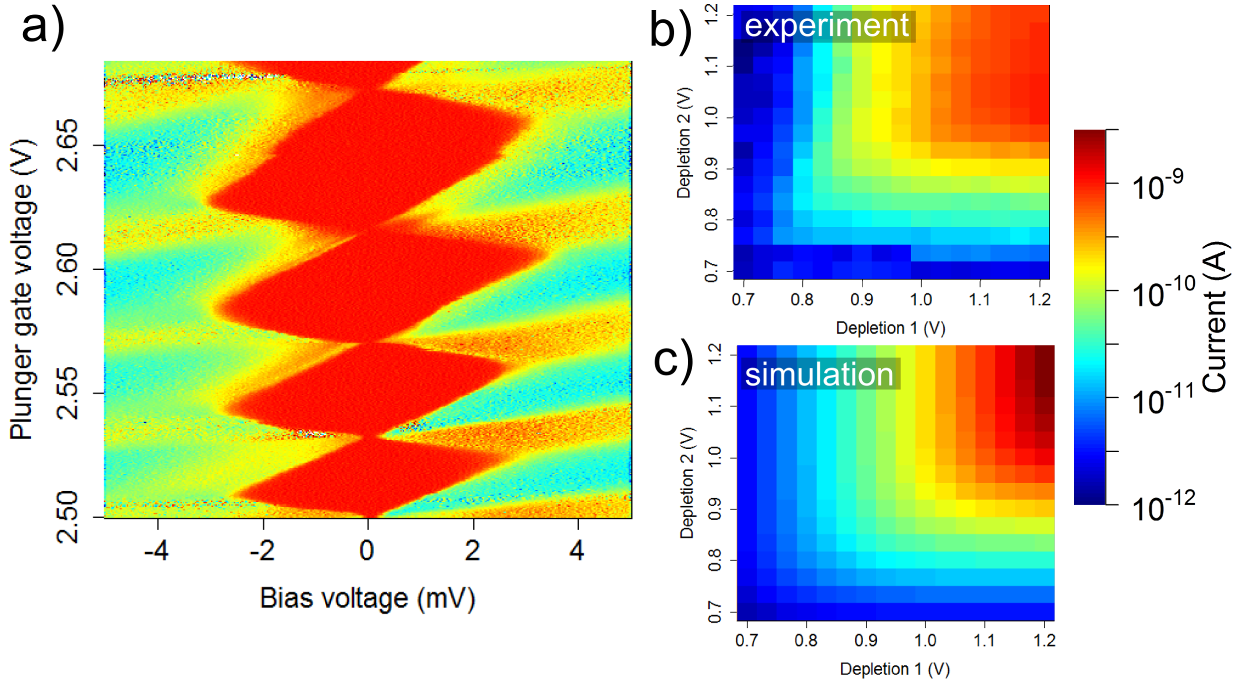

Figure 6.2: (a) dI/dV for a single dot at an electron temperature of 100 mK showing characteristic diamond structure indicative of Coulomb blockade. The red diamond regions are areas of zero current where the charge on the dot is fixed. The width of the diamonds is used to extract an average charging energy of 3 meV. (b) Maximum current through a quantum dot as a function of the two depletion gates which control the tunnel barriers on either side of the dot. Sweeping either gate to more negative voltages increases the height of the tunnel barrier suppressing the current. (c) Simulated current based on the model described in the text, which gives the best match to the data shown in (b). Tunneling rates for each barrier vary exponentially with gate voltage, and range from 40 MHz to 1 THz.

the current becomes extremely small[138]. Here, another quantum dot which has been fabricated close to the original dot (dot 1) is used as a charge sensor by measuring the current through the sensor dot (dot 2). Since the dots are capacitively coupled, changes in the number of electrons in dot 1 modulates the chemical potential of dot 2. If dot 2 is tuned such that it has a large value of dI/dV_g, such as on the side of a Coulomb blockade peak, these changes induced by dot 1 can lead to large changes in current. This effect is demonstrated in figure 6.3a,b, where dot 1 is tuned to a regime where it still passes current, and the current through both dots is measured as a function of P_1. There is an

obvious correlation between the Coulomb blockade peaks in dot 1 and sharp jumps in dot 2's current, that occur when the charge state of dot 1 changes by a single electron. The agreement between the two currents is reinforced by the similarities of figure 6.3c,d, which show a stability diagram in dot 1 as a function of its two depletion gates and the sensor current in dot 2.

The charge sensor allows measurement down to the last electron in dot 1, by looking for the last charge transition out of the dot. The sensor current as a function of P1 is shown in figure 6.4a as the dot is pushed from the many electron to single electron regimes. In order to maintain a usable sensor signal, a compensating voltage is applied to P2 to keep the sensor current on the side of a Coulomb blockade peak. From counting the number of jumps between the last electron and the Coulomb diamond shown in figure 6.2a, it can be seen that the dot contained roughly 25 electrons. An important question when moving to the single electron regime is how the dot potential changes as the plunger gate is varied over nearly 1 V. To explore this question, stability diagram measurements of dot 1 were performed at various P1 values using the charge sensor. It is shown in figures 6.4(b-e) that the potential landscape moves from a predominately single well potential characterized by diagonal lines in (b), to a multi-dot potential showing honey-comb features in (c,d). While it may still be possible to perform QIP on an electron in this uneven potential, it is much more desirable to have a clean, well-defined single well. This variation is likely caused by defects in the Si or Si/SiO_2 interface, and future work should be focused on trying to address this issue.

6.3.3 Memristor

The capacitively coupled quantum dot system has potential applications outside of QIP, including implementation of novel memristive behavior. The memristor is a postulated two-terminal circuit element similar to resistors, capacitors, and inductors, but whose resistance is dependent on the history of current that has flowed through it [140, 141, 142, 143]. The element is appropriately named the memory resistor, or memristor. Several interesting applications of this memory effect have been identified including: ultra dense, low power memory [9, 10], novel stateful logic processes [144], and even neuromorphic computing where the memristor is seen as a synthetic analog of a neuron [145]. In this system, the resistive element is the sensor dot, and the memory is provided by the charge state of the other dot. By applying a voltage to both dots simultaneously, the charge state of the memory dot can be modulated in tandem with the current through the sensor dot. A circuit schematic of the system is shown in figure 6.5a, where a voltage V is applied to the bias of the sensor (dot 1) as well as one of the gates of the memory dot (dot 2). When

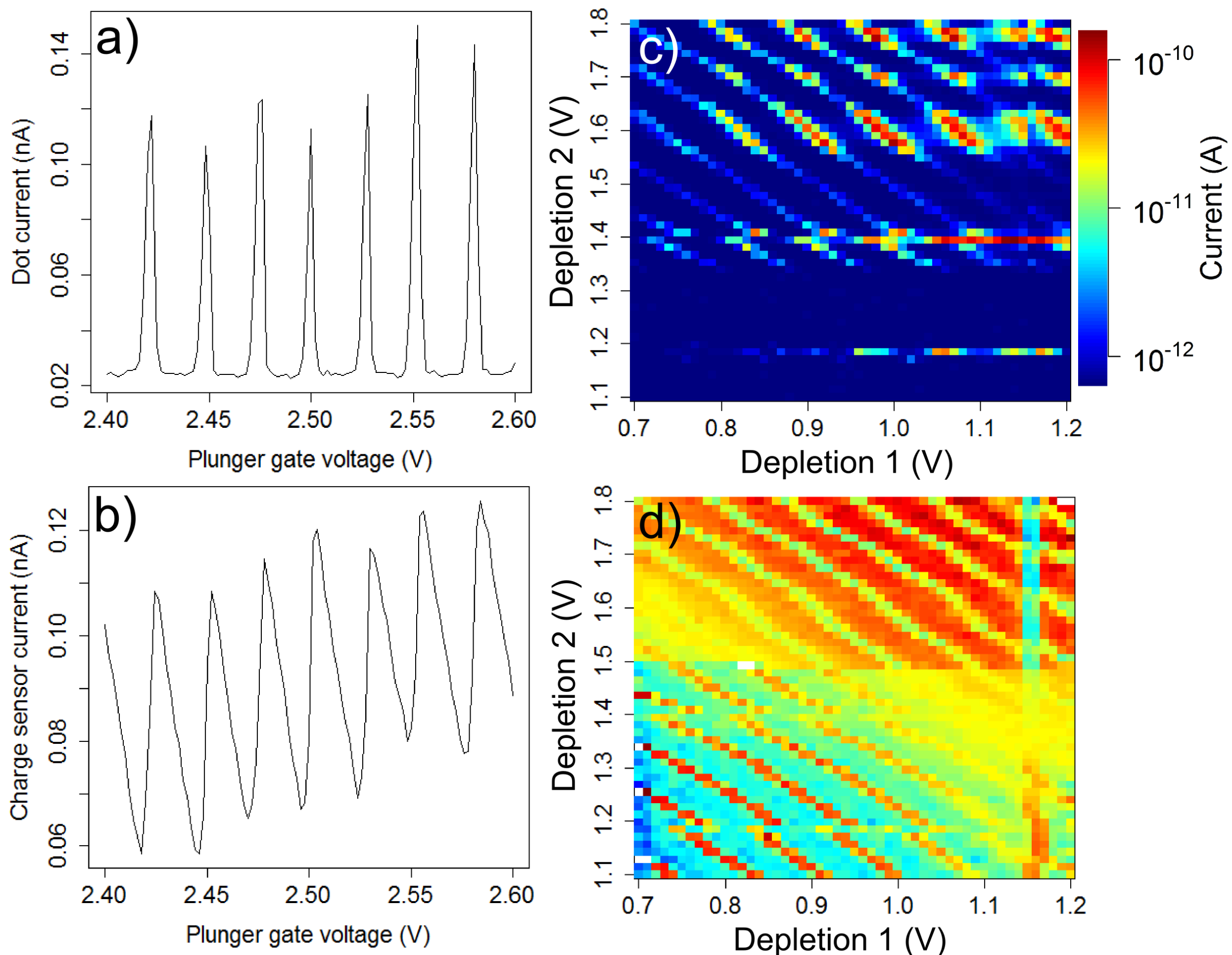

Figure 6.3: (a) Current through dot 1 as a function of P_1 showing Coulomb blockade peaks. (b) Charge sensing signal through dot 2 measured at the same time as (a). A jump is observed each time a peak occurs in (a) indicating a change in dot 1's charge state by one electron. (c) Current through dot 1 as a function of both depletion gates showing diagonal parallel lines indicative of a well-formed single dot. Charge jumps due to nearby traps are visible as abrupt horizontal lines. (d) dI/dVg for the charge sensor taken during the measurement of (c). A clear correspondence between the two measurements is easily seen, as well as the ability of the charge sensor to measure changes in dot 1's charge state even when current through that dot is suppressed.

this voltage is swept at a frequency comparable to the tunneling rate of the memory dot,

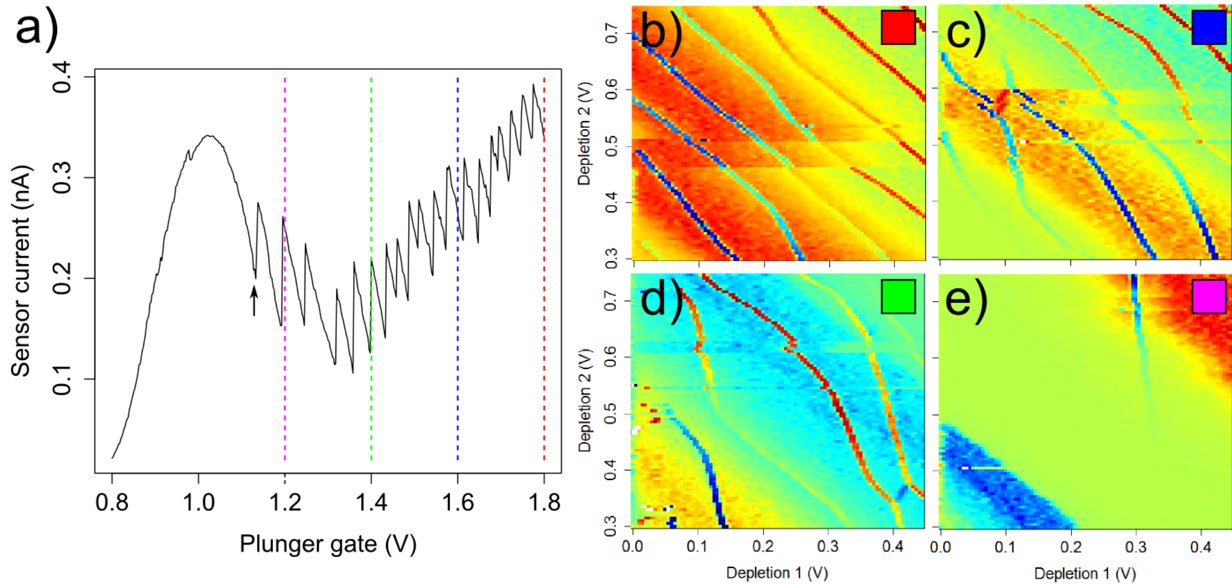

Figure 6.4: (a) Sensor current measuring charge transitions in quantum dot 1 down to the last electron. The last jump, marked by the black arrow, shows when the dot is emptied of all electrons, providing a reference point from which to estimate the electron number at any plunger gate voltage. (b-e) dI/dVg for the sensor dot showing stability diagrams over identical depletion gate voltage ranges. The value of P_1 for each measurement is indicated by the colored square in the upper right corner, which correspond to the dashed vertical lines in (a). (b) Parallel diagonal lines are indicative of a single dot potential in quantum dot 1. (c,d) As the plunger gate is made more negative the charge transition lines are no longer parallel and resemble a honey-comb structure typical of a multi-well potential. (e) In this regime only a single charge transition in visible. The steep slope of this line indicates that the dot is now more strongly coupled to depletion gate 1.

a hysteretic IV is observed indicative of memristive behavior.

The key feature of this system is the capacitive coupling between the two dots, which causes the current of the sensor dot to change depending on the charge state of the memory dot. The charge of the memory dot acts as an effective gate voltage shifting the chemical potential of the sensor dot by the coupling energy E_X. This shift in the chemical potential will change the bias dependence of the sensor dot as shown in figure 6.5b, where the black curve was taken in one charge configuration, and the red curve was measured after an additional electron was added to the memory dot. In this way, the charge state of the memory dot provides a means to control transport through the sensor dot, and thus its

resistance.

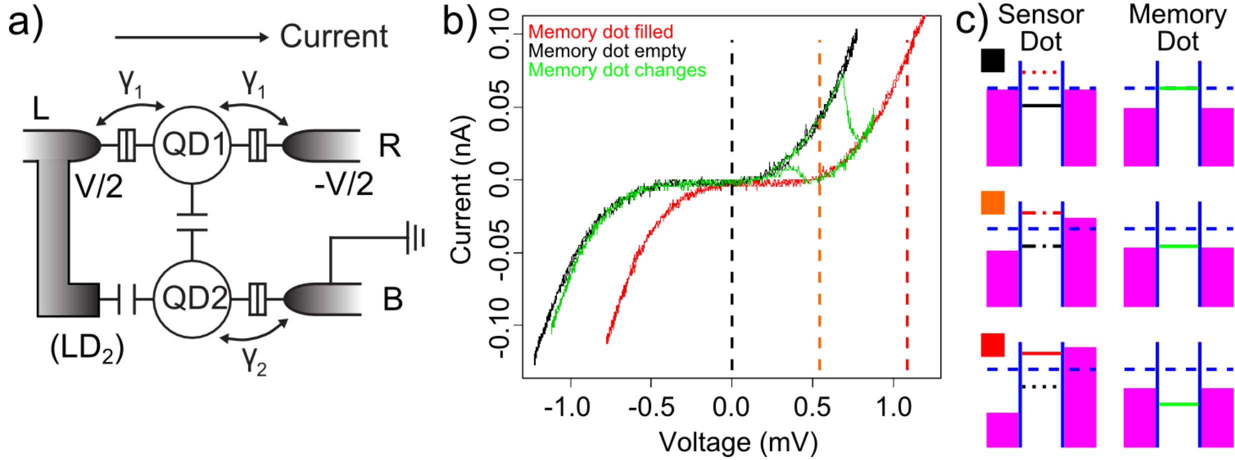

Figure 6.5: (a) Circuit schematic for the memristive system with two terminals: electrode-L and electrode-R. Two terminals are coupled to the sensor dot via tunnelling with the strength γ_1, hence current can go through the device via dot 1. The memory dot is capacitively coupled to dot 1 and the electrode-L and coupled to the electrode-B via tunnelling with the strength γ_2. (b) IV curves through the sensor dot for different charge states on the memory dot. (c) Energy level diagrams for the sensor and memory dot at three different V values, indicated by the colored squares, which correspond to the dashed vertical lines in (b). The horizontal black and red lines are the sensor dot energy level when the memory dot is empty and filled respectively. The pink shaded regions are the chemical potentials of the leads. At zero bias (black square) neither energy level falls in the bias window, and both curves show zero current. The energy level of the sensor dot is above the leads favoring the empty charge state. At large positive bias (red square) either energy level of the sensor dot would fall in the bias window yielding non-zero current for both curves. The energy level of the memory dot is now below the level of the leads favoring the filled state. At small positive V (orange square) the energy level of the memory dot is aligned with the leads allowing for transitions between the two charge states and current hysteresis. In the sensor dot only the black energy level falls in the bias window giving finite current for the black curve and suppressing current for the red curve.

The next ingredient for the memristive system, is that the memory changes as a function of the current through the system. This can be achieved by applying the voltage V to one of the gates of the memory dot. If the dot is tuned properly, this additional voltage will push the dot energy level across the chemical potential of the leads. As the energy level

moves above the potential of the leads, it becomes energetically favorable for the electron to exit the dot, and it does so with the tunneling rate γ_2. Therefore, the charge state of the memory dot, and thus the resistance of the sensor dot can be controlled with V. What is interesting is the effect of the sweep rate of V on the behavior of the coupled dot system. If V is swept much faster than γ_2, the charge state of the memory dot is unable to respond fast enough, and remains constant, giving an IV curve with no hysteresis as shown in the black curve of figure 6.5b. When the sweep rate is much slower than γ_2 the memory dot changes in a very small voltage range resulting in a kink in the IV curve, but no hysteresis. However, if the two rates are similar the transitions into and out of the memory dot occur at different voltage values leading to an IV curve which is dependent on the sweep direction, i.e. hysteresis is observed. An example of this is shown by the green curve in figure 6.5b, where switching between the filled and empty charge states is observed for different sweep directions over a portion of the IV curve.

To measure hysteresis an AC sinusoidal voltage with a frequency of 1 Hz was applied to the bias of dot 2 (L) and the left depletion gate (LD2) of dot 1. The frequency is kept at 1 Hz since RC filters in the circuit limit the bandwidth to 2 Hz. A voltage of 10 mV is applied to LD2, while a 1/10 voltage divider is used to decrease the voltage applied to L to 1 mV. This is due to the lever arm between LD_2 and dot 2 being on the order of 0.2, so increasing the voltage applied to that gate by an order of magnitude puts the voltage applied to both dots on a similar energy scale. The current through dot 1 is amplified using a DL Instruments 1211 current voltage preamplifier before being input to a Tektronix DPO 7104 oscilloscope. Using this oscilloscope 10 second long traces were recorded with a sampling rate of 1 kS/s.

To model this hysteresis behavior, the current through the sensor dot is calculated using [146]:

$$I = \frac{e\gamma_1}{2}[f(n_2E_X - \mu_L + E_1) - f(n_2E_X - \mu_R + E_1)] \tag{6.1}$$

where n_2 is the charge of the memory dot, E_1 is the energy offset of the energy level of dot 1, and $f(E)$ is the Fermi-Dirac distribution. The chemical potentials of the leads $\mu_{L,R}$ are related to the applied bias through: $\mu_L = VC_L/C$ and $\mu_R = -V(1 - C_L/C)$, where C_L is the capacitance between the dot and the left lead, and C is the total capacitance to the dot. Equation 6.1 thus gives the current through the sensor dot dependent on the charge of the memory dot (n_2). This equation is very similar to equation 1.10, with the addition of the shift in the chemical potential due to the memory dot. The current from this equation was presented in figure 1.4, and showed step like increases in current each time a new energy level entered the bias window. Here, there is only one state, so a single sharp step is expected in current. The current through the real device shows suppressed

current at low bias, indicative of a small unintentional tunnel barrier in series with the dot. This effect is included in the model by considering the dot and tunnel barrier as a pair of voltage dependent resistors in series. The IV curve is calculated from the total resistance, which changes as a function of V depending on how the voltage is dropped across the two resistors. The voltage drop across the dot and the tunnel barrier are denoted as V_d and V_b respectively, and are related to the bias voltage by: $V = V_d + V_b$. The resistance of the dot $R_d(V_d)$ is calculated from equation 6.1 using $R = V_d/I$. For the tunnel barrier, resistance $R_b(V_b)$ is calculated by assuming transmission through a square barrier. Using equation 1.5 with the correct transmission coefficient, the current through the barrier can be found as a function of the bias across it. The transmission coefficient for a square barrier is[147]:

$$D(E) = exp(\frac{4\pi s}{h}\sqrt{2m^*(\phi - E)}) \tag{6.2}$$

where s is the width of the barrier, m^* is the effective mass of the electron in Si, and ϕ is the height of the barrier in eV. The best match to the data presented in the figure 6.5 is found for $s = 40$ nm, and $\phi = 0.3$ meV. The current through the barrier is found by integrating Eqn 1.5 over energy at each V_b point.

To model how n_2 changes as a function of V, the tunnel rate into and out of dot 2 are calculated using:

$$\gamma_{in} = \gamma_2 f(\mu_L + E_2)\gamma_{out} = \gamma_2[1 - f(\mu_L + E_2)] \tag{6.3}$$

where E_2 is the energy level offset of dot 2. A voltage sweep can be simulated, by discretizing the sweep in time steps dt and calculating the current at each point. The charge state of dot 2 is monitored at each time point, and has a probability to switch states given by: $P = \gamma_{in,out}dt$. A random number is then generated and compared to the probability to determine whether the charge state successfully changes at that time point. An IV curve produced with this procedure is shown in figure 6.6, along with an experimental trace which shows similar behavior.

Tuning the DC voltages applied to dot 2 varies the hysteresis shape in two distinct ways. The plunger gate P_2 controls the value of E_2. This changes the position of the dot level relative to μ_B, so that a different value of μ_L is required to change the charge state of dot 2. The position of the hysteresis loop is thus shifted along the IV curve, as shown in figure 6.6c. This confirms that the observed jumps in the current of dot 1 are due to charge transitions on dot 2. If dot 2 is detuned far enough, the voltage V will no longer be sufficient to cause the dot level to cross μ_B, and no hysteresis will be observed.

The width of the hysteresis loop is modulated by adjusting the tunnel rate of dot 2, γ_2. This is controlled by the DC voltage on the depletion gate LD_2. Making this voltage

more positive increases the tunneling rate. As the tunnel rate becomes faster relative to the sweep rate, the charge transitions occur closer together, as shown in figure 6.6d. If the tunnel rate were further increased the hysteresis would eventually disappear. The tunneling rate γ_2 can be estimated for a given IV curve as the ratio of the average voltage sweep rate to the distance between the two charge transitions: $\gamma_2 = 8\pi V_a/(\omega \Delta V_{hyst})$, where ΔV_{hyst} is the hysteresis width. Average sweep rate is used since the instantaneous rate varies with V for a sinusoidal drive. For the curves in figure 6.6c,d, tunneling rates of 8 Hz and 33 Hz are estimated, respectively.

6.4 Conclusion

Electron transport through a pair of capacitively coupled Si MOS quantum dots in a parallel configuration is demonstrated. The combination of two dots allows one to be used as a charge sensor to probe the charge state of the other in the when its current becomes vanishingly small. This provides a means to study the electrostatic potential as the dot is pushed to the single electron regime, where quantum information processing could be implemented. Additionally, this system is used to demonstrate a novel current hysteresis effect indicative of quantum memristive behavior. These results combined with the potential to scale this system, using the expertise of the Si industry, make it an exciting platform for implementing spin-based quantum information processing.

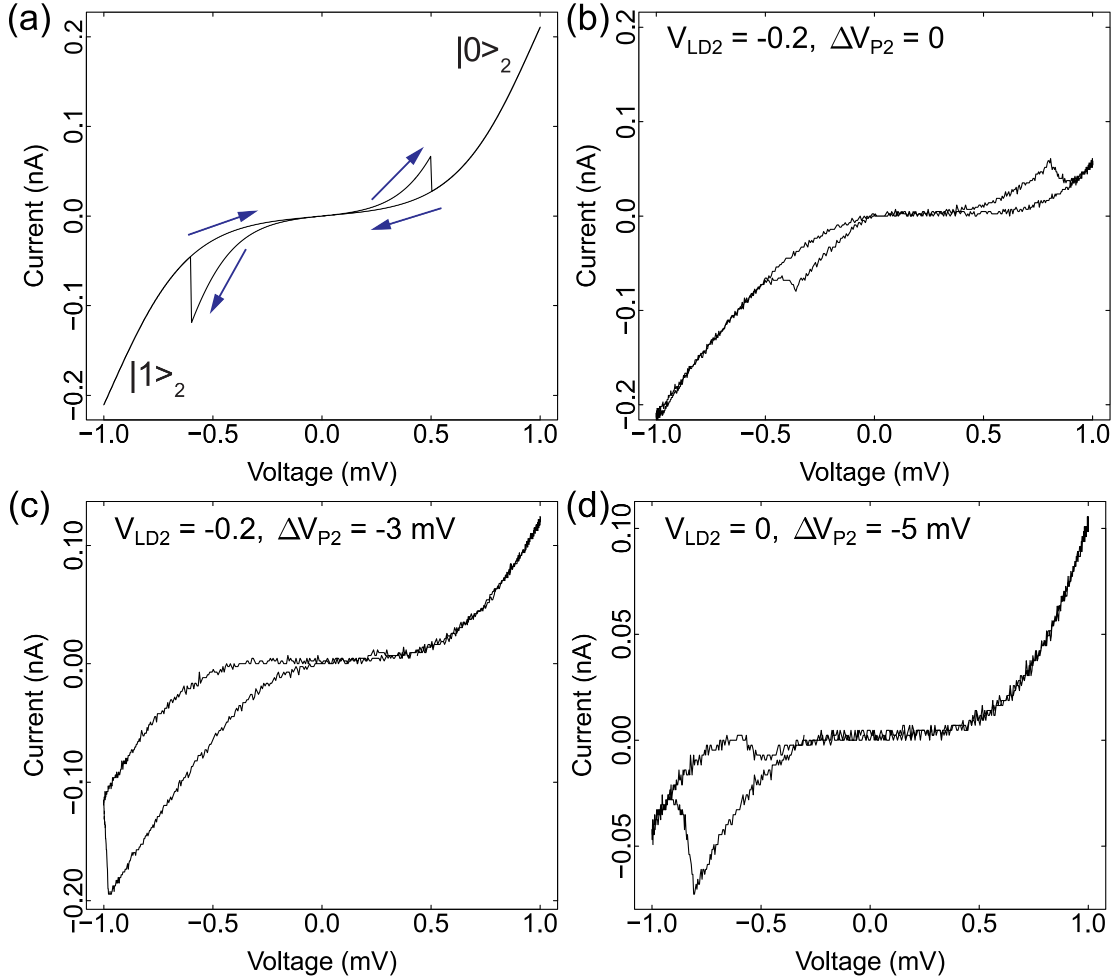

Figure 6.6: Simulated and experimental IV curves showing current hysteresis in the Si double dot system shown in figure 6.1(a). (a) Simulated IV curve of dot 1 for one sinusoidal voltage cycle with an amplitude of 1 mV. A weak suppression of current near zero bias is due to a small, unintentional potential barrier in series with dot 1. The blue arrows relate the curves to the voltage sweep direction. $|0\rangle_2$ and $|1\rangle_2$ indicate the charge state of dot 2. (b-d) Measured current through dot 1 for one voltage cycle with a frequency 1 Hz. (b) Two-looped hysteresis showing similar behavior as in (a). (c) The position of the hysteresis is shifted to negative bias by lowering V_{P2} which changes the energy level E_2 in dot 2. ΔV_{P2} denotes the difference in voltage applied to V_{P2}, relative to when the hysteresis is symmetric about zero bias. (d) Raising the DC voltage on LD_2 lowers the tunnel barrier and increases γ_2, causing the hysteresis width to narrow. The estimated tunnel rates γ_2 for (c) and (d) are 8 Hz and 33 Hz, respectively.

Chapter 7

Conclusions and outlook

This work focused on the study of electron transport in InAs nanowires and Si MOS quantum dots. The goal of working with both systems is the implementation of spin based quantum information processing using electrostatically defined quantum dots. A more complete understanding of the dominant transport mechanisms presented in this thesis will allow for more reproducible and robust devices to be realized. In section 7.1 the conclusions of this thesis are presented. In section 7.2 I will discuss the next steps that should be achieved to move towards realization of a spin based quantum information processor.

7.1 Conclusions

The results presented in this thesis demonstrate many of the dominant mechanisms of electron transport in InAs nanowires and Si quantum dots. We have aimed to understand these mechanisms to develop methods to reduce device variability, and fabricate more robust systems. For small scale systems variability can be overcome by fabricating many devices at once, such that the yield of working devices is high enough to allow the desired effects to be observed. However, as the complexity of the system increases, this approach rapidly becomes unfeasible due to the drop in the yield of working devices. Therefore, working to reduce the variability is an important step towards achieving scability in these systems.

For InAs nanowires, there is some nanowire to nanowire variation even between nanowires from the same growth with similar dimensions. Some of this variation comes from imperfections in the crystalline structure of the nanowire, but we have worked to limit this effect

through optimization of the growth parameters. Instead, a majority of the variation seems to come from the surface of the nanowire, as shown in chapters 2 and 5. This variation could be caused by differences in the native oxide, changes in the donor-like surface states, or molecules adsorbed on the surface. The roles of these effects on transport have been studied in this thesis and have yielded several key conclusions:

- Mobility is limited by ionized impurity scattering from positively charged surface states.
- Charge noise arises from changes in the occupation of single electron charge traps often located in the native oxide.
- The degree of surface band bending and occupation of transverse subbands can be probed through magnetoconductance.
- Encasing the nanowire in a dielectric shell can lead to creation of traps at the interface limiting mobility and subthreshold swing. Chemical passivation of the nanowire prior to deposition of the shell can mitigate these effects.
- Materials in close proximity to the nanowire, such as the dielectric shell, can be another source of charge traps leading to increased noise. Care should be taken to select a low defect density dielectric to avoid degrading the transport properties of the nanowire.

The study of the temperature dependence of mobility in chapter 2 was accomplished through the comparison of experimental results with a numerical model of scattering from ionized impurities. The turn-over in mobility seen in bare InAs nanowires was explained by a thermal activation of these surface states above ~ 40 K. The role of surface states was confirmed by studying the mobility of core/shell InAs/$In_{0.8}Al_{0.2}As$ nanowires. Here, the temperature dependence showed a different behavior, with mobility continuing to increase as the temperature was lowered. This change was attributed to a decrease in the density of scatterers, and was reflected in changes to the numerical parameters used to fit each mobility curve. The addition of the epitaxial shell means that the outer surface of the nanowire is now physically separated from the conducting core leading to a decrease in the effectiveness of these scatterers. Unfortunately, the decrease in the number of surface states also made the core/shell nanowires less conductive at low temperature. We attempted to make quantum dot devices with these nanowires, but found it unfeasible to induce a sufficient free carrier density while realizing the desired potential landscape. Regardless,

these results showed the importance of tailoring the surface states to minimize electron scattering.

Chapter 3 addressed the role of charge noise due to single electron charge traps. The temperature and gate voltage dependence of the dynamics of these traps was fit to a model based on a Coulomb potential barrier. The model showed good agreement with the data giving trap energies from 1 to 100 meV, and putting an upper limit of $\sim$ 10 nm on the radial location of the traps from the crystalline nanowire surface. This information indicates that the single electron traps were located in the native oxide of the nanowire, further confirming the important role of the nanowire surface on transport.

The main result of chapter 4 was the creation of a model which could provide information on the radial potential and subband occupation of a nanowire based on its magnetconductance behavior. The model used the Landauer formalism to draw a connection between the subband occupation and conductance, providing a means to experimentally probe the subband structure. As a test of the model, magnetoconductance as a function of gate voltage was measured for a short-channel InAs nanowire device. The results showed several distinct features, which matched the model allowing for an estimate of the radial potential. The data was somewhat complicated by unintentional mesoscopic effects due to disorder, and future measurements in nanowires closer to the ballistic regime would provide a more definitive match to the model.

The previous chapters focused on analyzing and understanding electron transport, while the goal of chapter 5 was to actually improve transport and gate-ability of the nanowires with different surface processing techniques. The most promising combination for the removal of charge noise and interface traps was to form a self assembled monolayer of octadecanethiol prior to depositing an Al_2O_3 dielectric layer. This process showed the smallest gate hysteresis and a low value of subthrehold swing indicating the removal of defects and traps. Somewhat surprisingly this combination did not provide the best mobility, and this was attributed to the removal of dynamic rather than stationary charge defects. For the purpose of realization of electrostatically defined quantum dot we deemed charge stability to be a more important criteria than high mobility. This was then tested experimentally through the fabrication of a top-gated nanowire, which was used to realize a double quantum dot. We showed for the first time that top-gating could be used to define few electron quantum dots, something which had previously only been done using bottom gates. This was achieved using a novel entrenched design, which allowed the top gates to be made suitably narrow and closely spaced to reach the few electron regime. The device showed clear double dot transport characteristics that were readily fit to a capacitive model, and minimal charge noise over hours long experiments. These results demonstrate the ability to tailor the nanowires properties through fabrication, and provide a more robust system

in which to realize spin based quantum information processing.

Moving away from nuclear spin abundant InAs nanowires, to Si, chapter 6 covered electron transport in Si MOS quantum dots. Si is an promising platform for spin-based quantum information processing, since it can be isotopically purified (^{28}Si) to have no nuclear spins, minimizing coupling to the electron spin qubit, and improving coherence times. While the material system changed, many of the transport ideas were similar, including the necessity of minimizing device to device variation. One cause of variation in these devices was differences in the electrostatic potential in the area of the dot leading to the formation of a multi-welled potential when the dot was pushed towards the single electron regime. A way to characterize this variation was presented by measuring the dot stability diagram using another capacitively coupled quantum dot. A likely source of this variation is due interfaces, such as the Si/SiO_2 or SiO_2/Al_2O_3 interface. We have already found that annealing in forming gas greatly reduces potential fluctuations in these devices, likely due to H passivation of defects at the interfaces. Working to improve these interfaces using different dielectric materials and surface preparation schemes should be an immediate goal of future testing in these devices. In addition to the characterization of the Si quantum dots for quantum information processing, novel memristive behavior is also shown. This provides a proof of concept demonstration of this implementation, showing the versatility of Si MOS quantum dots.

7.2 Outlook and future

7.2.1 Fast charge sensing

The method of spin readout introduced in section 1.3.3 is destructive, such that the spin information is lost during measurement. Through the use of a capacitively coupled charge sensor like the one used in chapter 6 this measurement can be performed non-destructively via spin to charge conversion. In this case, we attempt to push both electrons into the same dot, and then measure the resulting charge configuration. If the two spins are in a triplet state, they remain in their respective dots giving a (1,1) charge state. However if they are in a singlet state, and can occupy the same dot, a (0,2) charge state is measured. The electrons need not exit the dots for the measurement to be performed, and thus their spins are preserved. However, the charge sensor shown in chapter 6 was operated in a DC mode, which is quite slow. The bandwidth of this circuit is usually limited by the RC time constant of the device and the DC lines, which is often in the kHz regime. For systems like InAs where the dephasing time is on the order of ~ 10 ns, this is not nearly fast enough for a

single-shot spin measurement. Instead, radio frequency reflectometry can be used to probe the charge state with integration times as fast as 100 ns [148]. These systems operate by attaching an LC resonator to the source of the device, and applying a microwave tone near the resonance frequency [149]. As the impedance of the device changes, the transmission of the resonator also changes, causing a shift in the reflected power. In addition to simple LC circuits, devices have been placed inside quarter wavelength transmission line resonators to achieve higher quality factors and improved signal to noise ratios [150]. Embedding a Si quantum dot in such a resonator, would combine the longer coherence times of Si with fast charge sensing for a powerful spin readout system.

7.2.2 Long distance spin coupling

Transmission line resonators coupled to quantum dots can also be useful for implementing long distance spin interactions. In this setup, the electric field of the cavity couples to the spin of the electron via the spin orbit interaction [150]. In the limit of strong coupling dressed states are formed, where information can be coherently coupled between the cavity and the dot. For example the excited spin state in the dot can transition to the ground state by emission of a single photon into the cavity. In this way, the spin information of the electron can be coupled into the cavity, where it will be coherent over long distances. The photon in the cavity can then be coupled to the spin of an electron in a different quantum dot well separated from the initial one. In this way long distance spin interactions can be mediated. As mentioned previously, this coupling is achieved by the spin orbit interaction, where the motion of the electron induced by the electric field of the cavity actively rotates the electrons spin. In systems like Si, the intrinsic spin orbit interaction is very weak, making the strong coupling regime unreachable. The use of micromagnets, could provide a field gradient that would serve the same purpose, but these strong magnetic fields will likely spoil the properties of the superconducting cavity. InAs on the other hand has a relatively strong spin orbit interaction, and is a much stronger candidate for implementing this long range spin coupling.

7.2.3 Error correction

One of the ubiquitous challenges with quantum information processing is the handling of errors that will inevitably arise during computation. The field of research dedicated to this problem is appropriately named quantum error correction [151, 152, 153]. While several theoretical schemes for handling error have come from this field, only minimal

experimental realization has occurred in solid state spin systems, due to the large number of qubits needed to implement the processes. The three qubit bit flip code is one such example, where an array of physical qubits is used to encode a single logical qubit [154]. Each of the physical qubits can then be monitored and manipulated to remove errors from the logical qubit. This could be achieved in Si MOS quantum dots by fabricating a square array of four quantum dots. In this configuration, each dot would be capacitively to all other dots, and could be independently controlled. Three of the dots would then be used to encode the logical qubit, and the fourth dot would be used to perform spin readout via the Pauli exclusion principle. As suggested by the name, this code can only remove bit flip errors, but its implementation would serve as an important proof of principle. Other more complicated codes such as the Shor code [155] could then be achieved by scaling up the total number of qubits.

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APPENDICES

Appendix A

Fabrication

Strict attention to detail is one of the most important aspects of nanofabrication. Since these complex devices consist of many complex steps, variation at each point of the process can drastically affect the yield of devices or their characteristics. This guide is designed to convey the recipes for fabricating the various devices presented in this thesis, as well as provide useful tips for each step of the process. The appendix outlines the overall recipes for each device before going into detail about process.

A.1 Si quantum dots

This section contains the overall steps for fabricating the Si quantum dot devices. More information about the details of each step can be found in the following sections.

1. Cleave 4” Si wafer with 300 nm thermal oxide into 4 quarters
2. Photolithography (single layer) for mesa
3. Etch in HF to thin oxide down to 12-15 nm (remove 285-288 nm of 300)
4. Liftoff resist in heated PG
5. Photolithography (single layer) for ion implantation
6. Etch in HF to remove all 300 nm of oxide

7. Ion implantation: $1.5 \mathrm{x} 10^{15}$ cm^{-2} at 12keV (phosphorus).
8. Remove resist with heated PG
9. Clean wafer in RCA 1 and 2
10. Anneal at 950 ° for 1 minute in N_2
11. Deposit 6 nm of ALD Al_2O_3
12. Photolithography (single layer) for wirebonding pads
13. Etch in HF to remove Al_2O_3 from source drain pads
14. Liftoff resist in heated PG
15. Photolithography (bi-layer) for gates and wirebonding pads
16. Ion milling (10 min) + metal deposition (Ti/Au 30/50 nm)
17. Liftoff metal in heated PG
18. EBL (PMMA A4 950K) for alignment marks
19. Metal deposition Ti/Au 30/50 nm
20. Liftoff metal in heated PG
21. EBL (PMMA A3 950K) for first layer of gates
22. Metal deposition Al 20 nm
23. Liftoff metal in heated PG
24. Oxidize Al gate metal in YES asher
25. EBL (PMMA A3 950K) for second layer of gates
26. Metal deposition Al 20 nm
27. Liftoff metal in heated PG

A.2 Nanowire top-gated field effect transistors

The steps for fabricating the top-gated nanowire transistors are listed below. The recipe for fabricating simple FETs is similar, but omits the steps for creating the trench, and the top-gates.

1. Prepare nanowires with desired surface passivation
2. Cleave 4” Si wafer with 300 nm thermal oxide into 4 quarters
3. Photolithography (bi-layer) nanowire wirebonding pads
4. Metal deposition (Ti/Au 30/50 nm)
5. Liftoff metal in heated PG
6. EBL (PMMA A4 950K) for alignment marks
7. Metal deposition Ti/Au 30/50 nm
8. Liftoff metal in heated PG
9. EBL (PMMA A3 950K) for trenches
10. Etch 60 nm oxide in dry etcher
11. Etch in HF to remove 3 nm
12. Liftoff resist in heated PG
13. Deposit nanowires into trenches
14. Use SEM + Matlab to locate nanowires
15. EBL (PMMA A3 950K) top gates
16. Metal deposition Ti/Au 10/20 nm
17. Liftoff metal in heated PG
18. EBL (ZEP 520A) for source/drain contacts
19. HF etch nanowire shell material
20. Ion milling (4 min) + metal deposition (Ti/Au 30/50 nm)
21. Liftoff metal in heated PG

A.3 Photolithography

Photolithograhy is used to create a polymer mask on the substrate for patterning large features. A thin polymer resist is spun onto the substrate, and a UV light source is used to expose areas of the resist. For positive tone resist this light breaks up the polymer chains causing it to become soluble in the developer solution. A glass photomask is used to control the areas of the polymer that are exposed to light allowing the resist to be patterned into the desired features. The advantage of this process is its ability to pattern large areas quickly, but it suffers from a limited resolution, with a minimum feature size of $\sim 1\mu$m. Photolithography is used for the devices shown in this thesis to create etched mesas, ohmic contacts, large metal gates, and wirebonding pads.

Wet etch recipe (single layer)

1. Apply HMDS at 150 °C using a 2 step pump purge cycle
2. Spin Shipley S1811 at 5000 RPM for 45 seconds
3. Bake at 120 °C for 90 seconds
4. Place sample in MA6 and align to desired features using alignment gap of 30 μm
5. Expose for 4.2 seconds in soft contact mode
6. Develop in MF-319 for 60 seconds
7. Stop development in DI water for 45 seconds
8. Blow dry using nitrogen gas

Metalization recipe (bilayer)

1. Apply HMDS using HMDS oven
2. Spin PMGI SF-7 at 5000 RPM for 45 seconds
3. Bake at 180 °C for 3 minutes
4. Spin S1811 at 5000 RPM for 45 seconds

5. Bake at 120 °C for 90 seconds
6. Place sample in MA6 and align to desired features using alignment gap of 30 μm
7. Expose for 4.2 seconds in soft contact mode
8. Develop in MF-319 for 60 seconds
9. Stop development in DI water for 45 seconds
10. Blow dry using nitrogen gas

Comments

HMDS: The HMDS layer is critical for the bilayer process since PMGI generally has poor adhesion to most substrates, and will peel off in the development process if HMDS is not used. For the single layer recipe HMDS is optional, but should be used if there will be poor adhesion of the resist layers. Poor adhesion most frequently occurs on oxide layers that have recently undergone an HF etch.

Resist on the back of the substrate: When spinning resist, it is typical for some resist to leak onto the backside of the substrate particularly around sharp corners. The main concern with this is that it may prevent chips from sitting in good thermal contact with the hotplate, altering the effective temperature seen by the chip. This resist leakage should be removed from the back of the chip using a cleanroom swab moistened with acetone. Care should be taken to only remove the excess resist without damaging the mask on the front side of the chip.

Wedge error correction (WEC): During fabrication it is often necessary to expose small wafers pieces rather than a full wafer in the mask aligner system. Part of the mask aligner loading routine is a process called wedge error correction (WEC), which is designed to correct for small tilt errors when exposing wafers. Unfortunately, this process can lead to large exposure errors if only a wafer piece is placed in the aligner, since it may attempt to correct for the tilt between the sample and the uncovered areas of the chuck, see figure A.1. To avoid this problem one should place dummy samples in these blank areas, so that material of the same height appears to cover the whole wafer area.

A.4 Liftoff

Liftoff refers to the removal of metal present on top of a resist mask following a metal deposition. Additionally, a similar process should be used any time resist is to be removed

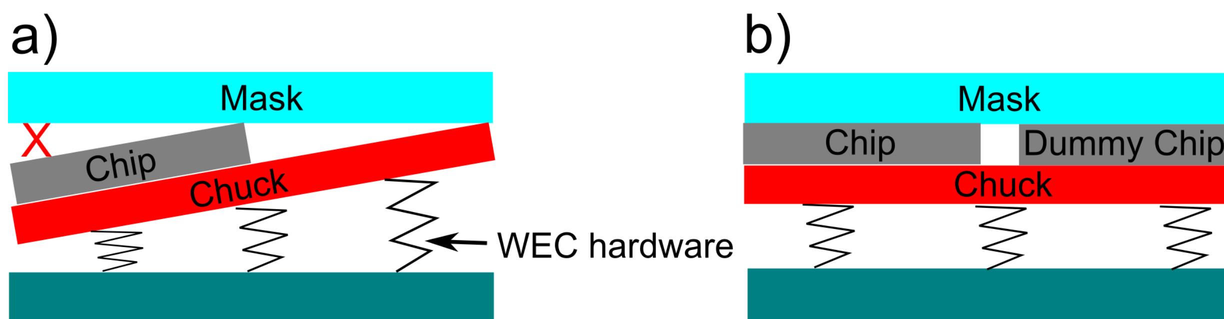

Figure A.1: Cross-section schematic of the photolithography mask aligner showing wedge error correction on small wafer pieces. (a) A single wafer piece is loaded into the aligner causing a wedge error correction (WEC) error, highlighted by the red X. (b) Loading a dummy chip along with the actual chip allows the system to perform WEC correctly resulting in good contact between the mask and the chip.

from a sample after some type of processing. The removal is achieved by soaking the substrate in a heated solvent, most often NMP (N-Methylpyrrolidone), to dissolve the resist polymer under the metal layer. Once the resist is dissolved, the metal appears bubbly and loose, or may simply float away from the substrate. To successfully remove all unwanted metal from the substrate, it is usually necessary to blow some of the heated solvent over the surface of the chip using a small pipette. This blowing helps to break any metal connections that may have formed over the resist sidewalls, and physically moves the metal away from the surface.

1. Place sample piece in NMP (Remover PG) and let soak for at least 12 hours
2. Heat the solvent to 80 ° C for 15 minutes
3. Begin blowing the metal off the surface using a glass pipette. Try to remove the metal in one big sheet by starting from one side of the chip and slowly working across
4. Reheat solvent and allow chip to soak for 5 minutes
5. Repeat the blowing and heating cycle several times until all metal is removed from the chip. Blowing from different directions/angles may help remove stubborn pieces.
6. Examine the chip while still in solution to confirm that all metal has been removed. Small unwanted pieces of metal will reflect light differently than the metal properly adhered to the surface, and can be spotted by viewing the chip from different angles.

7. If all unwanted metal has been removed, remove the chip from NMP and immediately rinse in IPA
8. Rinse in acetone
9. Rinse in IPA
10. Blow dry using nitrogen gas

Comments

Resist without metal: As mentioned above, it is recommended to apply the above liftoff procedure for removing resist from a substrate after any type of processing. This is especially important when the resist has been exposed to acids, bases, or plasmas, as they tend to form a cross-linked film on the surface of the resist. This film is no longer soluble in the liftoff solution, and should be physically removed using the liftoff procedure, to prevent it from adhering to the substrate. If this cross-linked layer is improperly removed, and allowed to stick to the surface, it can be etched away with an oxygen plasma descum/ash.

Sonication: Sonication can be a useful tool for facilitating the liftoff process, but should be used sparingly due to its potential to damage small features. For this reason substrates with contacted nanowires, or features thinner than 200 nm should never be sonicated. If sonication must be used, it is recommended to sonicate for less than 10 seconds at a time, and to hold the beaker while it is in the sonicator to dampen the vibrations.

A.5 Metal deposition

Metal deposition is performed using electron beam evaporation of a variety of metals in a high vacuum chamber. The electron beam is emitted from a filament, and directed to the crucible using a combination of electric and magnetic fields. The impinging electron beam heats the metal in the crucible until it begins to evaporate and coat the sample. Deposition rate is carefully monitored and controlled to ensure a high quality film of the desired thickness is produced. The chamber is also equipped with an Ar ion gun allowing samples to undergo ion milling and metal deposition without breaking vacuum.

Recipes

- Bonding pads, alignment marks: 30/50 nm Ti/Au

- Nanowire contacts: 4 min ion milling, 30/50 nm Ti/Au
- Silicon ohmic contacts: 10 min ion milling, 30/50 nm Ti/Au
- Silicon top gates: NO ION MILLING, 20 nm Al
- Nanowire top gates: NO ION MILLING, 10/30 nm Ti/Au

Comments

Deposition thickness variation: While the deposition rate is monitored, there is some variation between this number and the rate actually seen by the substrate depending on its location on the deposition chuck. For samples placed close to the center the rate matches the listed rate, however at the edge of the chuck, the rate and thus the final thickness is about 72 % lower. In general samples should be placed near the center to avoid this effect, and to minimize shadowing from angled evaporation. However, if deposition near the edge is required, the total thickness should be scaled by 137.5 % to correct for this variation.

Properly securing samples: Many of the deposition chucks for the deposition system feature a set of metal clips for securing samples to the chuck. While these clips generally work quite well, Kapton tape should also be used to help ensure pieces sit flush against the chuck, and when securing pieces too small to safely fit under a clip.

A.6 Dry etching

A plasma made from a variety of gases is exposed to the sample to remove material using a combination of chemical and physical etching processes. Specific etch chemistries should be selected depending on the material to be etch and the masked being used. Dry etching has the advantage of being significantly more directional and repeatable than wet etching, but is more likely to damage the substrate.

Nanowire trench recipe

1. Spin PMMA A3 950K at 5000 RPM for 45 seconds
2. Bake at 180 °C for 15 minutes
3. Expose using electron beam lithography at 25 kV with a 10 μm aperture and a dose of 400 μC/cm^2

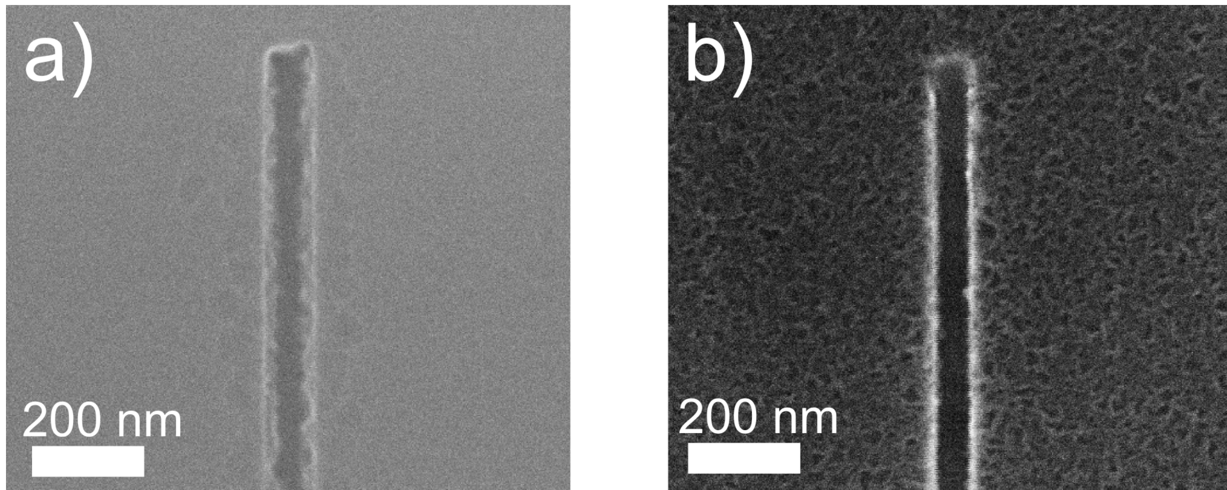

Figure A.2: 60 nm wide trench etched in SiO_2 using dry etching. (a) Etching performed without properly cleaning chamber before starting the process leading to buildup of material along the side walls of the trench. (b) After proper cleaning the trench is fully cleared and shows smooth side walls.

4. Develop for 30 seconds in a solution of IPA/DI with a ratio of 7/3
5. Stop in DI for 30 seconds
6. Run O_2 clean in the RIE metal etcher on a blank silicon wafer. This is essential to remove contaminants from previous users
7. Etch the real sample in the RIE metal etcher using OTP SiO2 etch for 10 seconds
8. Etch in 10:1 BOE for 5 seconds. This step removes a thin layer of oxide in hopes of removing the material damaged during the dry etching
9. Liftoff resist in NMP overnight

Comments

Etch depth: The etch depth for the above recipe is limited by the PMMA mask, which is almost completely removed by the etching process. If deeper trenches are required a thicker PMMA mask, or a mask made out of a resist more suited to dry etching such as ZEP should be used instead.

A.7 Aluminum gate oxidation

Gate oxidation provides a means to create an insulating dielectric layer between different metal layers, without the need to deposit these insulating layers over the entire substrate. This simplifies fabrication, and prevents additional dielectric layers under certain gates, which could lower the capacitive coupling between these gates and the conducting part of the substrate. Aluminum is used as the gate metal, since it is readily available and easily forms strong oxides with relatively large dielectric constants. Oxidation is performed by heating the sample and exposing it to a weak oxygen plasma. It was found that heating the sample in oxygen without applying a plasma formed an oxide, but the oxide showed poor leakage properties and would undergo breakdown at <1 V of bias. Conversely, applying a high power plasma in conjunction with heating formed a strong oxide, but also induced a large number of charged defects in the substrate, which screened subsequent gate layers. A happy medium was found by using a plasma power of 25 W, such that a robust oxide was formed with minimal damage to the underlying substrate.

Recipe 150 °C, 25 W plasma, 200 mTorr O_2, for 120 seconds. Carried out in a YES O_2 plasma asher.

A.8 Wet etching

Samples are placed in a solution designed to chemically etch the desired material. Etchants are usually very caustic, containing a strong acid or base to carry out the etching process. Wet etching has the advantage of being cheaper and more selective than dry etching, but suffers from less reproducible etch rates. The etching solution should be gently stirred during etching to ensure the solution remains homogeneous and the etch rate stays constant. The most common etchant used in the fabrication of these devices is buffered oxide etchant (BOE), which is a mixture of hydrofluoric acid and ammonium fluoride. Some etch rates for various materials in 10:1 BOE are listed below. These etch rates are highly dependent on the quality of the material being etched, as well as the temperature and concentration of the etching solution. It is recommended to perform a quick etch rate test before using this etch on real devices.

- Thermal SiO_2: 0.85 nm/s
- PECVD SiO_2: 5 nm/s
- ALD Al_2O_3: 1.8 nm/s

- PECVD SiN_x: 1 nm/s
- InAs native oxide: 2 nm/s
- InAs: <5 nm/min

Comments PMMA adhesion: HF and PMMA are a notoriously poor combination, which can lead to peeling of the mask material. Thankfully using BOE instead of pure HF somewhat reduces these effects, but still causes the mask to separate from the substrate around patterns in the resist. This separation allows the etchant to reach the substrate outside the masked area etching undesired parts of the substrate. The effect can be reduced by using an adhesion promoter (HMDS) immediately before spinning on the resist, and by switching to a different resist such as ZEP. The combination of HMDS and ZEP was found to almost completely remove this adhesion issue.

A.9 Nanowire chemical passivation

Chemical passivation of III-V materials aims to remove the native oxide at the surface, and replace it with a chemically stable layer that will prevent further oxidation. These changes to the surface could drastically affect transport through materials like nanowires, where the conduction electrons are always in close proximity to the surface. For example, removal of the oxide could lower the number of surface defects leading to improved mobility, or decreased charge noise. In order to prevent further oxidation, a relatively strong chemical bond must be formed between the passivation material and the nanowire surface. Molecules containing sulfur are used in this study due to their affinity for InAs. Specifically, ammonium polysulfide, and octadecanthiol (ODT) are chosen.

Sulfur passivation recipe

1. Measure out 22.4 mg of sulfur powder
2. Sonicate sulfur powder in 1 mL 20 % $(NH_4)_2S$ for 30 minutes or until powder is completely dissolved
3. Dilute sulfur solution in 500 mL DI water
4. Turn on 100 W lamp and place as close as possible to the NH_4S_x solution
5. Etch substrate in 10:1 BOE for 5 s. This removes the native oxide

6. Rinse in DI water for 1 minute
7. Hold sample in passivation solution for 90 seconds, with active areas facing towards the light source
8. Rinse in DI water for 1 minute

ODT passivation recipe

1. Measure out 71.6 mg of ODT powder
2. Heat 50 mL of IPA on hotplate to 60 °C
3. Use magnetic stirrer to mix ODT into heated the IPA for 15 minutes or until powder is completely dissolved
4. Etch substrate in 10:1 BOE for 5 s. This removes the native oxide
5. Rinse in DI water for 1 minute
6. Place sample into a beaker containing the passivation solution and seal with parafilm
7. Let the sample sit in the heated solution for 1 hour
8. Rinse in IPA for 1 minute

A.10 Nanowire deposition

Nanowire deposition is the process for moving nanowires from the growth substrate onto the device substrate. The form of deposition used here is dry deposition, where the growth substrate is physically touched to the device substrate to transfer wires between the two. The growth substrate is first cleaved into small pieces roughly 1 mm x 1 mm in size. This pieces are then flipped so that the nanowires are facing down and lightly placed onto the device substrate. The back of the growth substrate is lightly touched with a pair of tweezers to press the two pieces together and transfer the nanowires. The back of the growth piece should be touched as lightly as possible to avoid depositing too many nanowires at once. Generally it is better to do many light depositions until the desired density is achieved, rather than over depositing nanowires as they are difficult to remove. Nanowires tend to be transferred mostly near the edges of the growth substrate, likely due to uneven pressure

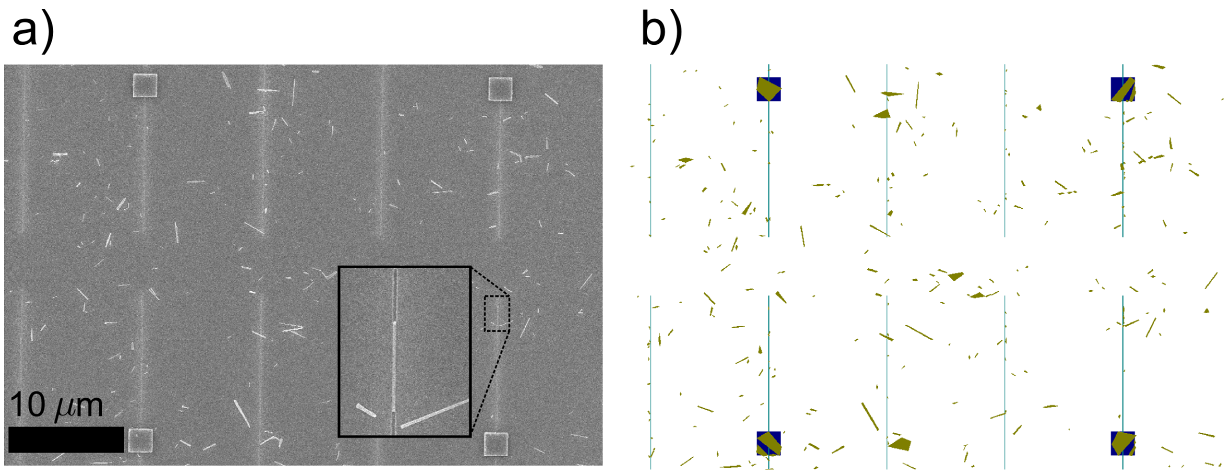

Figure A.3: a) SEM image showing nanowires deposited onto a SiO_2 on Si substrate with trenches etched into the oxide. The small square at each corner of this image serve as alignment marks for nanowire location. The inset shows a zoomed in view of a nanowire sitting in one of the trenches. b) EBL pattern in the Raith software showing the same area as a). Blue squares are alignment marks, teal vertical lines are the trenches, and gold polygons are the objects extracted from a) using the location script. Note the excellent agreement between the nanowires in a) and the located objects in b) allowing for accurate design of the contact patterns.

when touching the back of the growth chip. Therefore, one should try to align edges of the growth chips with the device area, so that a majority of nanowires are deposited in this area. For device substrates with trenches, a brief (<10 seconds) sonication of the device chip in acetone can help to move nanowires into trenches, as well as remove nanowires around trenches. Each chip should be inspected using an optical microscope to ensure the desired density of nanowires is present, or that an appropriate number of nanowires appear to be sitting in trenches.

A.11 Nanowire location

Nanowire location involves locating the position of deposited nanowires relative to prepatterned alignment markers, so that they can be contacted using electron beam lithography. Nanowire location is performed by first taking the appropriate images of each nanowire using SEM, and then running these images through a Matlab script to create a map of the

nanowire locations that can be opened in the Raith software. SEM images of the nanowire should be taken at a voltage of 10 kV with a 30 μm aperture, a magnification of 2 kx, and positioned such that four alignment marker boxes can be seen around the image. Figure A.3a shows an example image. The image should be named after the writefield letter and number where it was taken, i.e. A8, this way it can be properly placed by the Matlab program. An additional image of each nanowire should be taken with a magnification of 10 kx, such that the dimensions of the nanowire can be estimated. With all of the SEM imaging, care should be taken to minimize the exposure of each nanowire to prevent damaging the material. Once all images are collected they can be analyzed using the Matlab script on the lab computer. The output of this script is an asc file containing the nanowire positions which can be directly loaded into the Raith software. An example of this output is shown in figure A.3b.

A.12 Electron beam lithography (EBL)

Electron beam lithography uses a beam of focused electrons to expose a polymer layer to create patterned features. Similar to photolithography, the beam of electrons change the molecular structure of the polymer causing certain areas to become soluble in a developer solution. The advantages of EBL over photolithography, are the ability to change masks on the fly, and the increased feature resolution of $\sim$ 40 nm. Unlike photolithography which exposes large areas to the UV light simultaneously, EBL uses a rastering beam making it significantly slower at patterning large areas. The versatility of the EBL system can be somewhat overwhelming, therefore I've tried to make this guide as detailed as possible to help new users use the tool efficiently to achieve the greatest results.

A.12.1 Overview

The EBL system used here is a RAITH150 Two. As an example I will show how a set of gates for a Si quantum dot device are written in PMMA A3 950K with a thickness of 120 nm. PMMA is the most common resist used to fabricate devices in this thesis, and this process is as complicated as it gets. The pattern for these gates is shown in figure xxx. Features shown in blue are metal already present on the chip, with a square of 24 bonding pads designating a single device. Features in red are areas written with a small high resolution aperture, and pink features are areas written with a large high current aperture. The reason two apertures are used is that the small aperture is needed to achieve the desired resolution at the device, but would take too long to write the large

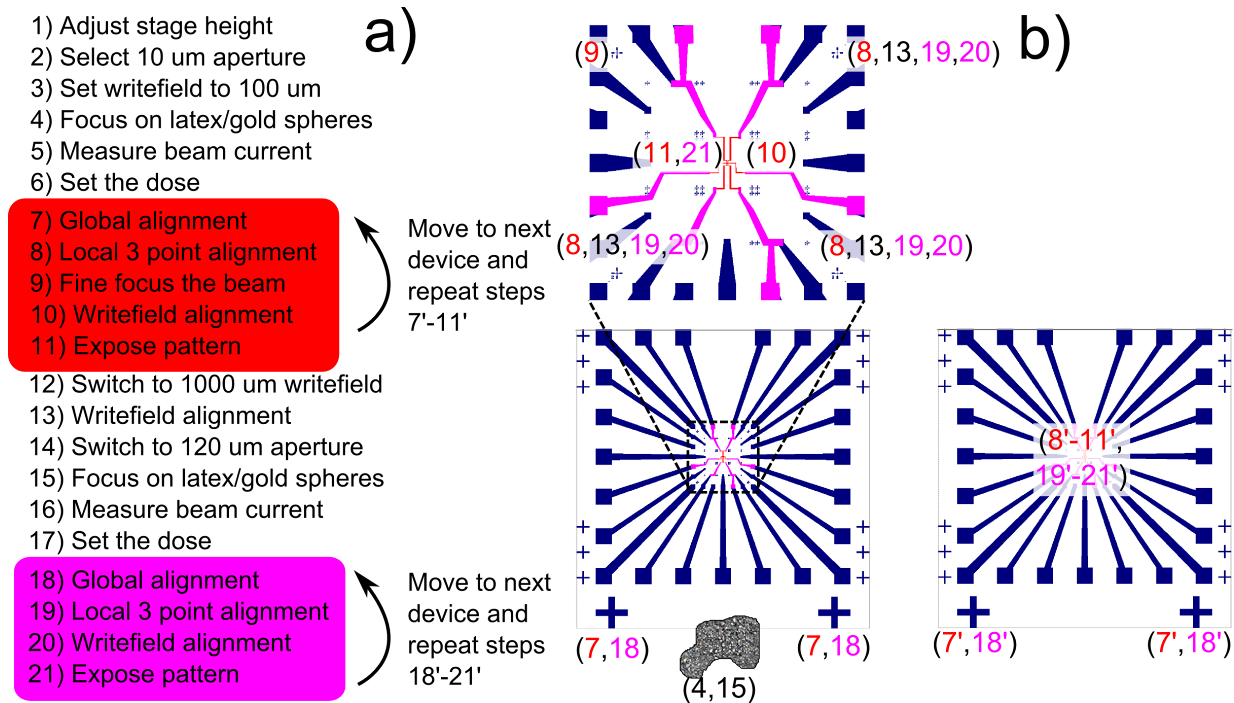

Figure A.4: a) EBL patterning sequence as described in the text. The red and pink block show the steps that are repeated to write patterns with the 10 μm and 120 μm apertures respectively. b) Layout of two identical devices to be patterned with EBL. The numbers show where the steps in a) are implemented. The upper panel shows a zoom-in of the working area for one of the devices.

features connecting the gates to the photolithography patterns. I have found that writing fine features with the small aperture, then switching to the biggest aperture for large areas, is significantly faster than trying to write everything with the small aperture. The overall procedure for aligning to the sample and exposing is shown in figure A.4. The block shown in red is written with the 10 μm aperture, and repeated on each device on the chip before switching to the larger aperture. Similarly, the pink box shows all steps repeated on each device with the 120 μm aperture. The sequence for exposing n devices on a chip would thus be: steps 1-5, steps 6-10 repeated n times, steps 11-15, and finally steps 16-19 repeated n times.

Resist	Aperture	Min feature size	Dose	Step size
PMMA 950K 120 nm (A3)	10 μm	40 nm	220 μC/cm^2	4 nm
PMMA 950K 120 nm (A3)	120 μm	1 μm	260 μC/cm^2	200 nm
PMMA 950K 400 nm (A4)	10 μm	150 nm	300 μC/cm^2	10 nm
PMMA 950K 400 nm (A4)	120 μm	2 μm	340 μC/cm^2	160 nm

Table A.1: Rough estimates for the minimum feature size, dose, and step size when performing EBL at 25 kV.

A.12.2 Designing a pattern

Patterns should be designed using the Raith software before entering the cleanroom. The software is identical to that used during operation of the Raith allowing users to design patterns, create position lists, and check exposure times. When designing very small patterns users should be aware of the step size they plan to use to expose the beam. Polygons should be designed to hold an integer number of steps, or else there is the risk of polygon size changing when fracturing occurs. This occurs when the tool adds or subtracts a single step size to a polygon when it rounds the designed polygon size to fit on the step size grid. While the minimum feature size for the tool is $\sim$ 40 nm, this is only achievable for very thin resists. A rough list of minimum feature size for various resists and apertures is shown table A.1:

A.12.3 Setup and focus

10 μm aperture: steps 1-5 Once the extra high voltage is enabled, the beam should be set to 25 kV. The system is now ready to be set to the standard working conditions: stage height of 10 mm, aperture of 10 μm, and a writefield of 100 μm. A rough focus should be acquired by moving to latex or gold spheres that were deposited on the sample immediately prior to loading into the Raith. Focus on the spheres can be achieved by carefully adjusting the working distance while zooming into a magnification of 50 kx. At this point the rough outline of spheres should be visible. Aperture alignment can be optimized by turning on the focus wobble and carefully adjusting the alignment until spheres appear to remain in the same spot as the focus shifts. To adjust stigmation, turn off the wobble and look at the sharpness of features as you change the stigmation. For this aperture, changes in stigmation are subtle, so stigmation may need to be varied by 10% to see a change in focus. By shifting the stigmation in positive and negative directions it should be clear where the point of best focus and thus optimized stigmation is achieved. Once stigmation

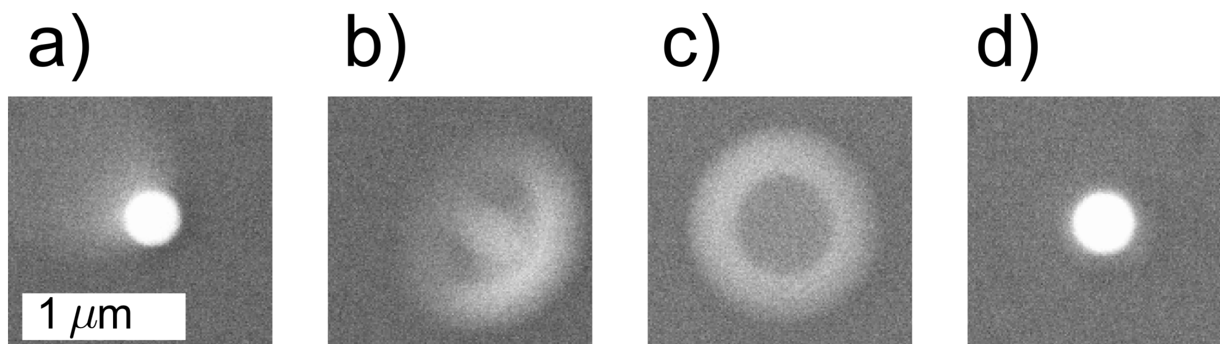

Figure A.5: SEM images of a single sphere using the 120 μm under different focus conditions. a) Working distance correct, aperture alignment off, notice the uneven light shadow around the sphere. b) Working distance and aperture alignment not properly set, the effects in a) are more clearly visible at this working distance. c) Working distance not properly set, but aperture alignment is corrected, the shadow around the sphere now appears symmetric. d) Both working distance and aperture alignment are correct yielding a sharp symmetric circle.

and aperture alignment are set adjust the working distance to achieve the best possible focus. Measure the beam current using the stage Faraday cup, a typical value for these settings is $\sim$ 28 pA.

120 μm aperture: steps 14-16 At this point most of the parameters of the system have already been set, and the aperture just needs to be focused. The process is similar to that outlined for the 10μm aperture above, but the effects to look for when setting the aperture alignment and stigmation are different. For this aperture, focus wobble tends to create a "shadow" that moves away from the object, rather than shifting the position of the object. Proper aperture alignment can be achieved by shifting the alignment until this "shadow" appears to expand isotropically around the sphere. Here aperture alignment is much less sensitive to the percent change, so it may take a relatively large shift to see a change in the "shadow" direction. Stigmation of this aperture is much more sensitive to changes in the stigmation value, but is optimized similarly to the 10 μm aperture, i.e. one should try to achieve the best possible focus. When good focus is found, measure the beam current, a typical value for these settings is $\sim$ 4.2 nA.

A.12.4 Set the dose: steps 6 and 17

After the beam current is measured, the dose can be set. A rough list of doses can be found in table A.1, but a dose test should always be written when trying to write a new pattern containing features near the minimum features size of that aperture. Step size should can be adjusted when changed dose, and should be selected to be as small as possible, while maintaining a beam speed of less than 7 mm/s. Some typical step sizes are included in table A.1. The reason for keeping step size as small as possible is to allow for a more even dose to be applied across the pattern, and to prevent roughness at the edge of patterned features. Beam speed, and thus step size have no direct effect on total write time, but beam speeds greater than 7 mm/s can lead to write errors.

A.12.5 Global alignment: steps 7 and 18

The global alignment marks are part of the photolithography pattern used to create each set of bonding pads, and serve as a point of reference when moving between different devices on a single chip. This means that once a user has completed exposure of a single device, they can simply enter the relative position of the next device to find its global alignment marks and begin the alignment procedure on the new device. Global alignment consists of origin adjustment, and angle correction to the photolithography marks. Since the width of each mark is 50 μm, it is difficult to align to the center of the mark, and thus alignment is made to the lower left corner at a magnification of 1 kx. This procedure is identical for the two different aperture sizes.

A.12.6 Local 3 point alignment: steps 8 and 19

The purpose of the local 3 point alignment is to map the GDS file onto the chip, thereby defining the position of each writefield. Failure to perform this step correctly could lead to stitching errors between writefields, or misalignment to previous layers. Ideally, the distance between the global alignment marks and the local 3 point marks is known exactly, so that one can simply type in the coordinates to move there. This saves time, and avoids exposing the sample near the device area. Before unblanking the beam, magnification should be increased to 20 kx to minimize the area exposed to the beam. Once the mark is found, the coordinates should be switched to local mode and the 3 point alignment performed. The (u,v) coordinates of the 3 point marks can be saved in the software, allowing one to quickly jump to each point and make the necessary minor adjustments very efficiently. Again, this procedure is identical for the two apertures.

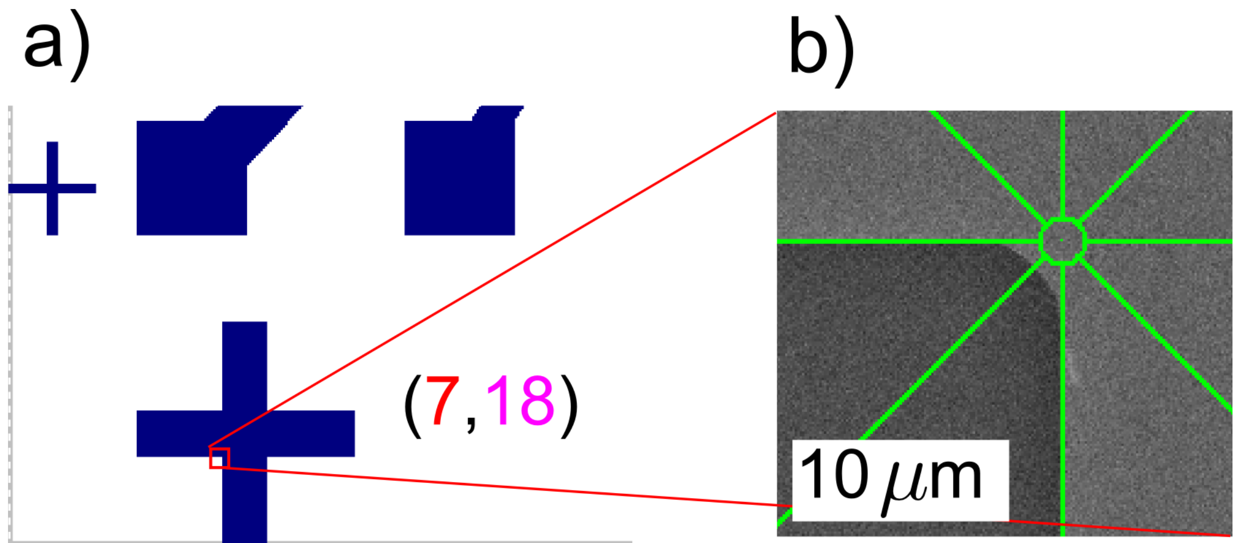

Figure A.6: a) EBL layout showing the photolithography alignment mark and surrounding features. The small red box indicates where the global alignment is performed. b) SEM image taken at 1 kx magnification showing how the global mark is aligned to the crosshair.

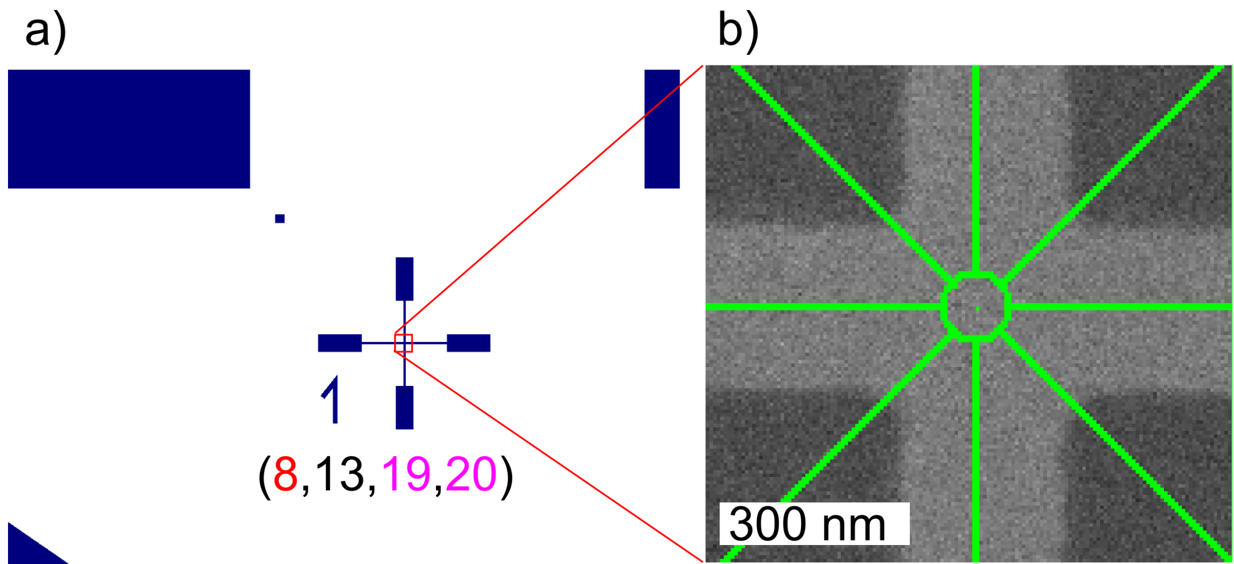

Figure A.7: a) EBL layout showing the EBL alignment mark and surrounding features. The small red box indicates where the local alignment is performed. b) SEM image taken at 20 kx magnification showing how the local mark is aligned to the crosshair.

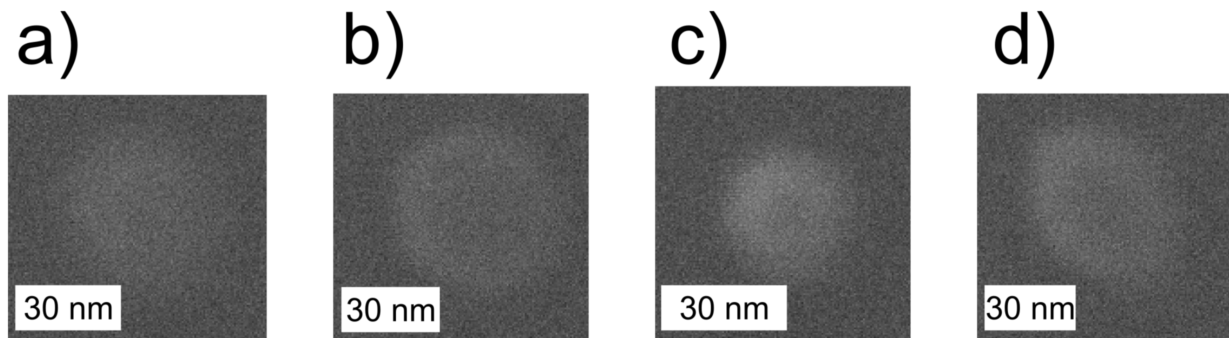

Figure A.8: SEM images of a series of spots burned in PMMA using the 10 μm aperture under different focus conditions. a) First spot burned after rough focusing, spot is out of focus (blurry) and large. b) Same spot as in a), when working distance has been adjusted to bring it into focus. Once in focus, the spot appears as a relatively bright sharp ring around a dark center. Despite appearing to be in focus, the size of the dot is still greater than $\sim$ 20 nm, another dot should be burned at this working distance to confirm everything is properly set. c) Spot burned at the proper working distance. It is small, bright, and sharp indicating good focus. d) Non-circular dot due to incorrect stigmation when burning the dot. Stigmation should be adjusted such that the burn resembles a circle.

A.12.7 Fine focus: step 9

Here the electron beam is precisely focused on the top of the resist minimizing the beam size, and ensuring the best possible resolution. This step is only required for the 10 μm aperture since it has a narrower depth of focus than the larger apertures. The beam is focused by repeatedly burning spots in the resist and adjusting the working distance to focus on these spots. This procedure is carried out in the upper left corner of the working area so that the resist height is similar to the height in the device area. To burn a spot the magnification is increased to 250 kx, and the beam is held at a single point for 12 seconds. Once a spot is burned the working distance is adjusted until the spot is in focus, this occurs when spot appears as a clear ring. This process is then repeated, leading to a small burned spot size since it is being burned with a better focus. Optimal focus is achieved when the spot size is reduced to $\sim$ 20 nm. If the spot appears non-circular stigmation can also be adjusted to correct for this effect.

A.12.8 Writefield alignment

Writefield alignment is the process of calibrating the amount of beam deflection using known distances or known locations on the substrate. In this case, the beam is told to scan four alignment marks located at the four corners of the writefield. The user then looks at the images taken during these scans and tells the tool how far off it is from the actual mark positions. Using this information, the tool corrects for these errors to properly align the beam to the writefield. When writefield alignment of a particular writefield size is performed for the first time during a write, the beam is often way off from the actual positions. For this reason it is useful to perform this first scan with relatively large scan windows to ensure that the locations of the marks will be visible. Subsequent scans should be performed with a smaller window to improve alignment accuracy and minimize the resist area exposed to the beam. If alignment marks are difficult to see, the resolution and number of averages in each scan can be increased, at the cost of slower scans and increased exposure of these areas.

10 μm aperture, 100 μm writefield: step 10 First time alignment of this writefield should be performed with scans windows of 5 μm x 5 μm. All subsequent alignment should be done with 1 μm x 1 μm windows. Proper alignment using this procedure should result in misalignment errors of less than 10 nm. Since beam current is quite low from this aperture, the resist is unlikely to be completely exposed where these writefield scans were done.

10 μm aperture, 1000 μm writefield: step 13 This step is optional, but helps to minimize the areas exposed to the beam during the 1000 μm writefield alignment. Here first time alignment is carried out with the 10 μm aperture to correct for the large initial offset of the beam when the current is still small. Large scan windows of 22 μm x 22 μm can be used to more easily find the alignment marks without the risk of exposing large areas of the resist. If this step were carried out with the 120 μm aperture, each scan would fully expose the resist creating large open windows and increasing the probability of shorting together different device structures. The marks used for alignment in this step are the same marks that were used for the local 3 point alignment.

A subtle point of this process is that beam deflection parameters used to correct for writefield alignment are preserved across different apertures. Therefore, even though switching to the 120 μm aperture will require refocusing and redoing the global alignment, it will maintain relatively good writefield alignment. However, tool does not seem to remember these deflection parameters each time a new sample is loaded in. This means that every time a new writefield is selected in a given run, writefield alignment should be performed.

120 μm aperture, 1000 μm writefield: step 20 Since step 13 was already performed, the alignment should be close to the desired position. Therefore, a somewhat smaller scan window of 10 μm x 10 μm can be used, to improve the alignment accuracy and lower the chance of exposing outside the desired area. To clarify these are the same alignment marks used in step 13, which were also used for the local 3 point alignment.

A.12.9 Expose the pattern: steps 11 and 21

Once dose, focus, and alignment have been properly set, it is time to expose the pattern. Exposure times can be estimated using the "times" button in exposure properties. Generally times should be less than 10 minutes for a single device. Times longer than this are fine, but suggest inefficiency in the pattern design, or indicate that this process may not be suitable for EBL. Time is typically dominated by dwell time which is given by $t_{dwell} = A * dose * I$, where A is the total area of the pattern, $dose$ is the dose, and I is the beam current. If multiple writefields are to be written in a single exposure, one can set the tool to perform writefield alignment prior to writing each field if strict alignment is required.

A.12.10 Develop

When all patterning has been completed, the samples can be removed from the Raith and developed. PMMA development of the doses listed above is carried out with a mixture of IPA and DI water in a ratio of 7 to 3. The developer should be mixed each time a set of chips is to be developed, and allowed to sit for 5 minutes to reach room temperature. Changes in temperature will lead to changes in the dose necessary to clear the resist, so care should be taken to ensure the solution has reached room temperature before using it. Chips are developed by slowly agitating them in the developer for 30 seconds, followed by stopping the development for 30 seconds in DI water. This IPA/DI developer was chosen over other developers such as MIBK/IPA since it requires less dose to clear the patterns, and provides better contrast between exposed and non-exposed areas.

Appendix B

Measurement setup

B.1 Introduction

Quantum transport effects are inherently small, requiring the reduction of spurious effects such as noise to create a measurable signal. While some noise sources may be intrinsic to the device itself, noise can also be dominated by the cryostat and measurement setup, if care is not taken to properly engineer these systems. Most experiments on quantum dot devices require a combination of low noise high frequency (RF) and DC voltages to be applied to a device, while maintaining an electron temperature of <100 mK. While the thermal part of this setup seems easy to achieve, i.e. by placing the sample on the mixing chamber of a dilution fridge, this may only result in a low lattice temperature leaving the electron temperature significantly higher. This is just one example of the numerous subtleties of these measurements that will be addressed in the following sections to achieve the previously mentioned goals. The cryostat for this system is an Oxford Instruments DR200 dilution fridge. A schematic of the wiring inside the fridge as of November 2016 is shown in figure B.1.

B.2 Voltage source

The first place to start reducing noise is at the source. In this case, a major source of noise actually comes from the DC voltage source itself, in the form of high frequency noise. Interestingly, the noise is present on both the inner (HIGH) and outer (LOW) sections of each voltage channel. This prevents the direct filter of the HIGH to the LOW using passive

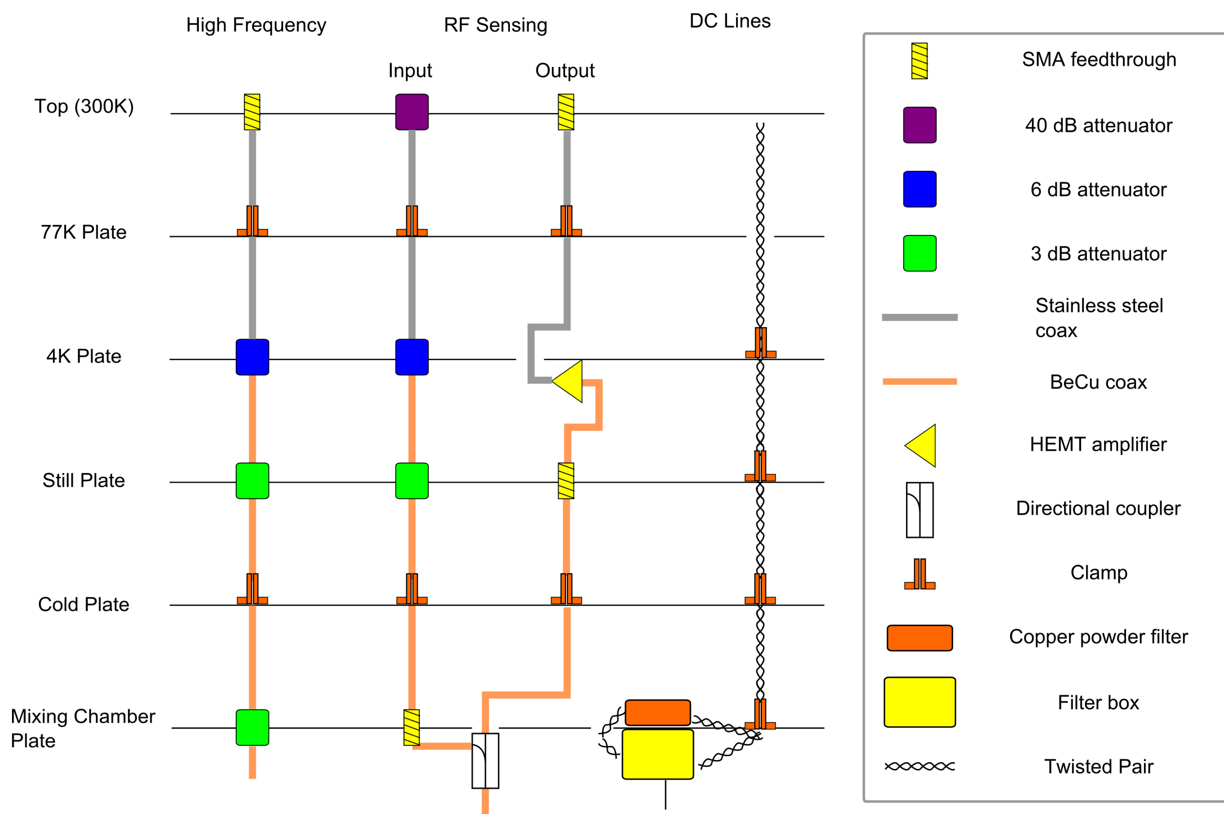

Figure B.1: Wiring schematic for high frequency and DC lines inside the dilution fridge. Symbols show how each line is thermalized, anchored, or filtered at each plate.

RC filters since the noise is present on both sections. Instead, the LOW of the voltage source is directly connected to the main grounding point of the system, providing a low impedance path to ground for the noise on the LOW, and creating a cleaner ground at the breakout box. This cleaner ground can then be used to properly filter the HIGH with passive RC filters. A schematic of the system in both configurations is shown in figure B.2.

B.3 Passive filters

RC filters are used at the breakout box and at the mixing chamber to reduce electrical noise. The external filters are packed in individual BNC connectorized boxes, as shown in figure B.3,to allow for modularity when running different experiments. Output from the

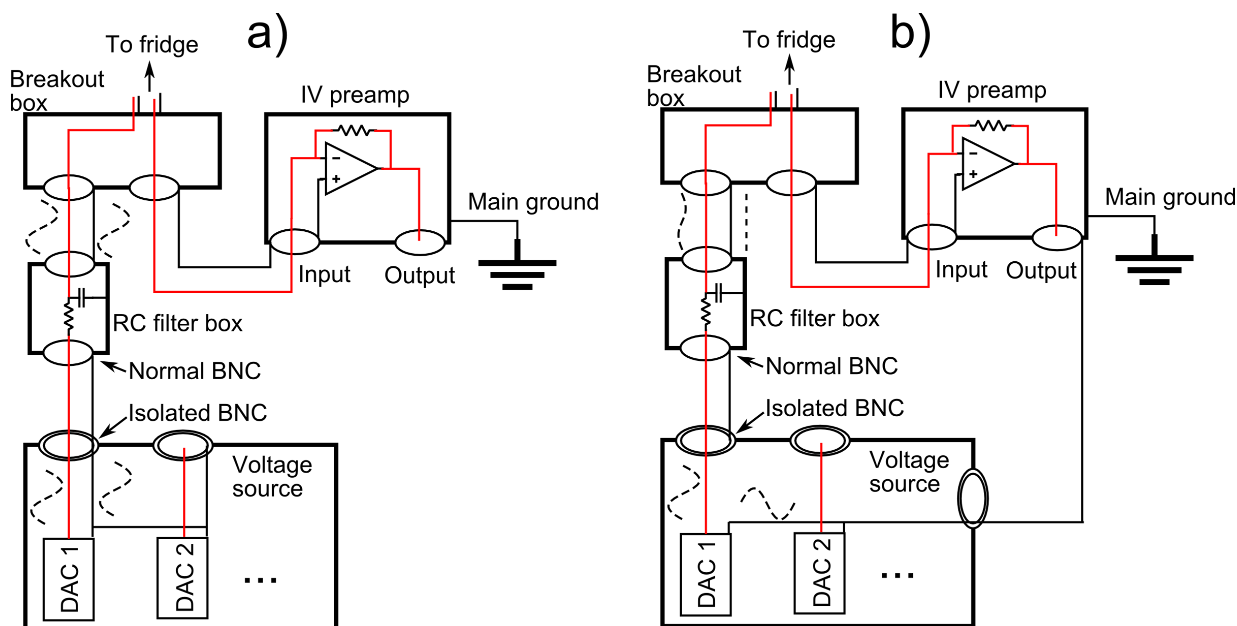

Figure B.2: Schematic of the DC measurement setup outside of the dilution fridge in two configurations. Red lines are the signal carrying inner conductors (HIGH), black lines are the cable shielding providing a path to ground (LOW), and dashed sine waves next to lines show the relative amount of noise in that line. a) The path to ground for the voltage source is provided through the breakout box, allowing noise on the voltage source HIGH and LOW to reach the breakout box and enter the fridge. Since noise in present on the LOW, the RC filter before the breakout box is ineffective. b) Voltage source ground is connected directly to the main ground providing a low impedance path for noise, effectively removing from the system. In this case noise is only present on the HIGH coming out of the source, and can be attenuated using passive RC filters before the breakout box.

voltage source is filtered with a first-order filter with a 3 dB point of 1.6 Hz (10 μF, 10 kΩ). In future these filters should be changed to higher-order filters to improve the roll-off. Output from low frequency AC sources such as lock-in amplifiers are filtered using a 1/100 voltage divider (10 kΩ, 100 Ω).

Filtering at the mixing chamber is achieved using second-order low-pass RC filters. The 24 DC lines are divided into three groups and filtered differently to allow for a variety electrical measurements. One set of six lines is denoted the “low resistance lines”, and has minimal filtering to allow for AC measurements in the kHz, and to provide low impedance connections for highly conductive devices. These filters consist of a 640 kHz filter (50 Ω,

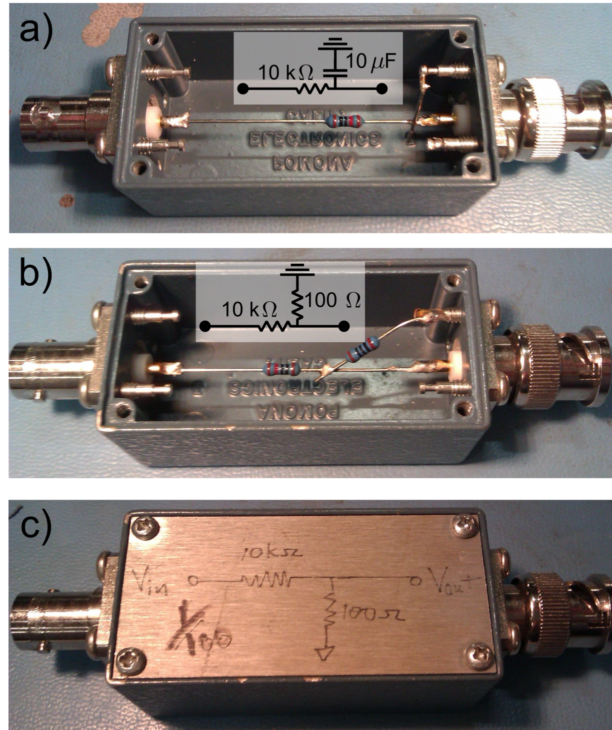

Figure B.3: Photographs of the external filter boxes used to remove noise from signal lines before entering the breakout box. The insets in the upper two images show the circuit diagram for each filter. a) RC filter, b) voltage divider, c) voltage divider with lid.

5 nF), followed by a 320 kHz filter (50 Ω, 10 nF). The poor filtering of these lines at the mixing chamber requires that they be heavily filtered at the breakout box to minimize the noise transmitted to the sample. Another set of four lines are the "source/drain lines" and are used to bias devices which have high resistance such as quantum dots. The filters on these lines are a 64 Hz filter (499 kΩ, 5 nF), and a 106 Hz filter (1.5 MΩ, 1 nF). In addition to the filtering these "source/drain lines" also pass through copper powder filters to achieve better thermalization, which will be discussed in one of the following sections. The rest of the DC lines are used as "gate lines" and are the most heavily filtered since they are intended for applying constant DC voltages to gates in a device. The low pass filters on these lines both have a 3 dB point at 21 Hz (499 kΩ, 15 nF) and (1.5 MΩ, 5 nF).

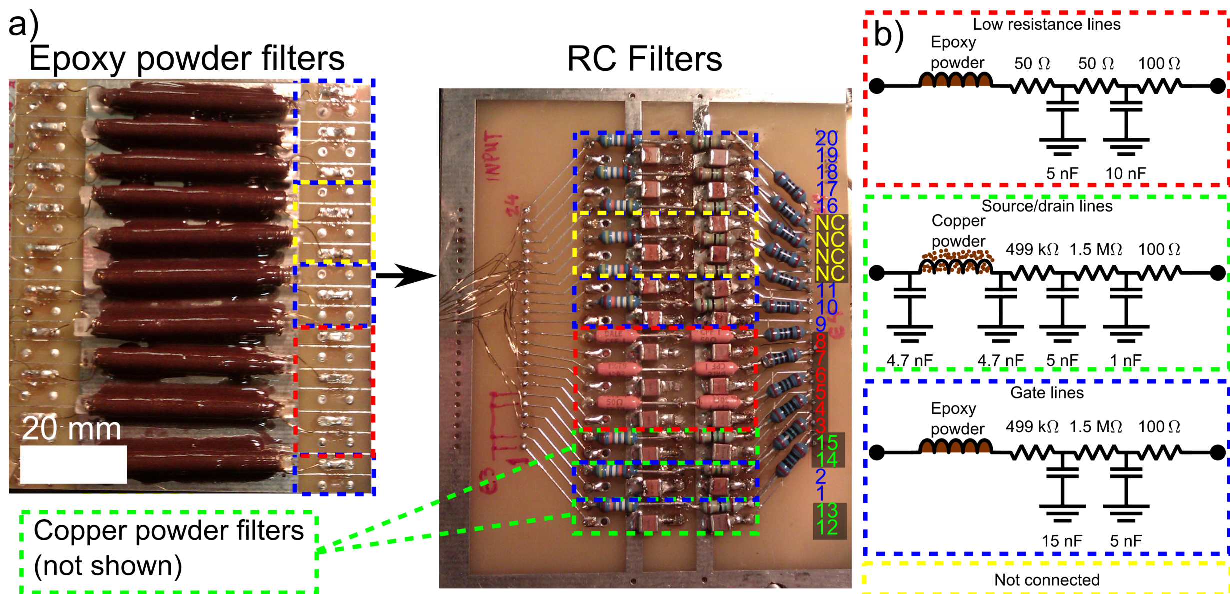

Figure B.4: (a) Photographs of the epoxy powder filters and 2-pole RC filters used to filter the DC lines at the mixing chamber of the dilution fridge. Each board is double sided with an identical set of filters on the opposite side. Colored boxes designate the three groups of lines which undergo different filtering. The colored numbers on the right side of the RC filter board show how each line is mapped to the inputs at the breakout box. NC indicates lines which are not connected in the current configuration. (b) Circuit schematics for each of the three groups of DC lines. The colored boxes match those in (a) showing how the different circuits correspond to the components on the board.

B.4 Inductively coupled noise

Another path for noise to couple into the system is inductively via flux through large ground loops. Sources of this noise are often hard to eliminate since they arise from things like pumps, computers, and fluorescent lights. Instead, the best way to counteract this noise is by removing the ground loops themselves, either by physically breaking the loops, or by minimizing the area enclosed by the loop. To prevent ground loops the entire system is grounded at a single point, in this case the current voltage preamplifier, with all other grounds tied to the main ground point in a star pattern. Thus the preamplifier serves as ground for the fridge itself via the breakout box, and for other instrumentation such as the voltage source. An outline of the setup is shown in figure B.2b. In some cases, multiple paths connect two ground planes together, such as in the cabling used to connect

the breakout box to the fridge. Here, each signal is carried in the core of the flexible coax line, while each shield is connected to ground. In this case the area of the each ground loop is minimized by twisting all the cables together to form a tightly packed single cable. Similarly, in the fridge, the DC signals are carried on ribbon cables of constantan twisted pairs, where each pair consists of a signal line twisted with a ground line. As of October 2016, after the completion of the work in this thesis, the whole fridge has been placed inside a copper shield room, with all noise producing elements outside the room, to help further reduce this noise.

B.5 Thermalization

In addition to the reduction of electrical noise outlined in the previous sections, thermal noise must also be properly removed to reach electron temperatures below 100 mK. The wiring is thermalized at each plate in the fridge by sandwiching it in a gold plated copper clamp, as shown in figure B.5. This lowers the lattice temperature of the cable to match the temperature of each plate, beginning the thermalization process, and lowering the heat load on subsequent plates. The wire itself is also made from constantan which has a lower thermal conductivity than copper, and should reduce the heat carried by the wire. Once the cables reach the mixing chamber they are passed through copper powder filters before entering the RC filters discussed previously. The copper powder provides an additional means of thermalization, by dissipating microwave frequency noise as it induces eddy currents in the copper grains. Two types of copper powder filters are used to thermalize different subsets of the DC lines. “Gate lines” and “low resistance lines” are passed through epoxy powder filters, while “source/drain lines” go through copper powder filters. The epoxy based filters are more compact, but less strictly built providing a quick way to moderately thermalize many lines. These filters consist of 1 m of insulated constantan wire wrapped around a G-10 rod. The wire-wound rods are then covered in stycast epoxy loaded with copper powder, and placed on a metal ground plane to set, see figure B.4a. The long length of wire in good thermal contact with a metal plane tied to the mixing chamber plate provides an efficient thermal path to dissipate heat in the wire.

The copper powder filters work on a similar principle, but follow much stricter design specifications leading to superior attenuation. Each copper powder filter consists of 2 m of 40 gauge insulated copper wire wrapped around a 1/8” G-10 rod with slits milled along the length of the rod. The wire is wrapped such that each turn is symmetric, and sits in direct contact with the previous turn. Halfway along the rod, the wire is passed through a small hole in the rod and counter-wound to cancel out inductive pickup. Each rod is

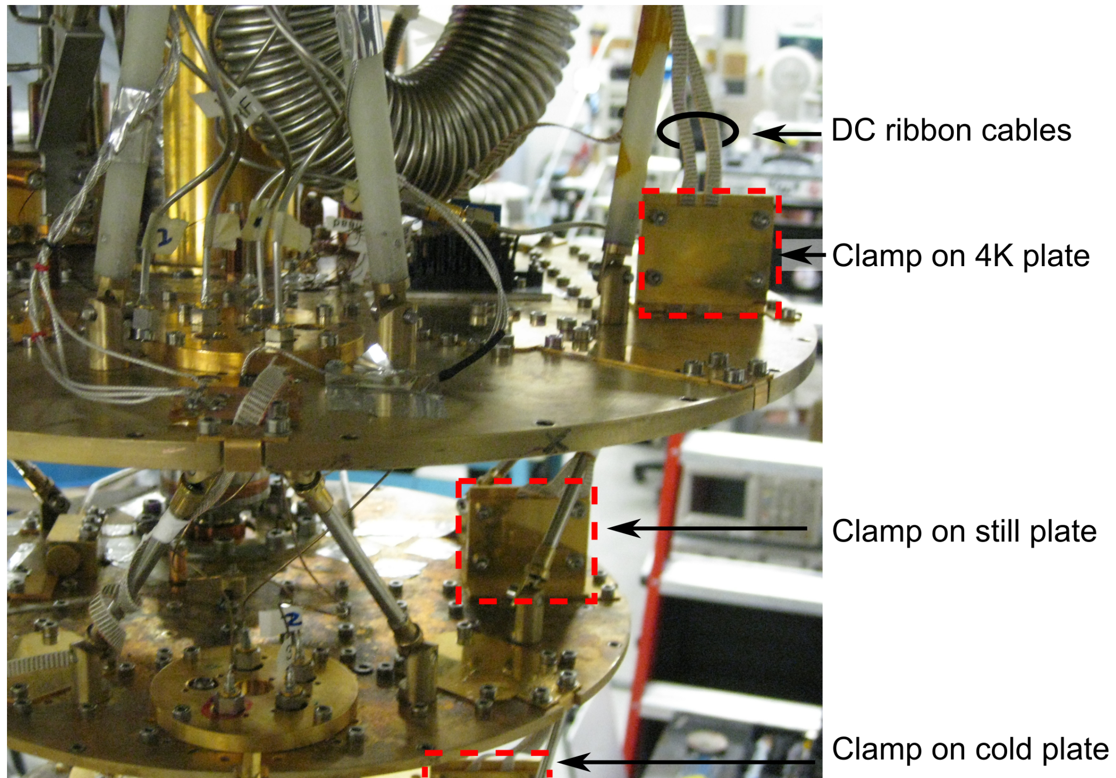

Figure B.5: Image of the 4K and still plates in the dilution fridge showing the clamps used to thermalize the DC lines. The DC lines consist of two ribbon cables each with 12 constantan twisted pairs. The clamps help the wiring reach the temperature of the plate they are attached to, and using constantan helps limit the heat transfered between each plate.

then placed in a 1/4" diameter hole drilled through a piece of oxygen free copper. The space around the rods is filled with tightly packed copper powder with a grain size of 10 μm. The slits in the G-10 rod allow the copper powder to better cover all sides of the wire improving attenuation at higher frequencies. The end of each wire is soldered to the center pin of a press-fit SMA connector, and a 4.7 nF capacitor is connected between the center pin and the ground of the connector. These connectors are then press-fit into the oxygen free copper and further sealed with a thin layer of stycast epoxy. The extra attention to detail used when building these filters pays off giving a transmission of less than -100 dB for frequencies above 10 MHz.