45-nm SOI CMOS Bluetooth Electrochemical Sensor for Continuous Glucose Monitoring

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Due to increasing rates of diabetes, non-invasive glucose monitoring systems will become critical to improving health outcomes for an increasing patient population. Bluetooth integration for such a system has been previously unattainable due to the prohibitive energy consumption. However, enabling Bluetooth allows for widespread adoption due to the ubiquity of Bluetooth-enabled mobile devices. The objective of this thesis is to demonstrate the feasibility of a Bluetooth-based energy-harvesting glucose sensor for contact-lens integration using 45 nm silicon-on-insulator (SOI) complementary metal-oxide-semiconductor (CMOS) technology.

The proposed glucose monitoring system includes a Bluetooth transmitter implemented as a two-point closed loop PLL modulator, a sensor potentiostat, and a 1st-order incremental delta-sigma analog-to-digital converter (IADC). This work details the complete system design including derivation of top-level specifications such as glucose sensing range, Bluetooth protocol timing, energy consumption, and circuit specifications such as carrier frequency range, output power, phase-noise performance, stability, resolution, signal-to-noise ratio, and power consumption. Three test chips were designed to prototype the system, and two of these were experimentally verified. Chip 1 includes a partial implementation of a phase-locked-loop (PLL) which includes a voltage-controlled-oscillator (VCO), frequency divider, and phase-frequency detector (PFD). Chip 2 includes the design of the sensor potentiostat and IADC. Finally, Chip 3 combines the circuitry of Chip 1 and Chip 2, along with a charge-pump, loop-filter and power amplifier to complete the system.

Chip 1 DC power consumption was measured to be 204.8 μW, while oscillating at 2.441 GHz with an output power P_{out} of -35.8 dBm, phase noise at 1 MHz offset L(1 MHz) of -108.5 dBc/Hz, and an oscillator figure of merit (FOM) of 183.44 dB. Chip 2 achieves a total DC power consumption of 5.75 μW. The system has a dynamic range of 0.15 nA – 100 nA at 10-bit resolution. The integral non-linearity (INL) and differential non-linearity (DNL) of the IADC were measured to be -6 LSB/$\pm$0.3 LSB respectively with a conversion time of 65.56 ms. This work achieves the best duty-cycled DC power consumption compared to similar glucose monitoring systems, while providing sufficient performance and range using Bluetooth.

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Chapter 1

Introduction

1.1 Motivation

As obesity rates continue to rise, the risk of on-set diabetes has increased significantly over the last 40 years [13]. Management of the disease requires frequent monitoring of blood sugar levels to ensure that they do not increase to dangerous levels. Currently, the majority of patients manage their blood sugar through the use of blood glucose measurement meters. These systems are often inconvenient and invasive, which has led to interest in less invasive glucose monitoring systems [3].

A potential solution is to monitor the glucose levels found in tears using a sensor embedded on a contact-lens. Glucose levels in tear glands are correlated to blood sugar levels, and thus can be used as a proxy when monitoring and controlling human insulin levels [14]. A prototype system has been developed by Verily Life Sciences and Novartis International (Figure 1.1). The system includes a loop antenna surrounding the periphery of the contact lens, a glucose sensor to measure glucose, a capacitor to store harvested energy, and a controller which contains the sensor and communication electronics. This system is an enhanced version of research conducted by Liao, et al., which included a potentiostat, sensor readout, energy harvester and wireless communication circuitry within the controller[2]. The patient uses an external reader in close proximity to power the system with radio-frequency (RF) energy. RF energy is converted into DC power which is then used to measure glucose levels, and transfer this information back to the reader using a radio frequency identification (RFID) device through, for example, backscattering techniques [2][15].

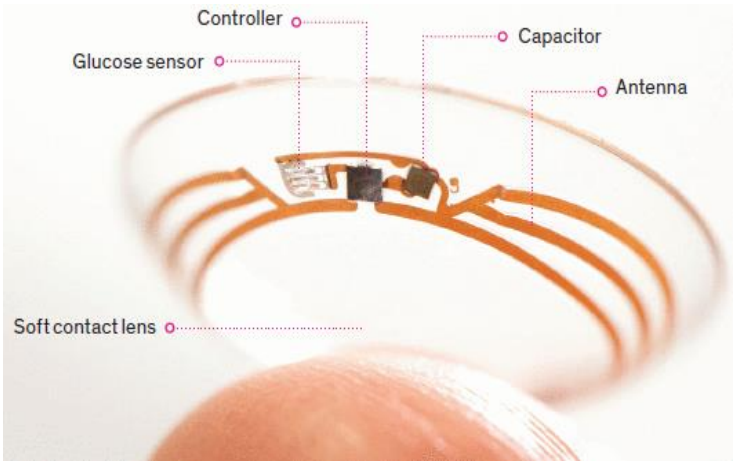


Figure 1.1: Smart contact-lens energy harvesting glucose monitoring system [3].

A major drawback to this scheme is that the reader must be continuously transmitting RF power for the sensor to backscatter data, thus requiring that the glucose monitoring system consume less power than it is able to harvest since these operations occur simultaneously. This scheme requires tight power consumption constraints to meet these requirements. Furthermore, the external reader must transmit +30 dBm of power to harvest an appreciable amount of power at the receiver [2]. This may lead to long-term health risks to the patient as ocular tissue could be damaged over time by the incident RF power required to activate the glucose monitoring system. Finally, the external reader proposed requires patients to carry an extra device as the RFID technology used by the glucose monitoring system is not compatible with mobile phones. Mobile phones typically implement near-field communication (NFC) as their RFID technology, which operates at 13.56 MHz. However, the system in [2] operates at 1.8 GHz, thus requiring a separate reader device.

1.2 Scope

In order to address the above shortcomings, this thesis proposes a new energy harvesting wireless glucose sensor based on the Bluetooth^{TM} standard. Bluetooth implementation allows the patient to use their smartphone to power the system, which encourages widespread adoption of the technology. Furthermore, the system can now harvest energy and then transmit data, rather than doing both simultaneously. This allows the smartphone to transmit less energy over a longer period, addressing the potential safety concerns mentioned previously. However, traditional Bluetooth implementations are infeasible for a

glucose monitoring system as they consume more than 1 mW [16]. Thus, the goal of this research is to design some of the ultra-low-power blocks required to enable this application, as shown in Figure 1.2. To reduce the scope of this thesis, certain subsystems have not been implemented.

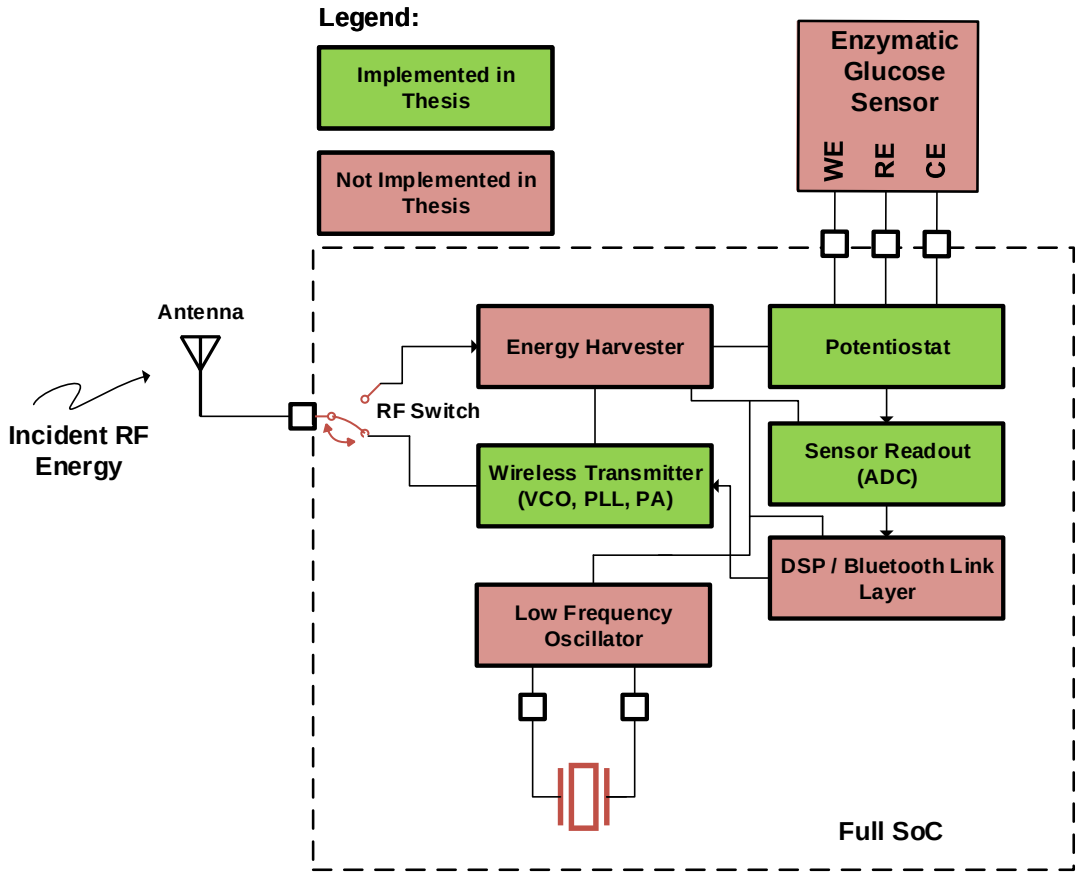


Figure 1.2: Overview of the proposed glucose monitoring system.

The system requires an antenna designed for 2.4-GHz ISM-band operation residing on the outer rim of the contact lens. This would receive incoming RF energy and direct it through an RF switch to the energy harvester subsystem. This system is effectively a rectifier, converting RF energy into DC energy to be used by the remainder of the electronics. Furthermore, an enzymatic glucose sensor, which has been constructed with specific materials and enzymes, is placed on the contact lens to act as a reaction site to

sense the glucose levels in the basal tear fluid coating the eye. This sensor is controlled by a potentiostat which acts as voltage source to sustain the glucose reaction, as well as sink the signal current produced by the sensor. The current is then digitized using sensor readout circuitry. The digital subsystem obtains the sensor data and creates a Bluetooth packet in order to transmit the sensor data to the smartphone. This packet is then sent via the wireless transmitter and antenna to the smartphone. The low-frequency oscillator is a stable reference clock for the entire system.

The focus of this thesis is the design and characterization of the wireless transmitter, potentiostat, and sensor readout circuitry. First, a two-point in-loop modulation topology is utilized to reduce the power consumption of the Bluetooth transmitter shown in Figure 1.2. This approach is attractive as it reduces power consumption while reducing channel frequency drift. Second, a low-supply-voltage current-mirror-based potentiostat architecture is employed. Finally, low-supply-voltage sensor readout circuitry is implemented using a first-order, continuous-time incremental analog-to-digital converter (IADC).

1.3 Design Challenges and Objectives

In this section, the challenges associated with building a glucose monitoring system are described and design specifications are derived.

1.3.1 Bluetooth Compliance

For this application, a subset of the Bluetooth Low Energy (BLE) protocol is implemented to reduce the complexity and power consumption of the transmitter. The BLE protocol operates in the 2.4 GHz ISM band. BLE transmits at 1 Mbit/s using a Gaussian frequency shift keying (GFSK) signal with a modulation index of 0.5. A frequency hopping transceiver is implemented in the standard, which operates in two modes: advertising mode and connected mode [1]. In advertising mode, only three frequency channels are used by the system, as illustrated in Figure 1.3.

For the contact lens system, only glucose concentration must be transmitted. Therefore, an advertising-only transmitter is implemented to reduce power consumption and system complexity. The protocol chosen changes the system requirements, and indirectly the power and energy consumption of the transmitter.

Table 1.1 lists relevant system-level specifications imposed by the BLE standard, which must be satisfied. However, meeting these specifications while significantly reducing the

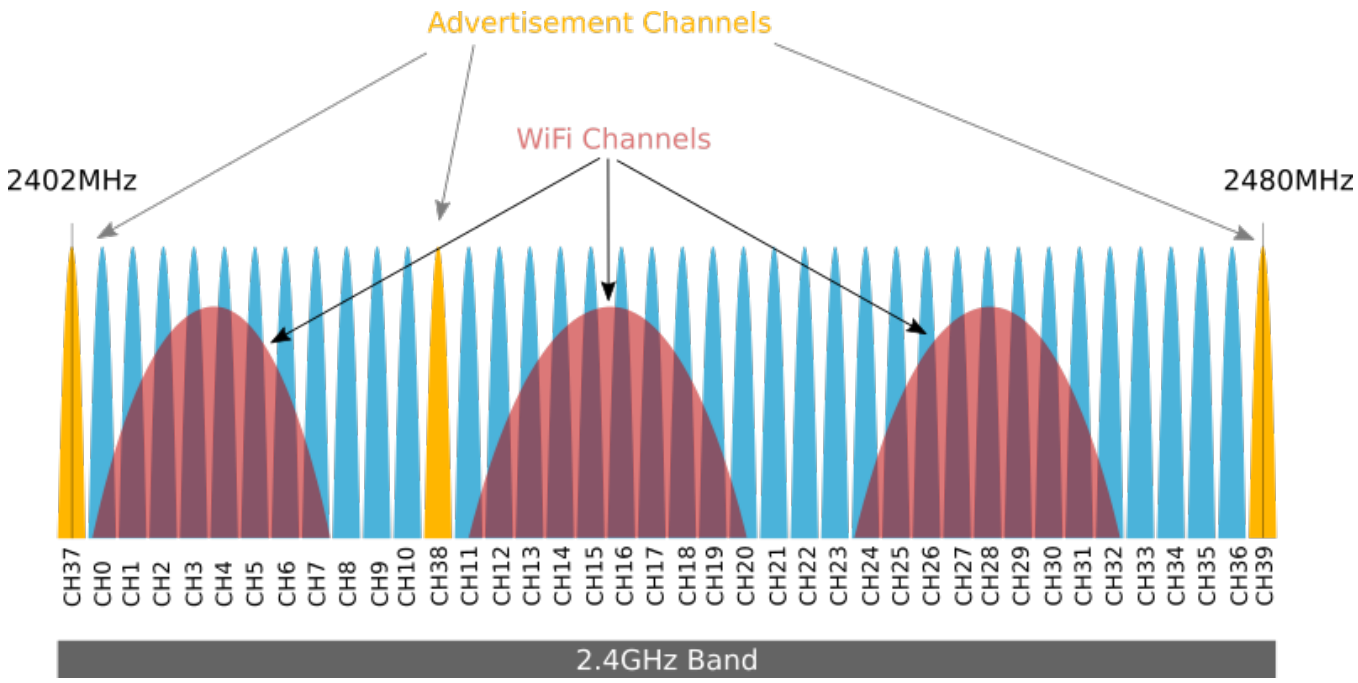


Figure 1.3: BLE Frequency Spectrum [4]

power consumption is challenging, because power is traded-off to meet various performance parameters.

Table 1.1: BLE Transmitter Requirements [1]

Specification	Minimum	Maximum
RF Output Power P_{out}	-20 dBm @ the antenna	+10 dBm @ the antenna
Channel Frequency Range	2402 MHz	2480 MHz
Modulation Frequency Range	-250 kHz	+250 kHz
Adjacent Spur @ 2MHz offset		-20 dBm
Adjacent Spur @ 3MHz offset		-30 dBm
Frequency drift		$\pm$ 50 kHz
Drift rate		400 Hz/μs

1.3.2 System Energy Budget

Many of the overall system requirements may be determined from the energy available to the system. The contact lens system requires that energy must be harvested from 2.4 GHz ISM band energy such as Bluethooth and/or WiFi. To calculate the received power many assumptions need to be made. For example, the input power P_{TX} is assumed to be solely harvested from a smartphone's Bluetooth transmitter. Thus, P_{TX} is assumed to be 10 dBm. However, the system could instead/in addition harvest energy from WiFi, which emits a much higher output power of 21 dBm. However, this thesis uses a stricter power budget to target more aggressive power savings on the smartphone. The gain of the transmitter antenna G_{TX} is assumed to be 1.76 dBi, which is standard for omni-directional smartphone antennas. The gain of the loop antenna G_{RX} was simulated using Ansys High Frequency Structure Simulator (HFSS) with a 5 mm radius, 0.5 mm trace width and 5 μm thickness, as was used in [2]. An additional loss of 18.5 dB is added to the receiver gain to account for dielectric losses attributed to the eye. The smartphone is assumed to be transmitting at a distance of 5 cm from the glucose sensor, which implies a path loss PL of 14 dB. Combining these terms using Friis' equation, one can find:

$$\begin{aligned} P_{RX}\ [\text{dBm}] &= P_{TX}\ [\text{dBm}] + G_{TX}\ [\text{dB}] + PL\ [\text{dB}] + G_{RX}\ [\text{dB}] \\ &= 10\ \text{dBm} + 1.76\ \text{dB} - 14\ \text{dB} + (-4.3 - 18.5)\ \text{dB} \\ &= -25.04\ \text{dBm} \\ &= 3.133\ \mu\text{W}. \end{aligned} \tag{1.1}$$

The expected received power is calculated in eq. 1.1 where the maximum transmit power is 10 dBm at 2.4 GHz (as per Bluetooth specification in Table 1.1) at a distance of 5 cm from the contact lens. Assuming an RF to DC conversion efficiency η_{RFtoDC} of 0.5, P_{DC} is found to be 1.566 μW. The energy harvested ($E_{Harvest}$) is dependent on the time given to harvest enough energy for the system ($T_{Harvest}$) as well as the DC power harvested, and is given by

$$E_{Harvest} = P_{DC} T_{Harvest}. \tag{1.2}$$

To create a power budget, the activation time for each step of the system is crucial.

- $T_{MEMSosc}$. This is the amount of time the MEMS oscillator is enabled. In this case, it must be enabled from the beginning, since it acts as the clock for the rest of the system.

- $T_{Reaction}$. This is the amount of time necessary for the glucose reaction to occur, which is approximately 20 s.
- T_{TX}. This is the amount of time the TX is enabled. Using an advertising-only based BLE protocol, this time can be reduced to approximately 1ms (19bytes×8bits×3channels / 1 Mbps+500 μs for overhead) [1]. This is sufficient due to the fact that the amount of data being sensed is trivial.
- T_{ADC}. This is the amount of time the sensor readout ADC is active, which is estimated to be 200 ms based on 3 samples with an estimated worst case conversion time of 65.5 ms.
- $T_{Digital}$. This is the amount of time the digital logic is active. This is estimated to be 210 ms, assuming a worst case of 10000 clock cycles at 1 MHz necessary for the system.

Figure 1.4 details the timing of the system. To make the application viable, the time spent making a measurement needs to be as small as possible. The following equations related Time A (time to harvest energy and activate sensor), B (time to read out the sensor), and C (time to transmit sensor data) to the timing variables above:

$$\begin{aligned} T_A &= T_{Harvest} = T_{Reaction} + 5s \\ T_B &= T_{ADC} + T_{DIGITAL} \\ T_C &= T_{TX} \\ T_{MEMSosc} &= T_A + T_B + T_C \end{aligned} \tag{1.3}$$

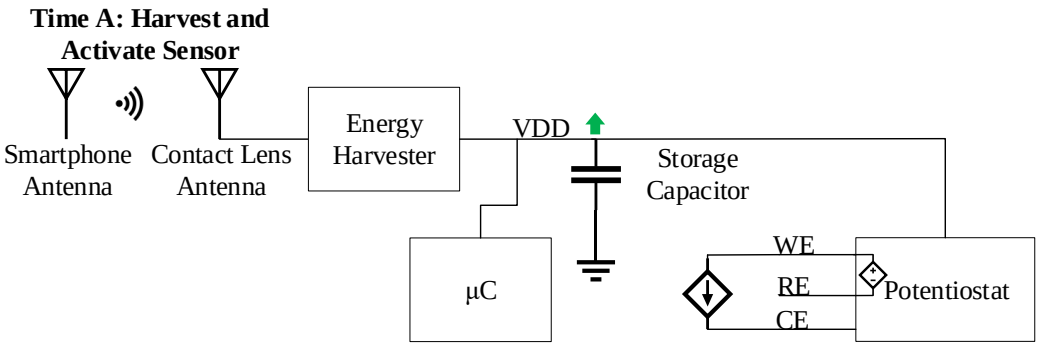
Given these activation times, the overall energy consumption can be found as:

$$E_{System} = P_{MEMSosc}T_{MEMSosc} + P_{Potentiostat}T_{Reaction} + P_{ADC}T_{ADC} + P_{TX}T_{TX} + P_{Digital}T_{Digital}. \tag{1.4}$$

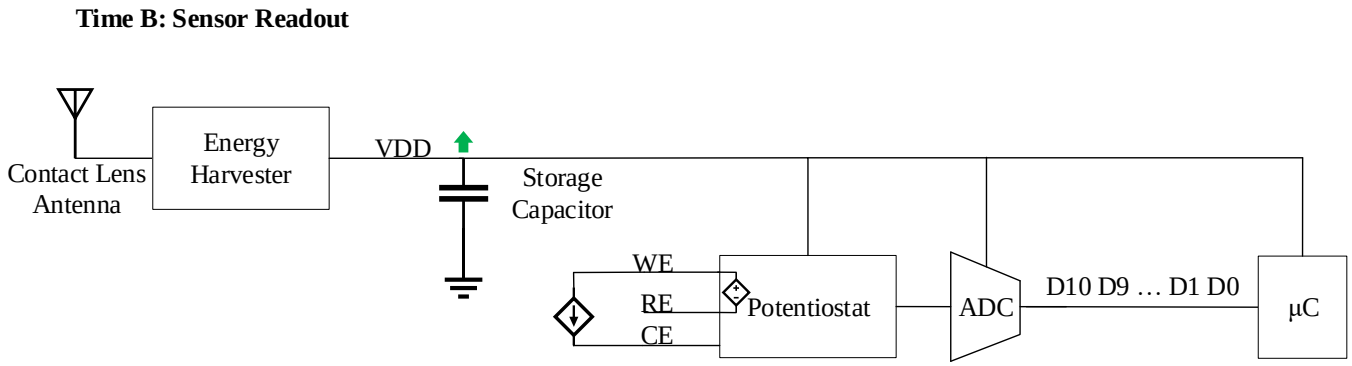
Therefore, reasonable power targets were pursued as detailed in Table 1.2. It is important to note that there are many assumptions implicit in these estimates. For example, it is assumed that Friis' equation holds when calculating input power. However, the system is not completely within the far-field at 5 cm distance. Furthermore, power consumption of the power distribution network is ignored, which would tighten the total power budget further.

Table 1.2: System Power and Energy Budget

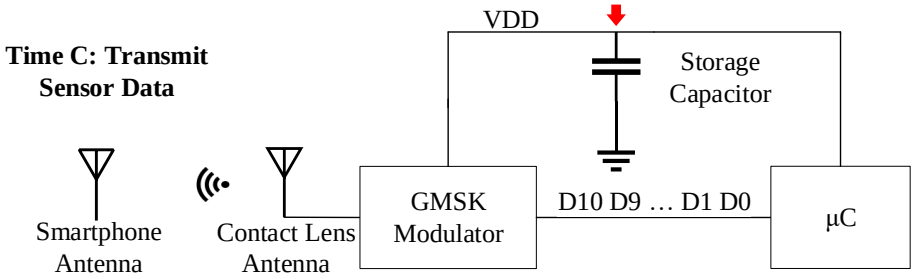
Energy Harvested	Power Generated [μW]	Time Active [s]	Energy [μJ]
Total	1.566	25	39.2
Energy Consumed	**Power Target [μW]**	**Time Active [s]**	**Energy [μJ]**
MEMS Oscillator	1	25.21	25.21
Potentiostat	0.3	20	6
Sensor Readout	6	200 m	1.2
Digital	10	211 m	2.11
Bluetooth TX	250	1 m	0.25
Total	-	25.21	34.77



(a) Smartphone powering the device with RF energy while potentiostat activates sensor.



(b) ADC digitizes sensor current.



(c) RF Modulator transmits sensor data to the smartphone.

Figure 1.4: System timing overview

1.3.3 Glucose Sensor Specifications

The key principle behind an electrochemical glucose sensor is a reduction-oxidation (redox) reaction that releases a number of electrons in proportion to the concentration of the reactants. Glucose sensors function by converting glucose into gluconic acid (gluconolactone). This reaction is catalyzed with immobilized glucose oxidase (GOD). A biproduct of this reaction, hydrogen peroxide (H_2O_2), is then oxidized, and the free electrons are sensed in the reaction as shown below:

$$\begin{aligned} &D\text{-}glucose + O_2 \xrightarrow{GOD} H_2O_2 + D\text{-}gluconolactone \\ &H_2O_2 \rightarrow 2H^+ + O_2 + 2e^-. \end{aligned} \tag{1.5}$$

When H_2O_2 is oxidized, electrons flow in the external circuit. The amount of current flowing is proportional to the glucose concentration [9].

The sensor requirements derive from the physical characteristics of the sensor. Assuming a sensor geometry similar to [2], 2 nA$-$40 nA of current is to be sensed, which corresponds to a 0.05 mM$-$1 mM glucose concentration. The system is designed to target 0.1 nA resolution for input currents in the 1 nA-100 nA range, while applying a 0.4 V bias to the sensor to facilitate the reaction. This corresponds to 10-bit ADC resolution. These specifications must be satisfied while also meeting the corresponding block-level power requirements.

1.3.4 Low-Voltage, Low-Power Design

To meet the strict power budget detailed in Table 1.2, a reduced supply voltage V_{dd} is employed. The technology used in this thesis is a 45nm CMOS RF silicon-on-insulator SOI technology (45RFSOI) offered by Global Foundries [17]. The 45RFSOI process is an offshoot of a digital 45nm process (12SOI) with higher resistivity substrates and thicker top metals to improve performance of RF passives. The nominal supply voltage in this technology is V_{dd} at 1 V, however, the supply voltage used throughout the system is 0.5 V. For digital circuitry, the dynamic power consumption $P_{dynamic}$ is given by [18]

$$P_{dynamic} = CV_{dd}^2 f_{clk} \alpha, \tag{1.6}$$

where α is the activity factor, C is the capacitance switched by digital circuitry, and f_{clk} is the switching frequency of the circuitry. Ideally, the digital circuitry power consumption

should be reduced by 75% as a result of the reduction in supply voltage from 1 V to 0.5 V which applies to the digital portion of the wireless transmitter and sensor readout circuitry. For analog circuitry, most circuits are designed with a specific bias current I_{dd} in mind, thus, the DC power P_{dc} saved when operated at 0.5 V supply should be ideally be 50% as seen from eq. 1.7:

$$P_{dc} = V_{dd} I_{dd}. \tag{1.7}$$

However, the reduction in supply voltage affects other parameters such as voltage swing, signal-to-noise ratio, frequency response, offset, etc. which may require a change in bias current. For example, transistors in the CMOS technology employed which have a threshold voltage V_{th} of 0.3 V to 0.4 V may be forced to operate in the subthreshold region ($V_{gs} < V_{th}$), due to the limited headroom available. In subthreshold, the transistors are inherently slower (reduced bandwidth) due to their reduced transition frequency f_T as they either have low transconductance g_m or large width which implies higher parasitic capacitance (i.e., high gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd}), as described in eq. 1.8

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}. \tag{1.8}$$

For example, in an LC-based voltage-controlled oscillator (VCO), high parasitic capacitance affects the frequency tuning range. Moreover, subthreshold operation causes the system to be more sensitive to process, voltage, and temperature variation; as the drain-source current (I_{DS}) is now exponentially related to temperature through thermal voltage V_t, according to

$$I_{DS} = I_{D0} \frac{W}{L} e^{(V_{GS}/(nV_t))}(1 - e^{-V_{DS}/V_t}), \tag{1.9}$$

where V_t is given by $V_t = \frac{kT}{q}$, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, I_{D0} is a process constant which varies with temperature, n is a process constant greater than 1 and W/L is the width-to-length ratio (aspect ratio) of the transistor.

1.4 Thesis Organization

The following chapters are organized to guide the reader through the relevant background and contributions by this thesis. Chapter 2 describes the prior art and delves into topology selection for relevant subsystems including: Bluetooth protocol, integer-N phase-locked

loops (PLL), switching power amplifiers, electrochemical sensors, and sensor readout circuitry. Chapter 3 details the design and simulation of the low-power wireless transmitter. Chapter 4 focuses on the design and simulation of the potentiostat and sensor readout circuitry. Chapter 5 presents chip-level implementations of the system, and compares the experimental data with simulation results. Lastly, Chapter 6 provides conclusions on the body of work completed and provides topics for future research.

Chapter 2

Literature Survey and Topology Overview

This chapter initially reviews similar low-energy RF sensor systems in the literature. Following this, the chapter moves on to describe the different aspects of the proposed system. Specifically, a brief overview of each subsystem is given to arrive at key topologies and specifications to be discussed in detail in the following chapters.

2.1 Review of Wireless Sensor Systems

Much research has been conducted on both system level designs as well as various circuit subsystems for wireless glucose sensors. A summary of the literature published on wireless glucose sensors (but not necessarily for contact lens-based applications) is presented in Table 2.1 and Table 2.2. In addition, previous work in this area by Liao et al. [2], Zhang et al. [5] and Xiao et al. [6] are described in detail.

Table 2.1: Performance summary of energy harvesting wireless biosensors.

	JSSC '12 [2]	JSCC '13 [5]	TBCAS '09 [19]	TCSII '15 [20]	ISCAS '15 [21]
General					
Application	Contact Lens Glucose Sensor	Batteryless EEG Sensor	Blood Glucose Implant	Low Voltage Potentiostat	Potentiostatic Glucose Sensor
V_{DD}	1.2 V	1.2 V AFE / 1 V LO / 0.5 V PA+DSP	1.8 V	1 V	1.8 V
Power Consumption	3 μW	19 μW	198 μW	22 μW	72 μW
	Regulator+Bandgap: 1 μW Ring Oscillator: 600 nW Potentiostat: 500 nW Digital: 400 nW	Supply Regulation: 3 μA TX: 0.14 μA with heavy duty-cycling AFE: 4 μA Digital: 4.6 μA	- - - -	Potentiostat: 22 μW - - -	Potentiostat: 11.5 μW - TIA: 40.3 μ -
Technology	0.13 μm	0.13 μm	0.18 μm	0.35 μm	0.18 μm
Chip size/Core Size	0.36 mm^2	8.25 mm^2	1.69 mm^2	0.13 mm^2	0.046 mm^2
Energy Harvesting Performance					
Energy Source	RF	Thermal+RF	Inductive	-	-
Input Harvesting Power	30 dBm	60 μW+10 dBm kick	-	-	-
Rectifier+Regulator Efficiency	20%	35%	-	-	-
Energy Storage Capacitor	500pF on-chip	off-chip	22nF off-chip	-	-
RF Performance					
Modulation scheme	FM-LSK	BFSK	LSK	-	-
Carrier Frequency	1.8 GHz	400 MHz	13.56 MHz	-	-
Output Power	-	-18.5 dBm	-	-	-
Sensor Performance					
WE Material CE Material RE Material	Ti/Pd/Pt + GOD Ti/Pd/Pt + GOD Ti/Pd/Pt + GOD	- - -	Ti/Ni/Au Ti/Ni/Au Ag/AgCl	Pt/Ag Pt/Ag Pt/Ag	VACNF Ag/AgCl Ag/AgCl
WE-RE Cell Voltage	0.4 V	-	0.6 V	0.7 V	0.781 V
Glucose level	0.05 mM - 2 mM	-	0-40 mM	2 mM-22 mM	0.5 mM - 25 mM
Settling Time	15 s	-	2 min	100 s	-
Potentiostat Performance					
Architecture	Current-Mirror	-	Current-Mirror	Current-Mirror	TIA
Current Range	50 pA - 150 nA	-	1 nA - 1 μA	70 nA - 2.6 uA	100 nA-5 μA
Sensor Readout Performance					
Topology	I-to-F Differential Ring Osc.	-	I-to-F Inverter Feedback	I-to-F Converter	Ring VCO
Resolution	400 Hz/mM	-	-	233 Hz/mM	100 kHz/mM

Table 2.2: Performance summary of energy harvesting wireless biosensors continued.

	VLSIC '14 [22]	JBHI '15[6]	JBHI '16 [23]	BioCAS '11[24]
General				
Application	Implantable CGM	Implantable RFID CGM	NFC Glucose Implant	Wireless Glucose SoC for CGM
V_{DD}	1.2 V	1.2 V AVDD/1.0 V DVDD	2.85 V AVDD/1.5 V DVDD	-
Power Consumption	6 μW	50 μW	760 μW	50.1 μW
	- - - -	RFID: 28 μW ADC: 3 μW Potentiostat: 4 μW Digital: 15 μW	ADC: 510 μW RF: 250 μW - -	Regulator+Bandgap: 10.5 μW Readout: 13.2 μW Potentiostat: 3.6 μW ADC: 132 nW
Technology	0.18 μm	0.13 μm	0.6 μm	0.13 μm
Chip size/Core Size	1.96 mm^2	2.4 mm^2	10 mm^2	10
Energy Harvesting Performance				
Energy Source	Inductive	Inductive	Inductive	Inductive
Input Harvesting Power	22 dBm@ 5 mm tissue+5 mm air	20 dBm @ 3 cm	-	-
Rectifier+Regulator Efficiency	60%	45%	72%	35%
Energy Storage Capacitor	400 pF on-chip	on-chip	on-chip	1 nF
RF Performance				
Modulation scheme	LSK	LSK	LSK	LSK
Carrier Frequency	900 MHz	13.56 MHz	13.56 MHz	13.56 MHz
Output Power	-	-	-	-
Sensor Performance				
WE Material CE Material RE Material	Pt Pt Ag/AgCl	- - -	- - -	- - -
WE-RE Cell Voltage	0.4 V	0.2 V	-	-
Glucose level	0 - 20 mM	0 -30 mM	-	-
Settling Time	-	-	-	-
Potentiostat Performance				
Architecture	TIA	Current-Mirror	-	-
Current Range	20 pA-500 nA	0-20 nA	-	10 fA - 100 pA
Sensor Readout Performance				
Topology	Dual-Slope ADC	Delta-Sigma ADC	Delta-Sigma ADC	SAR ADC
Resolution	7-bit	10-bit	11-bit	8-bit

2.1.1 System by Liao et al.

The aforementioned work by Liao, et al [2] is the only complete contact-lens-based wireless glucose sensor this author is aware of to date. The system block diagram is shown in Figure 2.1 and key specifications are summarized in Table 2.1.

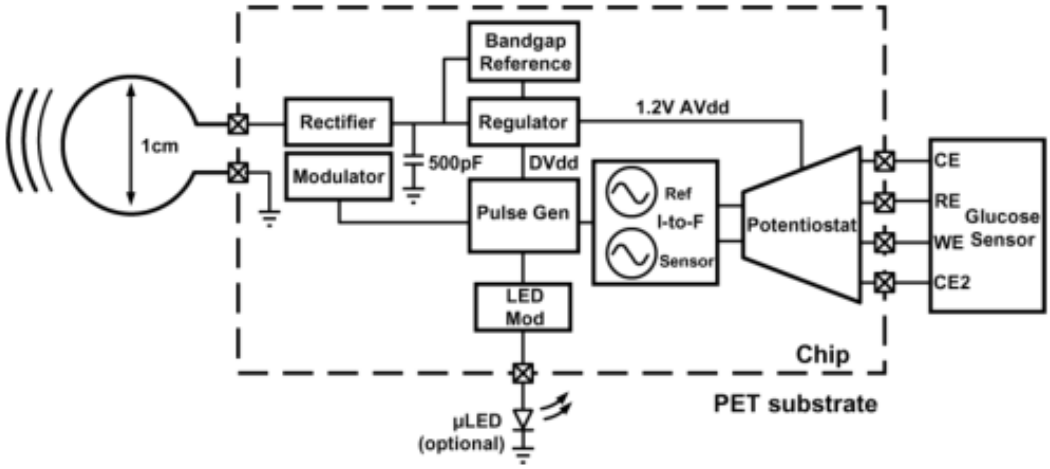


Figure 2.1: System architecture of [2]

The 1 cm loop antenna is area limited by the contact lens itself. The system voltage is a rectified continuous-wave (CW) 1.8 GHz signal from an external device. This voltage is then regulated to 1.2 V for the rest of the system. Once the system receives regulated power, it measures current from the glucose sensor via a current-mirror based potentiostat. The sensor implemented includes two CE terminals; one which senses glucose current while the other node only senses background noise current. The sensor and reference currents are converted to frequency directly through a current-starved ring oscillator. This choice was made to save power associated with an explicit ADC. Since the wireless transmitter is based on a backscattering scheme (modulating the reflection coefficient seen by the external device) via pulse width modulation to an NMOS switch, frequency data from the ring oscillator is sufficient to transmit sensor information. The entire system consumes 3 μW. As mentioned previously, one key drawback is the use of an arbitrary wireless protocol and frequency, which is not inter-operable with existing mobile phones. This

paper provides the basis for many of the assumptions made in later chapters regarding the key specifications and assumptions.

2.1.2 System by Zhang et al.

Given the limited literature on contact lens-based wireless glucose sensors, we compare the system with other implemented systems. For example, a 19 μW energy harvesting EEG wireless sensor is implemented in [5] (block diagram shown in Figure 2.2).

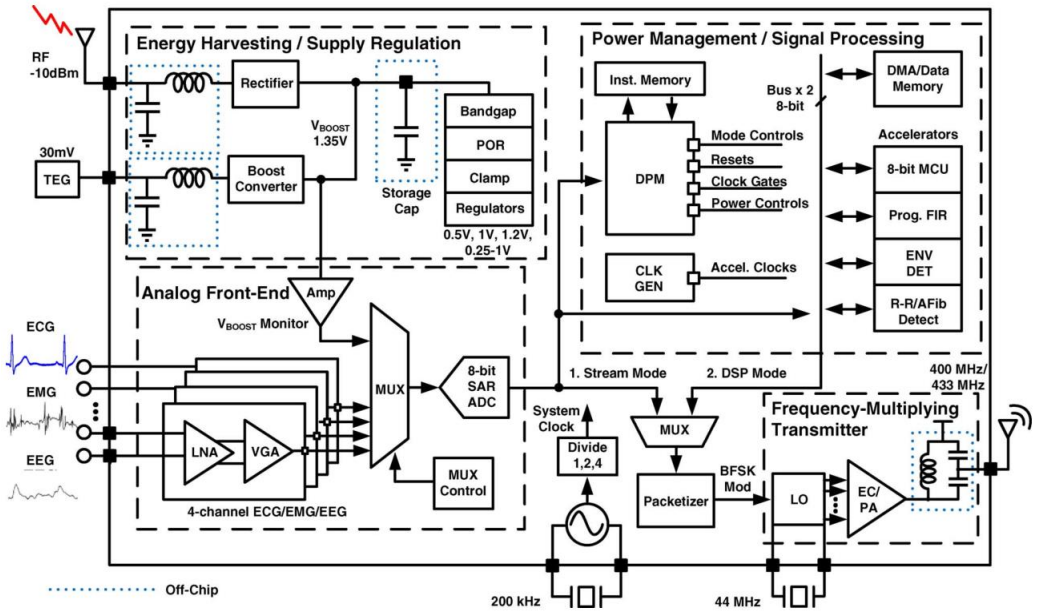


Figure 2.2: System architecture of [5]

The system primarily harvests thermal energy using an RF pulse as an initial startup kick to the thermal harvesting boost converter. The RF pulse is necessary due to the low voltages the thermal harvester is able to generate given the temperature delta and physical area of the harvester. Thus the RF pulse is used to kick-start the regulator boost circuitry. The RF transmitter is implemented using an injection locked 9-stage ring-oscillator at 1/9th the output frequency of 402/433 MHz. The modulation scheme implemented was BFSK, which is achieved by direct modulation of the reference crystal oscillator. Frequency

multiplication is achieved via a phase interpolated switching PA. this reduces the oscillator power consumption as it oscillates at a lower frequency. The RF subsystem burns 160 μW of power when active. The transmitter is heavily duty-cycled in order to drive down the power of the overall system.

2.1.3 System by Xiao et al.

The topology in [6] is particularly interesting, as the sensor subsystem is similar to the circuits implemented in this thesis. The system is a glucose sensor tag to be implanted in the arm of the diabetic patient in order to sense blood glucose directly. Figure 2.3 shows the system overview:

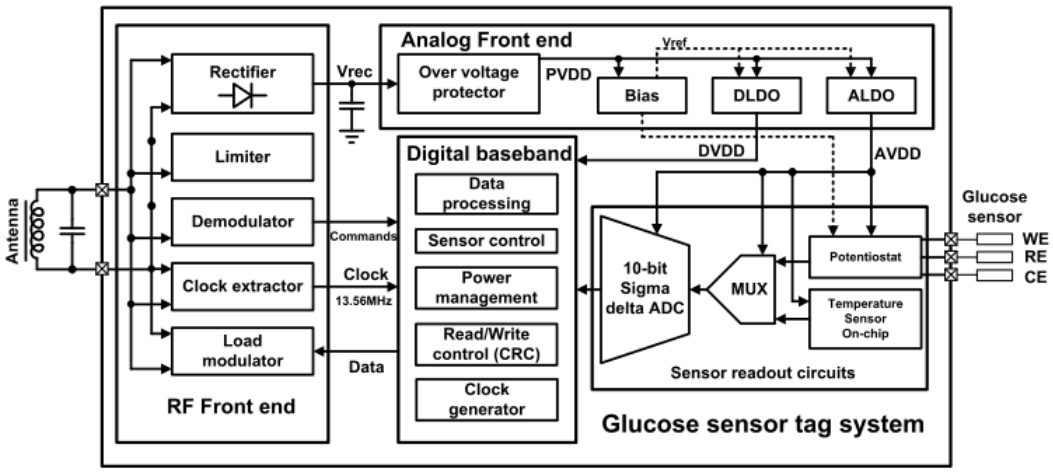


Figure 2.3: System overview of [6]

The system includes an off-chip resonant tank which is used for energy harvesting as well as communication. The system uses near-field inductive charging which couples energy from a -3.5 dBm source at a distance of 5 mm from the implant, through arm tissue. This RF energy is rectified and regulated to 1.2 V/1 V to power the rest of the system. The RF transmission is done through load-shift keying (LSK) whereby the system does not generate RF energy, but transmits data by modulating the antenna impedance in the presence of

an RF signal transmitted by an external device. The sensor subsystem uses a potentiostat to measure glucose current from an external glucose sensor. This current is mirrored and read-out by a 10-bit incremental delta-sigma ADC. The overall DC power consumption of the system is 50 μW.

Many other complete systems compared are shown in Table 2.1 and Table 2.2. In summary, they all attempt to harvest energy using back-scattering RFID schemes, mainly at 13.56 MHz. While 13.56 MHz is available on mobile phones as near-field communication (NFC), the required antenna would need to be much larger than the space available on the contact lens.

2.2 Review of Wireless Sensor System Components

2.2.1 Review of Bluetooth Transmitters

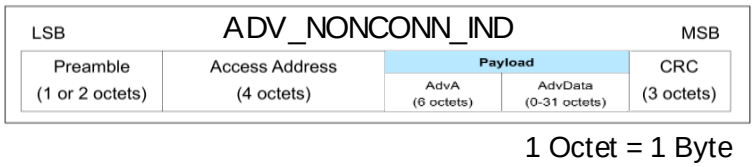
As mentioned earlier, this thesis proposes an energy harvesting system that uses Bluetooth Low Energy (BLE) at 2.4 GHz. Bluetooth is available in all modern mobile phones, and its operating frequency is high enough for an electrically-small antenna to fit on a contact lens.

Bluetooth Protocol

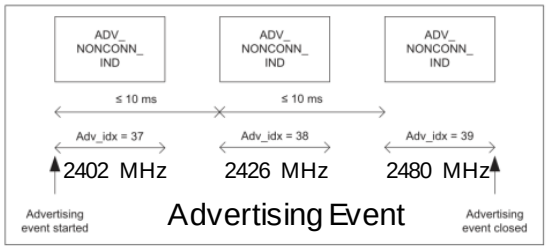
To use Bluetooth in an energy harvesting system, it is imperative that only the necessary parts of the protocol are implemented. This would to reduce circuit complexity and communication time to ultimately reduce the energy consumption. As mentioned previously, an advertising-mode-only approach was taken. This mode allows the system to only require a transmitter rather than a transceiver, saving power. Furthermore, advertising mode does not require the transmitter to use the 37 data channels, and it also does not require collision avoidance frequency hopping, reducing the digital system complexity.

Advertising mode can be used to send many different message types. For example, one message type allows the reciever to respond without switching from advertising mode to connected mode. The non-connectable non-scannable advertising packet is used in this system. This broadcasts data to any device listening to any of the advertiser channels. The packet is sent on all three advertising channels sequentially as shown in Figure 2.4. The packet can be 14-47 bytes long, depending on the data length. Assuming 47 bytes are transferred, the transfer time per advertising channel is 376 μs. Accounting for overhead,

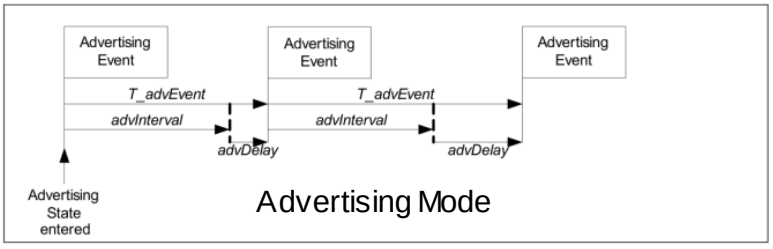
this implies a complete advertising event can be completed in approximately 2ms. To read this information, the reader (mobile phone) would be scanning for any packets on one of the advertising channels; the choice of channel is at the reader's discretion as the same information would be transmitted on all three advertising channels.



(a) Non-connectable, non-scannable, undirected advertising packet



(b) Advertising event timing consisting of a packet sent on all three advertising channels



(c) Timing in-between advertising events

Figure 2.4: Non-connectable non-scannable advertising event structure[1]

However, one drawback is that, in order to send subsequent advertising events, the transmitter would be required to wait 20 ms - 30 ms between events. This idle time is quite costly to the energy budget, and although the transmitter could be power-gated within this time frame, the system implemented in this work opts to only send one advertising event to save energy.

Low-Power Transmitter Topologies

Bluetooth employs Gaussian minimum shift keying (GMSK), which is equivalent to Gaussian filtered frequency shift-keying (GFSK) with a modulation index m of 0.5. The binary data is filtered by a Gaussian filter, which then modulates the carrier frequency by half the bit-rate. The output signal $x_{GMSK}(t)$ can be expressed as

$$x_{GMSK}(t) = Acos(w_c t + K_{VCO} \int x_{BB} * h(t)dt), \tag{2.1}$$

$$\begin{aligned} x_{GMSK}(t) &= Acos(w_c t)cos(\theta) - Asin(w_c t)sin(\theta), \\ where: \quad \theta &= K_{VCO} \int x_{BB} * h(t)dt, \end{aligned} \tag{2.2}$$

where K_{VCO} corresponds to the voltage to frequency gain of the voltage controlled oscillator (VCO), and $x_{BB}(t) * h(t)$ refers to the gaussian filtered baseband data signal.

There are two methods used to implement GMSK modulation. The most direct approach is to modulate a VCO directly with Gaussian shaped data. However, given that VCOs are prone to frequency drift over time, two-point modulation (shown in Figure 2.5) is used to implement eq. 2.1. In this scheme, the VCO is part of a frequency synthesizer circuit. The synthesizer uses 1-MHz reference clock to set the carrier to the selected channel (i.e., 2402/2426/2480 MHz). The signal data modulates both the reference and the RF VCO simultaneously to output the GMSK data. Both oscillators are modulated simultaneously such that the loop does not distort the incoming data stream.

The second is shown in Figure 2.6. Here, data is split into in-phase and quadrature (IQ) paths, and recombined after mixing with in-phase and quadrature of the carriers respectively. This scheme implements eq. 2.2.

There are clear tradeoffs between the two methods. The two-point modulation is simpler to implement, as it requires fewer circuit blocks and, consequently, requires less power. However, a disadvantage is that the modulation index depends on the gain of the VCO, which varies with circuit processing and is therefore difficult to control. In addition, the

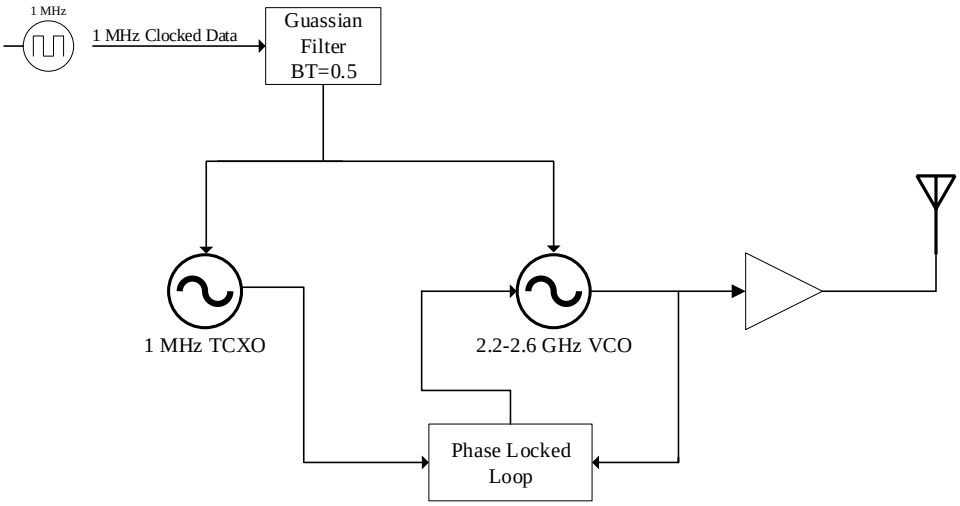


Figure 2.5: Two-point GMSK Transmitter Architecture

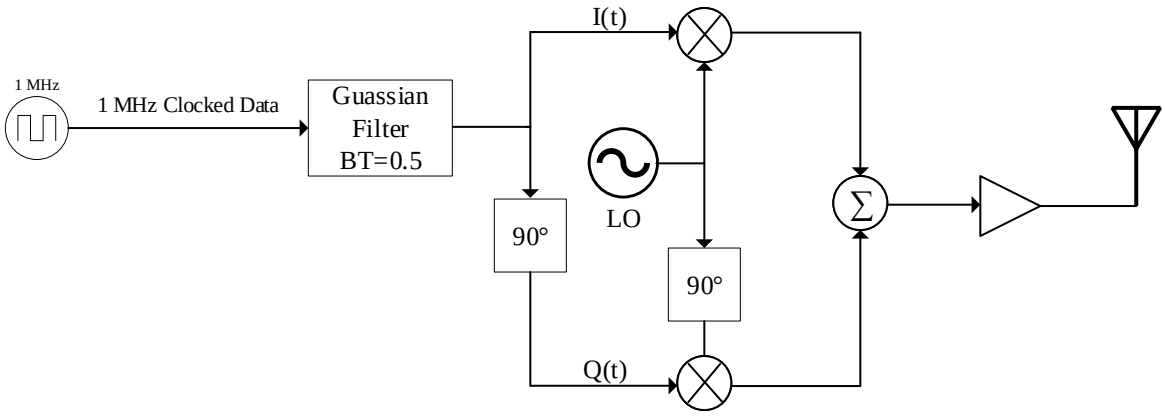


Figure 2.6: I/Q based GMSK Transmitter Architecture

baseband data amplitude must be controlled to ensure that the correct frequency spacing is achieved [25]. On the other hand, the I/Q method allows for precision in setting the modulation index if accurate phase shifts are applied to the LO and input data. This precision comes at the cost of complexity and power, as the LO frequency needs to be con-

trolled precisely and quadrature phases are required (which implies a PLL and LO driver circuitry). The mixer blocks also add power consumption depending on their implementation. Since power consumption is the most important aspect of the glucose monitoring system, the two-point scheme is chosen.

Review of Integer-N Phase-Locked Loops

Two-point modulation for Bluetooth in advertising mode requires a PLL that is able to select three advertising channels (2402/2426/2480 MHz). A PLL is a feedback control system that reduces the phase error between a reference signal and a fedback signal to a value as close to zero as possible. This is beneficial for frequency synthesis due to:

$$\begin{aligned} \phi_{error} &= \phi_{ref} - \phi_{feed} \\ \phi_{error} &\rightarrow \epsilon \\ f_{error} &= \frac{\mathrm{d}\phi_{error}}{\mathrm{d}t} \\ f_{error} &= 0 \end{aligned} \tag{2.3}$$

where ϕ_{error} represents the dynamic phase error due to a change in the input phase ϕ_{ref} to the fedback phase ϕ_{feed} and f_{error} corresponds to frequency error associated with ϕ_{error}. Furthermore, the PLL must be able to switch between various frequency channels accurately. The conceptual system is shown in Figure 2.7.

Generally, the reference oscillator is a low-frequency high spectral purity signal that is fixed at one frequency. Therefore, to accurately generate an RF carrier at a higher frequency than the reference input, the output frequency is divided before being compared at the input. If the divider value is represented by N, this implies that

$$F_{OUT} = NF_{REF}, \tag{2.4}$$

where F_{OUT} represents the output frequency, and F_{REF} represents the reference frequency. There are two types of PLLs classified by how the divider value is set: integer-N PLLs and fractional-N PLLs. Fractional-N PLLs allow for higher reference frequencies while still being able to synthesize closely-spaced frequency channels by using fractional division ratios. This permits higher system bandwidth and thus faster settling time. However, the cost is added complexity, power consumption and increased spurious output. Integer-N PLLs are simpler and therefore are more power efficient. For this application, the PLL

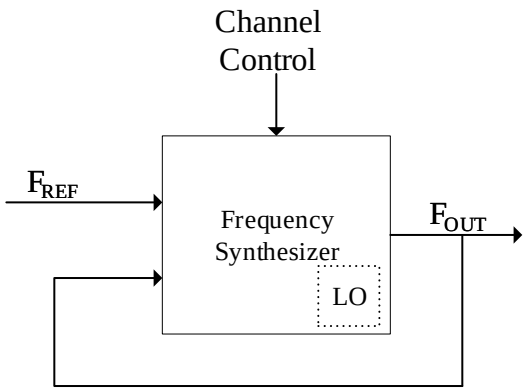


Figure 2.7: Conceptual RF Synthesizer [7]

only needs to switch between three channels. Moreover, the speed of channel selection is not critical as compared to the overall power consumption. Hence, the integer-N architecture was chosen.

A PLL used to enable integer channel spacing is shown in Figure 2.8. In this architecture, the reference is compared to a divided output frequency with a phase-frequency detector (PFD). The PFD outputs pulses to the charge pump (CP) to either speed up or slow down the PLL. The charge pump will either raise or lower the control voltage based on these pulses, as it drives current to/from the passive network. This voltage change will increase/decrease the output frequency, which will be fed back to the input through the divider, completing the feedback system.

To analyze the feedback system, a continuous-time approximation of the discrete time system in the phase domain can be made that assumes that the loop bandwidth is approximately at most less than one-tenth, the reference frequency. Figure 2.9 shows that the system has two integrator poles, which is defined a type-2 PLL. The system is stable due to the zero in the open loop transfer function.

The major contributor to the power consumption of the PLL is the VCO. The power consumed by the VCO stems from two main metrics: the transconductance needed for the system to oscillate and the phase noise requirements of the oscillator. To meet these requirements, a CMOS cross-coupled LC VCO is chosen to reduce the supply voltage while still providing enough transconductance. This circuit can be seen in Figure 2.10.

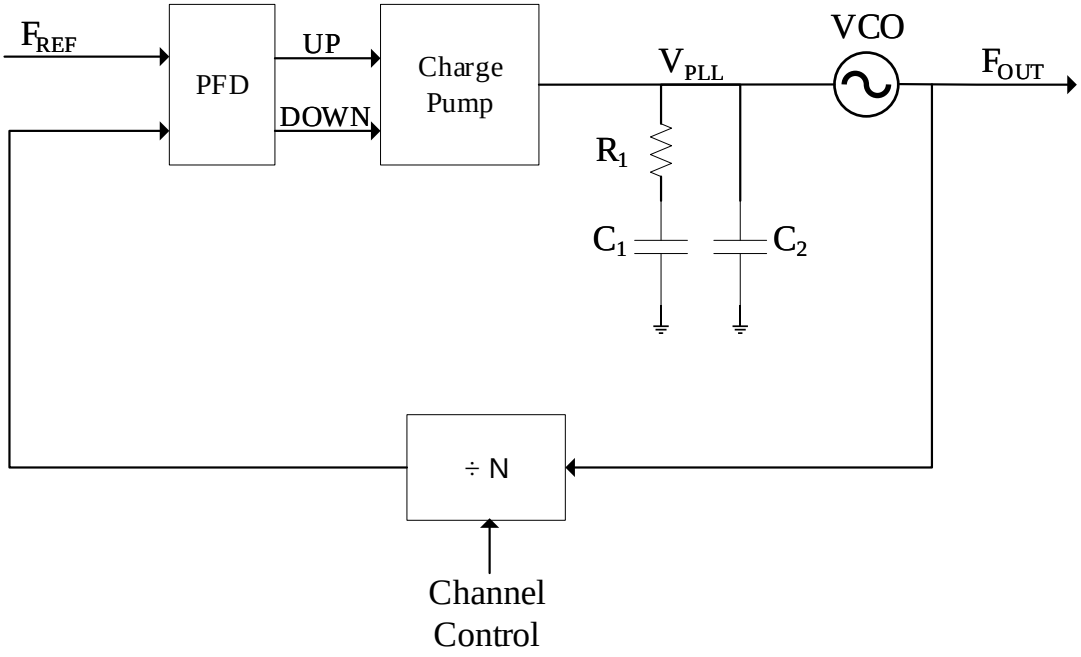


Figure 2.8: Integer-N PLL [7]

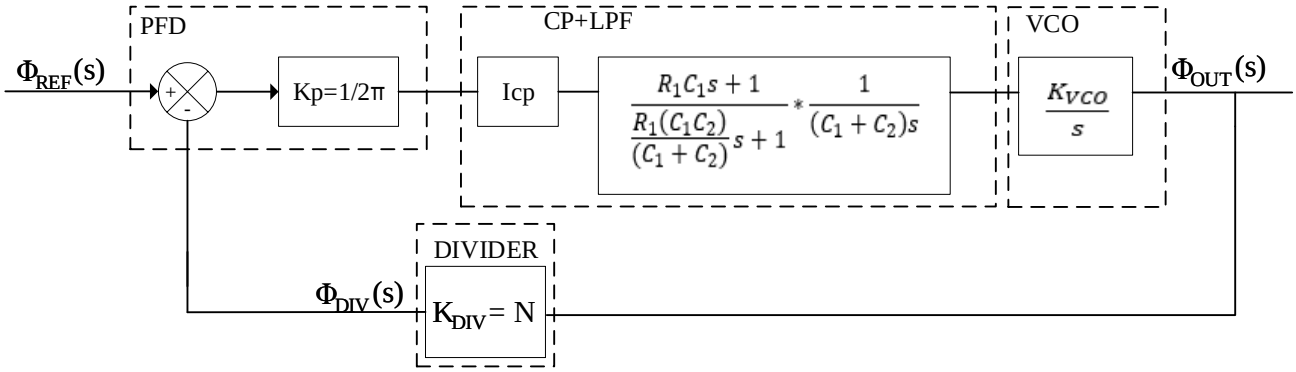


Figure 2.9: A block diagram of the PLL in the frequency domain.

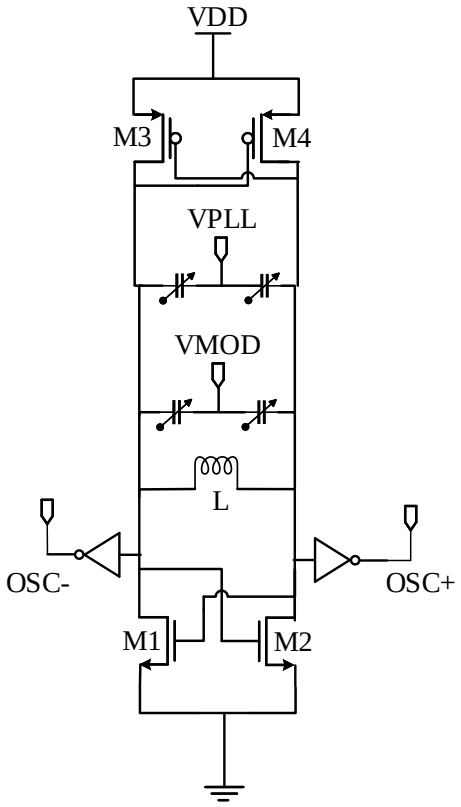


Figure 2.10: CMOS LC VCO-without tail current source [7].

From Barkhausen's stability criterion:

$$\begin{aligned} |\beta A| &= 1, \\ < \beta A &= 2\pi n, n \in \mathbb{W}, \end{aligned} \tag{2.5}$$

where $\beta A = 2g_m R_p$ is the loop gain of the feedback system, and R_p is the equivalent impedance shown by the LC-tank at resonance, which is generally set by the Q-factor of the inductance and is thus somewhat process specific. Therefore, $g_m = \frac{1}{2R_p}$ in order to meet the oscillation criteria. This topology provides the lowest g_m required to oscillate, and thus was chosen so that less bias current is required, thereby reducing the power consumption.

To implement the PFD, a digital state machine was used so that the input reference and feedback signal can be non-linear, reducing the overall system power consumption. For the

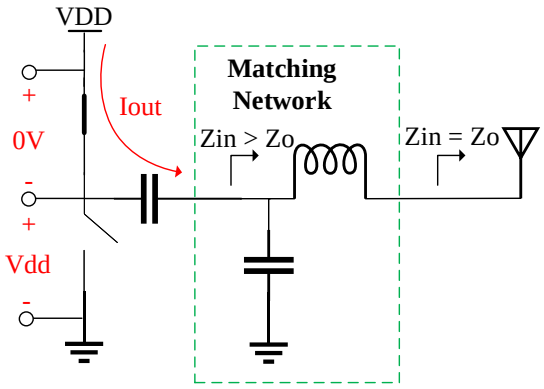
charge pump, a simple current mirror implementation with digital switches was used due to the reduced headroom available. Charge pumps suffer from mismatch due to channel length modulation. Thus, more advanced charge pumps implement error correction using feedback to match the current sources. These topologies were not implemented to save power. Furthermore, the reference spur specifications are relaxed for this application. Finally, the digital divider is designed using a swallow counter and a dual-modulus prescaler. Sequential logic was designed using dynamic logic circuits in order to reduce power consumption [7].

Switching-Mode Power Amplifiers

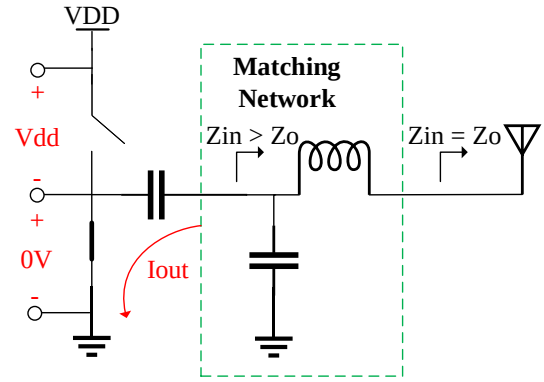
To transmit the sensor data to the antenna, a power amplifier circuit is required. Power amplifiers are designed to deliver RF power to the load while consuming as little DC power as possible. For this application, the transmitter is required to transmit $>$ -20 dBm of power. Furthermore, the output waveform can be heavily distorted, as information is encoded in the frequency rather than the amplitude. These requirements lend themselves to switching-mode amplifiers.

Class-D amplifiers are switching-mode amplifiers that can ideally realize close to 100% efficiency. An example switching amplifier is shown in Figure 2.11. In Class D, the switch either carries current $I_{SW}(t)$, or sustains a voltage drop $V_{SW}(t)$, but not both simultaneously. This implies that no power is consumed by the switches.

Typical power amplifier designs attempt to deliver the maximum power from the transistor to the load while being as efficient as possible. However, this design requires the transistor to output much less RF power (i.e., -20 dBm, or 10 μW) while still being efficient. Since a Class-D amplifier essentially act as a voltage divider between R_{sw} and R_{Load}, the output power is set by their combined impedance. Thus, to output less power, either the load or switch impedance must increase. However, increasing the switch impedance will reduce the power efficiency, thus, a matching network is inserted to increase the impedance presented by the antenna. An L-section matching network that uses a shunt capacitor and series inductor was chosen specifically because the inductor can be absorbed by the antenna impedance itself with careful antenna design.



(a) High side switch enabled



(b) Low side switch enabled

Figure 2.11: Ideal Class-D PA

Bluetooth Transmitter Prior Art

Despite efforts to reduce the power consumption of the Bluetooth physical layer (PHY) with the introduction of BLE, the power consumption is generally far too high for energy harvesting applications. Table 2.3 summarizes recent BLE implementations in the literature.

Table 2.3: Performance summary of BLE transmitters

	TMTT '13 [26]	TCAS '18 [27]	JSSC '16 [28]
V_{DD}	1 V	1 V/3 V	0.5 V/1 V
Technology	0.13 μm	55 nm	28 nm
Power Consumption	5.9 mW	3.9 mW	5.8 mW
VCO	0.4 mW	0.7 mW	0.4 mW
Dividers	-	0.5 mW	0.2 mW
PFD+CP	0.27 mW	-	0.6 mW
PA	5.3 mW	2.5 mW	4.4 mW @ Pout=0dBm
Chip size/Core Size	2.1 mm^2	0.53 mm^2	0.65 mm^2
Osc. PN @ 1MHz (dBc/Hz)	-110	-119	-116
Osc. FOM(dB) [1]	-	-	188
Osc. tuning range	-	-	2.05-2.55 GHz
PLL in-band PN (dBc/Hz) [2]	-80	-81	-92 @Fref=5 MHz / -101 @Fref=40 MHz
Integrated PN (degree)	-	-	1.08 @Fref=5 MHz / 0.87 @Fref=40 MHz
PLL FOM (dB)	-	-	-238
PLL settling time (μs)	-	-	15
Reference/Fractional spurs (dBc)	-75/-46	-	-80/-60
TX Modulation error	-	3.48%	2.70%
Output Power (dBm)	1.6	1.6/10	-5 to +3
TX efficiency	24.5%	24%	23-28% @ Pout=0 dBm
Total PA efficiency	-	-	41%
On-chip matching network	Yes	No	Yes

[1] Oscillator FOM represents the oscillator figure of merit
[2] PLL FOM represents the PLL figure of merit

For example, an all-digital-PLL-based direct FSK modulation transmitter implemented in [27] achieves an overall power consumption of 3.9 mW. The design uses an open-loop direct modulation scheme where the PLL is only used to set the carrier frequency to reduce power. However, the PA itself consumes 2.5 mW for an output power of 1.6 dBm. Another general purpose Bluetooth transceiver is implemented in [28], which achieves an overall power consumption of 3.7 mW. Of that, 3.1 mW of that power is again allocated to the PA in order to output 0 dBm of RF power. Systems where the power consumption is dominated by the PA are reasonable when building a general purpose Bluetooth link, as output power directly affects the range of operation. However, this is unnecessary for the proposed contact-lens glucose system as the mobile phone RX must be a short distance away to allow the TX to harvest energy anyway. This implies that the TX power can be -20 dBm, the absolute minimum allowed by the specification.

An attempt to merge the ubiquity of Bluetooth devices with the power savings of RFID techniques is presented in [8]. The idea is illustrated in Figure 2.12. A continuous-wave (CW) source provides an RF signal for which the BLE reflects a FSK modulated signal to the receiver. The concept also relies on the use of advertising-only Bluetooth operation to reduce baseband and RF complexity. This enabled a range of 13m between the tag and mobile device. Applying this concept to the proposed contact-lens system is not feasible, however, because the CW-source must be continuously powered to allow the modulation to occur. Furthermore, the tag is designed on a printed circuit board (PCB), which cannot be mounted on a contact lens. The range would also likely diminish given the electrically-small antenna length available on the contact lens itself.

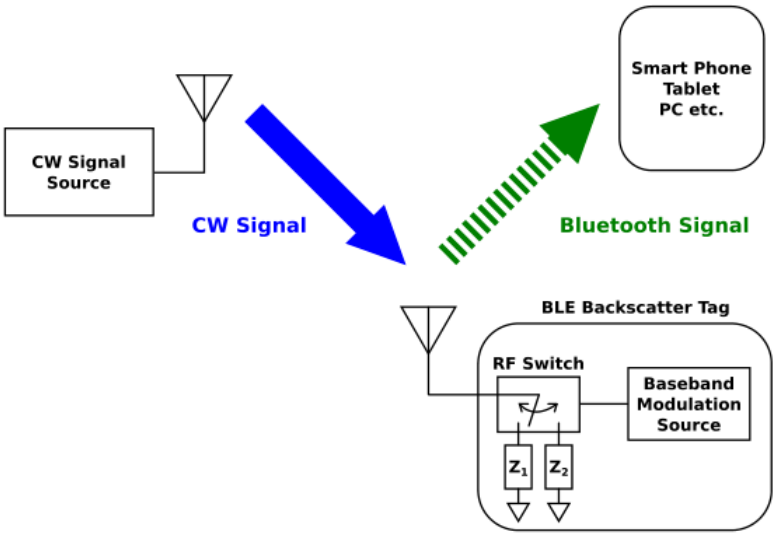


Figure 2.12: System architecture of [8]

Thus, part of the focus of this thesis is to design BLE compliant PHY which has dramatically lower power consumption.

2.2.2 Review of Electrochemical Glucose Sensors

Electrochemistry is the study of chemical reactions that cause electron transfer between a conductor and an electrolyte [9][10]. A typical three-electrode electrochemical cell consists of a working electrode (WE), reference electrode (RE) and counter electrode (CE). This is shown in Figure 2.13.

To sense glucose, one could either oxidize glucose directly, or use an enzymatic oxidation of glucose to oxidize a by-product of that reaction. In either case, the free electrons generated by the reaction are driven by an external circuit. These reactions are comprised of two independent half-reactions, where the reaction of interest is at the WE, and the auxiliary half reaction is at the CE. The potential used to drive the reaction is set by the potential between WE and RE. This potential is referred to as V_{CELL}. This three electrode system allows V_{CELL} to be constant throughout the sensor current range. The minimum

V_{CELL} required to drive the reaction varies based on the sensor materials used. The WE and CE are generally formed using one or a combination of the following metals: platinum (Pt), titanium (Ti), nickel (Ni), silver (Au), gold (Ag), or palladium (Pd). In addition, enzymatic glucose sensors also coat the surface of the electrode with either glucose oxidase (GOD) or PQQ-glucose dehydrogenases to catalyse glucose [9]. Finally, reference electrodes are typically made with silver/silver chloride (Ag/AgCl).

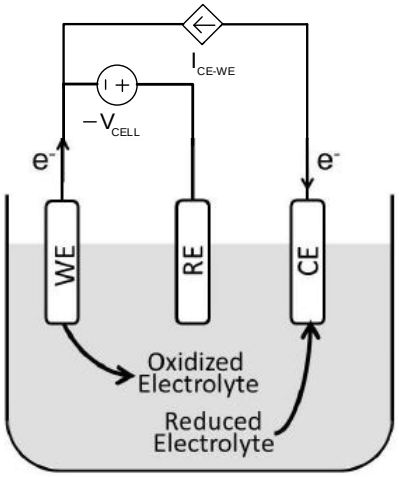


Figure 2.13: Standard three electrode system [9].

The design of the sensor is outside the scope of this thesis. However, a reference sensor is required in order to design low power driver circuitry. Therefore, this thesis is designed assuming the sensor designed by Liao et al. [2] is used and can be seen in Figure 2.14.

The physical dimensions of the sensor are critically important as they affect the electrical parameters of the sensor significantly, and are summarized in Table 2.4.

Table 2.4: Summary of Electrode Dimensions [2]

Electrode	Material	Area (mm^2)
WE	Ti/Pd/Pt with GOD	0.22
CE	Ti/Pd/Pt with GOD	0.33
RE	Ti/Pd/Pt	0.4

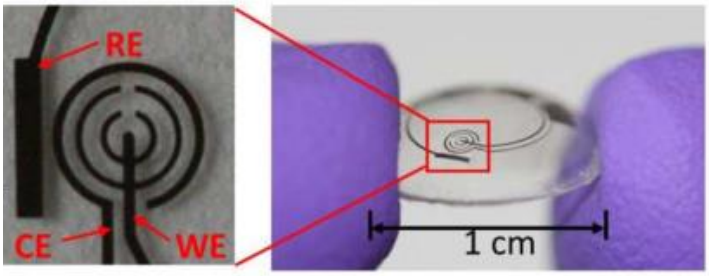


Figure 2.14: Contact Lens Glucose Sensor [2]

Electrochemical Cell Circuit Model

To design circuitry to drive the electrochemical cell, a circuit model must be developed. The standard cell model is shown in Figure 2.15. In this model, the dependent current source (I_{Sense}) represents the current flow from the sensing reaction. This appears on both the WE and CE to represent the two half reactions and keep the current flow consistent. $C_{Interface,WE}$, $C_{Interface,CE}$ and $C_{Interface,RE}$ represent the double layer capacitance formed between the electrode and the glucose solution. $R_{Interface,WE}$ and $R_{Interface,CE}$ model the static DC leakage (I_{Static}) through the electrodes. $R_{solution}$ models the loss within the solution. The sensor model parameters are strong functions of the dimensions (area) of the sensor, and their values are detailed in Table 2.5. For example, the capacitance at each electrode interface can be anywhere from 10-100 $\mu F/cm^2$ [10]. However, these parameters are difficult to predict accurately, and were not specified in the work carried out by [2]. As such, these parameters were extracted based on estimations of the size of the sensor, as specified in [10]. Due to the model uncertainty, the circuit design has been specified to handle one order of magnitude of variation above and below the nominal value for every component to account for model inaccuracy.

The total sensor current between the WE and CE (I_F) is:

$$I_F = I_{WEtoCE} = I_{Sense} + I_{Static}. \tag{2.6}$$

However, the expected leakage is insignificant and acts as a DC offset which can be calibrated out. Therefore,

$$I_F \approx I_{Sense}, \tag{2.7}$$

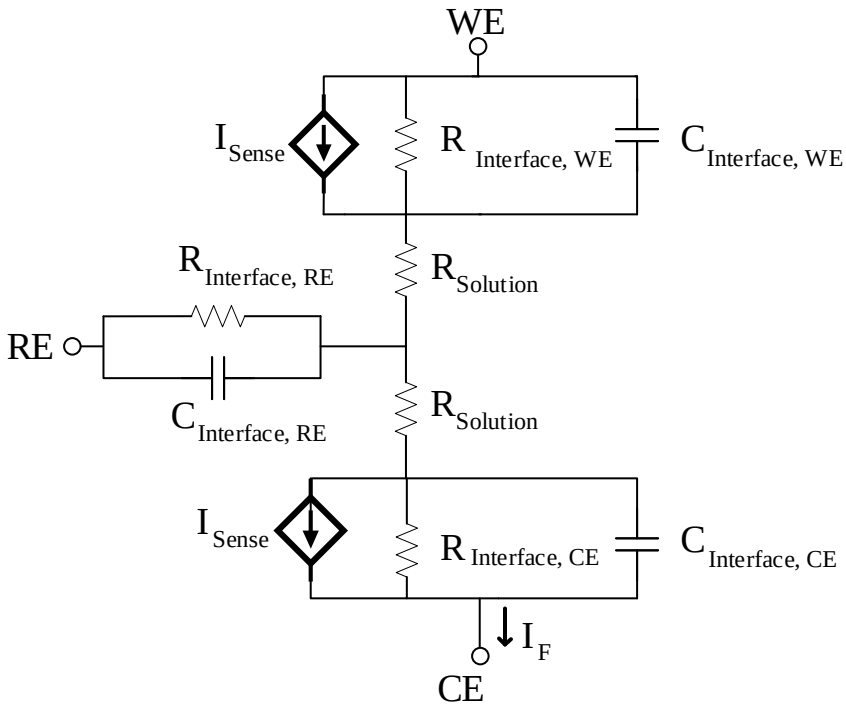


Figure 2.15: Model of Electrochemical Glucose Cell

for the remainder of this thesis.

Table 2.5: Parameters used to model the sensor implemented in [2]

Parameter	Electrode	Nominal Value
$R_{Interface,WE}$	WE	1 GΩ
$R_{Interface,CE}$	CE	0.666 GΩ
$R_{Interface,RE}$	RE	20 kΩ
$R_{Solution}$	-	10
$C_{Interface,WE}$	WE	110 nF
$C_{Interface,CE}$	CE	165 nF
$C_{Interface,RE}$	RE	10 pF
I_{sense}	-	1-100 nA

Potentiostat Architecture and Prior Art

To drive the reaction, a potentiostat circuit is used to set the voltage between WE and RE by sinking/sourcing the glucose sensor current from the CE. In addition, the glucose sensor current flowing from CE to WE needs to be measured.

The main topology used to set the potentiostat voltage is the grounded WE topology. An example of this is shown in Figure 2.16. This topology uses two amplifiers to set the voltage V_{CELL} between the WE and RE, while sinking current I_F from the CE. Simultaneously, a transimpedance amplifier (TIA) with feedback resistor R_F is used to sense I_F which corresponds to the glucose concentration, and convert it to a voltage for readout. There are some drawbacks to this topology for use in a contact lens system. First, as the WE is set via a virtual ground rather than an ac ground, it is sensitive to noise and interference. Second, the inductive input impedance of the transimpedance amplifier can cause stability problems with the control amplifier. Third, the minimum common mode voltage of the transimpedance amplifier subtracts from the limited voltage headroom available for the system.

To address these shortcomings, a current-mirror based topology such as the one implemented in [6] can be used. Figure 2.17 shows the potentiostat schematic used in [6]. The cell voltage V_{cell} is set by the difference between the V_{WE} and the control amplifier replica of V_{RE}. The cell current I_F is measured by a gain-boosted cascode current mirror and replicated as I_{F1}. This mitigates the current mismatch due to channel-length modulation and thus provides an accurate current replica to the current sensing block. I_{F1} can now be fed into any sensor readout circuitry depending on the system architecture. The advantage of this topology is that it decouples the potetiostat operation with from sensor readout. For example, if the currents I_P and I_N had fed into a TIA similar to Figure 2.16, the inductive input impedance would not cause stability issues, as this node is not in the feedback loop. Furthermore, the headroom constrains on TIA input voltage become relaxed.

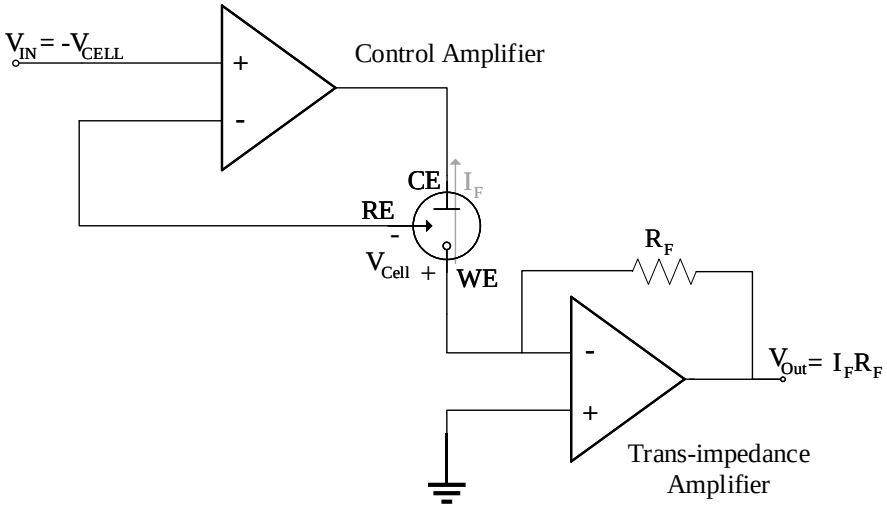


Figure 2.16: Example of a grounded WE topology [10]

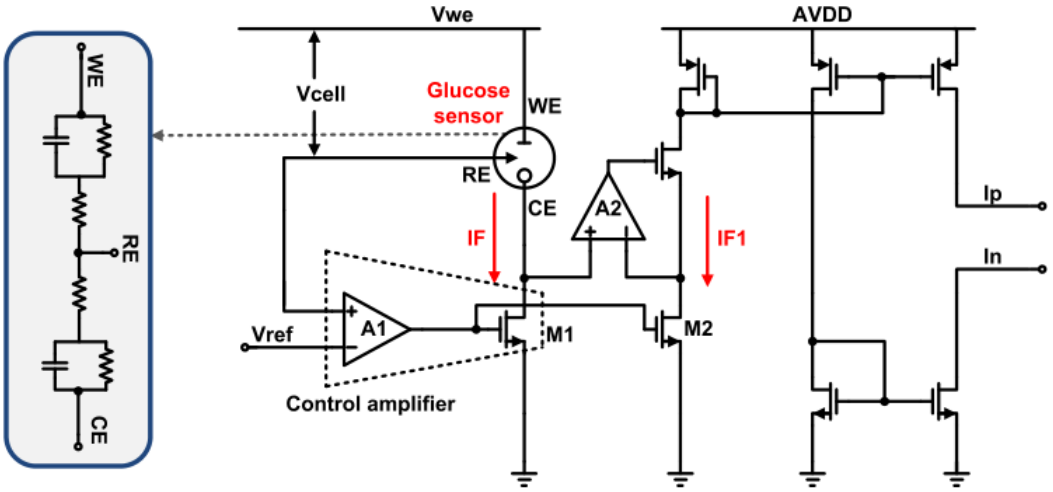


Figure 2.17: Potentiostat used in [6]

There has been an abundance of work on potentiostats for glucose sensing in the literature, a selection of which are summarized in Table 2.1 and Table 2.2. Depending on the

size and concentration of glucose, the current sensing requirements can vary significantly. For instance, work in [19] shows a blood glucose sensor implant that must sense 0 mM - 40 mM of glucose, which given the dimensions of the sensor, results in 1 nA - 1 μA of current. The sensor previously referenced in [2] senses 0.05 mM - 2 mM, which corresponded to 2 nA-80 nA of current.

A standard method used to reduce the power consumption is to reduce the supply voltage. However, this is limited by the reaction potential between WE and RE which is a function of the materials used to build the sensor. Work in [20] requires 0.7 V between WE and RE whereas the sensor in [2] could be at operated 0.4 V.

Many designs will convert current to frequency for use in backscattering RF transmitters such as in [2][19][20][23]. In these designs, since the system processes current directly, a simple current mirror can be used to replicate the glucose current into the current-controlled oscillator. However, another common method is to convert current to voltage using a TIA as in [21][22], which then feeds an analog-to-digital converter (ADC). The digital data is then fed into the RFID subsystem to be transmitted to the receiver.

2.2.3 Review of Sensor Readout

The potentiostat architecture is not complete without describing the current sensing block. In the case of the glucose sensor, the sensor current must be eventually transmitted over the integrated Bluetooth transmitter. This requires that sensor data is digitized into a code word so that it may be included within a Bluetooth packet. As mentioned previously, the sensor is required to measure 1 nA - 100 nA with 0.1 nA resolution, achieving an effective number of bits (ENOB) of 10. The signal-to-noise ratio (SNR) required to be accurate to 10 bits for a sine-wave input signal can be approximated as follows:

$$SNR = 6.02 \times ENOB + 1.76 = 61.76\ [dB] \tag{2.8}$$

Initially, a dual-slope analog-to-digital converter was proposed to digitize the current. However, the analysis of the standard topology showed that the integrating capacitor would need to implemented off chip to achieve 10-bit resolution. Given the contact lens application, this tradeoff was unacceptable. In order to meet this requirement, a 1st-order incremental analog-to-digital converter (IADC) was implemented.

Incremental Analog-to-Digital Converter Architecture and Prior Art

IADCs are periodically-reset delta-sigma modulators, and operate as Nyquist-rate converters rather then oversampling converters. To understand incremental converters, a brief overview of delta-sigma modulators is necessary. A linear model of a first-order delta-sigma ADC is shown in Figure 2.18. It consists of an integrator, a comparator (1-bit ADC), a delay, and finally a 1-bit DAC which feeds a summing node with the input.

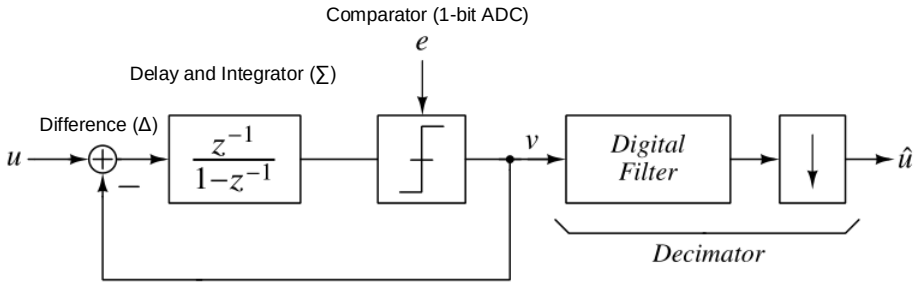


Figure 2.18: 1st order delta-sigma ADC Model [11]

Oversampling converters sample the input signal at a much higher rate than the Nyquist frequency using a less accurate ADC. Oversampling ratio (OSR) describes how much higher the sampling rate F_{CLK} is as compared to the Nyquist sampling rate $2F_{BW}$:

$$OSR = \frac{F_{CLK}}{2F_{BW}} = \frac{\omega_{CLK}}{2\omega_{BW}} \tag{2.9}$$

These converters use memory and feedback of multiple samples to refine the accuracy of the ADC output, thus higher OSR implies more refinement through feedback. In Figure 2.18 the input analog voltage u is applied to the difference junction (Δ) with the comparator output v. This output is then delayed and applied to an ideal integrator (Σ). This output is then digitized by a comparator, where the quantization noise is modeled by e. Analysing the noise transfer function (NTF) of the quantization noise e to the output, it is found that:

$$NTF(z) = 1 - z^{-1}, \tag{2.10}$$

where $z = Ae^{j\phi} = Acos(\phi) + jAsin(\phi)$. This feedback shapes the noise such that it is moved to higher frequencies away from the pass-band of the signal as shown in Figure 2.19, where

ω is frequency normalized to the sampling rate. The graph shows that below 0.4ω, the noise is attenuated, whereas the noise above 0.4ω is boosted. In addition, the noise is attenuated by at least 0.5 below the Nyquist rate $2\omega_{BW} = \frac{\pi}{OSR}$. Finally, a digital low-pass filter is used to filter out the high frequency shaped noise, so that the final spectrum has an improved SNR.

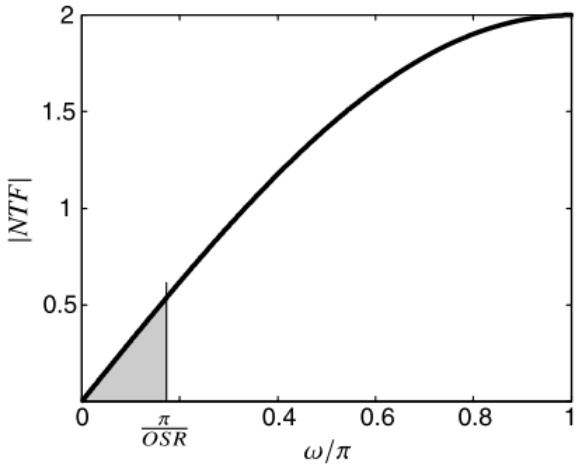


Figure 2.19: Noise Transfer Function for a 1st-order DS-ADC [11].

Compared to the typical delta-sigma architecture, the incremental architecture periodically resets both the digital filter and the integrator, where the digital bit-word is output after every reset. Therefore, there is a distinct sampling rate of the overall ADC which has a one-to-one sample correspondence at the reset signal rate. Therefore, the reset signal rate f_{reset} must be at least:

$$f_{reset} \geq 2BW_{sig} \tag{2.11}$$

where BW_{sig} represents the signal bandwidth. For this application, the signal being sampled is effectively DC (i.e. BW_{sig} is approximately 0), thus it is still possible to achieve a high OSR as f_{reset} can be pushed close to DC while still meeting the Nyquist criterion.

There are a number of advantages of IADCs over traditional sigma-delta ADCs. For example, higher absolute accuracy (20 bits) is easier to achieve as the instability with higher order sigma deltas is avoided. Another advantage is the ease of multiplexing the circuitry between multiple channels of a sensor. However, for this application, there are two main advantages: power savings and improved SNR. The power savings comes from the ability to put the ADC in sleep mode via the reset signal. The improved SNR is

specifically obtained when comparing a first order IADC to a first order delta-sigma ADC. The first order DS-ADC is prone to idle tones or limit cycles when a DC signal is applied, which degrades SNR. However, the IADC fundamentally cannot form limit cycles, which improves the SNR achieved [11].

The system in [6] implemented a 10-bit switched-capacitor-based IADC as shown in Figure 2.20. A differential circuit is used to improve the common mode rejection and suppression of clock feed-through and charge injection. Furthermore, chopping circuitry is added to the input of the IADC to reduce the impact of the 1/f noise on the overall noise performance. The input currents are then integrated by an inverter-based OTA. Following this, a differential comparator is used as a 1-bit ADC, the output of which is then summed using a counter to create the final digitized value D_{out}. The IADC is operated at a 1.2 V supply and achieves a DC power consumption of 3 μW. The IADC is sampled at 214-kHz and achieves an ENOB of 9.3 bits.

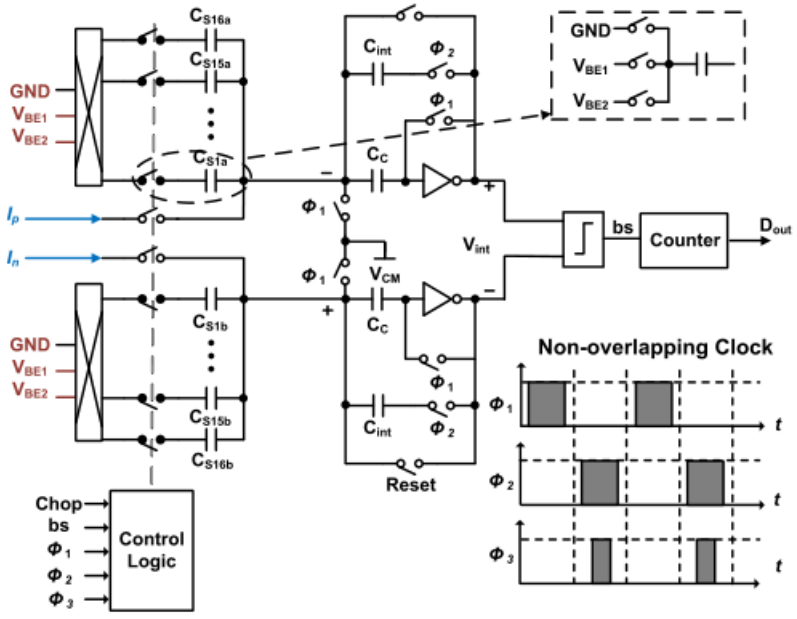


Figure 2.20: IADC used in [6]

Chapter 3

Low-Power Bluetooth Transmitter Design

One of the primary goals of this thesis is to design a Bluetooth™ (BT) transmitter (TX) suitable for a contact-lens energy harvesting glucose sensor. Key specifications derived from the BT protocol and system budget are repeated in Table 3.1 for convenience.

Table 3.1: BLE Transmitter Requirements [1].

Bluetooth Transmitter Requirements		
Specification	Minimum	Maximum
RF Output Power (Pout)	-20 dBm	+4 dBm
Channel Frequency Range	2402 MHz	2480 MHz
Modulation Frequency Range	-250 kHz	+250 kHz
Adjacent Spur @ 2MHz offset	-	-20 dBm
Adjacent Spur @ 3MHz offset	-	-30 dBm
Maximum Frequency drift	-	± 50 kHz
Bluetooth TX Power Budget	-	**250 μW**

As shown in Figure 3.1, the chosen architecture for the GFSK modulator is an in-loop, Integer-N PLL modulated at both the reference and the VCO (two-point modulation), followed by a power amplifier. Thus, the crux of the design focuses on the implementation of the PLL and PA such that they meet the specifications in Table 3.1.

The power budget for the system is 250 μW. The design evolved by implementing each

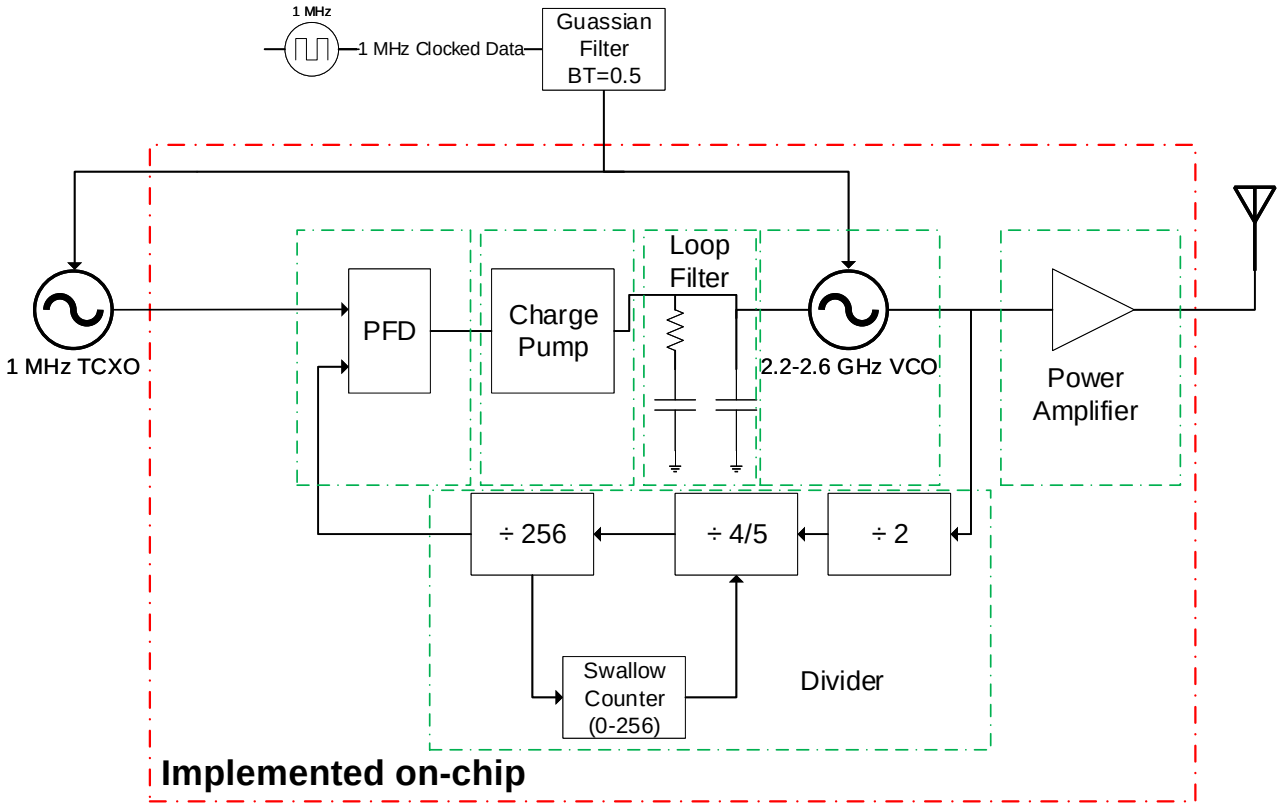


Figure 3.1: GMSK modulator system diagram.

sub-block with as low a power consumption as possible, and making adjustments to these estimates as necessary.

To achieve the power requirements, the entire modulator is designed assuming a supply voltage of 0.5 V, which is one half the nominal supply of 1 V for the technology. The remainder of the chapter details the design and simulation results of the Bluetooth transmitter implemented.

3.1 PLL Design

3.1.1 Voltage-Controlled Oscillator (VCO)

To design the VCO, circuit level requirements must be derived from the top-level specifications. The channel selection requires that the VCO must be tunable between 2.4 GHz – 2.48 GHz to oscillate at the advertising channels f_{ch} (2402/2426/2480 MHz). Given that the charge pump driving the VCO can only change at most by 0 V – 0.5 V, and that it must ideally be linear within the frequency range of the VCO, the gain of the VCO (K_{VCO}) was set by:

$$K_{VCO} = 200 \text{ MHz}/0.5 \text{ V} = 400 \text{ MHz/V}. \tag{3.1}$$

This ensures the required range for BT of 80 MHz can be met between 0.2 V and 0.4 V. Another key specification is the phase noise required by the VCO. This specification is derived by reviewing various specifications in the Bluetooth standard. Bluetooth specifies a bit-error-rate (BER) of 10^{-3} for advertising-packet only mode. A GMSK signal requires and SNR of 11 dB to meet this BER [29]. Assuming 15 dB is required, it can be shown that:

$$\begin{aligned} \frac{1}{SNR} &> 2\int_{f_{ch}}^{f_{ch}+500kHz} L(\Delta f)d\Delta, \\ L_{in-chan} &< \frac{1}{SNR \times BW} = -75 \text{ dBc/Hz}. \end{aligned} \tag{3.2}$$

where $L(\Delta f)$ represents phase noise as a function of offset frequency from the carrier and $L_{in-chan}$ represents the phase noise up to the channel bandwidth.

This derivation is largely unhelpful in setting the phase noise, however, since the in-band phase noise will be set by the reference oscillator as the PLL tracks the phase noise of the reference input up to the loop bandwidth. However, one can use carrier-to-interference ratios specified in the Bluetooth receiver requirements to derive a pessimistic value for phase noise as $L_{1.5MHz} < -92 \frac{dBc}{Hz}$ and $L_{2.5MHz} < -102 \frac{dBc}{Hz}$ [29].

Another specification is the tuning range associated with the data path. GMSK signaling dictates that:

$$\Delta f_{out} = BitRate/2, \tag{3.3}$$

where Δf_{out} represents the the frequency difference between a '1' and '0' at the output and $BitRate$ represents the input data rate. The BT bit rate is 1 Mbps, which requires $K_{VCOmod} > 1$ MHz/V. To give some margin to this value, K_{VCOmod} was set to 1.2 MHz/V.

Finally, the most important specification is the power consumption. In this topology, the VCO is the largest power consumer of the entire chip. Therefore, a budget of 160 μW was allocated to the VCO knowing that the RF inductor performance will dictate what is actually achievable. Table 3.2 summarizes the performance requirements of the VCO.

Table 3.2: VCO Specifications

Design Specification	Target
K_{VCO}	400 MHz/V
Phase Noise @ 1.5 MHz	-92 dBc/Hz
Phase Noise @ 2.5 MHz	-102 dBc/Hz
K_{VCOmod}	1.2 MHz/V
VCO Power Consumption	**160 μW**

The VCO schematic from Figure 2.10 is shown again in Figure 3.2 for convenience. This omits a tail-current source typically used in similar VCOs. A tail-current source would force a known bias-current into the oscillator which would improve the power consumption variation across corners. Furthermore, it would improve the common-mode rejection of the oscillator. However, to keep the current source in its linear region of operation, the output-swing would be limited, which ultimately degrades phase-noise due to reduced signal swing. Thus, the pseudo-differential CMOS based architecture was chosen.

The design process starts with the inductor design, as it will dictate how much g_m is needed to oscillate, which in turn will set the sizes of the cross-coupled pairs and, indirectly, the power consumption of the VCO. The goal is to design an inductor in a given area which maximizes the equivalent parallel impedance R_p, which is calculated as:

$$R_p = Q \times 2\pi f_{osc} \times L. \tag{3.4}$$

where Q is the quality factor of the inductor, f_{osc} is the oscillation frequency, and L is the inductance.

To reduce design risk, the inductor layout was chosen using the design kit inductor sizing tool provided. However, the inductor layout generated by the kit did not maximize R_p in a given area as compared to implementing a custom inductor layout. Nevertheless,

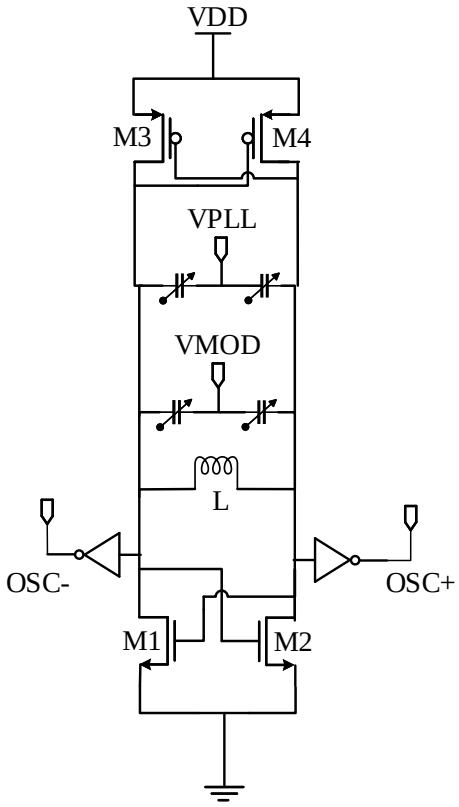


Figure 3.2: CMOS LC VCO implemented without PVT capacitor DAC.

kit inductors were preferred due to the model correlation to physical measurements. To obtain a high-Q at 2.4 GHz, relatively large inductor sizes are needed to increase the overall inductance and decrease the peak-Q frequency. Thus, the inductor used was a symmetric octagonal spiral inductor with 6 turns, an outer-dimension (OD) of 300 μm, conductor spacing (S) of 3 μm and wire width (W) of 8 μm. Table 3.3 summarizes the relevant performance metrics of the inductor chosen.

Table 3.3: Inductor Performance Summary

Specification	Simulated Result
Inductance L	10.08nH
Q @ 2.44GHz	22.5
R_p @ 2.44 GHz	3.52kΩ
Self-Resonant Frequency (SRF)	4.4 GHz

Although the absolute minimal loop gain required to oscillate is 1 V/V, the VCO is designed for a higher loop gain of 10 V/V so that the oscillator will reliably start up as well as enter the voltage limited regime in large-signal operation, maximizing swing to 0 to V_{dd} and thus improving phase noise. Obtaining rail-to-rail operation is important as it allows the use of open-loop inverters as drivers off chip, which reduces the buffer power consumption. However, too high a loop gain implies that there is unnecessary power being consumed by the oscillator. The loop gain target implies that

$$(g_{mn} + g_{mp}) = 10/Rp_{diff}, = 1.42 \text{ mA/V}. \tag{3.5}$$

The cross-coupled (CC) pairs were sized using minimum length transistors to obtain the maximum g_m/I_d and reduce the overall bias current. The sizing of the CC pairs and simulation results are summarized in Table 3.4 below. The median loop-gain achieved is 22 V/V, which, despite being higher than 10 V/V, allows for loop gain margin in oscillation frequency across Monte Carlo variation.

Table 3.4: Cross-coupling size and performance summary

Specification	Value
NMOS-pair W/L	12 μm/40 nm
PMOS-pair W/L	24 μmm/40 nm
Loop Gain	21 V/V (1.2 V/V - 500 V/V)
Power Consumption	50 μW +/- 30 μW 3σ variation

To obtain K_{VCO} = 400 MHz/V, a pair of MOS accumulator region varactors are implemented. Given 200 MHz of frequency tuning from 0 V - 0.5 V centered at 2.45 GHz, the change in capacitance required by the varactor (ΔC_{var}) using the differential inductance (L_{diff}) and the minimum and maximum frequency (ω_1 and ω_2 respectively) can be

calculated as

$$\Delta C_{var} = \frac{1}{L_{diff} * {\omega_1}^2} - \frac{1}{L_{diff} * \omega_2^2} \tag{3.6}$$
$$\Delta C_{var} = 70 \text{ fF}.$$

where $L_{diff} = 10$ nH, $\omega_1 = 2\pi(2.35 \text{ GHz})$ and $\omega_2 = 2\pi(2.55 \text{ GHz})$.

To size the varactor, an initial CV curve is obtained which is shown in Figure 3.3 which shows 130 fF (single-ended) tuning range. However, the size is tuned after observing the frequency vs. voltage tuning curve.

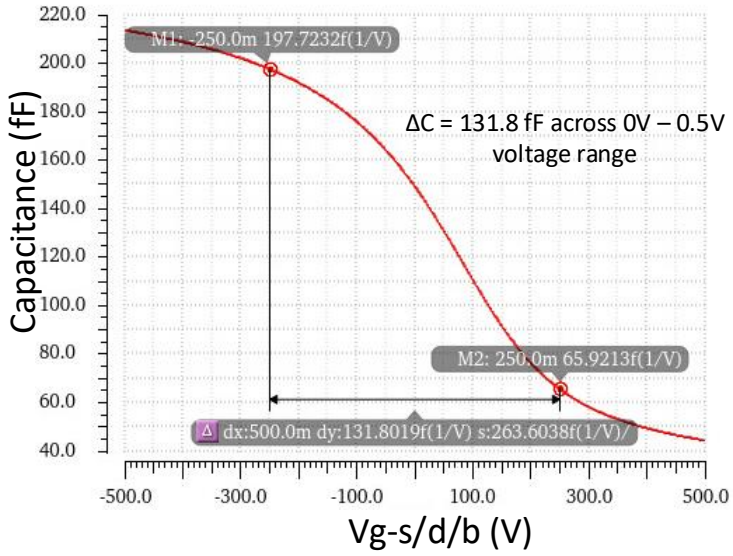


Figure 3.3: Accumulation mode varactor CV tuning curve.

Another tuning node is necessary to implement the GMSK modulation. Specifically, the tuning node V_{mod} must tune the frequency by +/- 250 kHz. This would require $\Delta C_{varmod} =$ 0.175 fF, which cannot be achieved with a minimum size varactor. Therefore, nineteen 0.6 fF capacitors were added in series with the varactor to reduce the change in capacitance.

To account for process variation, a binary-weighted 3-bit varactor DAC was added to the oscillator. Any remaining capacitance necessary to obtain 2.4 GHz resonance was added as fixed capacitance. The value of the fixed capacitance was reduced to accommodate additional layout parasitics following a parasitic extraction. Figure 3.4 shows the complete circuit diagram.

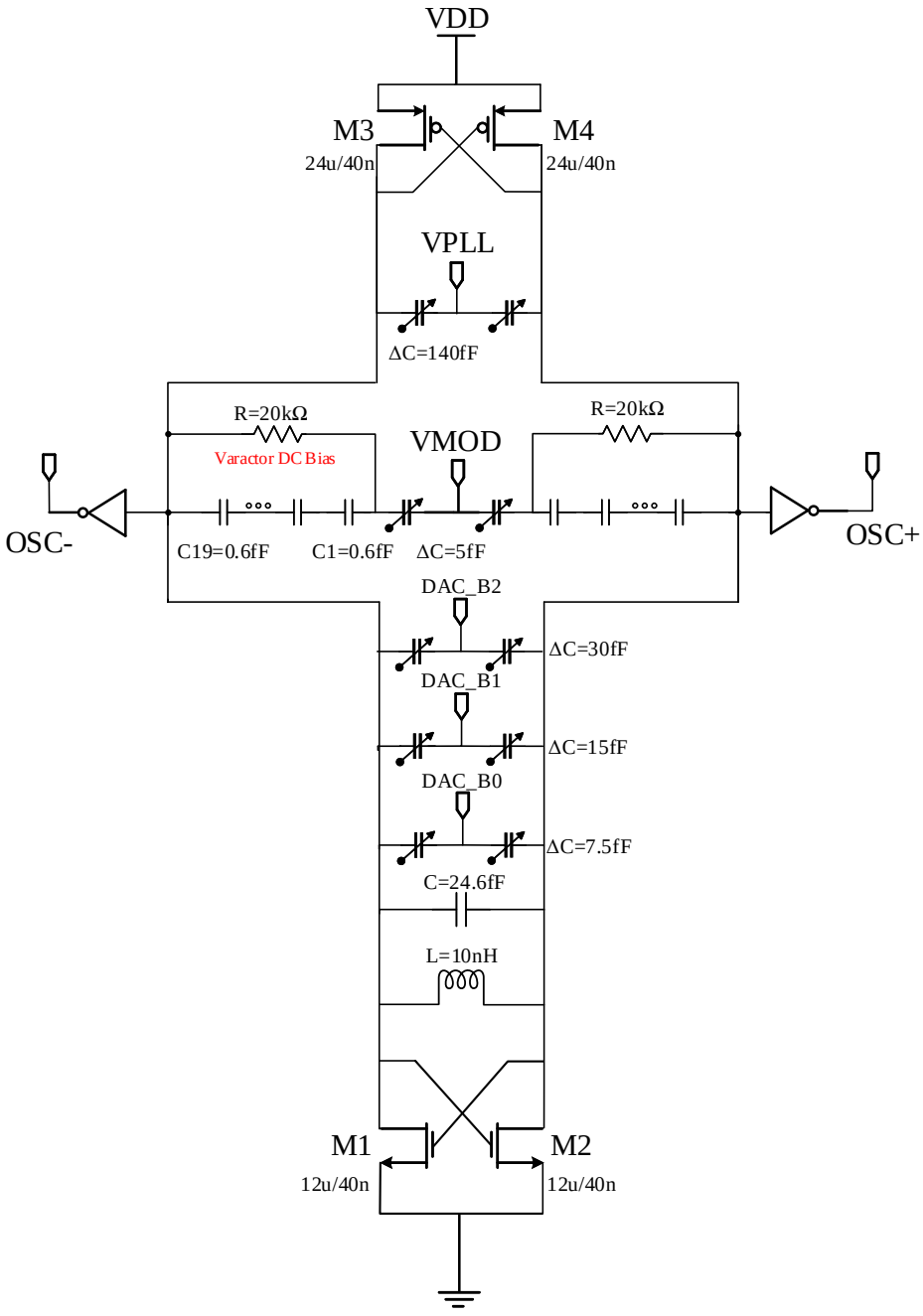


Figure 3.4: Annotated VCO schematic.

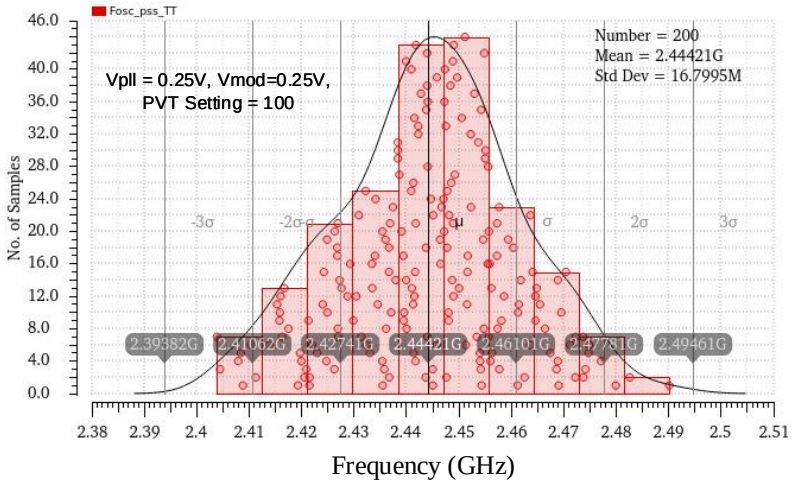


Figure 3.5: Monte Carlo simulation of oscillation frequency (200 trials).

The performance of the VCO was simulated to check that the design criteria was met. Figure 3.5 shows the oscillation frequency variation across Monte Carlo sampling. The centre frequency is set to 2.444 GHz with a standard deviation of 16.8 MHz accounting only for transistor variation. Thus, to ensure that the oscillator can be brought to the correct range, the tuning range of the oscillator must be able to tolerate at least 3 σ in each direction (50 MHz) in addition to the required 2402 MHz – 2480 MHz. However, the variation capacitance and inductance in the LC tank from simulated parameters will likely have a greater impact on resonant frequency. Unfortunately the Monte Carlo variation of these parameters could not be simulated.

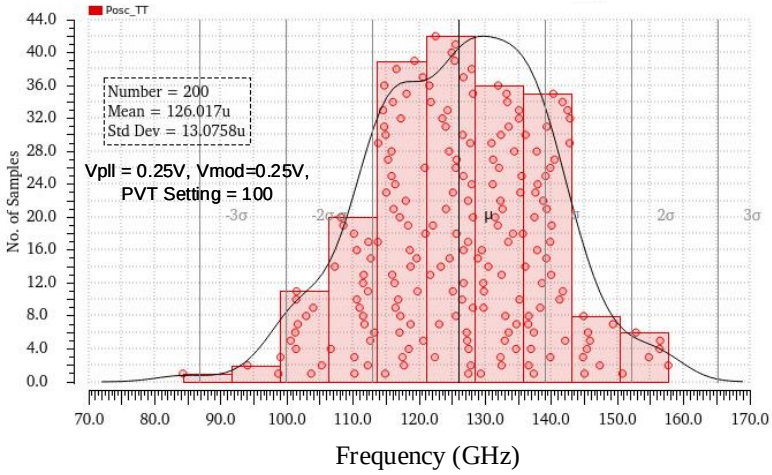


Figure 3.6: Montecarlo simulation of oscillator power consumption (200 trials).

Figure 3.6 from the Monte Carlo simulation shows the average power consumption of the oscillator as 126 μW, with a σ of 13 μW. This meets the 160 μW target within $\pm 2\sigma$. However, given that the loop gain simulated was 22 V/V, this implies that the oscillation transistors could be reduced in size obtain further power savings. That optimization was not implemented in this thesis.

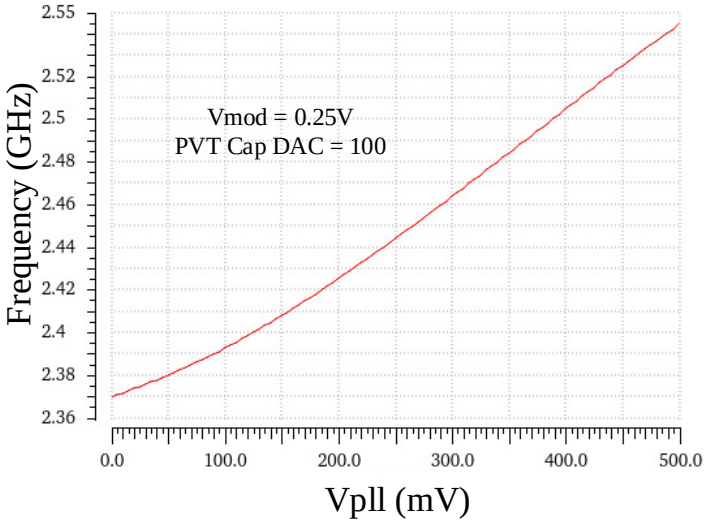


Figure 3.7: Oscillation frequency across tuning range

Figure 3.7 verifies the tuning range of the oscillator, showing that the required frequency range can be obtained from 0.1 V to 0.4 V. This is important as the voltage range of the charge-pump which drives the input to the VCO can only operate over this range.

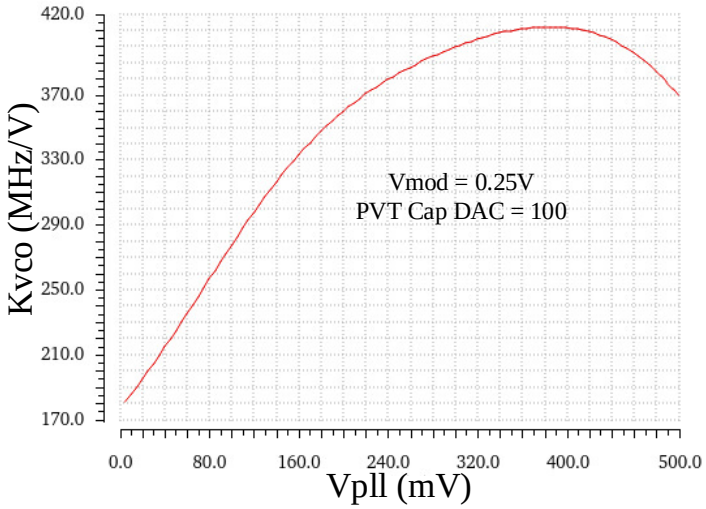


Figure 3.8: Oscillation frequency gain (Kvco) across tuning range.

Furthermore, Figure 3.8 shows that the K_{VCO} of the oscillator is slightly lower than the target gain of 400 MHz/V. The curve also shows that the gain of the oscillator is changing significantly across the tuning range. The impact of this is hard to predict without modelling this curve in an overall PLL system level simulation. The non-uniform gain stems from the varactor tuning curve non-linearity as the capacitance changes between depletion to accumulation mode.

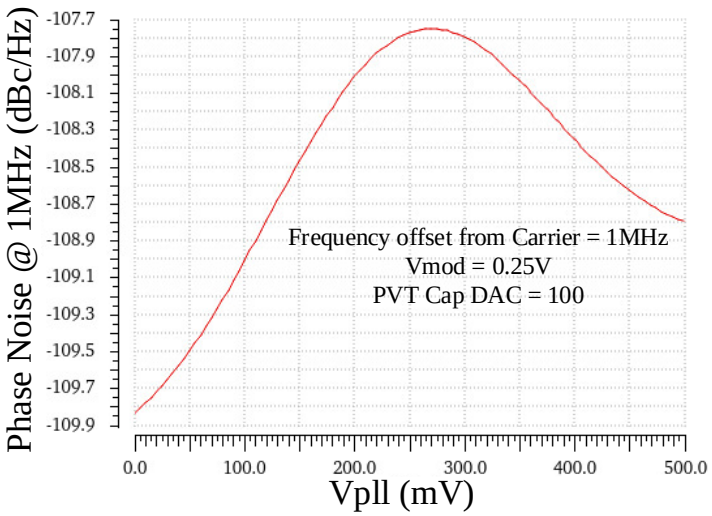


Figure 3.9: Phase Noise @ 1MHz across tuning range

The phase noise at 1 MHz offset, shown in Figure 3.9, is -107.7 dBc/Hz in the worst case. This guarantees that the oscillator meets the required -92 dBc/Hz at 1.5 MHz offset. Since the phase-noise comfortably meets the specification, further optimizations were not pursued.

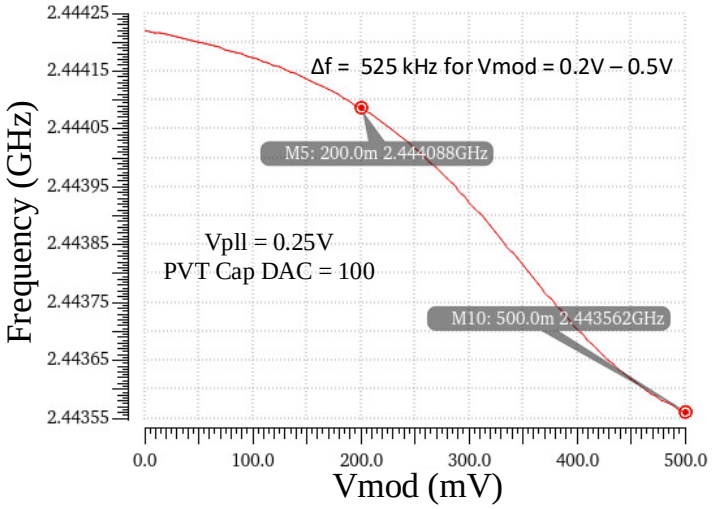


Figure 3.10: Oscillation frequency across modulation voltage.

Figure 3.10 shows that the modulation path obtains +/- 500 kHz tuning range from 0.2 V to 0.5 V. This range is non-ideal, as it requires a level shifter between the digital data output DAC to the input node to ensure correct operation.

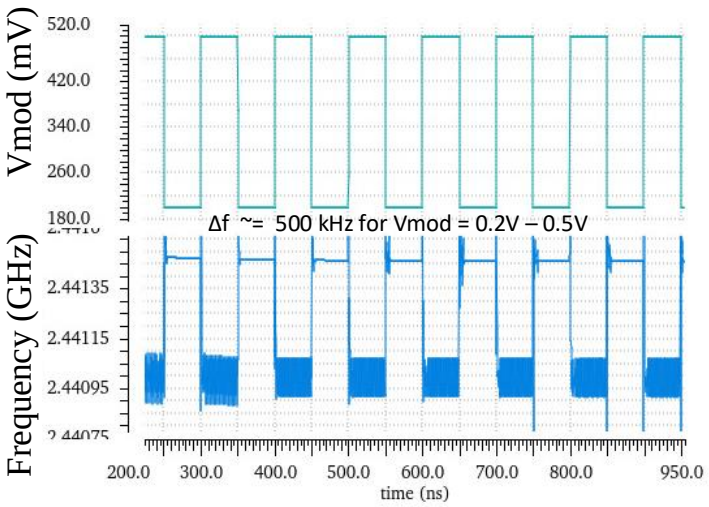


Figure 3.11: FSK modulation waveform applied to V_{mod}.

To show the transient performance, a 10 MHz signal is applied to V_{mod} (instead of the expected 500 kHz data stream) in Figure 3.11 to ensure that the oscillator frequency switches quickly.

Finally, a figure of merit (FOM) for the oscillator can be calculated as

$$FoM_{osc}[dB] = -L(F_{offset})[\frac{dBc}{Hz}] + 20log_{10}(\frac{F_{osc}}{F_{offset}})[dB] - 10log_{10}(\frac{P_{osc}}{1mW})[dB]. \quad (3.7)$$

Figure 3.12 shows the oscillation FOM as 184.6 dB, which is approximately 6 dB poorer than the state-of-the-art FOM in literature [30]. A major reason for this is that the output swing is limited to a range between 0 V to V_{DD} rather than 0 V to $2V_{DD}$, achievable with a signal CC-pair and resonant tank. Thus, the CMOS schematic phase-noise suffers as a result, reducing the overall FOM. State-of-the-art LC VCOs focus on reducing phase-noise to improve FOM by using transformers instead of inductors in the VCO to shape the harmonics of the oscillator to reduce phase-noise. This design does not use these structures since the phase-noise requirement has been comfortably met.

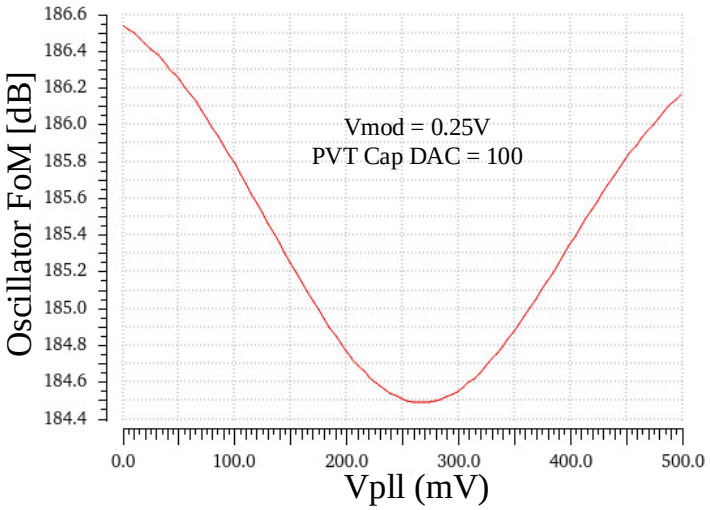


Figure 3.12: Oscillator Figure of Merit across tuning range.

3.1.2 Frequency Divider

The modulator must be able to be select 2402/2426/2480 MHz output frequencies. The PLL will lock the divided VCO frequency to the reference frequency. The divider requirements stem from two specifications: achieving channel selection and low power consumption. The power consumption allocated to this block is 30 μW. The divider implements the equation below:

$$F_{DIV} = \frac{F_{OSC}}{N}, \text{ where } N = 2(5S + 4(256 - S)) = 2(1024 + S) \tag{3.8}$$

where S represents a digital code that selects the PLL channel and can range from 0 to 255. Setting S to 177/189/216 selects the three respective advertising channels. Figure 3.13 shows the divider implementation. The initial divide-by-2 is implemented using a flip-flop. This was done to reduce the power consumption, as it limits how much energy is dissipated by charging and discharging capacitance at 2.4 GHz. Following this, the frequency is further sub-divided by a synchronous divide-by-4 or divide-by-5, dual-modulus divider as shown in Figure 3.14. The clock is first divided by 5, until S cycles have passed.

The divide ratio then changes to divide-by-4 for $256 - S$ cycles. This feeds a divide-by-256 divider implemented as a synchronous binary counter. Originally, this block was implemented as an asynchronous ripple-counter to reduce power consumption. However, two problems with this implementation are (1) the process-dependent delay of the divider which degrades loop stability as the delay manifests as a right-half plan zero [7], and (2) the effect of charge leakage of the dynmaic flip-flops internal nodes in the final divide stages. Since the later stages outputs are slower clocks, these flops cannot be implemented with dynamic logic, which increases power consumption. The swallow counter is combinational logic that compares the output of P with the channel setting (S as in eqn. 3.8) of either 177, 189 , or 216. It sets an RS-latch, which is set once $P = S$ and is reset when P reaches 255. Once set, the dual-modulus divider switches from 5 to 4. Finally, the divide chain output is re-timed to align to the VCO frequency with a final re-timing flip-flop in order to suppress phase noise associated with the divider [7].

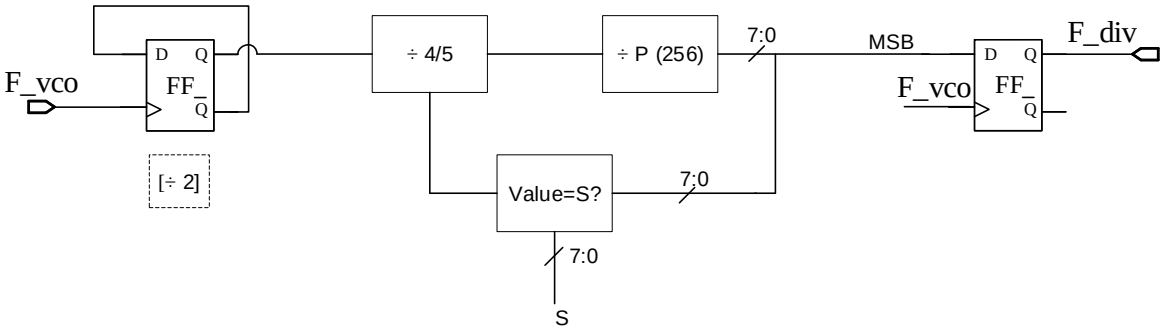


Figure 3.13: PLL Divider chain

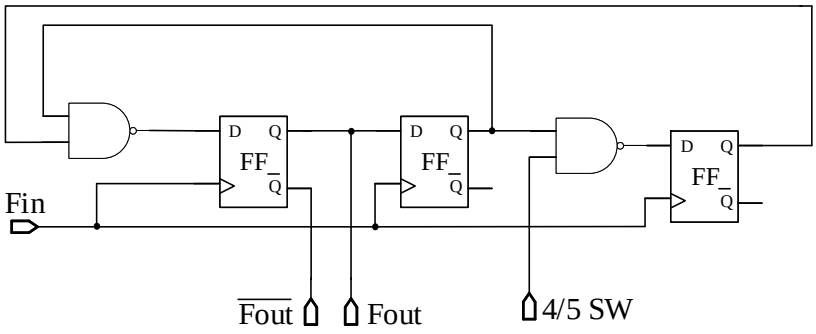


Figure 3.14: Dual-modulus divider block diagram.

The flip-flops were implemented with C^2MOS logic [31]. Figure 3.15 shows the D-flip-flop schematic, where setup time t_{setup} is 25 ps, hold time t_{hold} is 130 ps, and propagation delay t_{clktoQ} is 160 ps. Thus, the flip-flop can operate at the required speed at every stage of the divider.

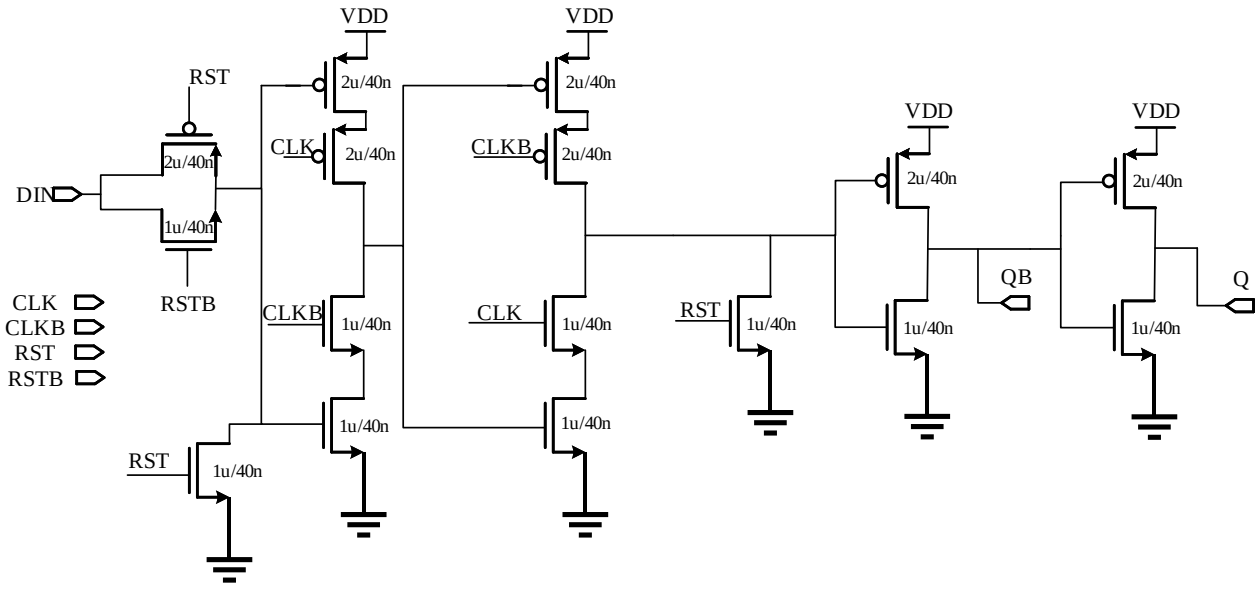


Figure 3.15: Dynamic C^2MOS D-flip-flop implementation.

The power consumption of each sub-component in the divider is summarized in Table 3.5. The overall power consumption of the divider is close to the target specification. Most of the power is consumed by the first two stages of the divider.

Table 3.5: Divider simulated power consumption.

Sub-block	Simulated Result
Divide by 2	11 μW
Dual-Modulus Divider	11 μW
Divide by 256	7.5 μW
Swallow Counter	3 μW
Total	**32.5 μW**

3.1.3 Phase/Frequency Detector and Charge Pump

Figure 3.16 shows the implemented PFD, which is a conventional flip-flop based design.

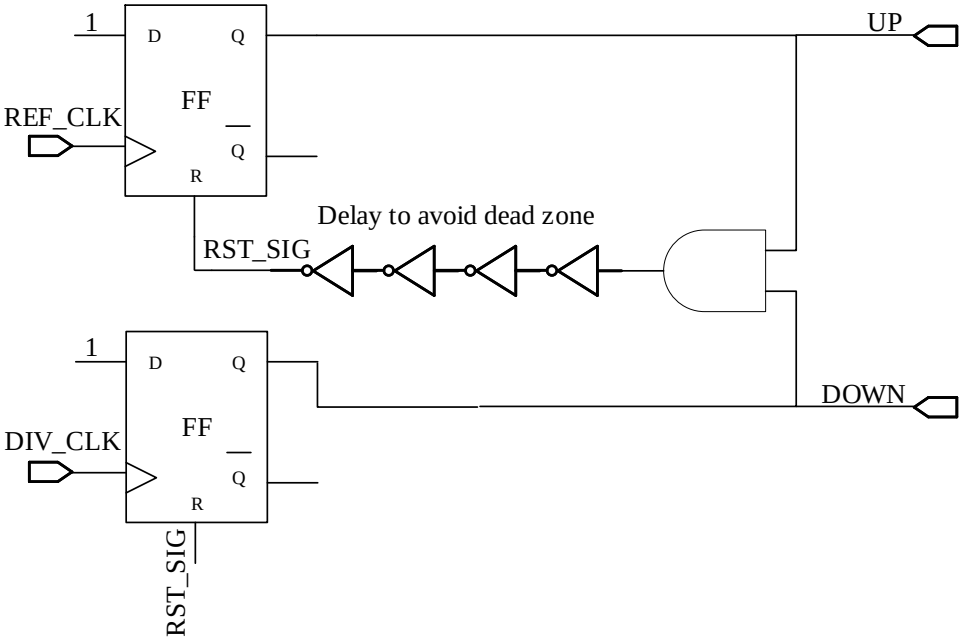


Figure 3.16: Phase-frequency detector implementation.

The flip-flops are implemented in static CMOS, due to the low speed requirements. To understand the circuit, consider the scenario where the reference clock is currently at a higher frequency than the divided clock as in Figure 3.17 a). In this case, if the reference clock rising edge arrives first, the UP signal is set high until the divider clock edge arrives, at which point it goes down again. However, if the frequencies are still far apart, it is likely that the reference clock edge will arrive first again, which will continue to assert UP until a divided clock rising edge arrives. This UP signal is feeds into an integrator which then drives the VCO, raising the divided clock frequency to try to speed up the divided clock edge. This is the essential operation of the frequency detector, reducing the error between the reference and divided clocks through negative feedback in the PLL. Once frequency locked, the UP or DOWN pulse will be at the reference clock frequency, where its duty cycle (average value) corresponds to the phase difference as shown in Figure 3.17 b). This is also corrected by the negative feedback of the PLL. Once locked, UP and DOWN ideally should remain at zero, but due finite propagation delays, is often a finite pulse width.

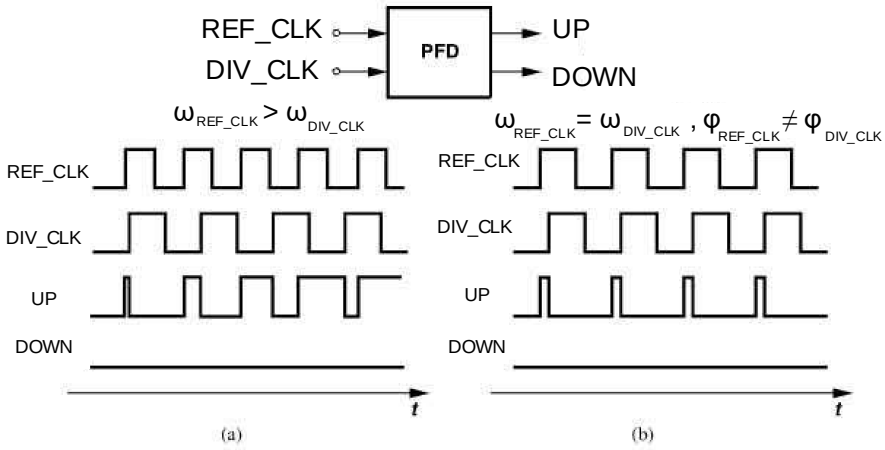


Figure 3.17: Response of a PFD to inputs with unequal (a) frequencies, or (b) phases [7].

Given that the PFD is driven by circuits at or around the reference clock frequency, its power consumption is negligible. However, there are two key performance concerns: dead-zone avoidance and reference spur generated by the circuit. Dead-zone in a PFD refers to the inability to respond to small phase errors (ex. 20 ps phase difference) which stems from the pulse width becoming too narrow to turn on switches in the following

charge-pump. A solution to this issue is to add delay to the reset path, to ensure that the PFD is on for a minimum time period, which was added to Figure 3.16. However, this increases the amplitude of spurious outputs from the PLL at carrier offsets equal to the F_{ref} and harmonics of F_{ref}.

Reference spur refers to spectral content at the output of the VCO which is at the frequency F_{osc} +/- F_{ref}. The inserted reset delay will cause a pulse to appear on both the UP and DOWN signal at F_{ref}, which propagate to VCO input, which modulates the VCO at F_{ref}, generating spurious outputs. This is simulated in Figure 3.18. These glitches can be attenuated and controlled using the loop filter which will be discussed. Furthermore, the added delay can introduce cycle slipping, where the PLL can miss edge transition at its inputs due to the finite reset delay causing the output to already be high, which can lead to limit cycles in the PLL.

An alternative solution to the dead-zone problem that avoids these pitfalls is to add a fixed current offset downstream, such that the PLL steady state lock region is not centred at 0° phase, thus avoiding the dead-zone without requiring elongated minimum UP/DOWN pulses. This solution was not implemented, but should be explored in future iterations.

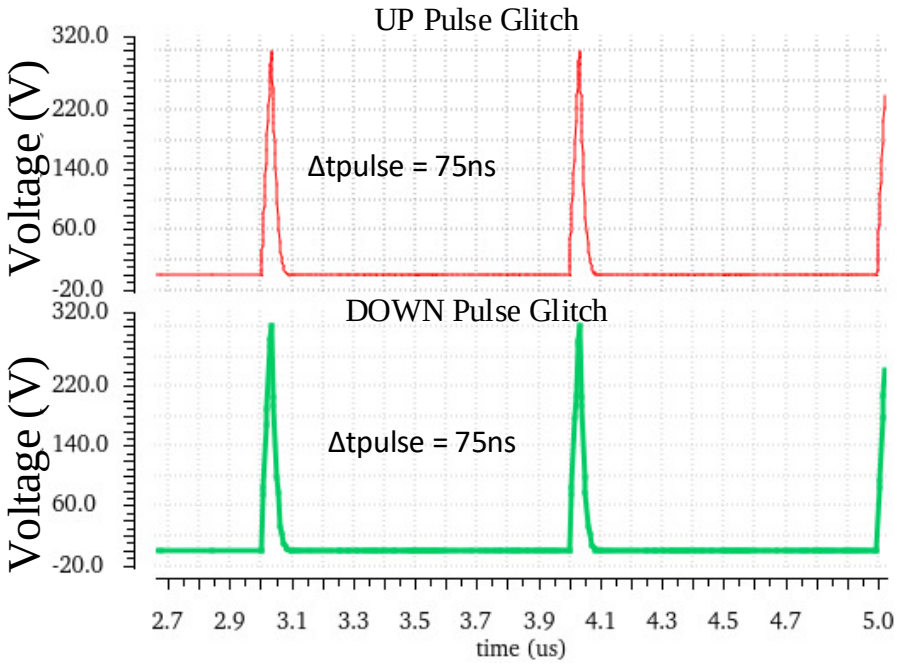


Figure 3.18: PFD UP and DOWN pulse glitch when locked.

The UP/DOWN pulses feed into a charge pump circuit to generate the VCO control voltage. The design must consume less than 20 μW. The effective output range of the charge pump is set by V_{dsat} of the UP/DOWN current sources. With 0.5 V supply range and subthreshold operation, 0.1 V - 0.4 V is the target output voltage range. After system-level analysis (to be shown in the following section), a drive current of 10 μA was chosen.

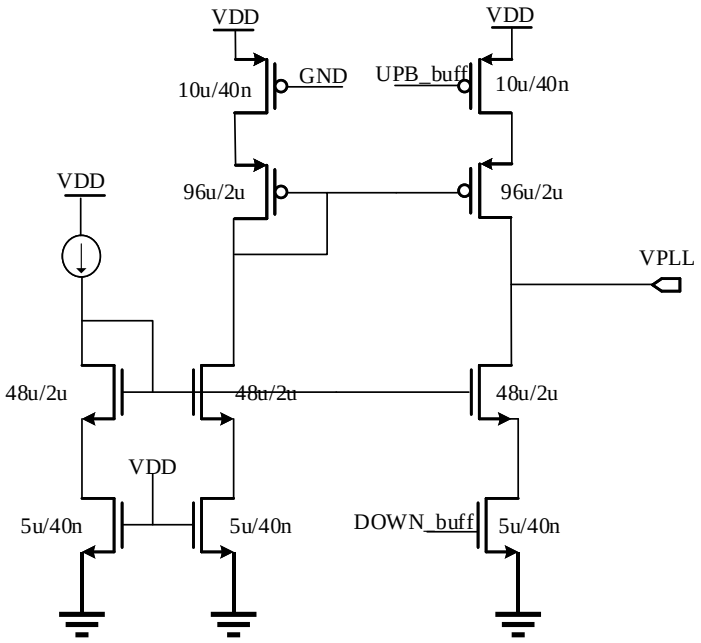


Figure 3.19: Charge pump circuit

The implementation is shown in Figure 3.19. This topology was chosen for low power consumption and simplicity. Larger width and longer length transistors are used to reduce transistor mismatch and reduce channel length modulation. The charge pump output characteristics are simulated in Figure 3.20, where it is clear that there is significant mismatch between the UP/DOWN currents at higher V_{PLL} voltages. The effect of this is explored in a later section. The power consumption of the charge pump is simulated at 15 μW.

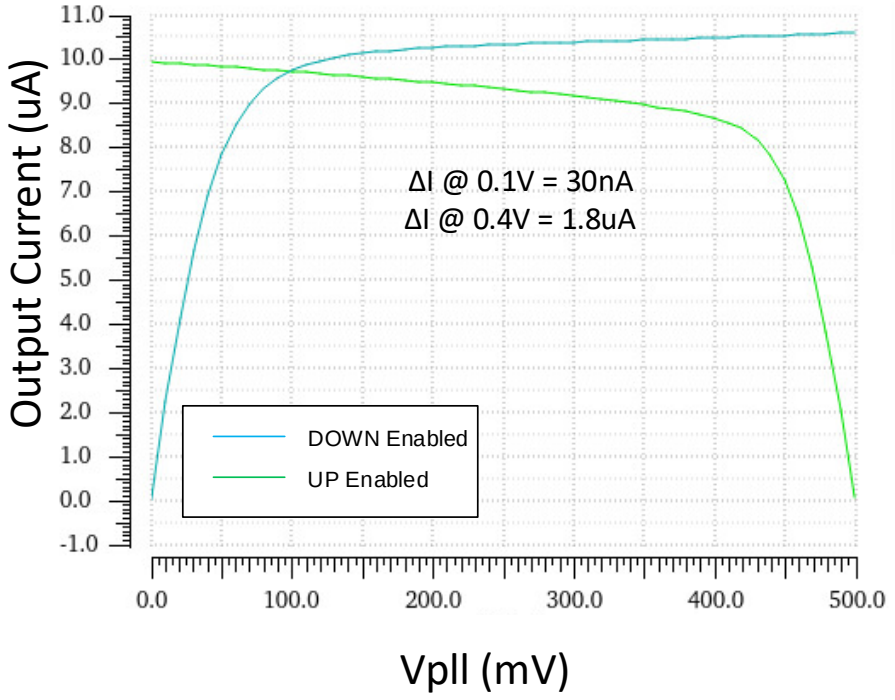


Figure 3.20: Charge pump output current vs. tuning voltage.

3.1.4 Loop Filter Parameters

The loop filter topology is shown in Figure 3.21. The loop-filter parameters are chosen to ensure the stability of the PLL. Stability is analyzed assuming a linear, phase-domain approximation of the system. The VCO and PFD+CP act as two integrators, which alone would be unstable. Thus, R_1 and C_1 in the loop-filter add a zero to the transfer function which ensures stability in the closed-loop system. However, due to the nonidealities in the PFD and CP mentioned previously, a reference spur will appear at the VCO output. Thus, another capacitor is added in parallel (C_2) to reduce the magnitude of the spur. However, this capacitance degrades stability by adding another pole to the open-loop transfer function. Also, given the contact-lens application, the filter must be small enough to be implemented on-chip.

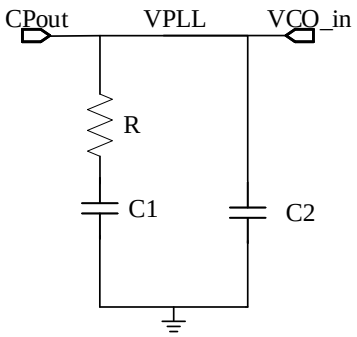


Figure 3.21: Loop Filter

The following equations were used to to calculate the relevant loop filter values:

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi M}}, \tag{3.9}$$

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi M}}, \tag{3.10}$$

$$C_2 = 0.2C_1, \tag{3.11}$$

where I_p represents the charge pump current, M represents the division ratio, ζ represents the system damping factor, w_n represents the natural frequency of the second order transfer function and ω_{in} represents the reference frequency. Given $I_p = 10\ \mu\text{A}, M = 2440, K_{VCO} = 400$ MHz/V, $\zeta = 1$, and $2.5\omega_n = 0.1\omega_{in}$ and additional tuning through simulations, $R_1 = 301.6\ \text{k}\Omega$, $C_1 = 26.4$ pF, and $C_2 = 6.09$ pF. These values are small enough to be implemented on-chip as required for the wireless glucose sensor application.

3.2 Power Amplifier (PA) Design

The PA is typically the greatest power consumer of a Bluetooth transmitter, as most systems are designed to deliver 0 dBm (1 mW) to the antenna. However, given that the receiver is physically close to the TX to provide the RF energy to harvest, the PA only needs to output minimal power to be Bluetooth compliant (i.e., -20 dBm (10 μW)). The DC power consumption allocated to the PA is 30 μW, which implies a drain efficiency target (η) of 33%. The PA was designed to match to a 50 Ω impedance since the test

equipment used to probe the output will also have a 50 Ω impedance. This usually does not impede the design of the PA since most antennas are designed to present a 50 Ω impedance. However, due to the limited space available for the antenna on the contact lens, the antenna in this system is electrically small. This implies that the loop antenna impedance will appear mainly inductive rather than resistive.

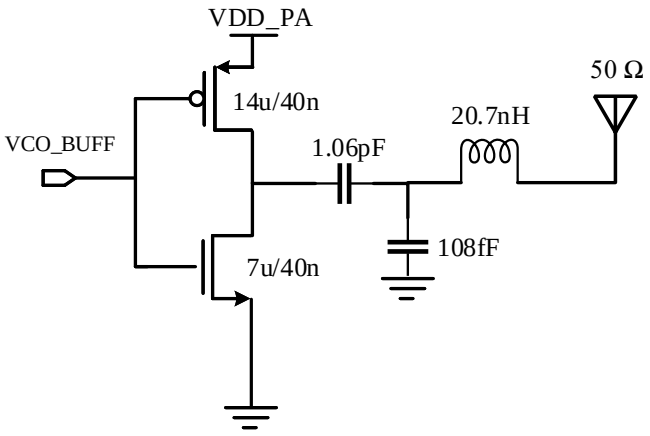


Figure 3.22: PA implemented for the GMSK modulator.

The implemented PA, which uses a Class-D topology, is shown in Figure 3.22. The Class-D topology is essentially an inverter driving a matched load. In the technology used, the propagation delay of the inverter is much less than the operating frequency of 2.4 GHz. Thus the inverter transistors are treated as switches for the remainder of this discussion.

To begin the design process, one needs to understand how power will be delivered to the load, and where power is consumed in the circuit. The circuit is AC coupled so that the antenna is not drawing DC current. On the input side, the oscillator output VCO_BUFF is driving a capacitive load, which consumes power proportional to the input capacitance as set by:

$$P_{input} = C_{in} V_{DDPA}^2 f_{osc}. \tag{3.12}$$

This implies the switch cannot be sized up without increasing the DC power consumption of the stage driving the PA. When driven low, the output voltage is set by the voltage divider formed by the switch resistance R_{SW} and the load resistance R_L. When driven high,

the output voltage is pulled to ground by the switch. The maximum power transfer theorem tells us that the output power transferred is maximized by matching the PA output impedance to the complex conjugate of the load impedance. However, maximum power efficiency is achieved if the switch impedance is much smaller than the load impedance. This leads to two key design trade-offs: (1) increasing the switch size increases the output power efficiency at the cost of power consumption from the stage driving the switch as already discussed, and (2) increasing the load impedance increases the efficiency and reduces the output power. One can find the output power P_{out} and the efficiency η as:

$$P_{out} = \frac{(Vo_{rms}\frac{R_L}{R_L+R_{sw}})^2}{R_L} \tag{3.13}$$

$$P_{DC} = C_{in}Vi_{rms}^2 f + \frac{Vo_{rms}^2}{R_{sw}+R_L} \tag{3.14}$$

$$\eta = \frac{P_{out}}{P_{DC}} \tag{3.15}$$

Given that a 1 μm width minimum-size transistor at 0.5 V input drive has a switch resistance of approximately 1 kΩ, it is clear that the load impedance needs to be raised to improve the overall efficiency. This is achieved with a matching network to raise the impedance of the antenna at 2.4 GHz. Given that the output is relatively narrowband signal (1 MHz), this matching network will not distort the signal given that the Q-factor of the inductor Q_{ind} designed would need to be:

$$Q_{ind} = Q_{filter} = \frac{\omega_{osc}}{BW} = \frac{2.4 \text{ GHz}}{1 \text{ MHz}} = 2400. \tag{3.16}$$

The inductor adds loss and thus decreases efficiency of the PA. Therefore, an inductor which has much higher Q than provided by the CMOS technology design kit was designed [1]. The inductor layout is shown in Figure 3.23. It is a six-turn inductor with 3.5 μm width and 5 μm spacing. It achieves an inductance of 20.7 nH, and Q-factor at 2.4 GHz of 39. Using this inductor, a matching network was constructed which increased the load impedance from 50 Ω to 2800 Ω. With this matching network in place, simulations were done by varying the width of the transistor to achieve the optimal efficiency given the low output power requirements. The simulation results of the design are summarized in Table 3.6. The output power (simulated) is -18.3 dBm, which meets the target requirements. The overall power consumption is higher than initially targeted, however, the efficiency exceeds

[1] Hassan Shakoor designed the matching inductor and helped with sizing the transistor switches.

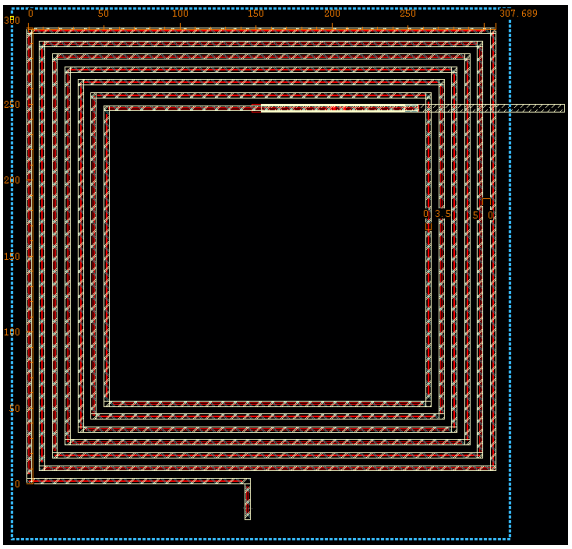


Figure 3.23: Inductor layout used in PA matching network.

targeted values. The overall area of the power amplifier is consumed almost entirely by the inductor used in the matching network. However, in the real system, the inductive loop-antenna would itself be used as part of the matching network, which would reduce the size of the matching inductor, thereby saving area.

Table 3.6: PA specifications vs. requirements

Specification	Target	Simulated Result
Output Power	-20 dBm	-18.3 dBm
Power Consumption	30 μW	37.45 μW
Efficiency	33%	39.5%
Area	-	0.1 mm^2

3.3 Transmitter Simulation Results

To verify functionality of the entire transmitter, a number of simulations were completed. The first was the time to acquire lock. Due to the the VCO frequency being much higher than the reference frequency, simulating the entire PLL is difficult due to the long time

constants associated with the loop filter. Thus, a Verilog-A model of the oscillator was developed (attached in Appendix C) to allow faster simulation turnaround of the system parameters. Figure 3.24 shows results from a simulation of the initial time to acquire lock. Figure 3.25 shows simulations of the frequency step response of the PLL, where the reference frequency is changed from 1 MHz to 1.0324 MHz, to mimic a change in channel value from 2402 MHz to 2480 MHz (worst-case channel change). The lock time for a step input is observed to be less than 100 μs, which comfortably meets the Bluetooth advertising event timing requirements.

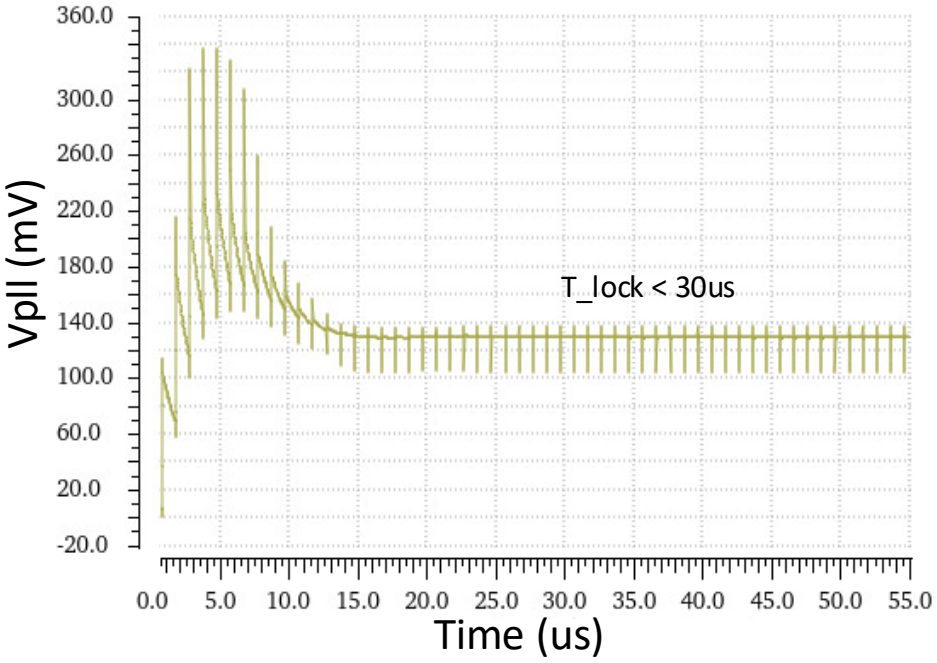


Figure 3.24: TX startup locking transient using a Verilog-A VCO model.

Another important simulation is the reference spur expected from the overall PLL. Again, this cannot be obtained directly from simulations of the entire PLL due to the excessively long simulation times. However, the work in [32] shows that one can find a relationship between the magnitude of reference signal at the VCO input to the reference spur *Spur* generated as:

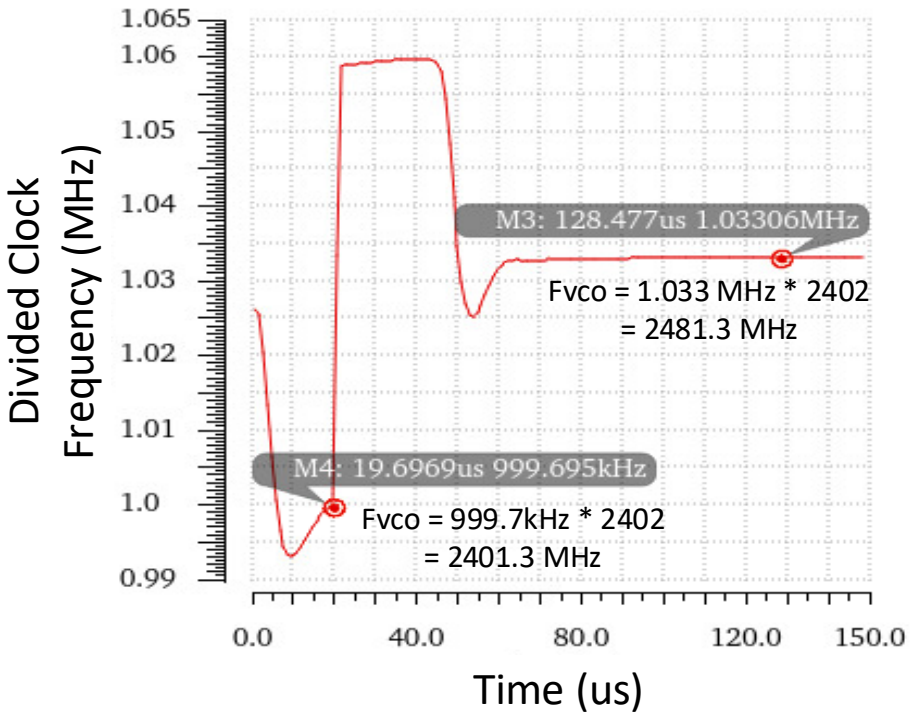


Figure 3.25: PLL locking transient between 2402 MHz and 2480 MHz channel using a Verilog-A VCO model.

$$Spur = \frac{Sideband}{Carrier} = 20\log(\frac{K_{VCO}E_m}{2f_{ref}}), \tag{3.17}$$

where E_m is the magnitude of the voltage at the input of the VCO at F_{ref}. Thus, a fast Fourier transform (FFT) algorithm was run on the simulation result from Figure 3.24, which found that the *Spur* is -29 dBc. Referring back to Table 3.1, the Bluetooth standard requires that the adjacent channel reference spur be less than -20 dBm. This is trivial to meet given the targeted -20dBm output power, which would set the absolute spur level at -49 dBm.

Once the design parameters are set, a fully transistorized SPICE PLL loop simulation is done to increase confidence in the initial behavioural simulations, and to confirm that the design meets the target specifications. Figure 3.26 shows the control voltage of the VCO as lock is acquired from an initial power down state. The lock time agrees quite closely with

initial simulations. Figure 3.27 shows the sinusoidal output at the antenna, which is stable at 2.402 GHz. Figure 3.28 shows the frequency spectrum of the output. The spectrum shows that the antenna output power at 2.402 GHz is -20.75 dBm, which is just shy of the target -20 dBm. Furthermore, the worst-case reference spur is at -33.47 dBm. This is much less than the -29 dBc predicted, but still meets the absolute requirements. An improvement to the design would be to further reduce the reference spur without incurring a large power consumption penalty.

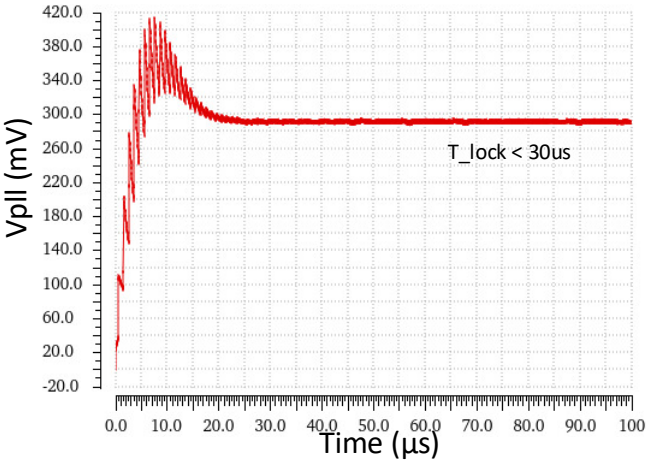


Figure 3.26: TX transient simulation showing locking transient from start-up to 2.402 GHz with transistorized VCO.

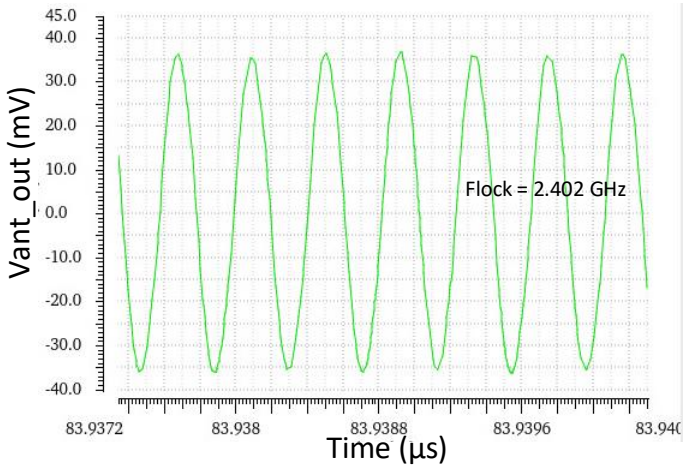


Figure 3.27: TX transient simulation showing output waveform at the antenna with parasitic extracted VCO.

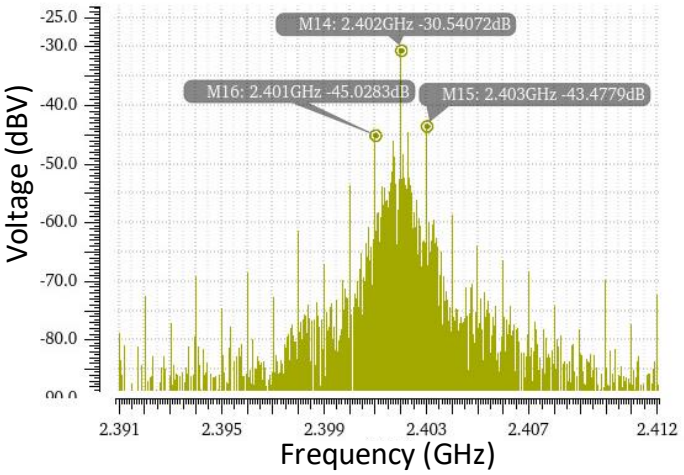


Figure 3.28: TX transient simulation showing FFT of output waveform with parasitic extracted VCO.

The power consumed when locked is summarized in Table 3.7. As expected, the most power-hungry component of the PLL is the VCO. However, the PA block's consumption

was significantly reduced by targeting the minimum required output power rather than the maximum. As can be seen in the table, the TX power consumption is more than 50 μW below the target specification. Finally, Table 3.8 summarizes the simulated performance vs. target specifications. Thus, the design of an ultra-low-power Bluetooth compliant GMSK modulator has been completed.

Table 3.7: TX power consumption summary.

Sub-block	Simulated Result
Oscillator	126 μW
Divider	32 μW
PFD+CP	15 μW
PA	25 μW
Total	198 μW
Bluetooth TX Power Budget	250 μW

Table 3.8: TX specifications vs. simulated results.

Specification	Target		Simulated Result
	Minimum	Maximum	
RF Output Power (Pout)	-20 dBm	10 dBm	-20.5 dBm
Channel Frequency Range	2402 MHz	2480 MHz	2.2–2.6 GHz
Modulation Frequency Range	-250 kHz	250 kHz	$\pm$250 kHz
Adjacent Spur @ 2MHz offset	–	-20 dBm	-30.5 dBm
Adjacent Spur @ 3MHz offset	–	-30 dBm	-49 dBm
Maximum Frequency drift	–	$\pm$ 50 kHz	–
Power Consumption	–	250 μW	200 μW
Phase Noise @ 1.5 MHz	-92 dBc/Hz	–	-107.7 dBc/Hz @ 1MHz
Lock Time	–	$\leq$ 100 μs	$\leq$ 30 μs

Chapter 4

Potentiostat and Sensor Readout Design

To implement a glucose sensor, a potentiostat is necessary to set a constant potential across the interface to drive the electrochemical reaction of interest. In the proposed measurement system, the current generated from this reaction is then converted to a digital value by an incremental delta-sigma ADC converter.

The requirements of these blocks stem from the sensor used. As mentioned earlier, to limit the scope of this thesis, the system assumes that the input sensor is equivalent to the sensor used in [2]. Important sensor parameters used in the design are re-summarized in Table 4.1 which refer to parameters in Figure 2.15.

The other driver of block requirements is the power consumption. Table 4.2 reiterates the power consumption requirements of the block. To meet these requirements, V_{DD} of 0.5V was used throughout the system (with one exception to be discussed). The remainder of this chapter delves into the circuit design of these two sub-blocks based on the specifications derived in Table 1.2 and topologies chosen in Chapter 1 and Chapter 2.

4.1 Potentiostat

Figure 4.1 shows the chosen potentiostat topology. This is similar to the architecture in [6], but the proposed potentiostat is designed in a 45 nm CMOS SOI technology (as opposed to a bulk CMOS technology as in [6]) and operates at a supply voltage of only 0.5 V. To design the potentiostat, circuit level requirements must be derived. Given the aggressive

Table 4.1: Sensor Specifications.

Specification	Nominal Value or Range
Sensor Output Current Range	1 nA - 100 nA
Required Sensor Current (I_F) Resolution	0.1 nA
Required Cell Voltage (V_{cell})	0.4 V
$R_{Interface,WE}$	1 GΩ
$R_{Interface,CE}$	0.667 GΩ
$R_{Interface,RE}$	20 kΩ
$R_{Solution}$	10
$C_{Interface,WE}$	110 nF
$C_{Interface,CE}$	165 nF
$C_{Interface,RE}$	10 pF

Table 4.2: Potentiostat and Readout Power Consumption Targets.

Sub-block	Target
Potentiostat	0.3 μW
ADC	6 μW

power target of 0.3 μW, the power distribution of the potentiostat must be partitioned into two distinct sections: (1) a section that establishes the electrochemical cell voltage V_{CELL} and (2) a section that measures the sensor current I_F. In Figure 4.1 the left side is powered by $AVDD_{POT}$, whereas the right side is powered by $AVDD_{ADC}$. During the initial reaction phase, only $AVDD_{POT}$ is powered on. Since the reaction time is on the order of seconds, the power consumed by $AVDD_{POT}$ consumes the most energy, and thus is the most power-sensitive block in the entire system. Thus, the design of the potentiostat is broken down into the design of the control amplifier feedback loop and the auxiliary amplifier mirroring.

The regulation circuitry must be able to sink 1-100 nA of current. Furthermore, given the range of sensor physical parameters, the input voltage V_{IN} was specified between 0 V and 0.5 V. This also allows the potentiostat flexibility to be tested with other sensors. The output voltage offset is specified to be +/- 5 mV (3σ), in order to set the cell potential relatively accurately. The phase margin (PM) of the voltage regulation loop was chosen to be greater than 65° across transistor PVT with nominal sensor parameters. Furthermore, a looser target specification of 50° of PM is targeted across the range of sensor parameters with typical (TT) transistors.

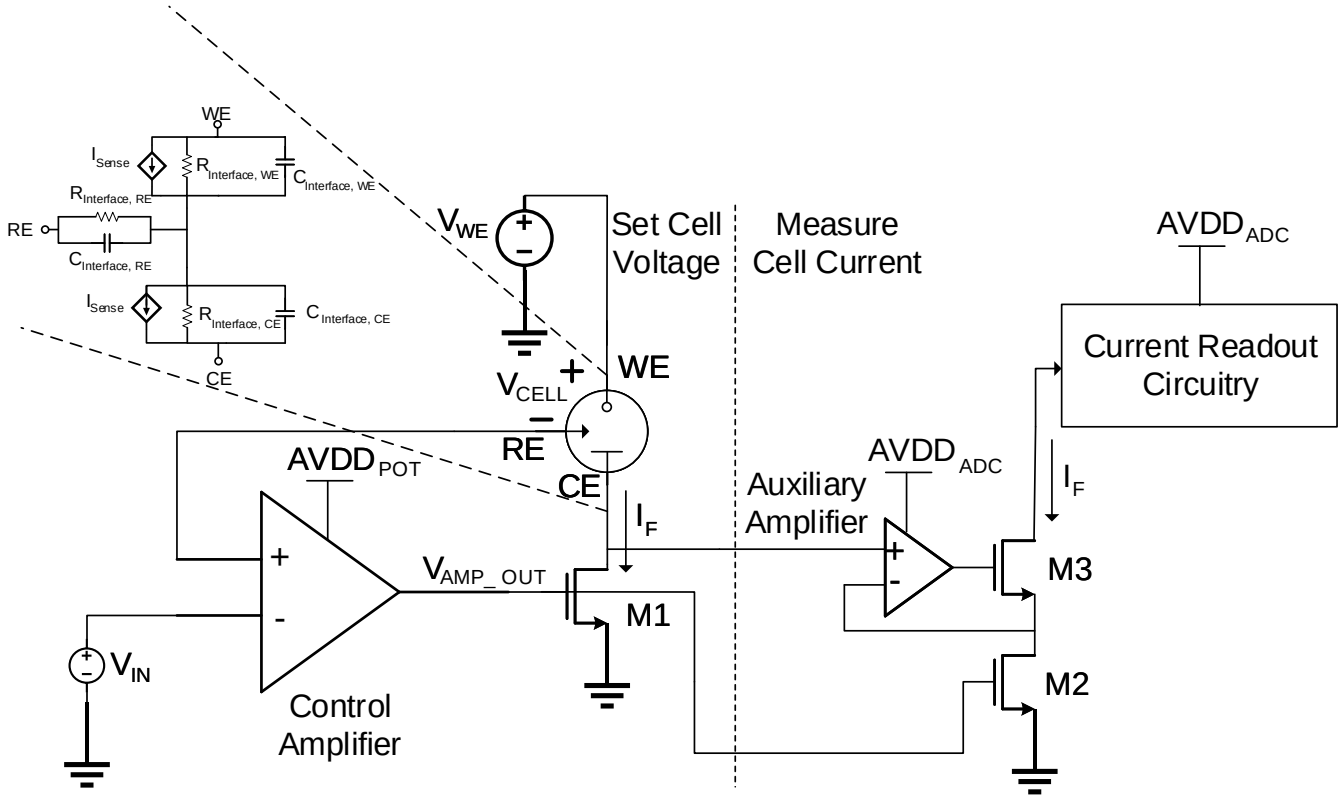


Figure 4.1: Potentiostat architecture

4.1.1 Voltage Regulation

Figure 4.1 shows a control amplifier which drives a common source output stage implemented using transistor M1. This is done to limit output voltage headroom consumed by the minimum V_{ds} necessary to keep M1 in saturation, V_{dsat}. For the output stage to operate in the linear region, the minimum V_{dsat} (which is the voltage at the CE V_{CE})for M1 is 0.1 V. To find the minimum voltage required at the WE (V_{WE}) necessary so that

transistor in Figure 4.1 remains in saturation, the following equation can be used:

$$\begin{aligned} V_{CELL} &= V_{WE} - V_{IN} \\ V_{WE} &= V_{CE} + \frac{V_{CELL}}{A_{CEtoWE}} + V_{CELL} \\ V_{WE} &> 0.1 + \frac{0.4V}{1.5} + 0.4 = 0.767 \text{ V} \end{aligned} \tag{4.1}$$

where for the assumed sensor, the cell voltage V_{CELL} is 0.4 V, the area ratio between the CE and the WE A_{CEtoWE} is 1.5, and the minimum CE voltage is 0.1 V. The voltage drop from V_{WE} and V_{CE} was calculated using the A_{CEtoWE}, since the voltage divider formed between the two nodes have resistances which scale to their relative area difference. Thus, it is impossible to bias the working electrode under the chosen supply voltage. Therefore, a voltage of 0.8 V is chosen for V_{WE} so that it is exactly double the required input voltage V_{IN} of 0.4 V, which sets V_{CE} at 0.133 V. This ratio is desirable, as it allows the generation of the working electrode voltage from a simple voltage doubler circuit. However, the work in this thesis currently provides V_{WE} and V_{IN} externally.

Figure 4.2 shows the control amplifier circuit and the regulation loop. The dual input stage formed using transistors M1, M2, M5 and M6 allows rail-to-rail input voltage operation. The voltage regulator loop is a 3-stage amplifier, which is stabilized by the large sensor capacitance. To improve stability, the internal amplifier stages were sized to maximize their bandwidth while still being longer length thick oxide transistors to reduce leakage currents. Despite the minimum sizing, the transistors operate in deep-subthreshold due to the small transistor current density $\frac{I_{DS}}{W}$ (to reduce power consumption), which impacts the phase margin of the overall loop.

Figure 4.3 simulates the loop bandwidth gain and phase of the loop with $I_F = 100$ nA. The loop bandwidth is less than 1 Hz, which is a consequence of using the sensor capacitance to stabilize the feedback loop. Furthermore, the phase margin for the system is 89°. The dominant pole f_{p1} is below 1Hz, the next pole f_{p2} is approximately 200 kHz, and the third pole f_{p3} is approximately 1 MHz. The phase margin was also measured after sweeping the sensor impedances with one magnitude of variation, along with process corners. The worst case phase margin for the voltage feedback regulator was simulated to be greater than 51°, where only the sensor capacitance C_{WE} and C_{CE} affected the overall stability. Approximate expressions for the poles of the system are:

$$
\begin{aligned}
f_{p1} &= \frac{1}{2\pi(r_{o_{M1}}//R_{WE})C_{WE}} \\
f_{p2} &= \frac{1}{2\pi(r_{o_{M11}}//r_{o_{M12}})C_{Stage2}} \\
f_{p3} &= \frac{1}{2\pi(r_{o_{M2}}//r_{o_4}//r_{o_{10}})C_{Stage1}}
\end{aligned}
\tag{4.2}
$$

where $r_{o_{M1}}$ is the small-signal output impedance of M1, C_{Stage1} is the capacitance to ground at the output of the first stage, C_{Stage2} is the capacitance to ground at the output of the second stage, f_{p1} is the dominant pole of the system, and $f_{p1} << f_{p2} < f_{p3}$. Since C_{WE} is approximately 110 nF (10^{-7}), as compared C_{Stage1}/C_{Stage2} which is on the order of 10^{-14}, f_{p1} sets the stability of the amplifier. Therefore, it is clear that increasing the sensor capacitance improves the phase margin (at the expense of bandwidth).

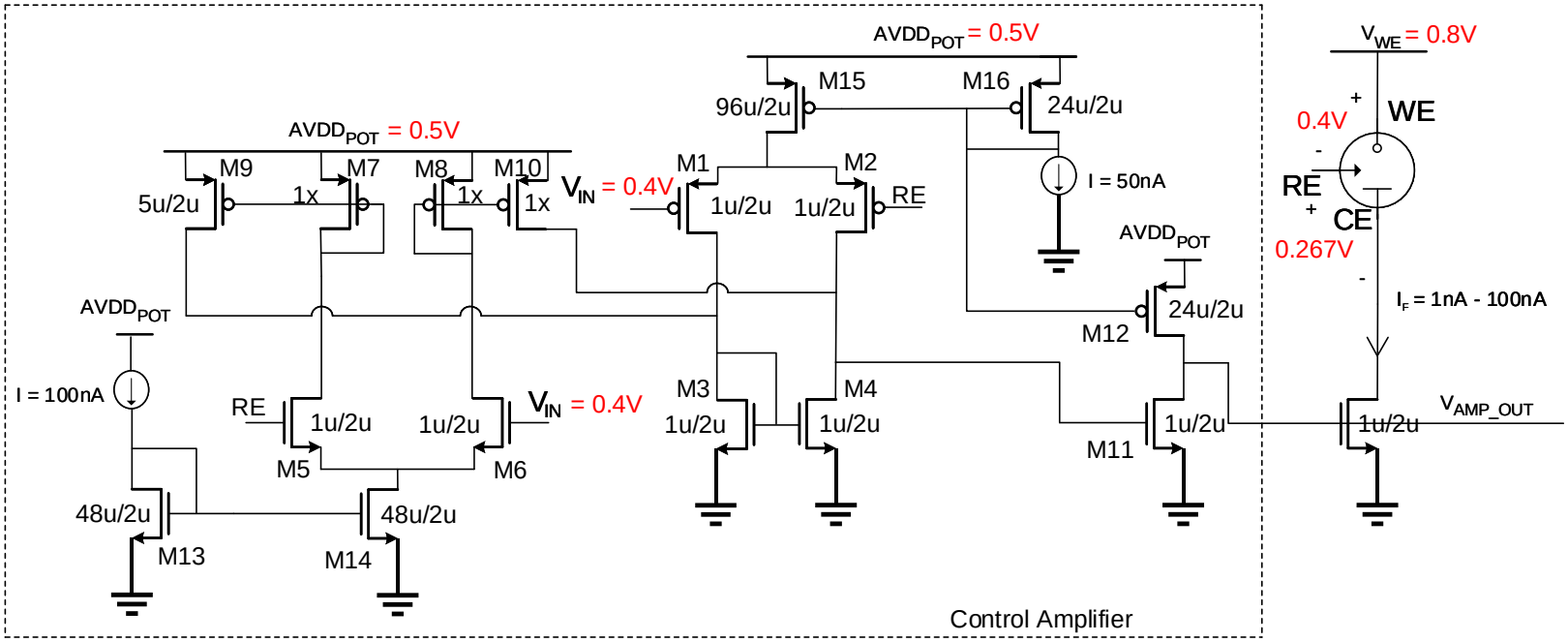


Figure 4.2: Control amplifier feedback loop.

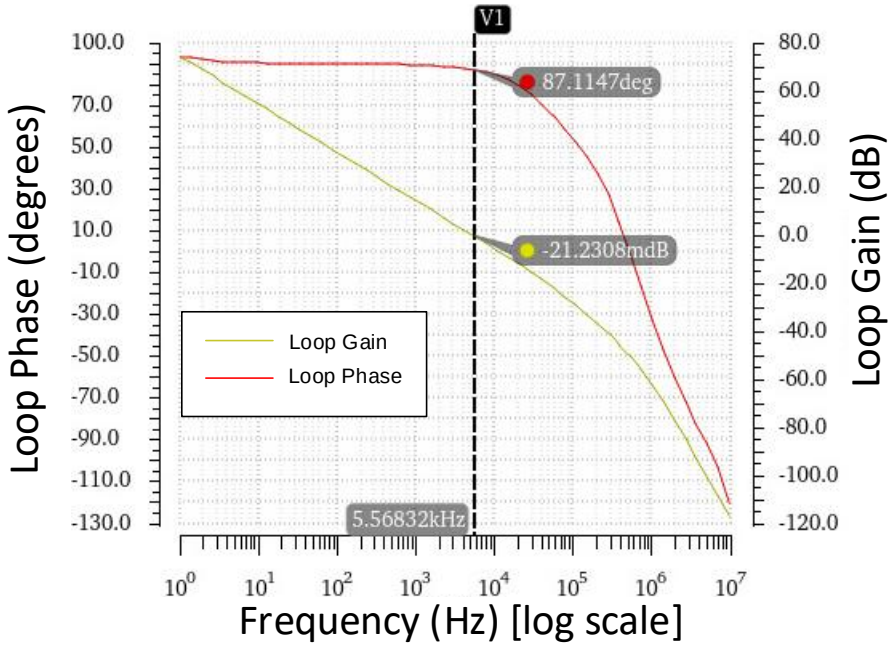


Figure 4.3: Simulated loop-gain and phase of control loop with nominal sensor parameters and I_F of 100 nA.

The gain of the feedback loop is simulated across input voltage V_{IN} in Figure 4.4. Due to the headroom requirements enforced by the sensor dimensions, the amplifier cannot operate at low input voltages as it would require the V_{CE} to move below 0 V. Thus, 0.289 V is the minimum V_{IN} necessary to properly regulate the loop. However, given an alternative sensor with much larger A_{CEtoWE} (which may be the case with commercial sensors), it is possible to reduce the minimum V_{IN} to 65 mV.

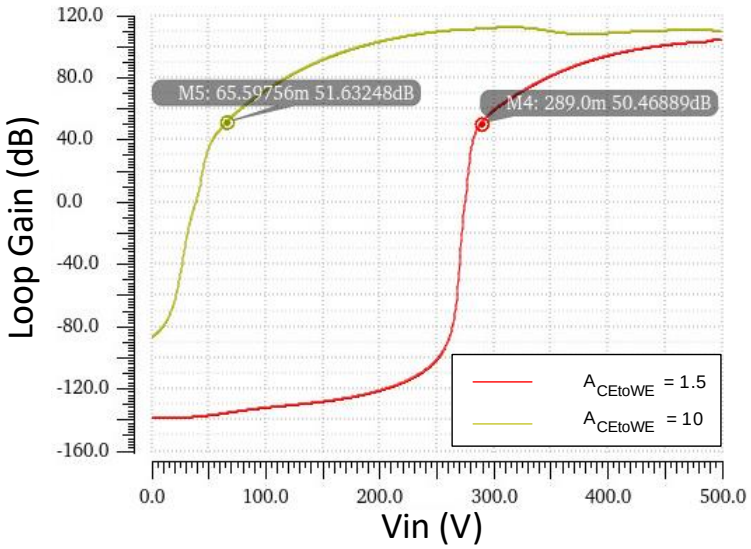


Figure 4.4: Simulated DC gain of control loop accross input voltage for two A_{CEtoWE} ratios.

The output voltage offset V_{offset} due to statistical mismatch and technology parameter variation was simulated to be 0.865 mV (3σ). This is well below the initial target of 5 mV.

Finally, the circuit power was simulated to be 268 nW +/- 66.5 nW (3σ), which includes the worst case power drawn from the working electrode. This is slightly above the targeted specification of 300 nW for parts above 1.45σ, which implies 8% of parts will fail this spec. Given that this is a research test-chip, this failure rate was deemed acceptable.

Table 4.3: Control Amplifier Performance Summary

Specification	Simulated Value
Power	265 nW $\pm$ 66.5 nW (3σ)
Loop Gain	>70 dB
Bandwidth	<1 Hz
Phase Margin	$> 50°$
Offset	0.865 mV

4.1.2 Gain-boosted current mirror

The design of the gain boosted current mirror is shown in Figure 4.5. The auxiliary amplifier differs from the control amplifier in that it follows a conventional two-stage operational amplifier design. The dominant pole is set by the differential input stage. The R-C compensation network is inserted between the first and second stages to increase the Miller capacitance and to move the inherent right-half plane zero to the left-half plane. The bias current in the amplifier is much higher than the control amplifier, as the amplifier needs to respond to transients that appear on the output of the mirror due to the ADC. Since these transients occur at the 1 MHz sampling clock of the ADC, the amplifier needs to have a unity gain bandwidth above this frequency.

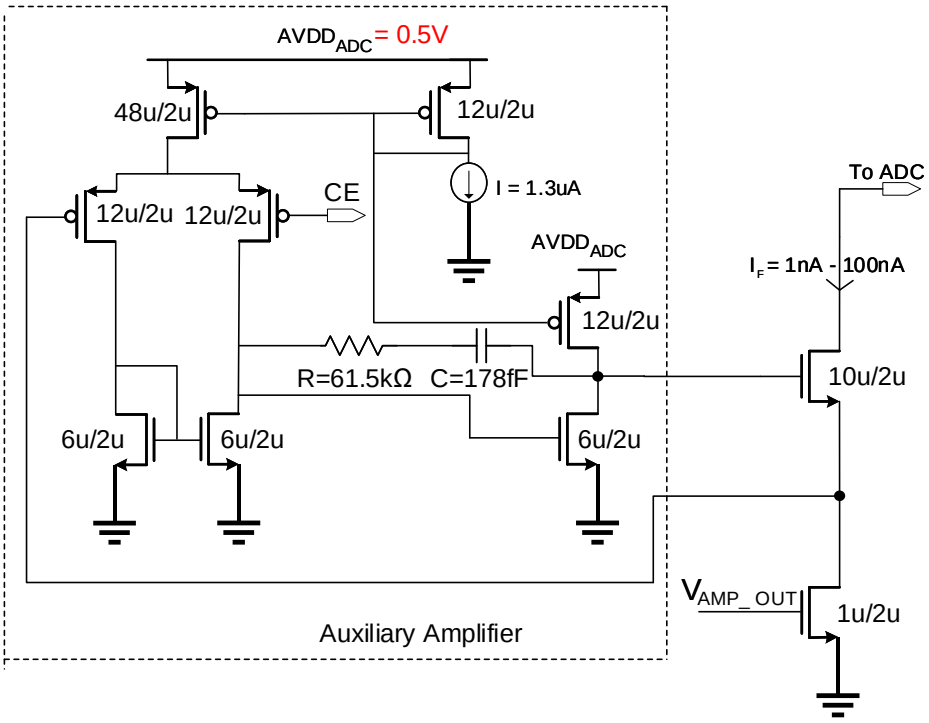


Figure 4.5: Schematic of gain-boosted current mirror.

Figure 4.6 simulates the loop gain and bandwidth of the auxiliary amplifier connected to the current mirror. The DC gain is 47 dB, the 3-dB bandwidth is 50 kHz, the unity-gain-bandwidth is 6.04 MHz, and the phase margin is 44°. Figure 4.7 simulates the improvement

in absolute current error due to mirroring between the gain-boosted cascoded mirror and a standard cascode current. It is clear that the gain error has been reduced to below 40pA, which is much below the required current resolution for the application. Furthermore, when including random variation, the maximum random variation of the gain-boosted mirror is 27.6 times less than the simple cascode mirror.

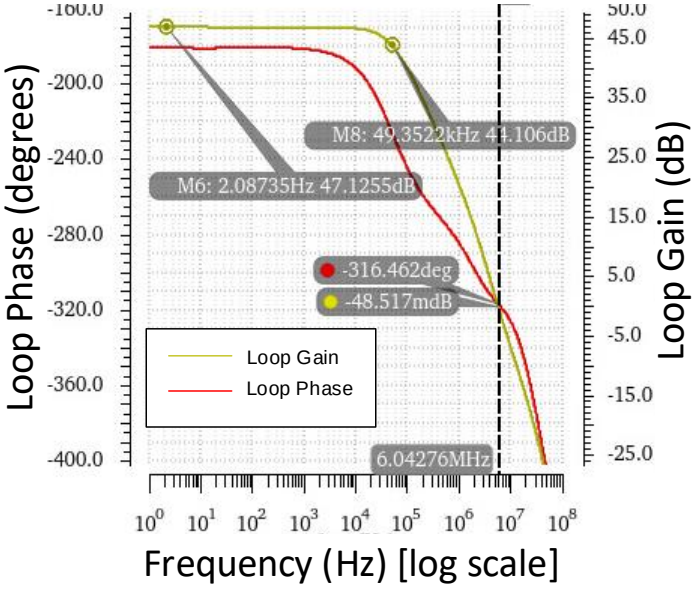


Figure 4.6: Loop gain and phase of auxiliary loop with I_F of 100 nA.

The power consumption of the gain-boosted current mirror is simulated as: 2.1 μW +/- 0.76 μW (3σ). This power consumption must be added to the incremental ADC power consumption to measure whether the power budget has been met.

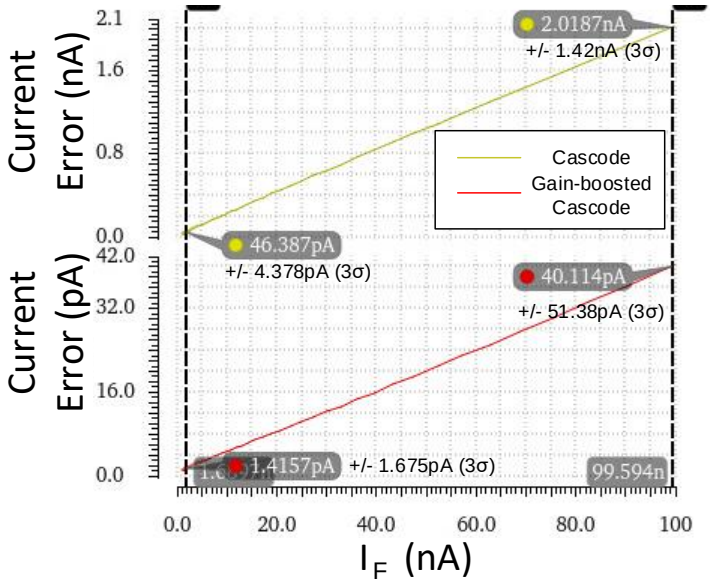


Figure 4.7: Absolute current error from sensor to ADC input.

4.2 Incremental ADC

Once I_F has been mirrored, it is fed into a 1st-order IADC to be digitized for the Bluetooth transmitter. The current ranges from 1nA to the full-scale (I_{FS}) value of 100 nA, which corresponds to 0.05 mM - 1 mM of glucose concentration. The system specification requires that 0.01 mM of resolution to adequately track the changes in blood sugar levels, which corresponds to an LSB current I_{LSB} of 0.2 nA. Thus, the resolution required in bits N_{bits} from the ADC can be derived from:

$$I_{LSB} = \frac{I_{FS}}{2^{N_{bits}} - 1} \tag{4.3}$$

,

where $N_{bits} = 10$. As mentioned in Chapter 2, the required signal-to-noise-and-distortion ratio (SINAD) to achieve an effective number of bits (ENOB) of 10 is 61.96 dB. The power budget for the ADC is 6 μW, including the gain-boosted auxiliary amplifier. Accounting for that block, the remaining budget for the ADC proper was 3 μW.

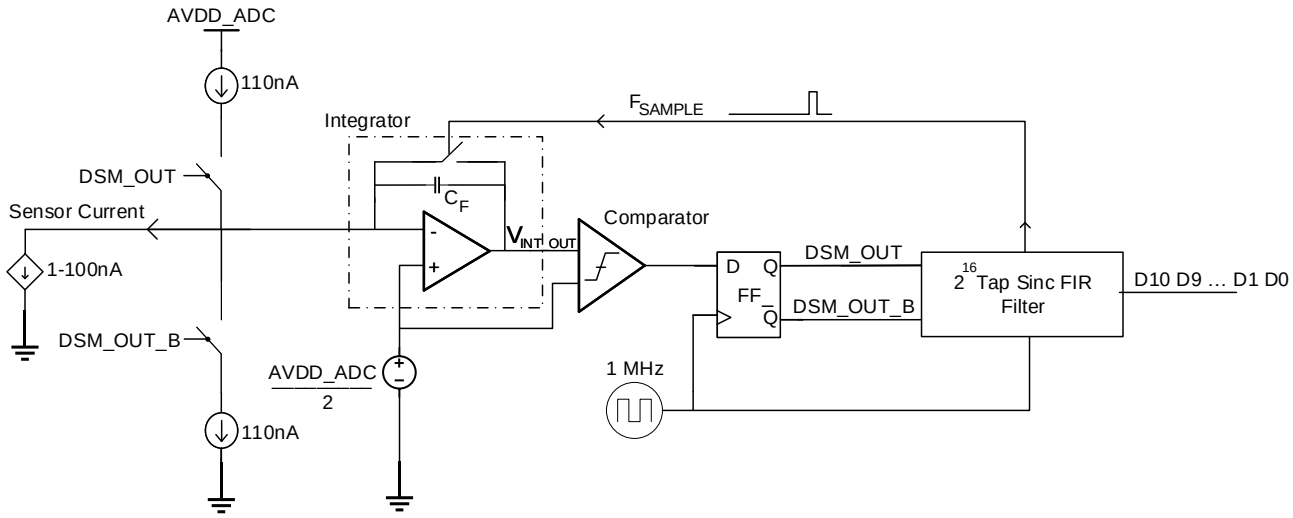


Figure 4.8: Incremental ADC architecture.

Figure 4.8 shows the architecture of the IADC. Current is integrated across the integrator op-amp (Σ), after which it is digitized by a 1-bit DAC (clocked comparator). The modulator output is fed back into the integrator (Δ) by either adding or subtracting a full-scale current of 110 nA. This current is set slightly higher than the maximum expected current range of the glucose sensor to ensure that the integrator output does not saturate. The comparator output is simultaneously filtered and decimated to a slower rate F_{SAMPLE}. As a consequence of the chosen topology, the IADC must be accurate to 11-bits to ensure 10-bit accuracy because the first bit acts as a sign bit. The clock rate for the ADC is set to 1 MHz, to coincide with the reference clock rate for the wireless subsystem. F_{SAMPLE} is set to $\frac{F_{CLK}}{2^K} = \frac{1MHz}{2^{16}} = 15.25$ Hz based on the 2^{16}-tap sinc filter implementation of the decimation filter.

Given these parameters, the oversampling rate (OSR) for the system can be calculated as:

$$OSR = \frac{F_{CLK}}{2F_{SAMPLE}} = \frac{F_{CLK}}{2\frac{F_{CLK}}{2^K}} = 2^{K-1} = 2^{15} = 32894 \tag{4.4}$$

where K represents the number of bits in the sinc FIR filter. The SQNR improvement as a function of OSR for a 1st-order delta-sigma ADC with a 1-bit modulator is calculated

as [11]:

$$\begin{aligned} \sigma_{sig}^2 &= \frac{1}{2} \\ \sigma_{q,sincfilter}^2 &= \frac{2}{3(OSR)^2} \\ SQNR_{ADC} = \frac{\sigma_{sig}^2}{\sigma_{q,sincfilter}^2} &= \frac{3(OSR)^2}{4} = \frac{3(2^{15})^2}{4} = 89 \text{ dB} \end{aligned} \tag{4.5}$$

where σ_{sig}^2 represents the signal power, $\sigma_{q,sincfilter}^2$ represents the quantization noise power of a 1st-order delta-sigma ADC with a sinc filter, and $SQNR_{ADC}$ represents the signal-to-quantization-noise ratio.

From the calculation above, the OSR is much higher than necessary to achieve the required accuracy level, and thus can be decreased to improve energy efficiency of the IADC. However, as will be shown later, circuit non-idealities reduce the effective OSR which reduces the overall accuracy of the converter.

4.2.1 Integrator

Due to the delta-sigma feedback, the output voltage from the integrator will form a triangle wave centred at 0.25 V. Figure 4.9 includes the schematic of the integrator op-amp. This amplifier was also designed as a two-stage amplifier with the same sizing as the gain-boosted amplifier, to maximize design re-use. Furthermore, a two-stage op-amp is the optimal candidate in the supply constrained system, as it has the most headroom available compared to telescopic or folded cascode amplifiers. In addition, given that the output must be able to source or sink current based on the input current in the feedback path, a two stage amplifier is ideal as it can drive resistor loads, rather than drive strictly capacitive loads. To set the size of the feedback capacitance C_F, both the output swing and noise requirements must be examined. The voltage swing V_{INTOUT} can be found as:

$$\begin{aligned} I_{integrate} &= I_F \pm 110 \text{ nA} \\ V_{INTOUT} &= \frac{I_{integrate}}{C_F F_{REF}} \end{aligned} \tag{4.6}$$

where $I_{integrate}$ represents the current integrated by the op-amp, V_{INTOUT} is the voltage at the output of the comparator, and F_{REF} is set to 1 MHz. Thus, if we set a limit to the maximum swing on the input to the comparator as ± 0.1 V to keep the amplifier in its

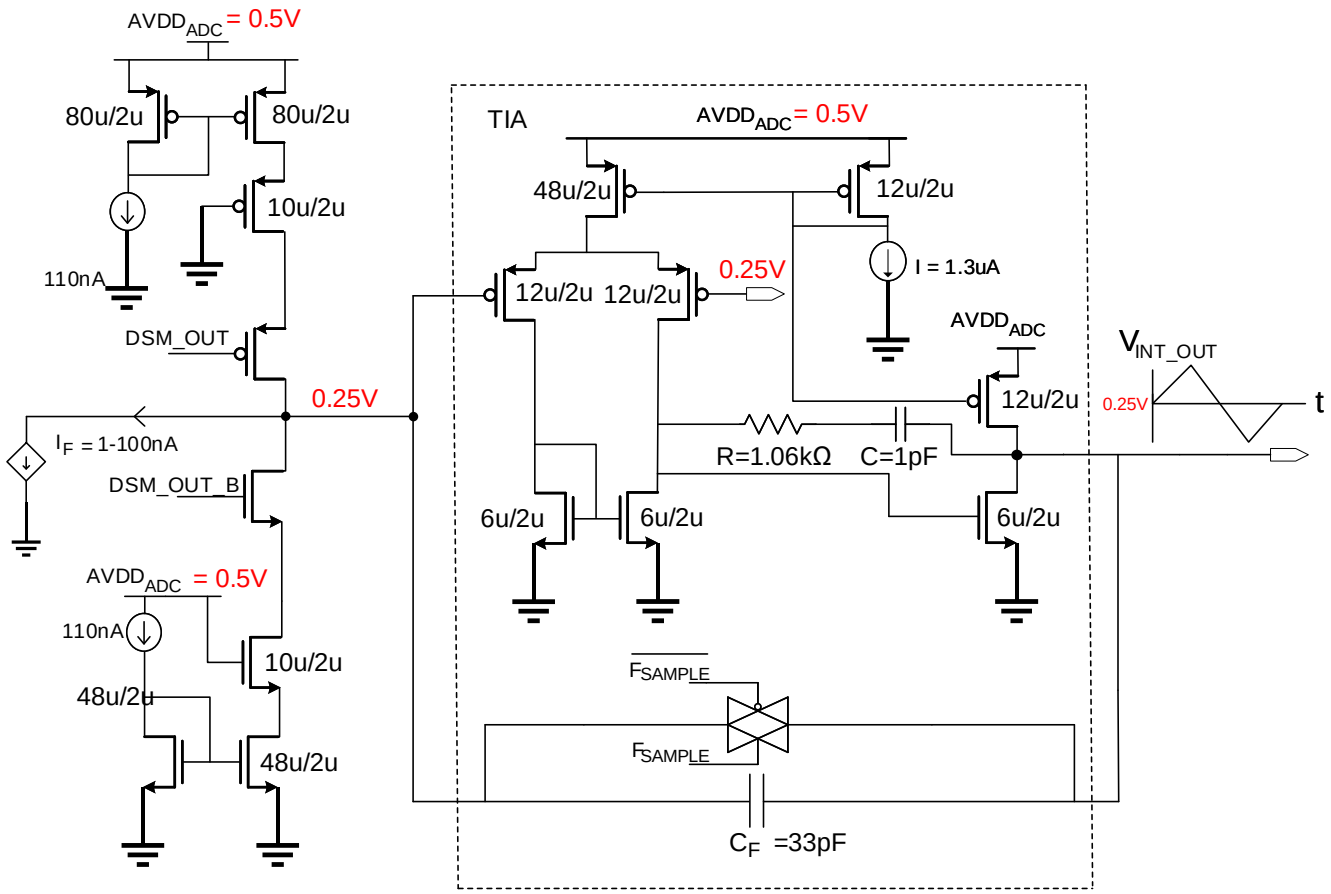


Figure 4.9: Schematic of integrator op-amp and current sources in delta-sigma IADC.

linear region of operation, the minimum feedback capacitance C_F is calculated as 2.1 pF. Using this value, the output swing for I_F of 1 nA is $\pm$ 52 mV.

In addition to signal swing, the impact of C_F on noise must be considered. To analyse the noise transfer from the potentiostat to the integrator, the transimpedance of the integrator needs to be derived. The transimpedance function of the periodically reset

integrator can be found assuming a nominal integration time T_{INT} as:

$$\begin{aligned} V_{INTOUT}(T_{INT}) &= \frac{1}{C_F}\int_0^{T_{INT}} I_{integrate}(t)\ dt \\ V_{INTOUT}(T_{INT}) &= \frac{T_{INT}}{C_F} I_{integrate}(t) * [u(t) - u(t - T_{INT})] \end{aligned} \tag{4.7}$$

Applying the Laplace transform to both sides gives:

$$\begin{aligned} V_{INTOUT}(s) &= \frac{T_{INT}}{C_F} I_{integrate}(s) \left[\frac{1}{s} - \frac{1}{s}e^{-sT_{INT}}\right] \\ V_{INTOUT}(f) &= \frac{T_{INT}}{C_F} I_{integrate}(f) e^{-j\pi f T_{INT}} \left[\frac{sin(\pi\ fT_{INT})}{\pi\ fT_{INT}}\right] \\ H(f) = Z(f) &= \frac{V_{INTOUT}(f)}{I_{integrate}(f)} = \frac{T_{INT}}{C_F} sinc(fT_{INT}) \\ \text{where } sinc(x) &= \frac{sin(\pi x)}{\pi x} \end{aligned} \tag{4.8}$$

For the output signal where glucose sensor signal changes much slower compared to T_{INT}, it is clear that

$$V_{INTOUT} = \frac{T_{INT}}{C_F}(I_F \pm 110\text{ nA}) \tag{4.9}$$

However, since we are only interested in signal power, the constant term will be ignored.

$$V_{INTOUT}^2 = \left(\frac{T_{INT}}{C_F}\right)^2 I_F^2 \tag{4.10}$$

For sensor noise stemming from the potentiostat, one can derive the output noise voltage assuming the noise PSD is white as:

$$\begin{aligned} \overline{V_{N,OUTPUT}}^2(f) &= |H(f)|^2 \overline{I_{N,Potentiostat}}^2(f) \\ \overline{V_{N,OUTPUT}}^2(f) &= \left[(\frac{T_{INT}}{C_F} sinc(fT_{INT}))\right]^2 \overline{I_{N,Potentiostat}}^2(f) \\ \overline{V_{N,OUTPUT}}^2 &= \int_0^\infty \left[(\frac{T_{INT}}{C_F} sinc(fT_{INT}))\right]^2 \overline{I_{N,Potentiostat}}^2(f) \\ \overline{V_{N,OUTPUT}}^2 &= (\frac{T_{INT}}{C_F})^2 (\frac{1}{2T_{INT}}) \overline{I_{N,Potentiostat}}^2(f) \\ \overline{V_{N,OUTPUT}}^2 &= \frac{1}{2}(\frac{T_{INT}}{C_F^2}) \overline{I_{N,Potentiostat}}^2(f) \end{aligned} \tag{4.11}$$

where $\overline{I_{N,Potentiostat}^2}(f)$ is the input current noise PSD from the potentiostat, $\overline{V_{N,OUTPUT}^2}(f)$ is the output noise PSD at the output of the integrator, and $\overline{V_{N,OUTPUT}^2}$ is the average output noise power (i.e., integrated noise PSD). Thus the overall SNR can be found as:

$$
\begin{aligned}
SNR &= \frac{V_{INTOUT}^2}{\overline{V_{N,OUTPUT}^2}} \\
SNR &= \frac{(\frac{T_{INT}}{C_F}^2)I_F^2}{\frac{1}{2}\frac{(T_{INT}}{C_F^2})\overline{I_{N,Potentiostat}^2}(f)} \\
SNR &= 2T_{INT}(\frac{I_F^2}{I_{N,Potentiostat}^2(f)})
\end{aligned}
\tag{4.12}
$$

The potentiostat output noise PSD is simulated in Figure 4.10 where $T_{INT} = T_{SAMPLE}$ (65.5 ms), $I_F = 1$ nA, and $C_F = 33$ pF. This simulation applies the eq. 4.11 to the potentiostat output current noise PSD to estimate the noise of the ADC. The integrated noise referred to the input of the IADC is 0.1 LSB at $I_F = 1$ nA and 0.3 LSB at $I_F = 100$ nA. Therefore, the thermal noise is below 0.5 LSB, implying that the dominant noise source will be the quantization noise of the IADC rather than the thermal noise.

Another potential noise source is the noise injected by the reset switch which resets the integrator every sample. During the transition between the reset phase and integration phase, noise from the switch will be sampled on to C_F. This noise would then act as an offset on the comparator input, which varies from cycle-to-cycle. Detailed analysis of the reset noise is omitted. However, intuitively, the noise sampled onto the capacitor would be proportional to $\frac{kT}{C_F}$ where k represents Boltzmann's constant and T represents absolute temperature. Thus, this implies that an increase in C_F would improve the reset noise. Referring $\frac{kT}{C_F}$ to the input of the ADC yields < 0.01 LSB however, which implies that the reset noise contribution isn't significant.

Therefore, the design requires a minimum C_F of 2-2.5 pF, so as to provide adequate swing into the comparator. However, the maximum feedback capacitance C_F is set based on a trade-off between the reset noise contribution and the output swing in the comparator. Despite analysis indicating that the reset noise is insignificant, C_F was set to 33 pF to reduce the impact of reset-noise in the system, which limits the output swing to the comparator to 3.3 mV per F_{REF} cycle. This causes issues in the comparator which will be highlighted shortly.

The open loop gain and bandwidth of the integrator is simulated in Figure 4.11. The open-loop DC gain A_{OPEN} is simulated to be 63.4 dB. Finite open-loop gain has subtle

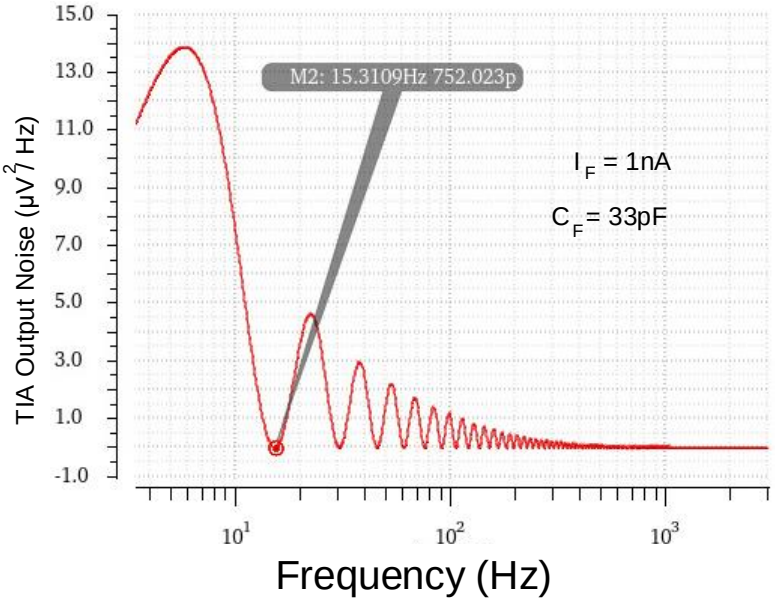


Figure 4.10: Simulated output voltage noise PSD of the integrator from current noise generated by the potentiostat.

effects on the overall delta-sigma system as it creates a leaky integrator. From a linear systems perspective, it can be shown that for DC inputs, the accuracy is limited to $\frac{1}{A_{OPEN}}$ [11], which is 77.8 pA in this case. Therefore, finite A_{OPEN} does not limit the ultimate resolution of the ADC since the minimum step is 107 pA for 10-bit accuracy. From a non-linear system perspective, finite DC gain manifests itself as a dead-band of $\frac{1}{2A_{OPEN}}$ around zero input current[11]. Thus, there is a dead-band from -0.04 nA to 0.04 nA. Since the minimum current from the sensor is 1 nA, this does not impact the performance of the ADC in this application.

Simulated PM of the integrator is 80°. The gain-bandwidth product is calculated to be 256 kHz, which may imply the circuit is too slow to be used with 1 MHz switching current inputs. However, given that the integrator is driven with a constant current and thus is used in a non-steady state manner, small-signal analysis does not adequately capture the speed requirements.

The amplifier output stage must be able to source or sink the current driven into its feedback node. Thus, the output stage will either source or sink an additional 0.25 μA

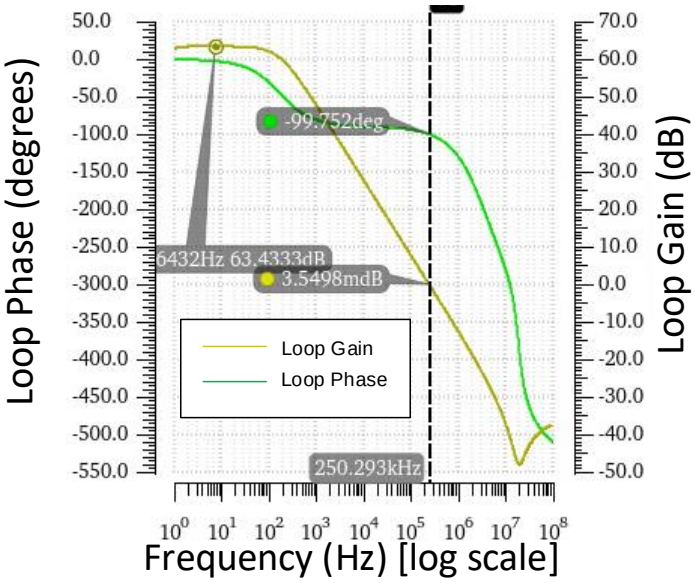


Figure 4.11: Open loop gain and phase of the integrator in integrating mode.

from its nominal value of 1.3 μA, which was set large enough to have its AC characteristics relatively agnostic to its load current.

The input voltage offset is simulated to be 2.6 mV +/- 0.8 mV (3σ). This offset voltage simply contributes to a DC offset in the output ADC code, which would ultimately be calibrated on a per sensor basis in the final system.

The input to the integrator is connected to the gain-boosted current-mirror in the potentiostat along with a pair of current-steered current sources (with dummy steered paths omitted in Figure 4.9). These mirrors were sized large enough to reduce the V_{dsat} to ensure that the cascoded current mirror can work with 0.25 V of headroom.

Finally, the power consumption of the integrator was simulated to be 0.9 μW $\pm$ 0.1885 μW (3σ). The power-savings comes from the PMOS input stage biased at mid-rail forcing the current mirror to act in triode, effectively limiting the first stage bias current to 0.12 μA, rather than the 5.2 μA expected except during slewing events.

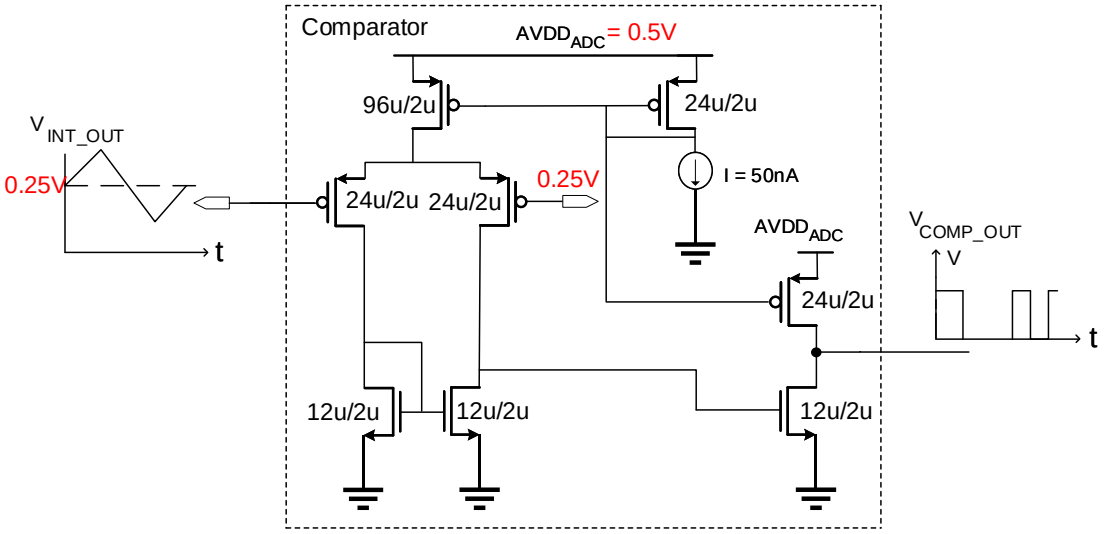


Figure 4.12: Implementation of 1-bit ADC

4.2.2 Comparator

The output of the integrator drives the comparator implemented in Figure 4.12. The comparator was also implemented as a two-stage amplifier. This topology was chosen to reduce design time. The comparator was biased at 50 nA for the following reasons: This current was used elsewhere in the sensor, so the bias generator could be reused; it increased the gain of the amplifier near the comparator trip point; and it was small enough to keep the DC power consumption of the block low. Since the same topology was used in the integrator, the sizing ratio was kept the same, but all transistor sizes were doubled. Furthermore, the compensation network was removed to increase the speed of the amplifier, since the comparator does not need to be stabilized.

Three key characteristics must be simulated: speed, hysteresis, and power consumption. Given that the circuit generally operates under large signal conditions, speed is characterized by transient simulation of propagation delay. Figure 4.13 shows the delay with large signal inputs to the comparator. The worst case delay is simulated to be approximately 1 μs, which is unacceptable, as the hold time of the following flip-flop would be violated.

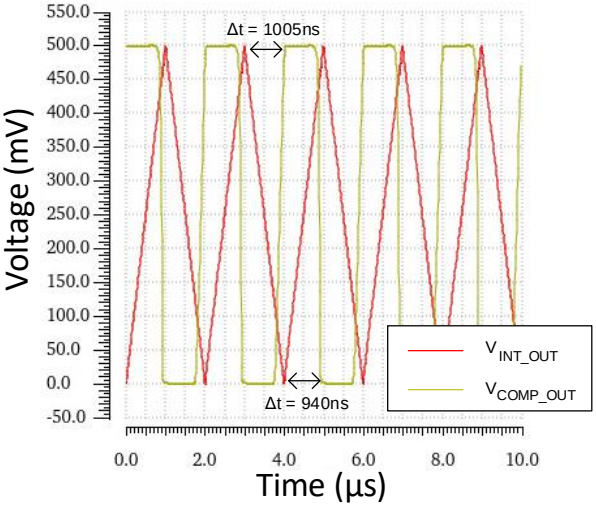


Figure 4.13: Transient delay of comparator with 1 MHz large-signal input data.

However, the delay problem becomes more severe for small signal inputs, which mimics the scenario where the glucose sensor current I_F is close to 0 nA. Given an integrator feedback capacitance of 33 pF, the integrator output changes at a rate of 3.3mV/μs. With this voltage at the comparator input, the output delay is simulated in Figure 4.14. In this simulation, the input voltage is continuously increasing until the comparator has switched values, after which point the input decreases. This mimics the operation of the delta-sigma ADC. The simulation results show that the output waveform is switching as if it is clocked at 220 kHz, rather than at 1 MHz. This has a side-effect of reducing the effective OSR to:

$$OSR_{EFFECTIVE} = 0.22\ OSR_{IDEAL}, \tag{4.13}$$

which directly impacts overall converter SQNR.

The offset voltage of the comparator is simulated as 0.2 mV +/- 0.2m V (3σ), which does not have a significant effect on the overall IADC. The hysteresis of the comparator was simulated to be approximately 20 nV which is negligible. Finally, the block level power consumption was simulated to be 83 nW.

Given the speed issues with the comparator operating at 1 MHz, a recommendation for future work would be to explore the use of a StrongARM architecture to increase speed without increasing power significantly [33].

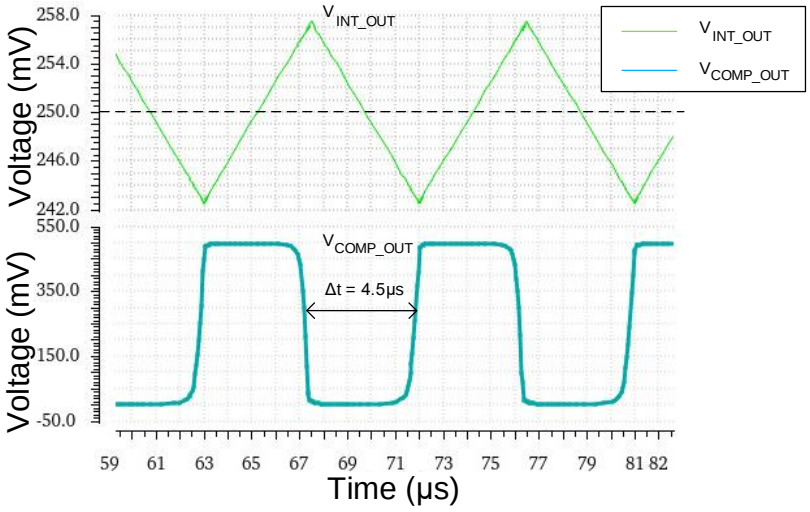


Figure 4.14: Transient delay of comparator with small-signal input data.

4.2.3 Decimation Filter

The decimation filter used in the IADC is shown in Figure 4.15 This circuitry implements a

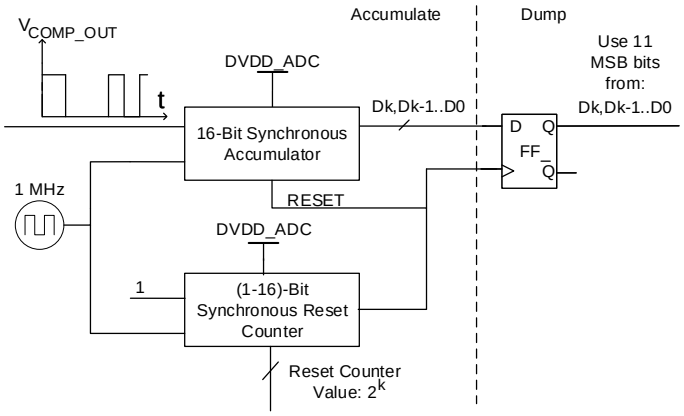


Figure 4.15: 2^{1-16} Tap Sinc FIR Decimation Filter.

1st-order sinc filter, which is effectively a moving average filter. This topology was chosen

to allow for simple digital circuitry that would consume little power, as well as be simple for hand layout. As the glucose current has been converted into the duty cycle of the modulator output, the synchronous accumulator in Figure 4.15 counts how many F_{REF} cycles the modulator has been high for within 2^k cycles. This value effectively becomes the digitized output, where the MSB is a sign bit. Thus, the effective sampling frequency is $F_{SAMPLE} = \frac{F_{REF}}{2^k}$. At the end of the sampling period, the accumulator is read and dumped onto output flip-flops, which represent the final digitized output. The value of k can be configured to be from 1 to 16. Higher values of k represent larger OSR values as well as longer conversion times, and, hence, larger energy consumption of the IADC. Since the accumulator output is k-bits wide, 11-bit output data (including signed MSB) can be extracted by taking the top 11 MSB bits from the k-bit output. The energy budget of the ADC has been specified assuming $k = 16$, which is the worst case. Based on earlier analysis, this should yield greater than 11-bit accuracy. The estimated power consumption of the sinc filter with $k = 16$ is 50 nW, which is negligible. Thus, k will be experimentally varied to verify the lowest value which achieves 11-bit SNR.

There is a distinct disadvantage to using a 1st-order sinc filter for a 1st-order delta-sigma system. Since this filter does not have strong sidelobe filtering compared to $sinc^2$ filtering, the noise shaped modulator output is not filtered as well, which amounts to a reduction in SQNR. The quantization noise power for an ideal filtered ($\sigma^2_{q,ideal}$), sinc filtered ($\sigma^2_{q,sincfilter}$), and $sinc^2$ filtered ($\sigma^2_{q,sinc^2filter}$) output data is shown as [11]:

$$\begin{aligned} \sigma^2_{q,ideal} &= \frac{\pi^2}{9(OSR)^3} \\ \sigma^2_{q,sincfilter} &= \frac{2}{3(OSR)^2} \\ \sigma^2_{q,sinc^2filter} &= \frac{2}{3(OSR)^3}. \end{aligned} \tag{4.14}$$

The $sinc^2$ filter is OSR times more effective than the sinc filter and approaches ideal filter performance. Thus, the digital circuitry should be changed in a future design iteration to use non-uniform weighted output taps on the FIR filter to achieve $sinc^2$ filtering. This would reduce the required OSR which would permit lower values of k. As a result, shorter conversion times wil be obtained, producing reduced energy consumption.

4.2.4 ADC Simulations

Figure 4.16 shows the simulated modulator output for a glucose current of 2 nA and 100 nA input to the potentiosat. For the first order modulator (MOD1), DC input signals are

encoded by the duty cycle of the output. Thus, the 2 nA signal appears at 50.9% duty cycle whereas the 100 nA input current appears as 95.45% duty cycle. As mentioned previously, due to the larger-than-necessary integrator feedback capacitance, the comparator and hence the modulator output switches at a slower speed than the 1 MHz clock rate. This is confirmed by simulating the integrator output voltage in Figure 4.17.

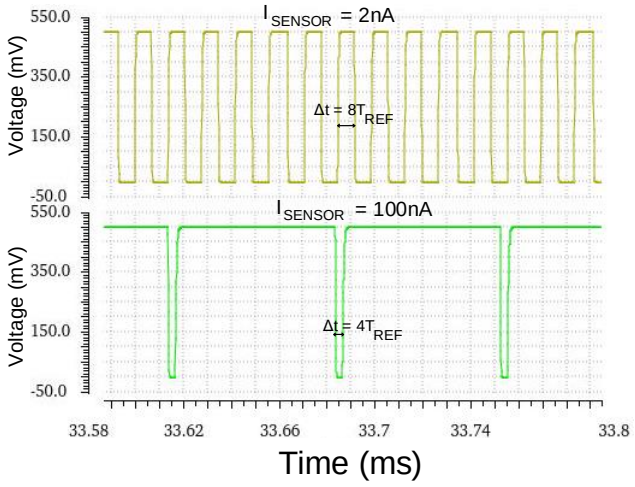


Figure 4.16: Modulator output for input glucose current of 2 nA and 100 nA.

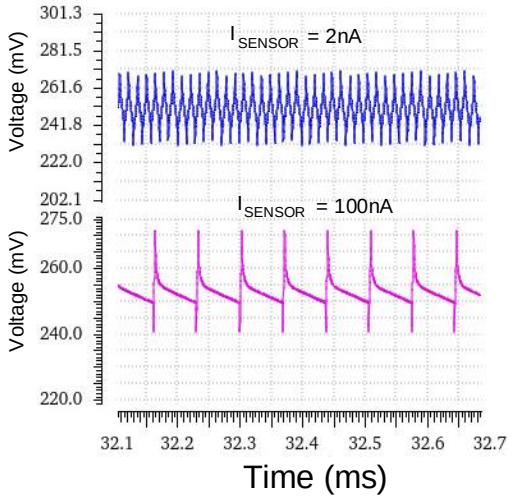


Figure 4.17: Integrator output for input glucose current of 2 nA and 100 nA.

An FFT of the modulator output is simulated in Figure 4.18 to confirm 1st-order modulator behaviour. The quantization noise has been shaped such that there is less in-band noise and higher out-of-band noise, which will be filtered by the decimation filter. Since the input is DC, the signal will always appear in the first bin (and one additional bin on each side due to Hann windowing). Due to signal leakage and insufficient transient cycles for low frequency bins, the noise in-band is extrapolated from the 20 dB/decade slope from 1kHz down to 10 Hz. The SQNR of the output, assuming an ideal decimation filter, is calculated to be:

$$\begin{aligned} SQNR &= \frac{P_{sig}}{P_{in-bandnoise}} \\ SQNR_{2\text{ nA}} &= -18dB-(-118-40+10log_{10}(0.5/NBW)) = 81.76\text{ dB} \\ SQNR_{100\text{ nA}} &= -12dB-(-118-40+10log_{10}(0.5/NBW)) = 87.76\text{ dB} \end{aligned} \tag{4.15}$$

where P_{sig} represents the signal power, $P_{in-bandnoise}$ represents the noise power in the bandwidth, $SQNR_{2nA}$ represents the signal-to-quantization noise ratio for a 2 nA input signal, and $SQNR_{100nA}$ represents the signal-to-quantization noise ratio for a 100 nA input signal. The simulated SQNR matches closely to the SQNR predicted in eq. 4.14, which is greater than the required SQNR for 11-bit accuracy.

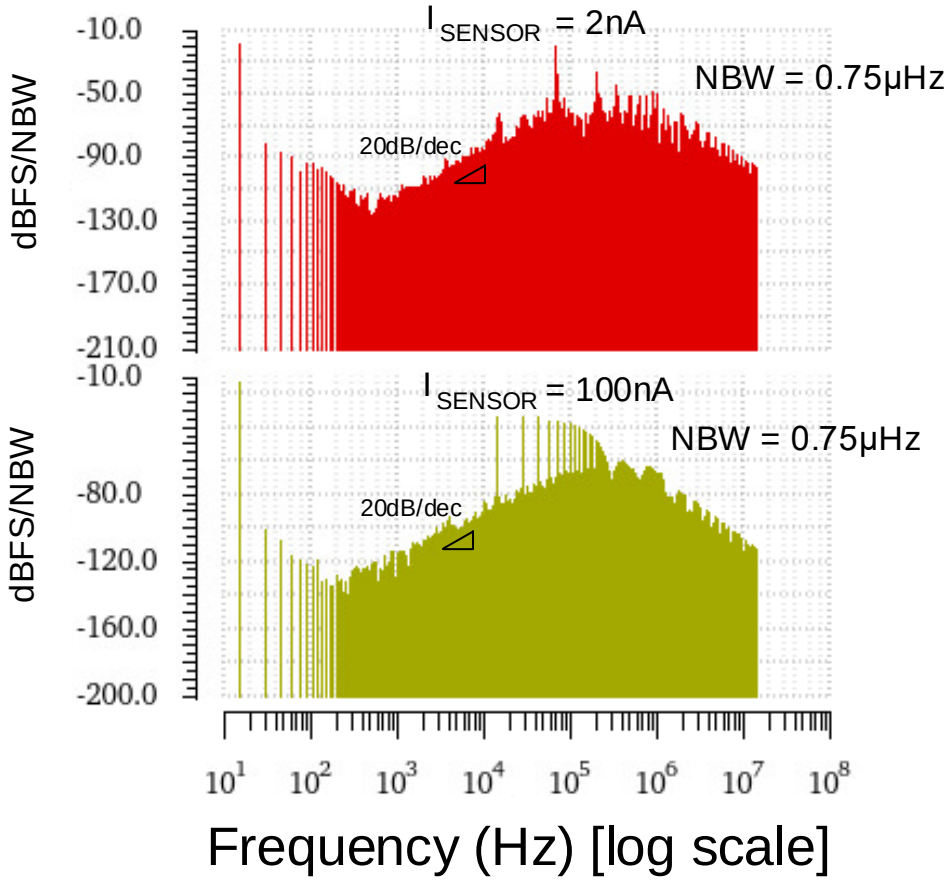


Figure 4.18: ADC output spectrum for input glucose current of 2 nA and 100 nA.

The circuit noise of the entire system will also degrade the overall system SNR. The noise sources which contribute to the overall circuit noise include the potentiostat control amplifier, the reset switch across the integrator, the dynamic switching transients of the 1-bit DAC, and the comparator circuit noise. Unfortunately, due to long simulation time required to simulate many samples, it is not possible to simulate the entire noise of the ADC at $F_{SAMPLE} = 15.26$ Hz. However, it is possible to simulate the noise of the circuitry at higher F_{SAMPLE} (thus lower OSR). Figure 4.19 shows the complete noise spectrum for

the entire IADC accounting for all sources of noise and non-linearity and includes the delta-sigma feedback connection with $F_{SAMPLE} = 5$ kHz ($OSR = 100$) (simulated using Spectre RF PSS and PNOISE). The PSD shows nulls at all harmonics of F_{SAMPLE}, which matches the expected output spectrum from Figure 4.10. However, the output voltage PSD shape does not match Figure 4.10 because the additional non-linearities simulated. The output noise PSD was measured at the integrator output so that it can easily be referred to the input of the ADC. The input referred noise of the ADC is found to be 3.06 LSB, where the dominant contributors are the thermal noise currents generated by the input stage of the control amplifier. The increased noise is expected due to eqn. 4.12 since the simulated $F_{SAMPLE} = \frac{1}{T_{INT}}$ is 327x higher than the real F_{SAMPLE} simulated previously. Thus it is expected that the circuit noise of the IADC will be acceptable given the correct F_{SAMPLE}.

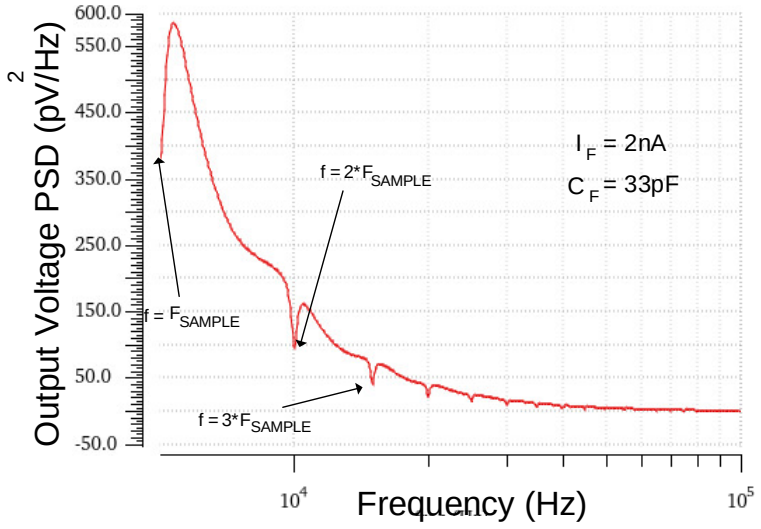


Figure 4.19: Simulated ADC noise PSD at the output of the integrator with $F_{SAMPLE} = 5$ kHz, $I_F = 2$ nA, and $C_F = 33$ pF.

The overall ADC and sensor power consumption is tabulated in Table 4.4. It is clear that the design meets the power targets initially specified based on energy analysis. Thus, the complete design of a glucose potentiostat and associated sensor readout circuitry has been presented.

Table 4.4: Overall Sensor Power Consumption.

Block	Supply	Power Consumption (TT)
Potentiostat + Bias	$AVDD_{SENSOR}$	268 nW
Gain Boost Amplifier + Bias	$AVDD_{ADC}$	2.2156 μW
Integrator + Comparator + Bias	$AVDD_{ADC}$	2.27 μW
Digital	$DVDD_{ADC}$	0.55 μW
Supply	Target	Total Simulated
$AVDD_{SENSOR}$	300 nW	268 nW
$AVDD_{ADC}$ + $DVDD_{ADC}$	6 μW	4.775 μW

Chapter 5

Experimental Results

To reduce circuit design risk, the Bluetooth TX and sensor circuitry were implemented incrementally in three separate test chips. The goal was to leverage testing of earlier designs to improve the performance of subsequent tapeouts. However, due to unforeseen significant delays with the fabrication facility, the first test chip (Chip 1) was received after the final test chip (Chip 3) was already taped out. Chip 1 focused on the design of the RF TX and included the VCO, divider, and PFD. This prototype was taped out on a digital variant of the aforementioned RF technology mentioned in this thesis. The second test chip (Chip 2) completed the entire design of the potentiostat and sensor readout circuitry on the RF process. Finally, a third test chip (Chip 3) was fabricated which completed the RF TX modulator and included the previously designed sensor circuitry. The remainder of this chapter focuses on the layout, testing, and experimental results resulting from each test chip.

5.1 Partial Bluetooth TX (Chip 1)

Figure 5.1 highlights the circuitry designed on the first tapeout. Chip 1 includes the VCO, frequency dividers and PFD discussed in Chapter 3. The design also includes an initial design of the PA shown in Figure 5.2, however, this was changed to the design referenced in Chapter 3 and fabricated in Chip 3. The PA design used in Chip 1 suffers from worse output power and efficiency compared to Figure 3.22. The simulation results shown in Chapter 3 were completed on a changed RF process that was used for Chip 2 and Chip 3, and thus the simulation results do not completely reflect the performance of the design on Chip 1.

The inputs to Chip 1 include a 1 MHz reference clock, two VCO control voltages (PLL and modulation paths), a digital reset signal, and a serial interface to program on-chip registers. The outputs include the RF output, two divided clocks (divide-by-8to10 and divide-by-16to20), and up/down pulses from the PFD. Finally, the supply system for this tapeout included an analog and digital supplies (0.5 V) and grounds for noise isolation and to be able to measure dc power consumption separately.

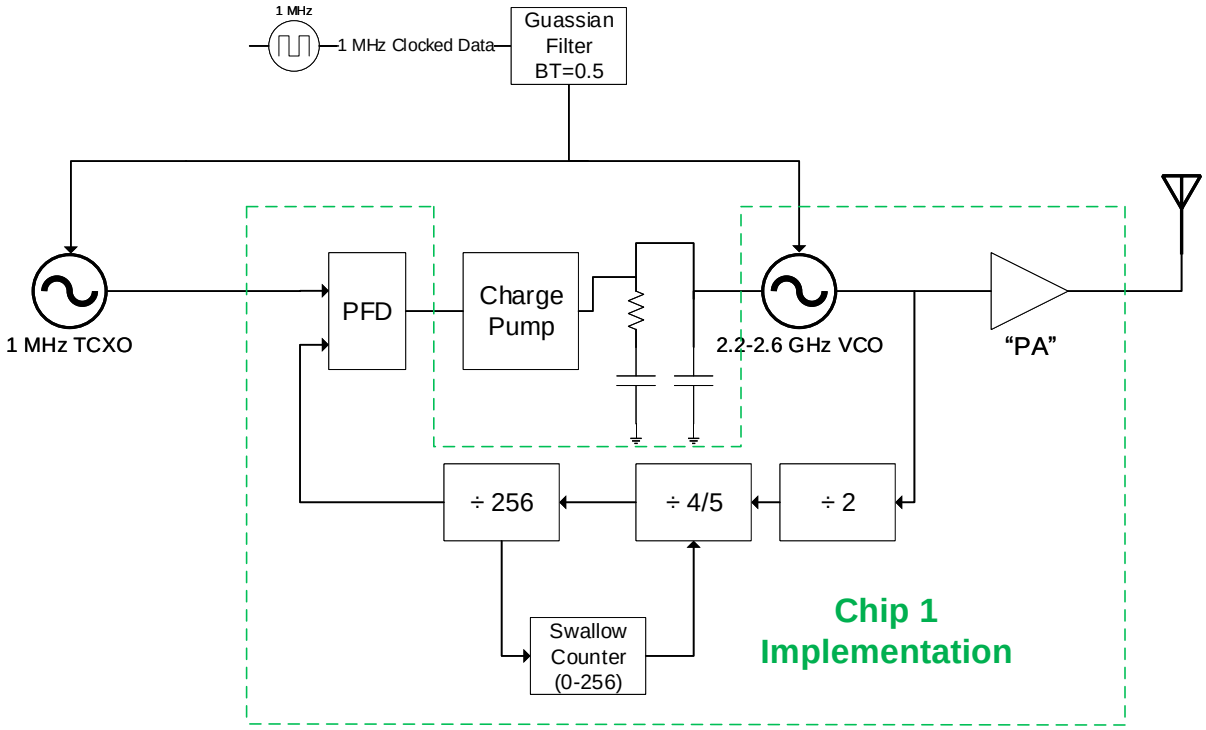


Figure 5.1: Architecture of Chip 1.

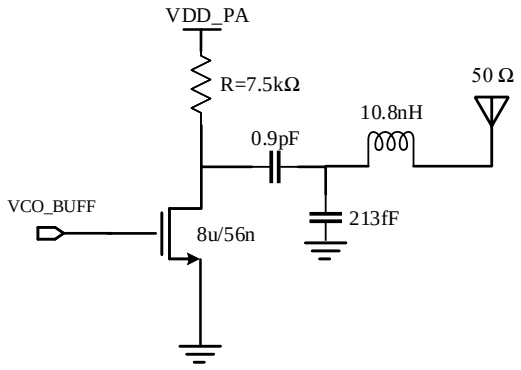


Figure 5.2: Initial PA design used in Chip 1.

5.1.1 Chip 1 Layout and Fabricated Device

Figure 5.3 shows the overall layout of Chip 1. As mentioned previously, this tapeout was completed on a discontinued variant of the RF 45nm technology of which the subsequent chips and simulation data is based on. As a result, RF passives used in the design such as inductors have a lower peak-Q and SRF than in the final design. The same inductor was used in both the VCO and PA and was provided by the design kit. This choice was made in order to reduce design risk, since the inductor models claimed to be correlated to silicon measurement data. However, one issue with the inductor layout is that no metal fill keep-out was put around them. This may cause some performance degradation of the inductors as the inductor could form additional parasitic capacitance to ground which would lower the SRF and peak-Q.

For the VCO, the components were kept in close proximity to reduce parasitics. The cross-coupled negative conductance pairs were interdigitated to reduce mismatch between them. Furthermore, all routing was done on higher metal layers where possible, to reduce parasitic capacitance to the substrate. Despite the thicker and wider wires used in the higher metals, the majority of interconnect capacitance is formed by fringing electric fields, rather than parallel plate capacitance. Thus, the distance from the substrate is more crucial than the width of the trace.

Separate analog and digital supplies were used to reduce crosstalk between digital circuitry and sensitive RF blocks. These supplies were distributed via a mesh rather than star connection in order to reduce supply inductance.

The overall size of the chip is 1.225 mm x 0.975 mm, with 28 pads. However, only 20 pads will be wirebonded to a test PCB, as the other 8 will be probed directly with an RF probe for RF measurements.

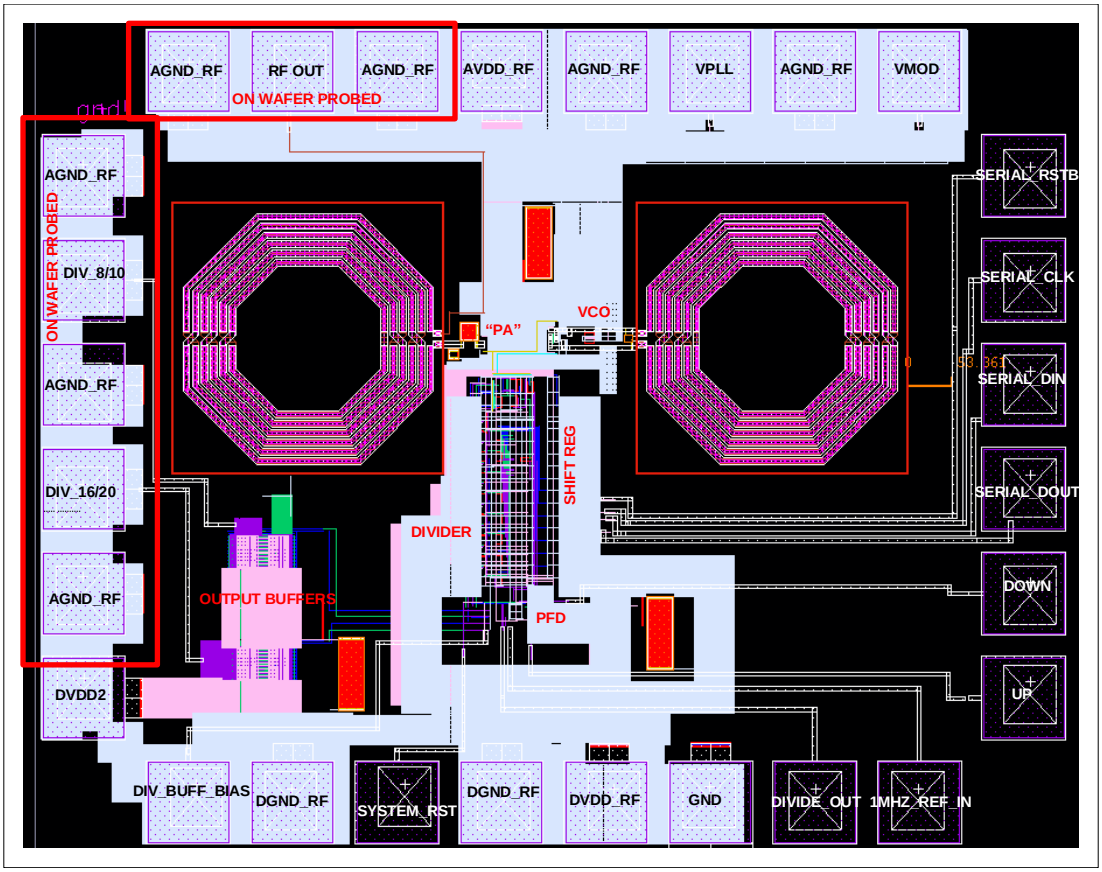


Figure 5.3: Layout of Chip 1

Figure 5.4 shows a photo of the chip die including ball-bonds. The pads on the left that do not have a ball-bond are clear so that they may be probed directly with a ground-signal-ground (GSG) RF probe.

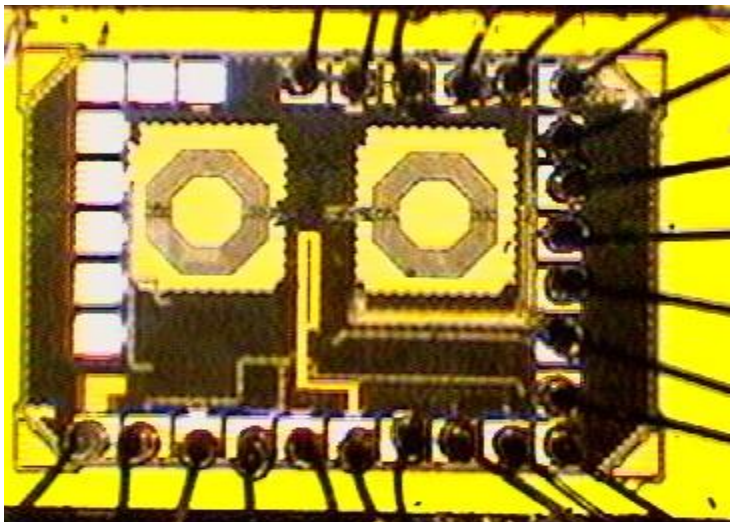


Figure 5.4: Die-photo of Chip 1

5.1.2 Chip 1 Test PCB

The remainder of the chip is wirebonded directly to the test PCB shown in Figure 5.5. The PCB includes supply decoupling, an on-board 1 MHz reference oscillator, an ardiuno interface for register programming (detailed in Appendix D), level shifting circuitry for digital inputs and outputs, and an on-board loop-filter and PFD+CP circuitry to be used to complete the PLL feedback loop.

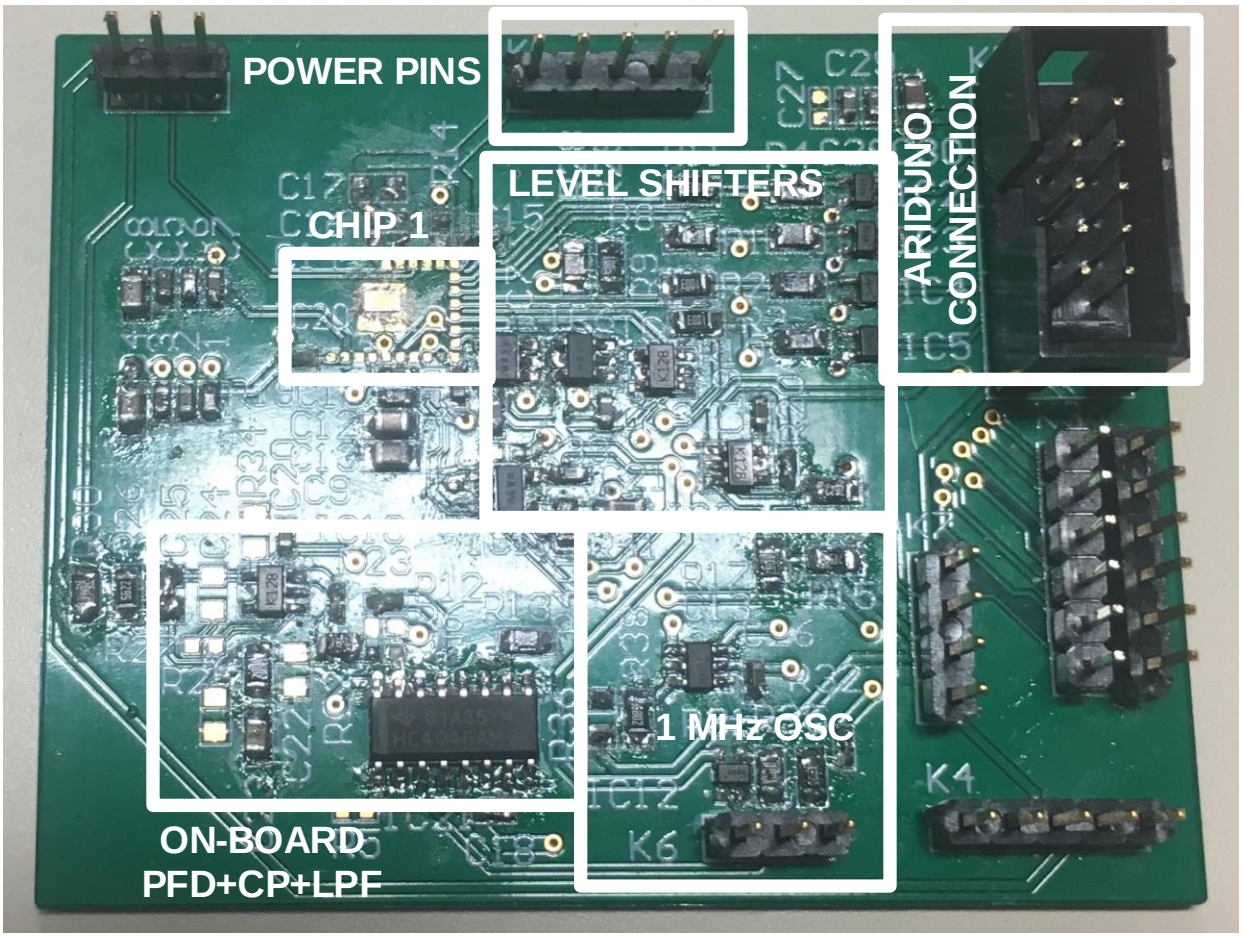


Figure 5.5: Test PCB for Chip 1.

5.1.3 Measurement Results

Given that this test chip taped out an incomplete PLL, the main purpose of this tapeout is to characterize the performance of the VCO and divider.

VCO and PA Measurements

Figure 5.6 shows the oscillation frequency F_{osc} plotted against the tuning voltage V_{PLL} at the minimum PVT code (which corresponds to the highest frequency) and maximum PVT code.

Due to an apparent hold-time violation of the flip-flops used in the configuration shift register, only minimum and maximum PVT settings could be tested. Despite simulations across corners showing adequate hold-margin, along with additional load capacitance inserted between flops, all chips measured seemed to exhibit hold-time violations. This problem caused the shift register to be programmed as all zero's or one's. The shift register mapping is shown in Appendix B, Table B.2. However, the chip was not rendered completely useless, since the shift register mainly controlled the capacitance PVT bank as well as the divider values. Thus the chip was tested with PVT code 0/7 and divider code 0/256.

Measurement results show that the LC VCO oscillates at a much lower frequency than simulated. The oscillation frequency barely reaches 2.45 GHz at the end of the control voltage range, instead of in the middle of the frequency range. This could be caused by a number of factors. For example, the simulation did not include metal fill, which could have increased the parasitic capacitance at the oscillation node. The inductor models used to simulate the inductor performance could also be inaccurate given that the process used in Chip 1 is not optimized for RF design. Typically, LC VCOs centre frequency tend to be slightly off in frequency range, and their designs need to be tuned after silicon measurements. However, given that Chip 1 was received after Chip 3 had already been taped out, these silicon results did not result in design changes. Despite mismatched center frequency, the overall tuning range and frequency gain closely matches simulation as shown in Figure 5.7.

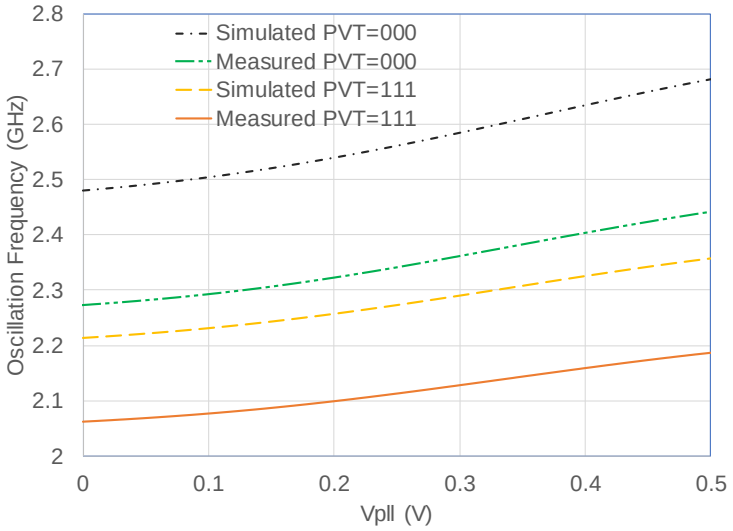


Figure 5.6: Oscillation Frequency vs. V_{PLL} at fastest (PVT=000) and slowest (PVT=111) settings.

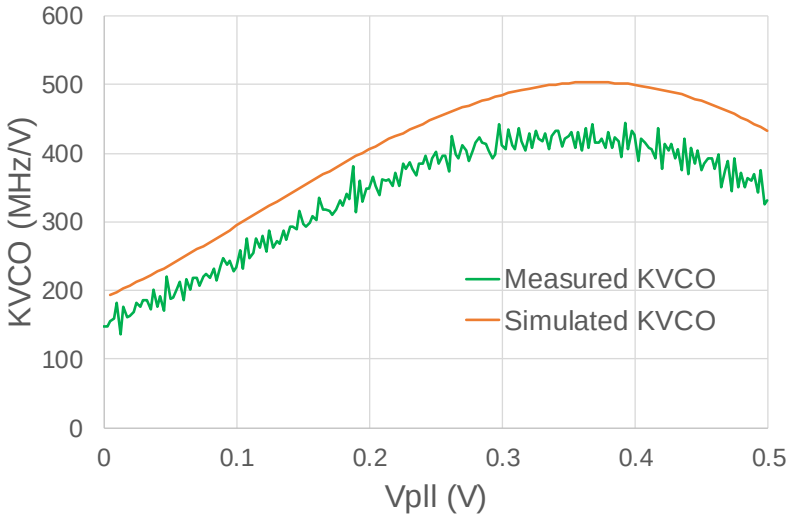


Figure 5.7: K_{VCO} vs. V_{PLL} at fastest PVT setting (PVT = 000).

The output power of the oscillator was also measured across V_{PLL} and shown to be approximately -37 dBm @ 2.4 GHz as shown in Figure 5.8. This is much lower than -20dBm required to meet Bluetooth specifications, however, the PA design in Chip 1 targeted an output power of -40 dBm. Since the power supply of the PA is coupled to the oscillator power, the PA efficiency cannot be measured directly.

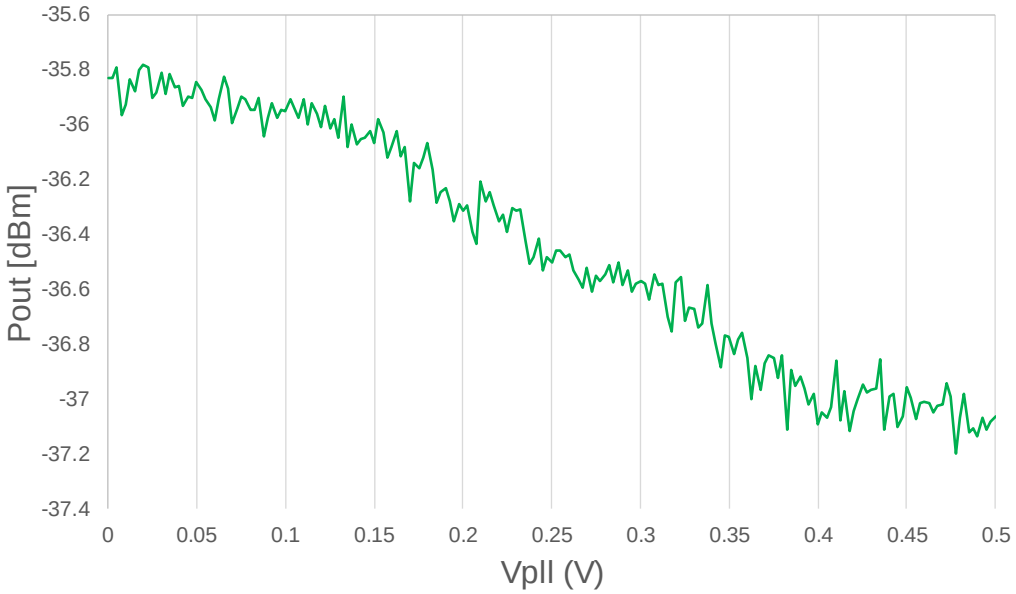


Figure 5.8: P_{OUT} vs. V_{PLL} at fastest PVT setting.

Another key measurement of the VCO is the phase noise. Figure 5.9 plots the measured phase noise results across offset frequency from 2.44 GHz. The phase noise at 1 MHz offset is measured at -108.5 dBc/Hz, which is well below the required phase noise of -92.5 dBc/Hz at 1.5 MHz offset.

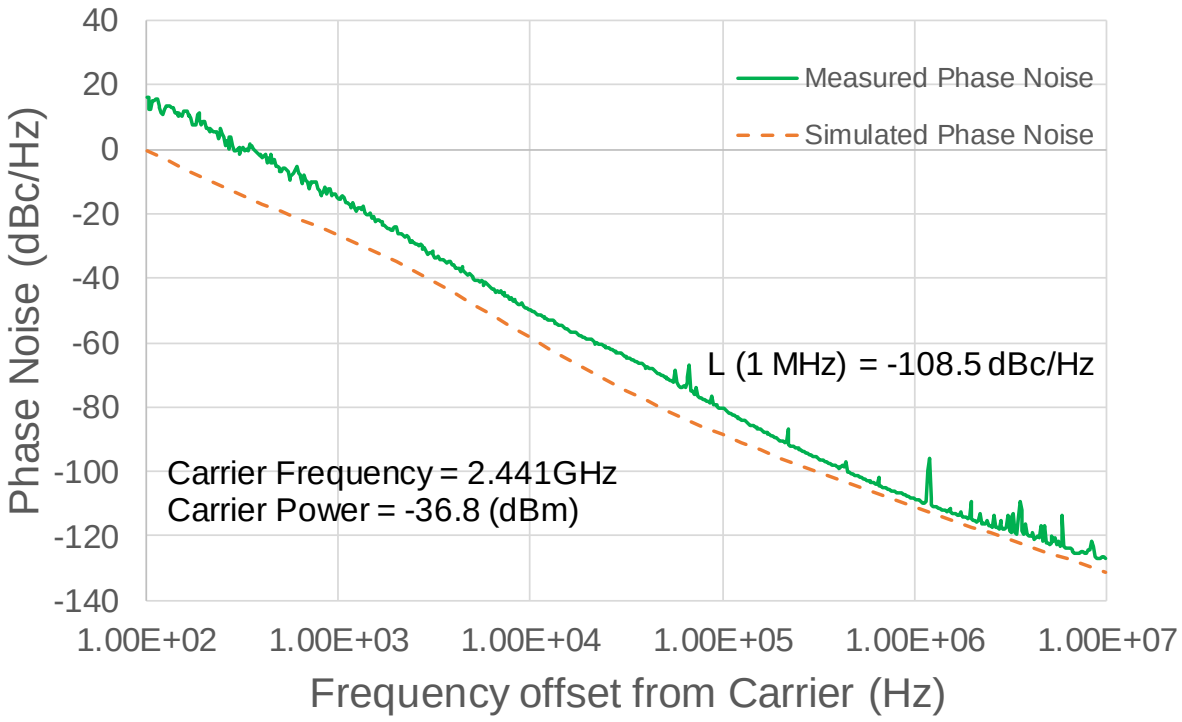


Figure 5.9: Phase-noise vs. F_{OFFSET} at 2.45 GHz at PVT=000 and $V_{PLL} = 0.5V$.

The Bluetooth modulator must be able to shift the output frequency by 500 kHz to generate an MSK signal. Figure 5.10 measures oscillation frequency F_{osc} against the modulation voltage V_{MOD}. The measured voltage input voltage for 500 kHz output frequency change is 0.178 V. This is much lower than the simulated voltage range of 0.2 V - 0.5 V and implies higher than expected VCO modulation gain. These results show that calibration loops are likely necessary to ensure the input modulation voltage is scaled appropriately, since the oscillator gain $K_{VCO,mod}$ is not a well controlled parameter.

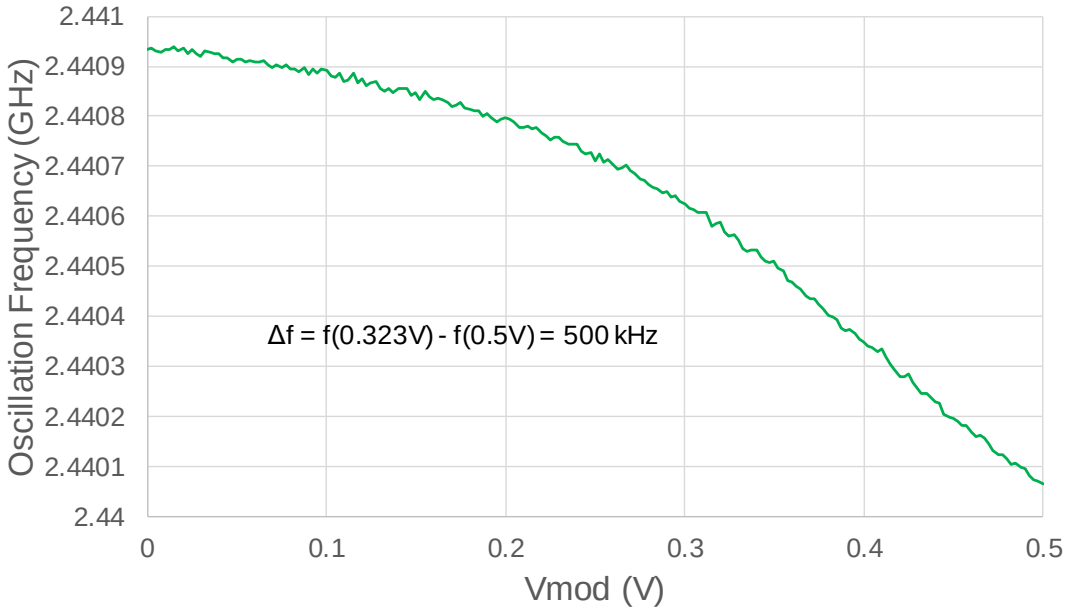


Figure 5.10: Oscillation frequency vs. V_{mod} at 2.45 GHz at PVT=000 and $V_{PLL} = 0.5\ V$.

Figure 5.11 measures the output spectrum of the modulator with the VCO modulated by a 1 Mbps alternating binary sequence with 500 kHz frequency spacing. The output spectrum shows the input spectrum shifted by the VCO carrier frequency. This result simply shows the functionality of the modulation path. However, the output spectrum of random data would not appear simply as harmonics since the input spectrum follows a sinc function.

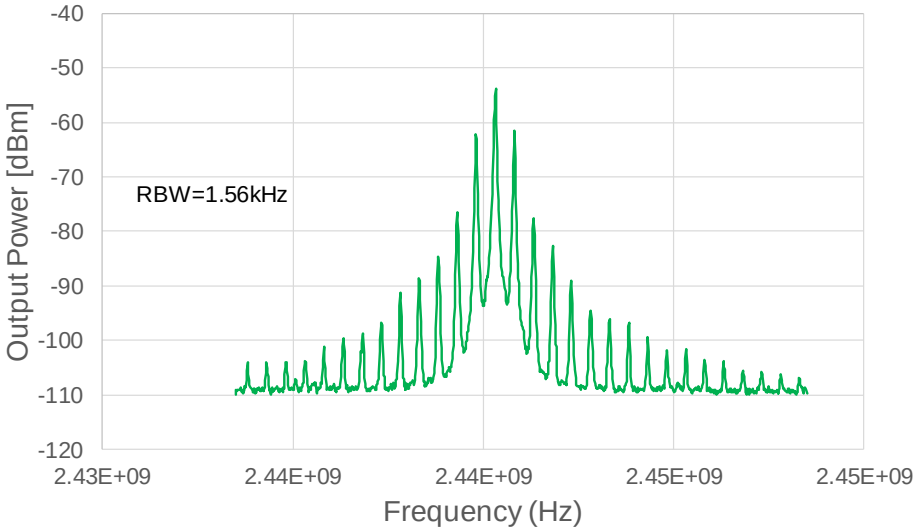


Figure 5.11: MSK Output Spectrum with $V_{mod} = 500$ kHz sine wave @ $K_{mod} = 1$ MHz/V.

The complete power consumption is measured as 200μW including divider power. This matches the simulated power consumption of 175.6 μW. The oscillator FOM was measured to be 183.44 dB, which is near the simulated value of 185.76 dB. Hence, these results are promising as they provide an upper bound to what is expected from Chip 3 due to improved inductor Q available in the RF process.

Overall, aside from the centre frequency shift, VCO measured performance is reasonably close to simulated performance. The performance characteristics are sufficient to meet Bluetooth requirements except for the output power specification (addressed in Chip 3), and the power consumption is within the allowable budget.

Divider Measurements

The divider division accuracy was measured by setting the divider to its maximum value (divide by 2560). Then, the the following outputs were measured: divide-by-10, divide-by-20 and divide-by-2560. The oscillation frequency measurements from the spectrum analyser for divide-by-10 and divide-by-20 are shown in Figure 5.12 and Figure 5.13 respectively. It is clear the divider is functioning correctly.

The divider phase noise performance was also measured in Figure 5.14. The phase noise is expected to improve by:

$$\begin{aligned} PN_{OSC} - PN_{DIV} &= 20log_{10}(N) \text{ [correlated noise region]} \\ PN_{OSC} - PN_{DIV} &= 10log_{10}(N) \text{ [uncorrelated noise region]} \end{aligned} \tag{5.1}$$

At low frequency offset, flicker and thermal noise both contribute to the phase noise, and thus the phase noise of the dividers should be improved by 20 dB and 26 dB, respectively. This is true at low frequencies, however, as we transition past the flicker noise corner, the improvement degrades as expected. At 1 MHz offset, the phase noise improvement is 15.7 dB and 22.3 dB, respectively. The noise spikes that are seen at higher frequencies are likely measurement environment induced noise. This is evidenced by the oscillator phase noise measurement shown in Figure 5.9 which does not have these spikes.

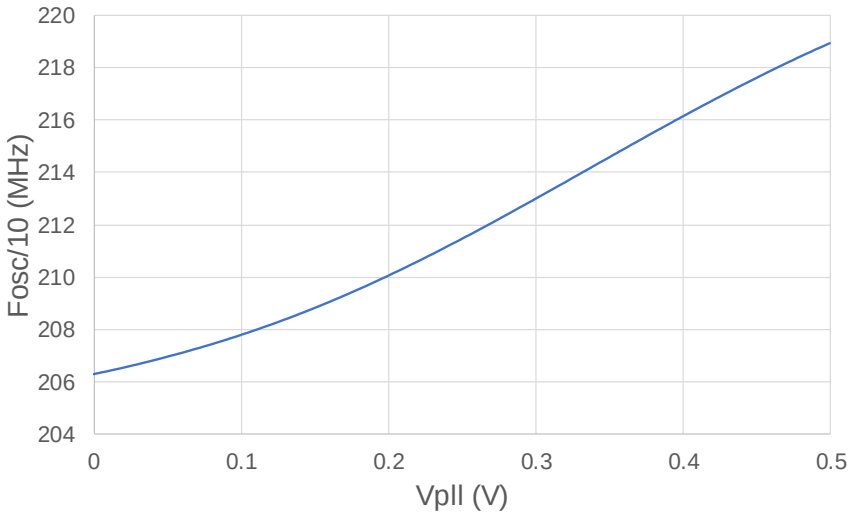


Figure 5.12: Divide-by-10 Frequency vs. V_{PLL} at slowest PVT setting [PVT=111].

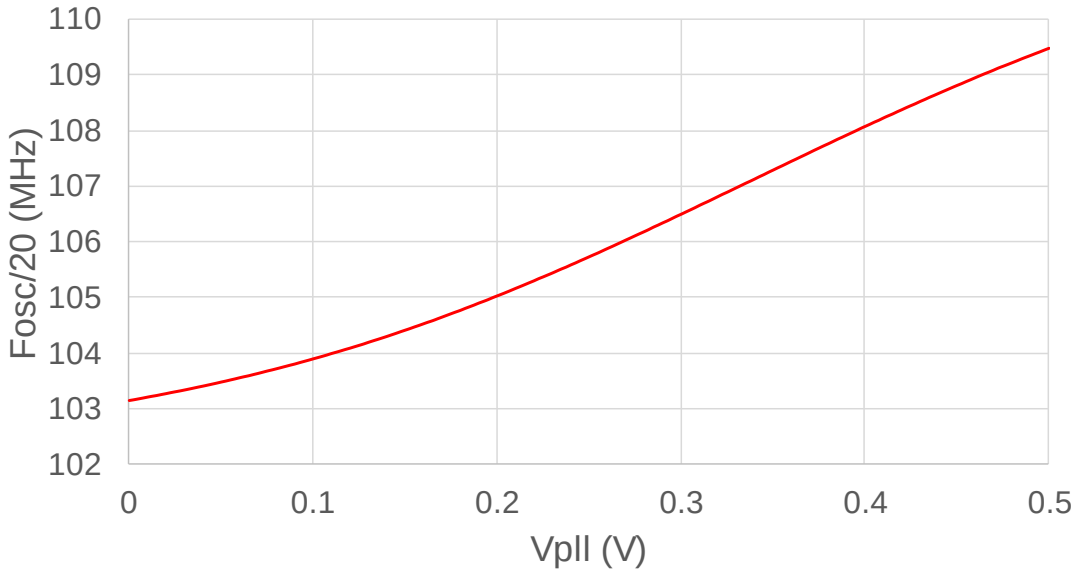


Figure 5.13: Divide-by-20 Frequency vs. V_{PLL} at slowest PVT setting [PVT=111].

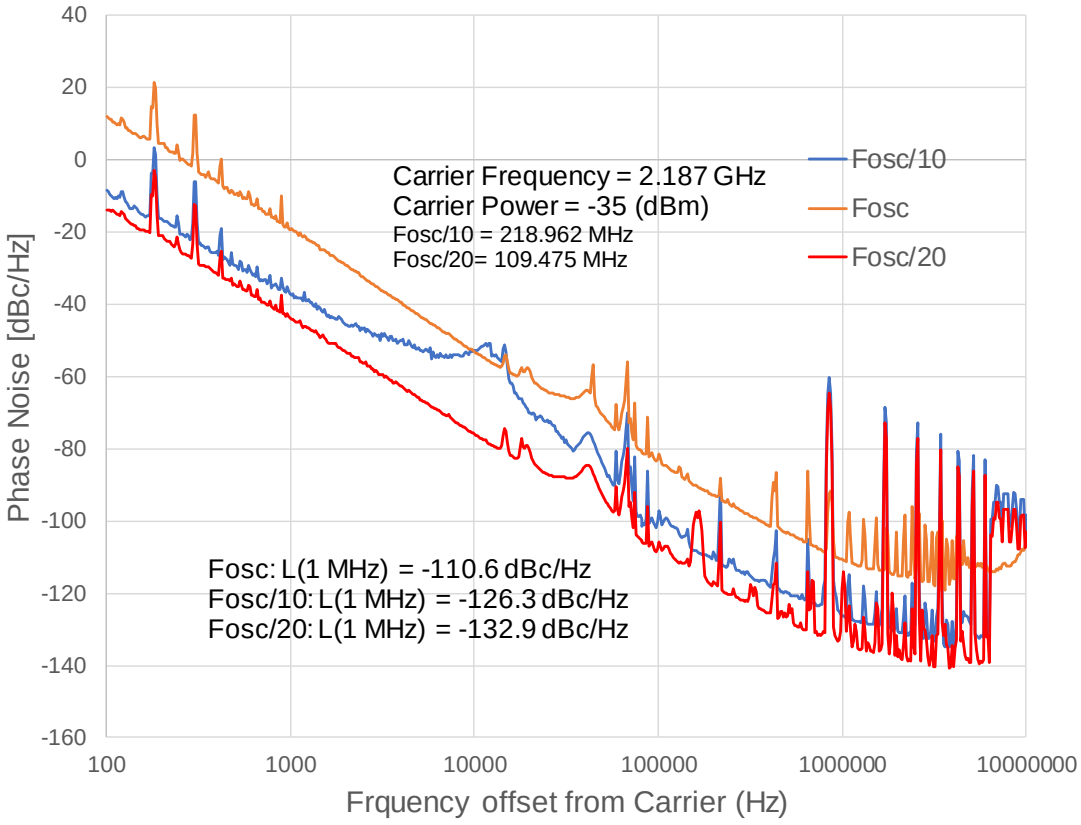


Figure 5.14: Phase-noise vs. F_{OFFSET} for carrier and divided outputs where $F_{OSC} = 2.187$ GHz.

PFD and PLL Measurements

Another design bug discovered after tapeout was limited output buffering for digital outputs from the chip. The output buffers were not sized to drive large PCB load capacitances, which caused issues when viewing the output of the UP/DOWN pulses, since the bandwidth of these pulses changed depending on the phase/frequency difference of the reference and the feedback clock. This caused the test-plan scope to be reduced as it was not possible to measure the PFD performance.

Furthermore, additional PLL measurements were not completed since the data would

not be useful given that PFD, CP and LPF would not match the circuit built for Chip 3. Thus, the performance characteristics of the partial PLL would not accurately map to the performance of the PLL in Chip 3.

In conclusion, the measurement results show that, despite some design errors, the key VCO and divider performance characteristics match simulation while meeting target power consumption targets as shown in Table 5.1. The oscillation frequency can easily be recentered with some additional tweaking. Furthermore, the results show that the PLL power consumption can be further reduced by lowering the oscillation supply voltage, as the oscillator is able to oscillate at a supply voltage below 0.5 V. Given that Chip 3 includes higher-Q RF passives (inductors, varactors), Chip 3 may be able to oscillate with even lower supply voltages than Chip 1, saving additional power.

Table 5.1: Simulation compared with experimental results with $V_{PLL} = 0.5\,V$, $PVT = 000$.

Specification	Simulated @ 0.5 V	Measured @ 0.5 V	Measured @ 0.46 V
F_{osc}	2.6425 GHz	2.441 GHz	2.4528 GHz
Tuning Range	193.2 MHz	169 MHz	177 MHz
K_{VCO}	400 MHz/V	325.64 MHz/V	491 MHz/V
P_{OUT}	-31.94 dBm	-35.8 dBm	-39.9 dBm
$L(1MHz)$	-110.6 dBc/Hz	-108.5 dBc/Hz	-
P_{DC} (including divider+PA)	175.6μW	204.8 μW	134 μW
Oscillator FoM (including PA)	185.76	183.44	-

5.2 Potentiostat and Readout Circuit (Chip 2)

The entirety of the potentiostat and sensor circuitry designed in Chapter 4 was taped out on Chip 2. Figure 5.15 shows the complete circuitry fabricated on Chip 2. The main circuit sub-blocks implemented are: a potentiostat, a gain-boosted current mirror, and a 1st order incremental delta-sigma ADC.

The glucose sensor connects to the chip via the WE, CE and RE. Other inputs to the chip include supply and bias currents. Furthermore, the inputs to the digital serial register to add chip programmability were added. Another input to the chip is a 1 MHz reference clock, which would ideally be shared with the RF circuitry. Finally, a test input directly into the delta-sigma was added to test the delta-sigma directly. Outputs from the chip include the ADC modulator output, the ADC digital output serial interface and additional

test outputs from the integrator and a replica integrator. A majority of these inputs and outputs exist for test-ability purposes only, and would be removed on a commercial tapeout so that the chip can be placed on a contact-lens.

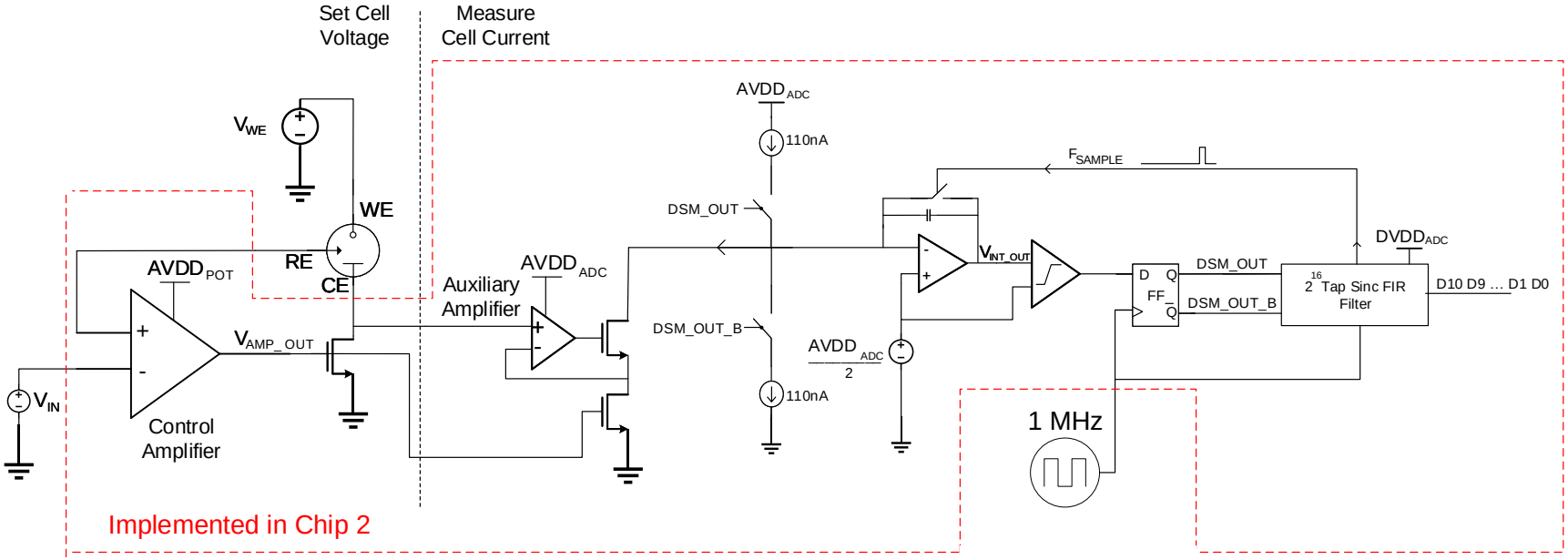


Figure 5.15: Architecture of Chip 2

5.2.1 Chip 2 Layout and Fabricated Device

Figure 5.16 shows the complete layout of Chip 2. The overall size of the chip is 0.92 mm x 0.93 mm, with 32 pads. However, the chip area is pad-limited, and thus the active area is much smaller. Standard analog layout techniques were applied to ensure that schematic performance would translate to layout including:

- Common centroid layout on transistor layouts where possible.
- Inter-digitated differential pairs and current mirrors.
- Ground and supply meshes rather than star connections to reduce their impedances.
- Separate analog and digital supplies and grounds to reduce high $\frac{dI}{dt}$ digital circuitry from coupling into analog circuitry.
- Bypass capacitors with series resistances to ensure good high frequency noise rejection while reducing resonant peaking with supply bondwire inductances.

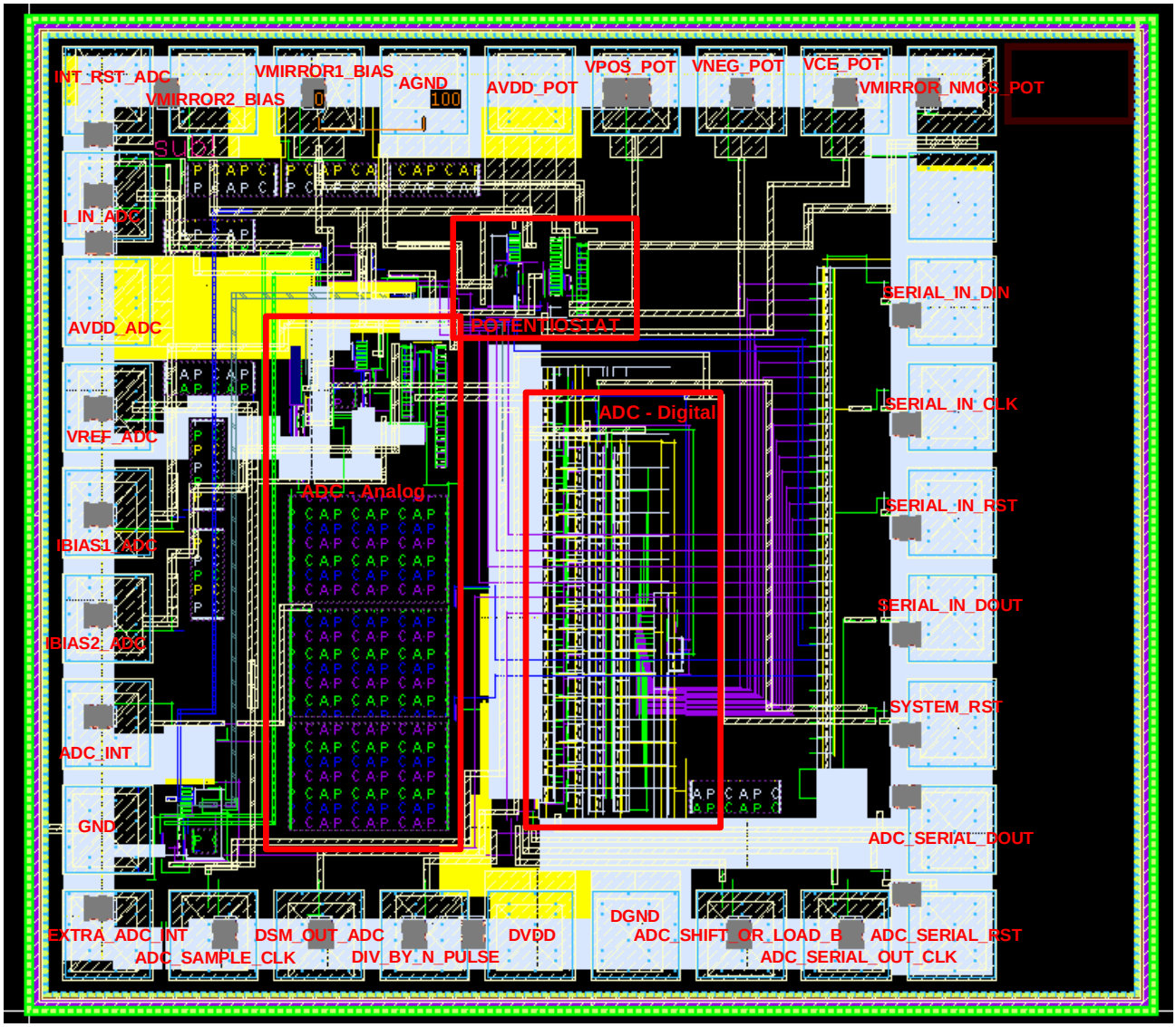


Figure 5.16: Layout of Chip 2.

Figure 5.17 shows a photo of the chip die including ball-bonds. The chip was wirebonded to a LSSP package which connected to a test PCB via a socket.

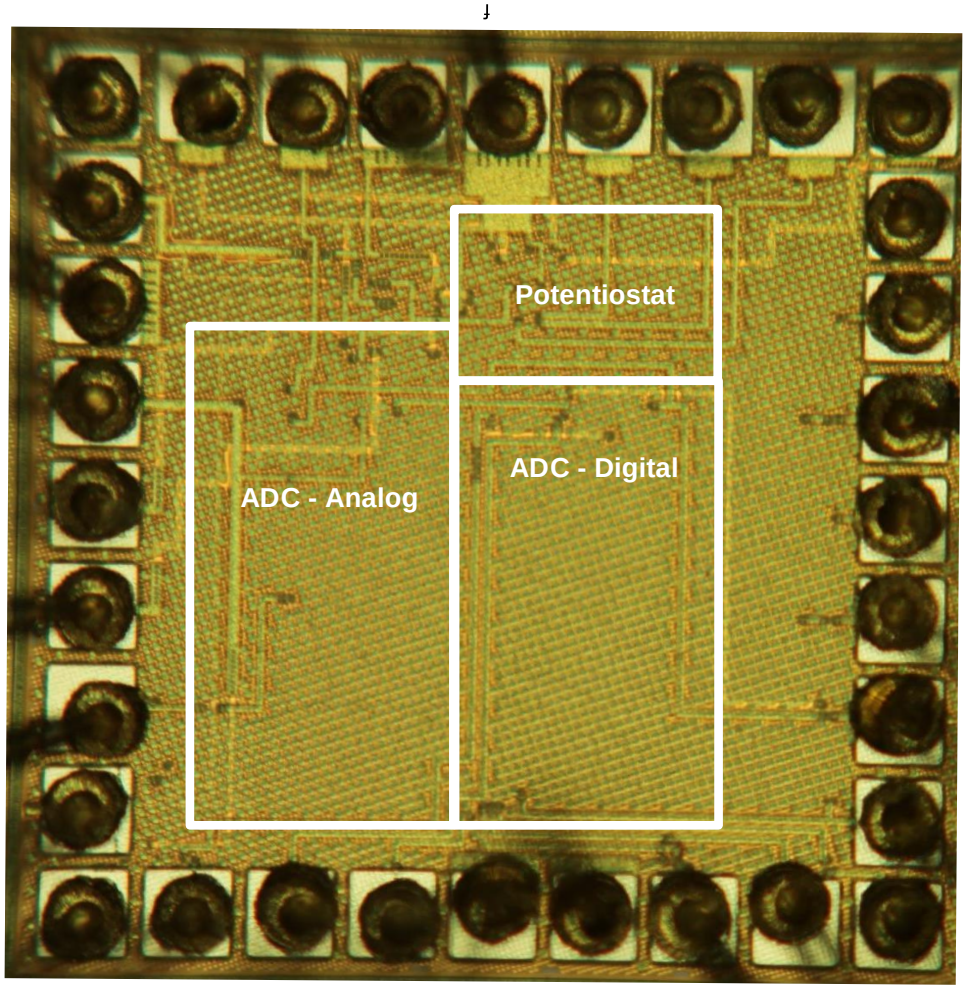


Figure 5.17: Die-photo of Chip 2.

5.2.2 Chip 2 Test PCB

The test PCB fabricated for Chip 2 is shown in Figure 5.18. The PCB includes supply regulators and decoupling, an on-board 1 MHz reference oscillator, an Arduino interface for register programming as well as ADC data streaming (detailed in Appendix D), level shifting circuitry for digital inputs and outputs, an electrical model of the glucose sensor, and variable resistors for bias current programmability.

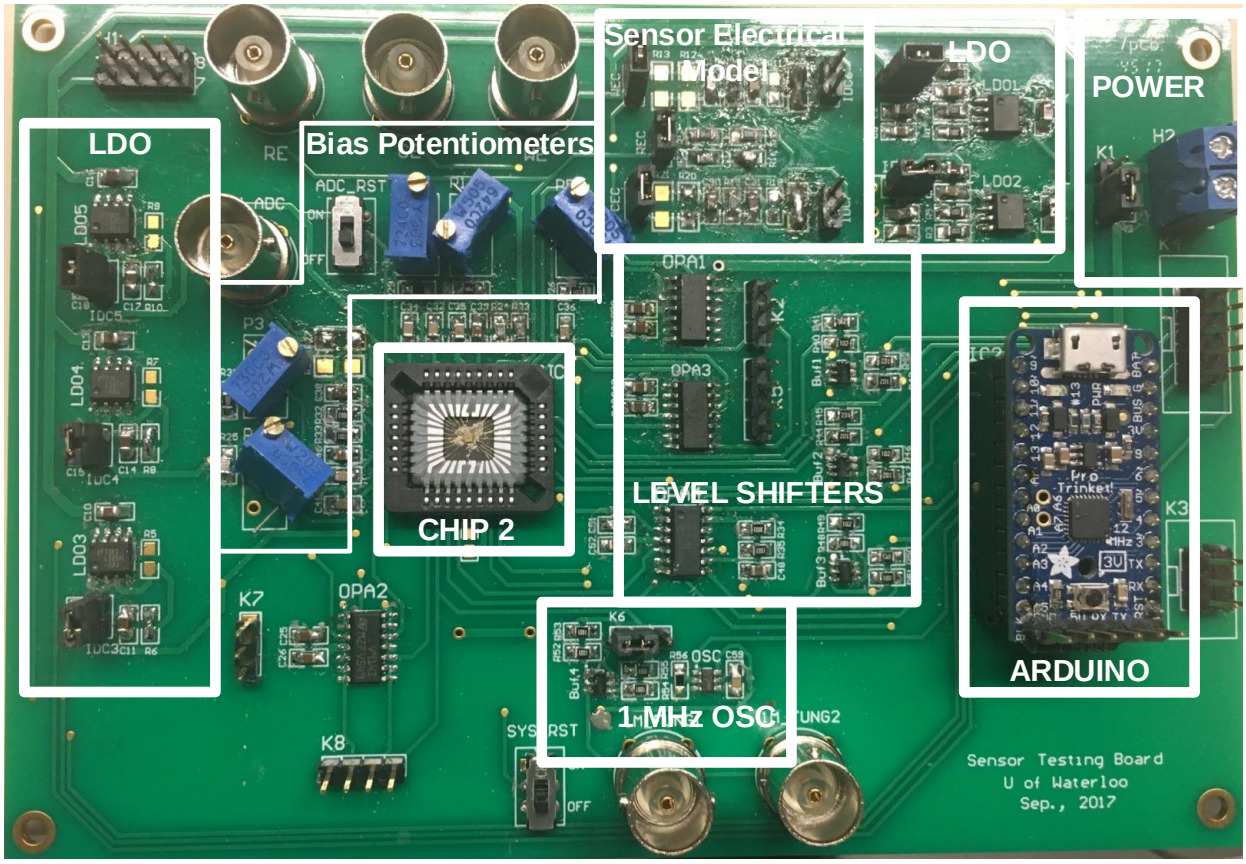


Figure 5.18: Test PCB for Chip 2.

During testing, a source measure unit (SMU) is utilized to provide a pico-ampere accurate current source, to model the sensor current driven into the circuit. To be able to source nano-ampere current accurately, a triax connector with cable shielding is used to reduce the effect of cable capacitance and leakage between the SMU and the WE/CE interface. Figure 5.19 shows how the SMU was configured to be able to act as a floating current source with cable shielding.

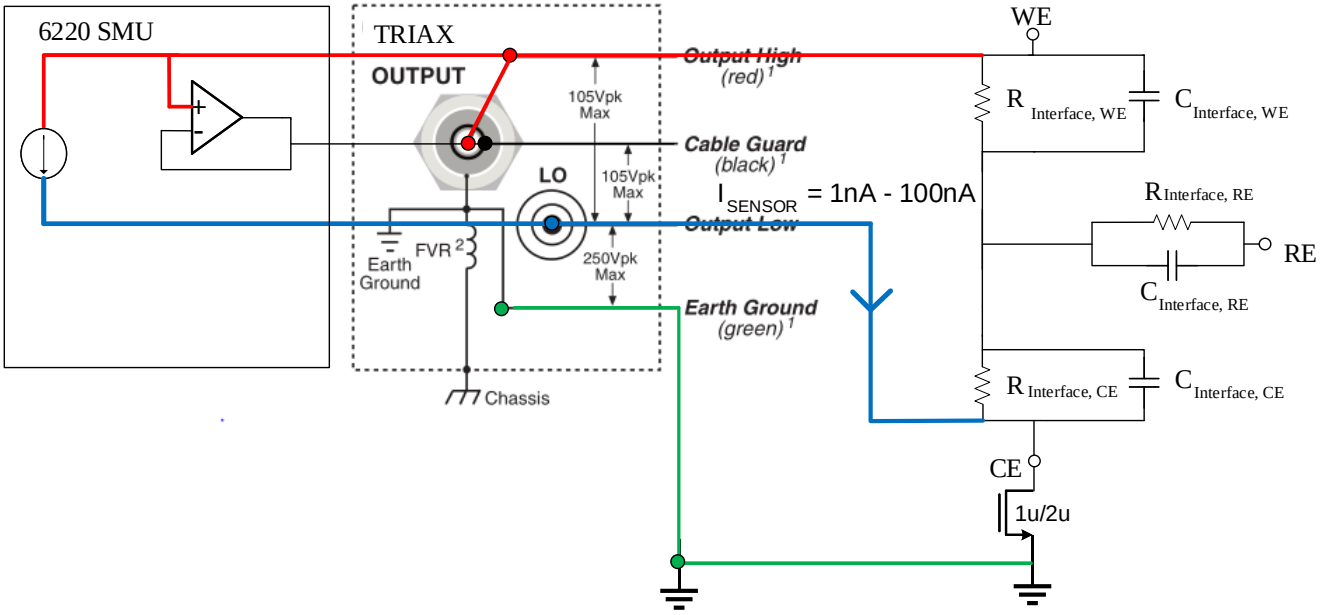


Figure 5.19: SMU connection to the sensor interface on the PCB.

Additional testing instruments include a digital multi-meter for μA current measurements, as well as an oscilloscope for measuring the analog voltage of the various outputs from the PCB and Chip 2. Finally, a computer is used to allow for automated testing and data collection from the various instruments used in measurement. The MATLAB code used to implement the data-processing and instrument control has been included in Appendix E.

5.2.3 Measurement Results

The full system was measured from the potentiostat input to the ADC output. The RE was measured to be regulating to the correct voltage (i.e., 0.323 V based on setting WE = 0.7 V) across I_F and while varying the sensor electrical model parameters by one order of magnitude on each side.

Figure 5.20 shows a scope measurement of the output of the integrator and clocked comparator within the delta sigma for 1nA input. Both waveforms show approximately

50% duty cycle as expected for a low current input. The integrator output exhibits a 1 MHz noise coupling onto the signal.

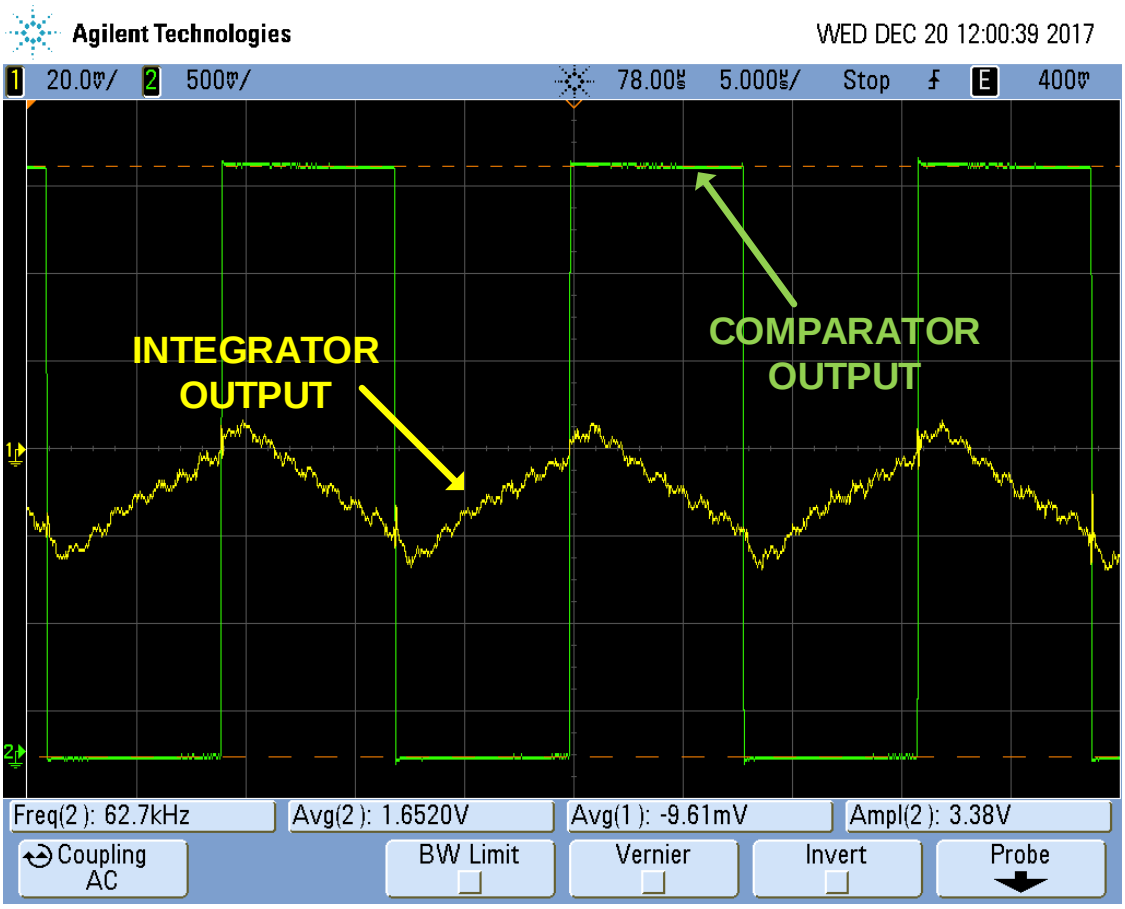


Figure 5.20: Measured Integrator and Clocked Comparator Output with $I_{SENSOR} = 1$nA.

The full system (Potentiostat and ADC) was characterized under two incremental sampling rates: $T_{converter} = 65.54$ ms (the original conservative rate that was used in the analysis in Chapter 4) and $T_{converter} = 16.4$ ms (a faster rate in order to reduce energy consumption). Figure 5.21 shows the potentiostat input current to output ADC code without gain and offset correction where the ADC output was sampled and averaged 50 times per 10 pA input current step. The output code starts near 1024 since the first bit is a sign

bit, and the potentiostat input current is strictly positive. It is clear that the ADC output is relatively linear. Additionally, the slower conversion time has less noisy outputs, which is expected given that the longer conversion time corresponds to a higher OSR. Due to ESD problems encountered during testing, the pad $I_{IN,ADC}$ which allows the ADC to be decoupled from potentiostat was not functioning correctly. As a result, part of the test plan was unable to be implemented.

Additionally, since the converter will only be used for a couple of samples before it is deactivated to save energy, it is pertinent to also measure the output code vs. input current without any sample-to-sample averaging. Figure 5.22 plots the ADC code against the potentiostat input current, plotting the the 4th sample's output. This sets the total ADC enabled time to 200 ms for the slower converter case, which was what was budgeted initially to measure the energy consumption of the overall ADC in Chapter 4. There is an anomalous code at the output of the 4th sample that is present in the 14-bit ADC measurement.

To quantify the static non-linearity of the potentiostat and ADC, differential non-linearity (DNL) and integral non-linearity (INL) was measured. A slow input sensor current ramp was applied to the system, and a histogram of the outputs was measured, with a total of 500000 samples taken from 0 nA to 100 nA. The histogram was then normalized and the DNL was measured in Figure 5.23. The DNL for $T_{converter}$ = 65.54 ms was +/- 0.3 LSB and +0.8/-0.3 LSB for $T_{converter}$ = 16.4 ms. These results show that the ADC is able to meet the required 11-bit static linearity with the longer conversion time only. The INL was measured by integrating the DNL curve and is shown on Figure 5.24 where the max INL for $T_{converter}$ = 65.54 ms was -6.2 LSB and -5.9 LSB for $T_{converter}$ = 16.4 ms. The results show a clear non-linearity across input current. However, INL is tolerable in this application as the non-linearity can be calibrated out. Since these measurements require many seconds of measurement time, it was not possible to compare these results against simulation directly, as the required simulation time is prohibitive.

The ENOB of the ADC (a dynamic measurement) could not be measured because a sine-wave input could not be driven into the potentiostat. However, since the ADC will only be measuring DC current, the *effective resolution* and *noise-free code resolution* can be used to estimate the achieved resolution of the sensor [34]. The *effective resolution* is analogous to SQNR but the noise source is the circuit noise in the system instead of quantization noise. The *noise-free code resolution* represents the number of bits that will not change at all due to circuit noise since it takes into account the peak-to-peak circuit noise (6.6 σ or 99.9% of the noise) instead of the rms noise (1σ or 67%). They are calculated

below:

$$\textit{Effective resolution} = log_2\left(\frac{2^N}{\textit{rms input noise (LSBs)}}\right), \tag{5.2}$$

$$\textit{Noise-free code resolution} = log_2\left(\frac{2^N}{\textit{6.6 rms input noise (LSBs)}}\right) \tag{5.3}$$

where N is the number of bits (11 in this case), and *rms input noise (LSBs)* represents the measured standard deviation of the noise in LSBs. To measure the LSB noise, the standard deviation of the 50 samples taken at each 10 pA input current level was measured and the median was chosen (to remove outliers) which found that the *rms input noise (LSBs)* was 0.82 LSBs (0.107 nA). Thus, the *Effective resolution* is 11.3 bits (above 11 bits because harmonic distortion is not accounted for) and *Noise-free code resolution* is 8.6 bits. These results show that the thermal noise of the system would need to be reduced further to reliably measure to 11-bits within 4 samples, and that the noise is thermal noise limited, not quantization noise limited. To improve the *Noise-free code resolution* to 11 bits, approximately 30 samples would need to be averaged, which is not possible given the energy consumption constraints on the system. However, averaging 4 samples achieves a 1-bit improvement, which may be an option worth exploring, as it would achieve 11-bit resolution at 2σ noise (95% of samples will experience noise $<$ 1 LSB). Another way to improve it would be to use a $sinc^2$ decimation filter, as it would provide more aggressive high frequency filtering.

Using this data, we can also calculate the limit-of-detection LOD of the sensor. The LOD is defined as the minimum signal which allows a signal-to-noise ratio $SNR > 3$. In this case, we can calculate the LOD as

$$LOD = \sqrt{3} \times \textit{rms input noise (LSBs)} = 1.4\ LSB = \frac{1.4}{2^{11}} \times 220\text{ nA} = 0.15\text{ nA}. \tag{5.4}$$

This translates to a minimum glucose concentration of 3.8 μM. Thus the overall sensor range is defined as 0.15 nA – 100 nA.

The final measurement to confirm the delta-sigma functionality of the ADC is shown in Figure 5.25. An FFT of the modulator output is measured similar to the simulation results shown in Figure 4.18. As mentioned previously, the ADC current could only be injected from the sensor. Due to this, only a DC signal could be injected into the input of the ADC. As a result, the FFT waveform shows the input signal in the first few bins (due to $Hann^2$ windowing), and the SINAD cannot easily be extracted from the FFT. However, one can easily see the noise shaping due to the delta-sigma feedback structure.

The power consumption of the various blocks within the signal chain are crucial for measuring the sucess of the design. As mentioned previously in Chapter 4, the gain-boosted amplifier was erroneously connected to $AVDD_{SENSOR}$ instead of $AVDD_{ADC}$, making a direct potentiostat measurement difficult. However, the measurement results vs. simulation results including this mistake are shown in Table 5.2. The total worst case-power consumption is 5.75 μW with all components functioning simultaneously. These measurement results match simulation closely. Thus, the overall potentiostat and ADC chain are shown to meet both power and performance targets specified during the design phase.

Table 5.2: Measured Sensor Power Consumption Compared to Simulation.

Supply	Simulated	Measured
$AVDD_{SENSOR}$ (Includes Gain-boost amplifier)	2.27 μW	2.55 μW
$AVDD_{ADC}$ (Not including Gain-boost amplifier)	2.22 μW	2.25 μW
$DVDD_{ADC}$	0.55 μW	0.95 μW
	Target	Measured
Total	6 μW	5.75 μW

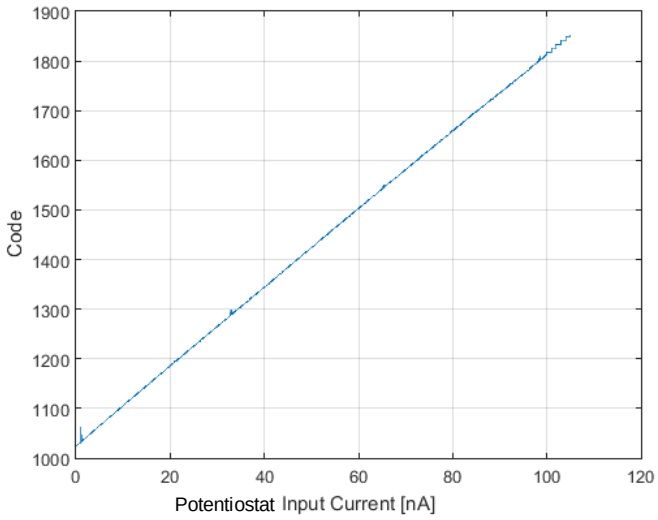
Table 5.3: Measured sensor performance summary.

Specification	Measured with $T_{converter}$ = 65.56 ms
Limit of Detection	0.15 nA
Applied Voltage	0.4 V
Sensor Current Range	0.15 nA – 100 nA
DNL	± 0.3 LSB
INL	- 6.5 LSB
Effective Resolution	11.3 bits
Noise Free Code Resolution	8.6 bits

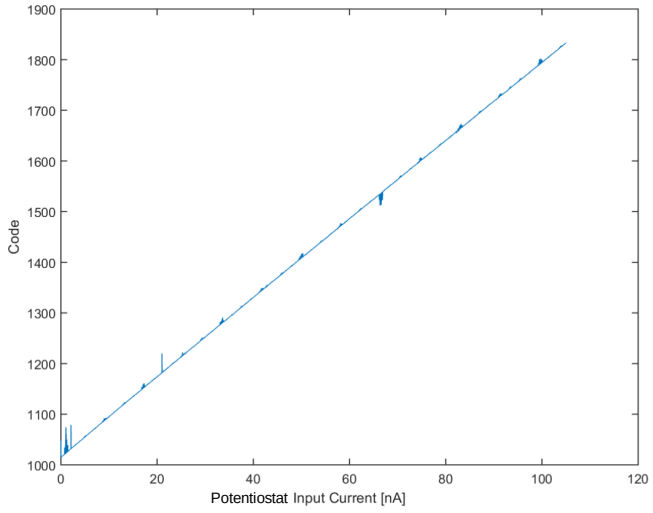
Using the above results, a figure-of-merit (FOM) for the potentiostat is defined in eqn. 5.5 as:

$$\text{FOM}_{\text{POT}} = \frac{(\text{Maximum Current} - \text{LOD})(\text{Applied Potential})}{\text{Potentiostat Power}} = \frac{(100\text{ nA} - 0.15\text{ nA})(0.4\text{ V})}{275\text{ nW}} = 0.145. \tag{5.5}$$

where the potentiostat power is taken from the simulated result since the measurement data does not isolate the potentiostat power on it's own.

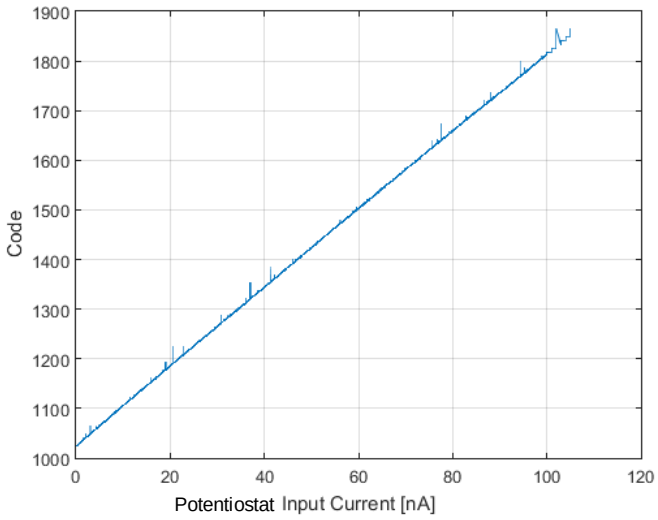


(a) ADC Code vs. Potentiostat Input Current, averaging 50 ADC samples for every 10 pA input current step, $T_{converter} = 65.54$ ms.

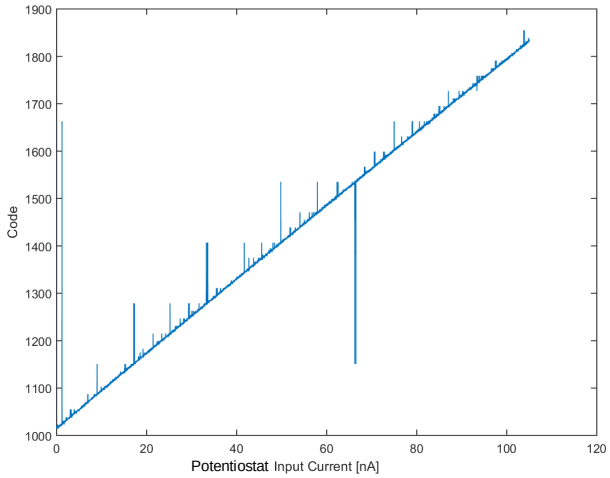


(b) ADC Code vs. Potentiostat Input Current, averaging 50 ADC samples for every 10 pA input current step, $T_{converter} = 16.4$ ms.

Figure 5.21: ADC Code vs. I_F for $T_{converter} = 65.54$ ms and $T_{converter} = 16.4$ ms.

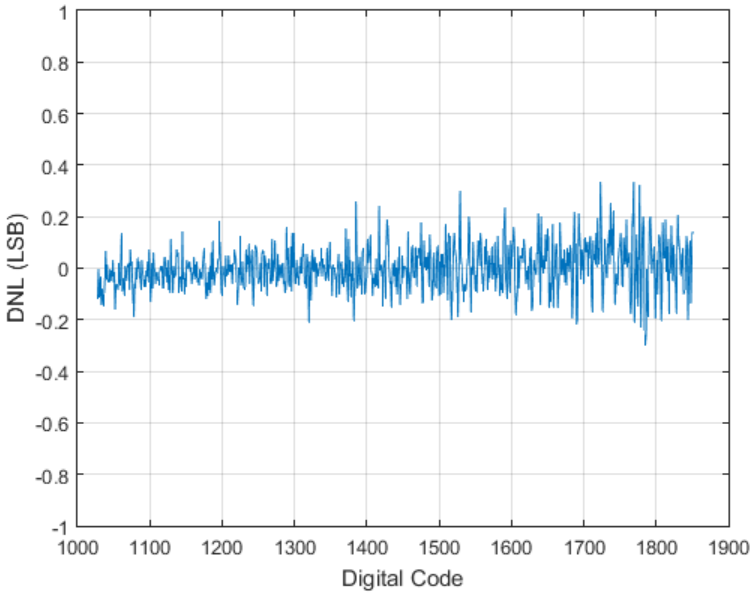


(a) ADC Code vs. Potentiostat Input Current, using the 4th sample, $T_{converter} = 65.54$ ms.

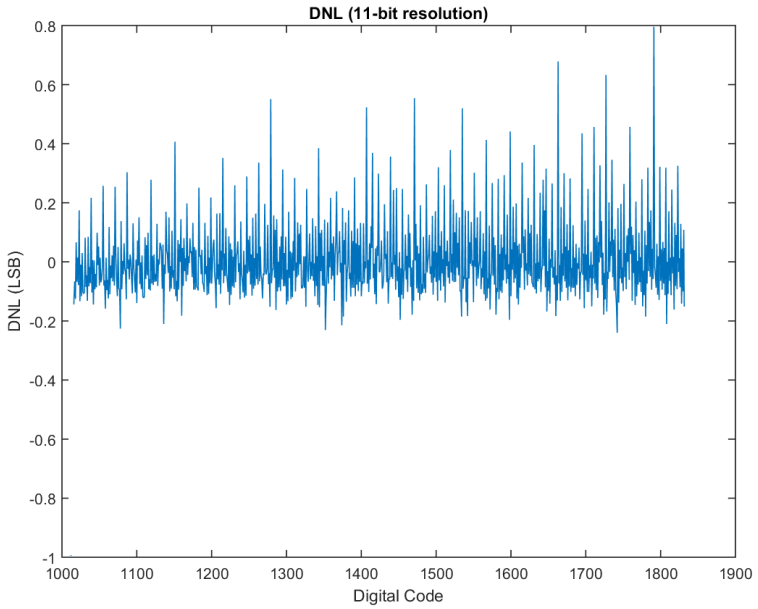


(b) ADC Code vs. Potentiostat Input Current, using the 4th sample, $T_{converter} = 16.4$ ms.

Figure 5.22: ADC Code vs. I_F Transient Output for $T_{converter} = 65.54$ ms and $T_{converter} = 16.4$ ms.

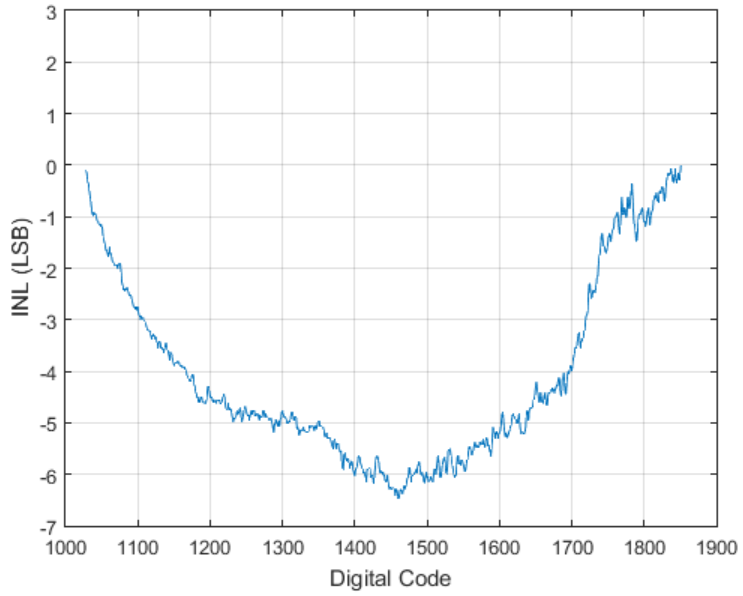


(a) DNL vs. ADC Code, $T_{converter} = 65.54$ ms.

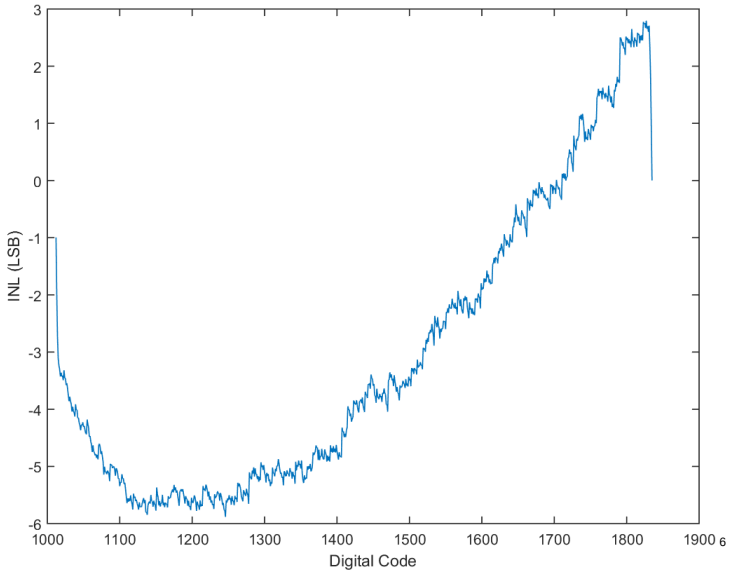


(b) DNL vs. ADC Code, $T_{converter} = 16.4$ ms.

Figure 5.23: DNL for $T_{converter} = 65.54$ ms and $T_{converter} = 16.4$ ms.

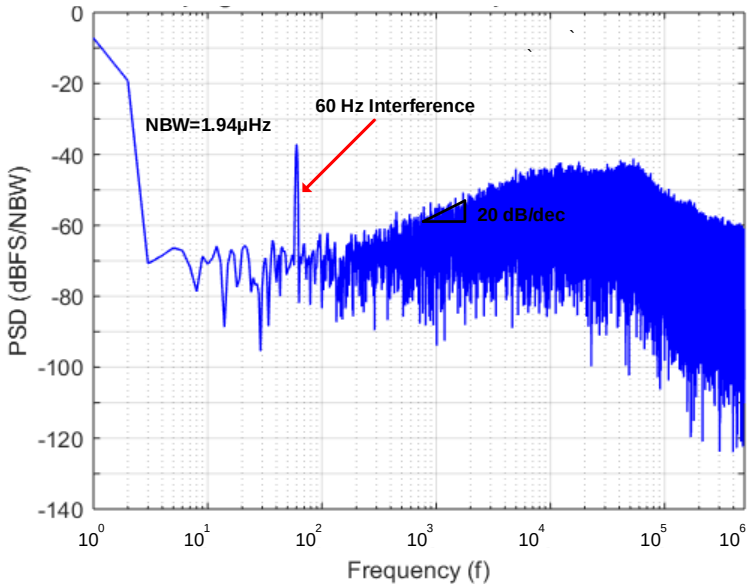


(a) INL vs. ADC Code, $T_{converter} = 65.54$ ms.

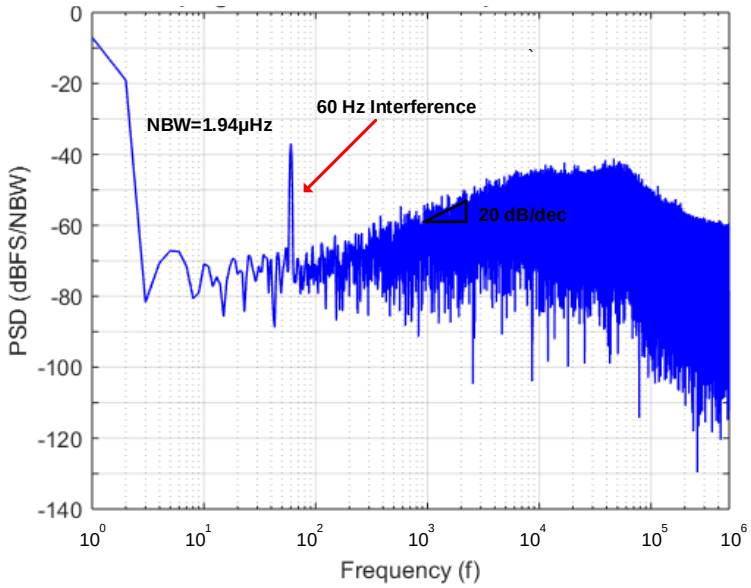


(b) INL vs. ADC Code, $T_{converter} = 16.4$ ms.

Figure 5.24: INL for $T_{converter} = 65.54$ ms and $T_{converter} = 16.4$ ms.



(a) Modulator Output FFT for I=100 nA, $T_{converter}$ = 65.54 ms.



(b) Modulator Output FFT for I=100 nA, $T_{converter}$ = 16.4 ms.

Figure 5.25: Noise Shaping FFT for I=100 nA, $T_{converter}$ = 65.54 ms and $T_{converter}$ = 16.4 ms.

5.3 Complete Bluetooth TX and Sensor Circuitry (Chip 3)

Chip 3 contains the designs of Chapters 3 and 4. It includes a complete Bluetooth TX including the VCO, PA, dividers, PFD, CP and on-chip LPF. In addition, Chip 3 includes the same potentiostat and ADC used in Chip 2. Figure 5.26 shows the complete system schematic. As in Chip 2, the potentiostat inputs include the electrochemical sensor (WE,CE and RE) as well as the voltage to be driven onto the RE. The 1 MHz reference clock for both the RF and sensor subsystems is also provided externally. The output data from the sensor is currently output from the chip to be processed by an external FPGA (replacing on-chip DSP digital logic), which is then Gaussian shaped and provided back as an input to the Bluetooth modulator. This is ultimately transmitted to the external antenna. The power supplies to the system include $AVDD_{POT}$, $AVDD_{ADC}$, $DVDD_{ADC}$, $AVDD_{RF}$ and $DVDD_{RF}$. In addition, the circuit uses the following grounds: $AGND_{SENSOR}$, $DGND_{SENSOR}$, $AGND_{RF}$, $AVDD_{RF,PA}$ and $DGND_{RF}$.

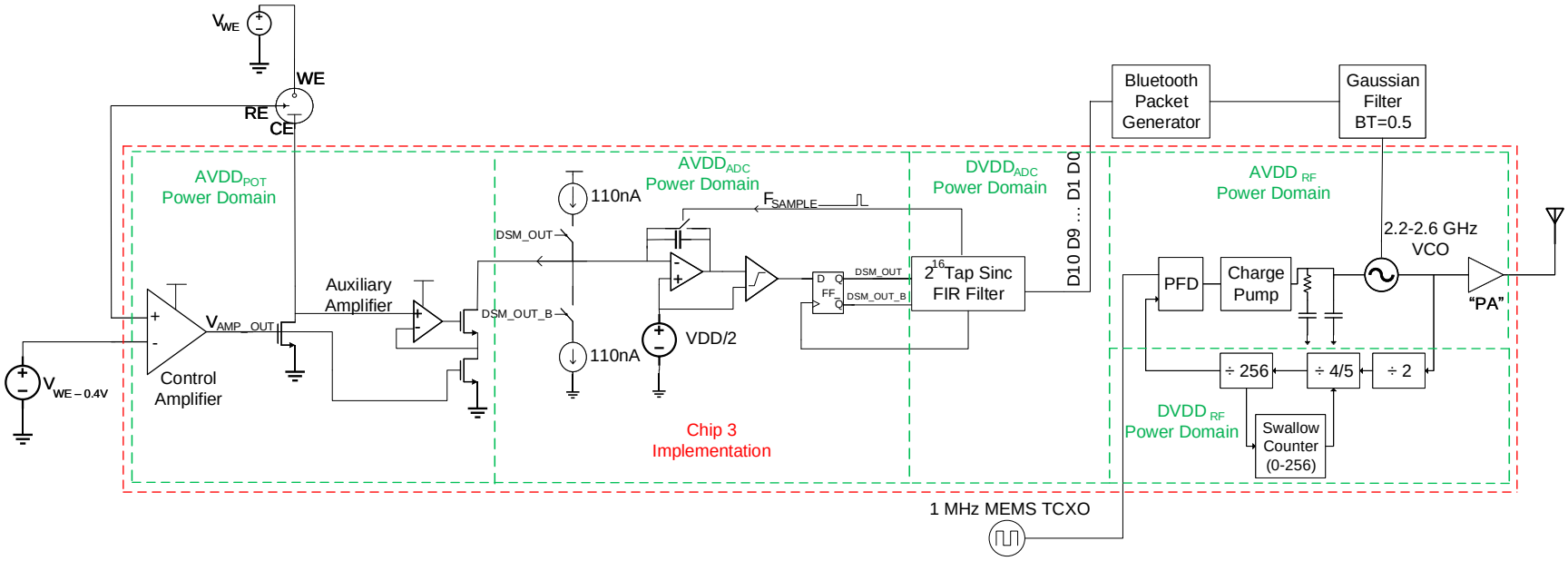


Figure 5.26: Architecture of Chip 3.

5.3.1 Chip 3 Layout

Chip 3 is 2.465 mm x 1.0356 mm with 58 pads with an additional 9 internal pads. Chip 3 is also pad-limited, and thus the active area is much smaller than the area needed for the output pads. To utilize the additional area, NMOS and PMOS test structures were placed within the chip to allow for transistor characterization.

In terms of additional layout from Chip 1 and Chip 2, the major changes are in the Bluetooth modulator. The PA output was changed to output -20 dBm output power. In addition, additional layout was completed to add the charge pump and loop filter to complete the integrated PLL design.

Due to fabrication delays, experimental results from Chip 3 will not be reported in this thesis. However, a test PCB has been designed to allow for testing to be completed when the chip arrives from the foundry. The schematic for this test PCB is detailed in Appendix F.

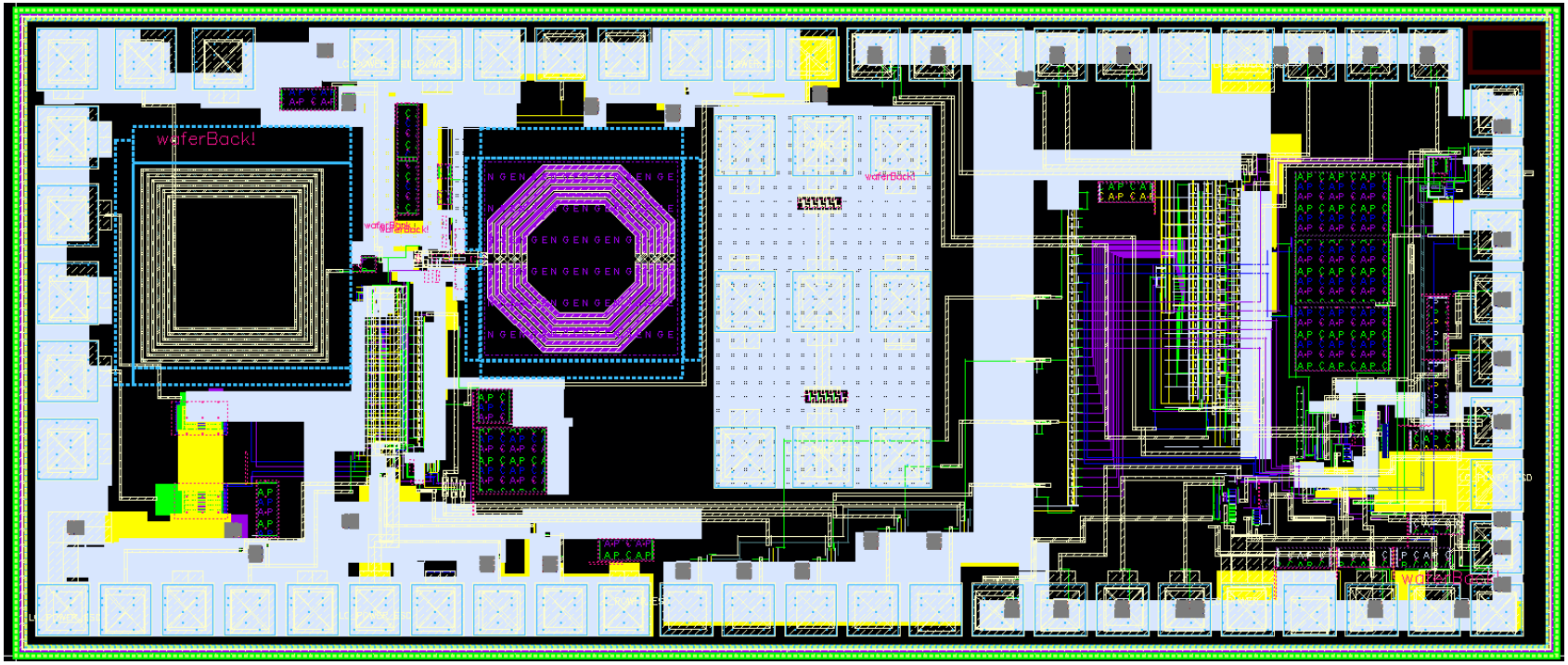


Figure 5.27: Layout of Chip 3

Chapter 6

Conclusions and Future Work

The motivation for contact-lens based glucose monitoring stems from the inconvenient and invasive available methods to measure blood sugar levels. Given rising rates of type-2 diabetes, there is a need to provide a more convenient solution which can quickly provide patients with reliable glucose measurements. The purpose of this thesis was to investigate the feasibility of a contact-lens based, Bluetooth energy harvesting glucose sensor.

Table 6.1 compares this work against prior art discussed in this thesis. In both prior art and this thesis, there is an expectation to run various blocks for short periods of time to reduce the energy consumption. This is analogous to scaling the DC power consumption of the block by the duty cycle of the measurement and transmission. To be able to accurately compare the power consumption of the blocks implemented, the block power consumption in this work are scaled based by the duty cycle of the block relative to the total on-time of the system $\frac{t_{on}}{t_{total}}$:

$$P_{DCdutycycled} = P_{DC}\frac{t_{on}}{t_{total}}. \tag{6.1}$$

where t_{on} and t_{total} were derived in Table 1.2. Compared to previous work, this work achieves the best duty-cycled DC power consumption $P_{DCdutycycled}$. It is clear that the power-budget of the system is only possible given the aggressive duty-cycling projected. However, this work does not include the power consumption of the energy harvester, voltage regulation and reference oscillator, as these blocks were not implemented in this thesis. Furthermore, these numbers are based on a target duty-cycle for each block. These numbers may change once the complete system is implemented. This work implements all sub-systems using a 0.5 V supply, instead of regulating multiple voltages per sub-system. The motivation behind this was to reduce the number of regulators necessary in the full system, increasing overall DC efficiency.

In terms of RF transmission, this work implemented a BLE compliant transmitter which consumes 200 μW (8 nW duty-cycled). The RF transmitter used in [2] and [5] is based on custom protocols which use RFID to transmit data. The main advantage of the proposed architecture here is that BLE is ubiquitously available in mobile phones, which makes this work more robust and realizable for practical applications. [6] implements NFC for RF communication, which is also available on mobile phones. However, due to the low frequencies used in NFC (13.56 MHz), the system requires a large off-chip inductor to transmit data, which is not feasible on a contact-lens. Thus, the work in [6] implants their device in the patients tissue, to sense blood glucose instead of tear glucose. This is an invasive procedure, which this work is trying to avoid.

The potentiostat implemented is a 0.5 V current-mirror based topology with $V_{CELL} = 0.4$ V, which consumes 275 nW (225 nW duty-cycled). Compared to [2], the proposed work implements a potentiostat operating with much lower headroom, which is required to support $V_{CELL} = 0.4$ V. The potentiostat implemented in this work is quite similar to the one implemented in [6]. However, the requirements in [6] are relaxed as they design the system assuming a lower $V_{CELL} = 0.2$ V. The DC power consumption of the potentiostat in this work is lower than either of the other complete systems. The $\text{FOM}_{Potentiostat}$ is the highest in this work as compared to the compared glucose potentiostats.

The sensor readout circuitry implemented in this work is a 11-bit IADC, which consumes 4.525 μW (36.2 nW duty-cycled). It achieves a Noise-free code resolution of 8.6 bits and and INL/DNL of $\pm$6 LSB/$\pm$0.3 LSB with $T_{conversion} = 65.56$ ms. The readout circuitry in [2] is a differential ring-oscillator, where the glucose current is converted to frequency to modulate the antenna for RFID communication directly. Thus, this system does not attempt to digitize the sensor data directly. However, the work in [6] implements a 10-bit IADC which also digitizes the glucose current. They achieve an ENOB of 9.3 bits with INL/DNL $\pm$0.6 LSB/$\pm$0.8 LSB. The IADC implemented in this work suffers from high circuit noise from the electronics, which would need to be reduced in another iteration to achieve the specified resolution. However, despite the reduced noise-free code resolution, the accuracy achieved is still adequate for clinical applications.

Table 6.1: Comparison of results against previous work

	JSSC '12 [2]	JSCC '13 [5]	JBHI '15[6]	This work
General				
Application	Contact Lens Glucose Sensor	Batteryless EEG Sensor	Implantable RFID CGM	Contact Lens Glucose Sensor
V_{DD}	1.2 V	1.2 V AFE / 1 V LO / 0.5 V PA+DSP	1.2 V AVDD/1.0 DVDD	0.5 V
Power Consumption [1] Power Consumption [2]	3 μW 1.1 μW	19 μW 5.6 μW	50 μW 35 μW	272 nW (206 μW non-duty cycled sum)
	Regulator+Bandgap: 1 μW Ring Oscillator: 600 nW Potentiostat: 500 nW Digital: 400 nW	Supply Regulation: 4.05 μW TX: 190 nW duty-cycled (160 μW non-duty cycled) AFE: 5.4 μW Digital+Clock Gen: 8.9 μW	RFID: 28 μW ADC: 3 μW Potentiostat: 4 μW Digital: 15 μW	Bluetooth TX: 8 nW (200 μW non-duty cycled) ADC: 36.2 nW (4.525 μW non-duty cycled) Potentiostat: 220 nW (275 nW non-duty cycled) Digital: 8 nW (950 nW non-duty cycled)
CMOS Technology	0.13 μm bulk	0.13 μm bulk	0.13 μm bulk	45 nm SOI
Chip size/Core Size	0.36 mm^2	8.25 mm^2	2.4 mm^2	2.55 mm^2
Energy Harvesting Performance				
Energy Source	RF	Thermal+RF	Inductive	RF (assumed)
Input Harvesting Power	30 dBm	60 μW+10dBm kick	20 dBm @ 3cm	10 dBm @ 5 cm (assumed)
Rectifier+Regulator Efficiency	20%	35%	45%	50% (assumed)
Energy Storage Capacitor	500pF on-chip	off-chip	on-chip	on-chip (assumed)
RF Performance				
RF Protocol	Custom	Custom	NFC	BLE
Modulation scheme	FM-LSK	BFSK	LSK	GMSK
Carrier Frequency Range	1.8 GHz	400 MHz	13.56 MHz	2.2 GHz - 2.48 GHz
RF Output Power (P_{out}) Phase Noise @ 1 MHz Reference Spur @ 2 MHz offset Oscillator FoM	- - - -	-18.5 dBm - - -	- - - -	-20 dBm (simulated) -108.5 dBc/Hz -30.5 dBm (simulated) 183.44 dB
Sensor Performance				
WE Material CE Material RE Material	Ti/Pd/Pt + GOD Ti/Pd/Pt + GOD Ti/Pd/Pt + GOD	- - -	- - -	Ti/Pd/Pt + GOD (assumed) Ti/Pd/Pt + GOD (assumed) Ti/Pd/Pt + GOD (assumed)
WE-RE Cell Voltage	0.4 V	-	0.2 V	0.4 V (assumed)
Glucose level	0.05 mM - 2 mM	-	0 -30 mM	3 μM - 2mM (assumed)
Settling Time	15 s	-	-	15 s (assumed)
Potentiostat Performance				
Architecture	Current-Mirror	-	Current-Mirror	Current-Mirror
Current Range	50pA - 150nA	-	0-20nA	0.15 nA - 100 nA
$FOM_{Potentiostat}$	0.12	-	0.001	0.145
ADC Performance				
Topology	I-to-F Differential Ring Osc.	-	1st order Incremental ADC	1st order Incremental ADC
Resolution	400Hz/mM	-	10-bit	11-bit
Conversion Time	-	-	-	65.54 ms
ENOB/Noise Free code resolution	-	-	9.3 bit (ENOB)	8.6 bit (includes potentiostat noise)
INL/DNL	-	-	$\pm$0.6 LSB/$\pm$0.8 LSB	-6 LSB/$\pm$0.8 or $\pm$0.3 LSB

[1] Total power consumption of all blocks

[2] Total power consumption of only blocks implemented in this work

Overall, this thesis shows that a contact-lens Bluetooth energy harvested glucose sensor is feasible to implement.

6.1 Future Work

Several design improvements can be made to the work presented here. For example, the modulation index is currently not well controlled, as it is a process varying parameter, thus the implementation can be reworked to reduce the sensitivity across process. Furthermore, the charge pump implementation could be improved to provide better current matching and hence reduced reference spur. Another method to reduce reference spur would be to change the PFD such that the glitch pulse is reduced. For the sensor, two important changes would be to reduce the TIA feedback capacitance as well as enhance the speed of the comparator used in the ADC. In addition, a fixed offset current could be added at the input of the ADC to allow the sensor current to use the entire dynamic range of the ADC, requiring 10 bits rather than 11 bits. Furthermore, to improve the energy consumption of the ADC, switching from a 1st-order modulator to a 2nd-order modulator is recommended. Despite the additional circuit complexity, the improved OSR-to-SNR tradeoff allows the ADC conversion time to be reduced significantly. Finally, power-gating should be added to every block to allow selective power-up during the different phases of the glucose measurement.

There are also many additional areas that require further research. On the circuit side, the implementation of the RF energy harvesting from the antenna to the regulated output requires a detailed analysis. In particular, detailed study of the efficiency of the rectifier and regulator are warranted as they directly reduce the harvested energy. In addition, the design of a Bluetooth RF receiver that can be powered on a limited energy budget is also an interesting topic for further research, as it enables many future applications. Moreover, low power digital circuitry needs to be integrated on-chip to interface between the sensor and the RF TX. The design of a 1 MHz silicon MEMS oscillator is also of interest as it currently is implemented off-chip. The performance of this oscillator is crucial to provide predictable performance for both the RF and sensor subsystems. For the sensor, further research into reducing the activation voltage of the glucose reaction would allow the WE to be powered off the same supply as the sensing electronics.

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APPENDICES

Appendix A

CMOS 45nm RFSOI Technology

A.1 CMOS Silicon-on-Insulator Technology

The technology used for design is the 45-nm RF SOI-CMOS technology. Figure A.1 shows a cross section of an NMOS transistor built in this technology.

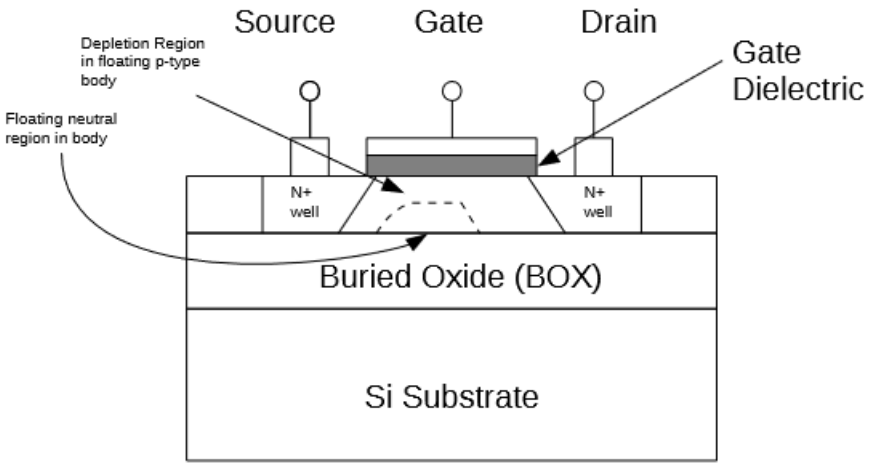

Figure A.1: PD-SOI NMOS cross-section.

SOI provides many benefits compared to standard bulk CMOS. These include rductions in off and substrate leakage currents, substrate noise coupling, V_{th} and short channel effects [35]. It achieves this by isolating the bulk of each transistor by an insulating buried oxide (BOX), which physically isolates the bulk from the substrate. However, in this technology, the bulk is only partially depleted, which causes a kink in the I-V curve of the MOSFET can occur when charge builds up in the floating bulk region [36]. Simulation data is shown in Figure A.2 which displays this. The partially-depleted transistor has a shift in the I-V curve at approximately 0.65 V, which corresponds to reduced output impedance and linearity. Fortunately, this design is using a supply voltage of 0.5 V, thus avoiding this effect altogether.

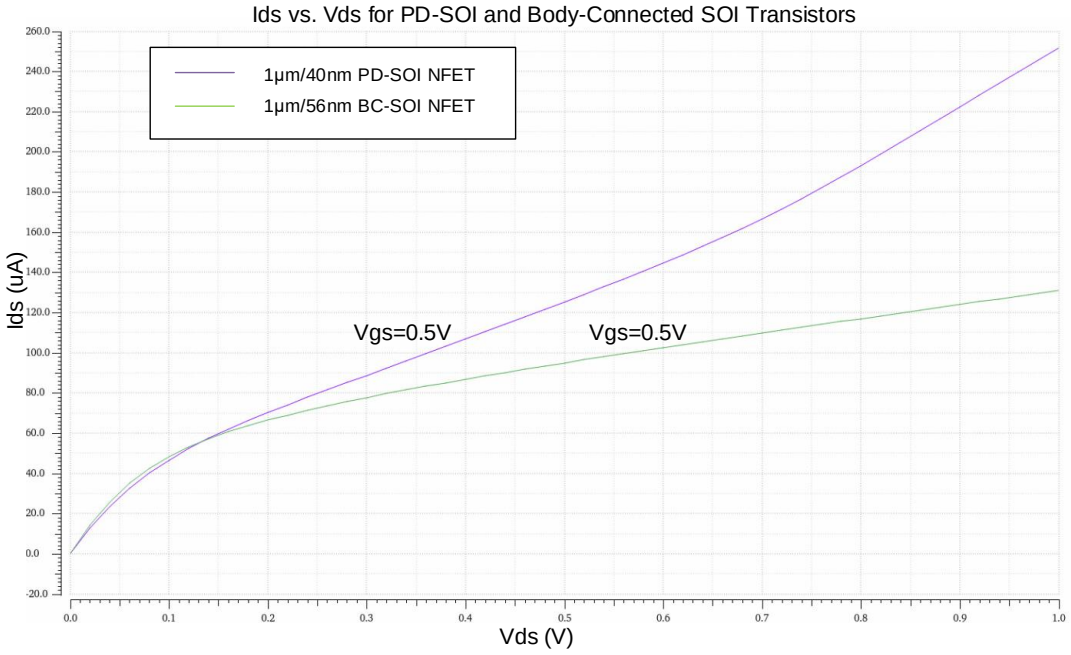

Figure A.2: IV-curve showing the kink effect present in PD-SOI.

Another clear advantage of this technology is the high resistivity substrate ($\rho = 3k\Omega - cm$). The sheet resistivity of the substrate improves the performance of passives such as inductors. Figure A.3 shows a single-section compact model for a spiral inductor. This model shows the inductance L_s, in series with a frequency varying resistance $r_{s(f)}$ which represents loss due to the metal interconnect. The substrate is modeled by C_{oxa}/C_{oxb} in series with an RC substrate model. It can be seen that with increased substrate resistivity

(r_{Sia} and r_{Sib}), the parallel substrate parasitic impedance will approach C_{Sia}/C_{Sib} at lower frequencies. This means that signal will be coupled to this node as set by the capacitive divider between C_{oxa}/C_{oxb} and C_{Sia}/C_{Sib}. The voltage divided signal will dissipate less real power as it appears across a larger resistance, which leads to higher Q-factor for inductors [12].

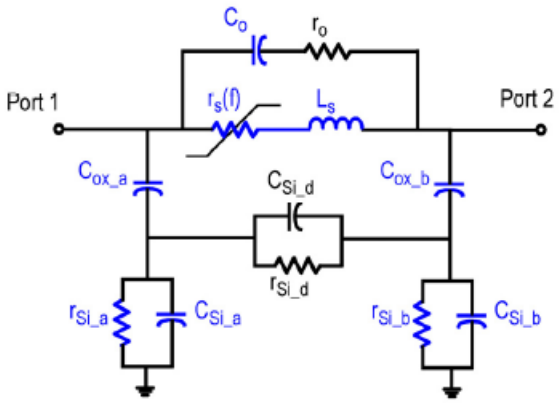

Figure A.3: Single-section compact model for a spiral inductor [12].

One disadvantage of this technology is the quantization of the length of transistors. Due to the complicated fabrication process, only specific lengths are allowed to be used in the design. This is particularly limiting in analog design as longer length transistors are generally used to obtain higher gain at the expense of bandwidth, and these limitations reduce the design space available.

Despite this, overall, this technology is particularly useful for this project. The high resistivity substrate improves the performance on the RF modulator. The isolation between transistor bulks allows for higher density digital circuitry to coexist on the chip without adversing affecting the performance of sensitive analog and RF circuitry, and finally, the reduced short channel affects improve the performance of the transistor itself.

A.2 Transistor Performance Simulations at 0.5V

Perhaps the most important parameter in supply limited designs is V_{th}. This thesis uses various transistor flavours for different sub-blocks. Floating-body PD-SOI FETs are minimum sized transistors (40 nm) which have partially depleted bulk regions. Another transistor type available is the body/bulk-connected transistor (BC-SOI), which allows the bulk to be externally driven to a voltage (but still isolated from other transistors by the BOX). Figure A.4 shows a cross section to illustrate the connection. Finally, for larger lengths, a thick-oxide BC-SOI transistor is available.

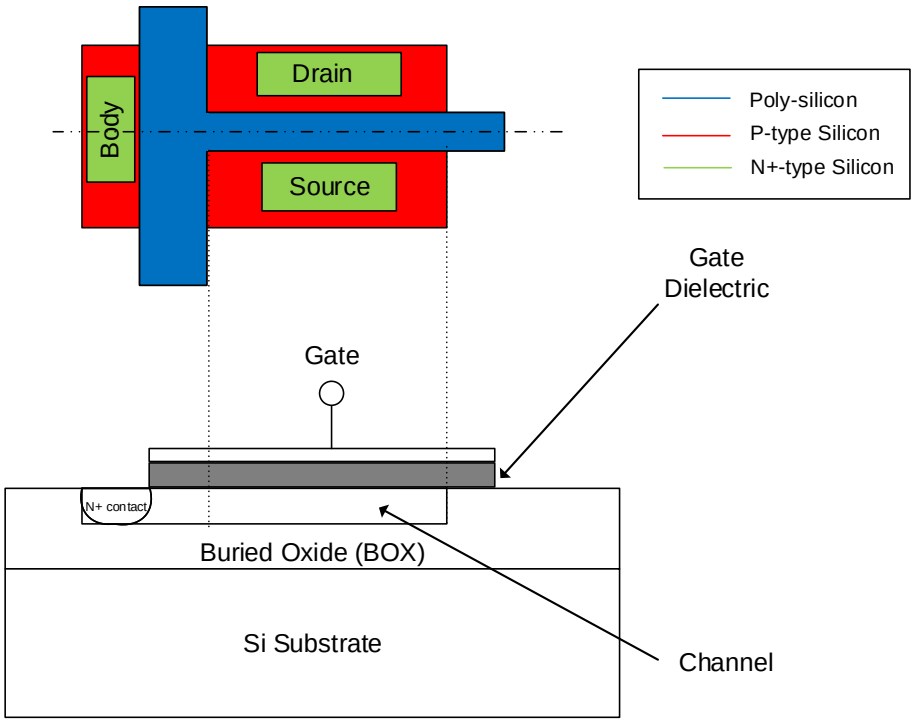

Figure A.4: NMOS BC-SOI layout and cross-section illustration.

Table A.1 summarizing the threshold voltage of various transistors in the technology. It is clear that many circuits will be forced to run in weak-inversion/sub-threshold operation due to headroom constraints.

A key specification for MOSFETs is the minimum V_{DS} voltage to stay in saturation. Square-law models predict that this would normally require

Table A.1: Summary of relevant transistors.

Transistor V_{th}			
Transistor	L	$V_{th}(Typical/Slow/Fast)$	I_{ds} @ $V_{ov} = 0$ V
Floating Body PD-SOI	40 nm	361.2 mV/386.6 mV/333.1 mV	29.3 μA
Body-connected SOI	56 nm	403.3 mV/431.1 mV/374.8 mV	32.48 μA
Thick Oxide BC-SOI	112 nm	468.7 mV/472 mV/401 mV	16.6 μA
Thick Oxide BC-SOI	2 μm	437.3 mV/438.4 mV/378.6 mV	0.4 μA

$$V_{DS} > V_{GS} - V_{TH}. \tag{A.1}$$

However, for transistors driven in weak-inversion, this equation is an inadequate estimate of minimum headroom requirements. In weak-inversion, the transistor acts a BJT formed by the source, drain, and body junctions. The minimum V_{DS} voltage is restated from Chapter 1 for convenience as:

$$I_{DS} = I_{D0}\frac{W}{L}e^{(V_{GS}/(nV_t))}(1 - e^{-V_{DS}/V_t}). \tag{A.2}$$

From eq. A.2, it is clear that I_{DS} will be relatively constant vs. V_{DS} when V_{DS} is greater than $5V_t$ where V_t is approximately 26mV at 25° C. Therefore, V_{ds} must be greater than 100 mV to keep the transistor in its linear region in weak-inversion. Simulation data for a 2 μm length transistor at various negative overdrive voltages shown in Figure A.5 confirms this result.

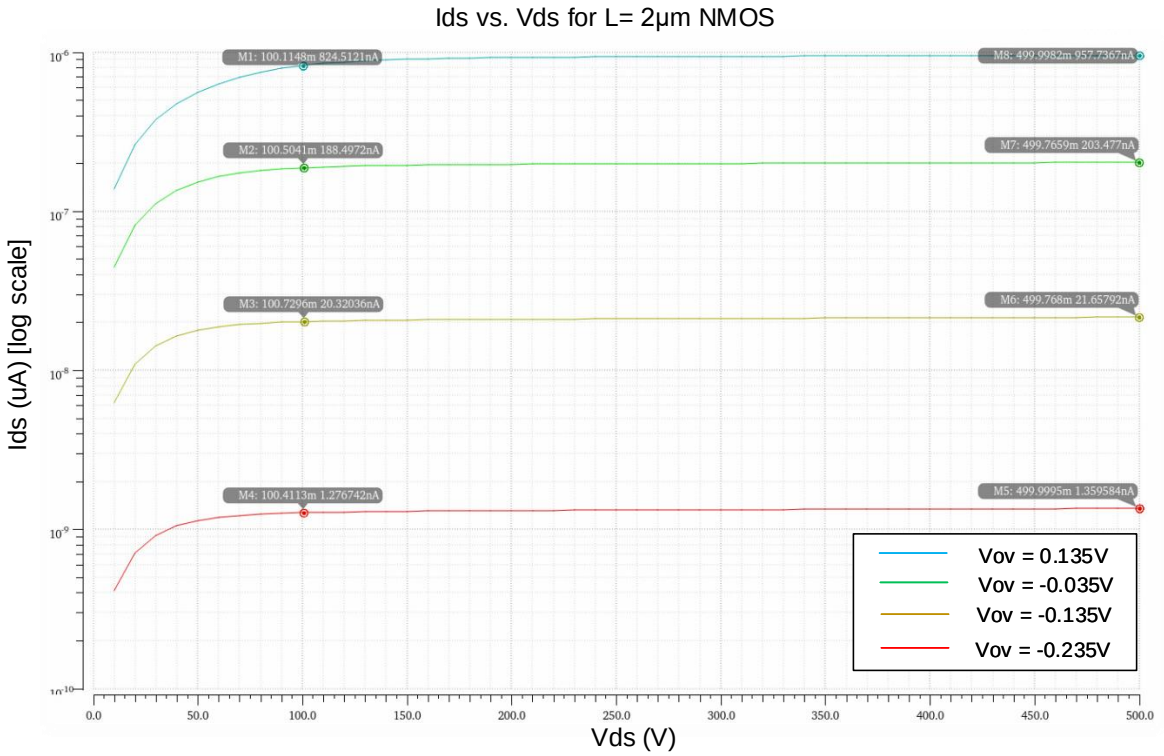

Figure A.5: Simulation of minimum V_{DS} for $V_{ov} < 0$.

Finally, simulation data is presented which summarizes various AC parameters is presented in Table A.2. From this data, it is clear that in the low current-density regime, 40 nm transistors are necessary for high-speed RF circuits. However, they suffer from low gain, thus unsuitable for many traditional analog sub-circuits. Thus, the longer length, slower transistors are utilized for many of the analog circuits implemented in this thesis.

Table A.2: Relevant simulation data for NMOS transistors.

Transistor	$I_d/W(A/m)$	V_{ov}(mV)	f_t(GHz)	$g_m(mA/V)$	$r_o(k\Omega)$	$g_m r_o$(V/V)
40nm PD-SOI	25.22	12	85	0.3404	21.5	7.39
56nm BC-SOI	15.32	-53.7	46	0.2311	53.1	12.26
112nm TOX-SOI	1.793	-130.6	6	0.03331	400.8	13.33
2um TOX-SOI	0.072	-87.3	0.036	0.001628	16647	271

Appendix B

Register Map and Pin Descriptions for all tape-outs

B.1 Chip 1

The bonding diagram for Chip 1 is shown in Figure B.1. The chip was bonded directly to the test PCB. The pin description for each pin is shown in Table B.1 and the 12-bit configuration register map is summarized in Table B.2.

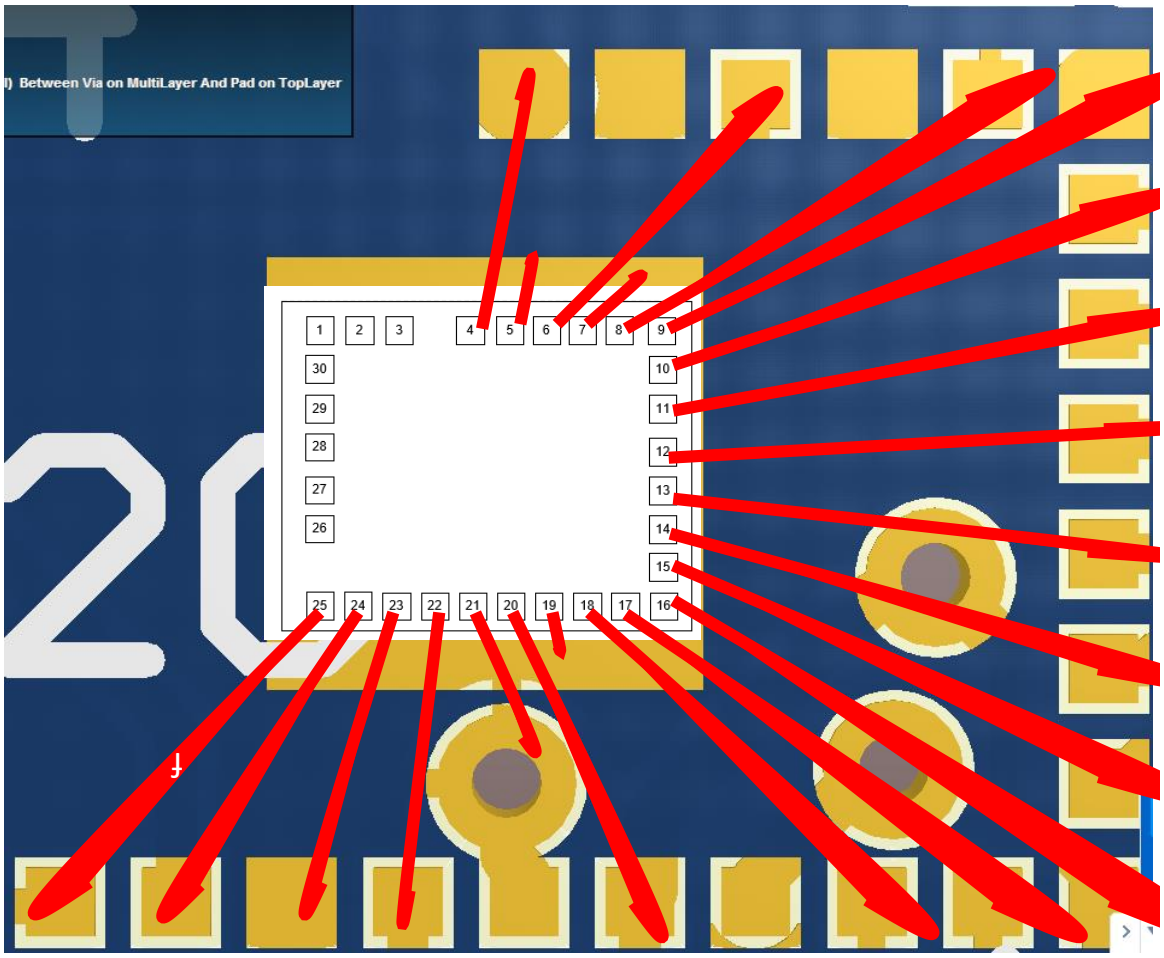

Figure B.1: Bonding diagram for Chip 1 annotated with pin numbers.

Table B.1: Register map for Chip 1.

Pin Number	Pin Name	Analog/Digital	Signal Type	Nominal Voltage / Voltage Range	Brief Description
1	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
2	V_RF_OUT	Analog	Ground	0 V	RF TX output to be probed using GSG
3	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
4	AVDD_RF	Analog	Power	0.5 V	RF power supply
5	AGND_RF	Analog	Ground	0 V	RF GND pad
6	VPLL	Analog	I/O	0 V – 0.5 V	PLL VCO control voltage, can be driven externally or generated internally
7	AGND_RF	Analog	Ground	0 V	RF GND pad
8	VMOD	Analog	Input	0 V – 0.5 V	Modulator VCO control voltage, driven externally
9	AVDD_RF	Analog	Power	0.5 V	RF power supply
10	SERIAL_IN_RST_B	Digital	Input	0 V – 0.5 V	Configuration register reset bar
11	SERIAL_IN_CLK	Digital	Input	0 V – 0.5 V	Configuration register clock
12	SERIAL_IN_DIN	Digital	Input	0 V – 0.5 V	Configuration register input data
13	SERIAL_IN_DOUT	Digital	Output	0 V – 0.5 V	Configuration register output data
14	DOWN	Digital	Output	0 V – 0.5 V	DOWN pulse from PFD
15	UP	Digital	Output	0 V – 0.5 V	UP pulse from PFD
16	DVDD_RF	Analog	Power	0.5 V	RF Digital Supply Voltage
17	V_REF_IN	Digtal	Input	0 V – 0.5 V	PLL Reference Frequency
18	V_DIVIDE_OUT	Digital	Output	0 V – 0.5 V	PLL Divider Output Frequency
19	DGND_RF	Digital	Ground	0 V	RF Digital GND
20	DVDD_RF	Digital	Power	0.5 V	RF Digital Supply Voltage
21	DGND_RF	Digital	Ground	0 V	RF Digital GND
22	SYSTEM_RST_RF	Digital	Input	0 V – 0.5 V	RF Digital Reset Signal, also resets shift register
23	DGND_RF	Digital	Ground	0 V	RF Digital GND
24	VBUFF_REG	Analog	Bias	0.4 V	RF Divider Buffer Gate driving voltage
25	DVDD2_RF	Analog	Power	1 V	RF Divider Buffer supply voltage
26	DGND_RF	Digital	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
27	V_DIV_16_20	Digital	Output	0 – 0.5 V	PLL Divide-by-16to20 CLK output to be probed using GSG + bias-T
28	DGND_RF	Digital	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
29	V_DIV_8_10	Digital	Output	0 V – 0.5 V	PLL Divide-by-8to10 CLK output to be probed using GSG + bias-T
30	DGND_RF	Digital	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded

Table B.2: Register map for Chip 1.

Bit	Function
LSB (B0)	PVT Bank Bit 0
B1	PVT Bank Bit 1
B2	PVT Bank Bit 2
B3	Divider Output Buffers Enable
B4	Channel Select B0
B5	Channel Select B1
B6	Channel Select B2
B7	Channel Select B3
B8	Channel Select B4
B9	Channel Select B5
B10	Channel Select B6
MSB (B11)	Channel Select B7

B.2 Chip 2

The bonding diagram for Chip 2 is shown in Figure B.2. The pin description for each pin is shown in Table B.3 and the 26-bit configuration register map is summarized in Table B.4.

The package used was a plastic leaded chip carrier (PLCC) package obtained from Spectrum Semiconductor with model number CQJ3207. It is a 32-pin 0.550" by 0.400" package with a 0.2" by 0.23" cavity. The pin numbers do not align to the pin numbers used by the package.

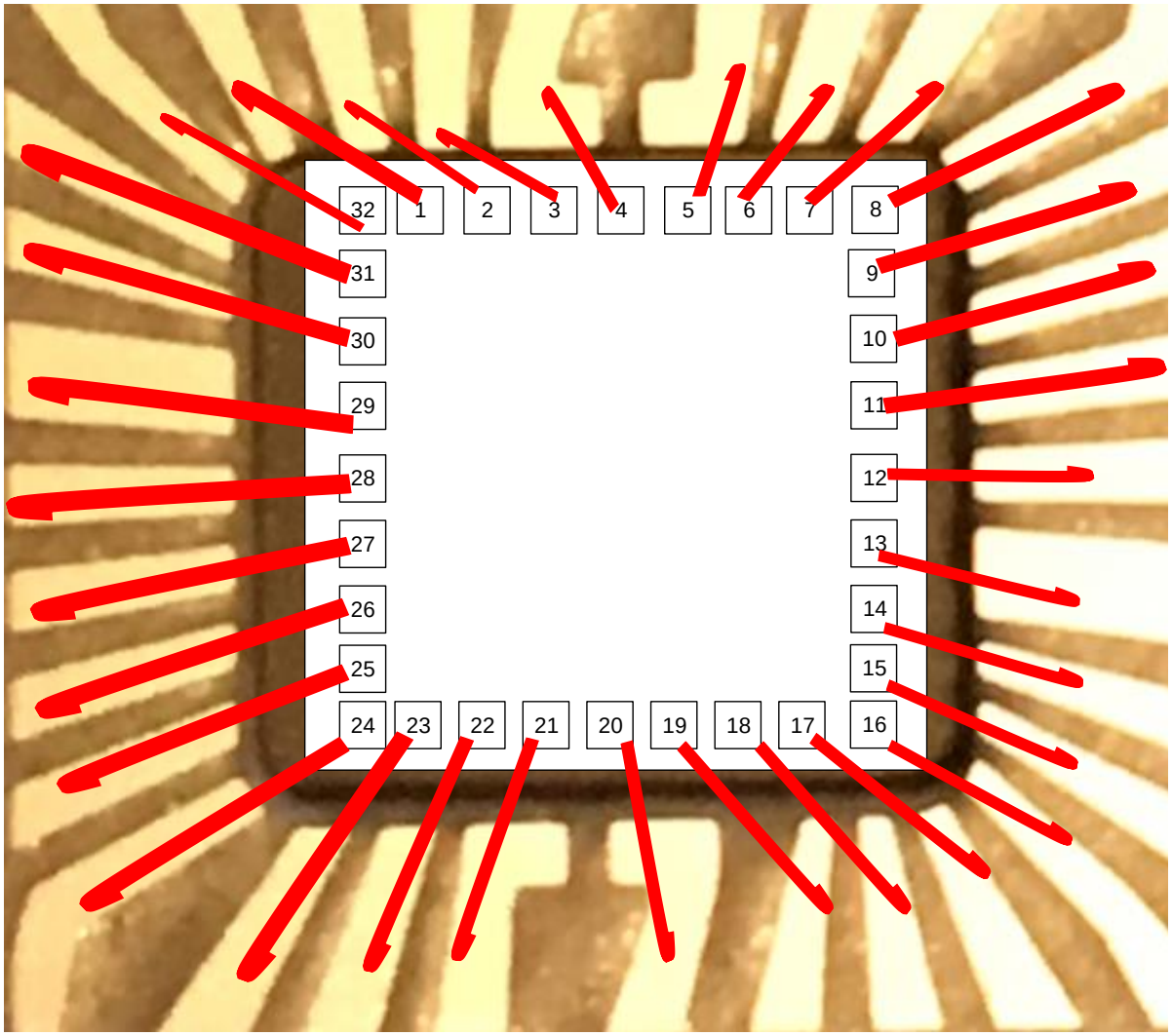

Figure B.2: Bonding diagram for Chip 2 annotated with pin numbers.

Table B.3: Register map for Chip 2.

Pin Number	Pin Name	Analog/Digital	Signal Type	Nominal Voltage / Voltage Range	Brief Description
1	VMIRROR2_BIAS_SENSOR	Analog	Bias	0.13 V	Ground side resistor bias from PCB, R=100 kΩ
2	VMIRROR1_BIAS_SENSOR	Analog	Bias	0.285 V	Ground side resistor bias from PCB, R=6 MΩ
3	AGND_POT	Analog	Ground	0 V	Potentiostat GND
4	AVDD_POT	Analog	Power	0.5 V	Potentiostat power supply
5	VPOS_POT	Analog	Input	0.375 V	Potentiostat input voltage which sets V_{RE}
6	VRE_POT	Analog	Output	0.375 V	Potentiostat output voltage to the RE
7	VCE_POT	Analog	Input	0 V	Potentiostat CE input
8	VMIRROR_NMOS_POT	Analog	Bias	0.24 V	Supply-side resistor bias from PCB, R=2.6 MΩ
9	-	-	-	-	-
10	SERIAL_IN_DIN	Digital	Input	0 V – 0.5 V	Configuration register input data
11	SERIAL_IN_CLK	Digital	Input	0 V – 0.5 V	Configuration register clock
12	SERIAL_IN_RST	Digital	Input	0 V – 0.5 V	Configuration register reset
13	SERIAL_IN_DOUT	Digital	Output	0 V – 0.5 V	Configuration register output data
14	SYSTEM_RST_SENSOR	Digital	Input	0 V – 0.5 V	Reset signal for digital circuitry (does not reset config register)
15	ADC_SERIAL_DOUT	Digital	Output	0 V – 0.5 V	ADC serial interface output data
16	ADC_SERIAL_RST	Digital	Input	0 V – 0.5 V	ADC serial interface reset
17	ADC_SERIAL_CLK	Digital	Input	0 V – 0.5 V	ADC serial interface clock
18	ADC_SHIFT_LOAD_B	Digital	Input	0 V – 0.5 V	ADC serial interface load sample or shift sample out
19	DGND_SENSOR	Digital	Ground	0 V	Sensor DGND pad
20	DVDD_SENSOR	Digital	Power	0.5 V	Sensor DVDD pad
21	DIV_BY_N_PULSE	Digital	Output	0 V – 0.5 V	ADC decimation-complete pulse
22	DSM_OUT_ADC	Digital	Output	0 V – 0.5 V	ADC modulator output
23	ADC_SAMPLE_CLK	Digital	Input	0 V	ADC system clock
24	EXTRA_ADC_INT_OUT	Analog	Output	0 V – 0.5 V	Duplicate integrator output, configured by shift register
25	AGND_SENSOR	Analog	Ground	0 V	Sensor AGND pad
26	INT_OUT_ADC	Analog	Integrator	0 V – 0.5 V	Integrator output, configured by shift register
27	IBIAS2_ADC	Analog	Bias	0.22 V	Ground-side resistor bias from PCB, R=2.75 MΩ
28	IBIAS1_ADC	Analog	Bias	0.3 V	Supply-side resistor bias from PCB, R=2.75 MΩ
29	VREF_ADC	Analog	Input	0.25 V	Reference voltage for integrator in ADC
30	AVDD_ADC	Analog	Power	0.5 V	ADC Analog power pad
31	IIN_ADC	Analog	Input	0.25 V	Input current source into ADC, configured by shift register
32	INT_RST_ADC	Digital	Input	0 V – 0.5 V	Integrator reset signal

Table B.4: Register map for Chip 2.

Bit	Function
LSB (B0)	ADC Counter Value $C15_{bar}$
B1-B15	ADC Counter Value $C14_{bar} - C0_{bar}$
B16	Disconnect DSM Feedback
B17	Connect ADC Input Current Pad
B18	Disconnect DSM Input
B19	Disconnect Potentiostat Output
B20	Connect TIA Output Voltage Pad
B21	Connect extra TIA Output Voltage Pad
B22	Disconnect Reference Electrode
B23	Disconnect Counter Electrode
B24	Disconnect 33nF of TIA feedback capacitance
MSB (B25)	Disconnect another 33nF of TIA feedback capacitance

B.3 Chip 3

The pin diagram for Chip 3 is shown in Figure B.3 and its bonding diagram is shown in Figure B.4. The pin description for each pin is shown in Table B.5 and Table B.6.

The package used for Chip 3 is a 1.000" square package with a 0.400" cavity (topside) with Kyocera part number KD-P86542-A. The pins of this package are arranged on an 10 x 10 pin grid at 0.1" centers. There are two full rows of pins around the outside. The pin numbers do not align to the pin numbers used by the package.

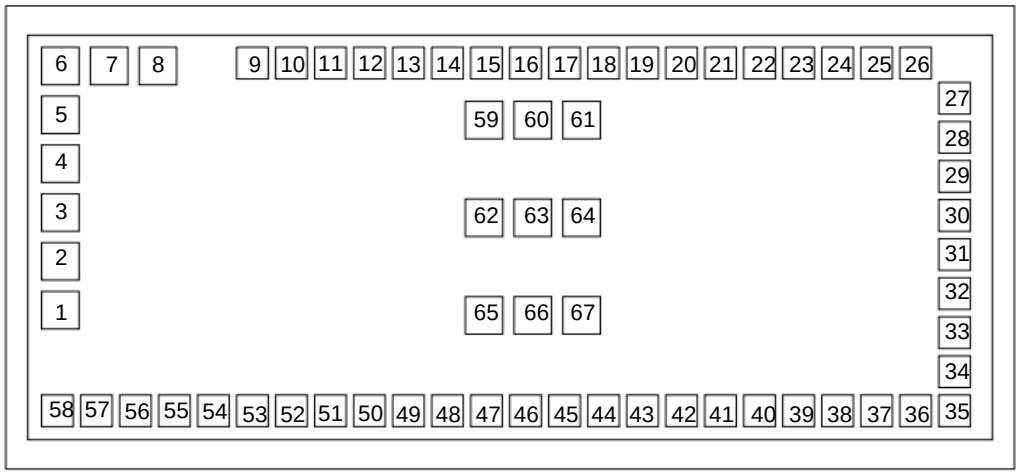

Figure B.3: Chip diagram for Chip 3 annotated with pin numbers.

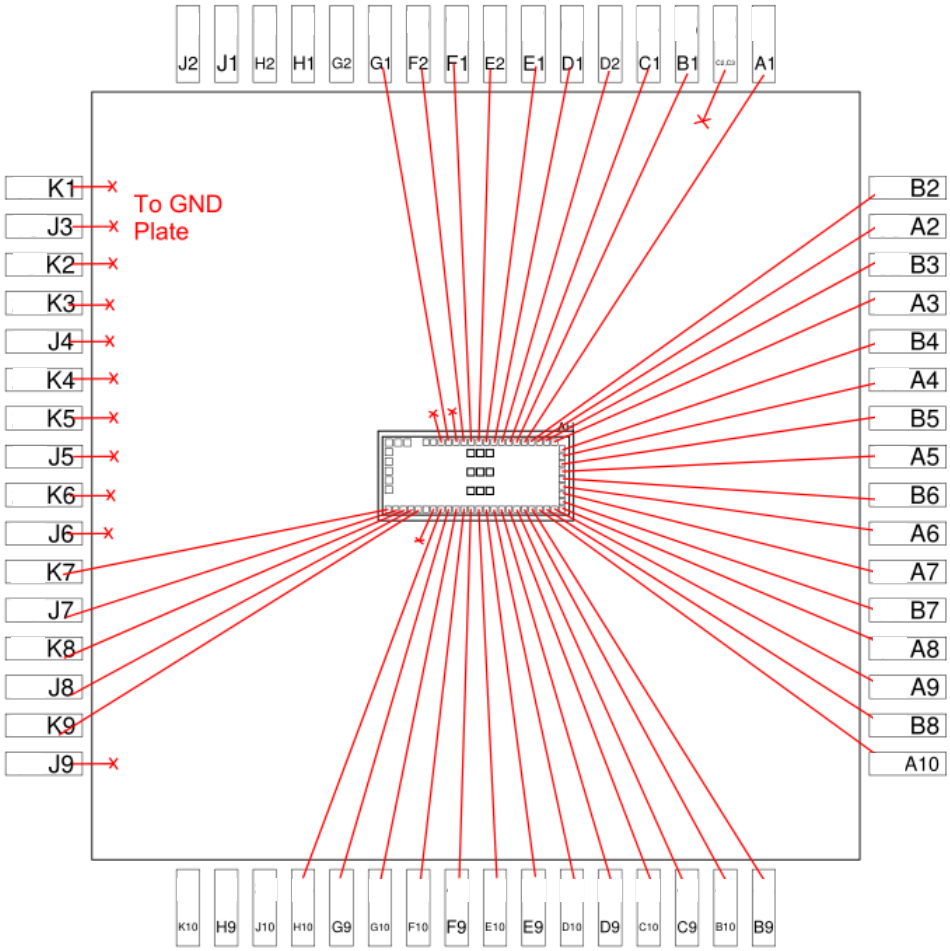

Figure B.4: Bonding diagram for Chip 3.

Table B.5: Pin description table for Chip 3.

Pin #	Name	Analog/ Digital	Signal Type	Nominal Voltage/ Voltage Range	Brief Description
1	DGND_RF	Digital	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
2	V_DIV_16_20	Digital	Output	0 – 0.5 V	PLL Divide-by-16to20 CLK output to be probed using GSG + bias-T
3	DGND_RF	Digital	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
4	V_DIV_8_10	Digital	Output	0 V – 0.5 V	PLL Divide-by-8to10 CLK output to be probed using GSG + bias-T
5	DGND_RF	Digital	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
6	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
7	V_RF_OUT	Analog	Ground	0 V	RF TX output to be probed using GSG
8	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
9	VDD_PA	Analog	Power	0.4 V	PA power supply
10	AVDD_RF	Analog	Power	0.5 V	RF power supply
11	AGND_RF	Analog	Ground	0 V	RF GND pad
12	VPLL	Analog	I/O	0 V – 0.5 V	PLL VCO control voltage, can be driven externally or generated internally
13	AGND_RF	Analog	Ground	0 V	RF GND pad
14	VMOD	Analog	Input	0 V – 0.5 V	Modulator VCO control voltage, driven externally
15	AVDD_RF	Analog	Power	0.5 V	RF power supply
16	IBIAS1_CP	Analog	Bias	0.4 V	Supply-side resistor bias from PCB, R=9.5 kΩ
17	SYSTEM_RST_SENSOR	Digital	Input	0 V – 0.5 V	Reset signal for digital circuitry (does not reset config register)
18	ADC_SERIAL_DOUT	Digital	Output	0 V – 0.5 V	ADC serial interface output data
19	ADC_SERIAL_RST	Digital	Input	0 V – 0.5 V	ADC serial interface reset
20	ADC_SERIAL_CLK	Digital	Input	0 V – 0.5 V	ADC serial interface clock
21	ADC_SHIFT_LOAD_B	Digital	Input	0 V – 0.5 V	ADC serial interface load sample or shift sample out
22	DGND_SENSOR	Digital	Ground	0 V	Sensor DGND pad
23	DVDD_SENSOR	Digital	Power	0.5 V	Sensor DVDD pad
24	DIV_BY_N_PULSE	Digital	Output	0 V – 0.5 V	ADC decimation-complete pulse
25	DSM_OUT_ADC	Digital	Output	0 V – 0.5 V	ADC modulator output
26	ADC_SAMPLE_CLK	Digital	Input	0 V	ADC system clock
27	EXTRA_ADC_INT_OUT	Analog	Output	0 V – 0.5 V	Duplicate integrator output, configured by shift register
28	AGND_SENSOR	Analog	Ground	0 V	Sensor AGND pad
29	INT_OUT_ADC	Analog	Integrator	0 V – 0.5 V	Integrator output, configured by shift register
30	IBIAS2_ADC	Analog	Bias	0.22 V	Ground-side resistor bias from PCB, R=2.75 MΩ
31	IBIAS1_ADC	Analog	Bias	0.3 V	Supply-side resistor bias from PCB, R=2.75 MΩ
32	VREF_ADC	Analog	Input	0.25 V	Reference voltage for integrator in ADC
33	AVDD_ADC	Analog	Power	0.5 V	ADC Analog power pad
34	IIN_ADC	Analog	Input	0.25 V	Input current source into ADC, configured by shift register
35	INT_RST_ADC	Digital	Input	0 V – 0.5 V	Integrator reset signal
36	VMIRROR2_BIAS_SENSOR	Analog	Bias	0.13 V	Ground side resistor bias from PCB, R=100 kΩ
37	VMIRROR1_BIAS_SENSOR	Analog	Bias	0.285 V	Ground side resistor bias from PCB, R=6 MΩ

Table B.6: Pin description table for Chip 3.

Pin #	Name	Analog/ Digital	Signal Type	Nominal Voltage/ Voltage Range	Brief Description
38	AGND_POT	Analog	Ground	0 V	Potentiostat GND
39	AVDD_POT	Analog	Power	0.5 V	Potentiostat power supply
40	VPOS_POT	Analog	Input	0.375 V	Potentiostat input voltage which sets V_{RE}
41	VRE_POT	Analog	Output	0.375 V	Potentiostat output voltage to the RE
42	VCE_POT	Analog	Input	0 V	Potentiostat CE input
43	VMIRROR_NMOS_POT	Analog	Bias	0.24 V	Supply-side resistor bias from PCB, R=2.6 MΩ
44	SERIAL_IN_RST	Digital	Input	0 V – 0.5 V	Configuration register reset, muxed between RF or Sensor register
45	SERIAL_IN_CLK	Digital	Input	0 V – 0.5 V	Configuration register clock, muxed between RF or Sensor register
46	SERIAL_IN_DIN	Digital	Input	0 V – 0.5 V	Configuration register input data, muxed between RF or Sensor register
47	SERIAL_IN_DOUT	Digital	Output	0 V – 0.5 V	Configuration register output data, muxed between RF or Sensor register
48	SERIAL_RF_SENSOR_B_EN	Digital	Input	0 V – 0.5 V	Configuration register mux select
49	DVDD_RF	Analog	Power	0.5 V	RF Digital Supply Voltage
50	V_REF_IN	Digtal	Input	0 V – 0.5 V	PLL Reference Frequency
51	V_DIVIDE_OUT	Digital	Output	0 V – 0.5 V	PLL Divider Output Frequency
52	DGND_RF	Digital	Ground	0 V	RF Digital GND
53	DVDD_RF	Digital	Power	0.5 V	RF Digital Supply Voltage
54	DGND_RF	Digital	Ground	0 V	RF Digital GND
55	SYSTEM_RST_RF	Digital	Input	0 V – 0.5 V	RF Digital Reset Signal, does not reset shift register
56	DGND_RF	Digital	Ground	0 V	RF Digital GND
57	VBUFF_REG	Analog	Bias	0.4 V	RF Divider Buffer Gate driving voltage
58	DVDD2_RF_SERIAL_CLK	Analog	Power	1 V	RF Divider Buffer supply voltage
59	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
60	TEST_STRUCTURE_PMOS_DRAIN	Analog	Output	0 V – 1 V	PMOS Drain for GSG probing, will not be wire-bonded
61	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
62	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
63	TEST_STRUCTURE_NMOS/PMOS_GATE	Analog	Input	0 V – 1 V	PMOS/NMOS Gate voltage for GSG probing, will not be wire-bonded
64	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
65	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded
66	TEST_STRUCTURE_NMOS_DRAIN	Analog	Output	0 V – 1 V	NMOS Drain for GSG probing, will not be wire-bonded
67	AGND_RF	Analog	Ground	0 V	RF GND pad for GSG probing, will not be wire-bonded

Chip 3 allows the register files of Chip 1 and Chip 2 to be accessed with the same mapping, with two additional outputs on Chip 1's register file in Table B.7 as shown below:

Table B.7: RF Register map for Chip 3.

Bit	Function
LSB (B0)	PVT Bank Bit 0
B1	PVT Bank Bit 1
B2	PVT Bank Bit 2
B3	Divider Output Buffers Enable
B4	Channel Select B0
B5	Channel Select B1
B6	Channel Select B2
B7	Channel Select B3
B8	Channel Select B4
B9	Channel Select B5
B10	Channel Select B6
B11	Channel Select B7
B12	Disconnect On-chip Loop Filter
MSB (B13)	Disconnect VCO Control Voltage Pad

Table B.8: Sensor Register map for Chip 3.

Bit	Function
LSB (B0)	ADC Counter Value $C15_{bar}$
B1-B15	ADC Counter Value $C14_{bar} - C0_{bar}$
B16	Disconnect DSM Feedback
B17	Connect ADC Input Current Pad
B18	Disconnect DSM Input
B19	Disconnect Potentiostat Output
B20	Connect TIA Output Voltage Pad
B21	Connect extra TIA Output Voltage Pad
B22	Disconnect Reference Electrode
B23	Disconnect Counter Electrode
B24	Disconnect 33nF of TIA feedback capacitance
MSB (B25)	Disconnect another 33nF of TIA feedback capacitance

Appendix C

Verilog-A model of VCO

```
‘include "constants.vams"
‘include "disciplines.vams"

module vco_model(vin, out);
/* IO Declarations */
input vin;
output out;
electrical vin;
electrical out;
/* Parameter Declarations */
parameter real Vmin=0; // Minimum input voltage
parameter real Vmax=Vmin+0.5 from (Vmin:inf); //Maximum input voltage
parameter real Fmin=2.35e9 from [0.0:inf); //Minimum output frequency
parameter real Fmax=2.55e9 from [Fmin:inf); //Maximum output frequency
parameter real ratio=1 from [1:inf]; //Divider ratio
parameter real Vamp=0.5 from [0:inf); //Ouptut sinusoid amplitude
parameter real ttol=1u/Fmax from [0:1*ratio/Fmax); //Crossing time tolerance
parameter real vtol=1e-9; //Voltage
//Minimum number of points per period for update
parameter integer min_pts_update=8 from [2:inf);
//Transition time for square output
parameter real tran_time = 10e-12 from (0:0.3/Fmax);
//std deviation of phase jitter (UI)
parameter real jitter_std_ui = 0 from [0:1);
```

```
/* Internal Variables */


real freq, phase, jitter_rad, dPhase, phase_ideal;
integer n, seed;
analog begin
@(initial_step)
begin
seed = 671;
n = 0;
dPhase = 0;
jitter_rad  = jitter_std_ui*2*‘M_PI;
end
// compute the freq from the input voltage
freq = ((V(vin) - Vmin)*(Fmax - Fmin) / (Vmax - Vmin)) + Fmin;
$bound_step(1/(min_pts_update*freq));
if ( freq > Fmax ) freq = Fmax;
if ( freq < Fmin ) freq = Fmin;
// change freq by ratio
freq = freq/ratio;

phase_ideal = 2*‘M_PI*idtmod(freq, 0, 1, -0.5);
phase = phase_ideal + dPhase;
@( cross(phase_ideal + ‘M_PI/2, +1, ttol, vtol)
or cross(phase_ideal - ‘M_PI/2, +1, ttol, vtol))
begin
dPhase = sqrt(ratio)*$rdist_normal(seed, 0, jitter_rad);
end
@( cross(phase + ‘M_PI/2, +1, ttol, vtol)
or cross(phase - ‘M_PI/2, +1, ttol, vtol))
begin
n = (phase >= - ‘M_PI/2)&&(phase < ‘M_PI/2);
end
//generate the output
V(out) <+ transition(n?Vamp:0, 0, tran_time);
end

endmodule
```

Appendix D

Arduino Code for testing

D.1 Chip 1

Below is the firmware used for the testing Chip 1:

```
//global pin list

int osc_board_en = 8;
int serial_rst_3v3 = 6;
int serial_clk_3v3_b = 5;
int serial_din_3v3_b = 4;
int system_rst_3v3_b = 3;
int vmod_ardiuno_3v3 = 11;

// PVT_D0, PVT_D1, PVT_D2, D_BUFF_ENABLE,
// ... SC_D0, SC_D1,SC_D2,SC_D3,SC_D4,SC_D5,SC_D6,SC_D7

byte pll_counter_val = 0; // want 177,189,216
//byte vco_options_val = (0<< 3) + (1 << 2) + (1 << 1) + (1 << 0);
// PVT_D0,PVT_D1,PVT_D2,D_BUFF_ENABLE
byte vco_options_val = 0; // PVT_D0,PVT_D1,PVT_D2,D_BUFF_ENABLE

void setup() {
  // put your setup code here, to run once:
```

```
  pinMode(osc_board_en, OUTPUT);
  pinMode(serial_rst_3v3, OUTPUT);
  pinMode(serial_clk_3v3_b, OUTPUT);
  pinMode(serial_din_3v3_b, OUTPUT);
  pinMode(system_rst_3v3_b, OUTPUT);
  pinMode(vmod_ardiuno_3v3, OUTPUT);
  digitalWrite(osc_board_en, HIGH);   // sets the on board oscillator on
  digitalWrite(serial_clk_3v3_b, HIGH);   // sets clk signal low
  digitalWrite(serial_din_3v3_b, HIGH); // set din to low
  digitalWrite(serial_rst_3v3, HIGH); // set serial_rstb to low
  digitalWrite(system_rst_3v3_b, LOW);   // reset the chip
  delay(1000);
  digitalWrite(serial_rst_3v3, LOW); // set serial_rstb to high
  digitalWrite(system_rst_3v3_b, HIGH);   // deassert chip reset
  delay(100);
  //configureNovChip(pll_counter_val,vco_options_val);
 // analogWrite(vmod_ardiuno_3v3, 128);
  //runOnce();
}
void configureNovChip(byte byte1, byte byte2){
  digitalWrite(system_rst_3v3_b, LOW); // set system_rst to high
  delay(100);
  digitalWrite(system_rst_3v3_b, HIGH); // set system_rst to high
  delay(100);
  shiftByte(byte1, 256);
  shiftByte(byte2, 16);
}
void shiftByte(byte transmitVal, int stopVal) {
  byte mask = 1; //our bitmask
  for (mask = 00000001; (mask>0)&&(mask<stopVal); mask <<= 1) {
  //iterate through bit mask
    if (transmitVal & mask){ // if bitwise AND resolves to true
      serialShift(1); // send 1
    }
    else{ //if bitwise AND resolves to false
      serialShift(0); // send 0
    }
  }
```

```
}
void testShiftRegister() {
  int mask = 1; //our bitmask
  bool flip = false;
  for (mask = 0; mask<24; mask++) {
    if (flip){
      serialShift(1); // send 1
    }
    else{
      serialShift(0); // send 0
    }
    flip = !flip;
  }
}
void serialShift(int value)
{
  delay(100);
  if (value == 1){
       digitalWrite(serial_din_3v3_b, LOW);   // sets din signal high
  }
  else {
       digitalWrite(serial_din_3v3_b, HIGH);   // sets din signal low
  }
  delay(100);
  digitalWrite(serial_clk_3v3_b, LOW);   // sets clk signal high
  delay(100);
  digitalWrite(serial_clk_3v3_b, HIGH);   // sets clk signal low
  delay(100);
  digitalWrite(serial_din_3v3_b, HIGH);   // sets din signal low

}
void runOnce(){
  //reset and wait
  digitalWrite(system_rst_3v3_b, LOW); // set system_rst to high
  delay(2000);
  digitalWrite(system_rst_3v3_b, HIGH); // set system_rst to high
  delay(2000);
```

```
  //shift 1
  serialShift(1);
  delay(100);
  serialShift(1);

  //digitalWrite(serial_din_3v3_b, HIGH);   // sets din signal low
  //delay(1000);
  //digitalWrite(serial_clk_3v3_b, LOW);   // sets clk signal high
 //serialShift(0);
 // delay(10000);
 // serialShift(0);

 for (int i=0; i<12; i++){
  //  delay(10000);
    serialShift(1);
  }

}
void loop() {
  // put your main code here, to run repeatedly:
    //testShiftRegister();

 //Cycle through PVT values for now without changing D_BUFF_ENABLE
 // delay(1000);

 /* digitalWrite(system_rst_3v3_b, LOW); // set system_rst to high
  delay(2000);
  digitalWrite(system_rst_3v3_b, HIGH); // set system_rst to high
  delay(1000);
  digitalWrite(serial_din_3v3_b, LOW);   // sets din signal high
  delay(1000);
  for (int i=0; i<12; i++){
    digitalWrite(serial_clk_3v3_b, LOW);   // sets clk signal high
    delay(1000);
    digitalWrite(serial_clk_3v3_b, HIGH);   // sets clk signal low
    delay(1000);
  }
```

```
*/
  /*if (vco_options_val < 16){
      configureNovChip(pll_counter_val, vco_options_val);
      vco_options_val = vco_options_val + 2;
  }
  else
  {
          vco_options_val = vco_options_val & 1;
  }
*/

/*  if (pll_counter_val < 256){
      configureNovChip(pll_counter_val, vco_options_val);
      pll_counter_val = pll_counter_val + 50;
  }
  else
  {
      pll_counter_val = 0;
  }*/
}
```

D.2 Chip 2

Below is the firmware used for the testing Chip 2:

```
//global pin list
int DSMOUT_ADC_3V3 = 9;
int ADC_SRST_3V3 = 10;
int ADC_S_Lb_3V3 = 11;
int ADC_SOUT_CLK_3V3 = 12;
int ADC_SDOUT_3V3 = 13;
int OSC_ENABLE_3V3 = 14;
int AVDD_EN_3V3 = 15;
int AVDD_ADC_EN_3V3 = 16;
int DVDD_EN_3V3 = 17;
```

```
int VDD_1V_EN_3V3 = 18;
int WE_EN_3V3 = 19;
int SIN_DIN_3V3 = 8;
int SIN_CLK_3V3 = 6;
int SIN_RST_3V3 = 5;
int SIN_DOUT_3V3 = 4;
int DBN_PULSE_3V3 = 3;

// USE_C15_B, USE_C14_B, USE_C13_B, ... USE_C1_B, USE_C0_B,
// DISCONNECT_DSM_FB, CONNECT_I_ADC_IN_PAD, DISCONNECT_DSM_IN, DISCONNECT_POT_OUT,
// CONNECT_VINT_ADC_PAD, CONNECT_EXTRA_INT_OUT, FLOAT_RE, FLOAT_CE,
// DISCONNECT_CAP1, DISCONNECT_CAP2

//SERIAL_IN_DOUT on 32 REGISTER

volatile int ADC_data_ready = 0;         // variable for reading adc data
volatile unsigned int ADC_OUTPUT_DATA = 0; //16 bit
volatile int ADC_OUTPUT_DATA_LOADED = 0;


void setup() {
  // put your setup code here, to run once:
  //synchronize to matlab
  //setup
 //supply enables
  pinMode(AVDD_EN_3V3, OUTPUT);
  pinMode(AVDD_ADC_EN_3V3, OUTPUT);
  pinMode(DVDD_EN_3V3, OUTPUT);
  pinMode(VDD_1V_EN_3V3, OUTPUT);
  pinMode(WE_EN_3V3, OUTPUT);

  //serial input to chip
  pinMode(SIN_DIN_3V3, OUTPUT);
  pinMode(SIN_CLK_3V3, OUTPUT);
  pinMode(SIN_RST_3V3, OUTPUT);
  pinMode(SIN_DOUT_3V3, INPUT);

 //on board oscillator
```

```
  pinMode(OSC_ENABLE_3V3, OUTPUT);

  //DSM Inputs to Ardiuno
  pinMode(DSMOUT_ADC_3V3, INPUT); //DSM Modulator data


  // DSM Serial Data
  pinMode(DBN_PULSE_3V3, INPUT); //Sample Ready Pulse

  pinMode(ADC_SRST_3V3, OUTPUT); //ADC output serial reset
  pinMode(ADC_S_Lb_3V3, OUTPUT);
  //Shift out to ardiuno or load from internal register to output register
  pinMode(ADC_SDOUT_3V3, INPUT); //Data out from chip serially
  pinMode(ADC_SOUT_CLK_3V3, OUTPUT); //CLK for output serial

//turn off supplies first

  digitalWrite(VDD_1V_EN_3V3, LOW);   // disables VDD_1V supply
  //delay(100);
  digitalWrite(AVDD_EN_3V3, LOW);   // disables AVDD_SENSOR supply
  //delay(100);
  digitalWrite(AVDD_ADC_EN_3V3, LOW);   // disables AVDD_ADC supply
  //delay(100);
  digitalWrite(DVDD_EN_3V3, LOW);   // disables DVDD supply
  //delay(100);
  digitalWrite(WE_EN_3V3, LOW);   // disables WE power supply
 // delay(100);

  // turn on rest of the system

  digitalWrite(VDD_1V_EN_3V3, HIGH);   // enables VDD_1V supply
  delay(10);
  digitalWrite(AVDD_EN_3V3, HIGH);   // enables AVDD_SENSOR supply
  delay(10);
  digitalWrite(AVDD_ADC_EN_3V3, HIGH);   // enables AVDD_ADC supply
  delay(10);
  digitalWrite(DVDD_EN_3V3, HIGH);   // enables DVDD supply
  delay(10);
```

```
  digitalWrite(WE_EN_3V3, HIGH);   // enables WE power supply
  delay(10);

  Serial.end();
  Serial.begin(115200);
  Serial.println('a');
  char a = 'b';
  /*while (a !='a')
  {
    a=Serial.read();
    delay(10);
  }*/

  //turn on oscillator
 digitalWrite(OSC_ENABLE_3V3, HIGH);   // enables on board oscillator
  delay(10);

  //need to reset system manually using switch
 // delay(1000);

  //Serial.println("resetting serial interfaces on chip");

  digitalWrite(SIN_DIN_3V3, LOW);   // sets serial in rst signal high
  delay(10);
  digitalWrite(SIN_RST_3V3, HIGH);   // sets serial in rst signal high
  delay(10);
  //digitalWrite(SIN_RST_3V3, LOW);   // sets serial in rst signal low
  //delay(10);
  digitalWrite(ADC_SRST_3V3, HIGH);   // sets serial out rst signal high
  delay(10);
  digitalWrite(ADC_SRST_3V3, LOW);   // sets serial out rst signal low
  delay(10);
  digitalWrite(ADC_S_Lb_3V3, LOW);
  // sets serial out load parallel data signal low
  delay(10);
//test
//
```

```
  //configureAprilChip(255,255,6,0,0);
  // configureAprilChip(0,0,6,0,0);
   // configureAprilChip(0,0,0,0,0);
   // attachInterrupt(1, loadADCdataISR, RISING);

   testShiftRegister();
   //test to see it come out
  int i=0;
  //serialShift(1); // send 1
  //serialShift(0); // send 1
  //serialShift(1); // send 1
  //serialShift(1); // send 1

  //for (i = 0; i<64; i++) {
  //    serialShift(0); // send 1
  //}
  //digitalWrite(SIN_RST_3V3, HIGH);   // sets serial in rst signal high
  //digitalWrite(SIN_DIN_3V3, HIGH);   // sets serial in rst signal high
  //digitalWrite(SIN_CLK_3V3, HIGH);   // sets serial in rst signal high

}
void configureAprilChip(byte ADC_counter_MSB, byte ADC_counter_LSB,
byte config_virtual_ground_node, byte config_potentiostat, byte config_tia_cap){
  // USE_C15_B, USE_C14_B, USE_C13_B, ... USE_C1_B, USE_C0_B,
  // |DISCONNECT_DSM_FB, CONNECT_I_ADC_IN_PAD, DISCONNECT_DSM_IN, DISCONNECT_POT_OUT,
  // CONNECT_VINT_ADC_PAD, CONNECT_EXTRA_INT_OUT|, |FLOAT_RE,FLOAT_CE|,
  // |DISCONNECT_CAP1,DISCONNECT_CAP2|
  // Serial.println("shifting data");

  shiftByte(config_tia_cap, 4);
  shiftByte(config_potentiostat, 4);
  shiftByte(config_virtual_ground_node, 64);
  shiftByte(ADC_counter_LSB, 256);
  shiftByte(ADC_counter_MSB, 256);

}
void shiftByte(byte transmitVal, int stopVal) {
  byte mask = 1; //our bitmask
```

```
  for (mask = 00000001; (mask>0)&&(mask<stopVal); mask <<= 1) {
  //iterate through bit mask
    if (transmitVal & mask){ // if bitwise AND resolves to true
      serialShift(1); // send 1
     // serialShift(1); //EXTRA FOR SOME REASON FOR SECOND SAMPLE
    }
    else{ //if bitwise AND resolves to false
      serialShift(0); // send 0
    }
  }
}
void testShiftRegister() {
  int mask = 1; //our bitmask
  bool flip = false;
  for (mask = 0; mask<64; mask++) {
    if (flip){
      serialShift(1); // send 1
      //serialShift(1); // EXTRA FOR SOME REASON NO IDEA WTF WHY
    }
    else{
      serialShift(0); // send 0
    }
    flip = !flip;
  }
}
void serialShift(int value)
{
  delay(1);
  if (value == 1){
       digitalWrite(SIN_DIN_3V3, HIGH);   // sets din signal high
  }
  else {
       digitalWrite(SIN_DIN_3V3, LOW);   // sets din signal low
  }
  delay(1);
  digitalWrite(SIN_CLK_3V3, HIGH);   // sets clk signal high
  delay(1);
  digitalWrite(SIN_CLK_3V3, LOW);   // sets clk signal low
```

```
  delay(1);
  digitalWrite(SIN_DIN_3V3, LOW);   // sets din signal low

}
void loadADCdataISR(){
  int i=0;
  int bitVal = 0;
  unsigned int outputVal = 0;
  digitalWrite(ADC_S_Lb_3V3, LOW);   // ensure that adc is loading parallel data
  digitalWrite(ADC_SOUT_CLK_3V3, HIGH); // clock in loaded data
  digitalWrite(ADC_SOUT_CLK_3V3, LOW);
  digitalWrite(ADC_S_Lb_3V3, HIGH);   // now serialize this data
  for (i=0; i<16; i++){
    bitVal = digitalRead(ADC_SDOUT_3V3);     // read the input pin
    outputVal = outputVal + (bitVal<<(15-i));
    digitalWrite(ADC_SOUT_CLK_3V3, HIGH); // clock in loaded data
    digitalWrite(ADC_SOUT_CLK_3V3, LOW);
  }
  digitalWrite(ADC_S_Lb_3V3, LOW);   // ensure that adc is loading parallel data
  ADC_OUTPUT_DATA = outputVal;
  ADC_OUTPUT_DATA_LOADED = 1;

}
void loop() {
  // put your main code here, to run repeatedly:
  if (ADC_OUTPUT_DATA_LOADED)
  {
    detachInterrupt(1);
    //for serial monitor
    Serial.println(ADC_OUTPUT_DATA);

    //for matlab
    //Serial.write(lowByte(ADC_OUTPUT_DATA));
    //Serial.write(highByte(ADC_OUTPUT_DATA));
    ADC_OUTPUT_DATA_LOADED = 0;
    ADC_OUTPUT_DATA=0;
    attachInterrupt(1, loadADCdataISR, RISING);
  }
```

```
}
```

Appendix E

Matlab Code for Chip 2

Below is various Matlab functions implemented to aid in the automated measurement of Chip 2.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [adcData,adcDataAverage] = readFromArdiuno(s,sampleAverage,ignoreSamples)
%format shorte;
%fclose(instrfind);

%while(s.BytesAvailable() > 0)
%    adcData=fgetl(s);
%end
adcData=zeros(1,sampleAverage);
for n = 1:sampleAverage+ignoreSamples
    adcDataRead=fgetl(s);
    if (n > ignoreSamples) %ignore first three read lines
        adcData(1,n-ignoreSamples) = str2double(adcDataRead);
    end
end
adcDataAverage =  mean(adcData);


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
function [ dout_Iin_matrix , dout_multi_samples_matrix] =
Chip2_stepped_current_measurement(prologix_com_port,
ardiuno_com_port,filename,min_current_val,max_current_val,currentStep,
adcSampleAverage)

format shorte;
fclose(instrfind);
fid = fopen(filename, 'w');
fprintf(fid,'%s,%s\n','Input_Current','Digital_Output_Bit_Value');

% Open serial port for prologix
s = serial(prologix_com_port);
set(s, 'DataBits', 8);
set(s,'StopBits', 1);
set(s,'BaudRate', 9600);
set(s,'Parity','none');
fopen(s);

%  Open serial port for arduino
s2 = serial(ardiuno_com_port);
set(s2, 'DataBits', 8);
set(s2,'StopBits', 1);
set(s2,'BaudRate', 115200);
set(s2,'Parity','none');
fopen(s2);
a='b';
while (a ~= 'a')
    a=fread(s2,1,'uchar');
end
fprintf(s2,'%c','a');


% Set mode as CONTROLLER
fprintf(s, '++mode 1');
% Set Keithly 6221 DC and AC source address
fprintf(s,'++addr 12');
%Turn off read-after-write to avoid "Query Unterminated" errors
fprintf(s,'++auto 0');
```

```
%Append LF to GPIB data
fprintf(s,'++eos 2');
%Assert EOI with last byte to indicate end of data
fprintf(s,'++eoi 1');

%Construct Commands to Keithley Device
% Enable remote mode (REN)

%time.sleep(1.0)



% CLEAR
cmd = 'CLEAR'
fprintf(s,cmd);
% CURRent:RANGe:AUTO ON
cmd = 'CURRent:RANGe:AUTO ON'
fprintf(s,cmd);
% CURRent:COMPliance 1
cmd = 'CURRent:COMPliance 1'
fprintf(s,cmd);


dout_Iin_matrix = zeros(length(min_current_val:currentStep:max_current_val),2);
dout_multi_samples_matrix = zeros(1,adcSampleAverage + 1,
     length(min_current_val:currentStep:max_current_val));

n=1;
adcData = 0;
adcDataAverage=0;
%loop i++ (10pA++)
for i = min_current_val:currentStep:max_current_val
    %   CURRent i (in amps)
    cmd = ['CURRent ' ' ' num2str(i)]
    fprintf(s,cmd);

    %   OUTPUT ON
    cmd = 'OUTPUT ON';
```

```
    fprintf(s,cmd);
    %   READ FROM CHIP
    %pause(1);
    flushinput(s2);
    [adcData, adcDataAverage] = readFromArdiuno(s2,adcSampleAverage,2);
    %pause(1);

    %   OUTPUT OFF (DONT DO THIS FOR NOW BECAUSE OF TRANSIENTS)
    %cmd = 'OUTPUT OFF';
    %fprintf(s,cmd);

    %store into array
    rowData=[i adcDataAverage]
    dout_Iin_matrix(n,:) = rowData;
    dout_multi_samples_matrix(1,1,n) = i;
    dout_multi_samples_matrix(1,2:end,n) = adcData;

    fprintf(fid,'%d,%f\n',i,adcDataAverage);
    n=n+1;
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

cmd = 'OUTPUT OFF';
fprintf(s,cmd);
% CLEAR
cmd = 'CLEAR'
fprintf(s,cmd);
fclose(s);
fclose(fid);
fclose(s2);

end

format shorte;
fclose(instrfind);
prologix_com_port='COM7';
filename='Noise_shaping_plot_100nA_14bit_sample2.csv'
%fid = fopen(filename, 'w');
```

```
%fprintf(fid,'%s,%s\n','Input_Current','Digital_Output_Bit_Value');

% Open serial port for prologix
s = serial(prologix_com_port);
set(s, 'DataBits', 8);
set(s,'StopBits', 1);
set(s,'BaudRate', 9600);
set(s,'Parity','none');
set(s,'InputBufferSize',2000000);
fopen(s);



% Set mode as CONTROLLER
fprintf(s, '++mode 1');
% Set Agilent MSO6052A address which is set on the scope itself
fprintf(s,'++addr 7');
%Turn off read-after-write to avoid "Query Unterminated" errors
fprintf(s,'++auto 1');
%Append LF to GPIB data
fprintf(s,'++eos 2');
%Assert EOI with last byte to indicate end of data
fprintf(s,'++eoi 1');

%Construct Commands to Keithley Device
% Enable remote mode (REN)

%time.sleep(1.0)

flushinput(s);
flushinput(s);
flushinput(s);
cmd = ':WAVeform:SOURCE CHAN2';
fprintf(s,cmd);

cmd = ':Acquire:type NORMAL';
fprintf(s,cmd);
```

```
cmd = ':WAVeform:POINts:MODE RAW';
fprintf(s,cmd);

cmd = ':WAVeform:POINts RAW';
fprintf(s,cmd);


cmd = ':WAVeform:FORMAT BYTE';
fprintf(s,cmd);


cmd = ':SINGLE';
fprintf(s,cmd);
pause(5);

cmd = ':Acquire:Srate?';
fprintf(s,cmd);
srate = fgetl(s)

cmd = ':WAVeform:POINts?';
fprintf(s,cmd);
size_waveform=fgetl(s)
size_waveform=str2num(size_waveform);


M=zeros(1,size_waveform);

done=0;


cmd = ':WAVeform:Data?';
fprintf(s,cmd);
header=fscanf(s,'%s',10)

for i=1:size_waveform
    M(1,i)=fread(s,1);
end
```

```
mid=(max(M) - min(M))/2+min(M);
M2 = M > mid;
M2 = double(M2);
M2(M2<.5) = -1;
csvwrite(filename,M2');
fclose(s);


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

res=14
fbin = 2;


%FFT of input data
mid=(max(M) - min(M))/2+min(M);
M2 = M > mid;
M2 = double(M2);
M2(M2<.5) = -1;
t=size(M2);
N=t(1,2);
OSR = 2^15;
% compute windowed FFT and NBW
w = hann(N).^2; % or ones(1,N) or hann(N).^2
nb = 5; % 1 for Rect; 5 for Hann.^2
w1 = norm(w,1);
w2 = norm(w,2);
NBW = (w2/w1)^2;
V = fft(w.*M2')/(w1)*1;
% Compute SNR
signal_bins = fbin + [-(nb-1)/2:(nb-1)/2];
inband_bins = 0:N/(2*OSR);
noise_bins = setdiff(inband_bins,signal_bins);
snr = dbp( sum(abs(V(signal_bins+1)).^2) / sum(abs(V(noise_bins+1)).^2))
% Make plots
figure(1); clf;
semilogx([1:N/2]/N,dbv(V(2:N/2+1)), 'b', 'Linewidth' ,1);
```

```
hold on;
[f p] = logsmooth(V,fbin,1,nb);
%plot(f,p, 'm', 'Linewidth' ,1.5)
%Sq = 4/3 * evalTF(ntf,exp(2*pi*f)).^2;
%plot(f,dbp(Sq*NBW), 'k--', 'Linewidth',1)
figureMagic([1/N 0.5],[],[], [-140 0], 10 , 2);
title(strcat('Noise-shaping PSD with 100nA DC input with BW=1MHz/2\^',num2str(res)));
xlabel('Normalized Frequency (f)') % x-axis label
ylabel('PSD (dBFS/NBW)') % y-axis label

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [adcData,adcDataAverage] = setupSerial(s,comPort)
%format shorte;
%fclose(instrfind);

%while(s.BytesAvailable() > 0)
%    adcData=fgetl(s);
%end
adcData=zeros(1,sampleAverage);
for n = 1:sampleAverage+3
    adcDataRead=fgetl(s);
    if (n > 3) %ignore first three read lines
        adcData(1,n-3) = str2double(adcDataRead);
    end
end
adcDataAverage =  mean(adcData);
fclose(s);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

Appendix F

Test PCB schematic for Chip 3

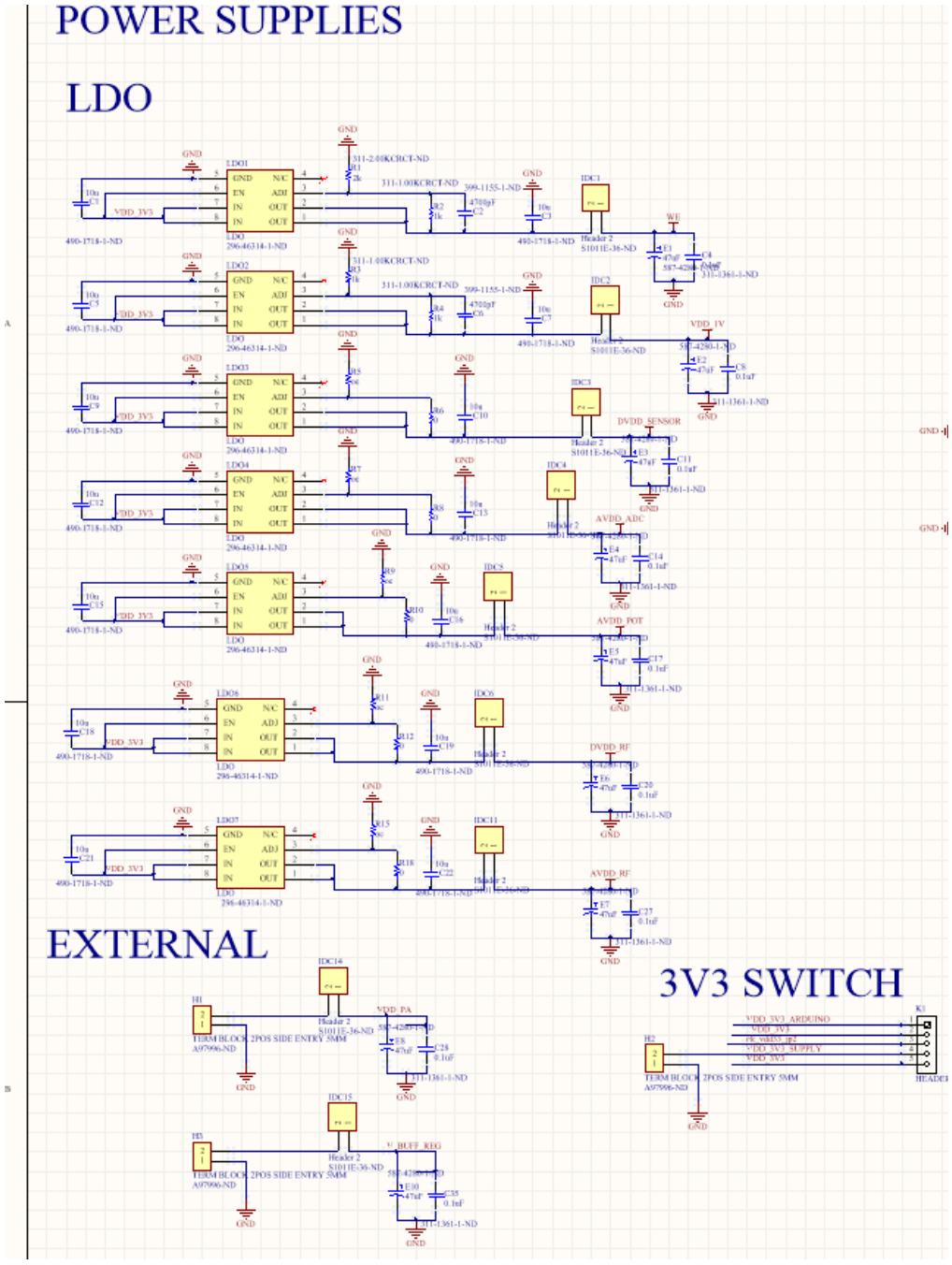

Figure F.1: Regulation and Power into Chip 3 Test PCB.

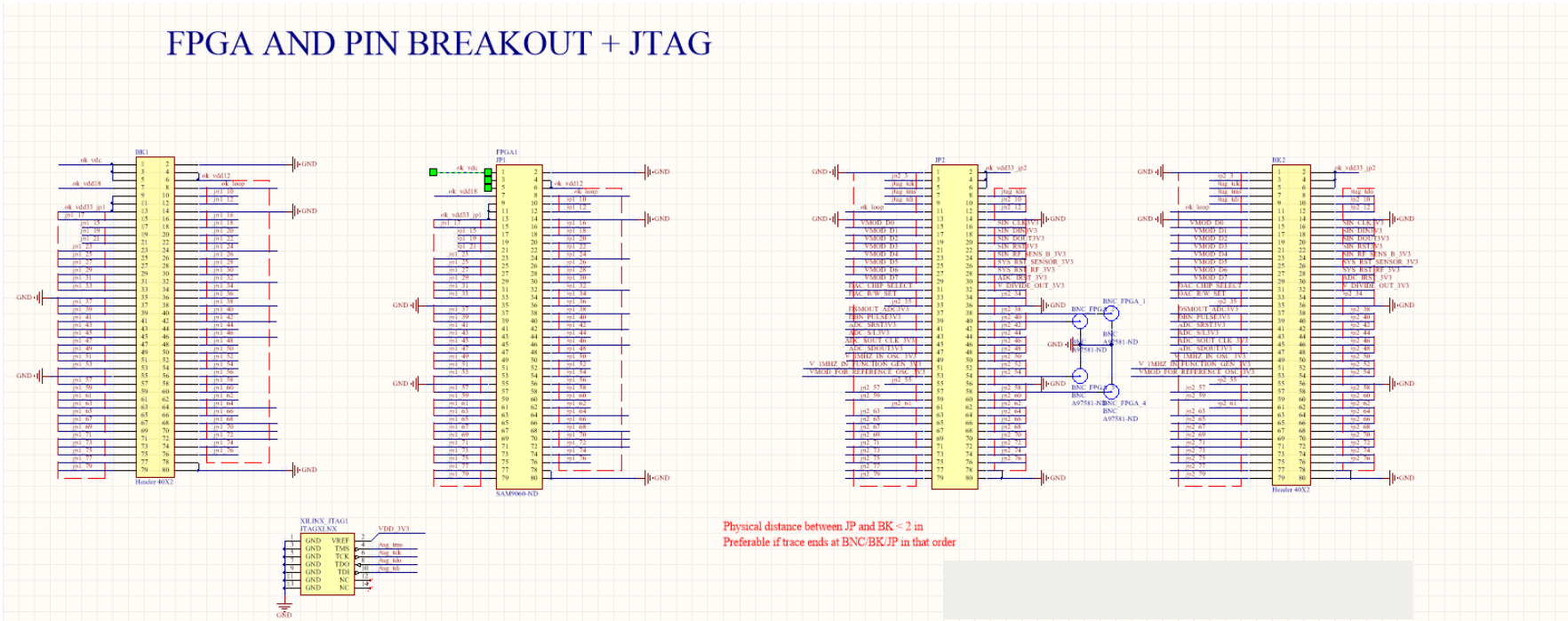

Figure F.2: Opal Kelly FPGA input to Chip 3 Test PCB.

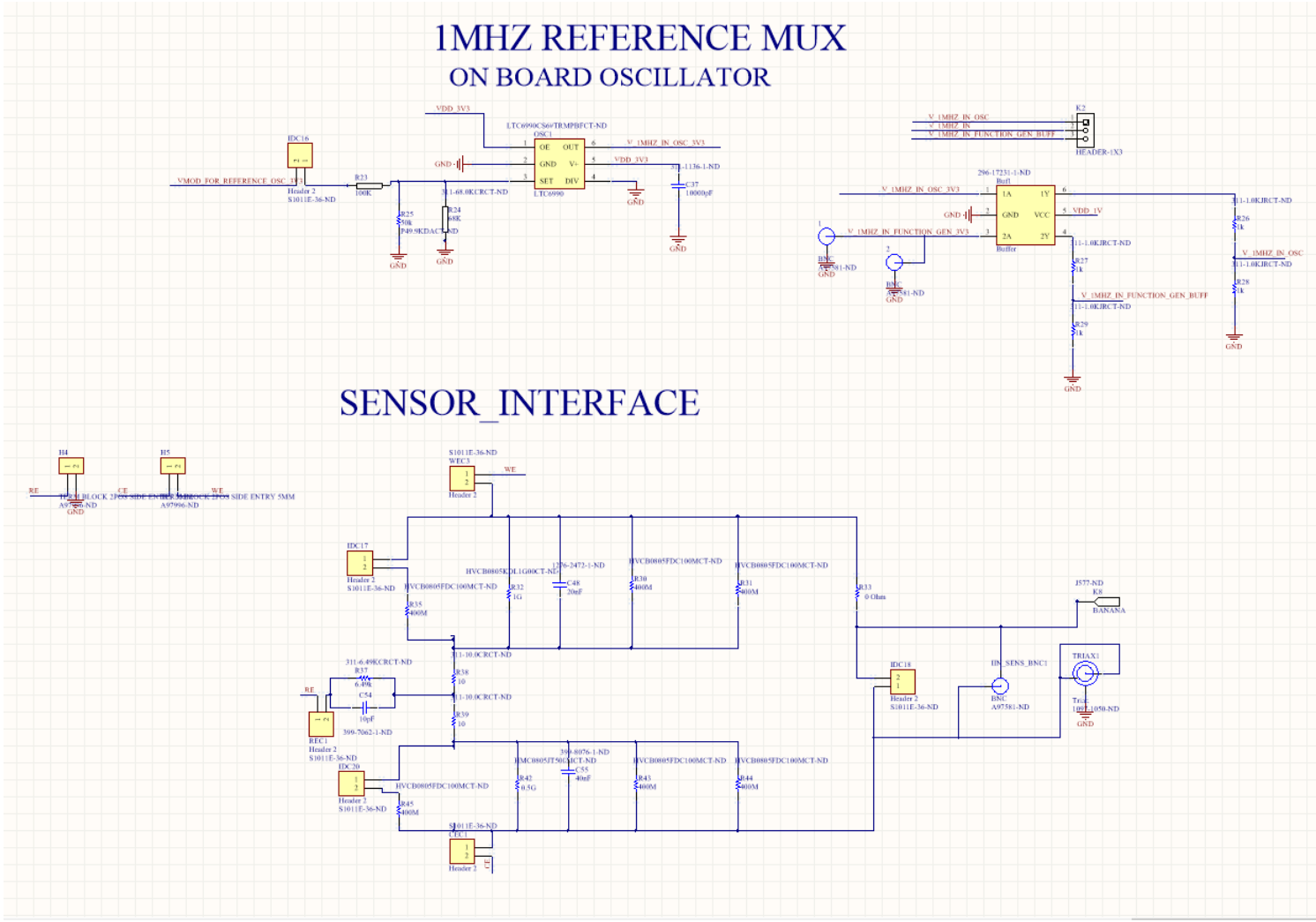

Figure F.3: On-board reference oscillator and sensor electrical model used on Chip 3.

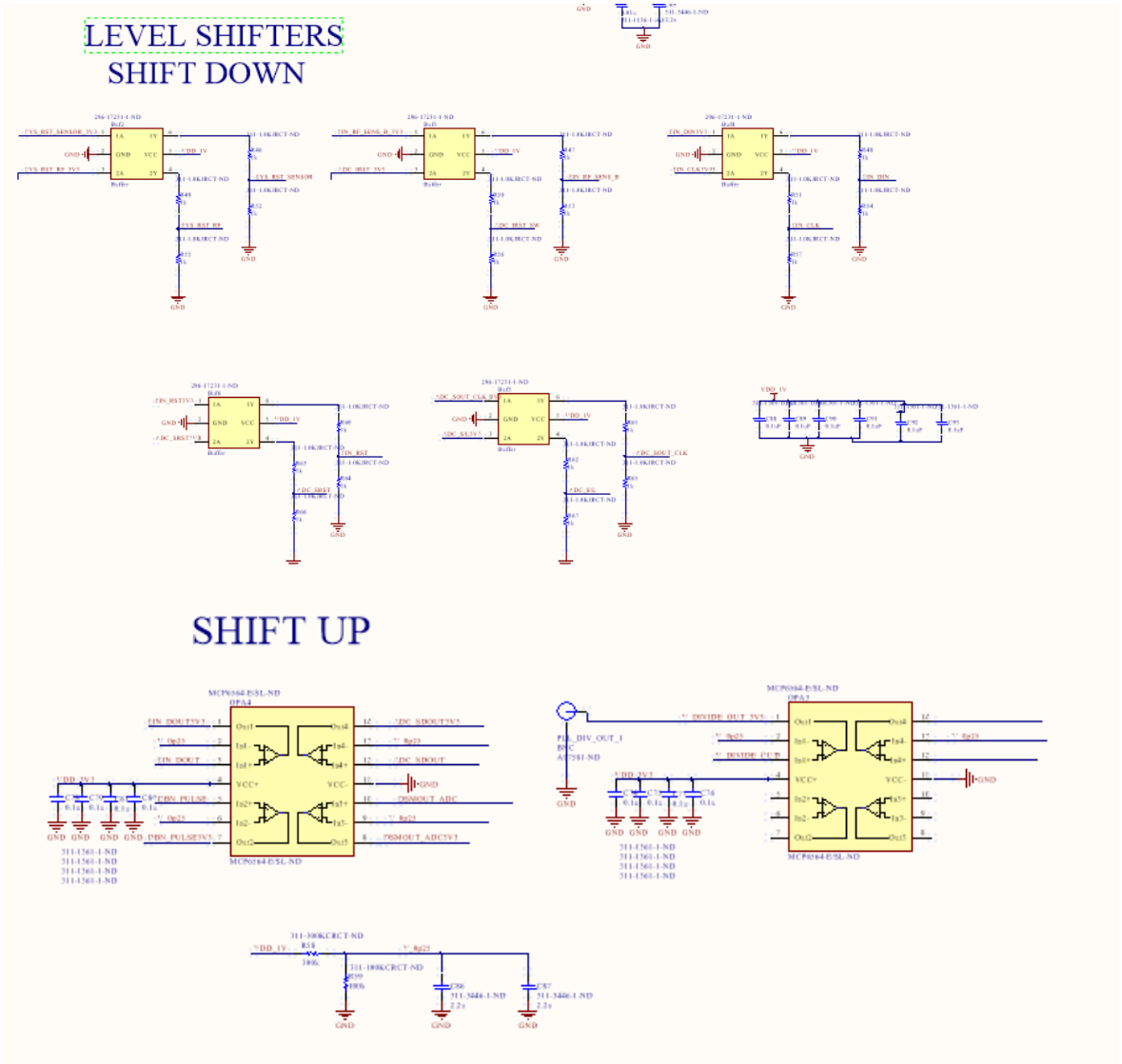

Figure F.4: Level Shifters for input/output data to/from Chip 3.

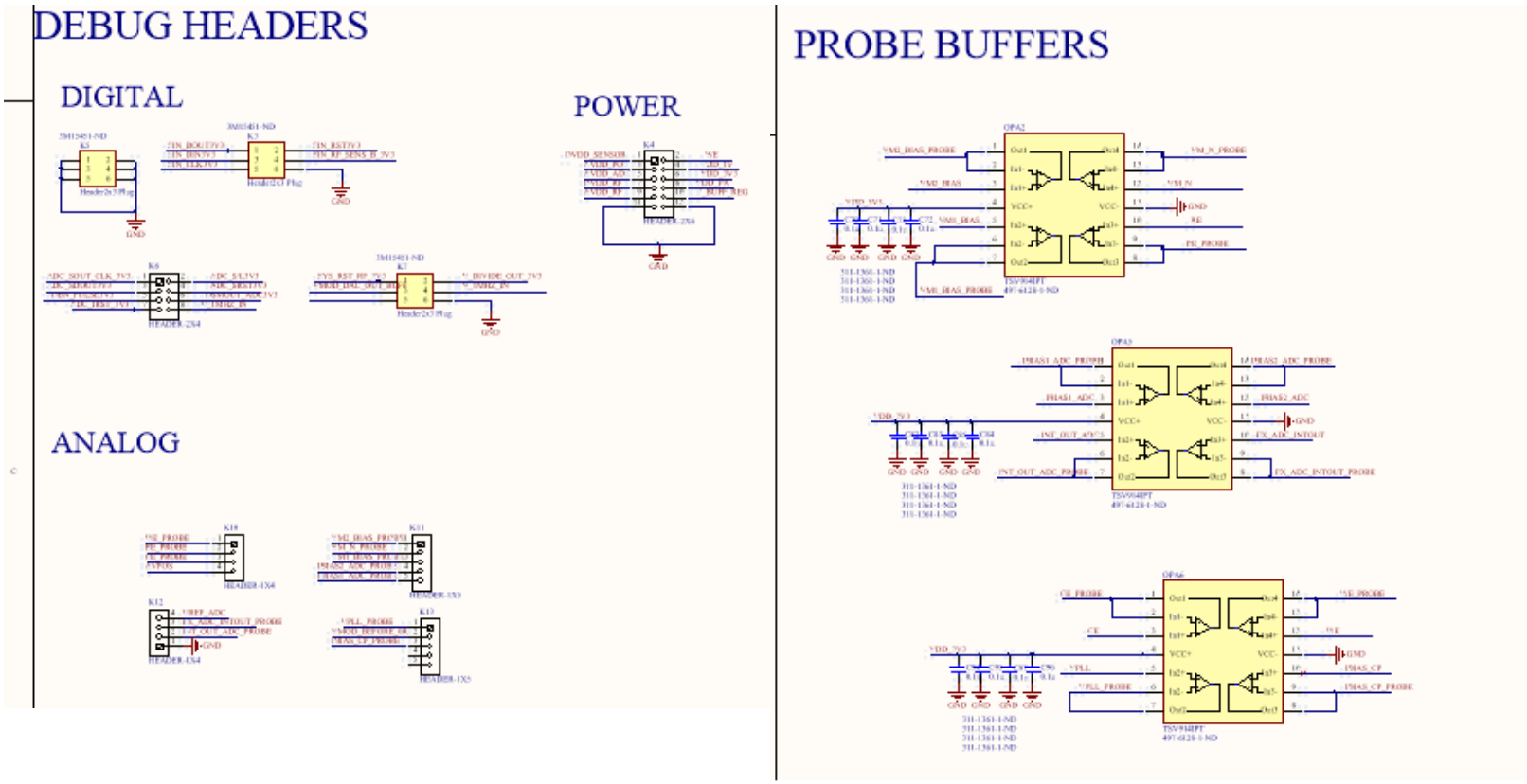

Figure F.5: Debug inputs/outputs on Chip 3 Test PCB.

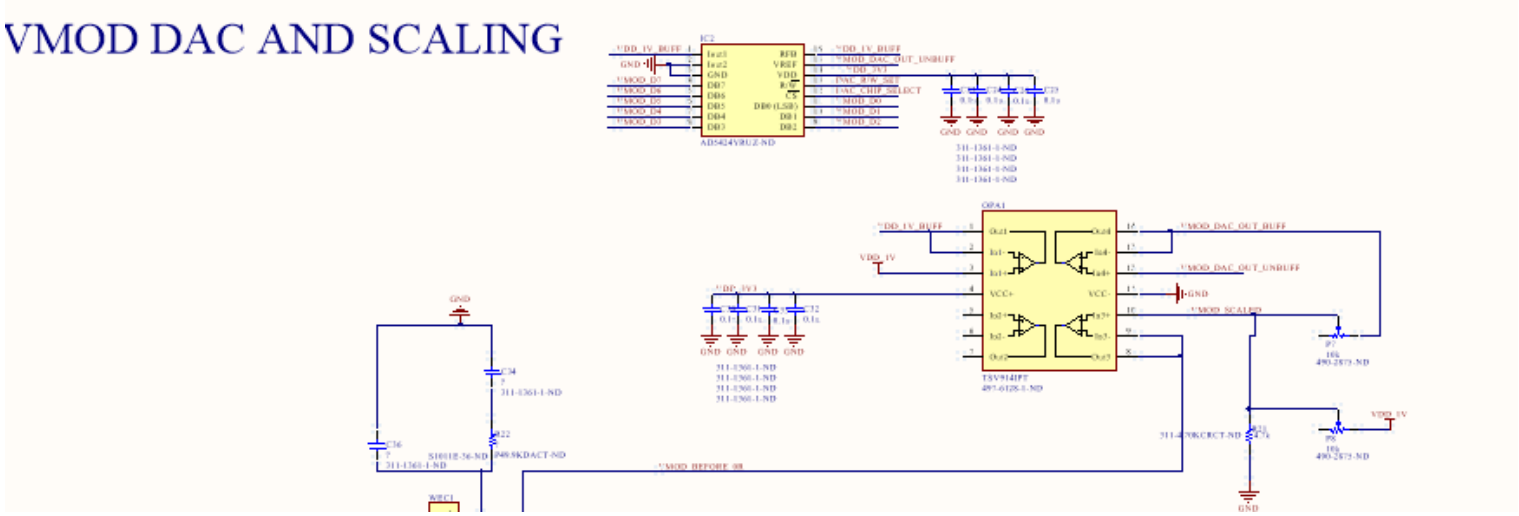

Figure F.6: DAC used to drive Bluetooth modulator on Chip 3 from the FPGA.

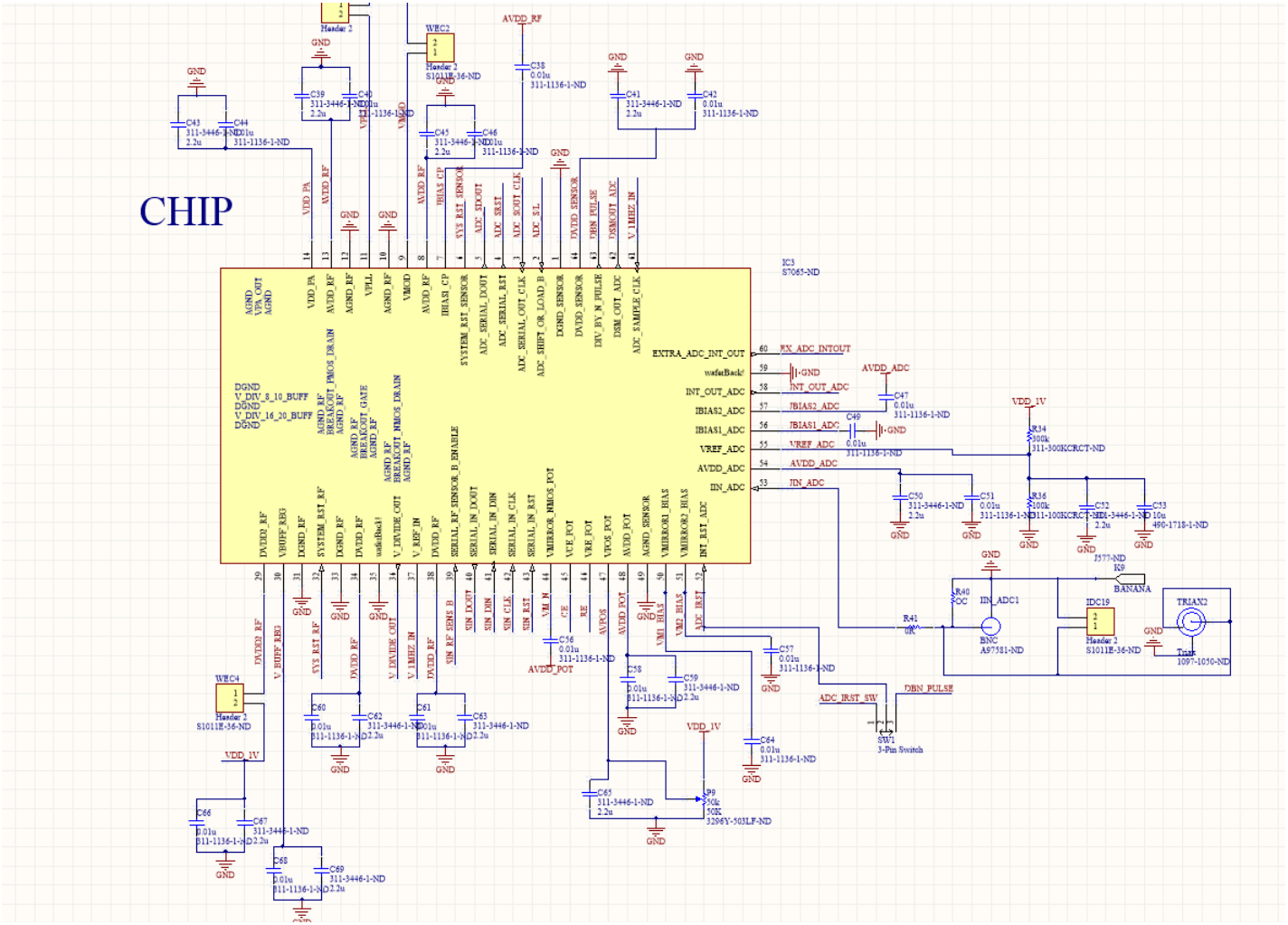

Figure F.7: Chip 3 with associated supply decoupling.