Two Port Network Theory Based Design Method of Broadband Doherty Power Amplifier

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

LTE-Advanced (LTE-A) is a widely used communication standard and it mainly features Carrier aggregation (CA). CA increases the user data rate and efficiently exploits the fragmented spectrum by combining various carrier frequencies. The intrinsic multi-band and multi-standard of CA, along with the existing high peak-to-average power ratio (PAPR), brings the challenges of broadband requirement and back-off (BO) efficiency enhancement when designing radio frequency power amplifiers (PA). The above two challenges inspire research interest in designing of broadband Doherty power amplifiers (DPAs), which maintain the high efficiency at BO power level and perform constantly versus frequency.

In this work, the continuous design space was discussed. Output combining and matching network (OCMN) and its impact on the impedances shown to the two transistors were analyzed based on two port network theory. ABCD parameters of matching networks was formulated to accommodate continuous class-B (class-J) operation to DPAs. Second harmonic was terminated to avoid clipping and efficiency degradation. By enlarging design space, the bandwidth was substantially expanded. The proposed design methodology allowed the adsorption of parasitics which was the one of the bandwidth limiting factor.

To validate the proposed methodology, an 8 Watts DPA was simulated to operate from 3 GHz to 5 GHz using Cree Gallium nitride (GaN) High-electron-mobility transistors (HEMTs). And simulation results showed that the 6dB BO efficiency was above 40% and Peak-envelope-power (PEP) of 50% over the frequency range of 3GHz to 5GHz.

The Doherty power amplifier prototype is fabricated on substrate of Rogers4003C and assembled in house. Continuous wave measurement showed that the PA could provide 8.2 - 10.6 dB gain in the frequency band of 2.7 to 4.3 GHz. The 6 dB back off efficiency was 40% to 43%. And at peak power, the drain efficiency reached 48% to 60%. 80 MHz inter-band modulated signal and 15MHz dual band signal measurement were carried out to investigate the linearizability. In the inter-band measurement, average power around 33dBm and average drain efficiency of 46% was obtained with PAPR of 6.4 dB. ACLR above 48.7 dBc after DPD verified the easiness of linearization for this PA. Dual band measurement using two carriers at 2.8 and 3.2 GHz showed even when the PAPR of two band were 7.6 and 8.0 dB separately, average power of 32.3 dBm power can still be extracted with average

efficiency of 40.5%. ACLR of 49.5 and 46.7 dBc of those two bands were good endorsement of the capability of inter-band concurrent amplification.

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Chapter 1

Introduction

1.1 Motivation

The modern wireless communication need to be able to manage higher data throughput to fulfill the increasingly high demand of multimedia services, which, accordingly, requires the emerging wireless network to support modulation schemes with high spectrum-efficiency and wide-band signals. Those newly adopted communication standards, such as Long Term Evolution (LTE), and existing legacy Wide-band Code Division Multiple Access (WCDMA) employ carrier aggregation (CA) to achieve better utilization of the fragmented spectrum. Fig 1.1 shows the three scenarios of carrier aggregation, (a) intro-band, contiguous, (b) intro-band, non-contiguous, and (c) inter-band, non-contiguous. The application of carrier aggregation causes large fluctuation in the envelope of signal waveform, i.e. large peak-to-average-power-ratio (PAPR). This characteristic of signals brings new design challenges for the transceivers, especially for the radio-frequency power amplifiers (RFPAs). First of all, as is shown in Fig 1.2(a and b), the transmitted signal is most likely at much lower power level compared with its peak value and possibility density analysis gives corresponding statistical illustration. That is to say, RFPAs will be operating in the low-efficiency region in a substantial period of time. Secondly, more strict linearity requirement has been put forward to avoid severe adjacent channel interference caused by leakage. As a consequence, RFPAs must be further backed off from its peak power level to operate linearly.

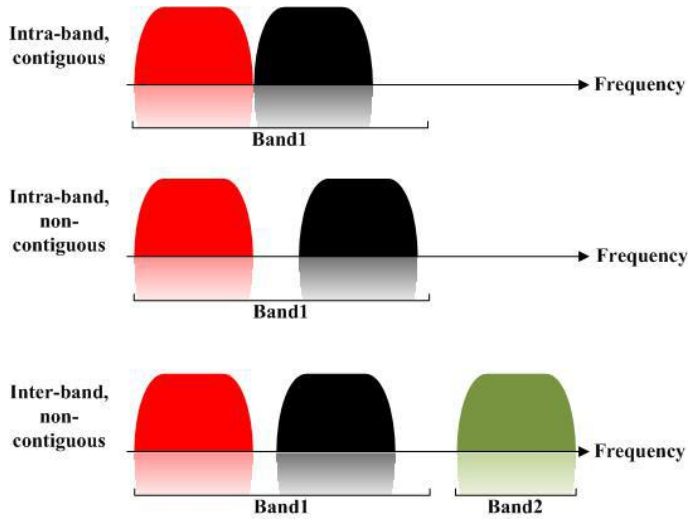


Fig 1.1: Three scenarios of carrier aggregation

An ideal class-B power amplifier is a good compromise between drain efficiency and linearity and could provide as high efficiency as 78.5% but only at the peak power level. At 6dB back-off (BO) power level, the efficiency is only 38%, 41% lower than maximum value. The degradation in efficiency will result in more power dissipated in form of heat and shortens the service life of devices. The heat caused by the lowered efficiency could increase the ambient temperature, which decreases the mobility of carriers and leads to further efficiency degradation, forming a vicious circle.

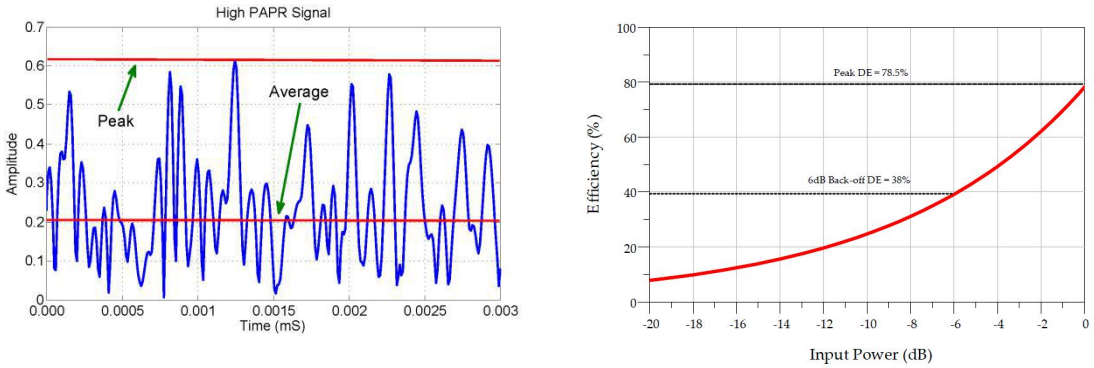


Fig 1.2: High PAPR signal and back off efficiency degradation [38] [9]

In addition, the employment of carrier aggregation is demanding in broadband or multi-standard concurrent operation of RFPAs since they have to amplify different signals in wide-spread carrier bands.

In conclusion, in frame of the modern wireless communication standards, power amplifier design is more challenging in terms of back-off power level efficiency, fractional bandwidth (FBW) and linearity.

1.2 Problem Statement

The PA is the most power consuming stage in the transceiver chain and thus is decisive in terms of the overall efficiency. Different methods have been studied to enhance the efficiency, including the reduction of conduction angle (class-B, class-AB, class-C, and class-J), harmonic tuned (class-F, class-F^{-1}, and their continuous mode), switch mode operation (class-E), and other operation modes derived from the above (push-pull, and class-S etc). Operating under those modes, the PAs could provide efficiency approaching 100% in theory but only at peak power level. While at back off power level, the efficiency drops remarkably with no exception.

To address the back-off efficiency degradation problem, several approaches have been proposed. Envelope tracking (ET) [5] increases the back-off efficiency by adaptively tuning DC power supply according to the input signal envelope waveform. In spite of the perfectness in theory, it is difficult to implement ET since it requires the envelope amplifier to be highly efficient, accurately controlled to be in-phase with input signal envelop, and have high speed when applied in broadband operation. Linear amplification using non-linear components (LINC) [7] first transfers amplitude-modulated signals into phase-modulated signals. The phase-modulated signals will then be efficiently amplified by RFPAs operating in high efficiency and poor linearity mode. The amplified signals is then restored to be amplitude-modulated at the output stage through power combining devices. In the frame of this technique, back-off efficiency drop issue is eliminated since signals to be amplified have no amplitude variation. Although this theory seems to be attractive and brings another possible solution, when realized, the efficiency and linearity is deteriorated by the combiner bandwidth, combiner isolation, precision of input power division, and bandwidth of PAs, etc.

Among all of those approaches toward back off efficiency enhancement, the Doherty power amplifier (DPA) keeps to be a research focus and wins out in commercial application. This is because DPA is linear amplifier intrinsically and easy to implement. Even though conventional DPA suffers from bandwidth limitation, it can be modified to exploit the good potential toward broadband operation.

During the past few years, the extension of the operation bandwidth of DPA has become a hotspot. Using asymmetrical biasing [13], the impedance profiles were allowed to be modified and impedance transformation ration for main amplifier was adjusted to be unit at back-off. Following this method, the designed DPA maintained efficiency above 50% in the range of 0.7 to 1GHz (FBW: 36%). As can be seen, the asymmetrical biasing increased the implementation complexity. And even though the bandwidth at back-off was extended, the bandwidth at peak-envelope-power (PEP) was sacrificed. Besides, the adsorption of parasitics into inverter can be done only in a limited bandwidth, which formed another bandwidth limiter. Push-Pull DPA using broadband balun as power combiner [25] could provide good second harmonic termination and octave operation bandwidth (600MHz to 1400MHz) was achieved because of the intrinsic wideband property of Push-Pull power amplifier unit and baluns. But the total four transistors used in the design, compared with only two transistors in conventional Doherty power amplifier, increased the design complexity and the baluns were only applicable at lower frequency.

In this thesis, a novel methodology for output combining and matching network (OCMN) design has been proposed to accommodate continuous class-B operation to DPAs to extend operation frequency bandwidth. The methodology proposed could tackle the bandwidth limitation caused by parasitics and provide the second harmonic termination required by broadband continuous mode operation. Due to the proper termination of 2^{nd} harmonic and absorption of parasitics the designed DPA maintained high efficiency above 40% at 6dB back-off and above 45% at PEP in the frequency range of 3 to 5GHz.

1.3 Thesis Organization

The organization of this thesis is as follows. In Chapter 2, the basic PA operation modes are introduced. The continuous class-B, suitable for broadband operation, is detailed. Following is the operation analysis of Doherty power amplifier, which is the focus of this thesis. This chapter is ended with a literature review including the past research and state of art implementation of DPAs.

In Chapter 3, the novel design methodology is presented which forms the core the thesis. The methodology, based on the two port network theory, solves the broadband matching problem for DPAs operating in a broadband continuous mode. Theoretical details are given. Absorption of parasitics is also detailed and 2^{nd} harmonic termination problem is also addressed in the implementation of the deduced network parameters. A DPA as proof of concept using this methodology is designed, simulated and measured and results are reported in chapter 4. Chapter 5 will conclude the thesis with a summary of the contribution and an expectation of the future work.

Chapter 2

Conventional Power Amplifier Overview

In this chapter, the basic concepts, various PA operation modes, advanced technique (continuous class-B), and back-off efficiency enhancement (DPA) will be discussed. At the end, the literature review and comparison table will be provided to summarize the previous research progress.

2.1 Basic Concepts

The power amplifier plays a significant role in the transmitter and is decisive in terms of the overall efficiency. It consumes DC power and transforms it into RF power proportional to the small input power. The output RF power will be large enough to be transmitted through antennas. The power amplification is described by the gain (transducer gain)

$$G = \frac{P_{del}}{P_{avs}} \tag{2.1}$$

where the P_{del} is the RF power delivered to the load in Watts and P_{avs} is the power available from the source in Watts. Since the PA consumes most DC power, its efficiency also determines the overall efficiency of the transmitter. There are two merits defined to describe the efficiency of DC to RF power transformation, the drain efficiency (*DE*) and power added efficiency (*PAE*)

$$DE = \eta = \frac{P_1}{P_{DC}} \tag{2.2}$$

where the P_{DC} denotes the DC power consumption in Watts and P_1 is the power delivered to the load at fundamental frequency also expressed in the unit of Watts. To reflect the gain in the efficiency expression, the power added efficiency is defined as

$$PAE = \frac{P_1 - P_{avs}}{P_{DC}} = \eta \times (1 - \frac{1}{G}) \tag{2.3}$$

As can be figured out in Equation (2.3), when the gain is large, the contribution of P_{avs} to the total efficiency is negligible and the *PAE* will approach *DE*.

2.2 Operation Mode of Power Amplifiers

Power amplifiers can be operating in different modes. If the transistors are used as the voltage-controled-current-sources (VCCSs), the operation modes can be categorized as class-A, AB, B (or continuous class-B), C, and F (or continuous class-F) based on the biasing point at the input and termination at the output. When the transistors are used as switches, the corresponding operation mode could be class-E or class-F^{-1}. Details will be given in the following

2.2.1 Class-A Operation Mode

Field effect transistor (FET) is the dominant technology in base-stations at present. To simplify the analysis, the transistors are modeled as a voltage-controlled-current-source. As is shown in Fig 2.1, the idealized transistors sense gate voltage V_{gs} and output drain current I_{ds} through the constant transconductance g_m within the linear region. In power amplifiers, the transistors are excited by large signals and maximally allowed voltage and current swings are utilized to exploit power capacity. So parameters describing the large signal behaviors of transistors are defined in Table 2.1. The nonlinear characteristics of transistors can be roughly captured by the abrupt turn-on when Vgs exceed threshold voltage V_{th} and the sudden flatness of I_{ds} when driving level reaches $V_{gs,max}$. The transfer function is indicated in Fig 2.2. In the simplified model, all parasitics are neglected and input and output impedances are both infinite. So the devices are unilateral and its behaviors are frequency-independent which can be fully depicted by the DCIV curve.

Table 2.1: Large signal transistor parameters

Parameter	Definition
V_{knee}	Knee voltage, minimally allowed drain voltage
V_{th}	Threshold voltage, minimum gate voltage for transistor to conduct
I_{max}	The maximum current that can be drawn from drain
V_{max}	Highest tolerable drain voltage before break-down
g_m	Transconductance
$V_{gs,max}$	Gate voltage that drives transistor to provide maximum drain current

Class-A is the operation mode when the gate voltage is the middle-way between V_{th} and $V_{gs,max}$. The input AC voltage could have the magnitude of $(V_{gs,max}-V_{th})/2$ so the input voltage could swing as low as V_{th} and as high as $V_{gs,max}$. According to the transfer function and DCIV curve, the output current will contain a quiescent component of $I_{max}/2$ and an AC component in magnitude of $I_{max}/2$. To maximize the output power, the instantaneous output voltage should also cover the full range from

V_{knee} to V_{max}, meaning that the voltage at the output contains a quiescent component of $V_{max}/2$ and single-tone AC component in magnitude of $V_{max}/2$. In that case, the optimum load R_{opt} is derived.

$$R_{opt} = \frac{V_{max}/2}{I_{max}/2} \quad (2.4)$$

Under the operation mode of class-A, the transistors are conducting during the whole period even when there is no AC signals. The DC power consumption is

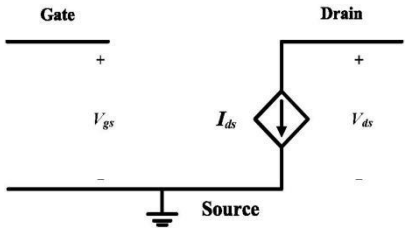
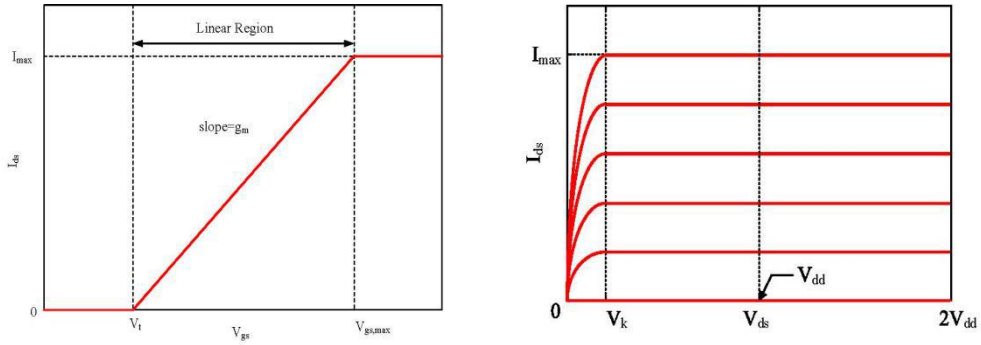


Fig 2.1: VCCS as transistor ideal model



(a) I_{ds} versus V_{gs} (b) I_{ds} versus V_{ds}

Fig 2.2: Transconductance and DCIV characterization of transistors

$$P_{DC,A} = \frac{V_{max} \times I_{max}}{4} \quad (2.5)$$

The output power and drain efficiency of class-A are dependent on the output power level and their theoretical maximum values are

$$P_{out,A} = \frac{1}{2} \times \frac{V_{max} \times I_{max}}{4} \quad (2.6)$$

$$\eta_A = \frac{P_{out,A}}{P_{DC,A}} = 50\% \qquad (2.7)$$

The above analysis is based on an assumption that V_{knee} is negligible. In practice, the non-zero V_{knee} and back-off operation will further decrease the efficiency.

Obviously, the transistor stays in the active region and conducts drain current in the whole cycle. As a consequence, the gain is predictably high. Transistors operating in class-A mode will neither intrude the cut-off region nor saturate the output current. So class-A is a linear operation mode, i.e. ideally no harmonics are generated, and thus suitable for wide-band operation and low-noise amplification. However, power amplifier under this operation mode could not reach an efficiency higher than 50% and accordingly, the application is narrowed.

2.2.2 Reduced Conduction Angle Operation Mode

The relatively low efficiency of class-A power amplifier is the result of two reasons, whole cycle conduction and the independence of DC power consumption to output power level. By reducing the conduction angle, those two reasons would disappear. The conduction angle is defined to be the fraction in a whole cycle in which the transistor is conducting current. And it can be reduced by lowering the V_{gs} biasing point. Fig 2.3 shows drain current waveforms for reduced conduction angle operation mode. The conduction angle 2π for class-A, π for class-B, any values between π and 2π is defined as class-AB, and class-C corresponds to conduction angle below π.

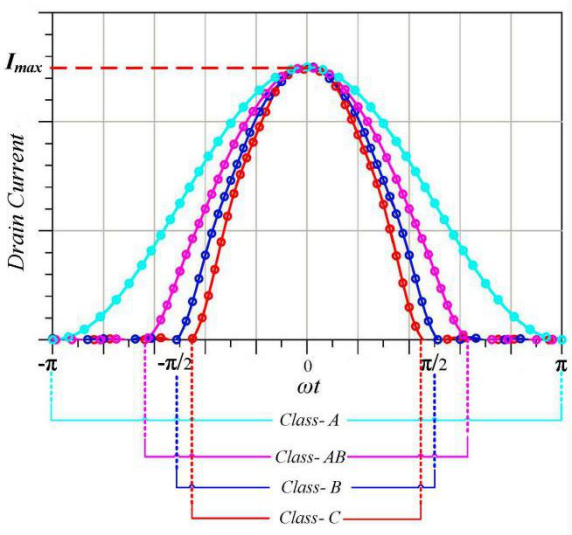


Fig 2.3: Reduced conduction angle operation modes

Conduction angle is reduced by lowering the gate biasing voltage. Before the gate could swing above V_{th}, drain current is zero. So one section of the load line lies on abscissa axis indicating that there is no DC power consumption in this period of time. As the conduction angle decreases, transistor conducts in shorter period and the abscissa axis section of load line is enlarged. As is shown in Fig 2.4, the crossover point of load line with V_{ds} axis further to left for smaller conduction angle and thus less DC power consumption.

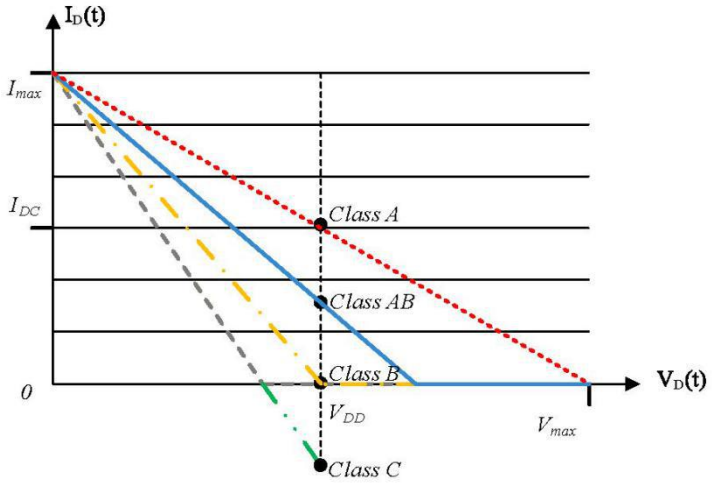


Fig 2.4: Load lines for reduced conduction angle modes

When the conduction angle is reduced, the drain current, as will be seen from Fourier transformation, contains fundamental as well as harmonics. In the conventional reduced conduction angle modes, all the harmonics are short-circuited, and fundamental current component will see a purely resistive load. Numerical analysis is given to reveal the efficiency improvement by reducing the conduction angle. For the purpose of simplification, it is assumed that knee voltage is zero, and transistors are turned on and off abruptly. Still, to maximize the output power, the drain current could always reach I_{max} in spite of the variation in conduction angle.

The waveform of drain current is described by the following equations

$$I_{ds}(\theta) = \begin{cases} 0, & -\pi \le \theta < \frac{\alpha}{2} \\ \frac{I_{max}}{1-\cos\left(\frac{\alpha}{2}\right)} \times \left[\cos(\theta) - cos\left(\frac{\alpha}{2}\right)\right] & -\frac{\alpha}{2} \le \theta < \frac{\alpha}{2} \\ 0, & \frac{\alpha}{2} \le \theta < \pi \end{cases} \quad (2.8)$$

where α denotes the conduction angle and $\theta=\omega t$.

Using Fourier transformation, magnitude of different components can be found. Since the 2nd and higher harmonics are assumed to be shorted, only the DC component and fundamental component are considered here as

$$I_{DC} = \frac{I_{max}}{2\pi} \times \frac{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cos\left(\frac{\alpha}{2}\right)}{1 - \cos\left(\frac{\alpha}{2}\right)} \quad (2.9)$$

$$I_1 = \frac{I_{max}}{2\pi} \times \frac{\alpha - sin\,(\alpha)}{1 - \cos\left(\frac{\alpha}{2}\right)} \quad (2.10)$$

and accordingly the DC power consumption, output power and efficiency can be derived as the following

$$P_{DC} = I_{DC} \times V_{DD} \quad (2.11)$$

$$P_{out} = \frac{1}{2} \times \frac{V_1 \times I_1}{P_{DC}} \quad (2.12)$$

$$DE = \frac{P_{out}}{P_{DC}} \quad (2.13)$$

As is implied in Equation 2.11, the optimum impedance to maximize output power is

$$Z_1 = R_{opt} = \frac{V_{DD}}{I_1} \quad (2.14)$$

because the drain voltage waveform is sinusoidal and in magnitude of $V_1 = V_{DD}$, which is the maximally allowed value to avoid clipping.

The above analysis reveals that the output power and the drain efficiency is a function of conduction angle α. Reduced-conduction-angle principle represents the generalization of operation modes in which the harmonic currents are ideally short circuited and fundamental current is terminated with a purely resistive load to fully utilize the voltage the swing and thus maximize the output power. The class-A operation mode which requires the transistor to conduct in the whole cycle, corresponds to a conduction angle of 2π. This leads to the previously predicted efficiency of 50%. Transistors operating under class-B mode conducts only half of the cycle and the conduction angel is π. The efficiency is

$$DE^B = \frac{\pi}{4} = 78.5\% \quad (2.15)$$

Compared with class-A operation mode, class-B could provide an increased drain efficiency. Unlike class-A in which the DC power consumption is constant, in class-B mode both output power and DC power consumption varies linearly with the input power, so back-off efficiency drop is less remarkable for class-B, and especially, when RF input power is zero, the DC power consumption is also zero. Because of the lowered biasing point at the gate, more input power will be needed to push the transistor into saturation so the gain is relatively lower. Meanwhile, the transistors are turned on and off alternatively in one cycle so both the nonlinearity of transconductance and nonlinearity of input C_{gs} will distort output current waveform, leading to an undermined linearity of the power amplifier.

Operation modes with conduction angle between π and 2π is defined as class-AB, and when the transistors are gate biased even lower than class-B, the operation mode is class-C. In addition to nonlinearity problems mentioned in class-B, the class-AB and class-C also suffer from their intrinsic nonlinearity issue caused by variation of conduction angle versus input power level. For class-C, the conduction angle expands and approaches class-B mode when the input power level increases. The gain will show expansion. But for class-AB, the conduction angle shrinks versus input power level and the gain will show compression even if the nonlinearity of transconductance and C_{gs} are neglected.

To ensure the drain current could reach I_{max}, more power will always be need to drive the transistor when biasing point is lower. So the achievable gain is decreased as the conduction angle is reduced. And trade-off between linearity, gain, and efficiency must be made when selecting the operation mode. Performance of those operation modes are compared in Table 2.2.

Table 2.2: Comparison of operation modes

Operation Mode	Linearity	Efficiency	Gain
Class- A	Good	Poor	Good
Class- AB	Moderate	Moderate	Good
Class- B	Good	Good	Moderate
Class- C	Poor	Good	Poor

2.2.3 Harmonic Tuned Power Amplifiers

2.2.3.1 Class-F Operation Mode

In class-F operation mode, the transistor is biased at the same level with class-B so the output current waveform is also rectified half-sinusoidal wave but the targeted voltage wave is rectangular wave totally staggered with current waveform as shown in Figure 2.5. Both voltage and current waveforms contains infinite order harmonics. After Fourier analysis of those two waveforms, the terminations for different current components is calculated by dividing the magnitude of voltage with those of current of the same order

$$Z_n = \frac{V_n}{I_n}, \quad n=1, 2, 3\ldots \tag{2.16}$$

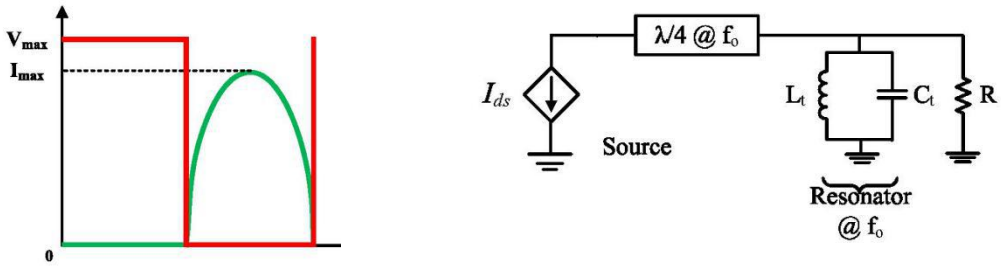
$$Z_1 = R_{opt}^F = \frac{4}{\pi} \times R_{opt}^B \tag{2.17}$$

The current waveform contains only even order harmonics while the rectangular voltage waveform contains only odd order harmonics. So termination at harmonics are

$$Z_n = 0, \quad n=2, 4, 6\ldots \tag{2.18}$$

$$Z_n = \infty, \quad n=3, 5, 7\ldots \tag{2.19}$$

Because there is no overlap between the drain current and drain voltage, the product of instantaneous values of current and voltage is always zero. So one conclusion can be drawn that the power amplifiers under this operation mode transforms all the DC power into RF power leading to efficiency of 100%.



(a) (b)

Fig 2.5: Class-F waveforms and one possible implementation

Theoretically, class-F operation requires careful selection of terminations for all. In practice, controlling up to the 3rd harmonic will guarantee the decent efficiency of 88.4% [4]. Tuning of higher harmonics will considerably add up the design complexity and results only trivial efficiency improvement.

Due to the stringent requirement of the harmonic termination, the impedance matching for class-F is only narrow band. In the recent work [2] extended design space is proposed to release the matching restriction imposed by conventional class-F operation mode. The extended design space brings a generalization of class-F mode and is regarded to be suitable for broadband operation. Even though, the widest fractional bandwidth in theory is 50% (wider bandwidth will result in overlap of 2nd and 3rd harmonic band).

2.2.3.2 Continuous Class-B Operation

Continuous class-B, also called class-J operation, represents a set of operation modes which ideally share the same efficiency, output power and linearity with class-B. At fundamental frequency, transistors under class-B operation mode must be terminated with its R_{opt} transformed from load R_L (usually 50 Ohm), i.e. only point-to-point is allowed. The continuous class-B operation mode, on contrary, allows the fundamental termination to be series of complex impedances with the same real part. Continuous class-B is suitable for broadband operation since the fundamental termination can vary versus frequency. Meanwhile, second harmonic must be shorted for class-B to achieve high efficiency. Unfortunately, this will be difficult to implement since matching networks built through distributed elements show periodicity so second harmonic termination cannot stay to be zero in a broadband. This seemingly matching issue does not exist in continuous class-B operation mode for the reason that second harmonic termination is not necessarily short circuit, which provides more flexibility for broadband design.

Same as conventional class-B, the current waveforms of continuous class-B is rectified half sinusoidal. But the voltage waveform is expressed as

$$\begin{aligned} V_{norm}(\theta) &= [1-\cos(\theta)] \times [1-\alpha\sin(\theta)] \\ &= 1-\cos(\theta)-\alpha\sin(\theta)+\frac{1}{2}\alpha\cos(2\theta),\ -1 \le \alpha \le 1 \end{aligned} \tag{2.20}$$

where the V_{norm} denotes the voltage waveform normalized by its DC component. Factorized Equation 2.20 includes four items. The first two items are DC component and real part of the fundamental

component which are the same with class-B operation mode. So continuous class-B can provide the same output power and efficiency as class-B. Worth noting are the last two terms, whose appearance in waveform generalize the operation of class-B to continuous class-B. The third item has a ninety degree phase shift with the fundamental component of current waveform and thus it is the imaginary part of voltage at fundamental. Apparently, the non-zero imaginary part enlarged the magnitude of fundamental voltage waveform and consequently the waveform will drop below zero and intrude knee region. This is obviously unacceptable since it will rise serious nonlinearity problem. To solve the problem, the nonzero out-of-phase second harmonic part is introduced to bring the lowest value of voltage waveform back above zero. Actually, when α varies from -1 to 1, Equation 2.20 describes a set of functions whose valleys graze but not intersect with zero. Therefore, the linearity performance of continuous class-B is similar to conventional class B.

Using Equation 2.15, the impedances at fundamental and harmonics can be calculated

$$Z_1 = R_{opt}{}^{B} \times (1 + j\alpha) \quad (2.21a)$$

$$Z_2 = -j\frac{3\pi}{8}\alpha R_{opt}{}^{B} \quad (2.21b)$$

$$Z_n = 0, n = 3, 4, 5... \quad (2.21c)$$

where

$$R_{opt}^{B} = \frac{V_{DD}}{I_{max}/2} \quad (2.22)$$

For different values of α, the current and voltage waveforms and impedances in smith chart are illustrated in Figure 2.6. As can be seen, for α equals zero, the operation becomes conventional class-B. When $\alpha=\pm 1$, the peak voltage value can be almost three times that of conventional class-B. So the transistors must be capable to handle the large voltage swing without being broken down.

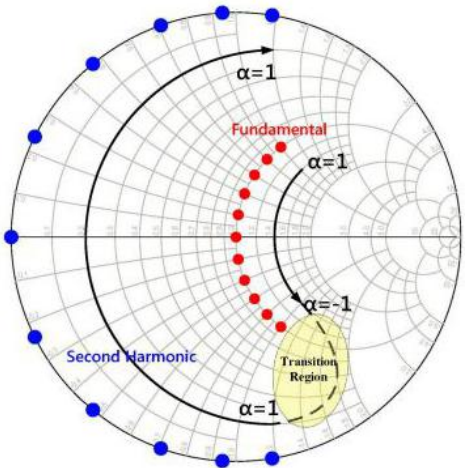


Fig 2.6: Continuous class - B design space

2.2.3.3 Switch Mode Power Amplifiers

Aiming to reduce the overlap between current and voltage waveforms could improve the efficiency, the switch mode power amplifiers, class-F^{-1} and class-E can theoretically achieve 100% efficiency. Conversely with class-F mode mentioned before, the current waveform of class-F^{-1} is rectangular wave while the voltage waveform is rectified half-sinusoidal. In practice, the rectangular current waveform is achieved through over-driving the transistor and voltage waveform is achieved by tuning the terminations. Terminations for different harmonics are

$$Z_1 = R_{opt}^F = \frac{4}{\pi} R_{opt}^B \quad (2.23a)$$

$$Z_{2n} = \infty \quad (2.23b)$$

$$Z_{2n+1} = 0, n = 1,2,3... \quad (2.23c)$$

The class-E power amplifier is widely used due to the simplicity of implementation [4]. Transistors are working as a switch to charge and discharge the load periodically. The current flowing to the load is filtered to get rid of the harmonics. And those prevented harmonic components are bypassed through shunt capacitors. Class-E has the ceilings for the highest allowable operation frequency due to the parasitic. Numerical analysis are based on the time domain. Both class-E and class-F^{-1} require the transistors to be switched on-and-off in one cycle, and accordingly, they are categorized into switch operation modes.

2.2.4 Doherty Power Amplifier

Doherty power amplifier is an efficiency enhancement technique presented by William Doherty in [1]. Among all the efficiency enhancement techniques, Doherty power amplifier has gained popularity due to its easiness of implementation. Despite the advantages, the traditional Doherty power amplifier suffers from various limitations such as bandwidth. We will introduce the principle of operation in the following. Design challenges are outlined and literature will be reviewed to report the state-of-art in Doherty power amplifier design. Solutions to those problem which forms the core innovation of the thesis will be detailed in the subsequent chapter.

2.2.4.1 Operation Principle of Doherty Power Amplifier

The configuration Doherty power amplifier is shown in Figure 2.7. Two transistors, idealized as voltage-control-current-sources, are utilized as main (or carrier) and peaking (or auxiliary) amplifiers. An inverter composed of a 90 degree transmission line with specified characteristic impedance performs power combining for those two amplifiers. Although in practice, the transconductance of a transistor is always nonlinear, we assume the drain current change linearly versus gate voltage to simplify the analysis. The fundamental components of main and peaking current (I_{main} and $I_{peaking}$) follow the expressions below

$$I_{main}(\delta) = \begin{cases} I_M \times \delta & 0 \le \delta \le 1 \\ I_M & \delta > 1 \\ 0 & \delta < 0 \end{cases} \quad (2.24)$$

$$I_{peaking}(\delta) = \begin{cases} 2 \times I_P \times (\delta - 0.5) & 0.5 \le \delta \le 1 \\ I_p & \delta \ge 1 \\ 0 & \delta < 0 \end{cases} \quad (2.25)$$

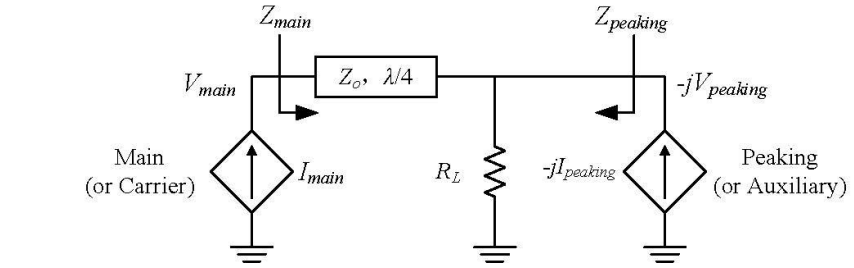
with δ the normalized input voltage. To combine the output power of the two paths in phase, there must be a 90 degree phase lag of peaking amplifier current. The circuit analysis reveals the following relation

$$Z_{main} = Z_T \times \left(\frac{Z_T}{R_L} - \frac{I_{peaking}}{I_{main}}\right) \quad (2.26)$$

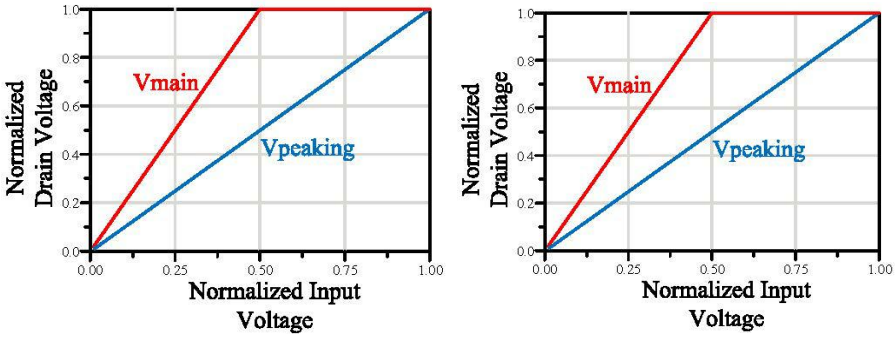
$$V_{peaking} = Z_T \times I_{main} \quad (2.27)$$

$$Z_{peaking} = Z_T \times \frac{I_{main}}{I_{Peaking}} \quad (2.28)$$

When $0 \leq \delta \leq 0.5$ (Doherty region), the peaking amplifier is off and only main amplifier is operating.



(a) Configuration of DPA



(b) Current Profile

(c) Voltage Profile

Fig 2.7: Doherty power amplifiers and current/voltage profiles

To maximize the drain efficiency when $\delta = 0.5$ (6 dB back-off), the impedance shown to the main amplifier needs to be $2R_{opt,main}$

$$Z_{main}^{BO} = \frac{Z_T^2}{R_L} = 2R_{opt,main} \quad (2.29)$$

When $\delta = 1$(PEP level), both impedances present to the two amplifiers must be R_{opt}.

$$Z_{main}^{PEP} = R_{opt,main} \quad (2.30)$$

$$Z_{peaking}^{PEP} = R_{opt,peaking} \quad (2.31)$$

Given the two transistors are symmetrically biased and the optimum impedances are the same, i.e., $R_{opt,main}=R_{opt,peaking}=R_{opt}$. Therefore, the parameters in the circuit are specified as

$$Z_T = R_{opt} \quad (2.32)$$

$$R_L = \frac{R_{opt}}{2} \quad (2.33)$$

$$I_{main} = I_{peaking} = I_{\max}, \delta = 1 \quad (2.34)$$

The parameters deduced above can boost the efficiency at 6dB (δ=0.5) back-off up to 78.5% ideally, the maximum efficiency for class-B operation.

Impedances and output power at different input power level are derived according to the current and voltage

$$Z_{main}(\delta) = \begin{cases} 2 \times R_{opt}, 0 \le \delta \le 0.5 \\ R_{opt}/\delta \ , 0.5 \le \delta \le 1 \end{cases} \quad (2.35)$$

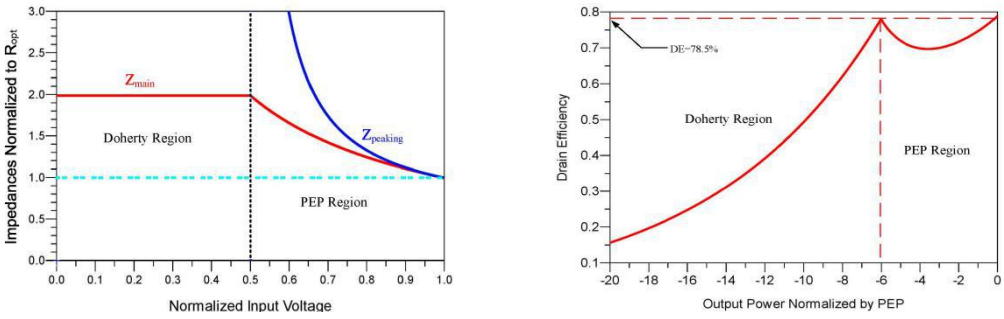
$$Z_{peaking}(\delta) = \begin{cases} \overset{\infty}{R_{opt}} & , 0 \le \delta < 0.5 \\ \dfrac{}{2 \times (\delta - 0.5)} & , 0.5 \le \delta \le 1 \end{cases} \quad (2.36)$$

$$\begin{aligned} P_{out} &= \frac{1}{2} Real\left(I_m \times V_m^* + I_p \times V_p^*\right) \\ &= \frac{(g_m * \delta)^2}{R_L} \end{aligned} \quad (2.37)$$

The square law demonstrated in Equation 2.37 means Doherty power amplifier is linear amplifier intrinsically. The efficiency can then be derived as the quotient of output power and DC power consumption. As is shown in Figure 2.8, there are predicted two efficiency peaks at peak-envelope-power level and 6dB back-off level. Since both Z_{main} and $Z_{peaking}$ are changing versus power level, the principle of operation is called load modulation.

2.2.4.2 Doherty Power Amplifier Design Challenges

Ideal voltage-control-current-source are helpful for capturing the basic operation principle and formalizing the circuit parameters. But in practice, the accurate compact model of transistors used for PA design are much more complex. Parasitics are not negligible at RF frequency and supposed to be absorbed into the external passive networks so that the intrinsic current generator can be accessible. Non-zero knee voltage limits the voltage swing and prevents power amplifier from approaching the theoretical efficiency. Parasitics of the active part of transistors can be slightly or strongly nonlinear which distort the waveforms. On top of those common issues encountered in general PA design, there are still problems existing specifically in DPA design. Those include soft turn-on and uneven transconductance required to provide the specified current profiles. Details are given in the subsections.



(a) Impedance profile

(b) Drain efficiency versus output power

Fig 2.8: Load modulation and efficiency enhancement

2.2.4.2.1 Parasitics of Transistors

The PN junction at the interface between different types of doped semiconductors can charge and discharge when the voltage drop changes and thus shows capacitive characteristics. The overlap between two electrodes may also result in plate capacitors connecting between those electrodes. For commercial transistors (GaN or LDMOS), there are still package-introduced parasitics such as capacitor caused by pads, (self- or mutual-) inductor caused by bond wires and other resistive components.

Usually the transistors should be modeled before they are used in power amplifier design. The Cold-FET modeling technique [3] is efficient and easy to implement. It starts with partitioning so that we can separate the active (intrinsic) part, which includes the active components and is always nonlinear, and external part, which is always passive and linear. For the active part of a transistor, the three most influential parasitic components are capacitors connecting every two electrodes, namely C_{gs}, C_{gd}, and C_{ds} as is shown in Figure 2.9. The models extracted for a 6 Watts GaN HEMTs shows that the C_{gs} at the input is highly nonlinear. The threshold voltage is -2.8 V and transistor can tolerate as high as 2 V gate voltage. As is shown in Figure 2.10, in this range, the capacitance vary from lowest value below 2 pF to highest value of 3.4 pF. The strong nonlinearity will generate high order harmonics and the waveform could be distorted. The distorted voltage waveform will then be transformed as the output drain current and reflected as nonlinear AM-AM/AM-PM behaviors. Even for the efficiency performance, the harmonics can play an important role so the termination condition of those harmonics is noteworthy. As is revealed in [9], the source impedance shown to the harmonics, once not carefully tuned, will fall into the sensitive region and deteriorate efficiency by distorting the

voltage waveforms. Designers use to use quarter wavelength transmission line shorted to ground as the biasing line at the input. The transmission line is an open circuit at center frequency so it does not influence the RF signal amplification at fundamental. Meanwhile it can short any even order currents and thus annul the effects of 2nd harmonics. But at the package plane, the short circuit may not be the optimum termination for efficiency and gain. In addition, this method is not suitable for broadband design because it poses contradictory requirements for the characteristic impedance, i.e., the characteristic impedance needs to be large to provide a broadband open circuit in fundamental band and meanwhile small to provide broadband short circuit for 2nd order harmonics.

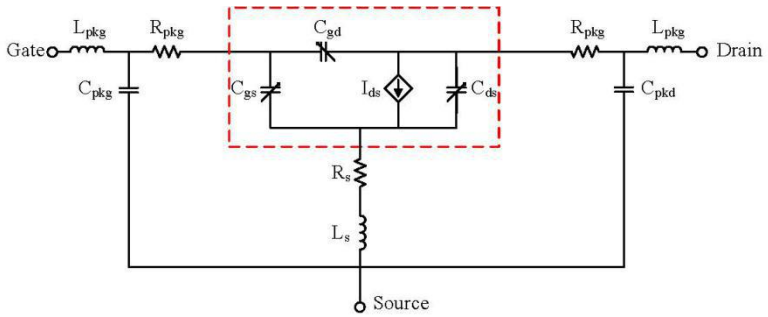


Fig 2.9: Compact small signal model of packaged transistor

The output capacitor, C_{ds}, is nonlinear for LDMOS [34] and slightly nonlinear for GaN as shown in Figure 2.10. The direct influence of C_{ds} is the impedance matching problem. According to Bode-Fano limit [15], the matching bandwidth is limited by the parasitic capacitor once the maximally allowed reflection ripple is specified. Extra care should be taken for C_{ds} especially when designing Doherty power amplifier because the impedance shown to both amplifiers are not constant when power level is changing. And the phase shift introduced by C_{ds} will impair the load modulation. C_{ds} can be resonated out by an inductive component but, still, the bandwidth is limited [8]. An alternative solution is to absorb it into the 90 degree inverter [34]. This is only valid at a relatively low frequency and the load still cannot be connected to the peaking amplifier as needed.

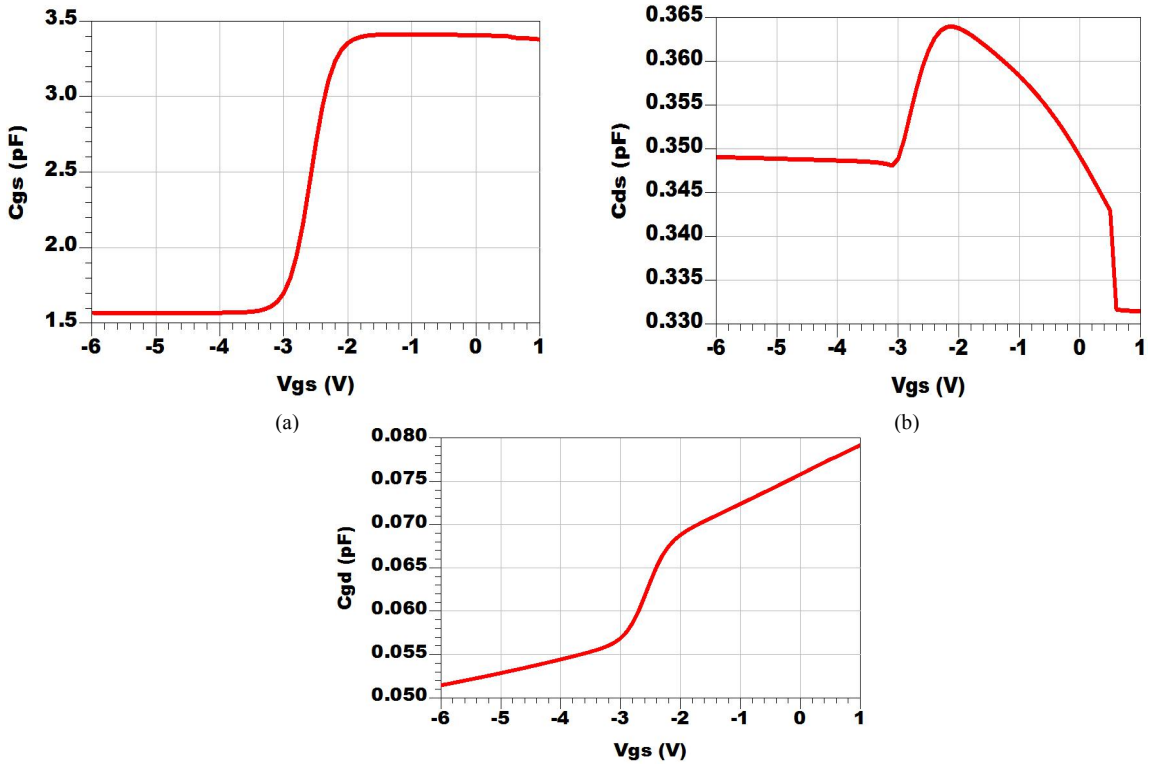


Fig 2.10: C_{gs}, C_{ds} and C_{gd} versus gate biasing voltage.

C_{gd} is the capacitor connected between gate and drain. Its value is usually one order smaller than the C_{gs}. But that does not make it negligible since the capacitor form the cross-talk between the input and output. The harmonics generated by the nonlinear C_{gs} could be directly fed to the output and decrease the quality of the waveform. In return, the output can also feedback signals to the input. This makes the transistors bilateral and stability problem arises. For transistors with smaller periphery, they may be regarded as unilateral devices. But for large transistors, the appearance of C_{gd} will make the design of input and output matching networks an iterative process.

At the outer side of the model, there are parasitics like C_{pkg}, C_{pkd} and L_{bond} at both input and output side. Those are introduced by the pads at gate and drain and bond arrays [3]. To be more accurate, the cross coupling modeled as a mutual capacitor and inductor should included for transistors with small periphery. Since the package contains only passive elements, those parasitics are usually linear.

2.2.4.2.2 Soft Turn-on Effect and Uneven Transconductance Requirement

In the previous analysis, it is assumed that the transistors can be turned on and off abruptly. In reality the current profile of the conventional DPA requires the peaking amplifier to be turned on in

the middle way of the input voltage. Turning on point of peaking amplifier can be adaptively controlled for dual-input DPA. But in single-input DPA peaking amplifier should operate in class-C mode. One the problem from class-C operation is the soft turn-on. When the gate voltage of the peaking transistor is below the threshold voltage, the transistor cannot be thoroughly turned off because there is current leaked into the drain through the parasitics. And because of the non-ideality of the transfer function, there is transition range in which the drain current increases gradually versus input power instead of changing abruptly. This bring challenges for providing needed current profile and approaching the theoretical Doherty operation. The soft turn on effect and its influence on the performance of the DPA can be roughly studied using ideal model in which the turning on point is modified to be prior or posterior to that of ideal operation. When the peaking amplifier is turned on earlier, the impedance to the main amplifier starts to drop before the drain voltage reach its maximum value. As a consequence, the efficiency at the back-off level is degraded. Inversely, if the peaking amplifier is turned on lately, the drain voltage of the main amplifier will drop below the knee voltage and seriously impair the linearity of the DPA. The current leakage issue can be partially solved by absorbing the output parasitics into the matching network on the peaking path. While the soft-on issue can be mitigated by careful selection of the source impedance at the input side.

As analyzed previously, the conduction angle of class-C is not a constant and expands versus the input power level. As a result, the fundamental component of the current is no longer a linear function versus the gate voltage. Meanwhile, the reduced conduction angle of class-C also decreases the gain of peaking amplifier compared with main amplifier. So the overall gain of DPA will not be as high as the main amplifier operating under class-B and will show compression.

The peaking amplifier, although is turned on in the middle way, must output the same current at peak-envelope-power level. Therefore, the slope of the peaking current versus voltage must be twice as the main current. Intuitively, we can achieve that by selecting larger transistor for peaking amplifier. In [36], two different GaN transistors of 25 W and 45 W were used in the main and peaking paths separately. The usage of asymmetrical devices allow the evenly power splitting at the input and thus release the burden of power splitter design. But the drawbacks are also obvious. The output power of conventional Doherty power amplifier is extracted evenly from main and peaking amplifiers so the larger device used as the peaking amplifier is underutilized. Meanwhile, the asymmetrical devices call for the separate design of input matching networks for the two paths, adding up the design complexity. To overcome those problem, the uneven power splitting method is a good

candidate. By inputting more power to the peaking path [37], the drain current could increase faster and satisfy the requirement of the operation of the Doherty power amplifier. The limitation is the reduced gain due to the relatively lower gain of class-C operation. Meanwhile, as is shown in [11], the Wilkinson splitters designed for uneven power division have more limited bandwidth compared with those designed for the even division. A systematic methodology for designing input matching networks (IMNs) of main and peaking amplifiers was proposed [9]. This methodology allows to use two symmetrical transistors and even power splitting. By driving the two transistors with different source impedances, the required current profile can be achieved. But in reality, because the transistor is bilateral, the optimal source impedances can not be selected without knowing load as priori.

For conventional Doherty power amplifier design, some other problems such as harmonic termination and knee region intrusion also need to be addressed. It is easy to understand that the increased efficiency of reduced conduction angle mode is the partially due to shorting harmonics. Once used in DPA, it is also a must to provide proper harmonic termination. The improper selection of the load at fundamental frequency will also lead to intrusion into the knee region.The conventional way utilizing stubs to short the even order harmonics is easy to implement but not suitable for broadband design. Stability issue in Doherty power amplifier is not the same with the single-transistor power amplifier. At peak-envelope power level, both amplifiers are operating and their current components, fundamentals or harmonics, will interact will each other and the terminations shown to the two transistors may not be confined within the Smith chart unit circle. Stability analysis has to be carried out with main and peaking amplifiers assembled.

2.3 Broadband Doherty Power Amplifier Literature Review

The configuration of DPA includes an inverter to provide the load modulation. Therefor it is a narrow band amplifier by nature. For this reason, modification of the conventional DPA to overcome the bandwidth limitation stays in the center of research focus. At the meantime, the modern communication system utilizes Carrier aggregation which requires not only efficient amplification of the signals with high PAPR but also capability for broadband multi-standard operation. Previously, the transceivers are designed to include several power amplifiers each working at one single carrier frequency and then digitally controlled by switch arrays. The redundant power amplifiers needed will increase the expense of implementation and different carriers in signals cannot be amplified concurrently.

Attempts to extend the bandwidth of Doherty power amplifier were started with the analysis of the bandwidth limitation [8, 10]. In these works, dispersion of the inverter and the effects on load modulation, output power and efficiency was studied. Conclusions were drawn that the reduced impedance transformation ratio of the inverter could help to extend the operation bandwidth. In [8, 34], the output capacitors of transistors were resonated out or absorbed using lumped or quasi lumped inverter instead of the quarter wavelength transmission line.

The modified impedance transformation ratio, although efficiently broadens the bandwidth, requires new current or voltage profiles. The work of [13] reformulated the needed impedance profile. And by setting the impedance transformation ratio to be unit, the bandwidth at 6dB back-off is unlimited theoretically. As a result, the needed current and voltage profiles were derived and final implementation used two different drain biasing voltages. At 6dB back off, the efficiency higher than 52% was achieved over the fractional bandwidth of 35% (700MHz-1000MHz). This approach required peaking amplifier to have higher breakdown voltage.

In [14], it was demonstrated that three-way Doherty power amplifiers had intrinsically wider bandwidth than two-way ones and can provide more freedom to optimize design specifications like back off level and bandwidth. Based on the assumption that harmonics were shorted, independent circuit parameters of load impedance R_L was selected to achieve widest bandwidth at 9.5 and 6dB back off power level. In the frequency range of 730 to 980MHz (30% fractional bandwidth), the 9dB back off efficiency was maintained above 49% and the 6dB back off efficiency above 42%. Even the theory indicated better performance but the bandwidth of this design was limited by the quarter wavelength transmission lines used to short the 2^{nd} harmonics.

It was explained that the inverter acting as resonators could partially nullify the frequency variation of the main impedance and extend the bandwidth [14]. This property was further exploited in [16, 17], where the novel output combiner for two-way DPA was proposed. By adding resonator ($\lambda/4$ short stub or parallel resonator) at the current combining junction, the variation of main impedance at back-off was mitigated and thus the performance was more constant. The added resonators was also used to absorb the output capacitor. Similarly, the work [18] used $\lambda/2$ open stub as the resonator and achieved better bandwidth over conventional Doherty power amplifier. Worth noting is that in [17], the main amplifier was actually operating at class-F mode at center frequency. This work along with [13] represents the bandwidth enhancement method which sacrifice the bandwidth at peak power level to get wider bandwidth at back off.

The Real Frequency Technique, firstly proposed by Carlin and Komiak [19], was adopted in DPA design [20]. The optimum impedances at the package plane were used as the optimization goal and broadband matching was achieved. In the actual design, they opted to optimize the impedance for the back off operation and tolerate the suboptimum operation at the peak power level or, on inversely, optimize the impedance for the peak power level and accept the back-off operation to be suboptimum. This was because two equal sized transistors were selected and it was difficult to achieve two point matching in a wide band. As explained, either back off or peak power operation had to be sacrificed and the harmonic termination required for high efficiency operation was not addressed. The analysis accepted uneven power contribution from the transistor without adopting asymmetrical drain biasing or impedance profile. So the efficiency could be further improved.

Similar to the [18], the λ/2 transmission line as a resonator was also used in [21, 22] and the potential of extending the bandwidth was exploited. But in [21, 22], the half-wavelength transmission line was split into two quarter wavelength lines with different characteristic impedances. The ratio of these two characteristic impedances was tuned to amplify the current from the peaking amplifier since the peaking current slope (fundamental component) needed to be twice of the main one. By this way, transistors could be selected of the same size and drain biasing and the input matching networks can be identical. In [22], the two absolute values of the characteristic impedances were further analyzed and optimized to contain the impedance dispersion within certain tolerance.

The concept of continuum was utilized to realize broadband operation [23]. Matching networks to absorb the parasitics for main and peaking amplifiers were designed and the harmonics was tuned to avoid the sensitive region. But the usage of offset line made the impedance shown to main and peaking amplifiers too dispersive and there was no link between the proposed theory and the actual implementation with respect to the harmonic termination. The increased bandwidth was achieved by showing higher impedance level than R_{opt}, which was not advisable for avoidance of intrusion into knee region.

Attempts of introducing continuous operation mode into Doherty power amplifier were also reported in [24]. At back off, the non-infinite output impedance of peaking amplifier was used, along with the matching network in that path, to create resonator-like behavior. This behavior, as was previously clarified in previous literature [21, 14, 16, 22], could be used to partially cancel the dispersive behavior so that at back off the efficiency or output power can be flattened versus frequency. Similarly, the same problem remained for that work, namely, the bandwidth at peak power

could no longer be as wide as predicted by conventional DPA. Meanwhile, the creation of resonator at the peaking path modified the amplitude and phase relationship between the two paths so load modulation was not intact. The resonator-like behavior cannot be arbitrarily determined as needed. Actually, it was determined by the value of parasitics (mainly the output capacitance). So the methodology will suffer from lack of universality. On top of that, there was no clarification about the load modulation and 2nd harmonic termination at peak power level.

The main and peaking PA units were designed in structure of push-pull to exploit the intrinsic broadband potential [25]. The push-pull operation and excellent frequency performance of balun guaranteed the wide bandwidth and the efficiency was enhanced through carefully tuned 2nd harmonic termination. Over one octave operation was achieved. Even though, the baluns was unfortunately confined within low frequency operation and so was push-pull Doherty power amplifiers.

In [26], the complex load varying versus frequency and input current control was used. The frequency broadband operation was achieved and efficiency was enhanced at around 9dB backoff. Another work [27] utilized the compensating network at the combining node and two point matching to expand the bandwidth without damaging the load modulation. A summary table on broadband DPAs is given in the following.

Table 2.3: Literature review on broadband DPAs

Ref.	Technique	Frequency (GHz)	Gain (dB)	P_{out} (dBm)	*η-6dB (%)*
2011 [8]	OCN	1.6-2.1	28	35	25/35
2011 [10]	OCN	1.7-2.6	12	37.5	40/50
2016 [12]	OCN	1.65-2.75	10	45	57/68
2012 [13]	Asymmetrical Biasing	0.7-1	16	49	60/67
2014 [14]	Three Way	0.73-0.98	11	42	56(*η-9dB*)/ 55(*η-6dB)/55*
2016 [16]	OCN	1.72-2.27	9.5	42	52/65
2014 [17]	OCN	0.7-0.95	15	43	53/62
2014 [18]	OCN	0.47-0.79	16	59	43/55
2012 [20]	SRFT	2.2-2.96	8	41	40/60

2014 [22]	OCN	1.05-2.55	10	40	45/55
2014 [21]	Transformer	0.79-0.96	19	55	49/58
2018 [24]	Continuous Mode	1.6-2.7	10	44	55/65
2016 [25]	Push-Pull	0.6-1.4	17	53	55/58
2015 [26]	Complex Load	1.8-2.2	11	42	55(η-*8.5dB*)/ 65
2016 [27]	OCN	1.7-2.8	14	44	53/64

Chapter 3

Systematic Method for Broadband Doherty Power Amplifier Design

In the previous chapters, the Doherty power amplifier operation principle is introduced. It is clear that the inclusion of the inverter for the conventional DPA limits the operation bandwidth. Accordingly, attempts have been made for the extension of bandwidth. On the other hand, the continuous class-B/F [28, 29] operation modes were proposed and the corresponding design spaces were defined. This design space represents a series of fundamental and harmonic impedances terminated by which, the power amplifier could provide the same output power, efficiency and linearity with class-B/F theoretically. The released design flexibility provided another path toward broadband operation. The validity of the continuous operation mode was then substantiated by the clipping contour method [30] and in the design of single-ended power amplifier, the continuous mode theory was implemented [31]. The bandwidth approached 1.2GHz (1.4-2.5GHz) and efficiency was maintained higher than 60%.

Just as all the other operation modes, once implemented in single-ended power amplifiers, the efficiency at back-off power level will be degraded compared with the decent efficiency achieved at only peak power level, which necessitates the introduction of efficiency enhancement technology like DPA. In this chapter, a systematic methodology on the design of DPA operating under continuous class-B mode is proposed. Based on two port network analysis, it is shown that the continuous design space can be introduced into Doherty power amplifier design by releasing the restriction of parameters of matching networks at the main and peaking paths. The potential of broadband operation can then fully exploited. Additionally, the proposed methodology can automatically take into account of the parasitics of the transistors so that the parasitics issue, as a source of bandwidth limitation, can be addressed. Meanwhile, 2^{nd} harmonic components in the drain current can be terminated as required by the continuous operation mode so that the efficiency can reach that of single-ended class-B power amplifier while back off efficiency is enhanced. Following this method, the design PA could have enhanced back-off efficiency and broad operation bandwidth.

This chapter starts with briefing the ABCD parameter analysis of a two port network. Then, matching networks supporting DPA with main and peaking amplifiers operating under continuous mode is formalized using ABCD parameters. As will be seen in the network analysis, parasitics can be absorbed into the networks and 2^{nd} harmonic termination can be placed into the safety region for

high efficiency operation. As a proof of proposed methodology, a broadband Doherty power amplifier is designed, fabricated and measured.

3.1 ABCD Parameter Analysis for Two Port Networks

ABCD parameters, also known as the transmission parameters, is used to describe the behavior of linear networks. In ABCD representation of a two port network, voltage and current at port 1 are defined to be dependant variables and the voltage current pair at port 2 are used as independent variables as shown in Figure 3.1

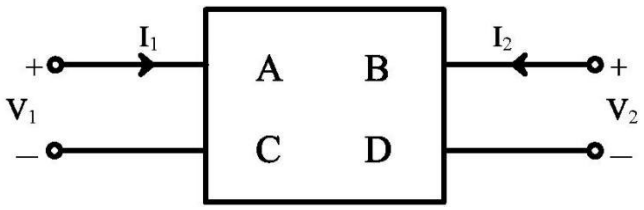


Fig 3.1: ABCD parameters

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \quad (3.1)$$

$$A = \left. \frac{V_1}{V_2} \right|_{I_2=0} \quad (3.2)$$

$$B = \left. \frac{V_1}{-I_2} \right|_{V_2=0} \quad (3.3)$$

$$C = \left. \frac{I_1}{V_2} \right|_{I_2=0} \quad (3.4)$$

$$D = \left. \frac{I_1}{-I_2} \right|_{V_2=0} \quad (3.5)$$

The above Equation 3.1-3.5 are enough to fully describe the behaviour of a linear two port network. *A* and *D* are voltage and current gain from port 2 to port 1 separately and they are dimensionless. The units for *B* and *C* are Ohm and Siemens since they represents the transimpedance and

transconductance from port 2 to port 1 separately. For reciprocal networks, the corresponding ABCD parameter must fulfill the following relationship

$$AD - BC = 1 \qquad (3.6)$$

And if the networks contains only passive and purely reactive elements, A and D must be purely real and B and C must be purely imaginary

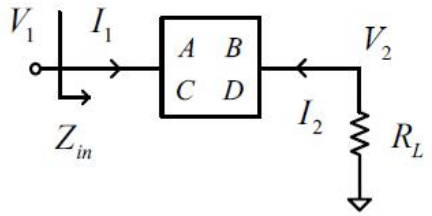


Fig 3.2: Impedance transformation

If port 2 (output port)is terminated with the load R_L as shown in Figure 3.2, the two port network will be degenerated into a single port network with the driving point impedance seen from input port to be

$$Z_{in} = \frac{AR_L + B}{CR_L + D} \qquad (3.7)$$

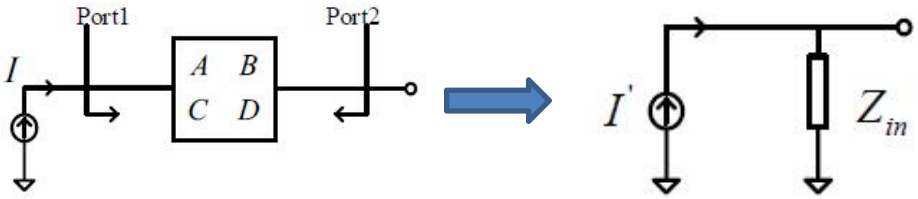


Fig 3.3: Current source equivalent circuit

To study the influence of matching networks to the transistor operation, we study the case in which the current source I is connected to a two port network described by its $ABCD$ parameter. The Thevenin equivalent circuit, contains a current I' and a source impedance Z_{in} as shown in Figure 3.3, in which the equivalent current source I' and its source impedance Z_{in} are

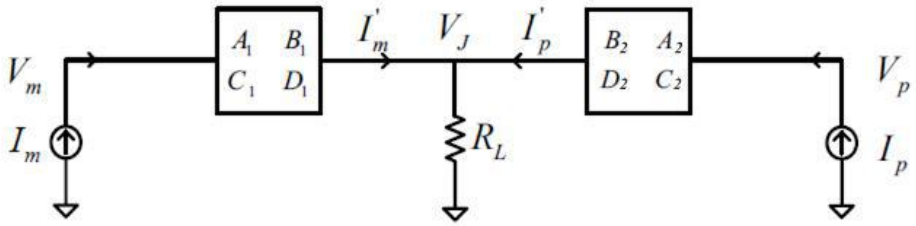
$$I' = \frac{I}{D} \qquad (3.8)$$

$$Z_{in} = \frac{D}{C} \qquad (3.9)$$

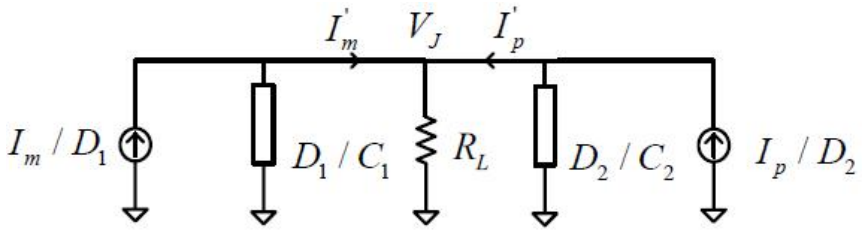
As can be seen from the Equations 3.8 - 3.9, singularity will appear once *D=0*. In that case, the equivalent circuit will take the form of a voltage source series with a zero-value source impedance. But for mathematical analysis, this singularity will make no difference.

3.2 Matching Networks for Doherty Load Modulation

In this subsection, a novel approach to employ the continuous operation mode into Doherty power amplifier design involving the two port network analysis is proposed. The continuous class-B operation mode is used. Figure 3.4 (a) is a generic illustration of Doherty power amplifier that includes two two-port matching networks at main and peaking paths separately. They are described by matrices $ABCD_1$ and $ABCD_2$. In this analysis, the ideal current source models are still used to model the two transistors. As shown, the V_m and V_p denote the drain voltages of main and peaking amplifiers and I_m and I_p are the drain currents extracted from the the two amplifiers. At the junction, V_j denotes the junction voltage and currents contributed from the main and peaking paths are I_m' and I_p'.



(a) Generic illustration of DPA



(b) Equivalent circuit of DPA

Fig 3.4: Proposed illustration of DPA and equivalent circuit

Using Equation 3.8 - 3.9, the circuit in Figure 3.4 (a) can be converted into the equivalent circuit shown in Figure 3.4 (b), where the two original sub-circuits connected to the junction are transformed

into their Norton equivalent counterparts. As can be seen, the equivalent circuit contains all components connected in parallel. So the KCL or superposition theorem can be used to solve the circuit equations. Here, the unknowns are I_m', I_p' and V_j and they are derived as

$$I'_m = (\frac{I_m}{D_1} + \frac{I_p}{D_2})(G_L + \frac{C_1}{D_1} + \frac{C_2}{D_2})^{-1}(-\frac{C_1}{D_1}) + \frac{I_m}{D_1} \quad (3.10)$$

$$I'_p = (\frac{I_m}{D_1} + \frac{I_p}{D_2})(G_L + \frac{C_1}{D_1} + \frac{C_2}{D_2})^{-1}(-\frac{C_2}{D_2}) + \frac{I_p}{D_2} \quad (3.11)$$

$$V_J = (\frac{I_m}{D_1} + \frac{I_p}{D_2})(G_L + \frac{C_1}{D_1} + \frac{C_2}{D_2})^{-1} \quad (3.12)$$

What we are interested in are the impedances shown to the main and peaking amplifiers and therefor the driving point impedances at port 1 and port 2 must be calculated. According to Equation 3.7, the main and peaking impedances denoted as Z_m and Z_p can be derived as

$$Z_m = \frac{A_1 Z_{j,1} + B_1}{C_1 Z_{j,1} + D_1} \quad (3.13)$$

$$Z_p = \frac{A_2 Z_{j,2} + B_2}{C_2 Z_{j,2} + D_2} \quad (3.14)$$

with $Z_{j,1}$ and $Z_{j,2}$ the impedances at the junction seen from main and peaking path to the junction respectively. The junction is a common node and $Z_{j,1}$ and $Z_{j,2}$ can be easily found out to be

$$Z_{j,1} = \frac{V_j}{I_m'} \quad (3.15)$$

$$Z_{j,2} = \frac{V_j}{I_p'} \quad (3.16)$$

and the resultant expression for Z_m and Z_p are

$$Z_m = \frac{A_1 + B_1 \frac{I_m'}{V_J}}{C_1 + D_1 \frac{I_m'}{V_J}} \quad (3.17)$$

$$Z_p = \frac{A_2 + B_2 \frac{I_m'}{V_J}}{C_2 + D_2 \frac{I_m'}{V_J}} \quad (3.18)$$

Evaluating two specific cases: *BO*, the back off power level where the peaking amplifier is off, and *PEP*, the peak envelope power level where both transistors are turned on, we have

$$Z_{m,BO} = \frac{(A_1D_2 + B_1C_2)R_L + B_1D_2}{D_1D_2 + (C_1D_2 + D_1C_2)R_L} \quad (3.19)$$

$$Z_{m,PEP} = \frac{(A_1D_2 + B_1C_2)R_L + (B_1D_2 + \sigma R_L)}{D_1D_2 + (C_1D_2 + D_1C_2)R_L} \quad (3.20)$$

$$Z_{p,PEP} = \frac{(A_1D_2 + B_1C_2)R_L + (B_1D_2 + \sigma^{-1}R_L)}{D_1D_2 + (C_1D_2 + D_1C_2)R_L} \quad (3.21)$$

where σ here denotes the current ratio between two paths and equals to I_p/I_m. The σ is complex number: the magnitude is the ratio of currents absolute values and the angle is the phase difference between those currents. For the typical condition σ is $-j$, and Equation 3.20 - 3.21 will be

$$Z_{m,PEP} = \frac{(A_1D_2 + B_1C_2)R_L + (B_1D_2 - jR_L)}{D_1D_2 + (C_1D_2 + D_1C_2)R_L} \quad (3.22)$$

$$Z_{p,PEP} = \frac{(A_1D_2 + B_1C_2)R_L + (B_1D_2 - jR_L)}{D_1D_2 + (C_1D_2 + D_1C_2)R_L} \quad (3.23)$$

and Equation 3.19 remains unchanged.

Note that the lossless property of two-port networks requires that *A* and *D* are purely real and *B* and *C* are purely imaginary. As well, reciprocity property of two-port networks also requires that Equation 3.6 must be satisfied. It is easy to see that $Z_{m,BO}$, $Z_{m,PEP}$, and $Z_{p,PEP}$ are complex. And their real part expressions are found to be

$$R_{m,BO} = \frac{D_2{}^2 R}{(D_1D_2)^2 - [(C_1D_2 + C_2D_1)R]^2} \quad (3.24)$$

$$R_{m,PEP} = \frac{D_2{}^2 R - j*(C_1D_2 + C_2D_1)R^2}{(D_1D_2)^2 - [(C_1D_2 + C_2D_1)R]^2} \quad (3.25)$$

$$R_{p,PEP} = \frac{-D_1{}^2 R + j*(C_1D_2 + C_2D_1)R^2}{(D_1D_2)^2 - [(C_1D_2 + C_2D_1)R]^2} \quad (3.26)$$

The above Equation 3.22 - 3.23 reveals that main and peaking impedances are determined by *ABCD* parameters of matching networks at two paths. And Equations 3.24 - 3.26 further illustrate the dependency of real parts on the network parameters. For continuous operation mode, the impedances shown to each path are of complex values and can vary versus frequency. But the real parts must

remain constant and are only determined by the power levels. Also, the absolute values of imaginary parts must not exceed the corresponding real parts [28]. So we have

$$Z_{m,BO} = R_{m,BO} + j * X_{m,BO}, \quad |X_{m,BO}| \le R_{m,BO} \tag{3.27}$$

$$Z_{m,PEP} = R_{m,PEP} + j * X_{m,PEP}, \quad |X_{m,PEP}| \le R_{m,PEP} \tag{3.28}$$

$$Z_{p,PEP} = R_{p,PEP} + j * X_{p,PEP}, \quad |X_{p,PEP}| \le R_{p,PEP} \tag{3.29}$$

For conventional Doherty power amplifier operating under the continuous mode, the main and peaking impedances will have real parts given by following equations

$$R_{m,BO} = 2 * R_{opt}{}^{B} \tag{3.30}$$

$$R_{m,PEP} = R_{opt}{}^{B} \tag{3.31}$$

$$R_{p,PEP} = R_{opt}{}^{B} \tag{3.32}$$

Combining Equation 3.30 - 3.32 and 3.24- 3.26, we can firstly conclude that $D_1=0$. And the expressions for main and peaking impedances can be further simplified in Table 3.1

Table 3.1: Summarized dependence of impedances to circuit parameters

Impedances	**Real Part**	**Imaginary Part**
$Z_{m,BO}$	$\frac{B_1}{C_1} G_L = 2 * R_{opt}$	$\frac{A_1}{C_1} = j * X_{m,BO}$
$Z_{m,PEP}$	$\frac{B_1}{C_1} G_L + j * \frac{B_1}{D_2} = R_{opt}$	$\frac{A_1}{C_1} = j * X_{m,PEP}$
$Z_{p,PEP}$	$j * \frac{A_2}{C_1} = R_{opt}$	$\frac{B_2}{D_2} = j * X_{p,PEP}$

As analyzed previously, in the scheme of conventional Doherty load modulation, it can be observed that operation modes of main and peaking amplifiers are class-C and -B, and that means [36]

1. Both the main impedance and peaking impedance are purely real.
2. The main impedance is $2R_{opt}{}^{B}$ until the specified back off power level and reduced to $R_{opt}{}^{B}$ at peak power level.

3. The peaking impedance is infinite at back off power level and R_{opt}^{B} at peak power.

4. Harmonics are terminated with ideal short circuits.

Combing the above statements and deduced expressions in Table 3.1, it can be seen that for conventional Doherty power amplifier, A_1 and B_2 must be zero, which provides only real to real impedance matching. The inverter which provides real to real matching, lumped or distributed, are narrow band. Attempts of enhancing the performance using doubly-terminated filter theory to achieve broadband matching proves to be effective in single-ended power amplifier design [32]. However, in Doherty power amplifier, the special group delay requirement for the matching network is difficult to satisfy in broadband and thus broadband matching theory cannot be simply employed. In above analysis, the A_1 and B_2 are allowed to take non-zero values and as a result, the impedances are complex whose imaginary parts are allowed to vary versus frequency. With imaginary parts controlled properly, the continuous design space can be exploited. Continuous operation mode is introduced into Doherty power amplifier without effecting the load modulation. The design flexibility of continuous class-B operation mode will eliminate the bandwidth limiting factors and broadband operation can be achieved.

3.3 Network Synthesis through Nonlinear Optimization

The starting point of nonlinear optimization is the Belevitch theorem [6]. The Belevitch theorem gives a criteria for checking whether a given S-parameter matrix can be constructed as a rational and lossless two port network. It is said in the theorem that: in the sense of network analysis, any networks composed of only lossless, reciprocal, passive, linear, and time-invariant elements can be described by its scattering parameter in form of:

$$S(s)=\frac{1}{g(s)}\begin{bmatrix} h(s) & f(s) \\ f(s) & (-1)^{nfz+1}h*(s) \end{bmatrix} \qquad (3.33)$$

where the *nfz* is the number of the finite zeros and *s* is real frequency which equals to $j\omega$. The polynomials at nominator, *h(s)* and *f(s),* and *g(s)* at denominator should satisfy the unitary condition which is required by the losslessness of the network

$$\left|S_{11}\right|^2+\left|S_{12}\right|^2=1 \qquad (3.34a)$$

$$|S_{22}|^2 + |S_{21}|^2 = 1 \quad (3.34b)$$

$$S_{11}{}^* S_{12} + S_{21}{}^* S_{22} = 0 \quad (3.34c)$$

Replacing the elements with the corresponding polynomials, we have

$$g(s)g(-s) = h(s)h(-s) + f(s)f(-s) \quad (3.34)$$

Also, to ensure the network can be realized through only passive elements, none of the poles should fall into the right half plane of complex frequency. And in reality, both capacitors and inductors are made of right-handed material meaning that permittivity and permeability of those reactive components could only take positive values. As a consequence, both capacitance and inductance are of non-negative values. These requirements, once reflected on the S-parameter matrix, are

1. The polynomial of *g(s)* must be Hurwitz polynomial.
2. And *h(s)* and *f(s)* must be real-positive(RP) polynomials.

The Hurwitz polynomials are referred to as polynomials the roots of whom are located only in the left-plane of complex plane. If *g(s)* is a Hurwitz polynomial, the network will contain only passive elements. Real-positive polynomials are polynomials that have only real and positive coefficients for items of all orders. This is to guarantee that the passive elements in this network will all take positive values.

It is necessary to explain the difference between this nonlinear optimization with the previously reported Simplified Real Frequency Technique (SRFT).The SRFT [33] is a simple while robust method for network synthesis methodology proposed by B. S. Yarman. After that it was successfully adopted in the design of antenna, LNA, and power amplifier. As an optimization solver, this technique could return results of reflection coefficient or transducer gain which are properly controlled or flattened in a broadband and those results can be realized through matching networks composed by only passive, lossless, linear and lumped or distributed elements. The network synthesis can be finished by applying systematic methods introduced in [35] or simply using low- or bandpass filter prototypes. In the original applications of SRFT, the coefficients of the above polynomials are optimized through nonlinear optimizer and the goal of the optimization is to maximally flatten the required transducer gain of amplifier or minimizing the reflection in a broad operation band. The load of the network to be synthesized can vary versus frequency but must be constant versus power level.

But as can be seen, in Doherty power amplifier design, the load at the junction is varying versus power level to modulate the amplifiers. And that means the spirit of SRFT must be modified to fit the design goal of Doherty power amplifier.

In this nonlinear optimization, the optimization variables are still coefficients of the three polynomials but the goal is no longer about the reflection or transducer gain from the source to the load. Instead, the S-parameter matrix is transformed into *ABCD* parameters at first. After that, optimization goals are set to drive the resultant *ABCD* matrices to approach the required *ABCD* values. Table 3.1 summarizes that A_1 and B_2 determine the imaginary parts of main and peaking impedance. Different from the conventional Doherty power amplifiers, A_1 and B_2 are allowed to be nonzero and vary versus frequency. But the variation is limited in a certain so that the resultant absolute value of these imaginary parts will not exceed their corresponding real part value. Following this procedure, the *ABCD* parameter matrices eligible for broadband Doherty power amplifier can be optimized.

3.4 Parasitics De-embedding

In the previous analysis, the *ABCD* matrices for main and peaking paths to provide Doherty load modulation are derived. But the analysis above is still established on the assumption that the transistors are ideal VCCSs and output matching networks implementing those *ABCD* parameters can be directly connected to the intrinsic current generator planes. As discussed in Chapter 2, the real transistor includes parasitics introduced by both packages or the internal active parts. Those parasitics issues, once improperly addressed, could impair the impedance matching resulting in the limited bandwidth, degraded efficiency and output power.

For designs of conventional Doherty power amplifier using $\lambda/4$ impedance inverter, the intuitive solution to parasitic caused issue is to optimize the electrical length and characteristic impedance of the inverter along with parasitics so that the quasi-lumped inverter [13] could mimic the behaviour of a standalone $\lambda/4$ inverter. Other attempts such as using the inverter built by lumped elements for parasitics absorption [8, 13] also follow this idea. The obvious disadvantage of that idea is that the parasitics can be absorbed in limited bandwidth around center frequency. And the imperfection of absorption will still limit the operation bandwidth. On top of that, parasitics adsorption will be more difficult when center frequency goes higher. Even the absorption is perfect, solutions in the scheme of using inverter (lumped or distributed) to provide load modulation will inevitably suffer from narrow operation bandwidth because the inverter itself is the intrinsic bandwidth limiter as stated in Chapter 2.

The usage of *ABCD* matrices in the above analysis gives an easy way for addressing the parasitics issue. Different with other representations of two-port networks, the *ABCD* and T parameters provide convenience in terms of the description for cascade connected networks. In the description through *ABCD* parameters, independent variables, as shown in Equation 3.1, are all defined at the output port and dependent ones are defined only at the input port. Meanwhile, the current at the output port takes the inward direction from that port but, in *ABCD* representation, it has minus sign. So from the physical meaning, we can see that if several two-port networks are connected in cascade, the output current from the previous stage can be directly used as the input of the following stage. As a consequence, the *ABCD* parameter of the overall cascade network is the product of *ABCD* matrices of all sub-networks in the order of the network connection. So to absorb the parasitics into the matching networks, we can simply synthesize the remainder network after the parasitics are de-embedded.

Parasitics at the output usually include capacitors such as C_{ds} and $C_{\_bond}$ *and* series inductors such as $L_{\_bond}$ and $L_{\_d}$. To de-embed the shunt capacitors, we can first specify the ABCD matrix of the shunt capacitor, which is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{shunt\_cap} = \begin{bmatrix} 1 & 0 \\ sC & 1 \end{bmatrix} \tag{3.35}$$

And the remainder matrix can be calculated by simply pre-multiplying the inverse matrix to the required *ABCD* matrix, which is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{int}rinsic} = \begin{bmatrix} 1 & 0 \\ sC & 1 \end{bmatrix} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{remainder} \tag{3.36}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{remainder} = \begin{bmatrix} 1 & 0 \\ sC & 1 \end{bmatrix}^{-1} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{int}rinsic} \tag{3.37}$$

And the series connected inductor can be described with the ABCD matrix as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{series\_ind} = \begin{bmatrix} 1 & sL \\ 0 & 1 \end{bmatrix} \tag{3.38}$$

Similarly, The corresponding de-embedding process is to do the premultiplication to the needed ABCD matrix which is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{int}rinsic} = \begin{bmatrix} 1 & sL \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{remainder} \quad (3.39)$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{remainder} = \begin{bmatrix} 1 & sL \\ 0 & 1 \end{bmatrix}^{-1} * \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{int}rinsic} \quad (3.40)$$

3.5 On the Termination of 2nd Harmonic

According to Equation 2.18a to 2.18c, for continuous class-B operation, the 2nd harmonic must be terminated with a reactive load which can be decided based on the imaginary part of fundamental impedances. The voltage waveform will always contain a 2nd harmonic component out phase with the imaginary fundamental part so that the dip of the waveform will not drop below zero and clip the transistor. If the fundamental and harmonic impedance strictly follow the relationship given in Equation 2.18, we will call the fundamental/harmonic impedances are matched with each other. It was shown in [34] that when the impedance pair are mismatched, the efficiency will suffer from degradation to a certain degree. And the amount of efficiency degradation was determined by the degree to which these two impedances are mismatched. The lowest efficiency below 40% occurs when the 2nd harmonic impedance has the same sign with the imaginary part of fundamental impedance. Reflected on the load pull result, the sensitive 2nd harmonic region can be observed on the Smith chart in which the efficiency drops significantly.

Also indicated in [34] is that there is a region at the package or intrinsic plane in which fundamental/harmonic impedance pair are mismatched but the resulted efficiency drop is slight. And this region is the targeted region of 2nd harmonic impedance placement. To achieve that, the bandpass filter prototype can be adopted. Observation of Equation 3.33, it is easy to conclude that for *f(s)* equals unit, the S-parameter matrix represents the typical lowpass filter. And if the polynomial of *g(s)* is one order higher than that of *f(s)* but shares the same order with *h(s)*, the driving point impedance seen from port 1 will show the band pass filter behavior. The operation frequency band can be arranged to overlap with the pass band and accordingly, the 2nd harmonic band will be the stop band. For bandpass filter implemented through lumped elements, driving point impedance in the stopband will be either open circuit (large impedance) or short circuit (small impedance). But for those implemented through distributed networks, the driving point impedance will be purely imaginary or with negligible real part. As discussed previously, once deviating from class-B operation, any other

operation mode in the scheme of class-B continuum requires purely imaginary 2nd termination. So the distributed elements are preferred. On the other hand, the methodology to address the parasitics absorption issue is introduced in previous sub-section. Naturally, one problem will arise questioning whether the ABCD parameters needed can be synthesized by a network with the first element a shunt capacitor. Actually, only lowpass or bandpass filter prototypes have this possibility. And thus the optimization will be initially set to provide bandpass filter behaviour.

The procedure of broadband Doherty power amplifier design can be summarized as:

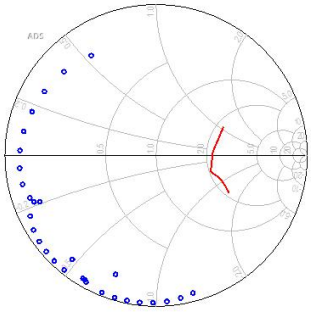
1. Determine the optimum impedance from load-pull or DCIV curve.
2. Calculate the needed parameters as listed in the summary table 3.1.
3. Realize the networks at the intrinsic plane by de-embedding the parasitics and providing proper 2nd harmonic termination.
4. Global optimization is needed of the assembled circuit to take into account of discontinuity or junctions.

Chapter 4

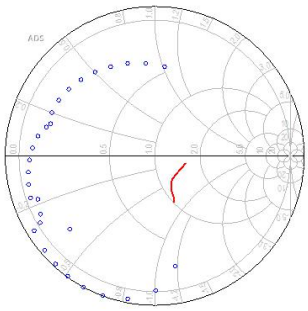
Broadband Doherty Power Amplifier Design and Measurements

4.1 Simulations

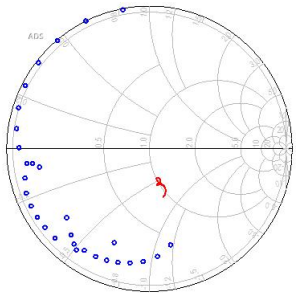
Based on the analysis developed in the previous, a broadband Doherty power amplifier was designed using packaged gallium nitride (GaN) high-electron-mobility-transistors (HEMTs) from Cree®. Cold-FET technology was used to extract the compact model and get access the intrinsic current generator plane. The two transistors used to finish the design are CGHV1F006S. The optimum impedance R_{opt} for class-B operation can be read from the DCIV curve or load pull. For this transistor, once biased at 28V drain voltage, the R_{opt} is 50 Ohm. Following the above methodology, the output combiner, is simulated on Rogers 4003C board. The targeted frequency range is 3 to 5GHz corresponding to fractional bandwidth of 50%. The combiner can show to main and peaking amplifiers (at current generator plane) the following impedances at fundamental and 2nd harmonic bands as can be seen in Fig 4.1. In the targeted frequency range, the real part of main and peaking impedances are almost constant while the imaginary parts are varying to exploit the design space. The real part of main impedance change from $2R_{opt}$ (100 Ohm) at back-off power level to R_{opt} (50 Ohm) at peak power level. And the peaking impedance has a real part of infinity at back-off power level and decreasing to R_{opt} at peak power level. The Doherty load modulation is maintained.



(a) Main impedance at back-off



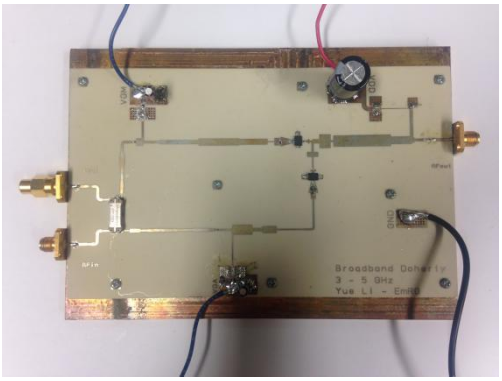
(b) Main impedance at peak power



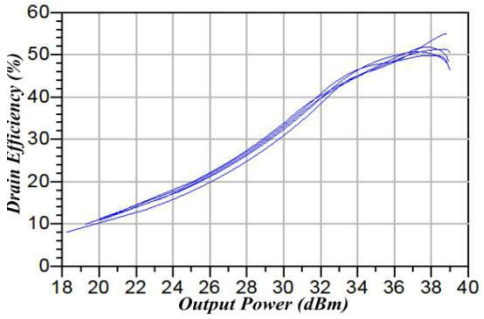
(c) Peaking impedance at peak power

Fig 4.1: Main and peaking impedances at various power level

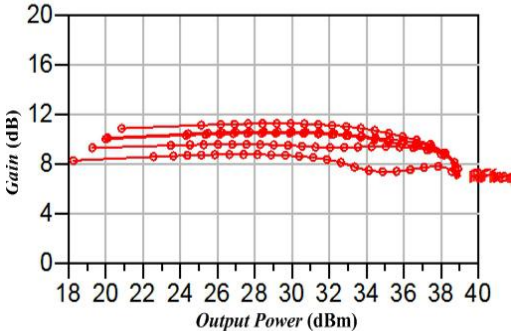
The red solid line is fundamental impedance and blue dots represents the 2nd harmonic impedance. The whole circuit layout and co-simulation results are shown in Figure 4.2 (b) and (c);



(a) Broadband DPA layout



(b) Simulated drain efficiency



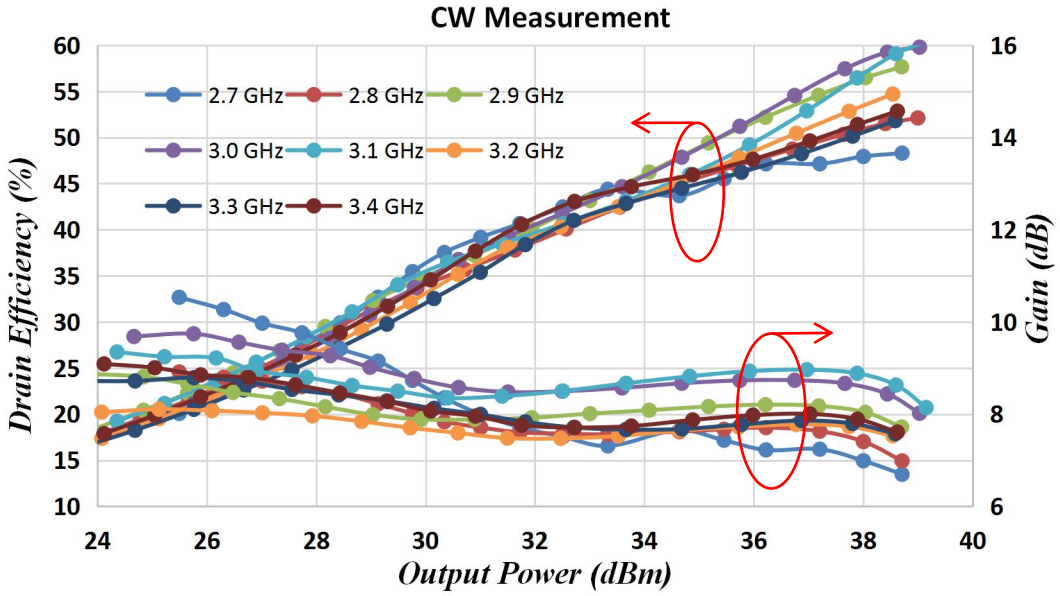
(c) Simulated transducer gain

Fig 4.2: Layout and simulation results from 3 to 5 GHz

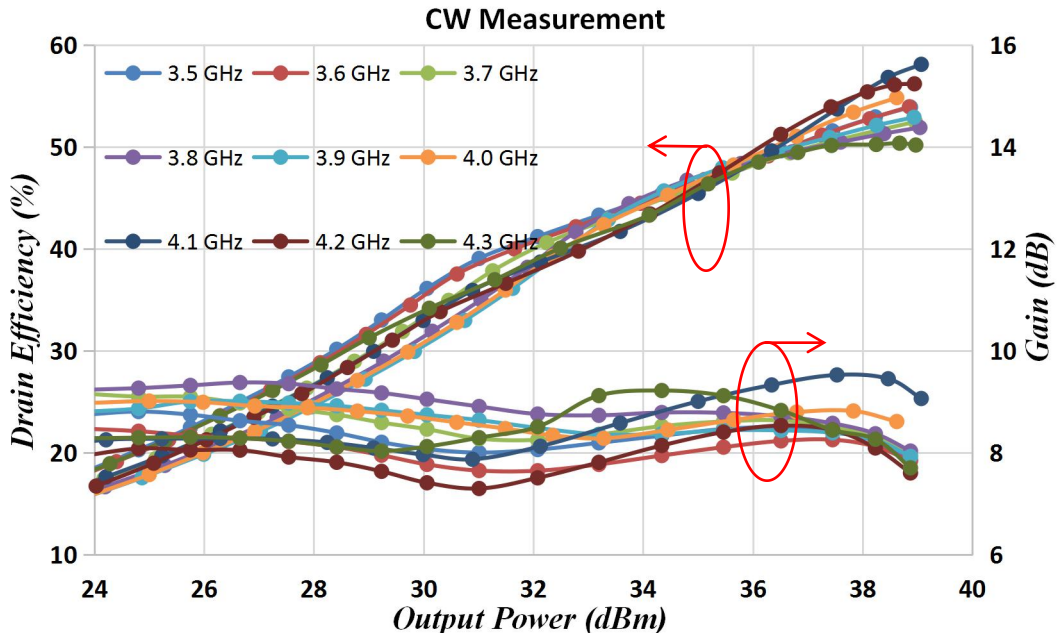
4.2 Measurements

As a validation of the simulation results, the Doherty power amplifier is fabricated on the substrate of Rogers4003C with the thickness of 20mil (Permittivity $\varepsilon_r=3.55$). Fig 4.2 (a) depicts the whole board assembled in home. At the RF input port, the commercial 90° hybrid coupler *IPP-7004* from Innovative Power Products® to provide the needed equal power division and nearly constant phase shift.

The performance of the Doherty power amplifier was first evaluated through continuous wave measurement. In this measurement, the duty cycle of the input signal is set to be 100%. So the performance of the Doherty power amplifier is presumably underestimated. The measured drain efficiency and gain versus output power level at different frequency points are illustrated in Fig 4.3.



(a) Performance from 2.7 to 3.4 GHz



(b) Performance from 3.5 to 4.3 GHz

Fig 4.3: Drain efficiency and gain performance under CW measurements

The variation of drain efficiency (at PEP and BO) and output power versus frequency is illustrated in Fig 4.4. In the range of 2.7 to 4.3 GHz (46% fractional bandwidth), the drain efficiency at 6 dB back off level varies in between 40% and 43%. And at PEP, the drain efficiency is 48.7% to 60%.

39dBm output power and gain of 8 to 10.5 dB can be obtained in the whole operation frequency range with very small fluctuation. At the peak output power, only around 1.4 dB gain compression was observed at all the selected frequency point, which gives a rough insight of the linearity of the power amplifier.

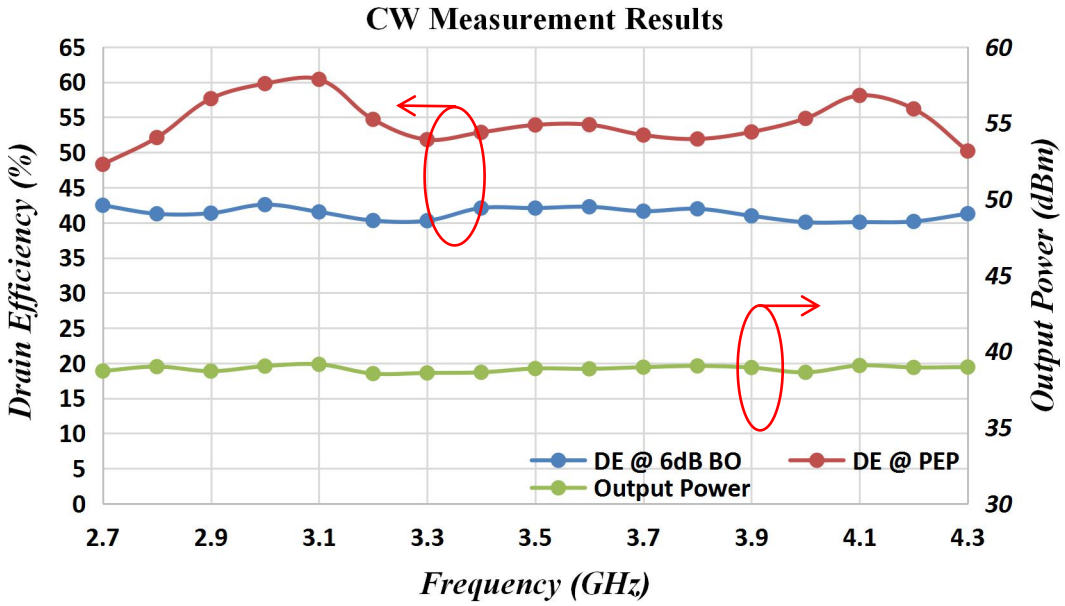
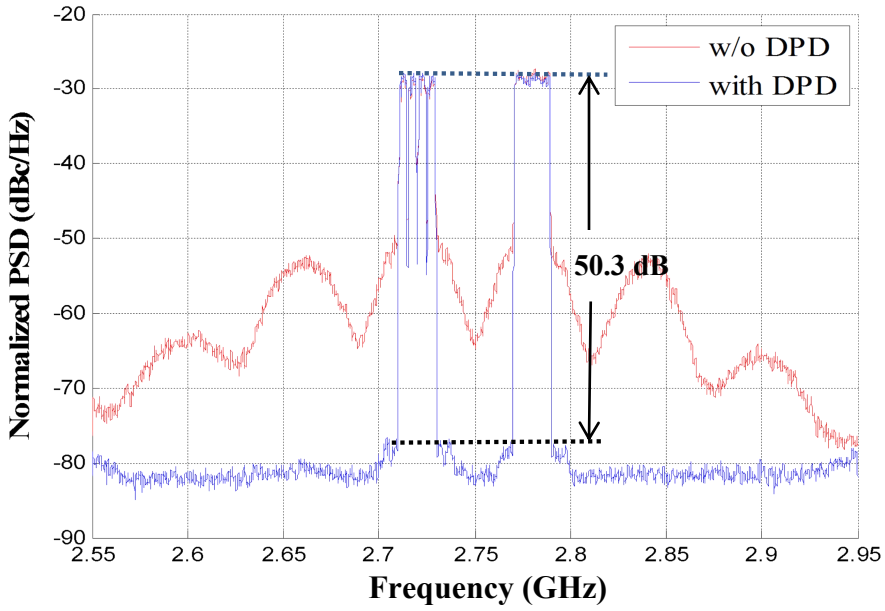


Fig 4.4: Drain efficiency and output power versus frequency under CW measurements

To look into the linearity of the amplifier deeper, modulated signal and concurrent dual band carrier aggregated signal test were carried out. In the modulated signal test, input signal is an intra-band 80 MHz WCDMA and LTE signal with the PAPR of 6.4 dB after clipping. Measurement results of 2.75 GHz were selected and shown in Fig 4.5



(a)

Fig 4.5: Measured output power spectrum at 2.75 GHz

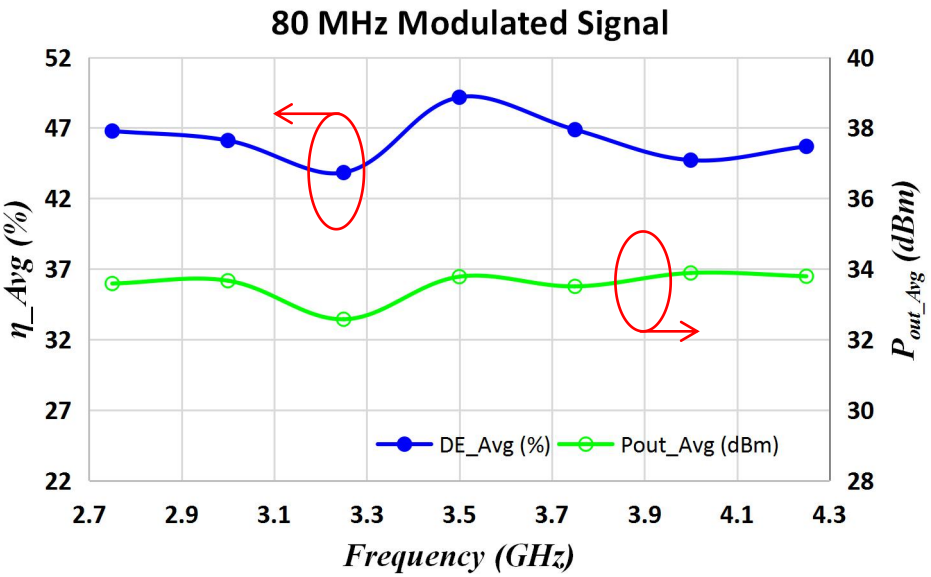


Fig 4.6: Measured average power and drain efficiency in frequency band 2.75 - 4.25 GHz.

The average efficiency and average output power versus frequency is depicted in Fig 4.6. Even with the PAPR of 6.4, the average power can be higher than 33 dBm. The relatively better

performance than continuous wave measurement results is mainly because the transistor is less susceptible to the thermal effect when using modulated signal as stimuli. As a consequence, the average drain efficiency is higher than that of CW measurement results (43% to 49%). Fig 4.7 shows the ACLR before and after DPD. The nearly 50 dBc ACLR after DPD in the whole frequency band is a proof of the good linearizability of the power amplifier.

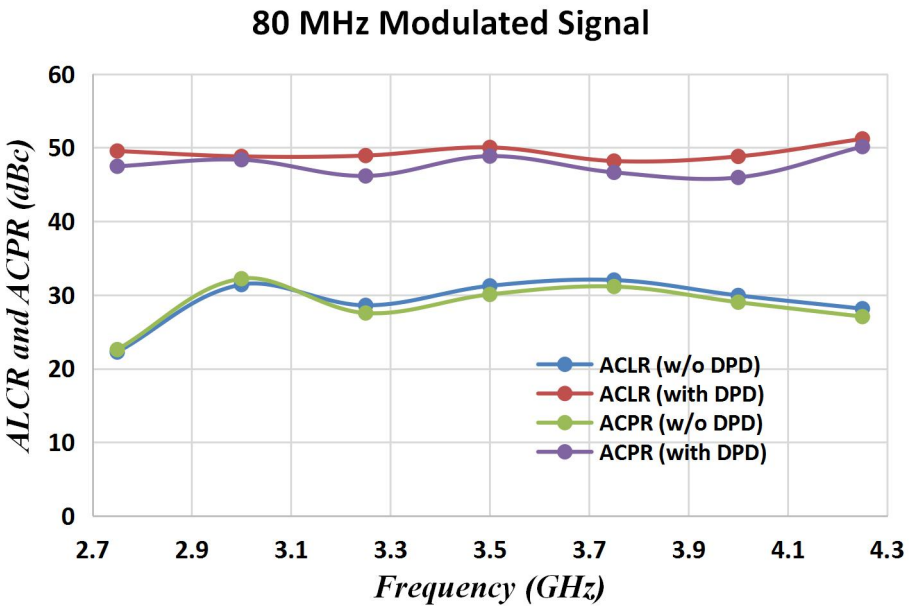
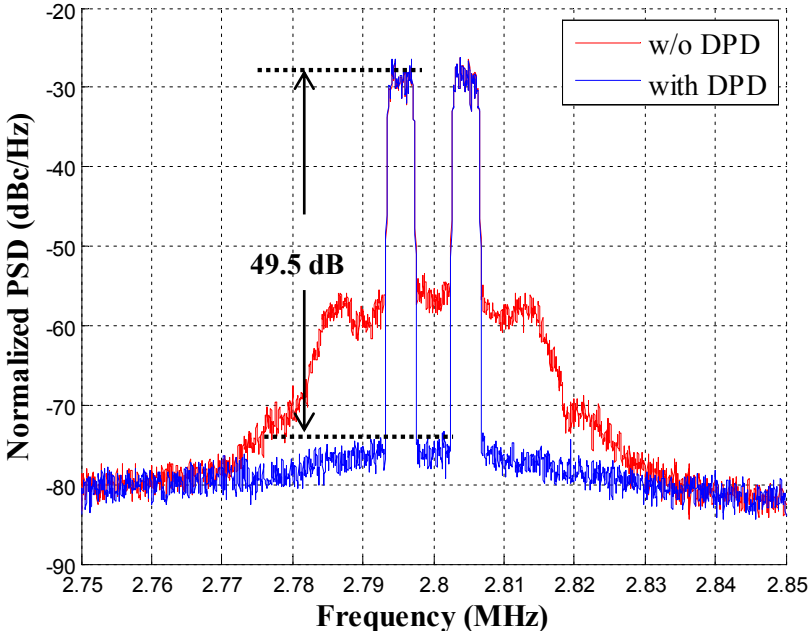


Fig 4.7: Measured ACLR before and after DPD in frequency band 2.75 - 4.25 GHz.

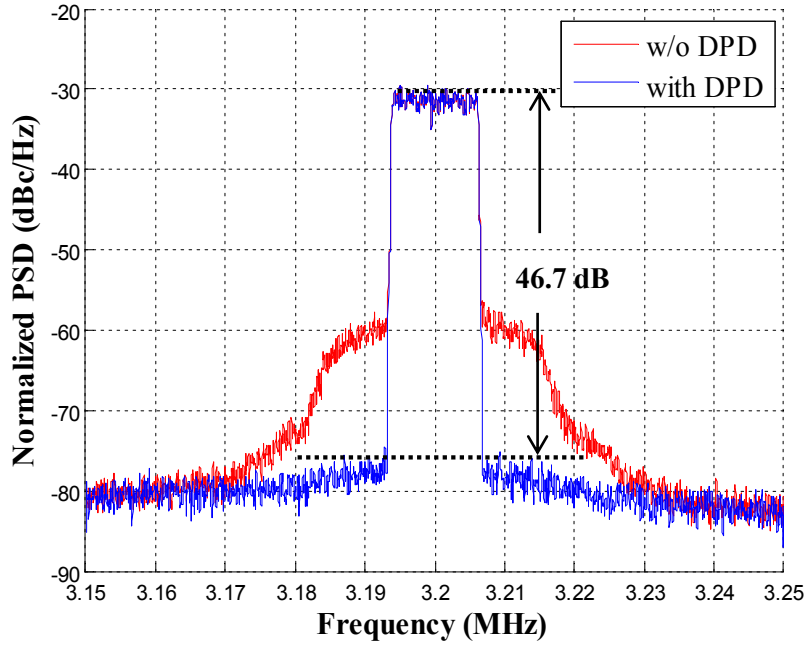
In reality, one application scenario of CA is inter-band non contiguous aggregation, which requires the power amplifier to concurrently process modulated signals whose carriers are spread into to two or more bands. To verify the amplification capability of this PA in this scenario, concurrent dual band test was carried out with 15 MHz modulated signals centered at 2.8 and 3.2 GHz. These dual band signals are 3C-WCDMA (centered in 2.8 GHz) and LTE (centered in 3.2 GHz). Using the dual-band DPD, the linearized output power has the spectrum with ACLR 49.5 dB at the lower band and 46.7 dB at the upper band. Fig 4.8 illustrates the measurement results before and after DPD. The PAPR of the output power at the lower and upper bands are 7.6 dB and 8.0 dB separately. The average output power is 32.3 dBm and average drain efficiency is 40.5%.

Thus far, the broadband operation, efficiency enhancement and linear amplification have been proved through continuous wave measurement and different carrier aggregation stimuli. Table 4.1 compares this work and some state of art progress reported in literature. Even though the targeted

50% bandwidth was not achieved, this design outperforms others in either high frequency operation, or efficiency and linearity.



(a)



(b)

Fig 4.8:Measured output power spectrum under inter-band WCDMA and LTE aggregated signals (15 MHz). (a) 2.8 GHz (b) 3.2 GHz.

Table 4.1: Comparison with published broadband DPAs

Ref.	Freq. (GHz)	Peak Power (dBm)	η_D (%) @ 6dB BO/ PEP	FBW (%)	Gain@6dB	Modulated Signals	
						Single Mode	Concurrent Mode
[13]	0.7-1	49	60/67	35	16	20 MHz	—
[14]	0.73-0.98	29	56(η-9dB)/ 55(η-6dB)/ 55	30	11	20 MHz	—
[9]	2.7-4.7	40-42	35-47/ 37-53	54	7.7-11	80 MHz	—
[25]	0.6-1.4	53	55/58	80	17	—	—
[36]	1.5-2.5	45-47	43-50/50-57	50	11-14	80 MHz	15 MHz
T.W	**2.7-4.3**	**39**	**40-43/48-60**	**46**	**8-10.8**	**80 MHz**	**15 MHz**

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis, firstly the demand imposed by the modern communication systems is discussed. It is natural that the application of carrier aggregation to improve the spectrum efficiency requires the radio transmitter to be capable to process wide-band signals at multiple carrier frequencies concurrently. Instead of resorting to power amplifier arrays whose units are controlled by switches, broadband power amplifier providing concurrent signal amplification is more attractive solution since the expense can be reduced. In addition to the wider bandwidth, signals resulted from the adoption of carrier aggregation intrinsically have high PAPR, which inspires the research interests in Doherty power amplifier as a solution to back off efficiency degradation problem.

Then rudimentary concepts about power amplifier and various operation modes are introduced, especially the continuous class-B mode and operation principles of Doherty power amplifier. In the literature review, it is clarified that the extant techniques of DPA design are either limited by deficiency in parasitics absorption so that their application is narrowed to only low frequency, or by the unsolved 2^{nd} harmonic termination issue so that the bandwidth extension is restricted. Furthermore, previous design methodologies rely highly on the optimization, which, in some cases, will lead to suboptimum solutions due to the lack of theory support.

So following in this thesis, the continuous class-B operation mode is introduced into Doherty power amplifier design to exploit the potential of extended design space and achieve broadband operation. To do that, a systematic methodology for designing matching and combing networks enabling the amplifier units to operate under continuous modes is proposed. By transforming the three-port combiner network of the DPA into two separate two-port networks, the application of two-port network theory allowed for a systematic determination of the circuit parameters. And the synthesis process is done by nonlinear optimization algorithm which minimizes the difference between the desired and achievable ABCD parameters versus frequency. Parasitics absorption is done by de-embedding and the 2^{nd} harmonic termination is controlled using the bandpass filter response. The first pass design of a proof-of-concept DPA prototype confirmed the excellent drain efficiency at 6dB back-off and peak power of about 40-43% and 48-60%, respectively, over the bandwidth of

2.70-4.30 GHz with a peak power of about 39dBm and a small signal gain of about 9dB. Measurement conducted using carrier-aggregated modulated signal with 80MHz modulation bandwidth confirmed its linearizability. Using generalized memory polynomial digital predistortion technique, the ACLR is around 50 dB while achieving around 46% average efficiency for an average output power of 33dBm. In the inter-band dual band test, two 15 MHz modulated signals (WCDMA and LTE) centered at 2.8 and 3.2 GHz are used as stimuli. The output power has 7.6 and 8.0 dB PAPR in each band. And the average power is 32.3 dBm with average drain efficiency 40.5%.

5.2 Future Work

The measurement results of the DPA prototype demonstrate the efficiency enhancement at 6 dB back off. But in reality, the PAPR of the carrier aggregated signals can be as high as 9 or 10 dB. And because the theory so far has been developed is based on the operation of conventional two-way Doherty power amplifier, attempts to extend the efficiency enhancement at wider back off is necessary. This can be achieved by modifying the current profile or utilizing multi-way Doherty configuration.

This design is firstly targeting the operation frequency band of 3.0 to 5.0 GHz (50% FBW). While the measurement results show a frequency down-shift to 2.7 to 4.3 GHz (50% FBW). This can be because of the inaccuracy of the transistor model or the discrepancy between the actual permittivity with nominal one. Even though this problem is quite common in RFPA design, it is still necessary to investigate the source of this shift so that in the future, the design process can be more empirically directed. This will be done by reproducing the measurement results in simulation while tuning the variables such as the permittivity of substrate.

With the advent of the 5G age, higher frequency range or even millimeter wave frequency will be further exploited. Progress in semiconductor technologies such as silicon-on-insulator (SOI), has lowered down the channel loss and made possible of the power amplifier design at millimeter wave frequencies. So another possible direction in the future is how to apply the proposed theory in IC Doherty power amplifier design. The synthesis should be done using only lumped components and the matching and combining networks will be lossy. But fortunately, there is theory about lossy networks.

Lastly, we must notice that except for continuous class-B, there is also extended design space for other operation modes, which also requires constant real part of fundamental impedances. So it is

worth considering to modify my proposed method for introducing those operation into Doherty power amplifier design with the hope of broadband operation and high efficiency.

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