0.42 THz Transmitter with Dielectric Resonator Array Antenna

by

Hamed Holisaz

A thesis

presented to the University of Waterloo

in fulfillment of the

thesis requirement for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2019

EXAMINING COMMITTEE MEMBERSHIP

The following served on the Examining Committee for this thesis. The decision of the Examining Committee is by majority vote.

External Examiner: Ehsan Afshari
                                                Associate Professor
                                  Electrical Engineering & Computer Science
                                                University of Michigan

Supervisor: Safieddin Safavi-Naeini
                                                   Professor
                                  Electrical and Computer Engineering

Internal Members: Raafat Mansour
                                            Professor and Director
                                  Electrical and Computer Engineering

                                               Vincent Gaudet
                                             Professor and Chair
                                  Electrical and Computer Engineering

Internal-External Member: James Martin
                                               Associate Professor
                                            Physics and Astronomy

AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

ABSTRACT

Off chip antennas do not occupy the expensive die area, as there is no limitation on their building material, and can be built in any size and shape to match the system requirements, which are all in contrast to on-chip antenna solutions. However, integration of off-chip antennas with Monolithic-Microwave-Integrated Chips (MMIC) and designing a low loss signal transmission from the signal source inside the MMIC to the antenna module is a major challenge and trade off. High resistivity silicon (HRS), is a low cost and extremely low loss material at sub-THz. It has become a prevailing material in fabrication of passive components for THz applications. This work makes use of HRS to build an off-chip Dielectric Resonator Antenna Array Module (DRAAM) to realize a highly efficient transmitter at 420 GHz. This work proposes novel techniques and solutions for design and integration of DRRAM with MMIC as the signal source. A proposed scalable 4×4 antenna structure aligns DRRAM on top of MMIC within 2 μm accuracy through an effortless assembly procedure. DRAAM shows 15.8 dB broadside gain and 0.85 efficiency.

DRAs in the DRAAM are differentially excited through aperture coupling. Differential excitation not only inherently provides a mechanism to deliver more power to the antenna, it also removes the additional loss of extra balluns when outputs are differential inside MMIC. In addition, this work proposes a technique to double the radiation power from each DRA. Same radiating mode at 0.42 THz inside every DRA is excited through two separate differential sources. This approach provides an almost loss-less power combining mechanism inside DRA. Two 140 GHz oscillators followed by triplers drive each DRA in the demonstrated 4×4 antenna array. Each oscillator generates 7.2 dBm output power at 140 GHz with -83 dBc/Hz phase noise at 100 KHz and consumes 25 mW of power. An oscillator is followed by a tripler that generates -8 dBm output power at 420 GHz. Oscillator and tripler circuits use a smart layer stack up arrangement for their passive elements where the top metal layer of the die is grounded to comply with the planned integration arrangement. This work shows a novel circuit topology for exciting the antenna element which creates the feed element part of the tuned load for the tripler circuit, therefore eliminates the loss of the transition component, and maximizes the output power delivered to the antenna. The final structure is composed of 32 injection locked oscillators and drives a 4×4 DRAAM achieves 22.8 dBm EIRP.

ACKNOWLEDGEMENT

… To the loving memory of my grandpa, Hossein Holisaz

… To my parents, my beautiful wife, and my two sweet angels Parmida and Atreesa

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AiP: Antenna in Package

AoC: Antenna on-Chip

CIARS: Centre for Integrated Antenna and Systems

CPWG: Co-Planar Waveguide Grounded

DR: Dielectric Resonator

DRA: Dielectric Resonator Antenna

DRAAT: Dielectric Resonator Antenna Array Tray

DRAAM: Dielectric Resonator Antenna Array Module

DRIE: Deep Reactive Ion Etching

EIRP: Effective Isotropic Radiated Power

FBO: Feedback Buffer Oscillator

HTCC: High Temperature Co-fired Ceramic

HRS: High-Resistivity Silicon

LTCC: Low Temperature Co-fired Ceramic

MTL: Microstrip Transmission Line

MS: Microstrip

MMIC: Monolithic Microwave Integrated Circuit

OOK: On/Off Key

SOG: Silicon On Glass

TL: Transmission Line

TRX: Transceiver

CHAPTER 1   Introduction to THz Source

The Terahertz (THz) region of the electromagnetic spectrum is situated between infrared light and microwave radiation. Here, THz range is accepted as the range within 0.1-10 THz. THz technology is one of the emerging technologies that has applications in high-resolution THz imaging [1], spectroscopy of large bio-molecules like DNA [2], gas analysis [3], [4], and sub-μm-precision vibrometry based on the Doppler effect [5].

Half of the luminosity of the universe and 98% of all photons emitted since the Big Bang belong to THz radiation [6], containing information about the cosmic space, galaxies, stars and planets formation. The interstellar dust has a spectrum profile that ranges from λ=1 mm to 100 μm (14 - 140 K below the ambient background on the earth). Historically, chemists and astronomers were the first who used THz spectroscopy for spectral characterization of the rotational and vibrational resonances and thermal-emission lines of molecules. Figure 1.1 shows the radiation spectrum of interstellar (dust, light and heavy molecules), a 30 K blackbody, and the 2.7 K cosmic background [7]. Through THz spectroscopy astrophysicists can probe into the early universe, star forming regions, and many other abundant molecules.

Air absorbs a THz signal power in wide spectral regions (except for narrow windows around f=35 GHz, 96 GHz, 140 GHz, and 220 GHz, and others shown in Fig. 1.2). Therefore, THz and millimeter waves are efficient at detecting the presence of water and therefore, are efficient to discriminate different objects on human body (water content of human body is about 60%) as clothing is transparent. In the longer wavelength region ($f < 30$ GHz) persons hiding behind a thin wall can be detected. In THz active imaging systems emission radiation frequencies should be inside an atmospheric transmission windows to avoid strong water vapor absorption.
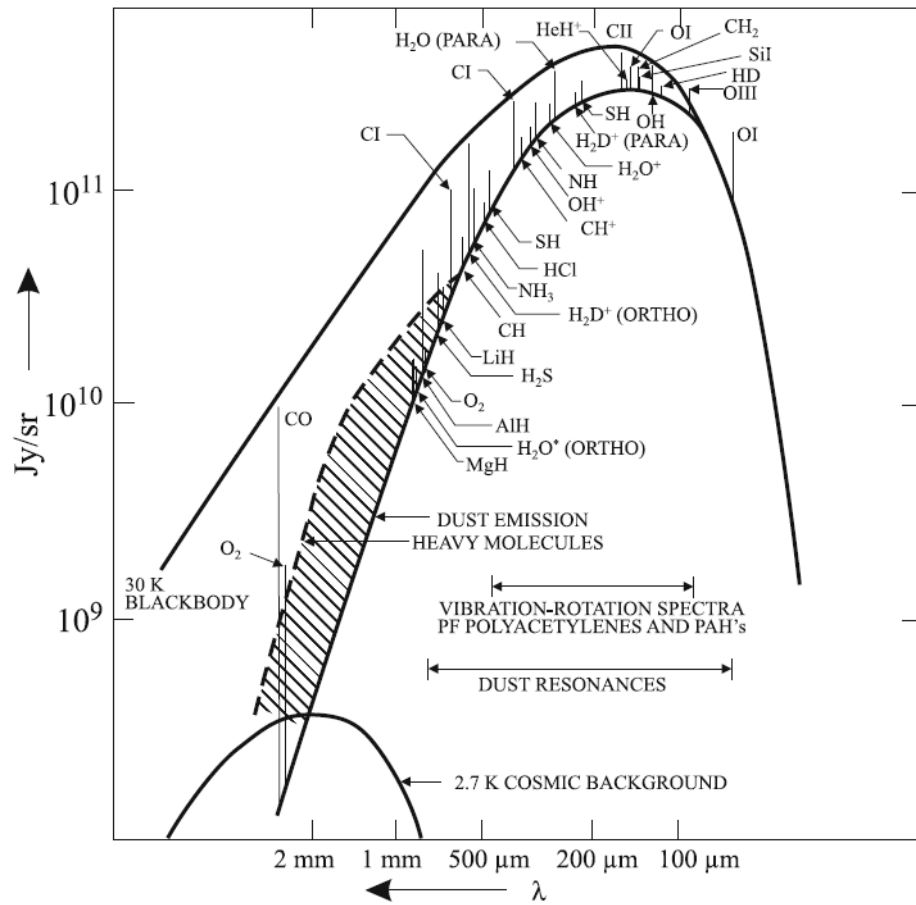
Fig. 1.1. Radiation signature of 30 K blackbody. Dust and heavy molecules have emissions at THz frequencies [7]
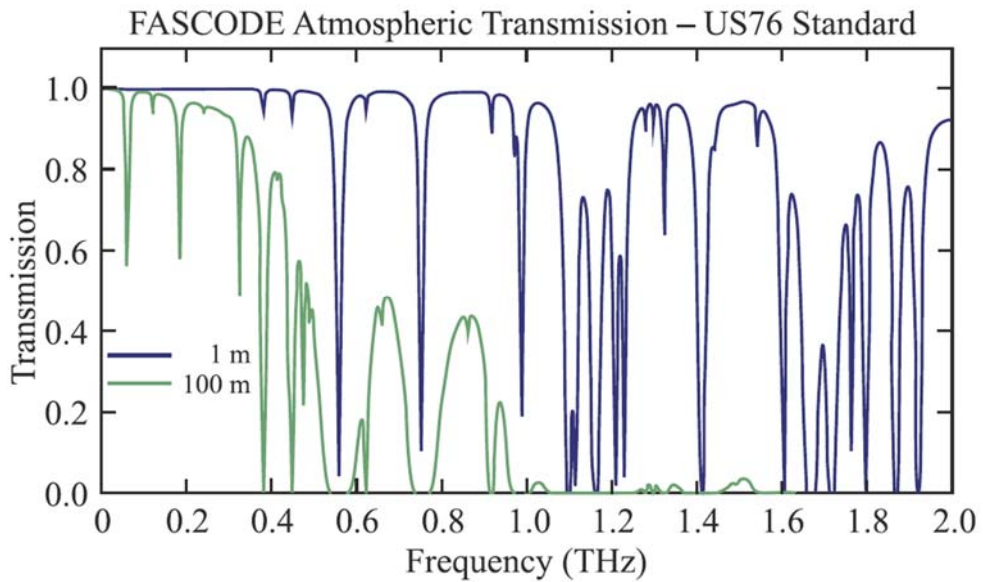
Fig. 1.2. Transmission of THz signal in air at two different raining conditions

Due to strong absorption, the transmission spectra of a lot of materials can provide information about the physical properties of the materials investigated. An interesting application of THz radiation is the ability to penetrate and distinguish between non-metallic materials.

In many of these applications THz transmitter and receivers require sources with reasonable output power in the range of 25 to 50 mW. However, the realization of high efficiency signal generation is a challenge as THz frequencies are too high for conventional electronics and the photon energies are too small for optical methods. In other worlds, THz radiation is quite difficult to generate by the techniques commonly employed in the well-established neighbouring bands.

A high-efficiency THz source consists of two fundamental components. One is the electronic circuit that generates the THz signal source, another is the antenna that radiates the THz signal. Chapter 2 describes the high efficiency oscillator at 140 GHz proposed in this research. The MMIC is composed of 32 injection locked oscillators which are all connected to an on-chip central oscillator through an H-tree network. Chapter 3 describes the implementation of the H-tree network with the transmission line inside the MMIC. The design of antenna array which is realized with HRS dielectric resonator antennas is described in Chapter 4. This work targets a 420 GHz transmitter by 3rd harmonic signal generation from the 140 GHz oscillator. In Chapter 5 an active tripler circuit that follows the 140 GHz oscillator and its co-design with the dielectric resonator antenna is described. The top architecture of MMIC is described at the end of Chapter 5. Antenna array fabrication and its integration with the MMIC is described in Chapter 6. Measurement result of the integrated transmitter is described at the end of Chapter 6. We finally conclude this research in Chapter 7.

In the following of this chapter, we briefly review some important sub-THz phase array transceivers (TRX) reported in recent years. It begins by reviewing the work done on THz array transceivers, and then reports the most fundamental work previously completed on critical components such as frequency synthesis, antenna and the interconnect aspect of THz chips.

1.1 Integrated Antenna Array Systems and Transceivers

In order to generate sufficient THz radiation power for practical applications, a multi-antenna/element source with free-space power combining is preferred. Many of the published transceiver designs above 200 GHz utilize integrated on-chip antenna arrays due to the propagation

loss of the signals at THz. However, antenna on-chip (AoC) hardly provides the best in class efficiency. One of the pioneer works, published in [8] reports a 0.38 THz single transceiver in SiGe BiCMOS, using two patch antennas with simulated gain of 6.6 dBi and radiation efficiency of $\eta_{rad} = 46\%$. In 32nm SOI CMOS process, [9] demonstrates a 210 GHz TRX incorporating a 2×2 on-chip dipole TX antenna. A 260 GHz fully integrated non-coherent OOK transceiver is presented in [10] in 65nm CMOS using a half-width leaky-wave on-chip antenna. A distributed array radiator (DAR) is introduced in [11]. The authors have developed a 4×4 on-chip radiating array in 45nm SOI CMOS, with an EIRP of 9.4 dBm at 0.28 THz. A 110 GHz 4×4 transmitter in SiGe BiCMOS is reported in [12]. It uses on-chip quartz antennas with 45% simulated efficiency. The on-chip antennas are implemented using a 100 μm thick quartz substrate which is attached to the silicon RFIC with epoxy.

IBM researchers have shown an Antenna-in-Package (AiP) that uses a folded dipole antenna suspended in a metal cavity using plastic mold injection technology with 90% efficiency for 60 GHz radio [13]. Toshiba engineers have demonstrated another AiP, with bonding wires, forming a three-dimensional triangular loop which has some distance from the chip [14]. A 245 GHz transmitter (TX) with an on-chip antenna has been realized in [15] in SiGe BiCMOS, which consists of a push-push VCO followed by a frequency doubler and a transformer coupled one-stage power amplifier. With localized backside etching for the on-chip antenna, the authors have been able to achieve 75% gain and more than 7 dBi in simulation. A 4×4 element I-Q W-band (85–95 GHz) transceiver is implemented in [16] in 45nm SOI CMOS.

A less complex way of beam forming can be achieved through beam-switching. [17] presents a 220–240 GHz four-element Butler matrix beam switching chip in SiGe BiCMOS technology with 2 dB insertion loss at 220 GHz. From the same authors, [18] reports a 220–250 GHz phased-array circuits in BiCMOS. This is one of the few articles that employs a fully RF phase shifting architecture at this range of frequencies. Each channel exhibits 360° phase control with 18 dB of amplitude control.

In [19] and [20], THz phased arrays based on inter-coupled harmonic oscillators were proposed in a 130nm SiGe technology and a 65nm CMOS technology, respectively. In [21], a phased array based on amplifier–multiplier chains was implemented at 0.4 THz using a 40nm CMOS technology. A short comparison between the discussed work is shown in Table 1-1.

1.2 Sub-THz Frequency Synthesizers

A significant challenge in building a low-cost sub-THz system is the design and development of a low-phase noise and efficient signal source. This is due to high DC power consumption and low efficiency of the solid-state frequency synthesizers. The so-called Mason's invariant, or the unilateral power gain of a transistor decreases by a slope of 20 dB/dec beyond $f_{max}/2$ and becomes unity at f_{max} [22]. The f_{max} of today's silicon technologies has not been improved enough by scaling down the device sizes to cover the THz gap. In addition, three main factors which are: the loss of passive elements, skin effect, and EM coupling to lossy substrate reduce the realizable fundamental frequency of an oscillator much lower than f_{max} of the technology.

Table 1.1. A short comparison between the recent work

	Freq. (GHz)	Prad (dBm)	PDC (W)	DC-to-THz Eff. (%)	EIRP (dBm)	Antenna Type	Config.	Tech.
[19]	344	-6.8	0.64	N/A	4.9	2×2 Patch	Inter-Coupled Osc.	130nm SiGe
[20]	338	-0.9	1.54	0.53	17	4×4 Patch	Inter-Coupled Osc.	65nm Bulk CMOS
[21]	390	-7	1.5	0.13	8	1×8 Patch on Quartz	Multiplier	45nm SOI CMOS
[23]	530	-12	0.156	0.4	25	4×4 Ring with Silicon Lens	Non-Coherent Osc.	130nm SiGe
[24]	553	-27	0.172	0.01	N/A	Ring with Silicon Lens	No Array PLL	65nm Bulk CMOS
[25]	546	-9	1.3	0.1	24.4	2×4 Ring with Silicon Lens	Inter-Coupled Osc.	65nm Bulk CMOS
[26]	428	-6.8	0.164	1.42	15	Slot with Silicon Lens	No Array Osc.+Multiplier	130nm SiGe
[27]	1010	-10.9	1.1	0.074	13.1	6×7 Slot with Silicon Lens	Inter-Coupled Osc.	130nm SiGe
[28]	528	-22	0.019	0.332	-7.4	Slot with Dielectric Lens	No Array Osc. + Multiplier	28nm Bulk CMOS
[29]	342	-10.5	0.425	0.21	1.2	1×4 Patch	Inter-Coupled Osc.	130 nm SiGe
[8]	380	-13	0.364	NA	-13	2×2 Patch	Harmonic Osc.	SiGe BiCMOS
[30]	160	5.5	2.2	NA	18.8	4×4 Patch-In-Package	I-Q Array Active Multiplier	65nm CMOS
[31]	144	10.1	0.457	NA	NA	Bondwire dipole Dielectric Lense	No Array Active Multiplier	65nm CMOS
[10]	260	13	1.17	NA	5	2×2 On-Chip Leaky-wave	Osc. + Active Multiplier	65nm CMOS
[11]	280	9.4	0.820	NA	-9	4×4 On-Chip Loop	Dist. Osc. + Active Mult. chain	45 nm SOI CMOS
[12]	110	1	3.4	NA	23	4×4 On-chip Dipole + Off-chip Dielectric Quarts	Single Osc. + power-divider	SiGe BiCMOS
[15]	245	1	0.380	NA	7	On-chip Dipole	No Array	SiGe BiCMOS
This Work	**420**	**7**	**0.7**	**0.7**	**22.8**	**4×4 Off-Chip DRA**	**32 Injection locked Osc.**	**65nm CMOS**

In order to generate THz frequencies beyond the f_{max} of the technology, two approaches have been followed in literature. The first approach is the use of harmonic oscillators, the second is through multipliers. Harmonic oscillators [32], occupy less chip real estate and consume less

DC power, but generally at the cost of a higher phase noise level when compared with the multiplier chain solution driven by ultra-stable low-frequency sources. In Harmonic oscillators, odd-harmonic or even harmonic of the fundamental frequency is extracted from a differential or common point of the oscillator circuit, respectively. Examples of the harmonic oscillators include "*push-push*" topologies (where the second harmonic is sensed) or "*edge-combining*" arrangements [33], also known as "*linear superposition*" [34] or " *N-push*" oscillators [35] [32]. Super-harmonic oscillators, typically provide only a single-ended output. If the application requires a differential output, they require Baluns, 90° couplers and buffers. In addition, the finite lower harmonics that leak to the output of a super harmonic topology may down-convert unwanted signals in a receiver. Creative signal source designs beyond 0.5 THz, based on harmonic oscillators, have been proposed in [28] [23] [24] [27]. A systematic approach applied for the design of CMOS N-push oscillators achieved an output power of -17 dBm at 256 GHz and -7.9 dBm at 482 GHz employing 3-stage single-ended ring topologies in a 130nm and a 65nm CMOS process node, respectively [36]. In [32], a triple push oscillator is designed using an optimal bias point proposed by the same researchers in their previous work. Harmonic oscillators are also implemented to realize tunable VCOs [37]. A high output power tunable VCO, utilizing eight pairs of oscillator-phase shifter/coupler and extracting the fourth harmonic to create an output at 256 GHz is shown in [38]. Signal sources at 220-330 GHz using SiGe HBT technology, have been demonstrated in [39], using a Colpitts–Clapp push-push topology.

In the second approach for generating frequencies above f_{max}, an active [40] or passive [37] multiplier is driven by a fundamental oscillator. An output power of -6.6 dBm at 244 GHz using a travelling-wave doubler in 65nm CMOS is shown in [40] [41]. Authors in [42] and [43] reported multiplier circuits in 0.13μm SiGe HBT with output power of -3 dBm at 325 GHz and -29 dBm at 825 GHz, respectively.

Another approach which vastly effects the performance of the oscillator circuit is the use of III–V technologies, such as InP [44], InAs [45], InGaAs [46], versus silicon-based Si/SiGe technologies. III-V devices in general offer better power and f_{max}. State-of-the-art fundamental frequency oscillators at 573 GHz with an output power of -19 dBm have been reported using InP DHBT device (f_{max} = 850GHz) [47]. Multiplier circuits in III-V MMICs at 300 GHz and 195 GHz are demonstrated in [48] to have an output power of -6 dBm and 0 dBm, respectively. The circuit topologies and integration solution proposed in this project is not limited to silicon-based or III-V

technologies for the MMIC and can be applied in both technology flows. However, our choice of TSMC65nm was due to the accessibility and lower fabrication costs of this technology.

1.3 Packaging and Antenna Module

The integration of THz phased arrays systems, [49] [50] at sub-THz frequencies requires low-loss transmission lines to distribute high frequency signals efficiently between the transceiver IC and other off-chip system components, such as antenna. Use of low or high temperature co-fired ceramic (LTCC/HTCC) substrates [51] [52], or organic packages and PCBs such as Liquid Crystal Polymer (LCP) [53] [54] [55] [56] have been tried before for system integration at sub 150 GHz. Fig. 1.3 shows typical layer stacking arrangements with these two approaches. A 2×2 160 GHz pulse transceiver in CMOS is reported in [57] using FR4 for the antenna substrate which shows 18 dBi directivity in simulation.
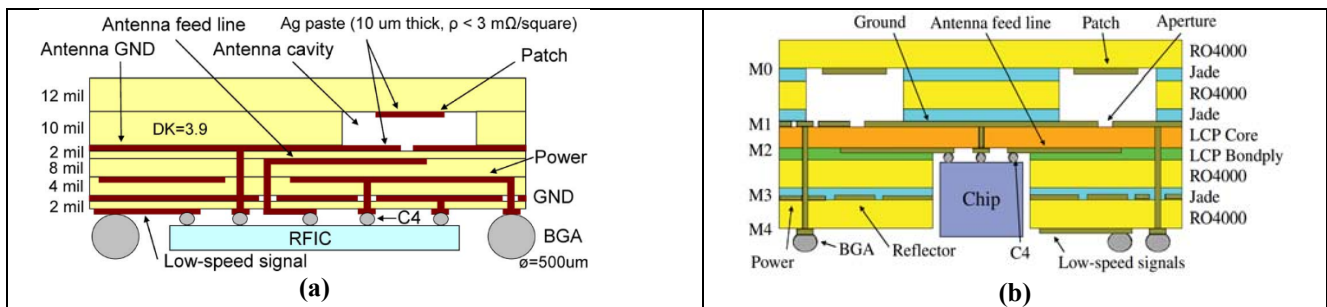
Fig. 1.3 (a) LTCC package arrangement [52]. (b) Organic packaging [53]

This work does not repeat any of the aforementioned and conventional integration techniques. Instead, it is based on a new idea of using a much superior material HRS. The HRS has been used to implement dielectric waveguides in photonic applications. A high field confinement inside silicon waveguides is well suited for creating low-loss transmission lines at THz frequencies. Realization of fully dielectric waveguide interconnects with IC-compatible processes has not been shown yet. The most pertinent work that has been done in this field is published in [58], where authors have developed a HRS-filled metallic-waveguide. They have shown how the metal on the top face of the waveguide can be patterned to implement slots for integrating antennas. Their work is essentially a metallic waveguide that will still suffer from the metallic losses at higher frequencies. Researchers at the Centre for Intelligent Antenna and Radio Systems (CIARS) at the university of Waterloo, have fabricated and measured many types of HRS

7

passive structures, e.g. dielectric waveguides [59] and antennas [60] [61] with exceptional performances at THz frequency. [61] shows a fully silicon five-beam annular grating antenna at 77 GHz with a remarkable radiation efficiency of 91% and a bandwidth of 5 GHz. This antenna has the advantages of low-cost, planar structure, ease of fabrication and integration in a silicon-platform. The work reported in [60] shows another high efficiency antenna on high resistivity silicon (HRS) at 60 GHz. The same antenna has been fabricated on a new integrated technology platform called silicon-on-glass (SOG), using photo-lithography and dry etching of the Si layer of the SOG wafer [59]. This work is going to use the same superior methodologies and technologies developed at CIARS over the past few years, to utilize HRS for implementation of dielectric resonator antennas. In addition, this work proposes a novel solution to directly couple a MMIC to an off-chip HRS antenna module.

CHAPTER 2 Frequency Synthesizer

A high efficiency continuous-wave (CW) signal generator at 420 GHz, beyond f_{max} of the TSMC65nm technology node, is implemented in this work. In our design, a frequency multiplier which is a tripler circuit, follows an oscillator at 140 GHz. The oscillator uses a transmission line for the inductor of the resonator tank. This high Q implementation of the tank has achieved a record phase noise. A new topology called "*buffer-feedback oscillator*", in which the peaking inductors of the VCO buffer couples to the VCO tank is implemented in [62]. Our circuit uses a similar buffer feedback mechanism, but uses transmission line which reduces the total circuit loss.

2.1 Oscillation Close To f_{max}

f_{max} is defined as the frequency at which the unilateral power gain of an active device falls to unity. Therefore, it is believed that f_{max} set the upper limit on the oscillation frequency. Based on the small signal model of a MOSFET, and ignoring the effect of drain-bulk junction capacitance, C_{DB}, it can be shown that for a MOSFET:

$$\omega_{max}^2 = \frac{g_m^2 r_o}{4R_G\,(C_{GS} + C_{GD})[C_{GS} + (1 + g_m r_o)C_{GD}]} \tag{2.1}$$

R_G denotes the lumped equivalent value of the gate resistance [16]. The effect of drain-bulk junction capacitance (C_{DB}) is ignored, as the transistor is assumed to be a unilateral device and embedded within a lossless network. A unilateral device nulls the effect of C_{DB}, as the input and output ports of the device are matched for maximum power transfer. Achieving an oscillation frequency near f_{max} from an actual design is almost impossible because of the loss of on-chip interconnects and passive network. My simulations predicted an f_{max} of roughly 280 GHz for 65nm nMOS devices (using lumped BSIM4 model) with a drain current density of 0.8 mA/μm. This current density differs from the value of 0.3–0.4 mA/μm recommended in [63] for maximum f_T. Gate resistance could be a cause of this discrepancy which directly impacts f_{max} but not the f_T [64]. A capacitor-less cross-coupled LC oscillator topology is used in this work, due to its robust operation when implemented using MOS devices. Fig. 2.1 shows a simplified version of this topology.
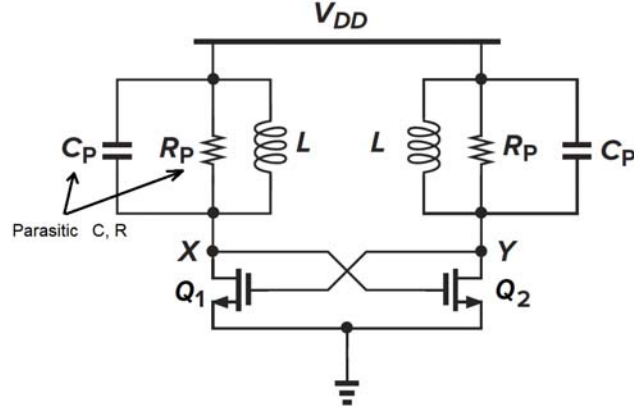
Fig. 2.1. Capacitor-less cross coupled LC-oscillator

C_p denotes the total parasitic capacitance seen at the output node and R_p the equivalent parasitic parallel resistance of the tank at the resonance frequency which is equivalent to $R_p = QL_1\omega$. To design this circuit at frequencies above 100 GHz, the loss mechanisms in the circuit need to be understood properly. As shown in Fig. 2.2, the oscillating signal within the oscillator positive feedback loop is affected by: (1) R_p ; (2) r_o of Q_1 and Q_2 ; (3) R_G of Q_1 and Q_2 ; and (4) the input resistance of the following stage, the buffer. If R_o represents all these losses at the node X, shown in figure Fig. 2.2, then $Re\{Y_{in}\}$ at resonance becomes (2.2):

$$Re\{Y_{in}\} = \frac{(1 + g_m R_0)R_0 C_{GD}^2 \omega^2}{1 + R_0^2 C_{GD}^2 \omega^2} \qquad (2.2)$$
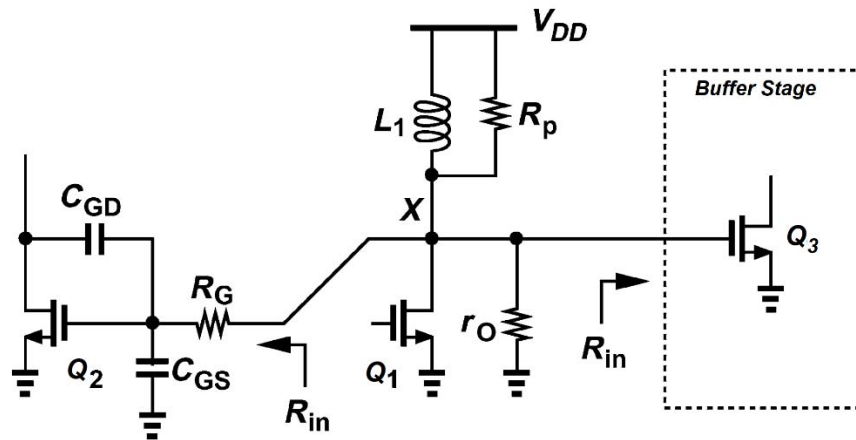
Fig. 2.2. Sources of loss in a cross-coupled oscillator

10

2.2 Feedback Buffer Oscillator (FBO)

The cross-coupled oscillator implanted in this work uses a buffer feedback configuration as shown in Fig. 2.3. In this configuration, the peaking inductors of the buffer couple some of their energy back to the oscillator tank inductors and consequently decrease the loss of the tank. This will result in an increase in the obtainable oscillation frequency.
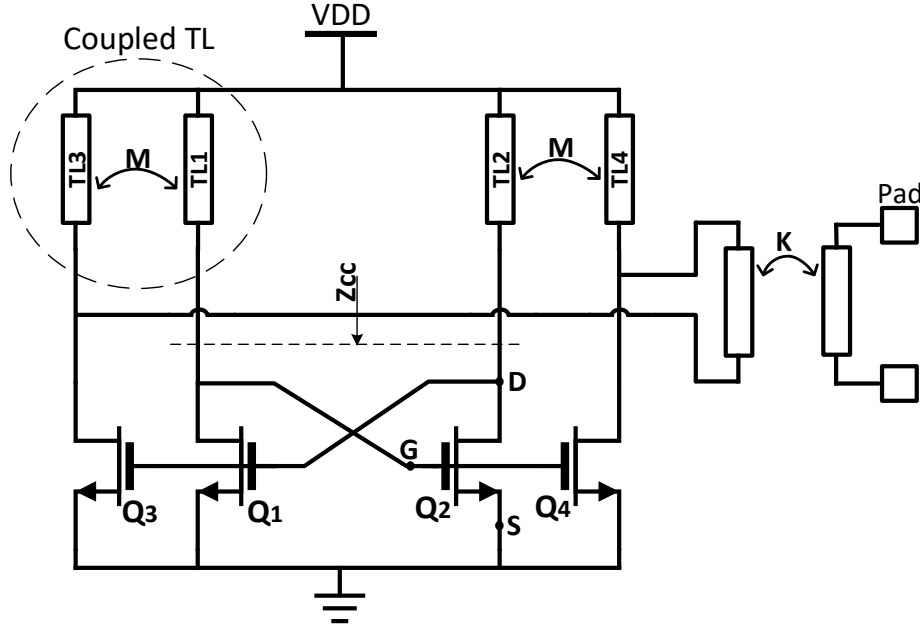
Fig. 2.3. Proposed buffer-feedback 140 GHz oscillator with transmission-line inductors

The tank inductors and buffer peaking inductors are implemented with 50 μm length and 4 μm thick transmission lines, each having 45 pH inductance and shown as $TL_{1,2,3\ \&\ 4}$ in Fig. 2.3. Transmission lines of cross-coupled and buffer, at each side of the differential pair, are routed adjacent to each other in the layout with 1.5 μm space between them. This results in mutual inductance (M) of 37 pH between the adjacent transmission lines. As shown in [65], this topology lowers the effect of tank parasitic capacitance by a factor of two. Total intrinsic and parasitic capacitance looking into the cross-coupled drains become (2.3):

$$C_{CC} \cong (1 + g_m R_G)\ C_{GS}/2 + C_{DB}/2 + 2\ C_{GD} \qquad\qquad (2.3)$$

where R_G is the base resistance of C_C transistors; g_m is transconductance of Q_1. The C_{GS}, C_{DB}, and C_{GD} are gate-source, drain-bulk, and gate-drain parasitic capacitances, respectively. Oscillation frequency can be calculated from $\omega_{osc}^2 = 1\ /\ [2\ (\ L_t + M\ )\ C_D]$, where C_D denotes the total parasitic

capacitance across the tank: $C_D \cong C_{CC} + C_{t/4}$, and C_t and L_t represent capacitance and inductance of each identical TL, obtained from T-section equivalent circuit. For circuit analysis, a T-section of lump components as shown in Fig. 2.4 used to model the TL. In this model, C_p, R, and L were obtained from ABCD parameters from EM simulation of the TL line as: $C_p = Im\{\ C^{-1}\ \}/\omega$, $R/2 = Re\{(A\text{-}1)\ C\}$, and $L/2 = Im\{(A\text{-}1)\ C\}/\omega$.
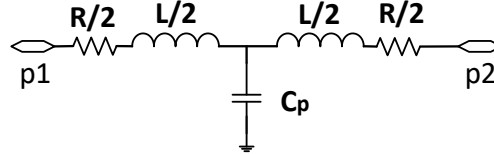
Fig. 2.4. A T-model for TL

Current density of 0.8 mA/μm is found to be an optimum value to maximize transistors transconductance at 140 GHz. To obtain oscillation, cross-coupled and buffer transistors, $Q_{1, 2, 3\ \&\ 4}$, are scaled with the same size and number of fingers to 8×0.8 μm. Therefore, each of the transistors in Fig. 2.5 has a total width of 6.4 μm.

An output transformer is designed for measurement of oscillator differential output. It uses two turns of metal-8 (*M8*) as the primary coil and one turn of metal-7 (*M7*) as the secondary coil. One port of secondary coil is connected to the output pad as shown in Fig. 2.5. Primary and secondary layout routes are staggered to reduce coupling capacitance between the two coils. The transformer shows an insertion loss of 3.6 dB at 140 GHz in simulation.

A D-band (110-170 GHz) OML harmonic mixer in conjunction with a Keysight Technologies spectrum analyzer is used in our measurement setup. The external harmonic mixer has an average loss of -60 dB across its 60 GHz band. In addition, we measured 3.4 dB of signal path loss for the combination of a Cascade waveguide Infinity probe, S-shape waveguide interconnect, and die pad using a pad-to-pad through-structure implemented on another test die. As shown in Fig. 2.6, the measured output tone has a power of -56.2 dBm at 141.824 GHz. Taking into account all the aforementioned path losses, this indicates a better than 7.2 dBm output power from the oscillator under test. The existence of the external harmonic mixer does not allow us to use the spectrum analyzer to directly measure the phase noise. However, setting the resolution and video bandwidth of the spectrum analyzer to 1 Hz, we measured better than -83 dBc/Hz signal

noise at 100 KHz offset as shown in Fig. 2.7. This noise is the combination of oscillator phase noise and that of the harmonic mixer. The oscillator core consumes 23.38 mW DC power from a 1.1 V supply. This translates to 22 % DC-to-RF efficiency.
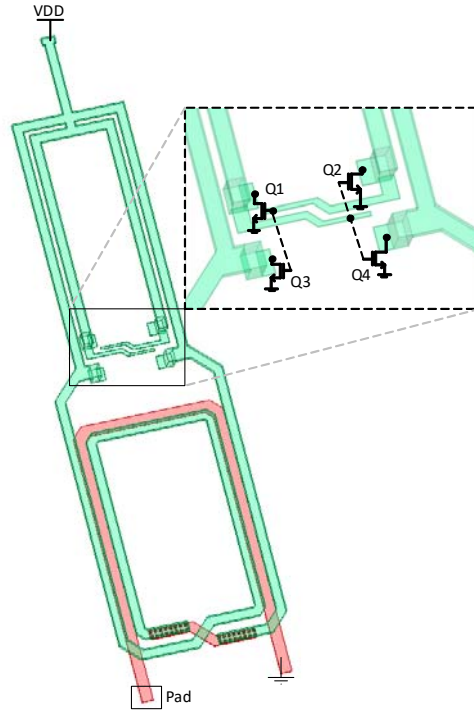
Fig. 2.5. Layout of 140 GHz oscillator passives and interconnects including the output transformer.
***AP* layer (TSMC65nm top metal layer) is not shown.**
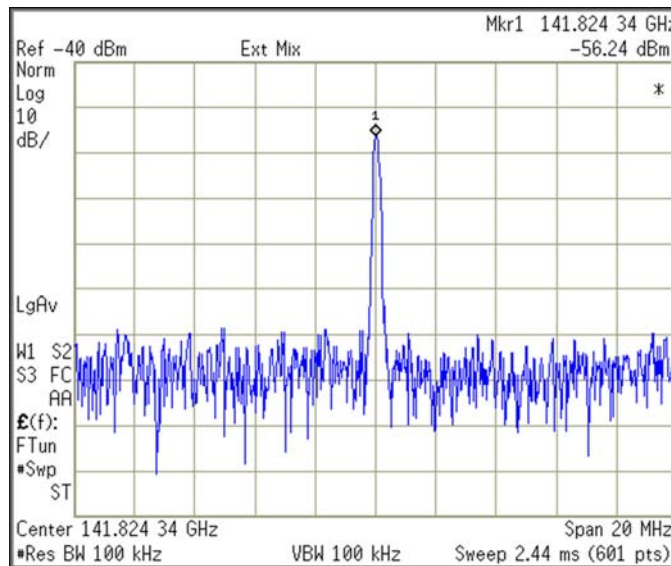
Fig. 2.6. Oscillator output tone. Peak power includes the harmonic mixer insertion loss and the path loss of measurement
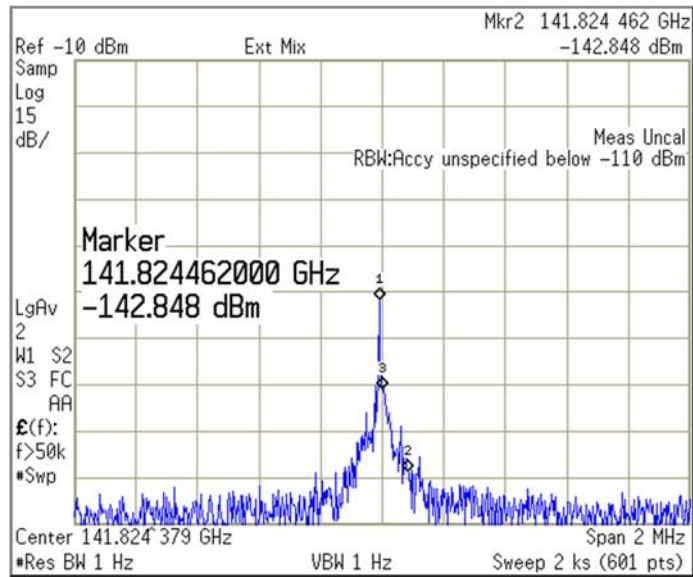
Fig. 2.7. Oscillator output noise at 100 KHz offset

The micrograph of the oscillator is shown in Fig. 2.8. However, as the entire chip is covered by the top metal *AP* layer, none of the underneath circuits are visible. The oscillator core occupies only $50\times50\mu m^2$ of the chip area.
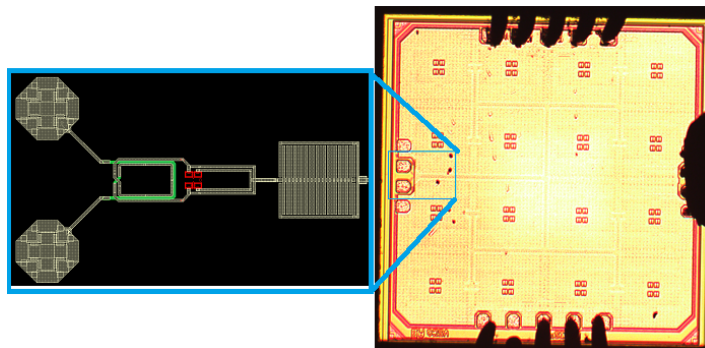
Fig. 2.8. Test chip of 140 GHz oscillator. Top metal layer (*AP*) is covering the underneath circuits

CHAPTER 3   Injection Locking Network

A fundamental coherency requirement of any antenna array dictates that each antenna element is driven with a signal source which is phase locked to those of the other elements. In a case where each antenna element is driven by a separate local oscillator, a coherence mechanism needs to be implemented to phase lock the independent local oscillators.

An oscillator phase can be controlled by injecting a signal from outside of the circuit into the feedback loop. This adds energy to the circuit at the injection frequency, making it easier for the circuit to sustain oscillation in-phase with the input signal. If the injected signal is strong enough, the oscillator will follow the injected signal phase instead of oscillating at in a free running mode. In this case, the oscillator is said to be "injection locked" in this condition. If many oscillators are injection locked by providing a reference signal paths to them, they will oscillate as a synchronized ensemble which is the scheme pursued in this work. In this chapter the injection locking transmission line network that carries the reference signal to the individual oscillators across the chip is explained. Planar on-chip transmission lines suffer from losses on the order of 1–3 dB/mm (or more) at THz. Furthermore, coupling to neighbouring structures can generate unwanted parasitic modes (e.g., parallel-plate modes and surface waves). The co-planar microstrip line implemented in this work has the smallest insertion loss reported to the best of our knowledge.

3.1   Reference Signal Distribution Network

A balanced H-tree clock distribution topology exhibits identical delay to the end nodes, due to its structural symmetry from the root of the distribution to all branches. If the termination impedance at the end nodes are matched to the characteristic impedance of the network, the reflection loss and clock skew can be zero. A passive balanced tree distribution network also exhibits a good tracking across Process-Voltage-Temperature (PVT) variations. T-junctions in the H-tree split the input signal into two branches, and must provide similar impedances at all ports in order to create the transmission line segments identical in the H-tree. This scheme also avoids incremental increase in the characteristic impedance of the transmission lines toward the root of

the distribution. In this work, an H-Tree composed of 100 Ω differential co-planar waveguide-grounded is designed and implemented as shown in Fig. 3.1. Design of the H-tree starts with designing a 50 Ω transmission line which is described in 3.2. Subsequently, the design of the differential 100 Ω CPWG is covered in 3.3. Modeling and simulation results of the proposed differential tapered T-junction are described in 3.4.
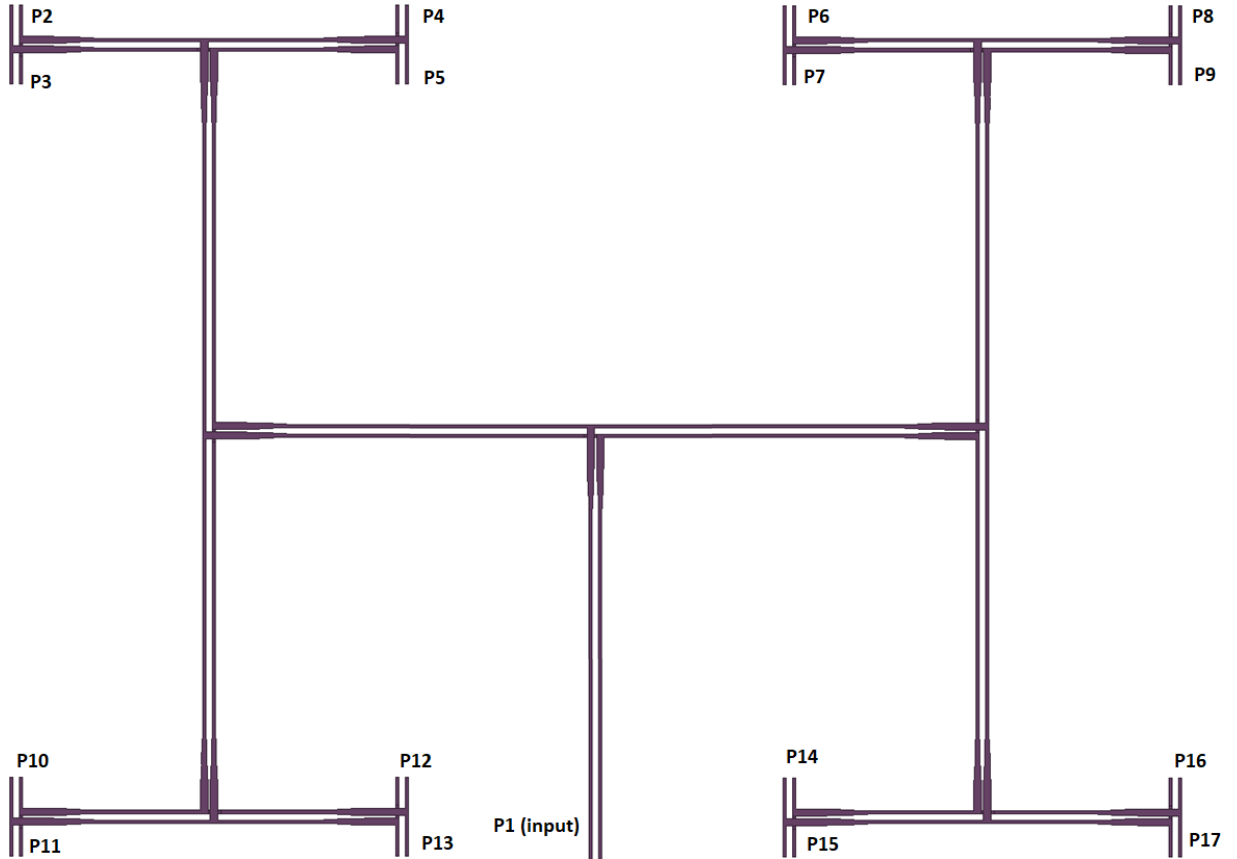
Fig. 3.1. H-tree differential clock distribution network

3.2 Microstrip Transmission Line (MTL)

TSMC65nm technology with 9 metal layer stack-up configuration is used in this project to design a MTL structure. The line is using 0.9 μm thick M8 for the signal and topmost 1.45 μm thick aluminum layer (*AP*) as the ground with 4.95 μm spacing between the two layers as shown in Fig. 3.2. All the stack up dielectric layers of TSMC65nm die are simplified and modeled with just two dielectric layers. The first layer from top is SiO2 with ε_r of 4.0 and loss-tangent = 0.002 and thickness of 11.025 μm which represent all the intermediate dielectric layers between metal

layers of TSMC65nm. The bottom layer is a 300 μm lossy bulk silicon with ε_r of 11.9 and conductivity of 7 S/cm. The proposed MTL design is rigorously analyzed by the full-wave HFSS electromagnetic simulator. Fig. 3.4 shows E-field plot of the line when propagating a 140 GHz signal. Propagation loss (α), and characteristic impedance (Z_0) are calculated for different widths (*W*) of the MTL as shown in Fig. 3.3. The propagation loss, α, has the same range of values as achieved in conventional implementations of MTL in the same technology [4] [5], which use 3.4 μm thick *M9* as signal line over *M1*, *M2* or *M3* ground layers. However, the proposed arrangement (Fig. 3.2) offers better isolation from the top of the die space.
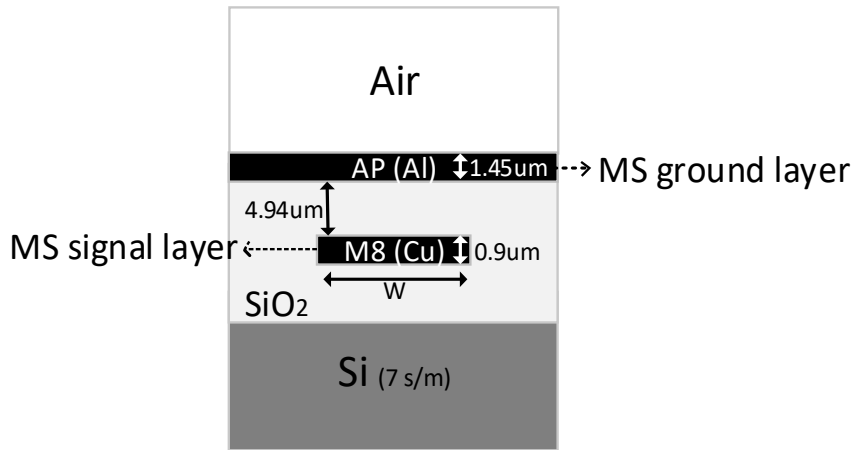
Fig. 3.2. Design of MTL in TSMC65nm. *AP* layer is used as MTL ground
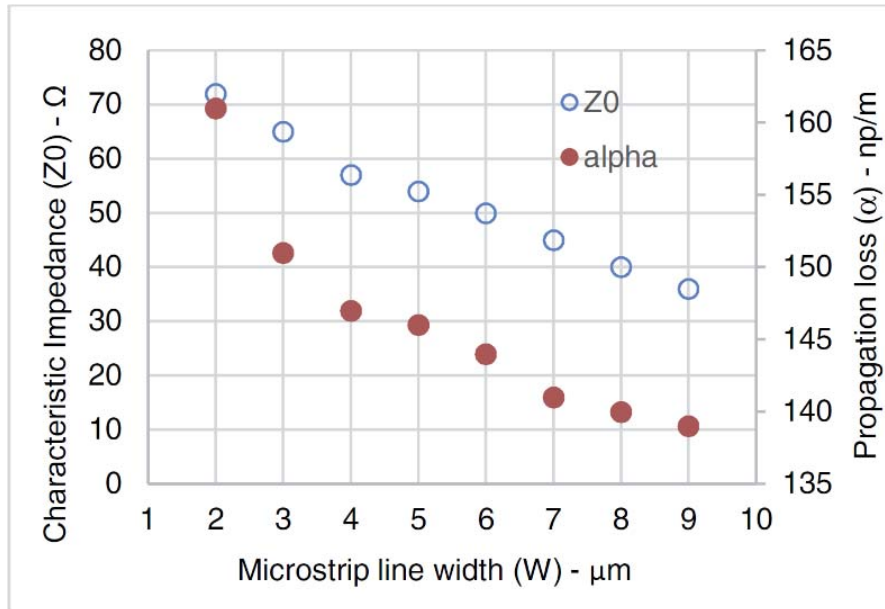
Fig. 3.3. Simulated *Zo* and α of the proposed MTL vs. line width at 140 GHz
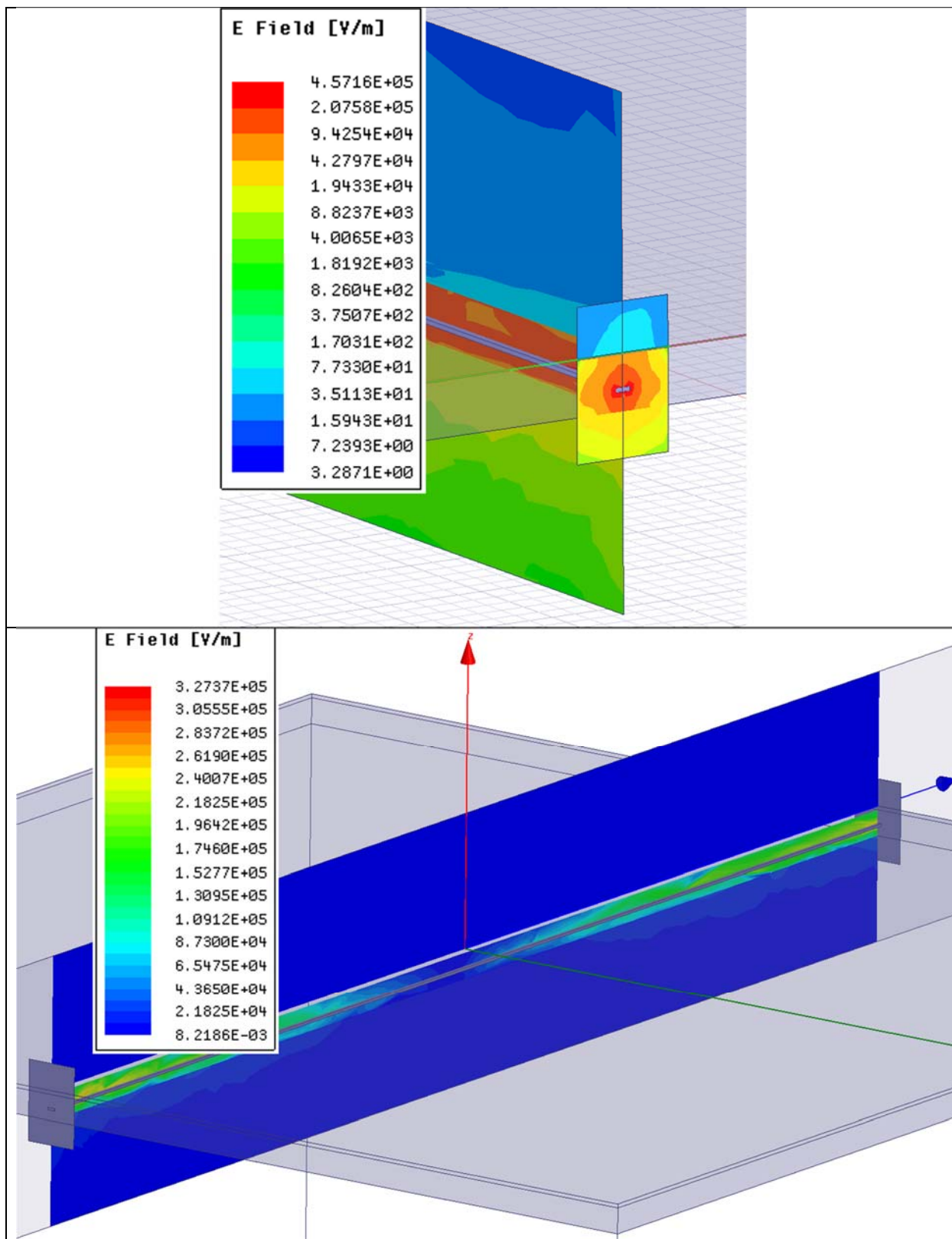
Fig. 3.4. Simulated field of MTL in TSMC65nm with 9 metal layers. *AP* is the ground layer.

3.3 Differential Co-Planar Waveguide Grounded (CPWG)

A differential CPWG is designed based on the basic MTL line described in the previous section. The CPWG uses *M8* layer for differential signal pair and *AP* for top ground. The space between the negative and positive lines of the differential pair is set to 6 µm. The gap between the signal line and the siding ground (*M8*) at both sides of the pair is 5 µm. *M8* and *AP* grounds are connected through *M9* layer and *M8* /*M9* VIAs, forming two ground shielding walls at both sides of the pair. Fig. 3.5 shows E field of the proposed CPWG when propagating a differential signal at 140 GHz. Fig. 3.6 shows the performance of this line.
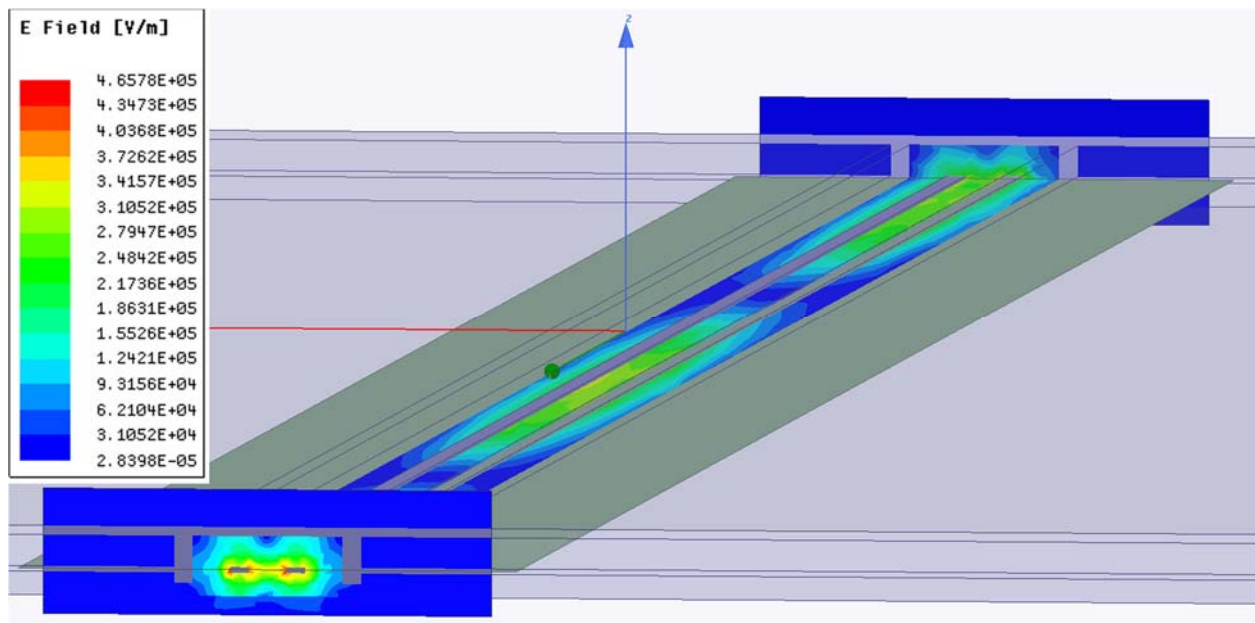
Fig. 3.5. Proposed differential CPWG. E-field of propagation of a 140 GHz differential signal

Name	X	Y
m1	141.0000	-22.6299
m2	141.0000	-1.7663

Curve Info
----- dB(St(Diff1,Diff1))
——— dB(St(Diff2,Diff1))
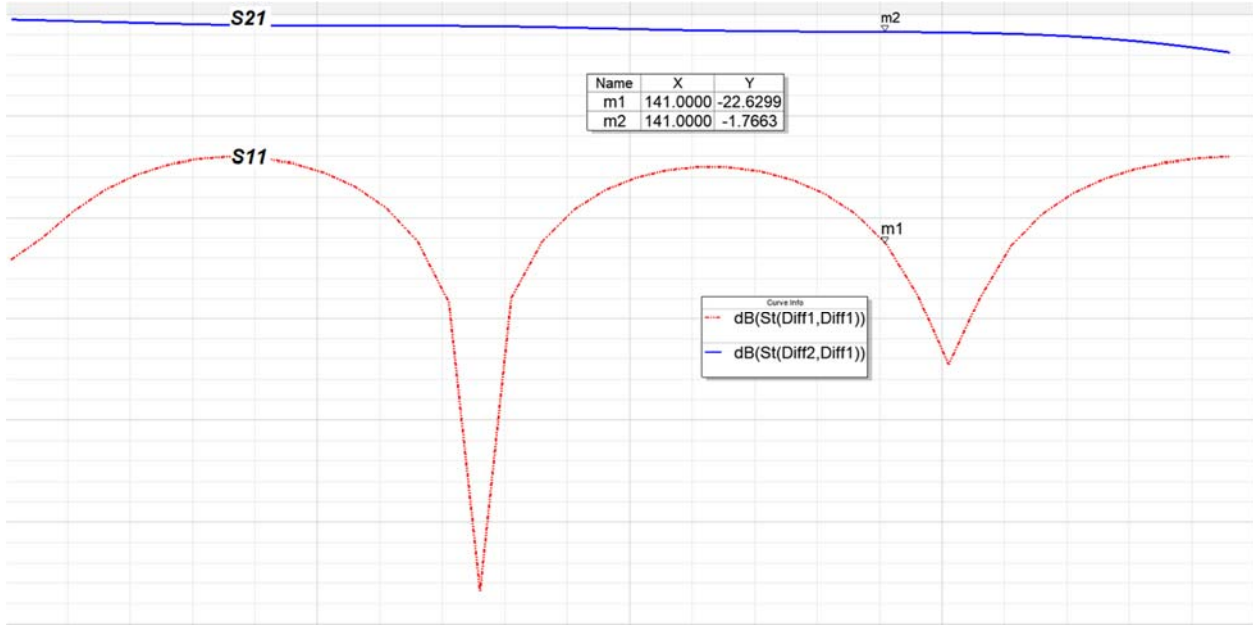
Fig. 3.6. Insertion loss (S21) and return loss (S11) of 1 mm of the differential CPWG

3.4 Tapered T-junction

The most critical component in the proposed differential H-tree clock distribution network is T-junction. The layout of the differential T-junction can not have a symmetrical design, since one of the signals must overlay the other, which will disturb the propagation mode. Changes in the propagating mode, cause phase offset between the positive and negative signals traveling in the differential pair after passing through a T-junction. The differential CPWG T-junction which is designed in this work have Z_0 of 50 Ω at each port. When the two 50 Ω lines merge at the intersection, the resulting impedance will be 25 Ω. There is a tapered transitional section that converts the Z_0 of 25 Ω back to 50 Ω. In order to cross pass two signal routes, one of the signals transits to the *M7* layer which is routed underneath another signal line, as shown in Fig. 3.7. An optimum number and arrangement of VIAs between *M7* and *M8* is found through EM simulations, which resulted in the least amount of field perturbation due to this transition. Simulation shows -1.1 dB insertion loss for this design as shown in Fig. 3.8. Reflection loss is shown in Fig. 3.9.
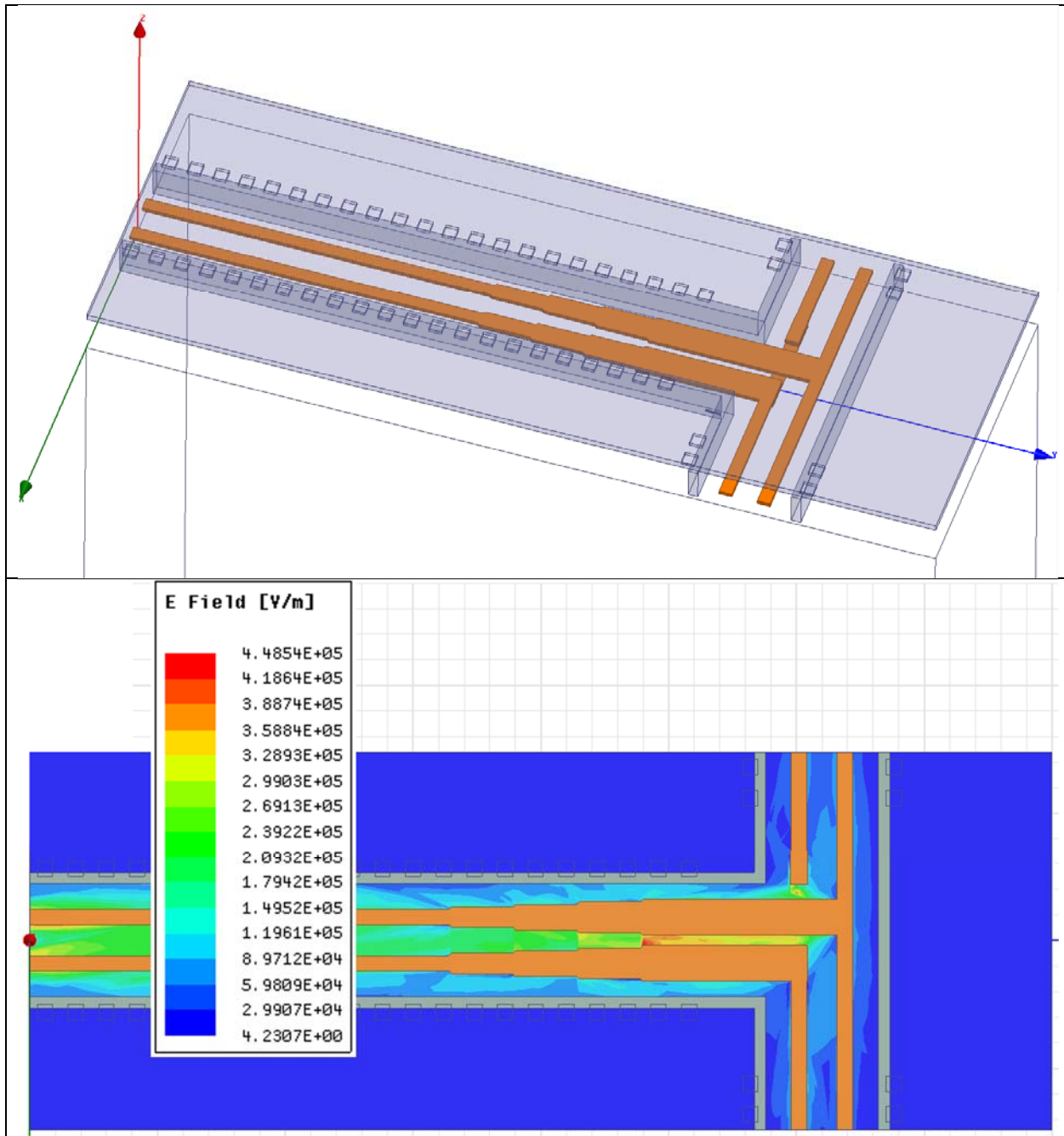
Fig. 3.7. T-junction implementation with differential CPWG
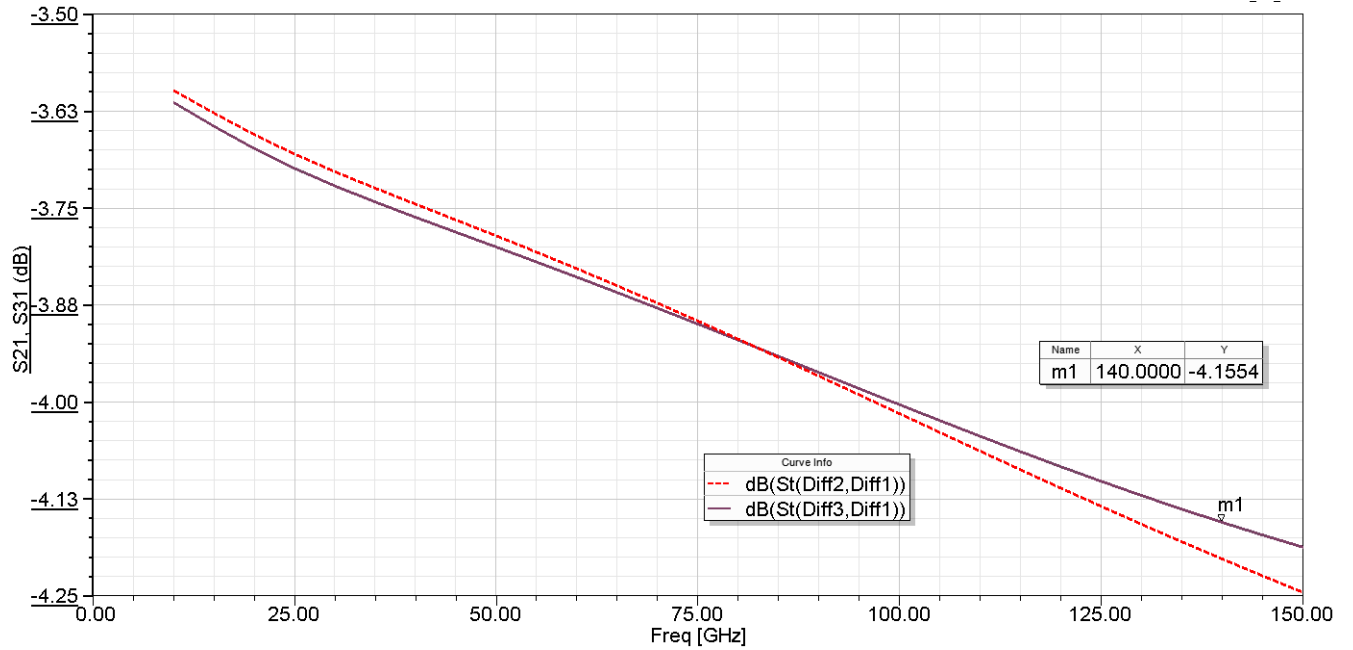
Fig. 3.8. Simulated S21 and S31 shows -1.15 dB insertion loss
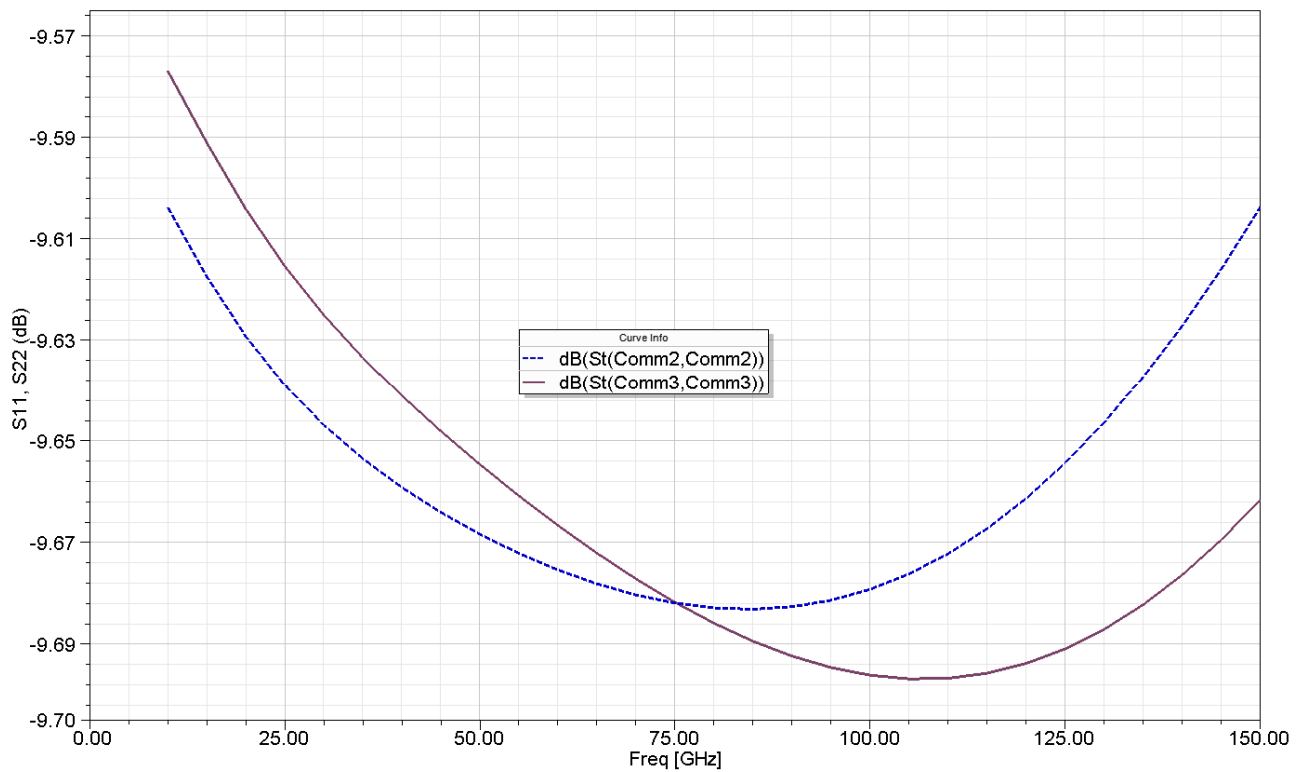
Fig. 3.9. Reflection coefficient (S11) of all ports which is better than -9.6 dB

3.5 H-Tree

An H-tree network forming a uniform 1-to-8 signal distribution grid, which is composed of differential CPWG and T-junctions, is modeled and simulated as shown in Fig. 3.10. As shown in Chapter 5, the layout of the branches are designed based on the 4×4 array structure. It is in accordance with that the distance between adjacent elements and therefore local oscillators in the final transmitter chip layout, therefore set to $\lambda_0/2$ = 360 µm. Clock skew of the network is calculated by comparing the phases of signals at end nodes and overlaying the phases of S21, S31, … S91, as shown in Fig. 3.11. Clock skew is simulated to be better than 2.5° across the network. All ports are impedance matched to 100 Ω differential load. Reflection loss of all ports are depicted in Fig. 3.12. Insertion loss at end nodes are better than 2 dB as shown in Fig. 3.13.
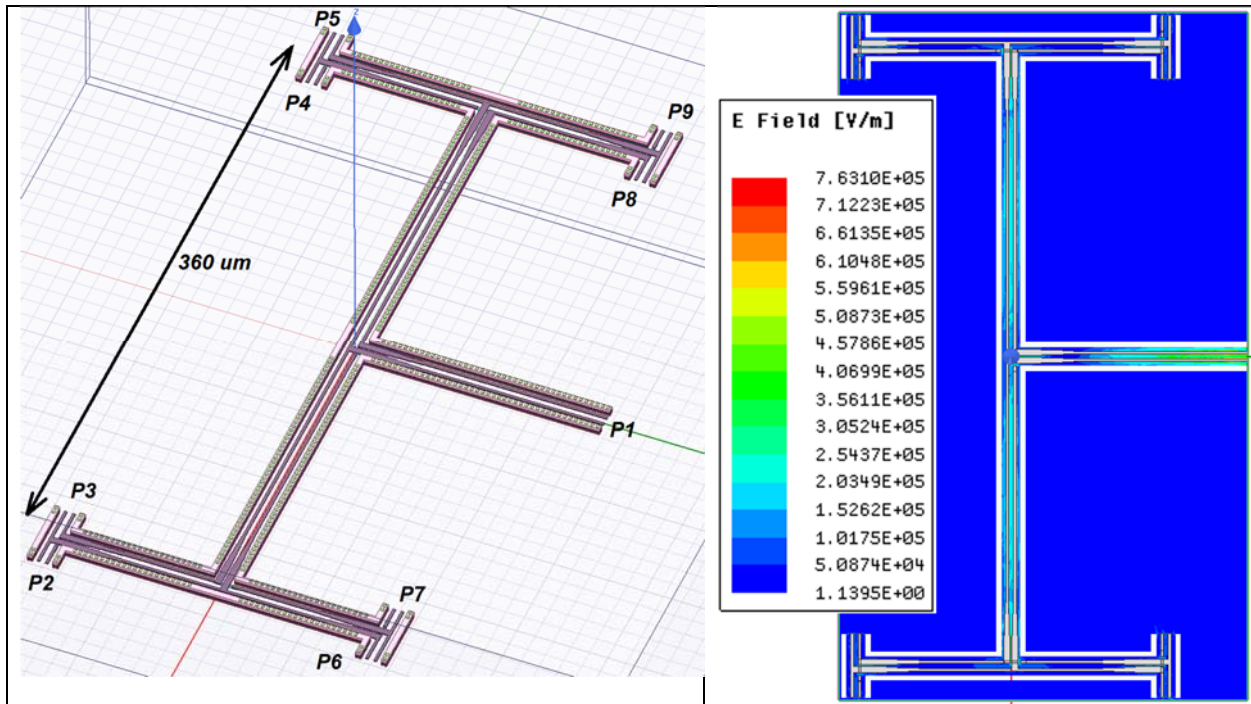
Fig. 3.10. 1-to-8 differential signal distribution network using CPWG
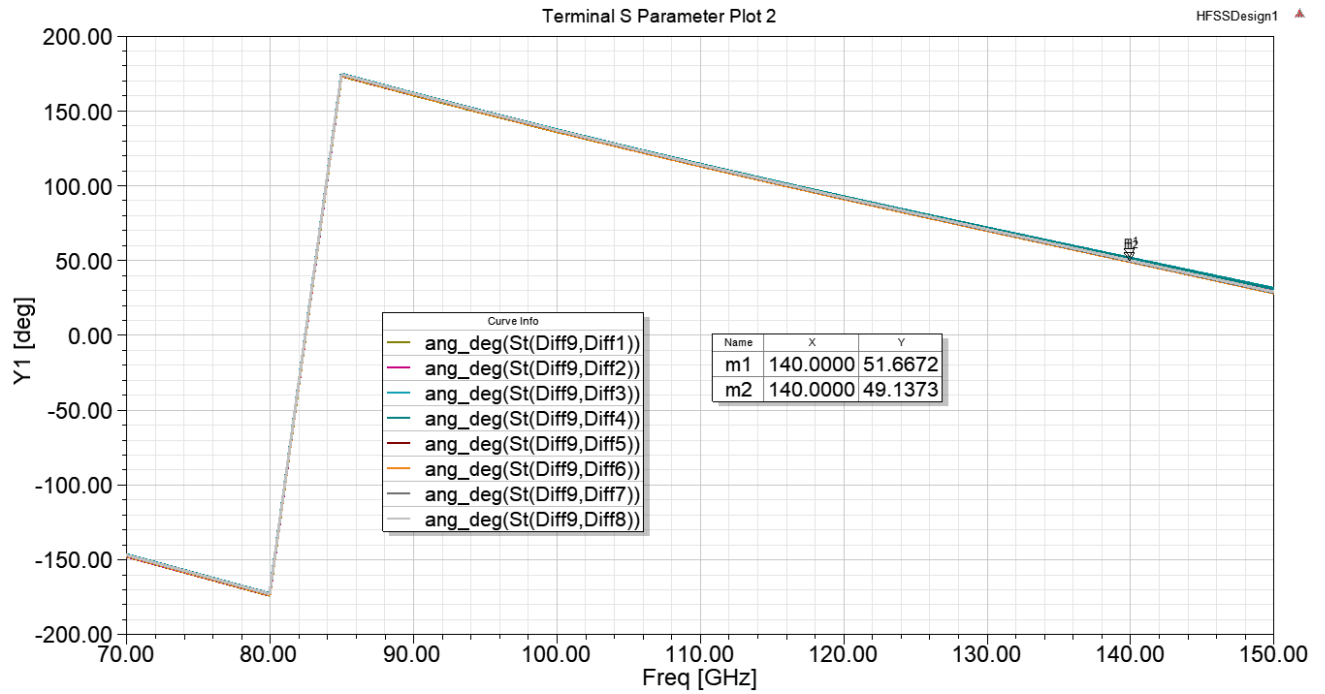
Fig. 3.11. Phase of S21, S31, … , S91
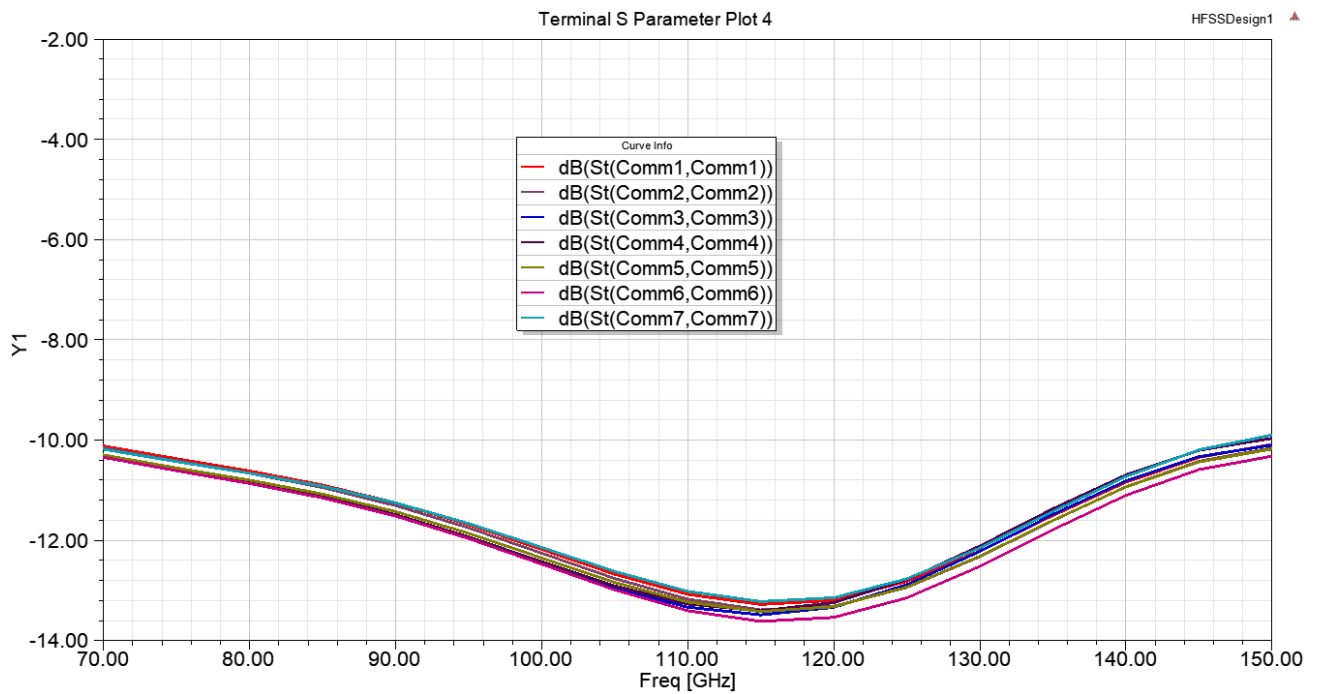
Fig. 3.12. Reflection coefficient at all ports

24
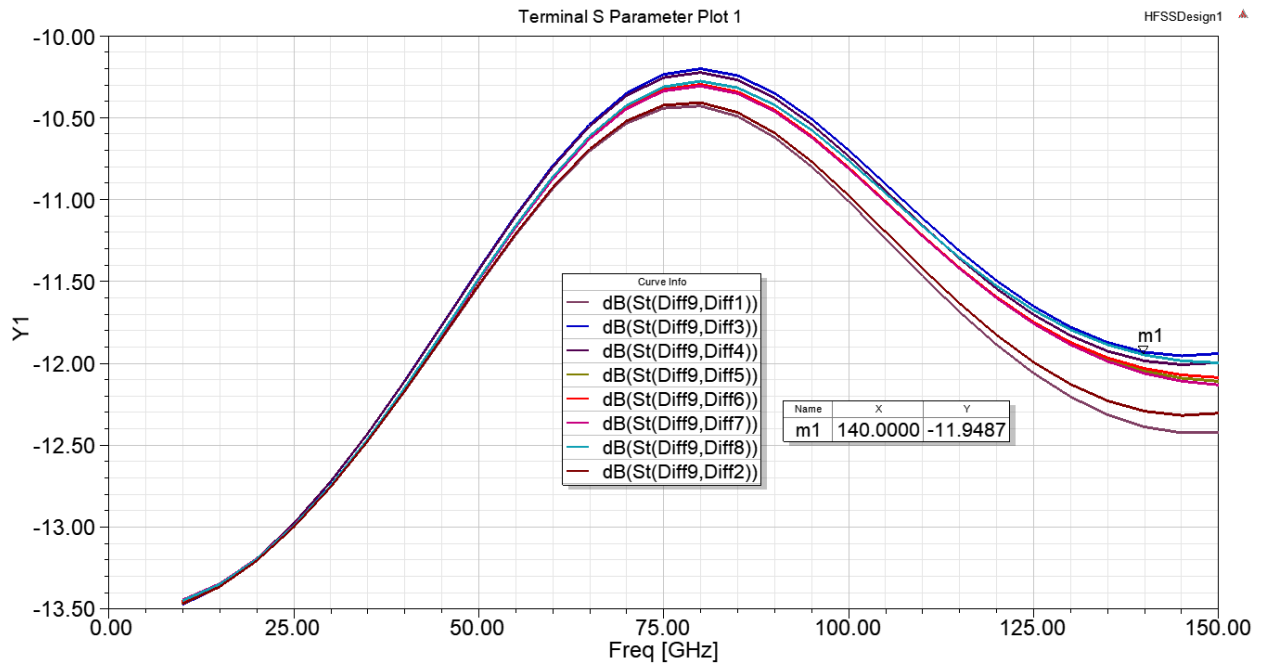
Fig. 3.13. Insertion loss for all the end port.

Plotting the phases of each individual signal when driven in differential mode, with 180 phase shift, is the best indicator for testing the performance of H-tree. Ideally, signals at each port must show the same 180° phase difference after propagating through the tree which indicates the differential symmetry mode has been preserved. This is shown in Fig. 3.14.
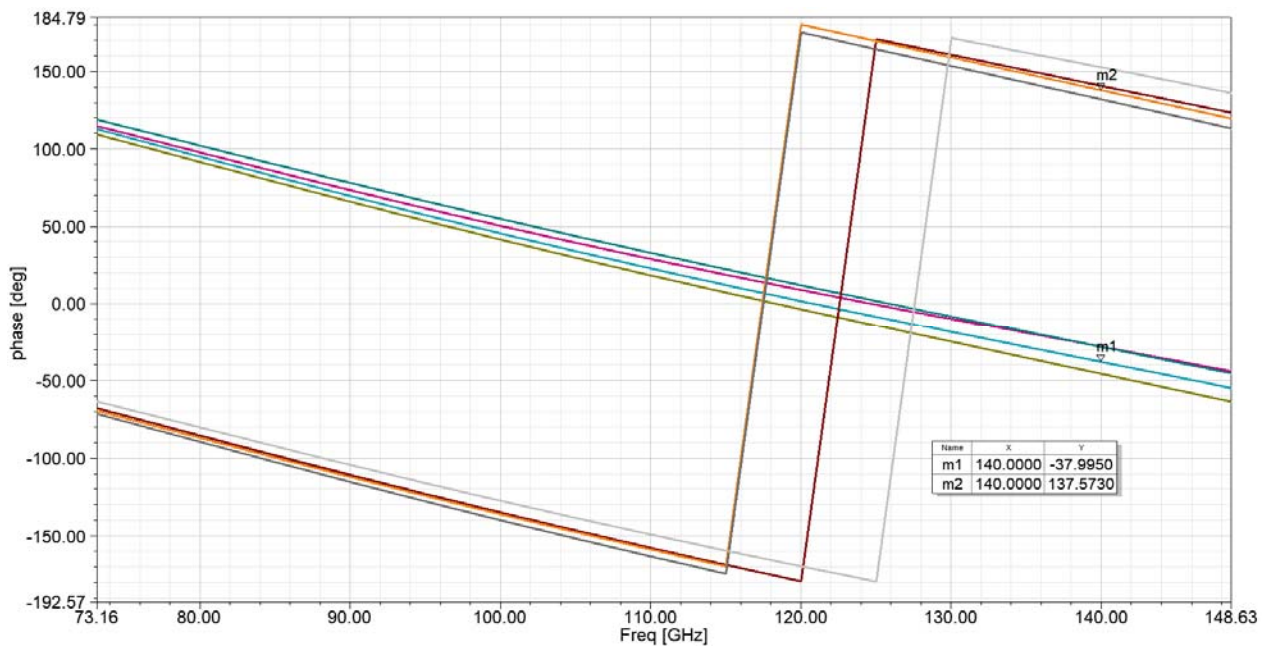
Fig. 3.14. Differential pairs show 174° phase difference at the end ports

CHAPTER 4   Dielectric Resonator Antenna Array

High conduction loss in metallic structures at sub-THz frequencies (100 GHz to 1 THz) severely limits their efficient usage over this range of frequencies. Besides, excessive size reduction and required higher precision, will considerably increase the cost and fabrication complexity of high gain, high performance metallic antennas such as open waveguide and horn antennas. An attractive alternative is antennas fully made of low loss dielectric materials. The Dielectric Resonator Antenna (DRA), introduced in early 1980's (see [66] for example). Various modes can be excited in dielectric resonator antennas, using proper type of excitation mechanism. During the 90's, emphasis was placed on applying analytical or numerical techniques for determining input impedance, fields inside the resonator and Q-factor [67] [68] [69] [70]. Current DRA literature focuses on compact designs to address portable wireless applications. Among them, new DRA shapes or hybrid antennas are developed for enhancing the antenna impedance bandwidth [71] [72] [73] or multiband antenna applications [74].

DRA has multiple electromagnetic modes at different frequencies. Different modes create radiating patterns with distinct profiles (number and position of lobs and nulls). In this work a broadside radiation pattern with a single main lobe is desired. A DRA that operates in its fundamental mode creates a broadside pattern.

DRA geometry must meet various requirements including: the resonant frequency, the impedance bandwidth, and the modal field distribution inside the resonator and its corresponding radiation pattern. Cylindrical shaped DRAs are used in this work as they offer great design flexibility. Both resonant frequency and Q-factor are dependent on the ratio of radius to height of the cylinder, noted as a/h in this research. As the first step towards designing a 420 GHz DRA antenna, analytical modal analysis of a cylindrical DRA will be performed to obtain initial optimal design parameters quickly and with reasonable accuracy. Then the design will be rigorously analyzed by a 3D EM simulator. Differential excitation and a novel loss-less power combining technique inside DRA is then scaled into a 4×4 array.

4.1 Theoretical Derivations and Modal Analysis of DR

For radiation pattern and resonant frequency calculation, a simple theory utilizing the magnetic wall boundary condition has been shown to correlate well with rigorous simulation and measurements. The geometry of the problem is shown in Fig. 4.1 using standard cylindrical coordinates. Consider a uniform DR, with the height value of (h) and radius (a), is placed on a perfect ground plane (PEC). The effect of the feed probe is temporarily ignored. Image theory is suitably applied, and the ground plane is replaced by an imaged portion of the cylinder extending to $z = -h$. The isolated cylinder is then analyzed with an implied boundary condition of $E_\rho = 0$ and $E_\phi = 0$ at $z = 0$. An approximate solution for the fields inside the cylindrical cavity is obtained by assuming that the surfaces are perfect magnetic conductors. This technique has been previously justified in [75]. It is shown in [66] that for such a cavity, wave functions TE_z and TH_z , can be written as:

$$\psi_{TE_{npm}} = J_n\left(\frac{X_{np}}{a}\rho\right)\begin{Bmatrix}\sin n\emptyset\\\cos n\emptyset\end{Bmatrix}\sin\left[\frac{(2m+1)\pi}{2h}\right] \tag{4.1}$$

$$\psi_{TM_{npm}} = J_n\left(\frac{X'_{np}}{a}\rho\right)\begin{Bmatrix}\sin n\emptyset\\\cos n\emptyset\end{Bmatrix}\cos\left[\frac{(2m+1)\pi z}{2h}\right] \tag{4.2}$$

where the mode indices n, p and m identify field variations in φ (azimuth), r (radial) and z (axial) directions, respectively. J_n is the Bessel function of the first kind, and X_{np} and X'_{np} are the roots of the Bessel's functions and their derivatives:

$$J_n(X_{np}) = 0, \ J'_n(X'_{np}) = 0, \ \text{for } n = 1, 2, 3, \cdots, p = 1, 2, 3, \cdots, m = 0, 1, 2, 3, \cdots$$

The separation equation $K_z{}^2 + K_\rho{}^2 = K^2 = \omega^2\mu\varepsilon$, leads to the expression that is used for calculating the resonant frequency of the npm mode as follows:

$$f_{npm} = \frac{1}{2\pi a\sqrt{\mu\varepsilon}}\sqrt{\begin{Bmatrix}X_{np}^2\\X_{np}'^2\end{Bmatrix} + \left[\frac{\pi a}{2h}(2m+1)\right]^2} \tag{4.3}$$

For the mode with smallest resonant frequency (dominant mode, TM$_{110}$) $n = 1$, $p = 1$, $m = 0$, and $X'_{11} = 1.841$. For lowest order mode resonant frequency of 0.42 THz for HRS with $\varepsilon_r = 11.9$, the initial values of h and a can be obtained from (4.3).

27
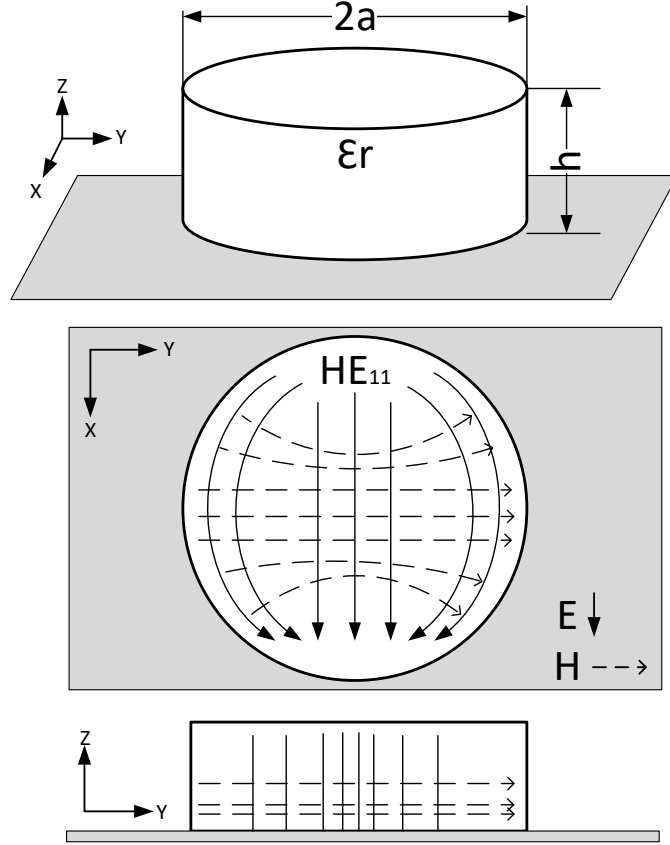
Fig. 4.1. DR Model for modal analysis

The wave function of the dominant mode is:

$$\psi_{TM_{110}} = J_1\left(\frac{X_{11}'}{a}\rho\right)\cos\emptyset\,\cos\left(\frac{2\pi}{2h}\right) \tag{4.4}$$

Far field radiation pattern associated with this mode is calculated by finding the equivalent surface currents. Surface currents are calculated from, $\vec{M} = \vec{E} \times \hat{n}$, using tangential electric fields which are obtained from:

$$E_\emptyset = \frac{1}{j\omega\varepsilon\rho}\frac{\partial^2\psi}{\partial\emptyset\partial z}, E_z = \frac{1}{j\omega\varepsilon}\left(\frac{\partial^2}{\partial z^2}+k^2\right)\psi, E_\rho = \frac{1}{j\omega\varepsilon}\frac{\partial^2\psi}{\partial\rho\partial z} \tag{4.5}$$

4.2   DRA Slot Excitation

Due to the planned integration of DRA with an active source, the DRA is exited through the rectangular slot. Slot coupling is also referred to as aperture coupling in literature. By keeping the slot dimensions electrically small, the amount of radiation spilling beneath the ground plane can be minimized. Aperture coupling offers the advantage of having the feed network located below

the ground plane, isolating the radiating aperture from any unwanted coupling or spurious radiation from the feed line. The slot can be considered as an equivalent magnetic current (M_s) whose direction is parallel to the slot length. When exciting the DRA with a magnetic current source, the source (slot) should be located close to an area of strong magnetic fields inside DRA in order to achieve strong coupling (χ), as shown in Fig. 4.2. Based on reciprocity theorem, coupling strength is calculated by the equation: $\chi \propto \int_v (H_{DRA} . M_s)dV$
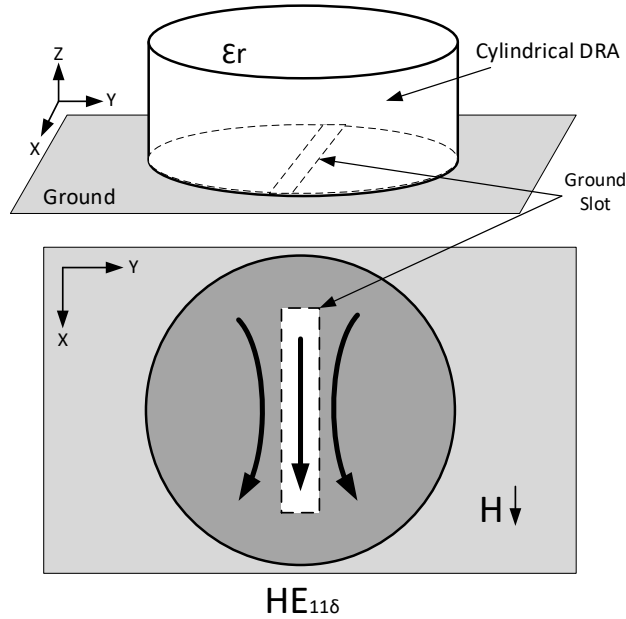
Fig. 4.2. Slot coupling to the magnetic field inside DRA

In [76] the method of moments has been applied to a DRA above PEC when excited through a magnetic source and provided an empirical formula to calculate resonance frequency of a cylindrical DRA in HEM$_{11\delta}$ mode:
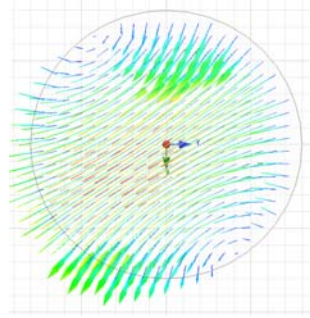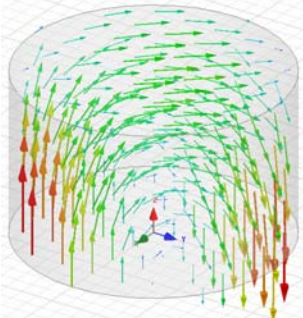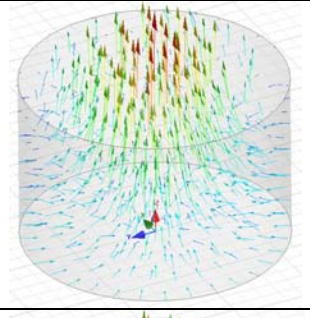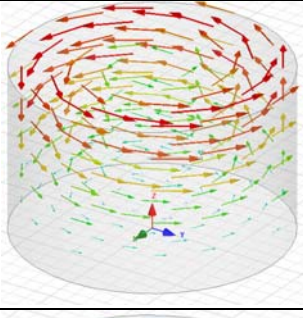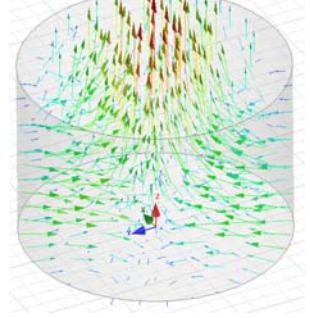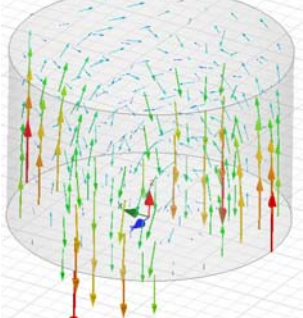
$$f_r = \frac{c}{2\pi a\sqrt{\varepsilon_r}}\left[1.71 + \frac{a}{h} + 0.1578\left(\frac{a}{h}\right)^2\right] \tag{4.6}$$

HEM$_{11\delta}$ is more accurate expression of the fundamental as compared to TM$_{110}$ in the previous Section. It uses an accurate set of boundary conditions between dielectric and air, instead of simple PMC surfaces. The formula (4.6) is useful for quick calculation of DRA resonant frequencies.

4.3 DR Modal Field Simulation

HFSS simulation is performed to verify the resonance frequencies of a cylindrical DR obtained from analytical method in Section 4.1. A cylindrical DR with a height of 100 μm and radius of 75 μm was modeled. PMC boundary condition was applied to the top and side surface of the cylinder. A PEC was assumed as the bottom surface of the DR. HFSS solver was set to find eigenmode solutions for the first 5 resonance modes. Table 4.1 shows the electric and magnetic fields of these first 5 resonance modes along with their resonance frequency. Since these not-radiating modes are similar to radiating modes, the DR dimensions obtained from this simulation are used to model the preliminary DRA structure in radiating mode.

Table 4.1. Electric and Magnetic fields for first radiating modes of cylindrical DR

Mode	F (GHz)	H Field Vector Plot	E Field Vector Plot
1 & 2 TM_{11}	406.8		
2 TE_{11}	499.2		
3 & 4 HE_{21}	610.9		

4.4 DRA on PEC Plane with an Ideal Magnetic Slot Excitation

A HRS DRA with height of 100 μm, and radius of 80 μm is put on a PEC. The PEC contains an aperture slot as shown in Fig. 4.3. A voltage source across the slot is exciting the DRA. This structure is placed on top of a two-layer cubical structure with the size of 300×300μm. This cube represents an active die in TSMC65nm technology. The first top layer of the cube which is underneath the PEC, is a 12 μm SiO2. This layer is representing all the interconnecting layers in the TSMC65nm technology with 9 metal layers and modeled as a loss-less material. The bottom layer is a 300 μm thick conductive silicon with σ = 7 S/m³ representing the bulk silicon of the die. The whole structure is enclosed inside a box with radiation boundaries.

(a)   (b)
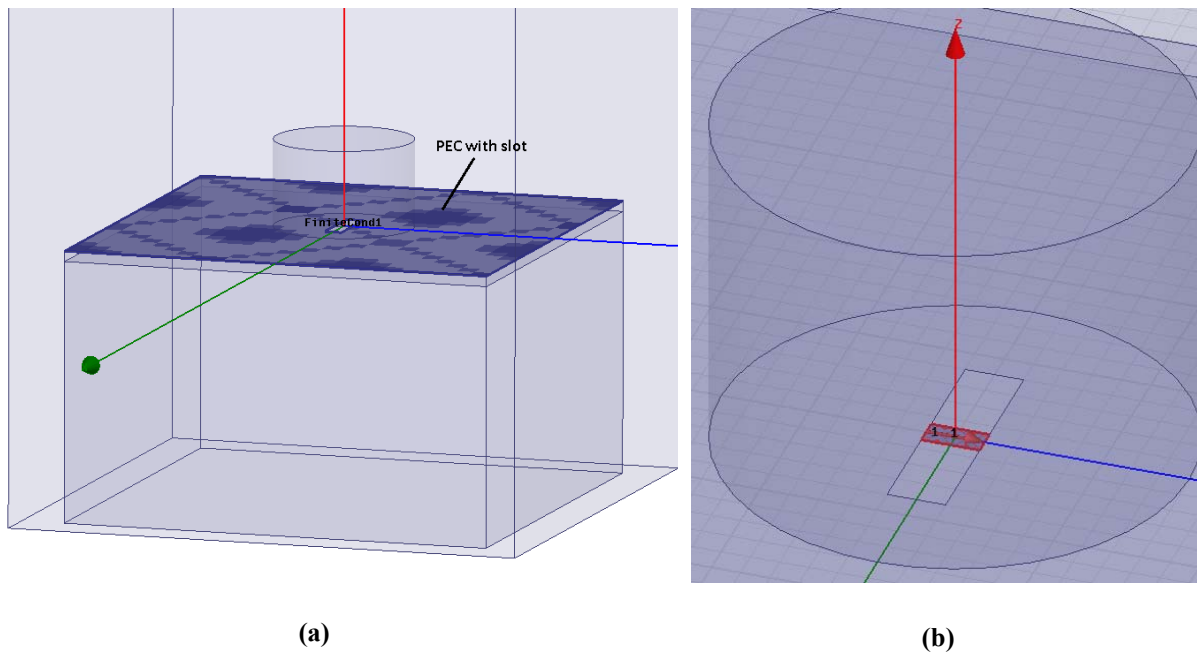
Fig. 4.3. (a) A cylindrical DRA is excited through a slot on PEC. DRA and PEC are placed on a TSMC65nm die model. (b) The ground slot on the PEC is excited with a lump port across the slot.

Since the perfect magnetic boundry conditions around the DRA is removed in comparism with eigenmode solutions model, height (H_d) and diameter (R_d) of the DRA are optimized around the values estimated in Section 4.3 to achieve maximum radiation efficiency at 420 GHz. Sweep of H_d and R_d of DRA versus radiation efficiency and maximum gain is shown in Fig. 4.4. H_d of 100 μm and R_d of 80 μm found to give maximum radiation efficiency of 0.94 and total maximum gain of 6.2 dB at broadside. Fig. 4.5, shows E-field and total gain pattern at these optimized

dimensions. Illustrated electric field distribution in the DRA at resonance frequency in Fig. 4.5(a), confirms the excitation of HEM$_{11\delta}$ radiating mode.
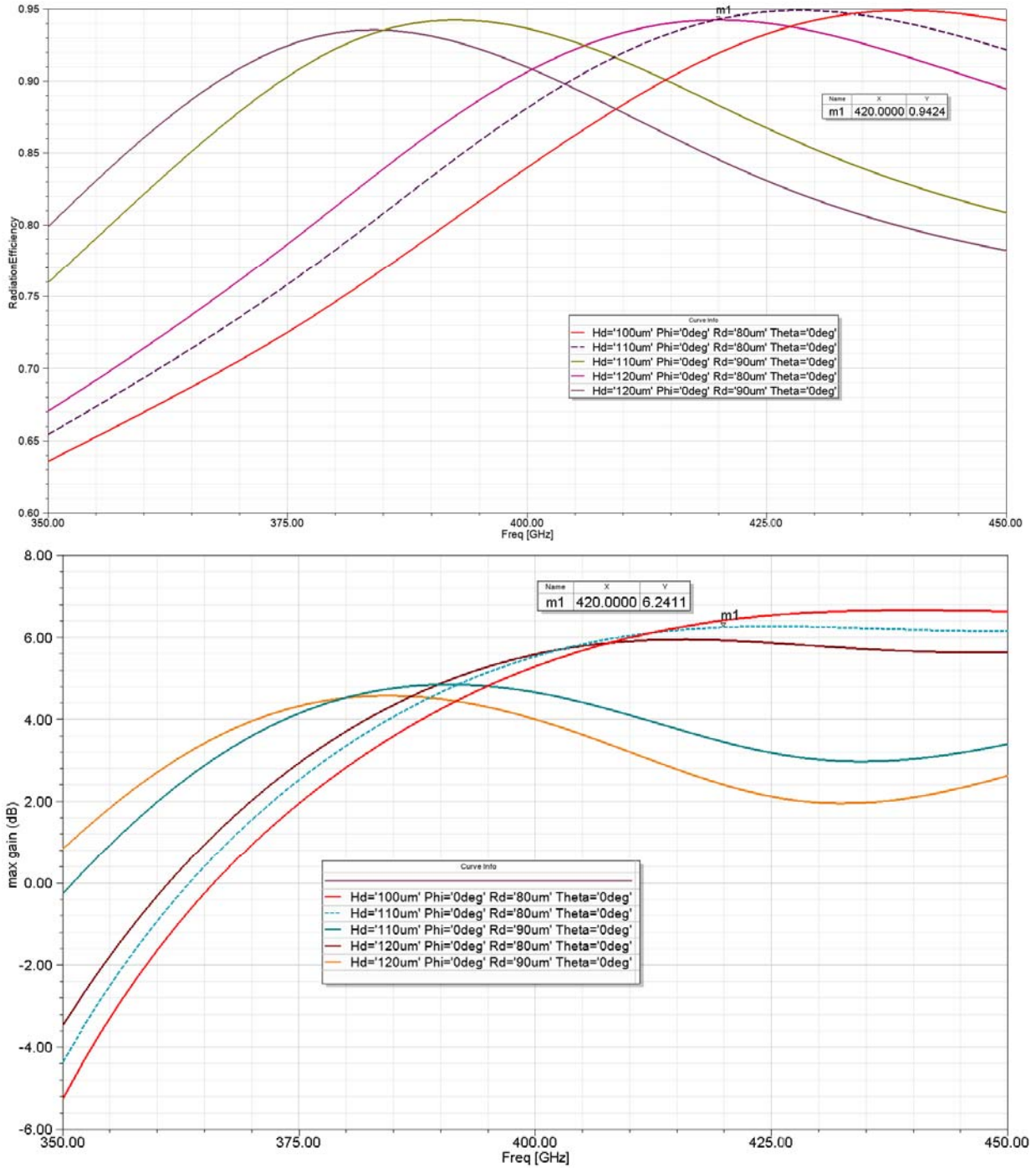
Fig. 4.4. Sweep of H_d and R_d of DRA. H_d at 100 μm and R_d at 80 μm gives maximum radiation efficiency of 0.94 and total maximum gain of 6.2 dB at broadside.
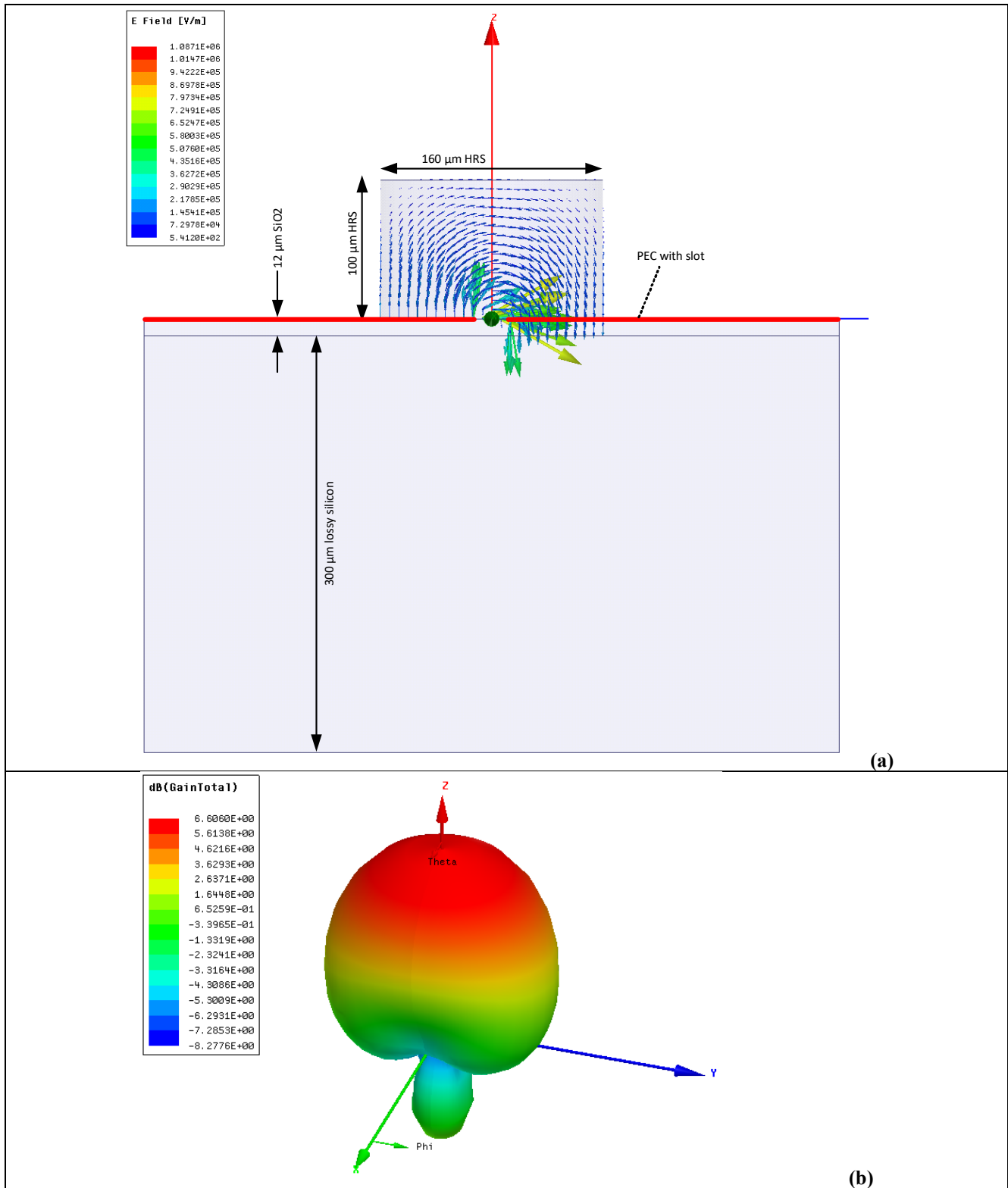
Fig. 4.5. (a) The Electric field inside the DRA at optimum dimention, (b) Total gain and radiation pattern

4.5 DRA with an Attached 30 μm Silicon Slab

A major challenge in the integration of a DRA with an active die is placing the DRA with acceptable precision on top of the die. Additionally, in an array structure, DRAs need to be placed at a designed coordinate from each other. In order to address these two fundamental requirements, a carrier layer to arrange and fix the DRAs in specific positions is proposed and developed. This carrier layer also makes the mechanical handling of the array structure feasible. In order to study the effect of this carrier layer on the performance of the DRA, the cylindrical DRA simulation model in Section 4.4 is modified. A 30 μm thick HRS slab with the identical material as DRA is attached to the DRA bottom. The two objects, DRA and the HRS slab, are then merged. This unified structure is put on a PEC covering the top surface of an active die model. The PEC embeds an excitation slot. The active die is modeled with the same layer stack up as the previous simulation. The H_d and R_d of the DR is optimized around their initial values to achieve maximum radiation efficiency and maximum gain at 420 GHz. Fig. 4.6 shows these sweeps. DR with H_d at 100 μm and R_d at 75 μm gives the maximum radiation efficiency of 0.93 and max gain of 5.3 dB at 420 GHz. The radiation efficiency of this structure compared to the stand alone DRA of Section 4.4, only decrease by 0.1. This indicates the carrier is not affecting the performance of the DRA. A closer look at the field inside the structure, as shown in Fig. 4.7 (a)(b) also indicates that the DRA field spill into the carrier slab is quite small. Fig. 4.7(c) shows directivity is reduced by 1.4 dB in compare to the model in Section 4.4.
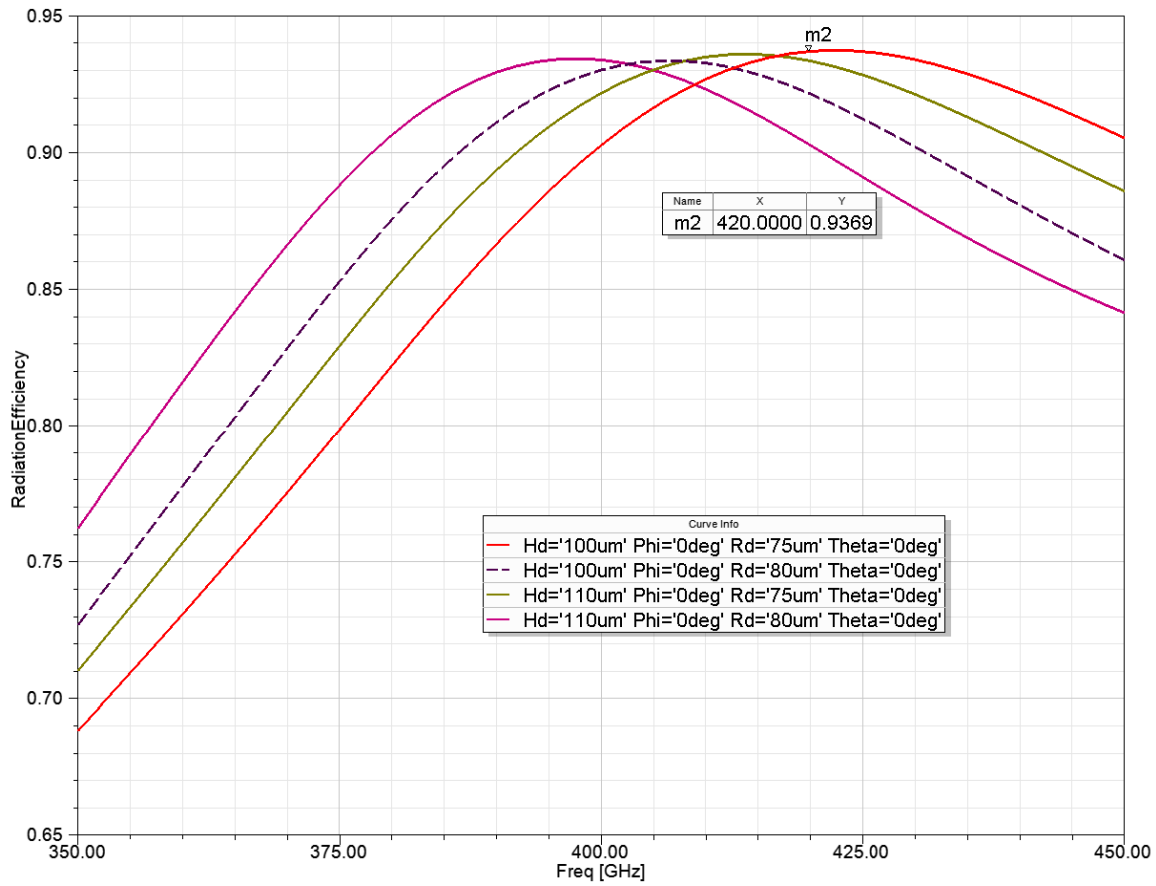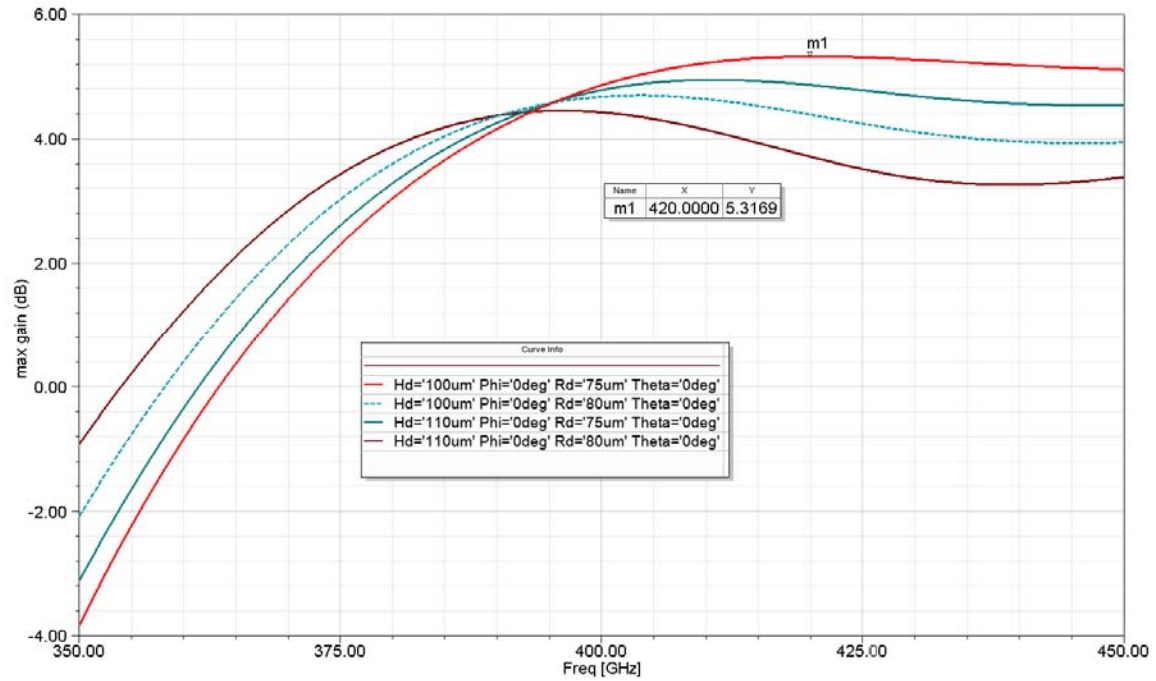
Fig. 4.6. Sweeps of H_d and radius R_d of DRA. H_d = 100 µm and R_d = 80 µm gives maximum radiation efficiency of 0.94 and total maximum gain of 5.2 dB at broadside

(a)

(b)

(c)
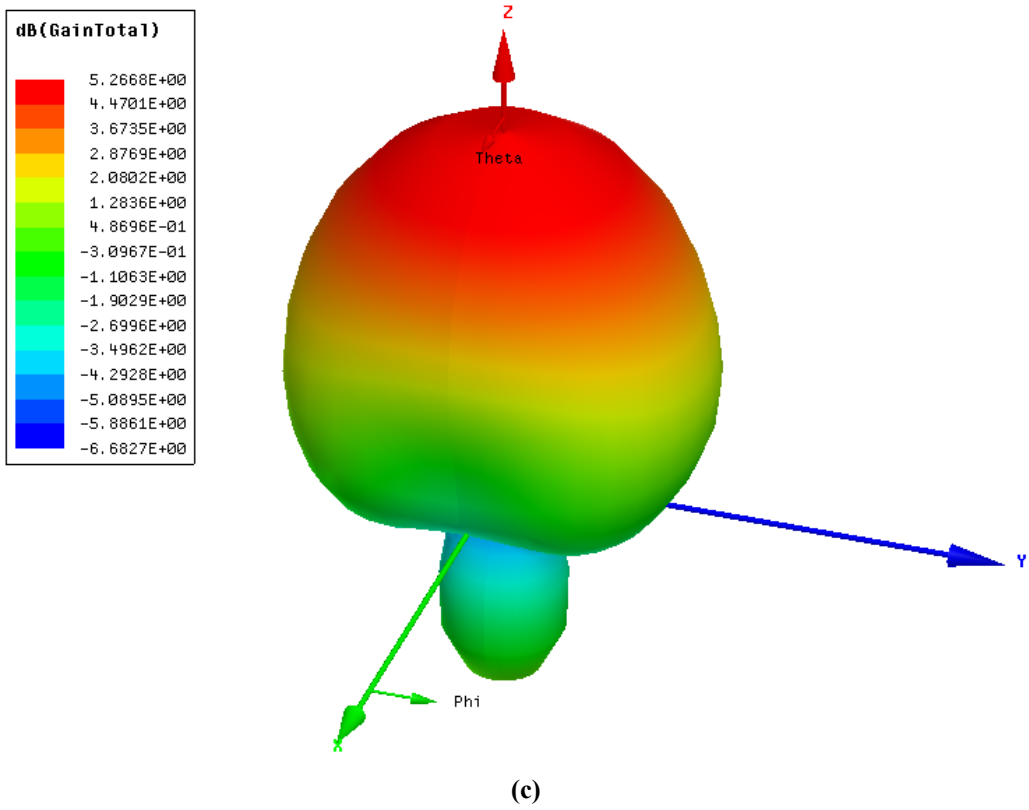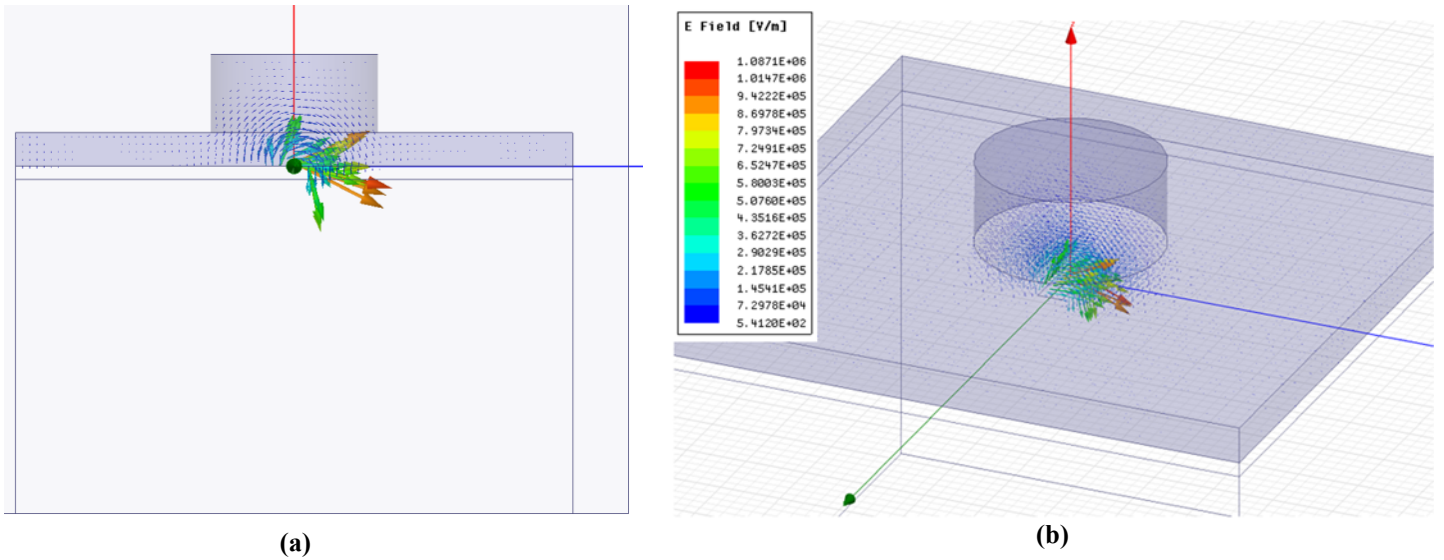
Fig. 4.7. (a)(b) Electric field inside the DRA structure with an attached HRS carrier layer, (c) Total gain and radiation pattern

4.6 DRA with Differential Excitation

In this simulation, the DRA structure of Section 4.6 with an attached 30 μm silicon slab is excited through two differentially driven slots. Fig. 4.8 shows this configuration. The two ports are driven with 180° phase shift and excited the same $HEM_{11\delta}$ mode inside DRA. Each slot dimension, slot width (W_S), slot length (L_S) and their separation (D_S) are optimized to obtain maximum coupling and radiation efficiency. Fig. 4.9 shows how the two differential ports contribute to excite the same $HEM_{11\delta}$ mode inside DR. Simulation shows radiation efficiency of 0.94 as shown in Fig. 4.10. This indicates the efficiency does not deteriorate in compared to the setup in Section 4.5 with single port excitation.

(a)

(b)
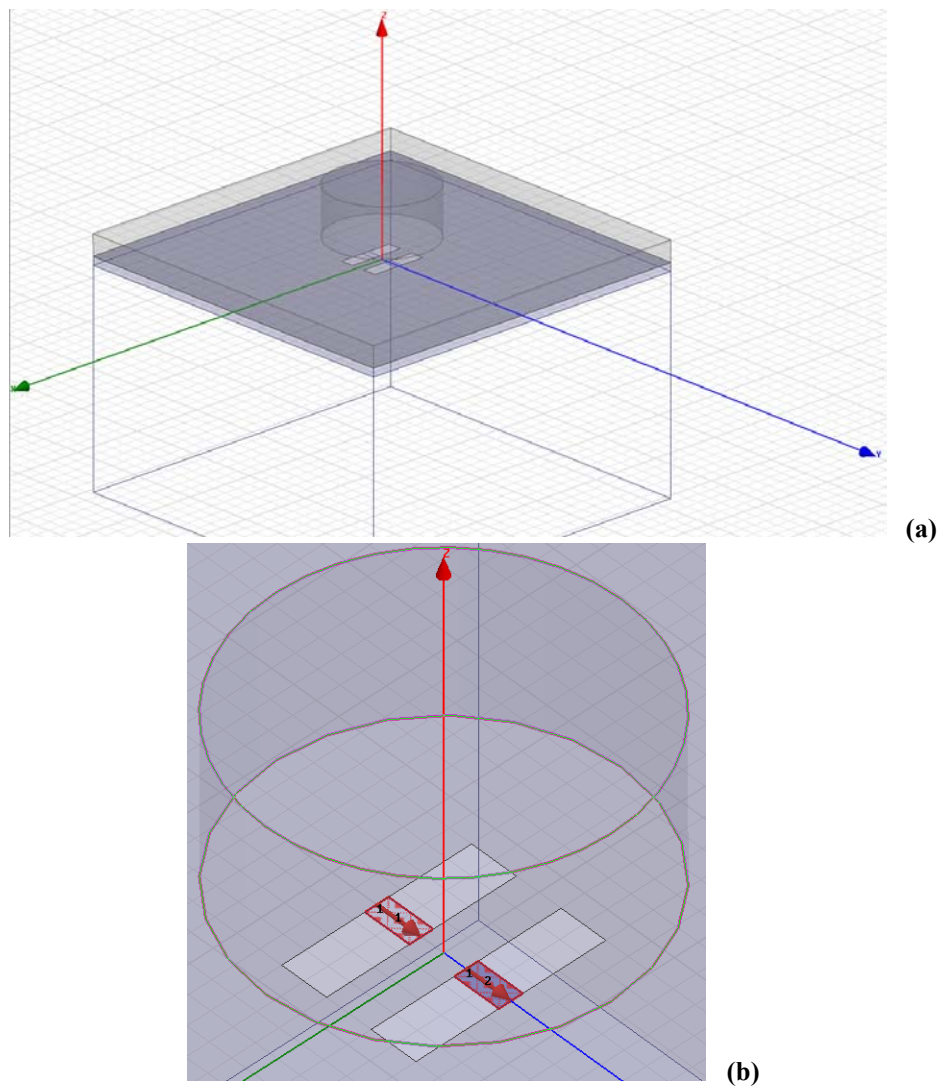
Fig. 4.8. (a) DRA with silicon slab excited through two ground slots, (b) Ports 1 and 2 are driven differentially with 180° phase shift
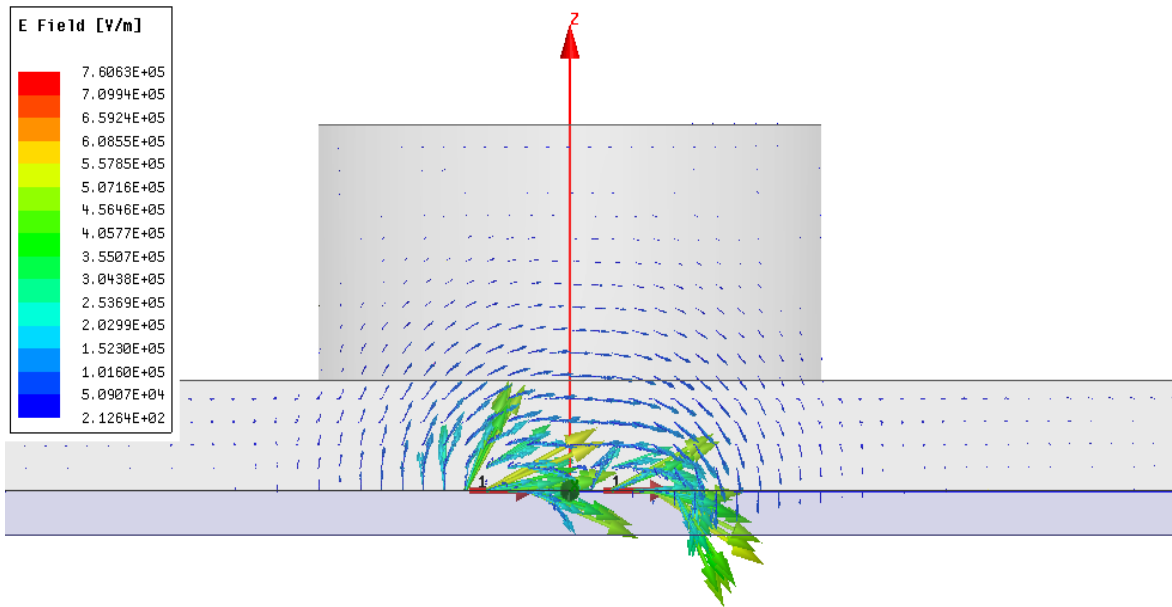
(a)
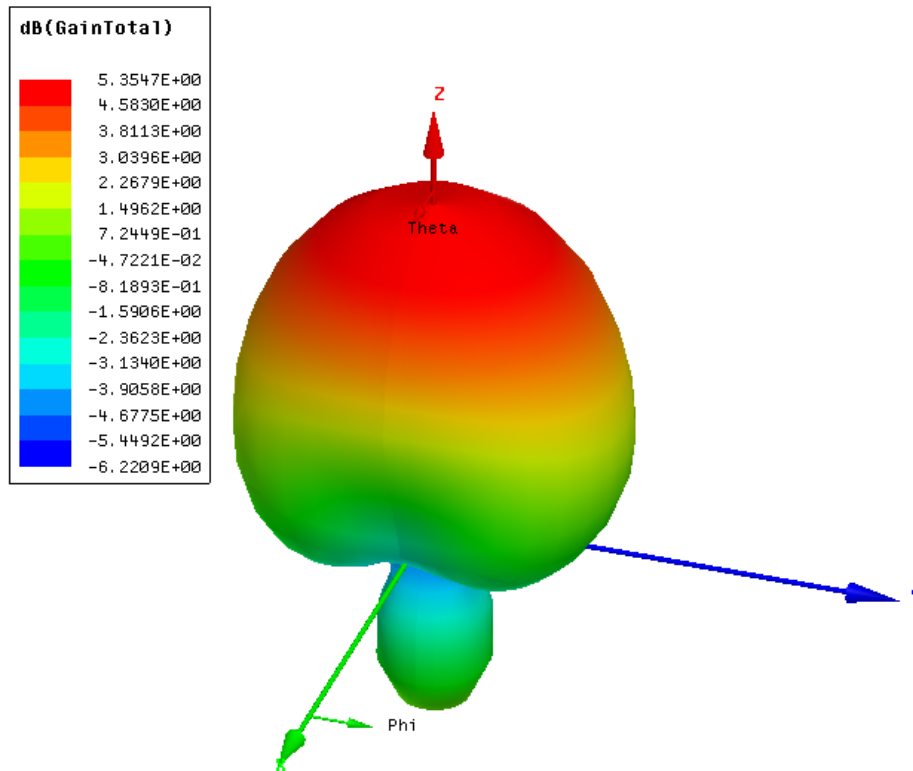
(b)

Fig. 4.9. (a) Electric field inside the DRA structure when excited with two differentially driven ground slots, (b) Total gain and radiation pattern
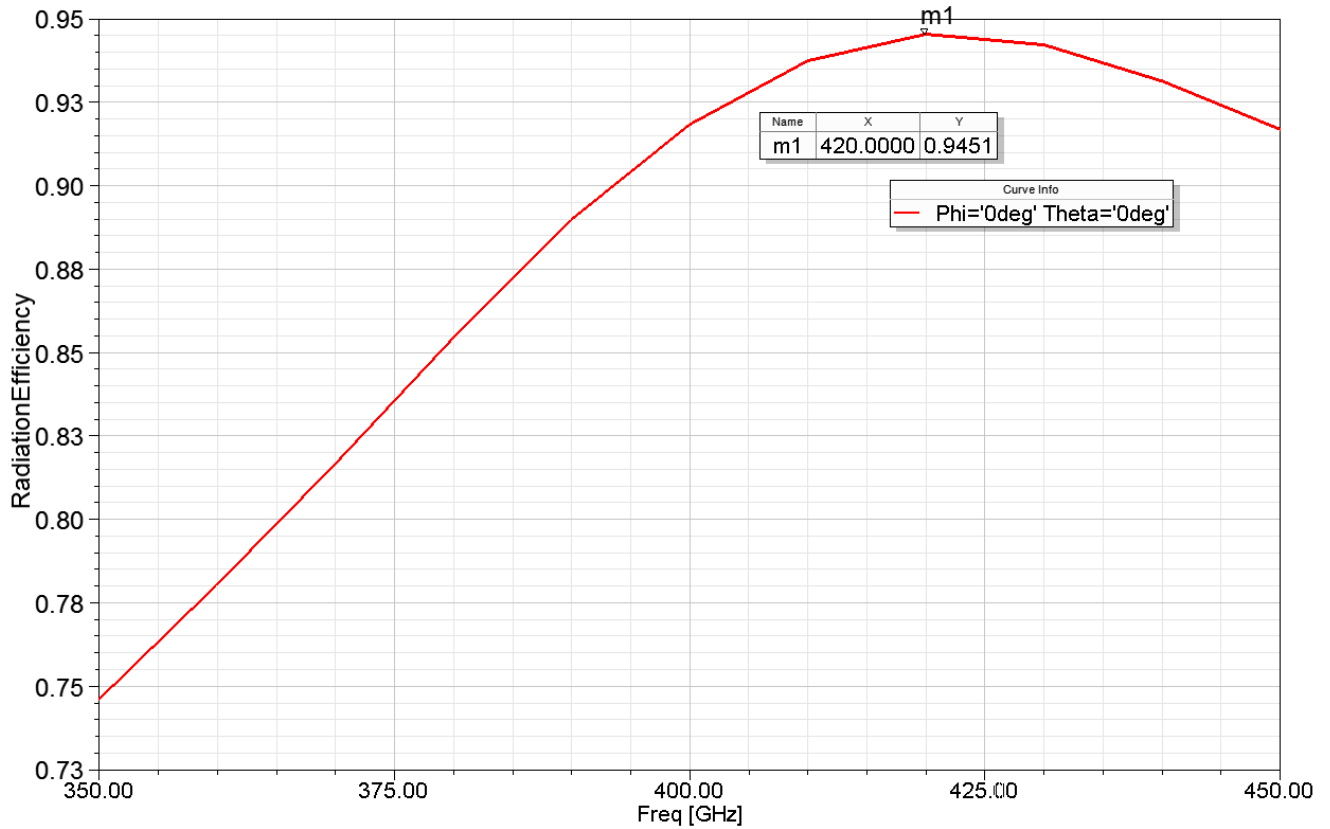
Fig. 4.10. Radiation efficiency of the DRA with differential port excitation

4.7 Power Combining inside DRA

A low-loss power combiner is an essential component in any sub-THz transmitter architecture for generating a high power output signal. In my quest to obtain higher radiation power, I realized that a DRA could also work as a power comber if excited through multiple co-phased ports. In this simulation setup, the same DRA structure of Section 4.5 with a 30 µm silicon slab attachment is excited through two pairs of differentially driven slots. These two pairs are oriented alongside each other in such a way that they both excite the same $HEM_{11\delta}$ radiating mode inside DRA. As a result, the power coming from all four ground slots is combined inside the DRA. Fig. 4.11 shows this configuration. The power combining performance can be verified by checking radiation efficiency of DRA when all 4 ports are driven. As shown in Fig. 4.12, *P1* and *P2* are driven differentially and have 180° phases shift. *P1* and *P3* are co-phased similarly to *P2* and *P4*. The four slots have identical dimensions of $W_S \times L_S$. Horizontal and vertical separation of the slots are optimized to obtain maximum radiation efficiency shown in Fig. 4.13.

39

(a)   (b)
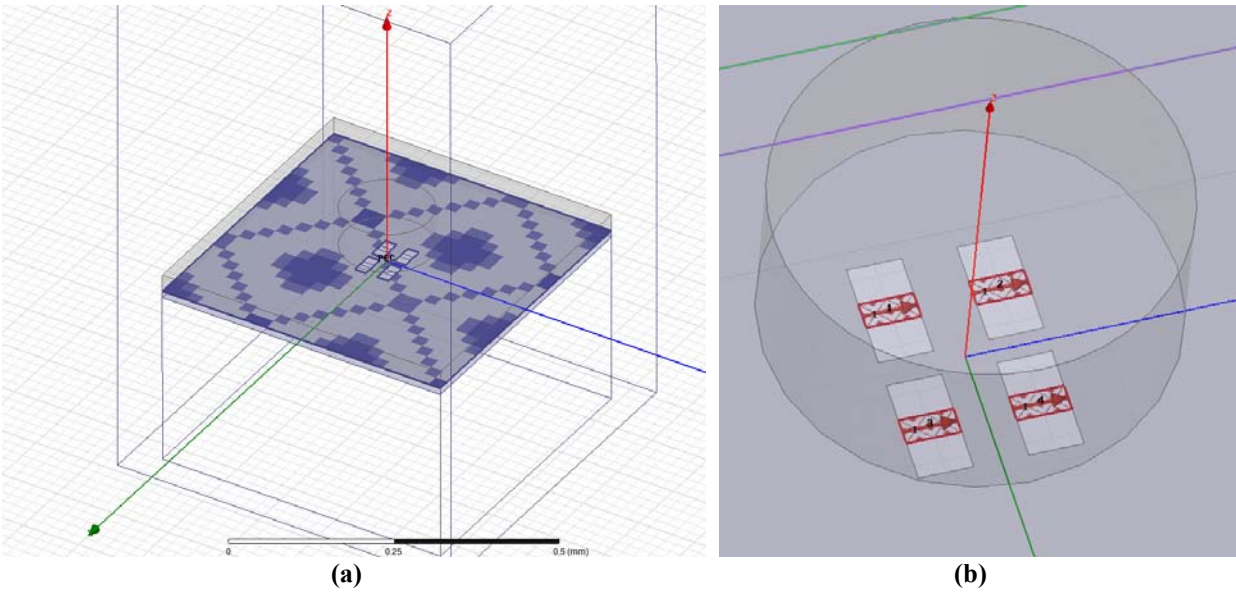
Fig. 4.11. (a) DR with silicon slab is excited through four ground slots. (b) Two sets of differentially driven ports excite the slots and excite a single DRA
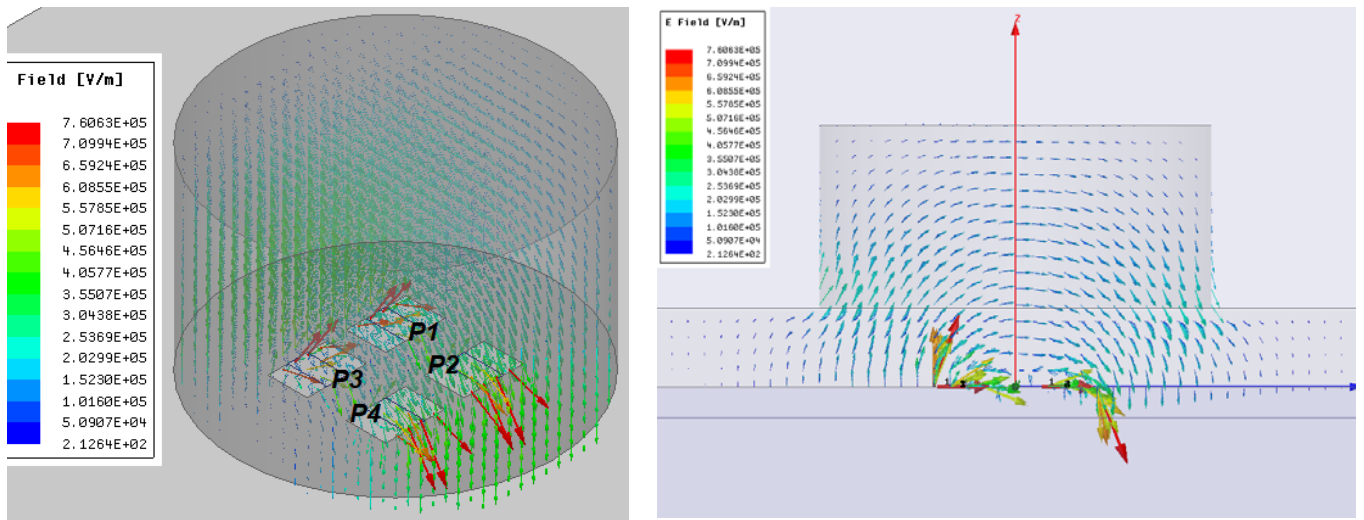
Fig. 4.12. The Electric field inside the DRA with differential ports
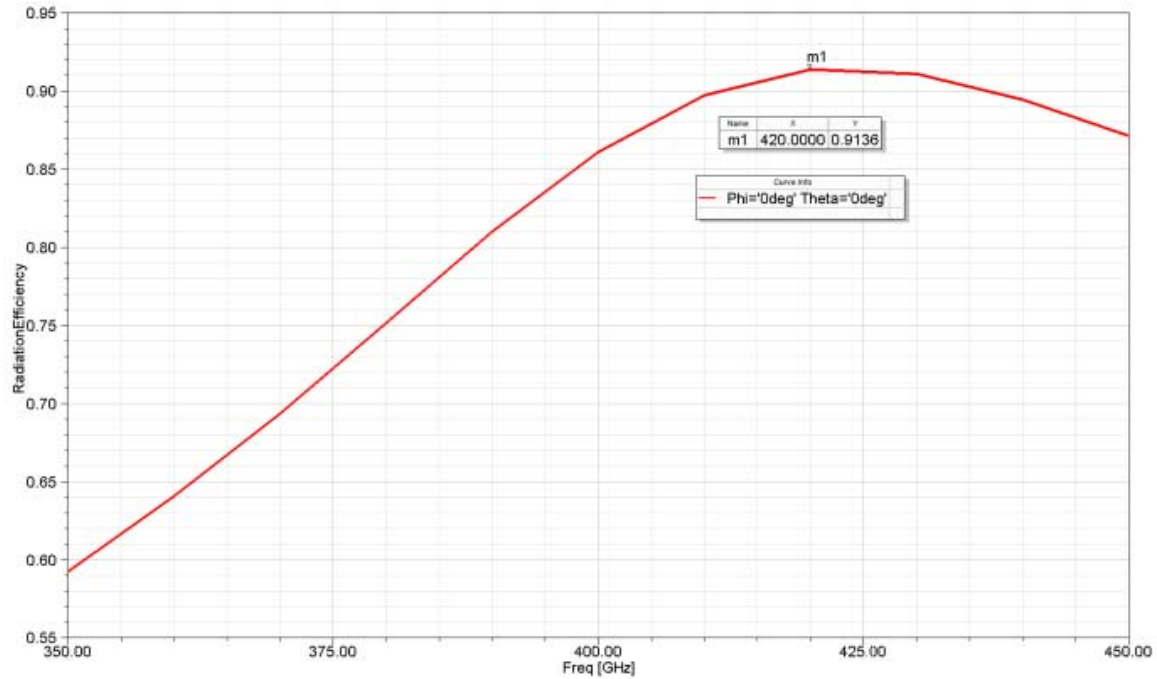
(a)
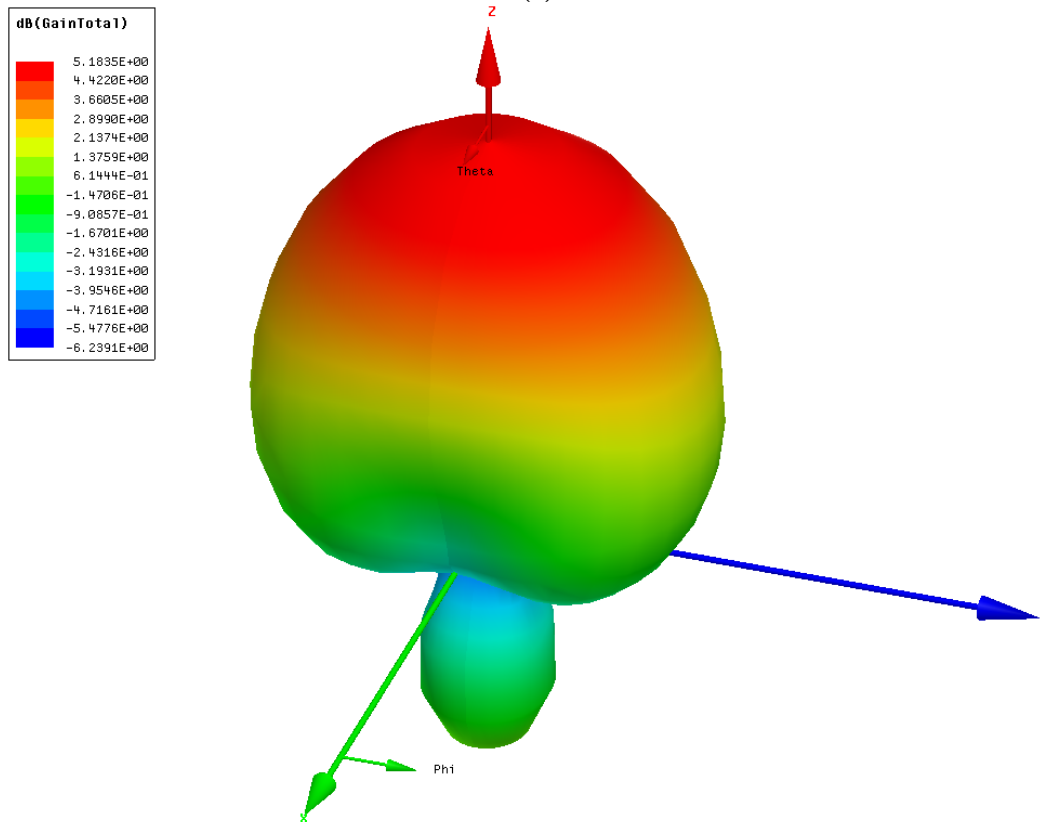
(b)

Fig. 4.13. (a) Radiation efficiency of a DRA excited by two differentially driven ports,
(b) Total gain and radiation pattern

The input impedance of the input ports: *P1*, *P2*, *P3* and *P4* are identical. The impedance reactance part is a function of W_S, L_S. Because the four slots are positioned symmetrically with respect to the XY-axis, W_S and L_S values of each slot are limited to the circular area underneath the DRA and the X-Y separation distance between the slots. Fig. 4.14 shows the variation of input port reactance due to the W_S and L_S sizes. It is important to note that as exciting ports across the slots are ideal the port resistance remains at around 1 Ω and vary not more than 0.1 Ω.
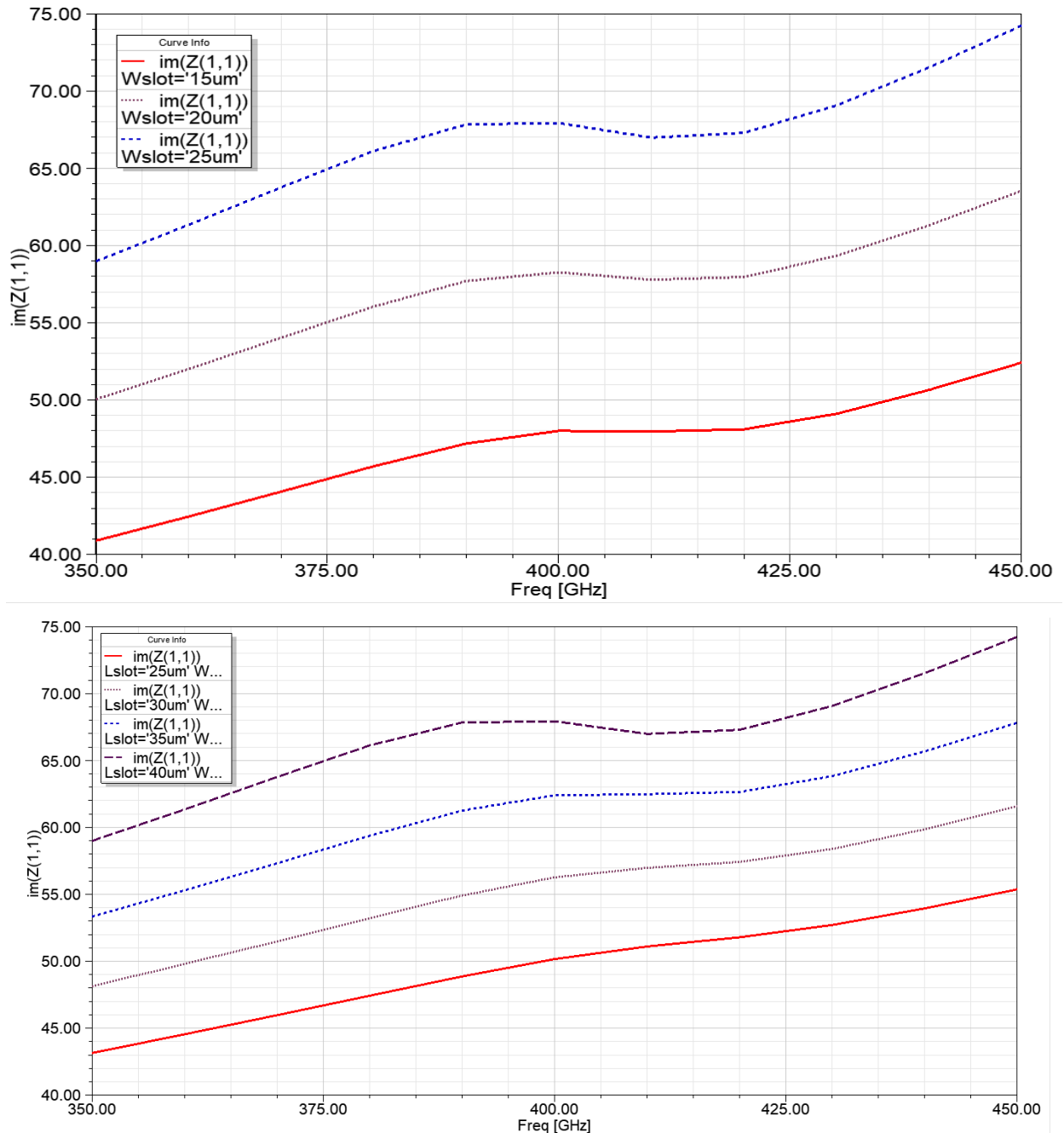
Fig. 4.14. Variation of input port reactance with W_S and L_S

4.8 DRA Array Tray (DRAAT)

Antenna arrays are used to achieve higher antenna gain and narrower main beam lope. Beam steering is another application of antenna array. Normalized array factor of arrays with n identical antennas (elements) is calculated from:

$$AF(\theta, \phi) = \frac{Sin(N\Psi/2)}{N\,Sin(\Psi/2)} \,, \quad \Psi = (kd\cos\theta + \beta) \tag{4.7}$$

where d and β are the distance and phase difference between the successive elements respectively. By changing β electronically, beam will steer to point at different directions in space. Since the objective of this work is to achieve maxim um gain for a given array size, all the antenna elements have identical current excitations with the same amplitude and phase. Therefore, β is considered as 0 through-out our design. By choosing $d = \lambda/2$, we can obtain maximum directivity in the broad side.

A 4×4 antenna array is investigated and developed in this work. In a simulation model, sixteen cylindrical DRAs are arranged in the form of a 4×4 array. DRAs are spaced at $\lambda_0/2 = 360$ µm from each other. All DRAs are attached together through a 30 µm HRS carrier with the same material as DRAs. The effect of addition of this carrier layer on the performance of the DRA was described in Section 4.5. This structure of 4×4 DRAs with the attached silicon carrier is referred to as DRA Array Tray (DRAAT) is shown in Fig. 4.15. DRAAT is first simulated with each DRA is excited by a single loss-less source. This simulation would provide the reference (best) performance metrics that is required for assessing the further adjustments to the DRAAT. Each DRA is excited by a single ground slot driven by an ideal port across the slot. DRAAT shows total gain of 15.83 dB and radiation efficiency of 0.98 as shown in Fig. 4.16 and Fig. 4.17 respectively.
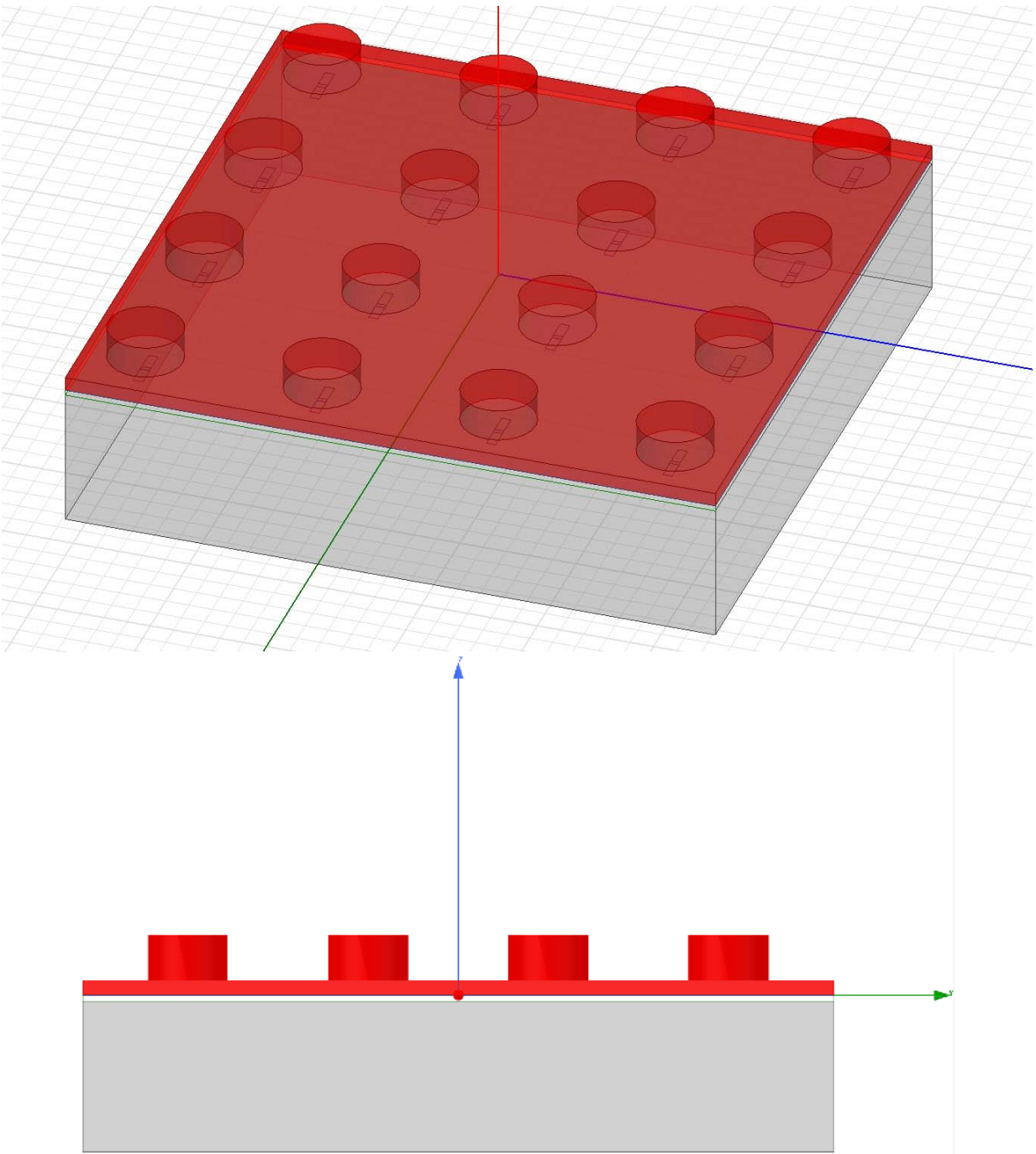
Fig. 4.15. The 4×4 DRAs connected through a 30 µm silicon slab (DRAAT). DRAAT is positioned on top of a TSMC65nm die model. Each DRA is excited through an ideal port across a single ground slot
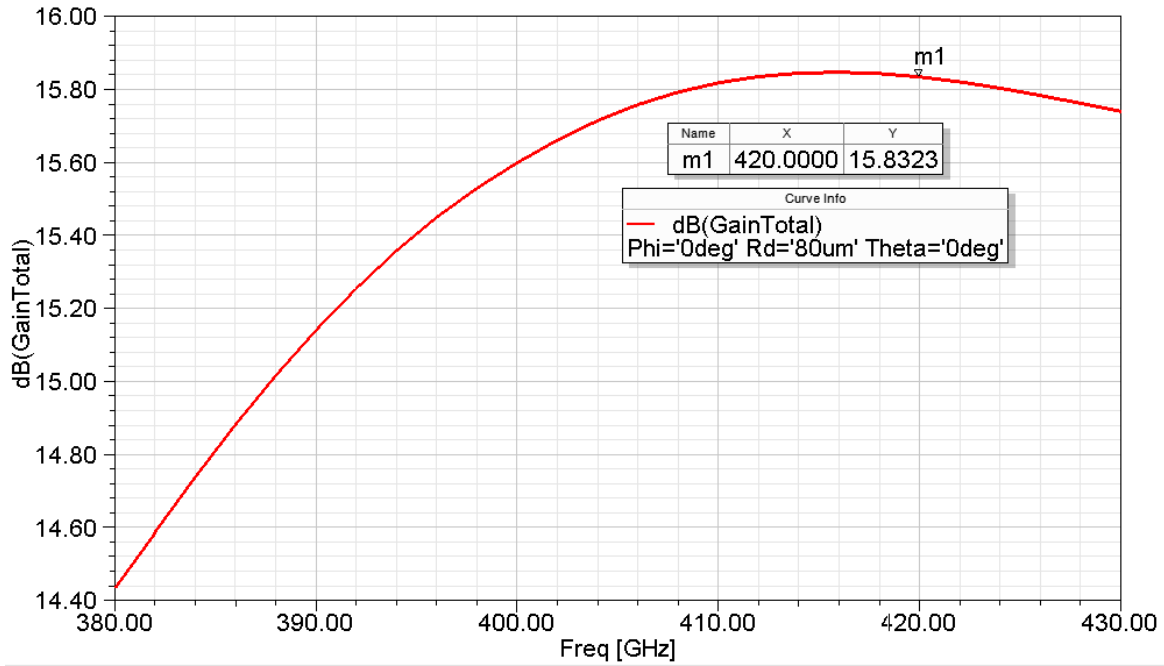
(a)
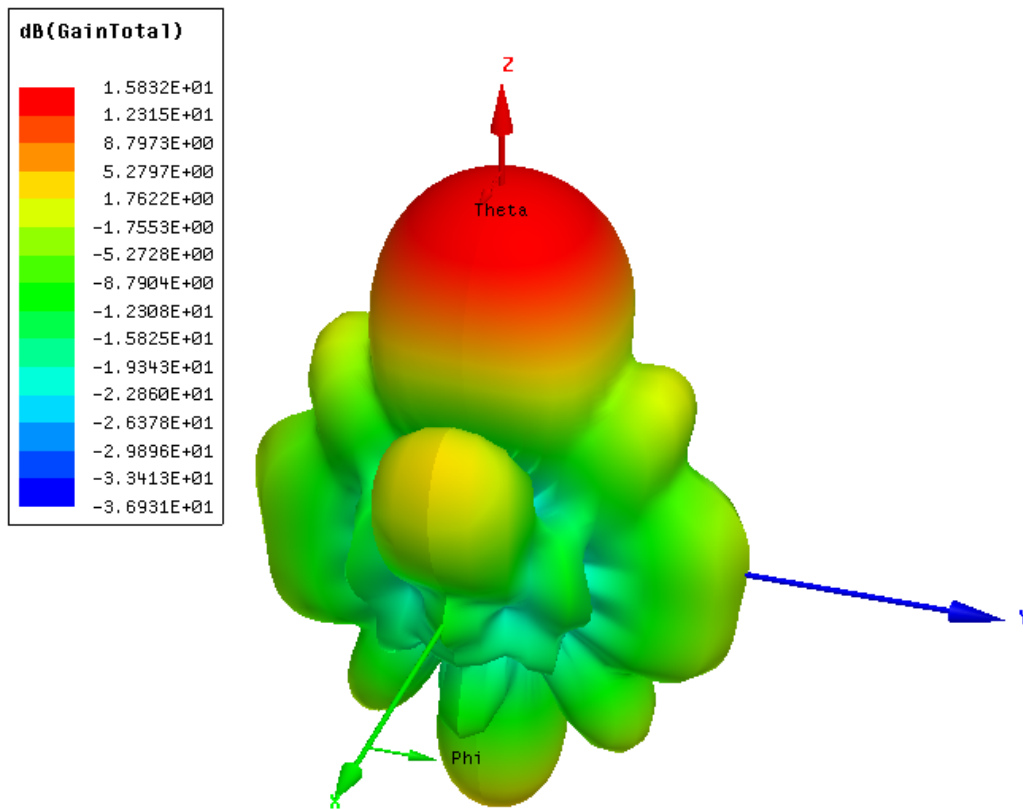
(b)

Fig. 4.16. Total gain of 4×4 DRA module with loss-less excitation. (b) Total gain pattern of array at 420 GHz
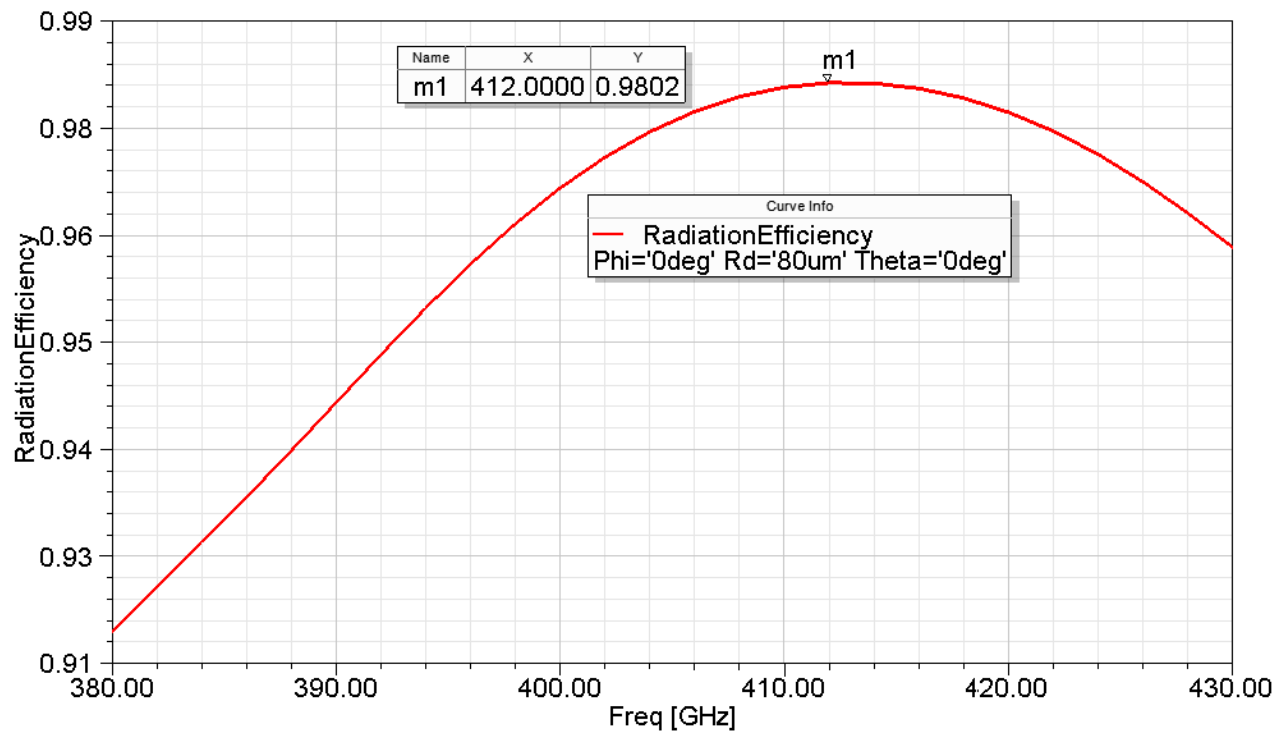
Fig. 4.17. Radiation efficiency of 4×4 DRAAT. DRAs are excited through a single loss-less ground slot

4.9 DRA Excitation with Microstrip Line

Now that we have verified the feasibility of implementing a DRA array as a separate module on top of an active die, more details of our proposed assembly scheme are added into the simulation models. In all previous simulation models, DRA was excited with ideal lump port across a ground slot. In our proposed integration scheme, the active die underneath the DRAAT excites the ground slots with a MTL implemented inside the active die. Therefore, in the following simulations, a MTL model replaces all the previous ideal ports. TSMC65nm with 9 metal layers configuration is used in this work to implement the active die. MTL vertical dimensions are determined by the metal layer stack up in TSMC65nm technology. The top metal layer of the die which is the *AP* layer is proposed to be grounded to embed the aperture slots for exciting the DRAs. For such an arrangement, an upside-down configuration for MTL is then anticipated to use the same top metal *AP* layer of the active die as the ground. *M8* is used to realize MTL signal line. Fig. 4.18 shows cross-section view of this configuration where a DRA is placed on top of a TSMC65nm die. The aforementioned configuration is used to model MTLs in a new simulation of DRAAT as shown in Fig. 4.19 (a)(b). Four MTLs underneath four ground apertures excite a single DRA.
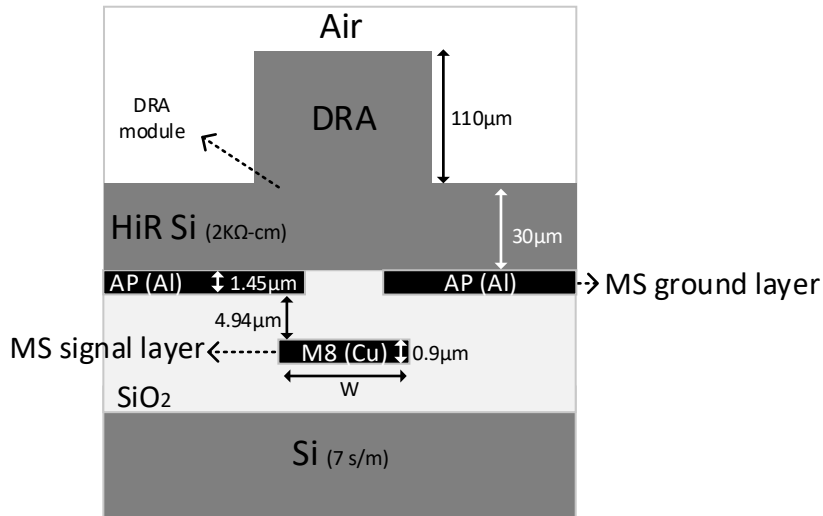
Fig. 4.18. Implementation of antenna feed line in TSMC65nm technology. *AP* **layer is used as MTL ground. DRA module is placed on top of active die. Ground slots in** *AP* **layer excite the DRA**

Two pairs of differential lump ports drive the four MTLs. Fig. 4.19 (c) shows the E-field vectors around the MTLs aligned with the fields of $HE_{11\delta}$ mode inside the DRA.

(a)

(b)

(c)
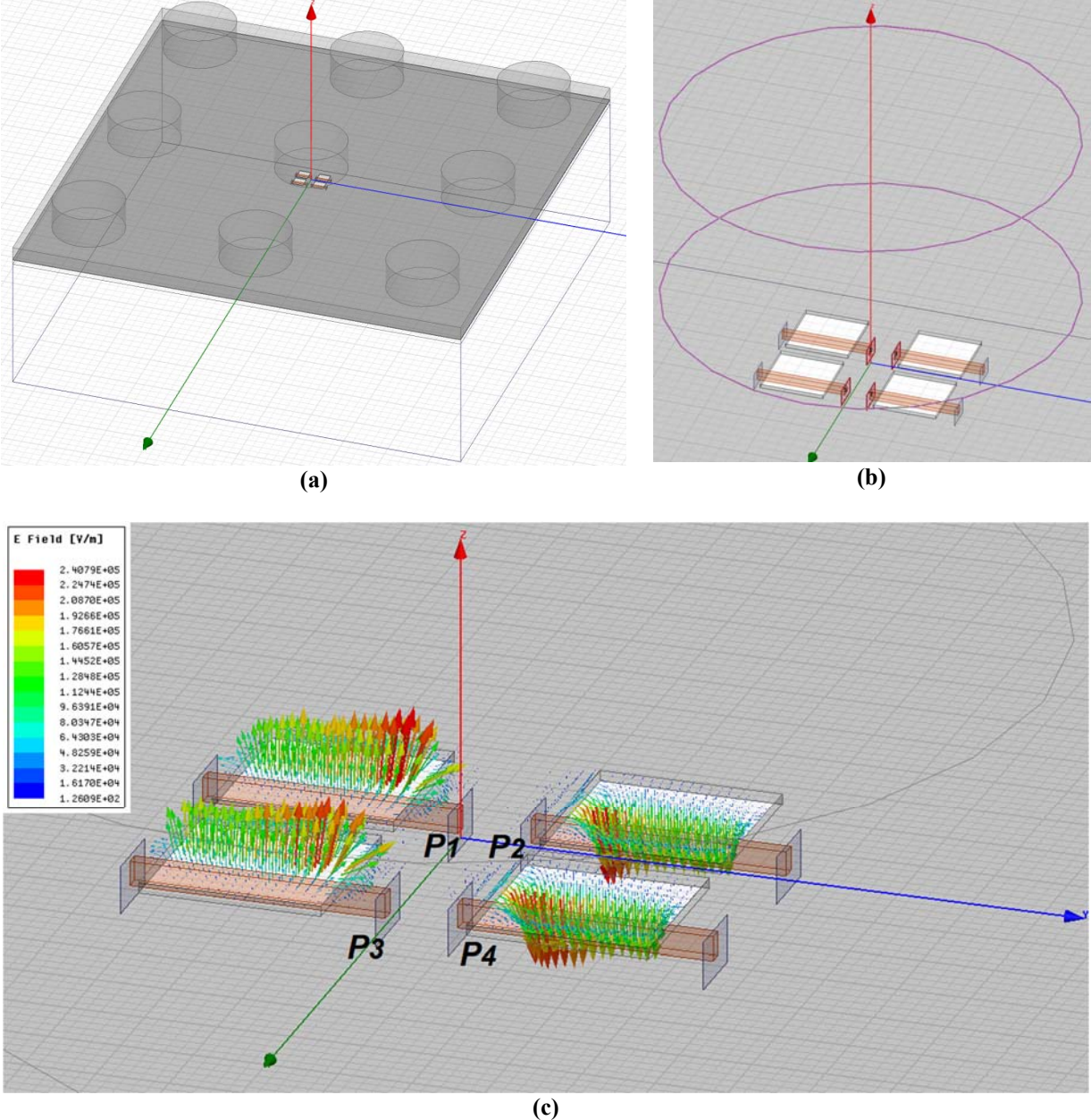
Fig. 4.19. (a)(b) DRAAT is placed on top a TSMC65nm die. (c) One DRA is excited trough four ground slots. Two sets of differentially driven MTLs excite the four ground slots

With all four ports driving a DRA, radiation efficiency is at 0.85 and the gain is 6 dB, as shown in Fig. 4.20.
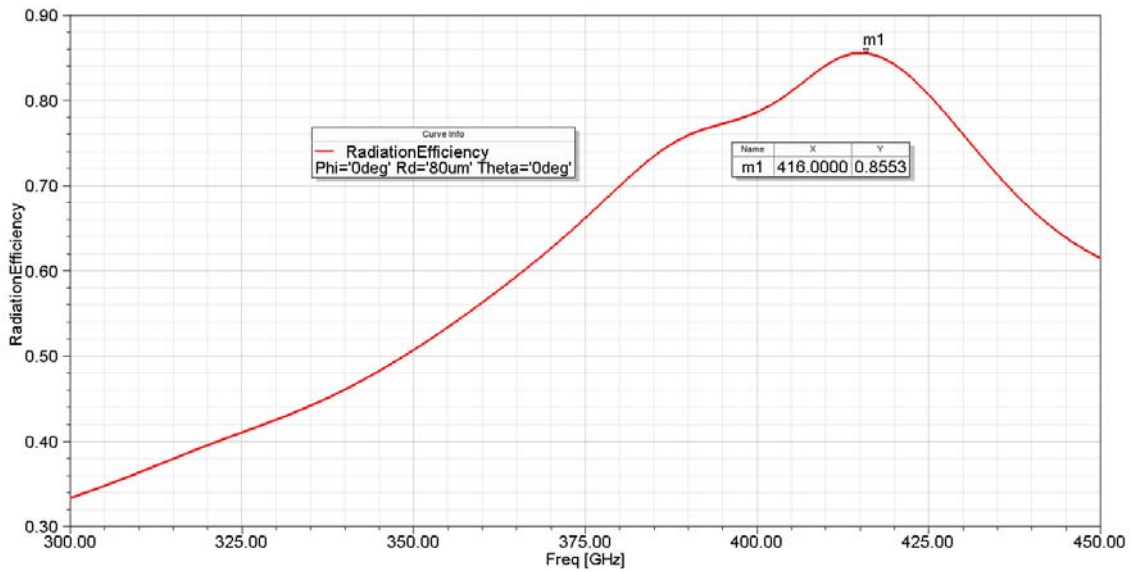
(a)
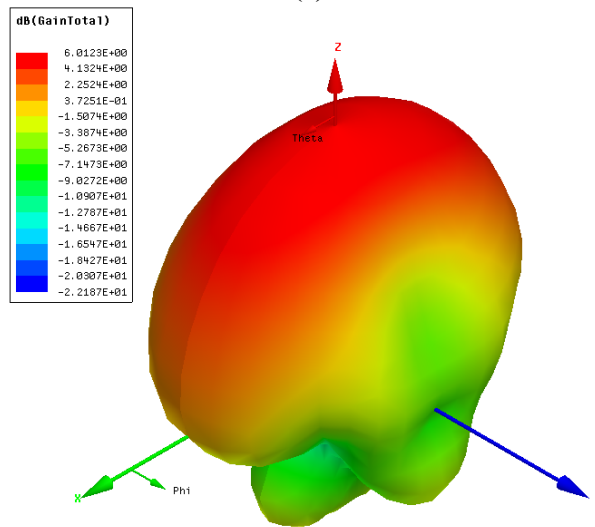
(b)

Fig. 4.20. (a) Radiation efficiency, (b) total radiating gain pattern of one DRA excited with differentially driven MTLs

The input impedance of the MS ports, $P1$, $P2$, $P3$ and $P4$ are identical. The impedance is a function of W_S, L_S, and the width of microstrip line. As shown in Fig. 4.21 wider and longer slots will result in higher reactance. The reactance can vary from 30 to 120 Ω which will result in an inductance of 34 to 125 pH at 420 GHz. The input resistance of the MS ports also changes as the

dimension of the slot varies. Fig. 4.22 shows the variation of the input resistance when the MS line has a fixed length at 35 µm and width of 5 µm. Resistance changes are from 2 to 20 Ω at 420 GHz.
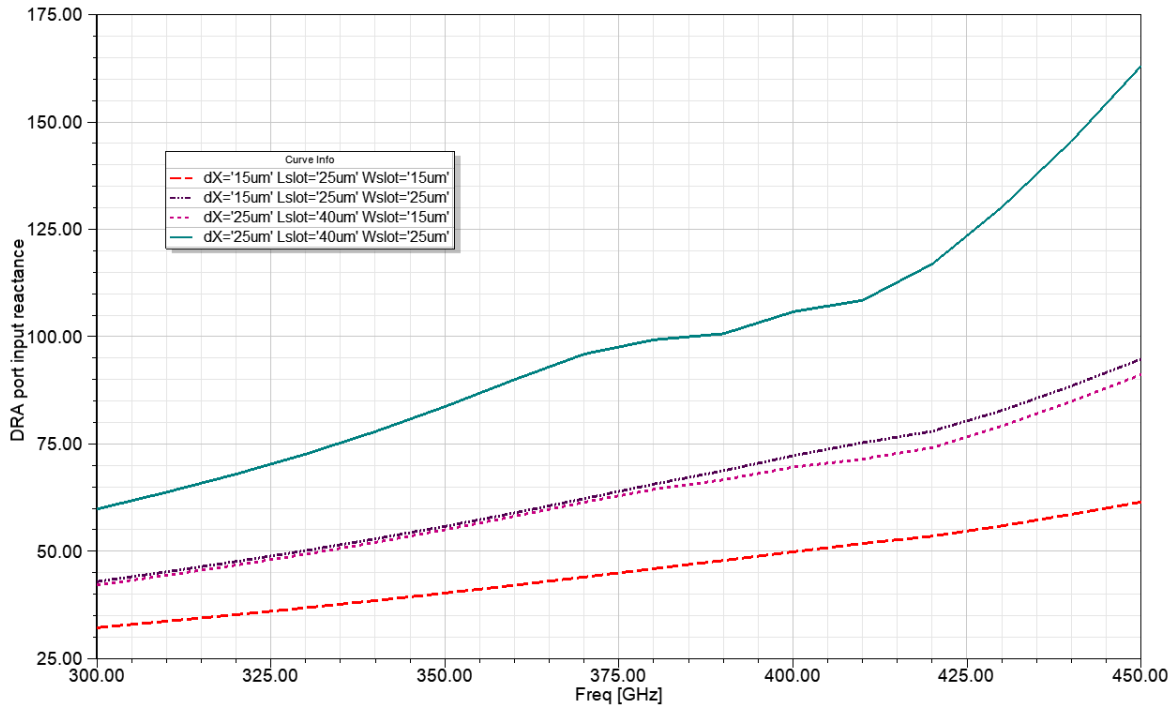
Fig. 4.21. Input reactance of each of the four MS ports
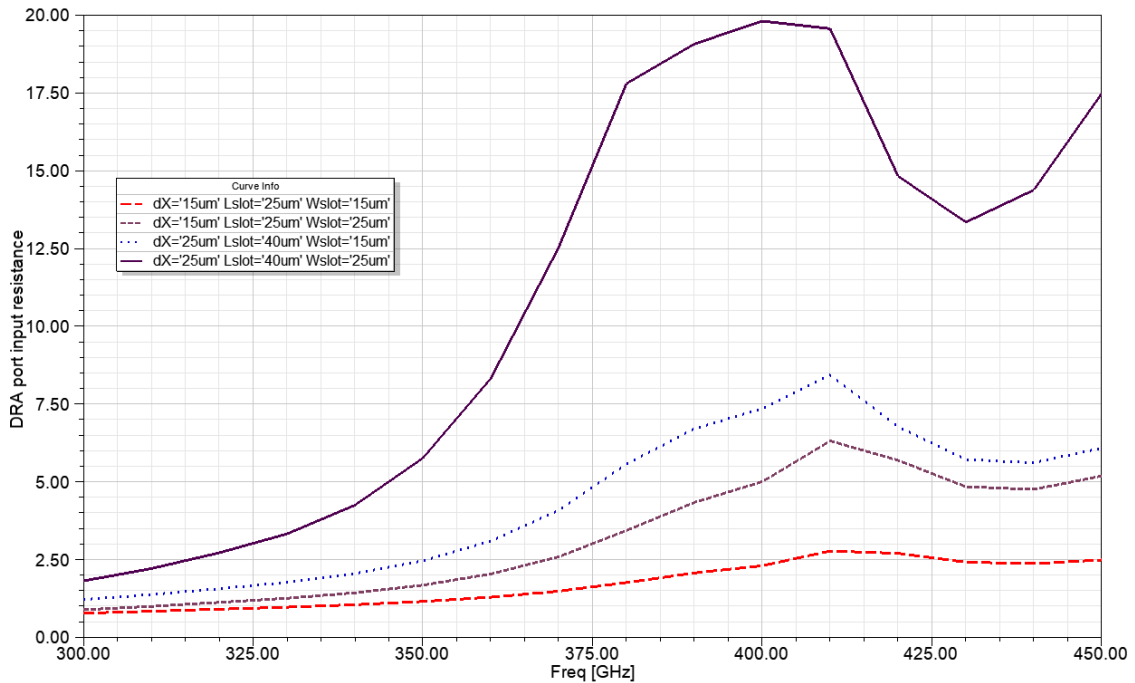
Fig. 4.22. Input resistance of each of the four MS ports

4.10   4×4 DRAAT

In this simulation, a 4×4 DRAAT is modeled where all 16 DRAs are excited through a total of 64 ground slots in the active die. Each DRA is excited through 4 ground slots, similar to the previous Section 4.9 model. Two pairs of differentially driven MTLs excite the 4 ground slots of each DRA. Fig. 4.23 shows the HFSS model. All MTLs are modeled in a way that they can be implemented in TSMC65nm technology with 9 metal layer stack up as shown previously in Fig. 4.18. The total gain radiation pattern with the peak gain of 15.8 dB is shown in Fig. 4.24.

(a)

(b)

(c)
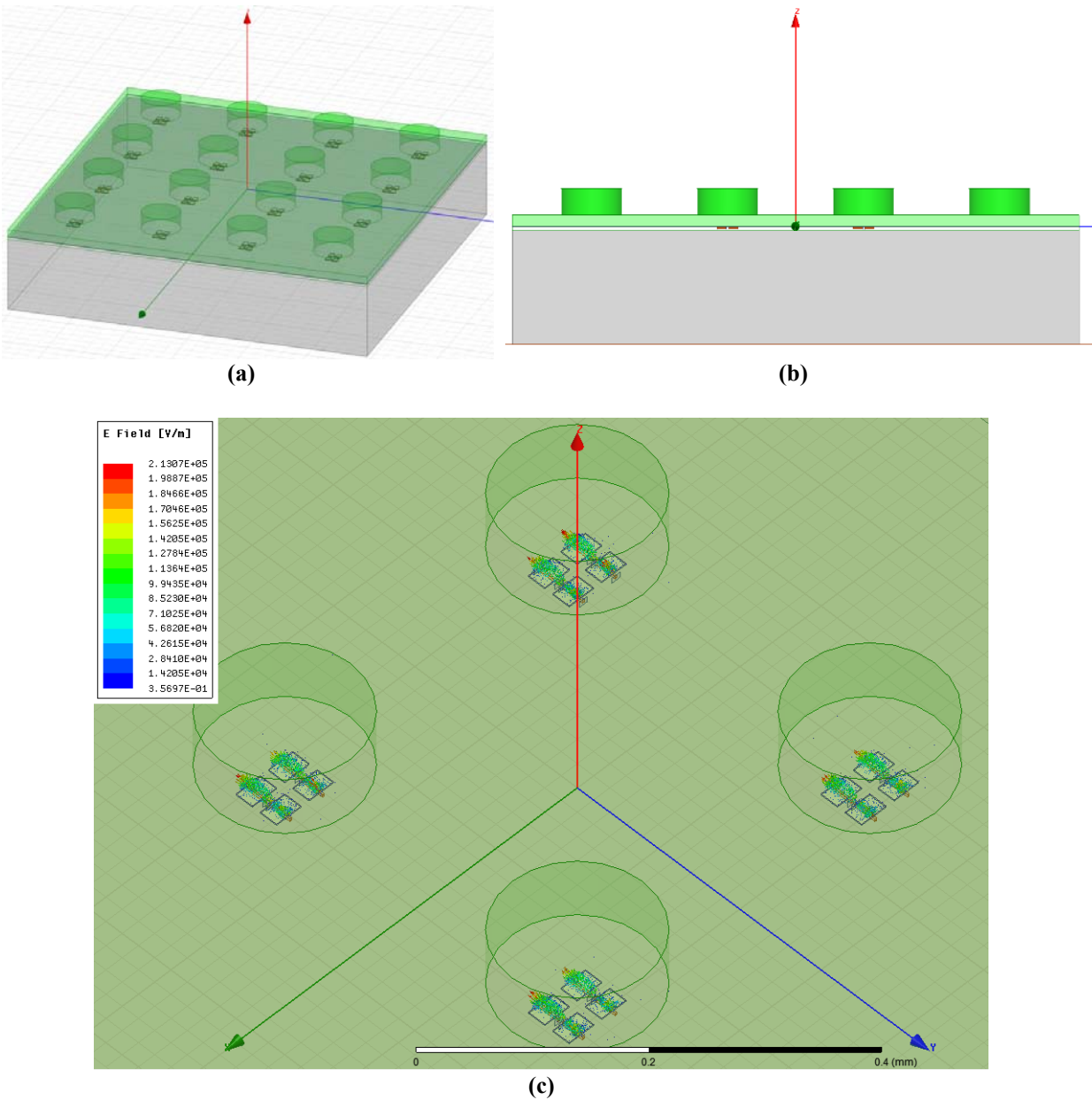
Fig. 4.23. E-field vectors around differentially driven MTLs for each DRA.
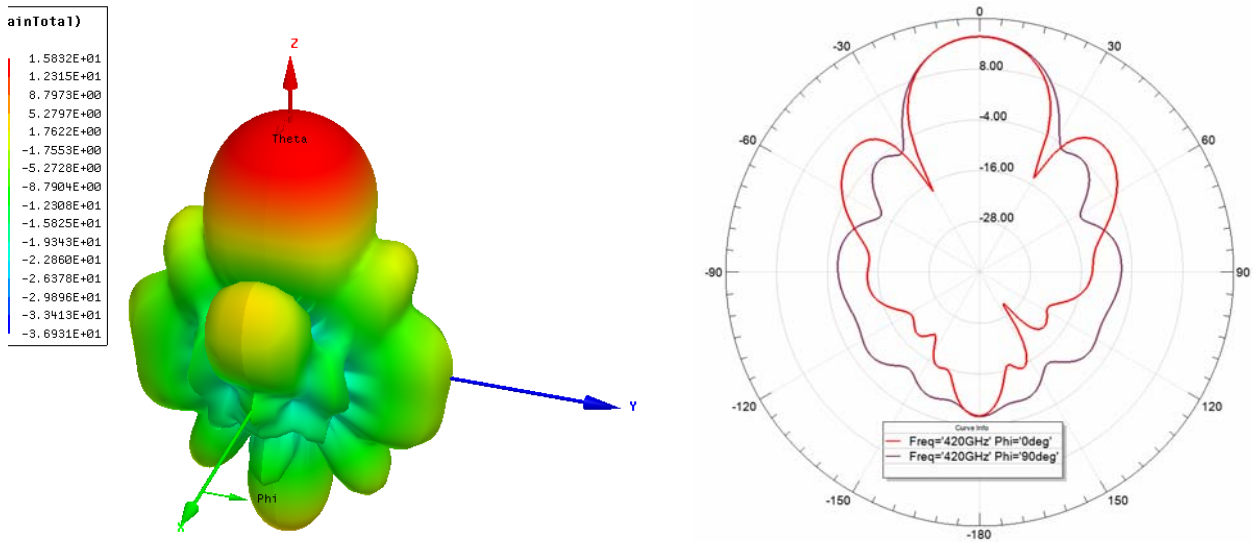
Fig. 4.24. Total gain radiation pattern of the 4×4 DARAAT

4.11   The 4×4 DRA Array Module (DRAAM)

The main challenge in 3D integration of multiple stack-up dies is the alignment mechanism. One major achievement of this work is the introduction of a new integration methodology for DRA array with an active die. This work proposes a pocket-shape structure as shown in Fig. 4.25 to address the alignment problem. The cavity has the same length and width of the active die which make the DRA module to fit tightly on top of the die. This approach keeps the DRA module in a fixed position on top of the active die during the assembly process, and it does not require any further alignment. The new structure is called DRA Array Module (DRAAM).

The active die should have DC connections to the outside. In our integration scheme, the top side of the die will be covered by the DRAAM. Some may suggest, use of through-silicon-via (TSV) in the active die is a suitable solution for these types of assembly scenarios. With TSV, IO pads can be routed to the bottom side of active die and will be accessible from the carrier PCB. Although TSV is an interesting solution, but it requires an expensive back-end-of-line (BEOL) processing. TSV is not an efficient and high performance interconnect technique for sub-millimeter-wave/THz range of frequencies. In the approach proposed here, two cut-outs are made in the structure of the DRA module to expose the die IO pads for wire bonding. These cut outs are

52

positioned wisely and have offset from the chip corners so they do not interfere with the alignment features of the structure. Simulated gain radiation pattern of DRAAM is shown in Fig. 4.26 when all 16 DRAs are excited through 64 sources. DRAAM shows an efficiency of 0.75 as shown in Fig. 4.27 at 420 GHz.
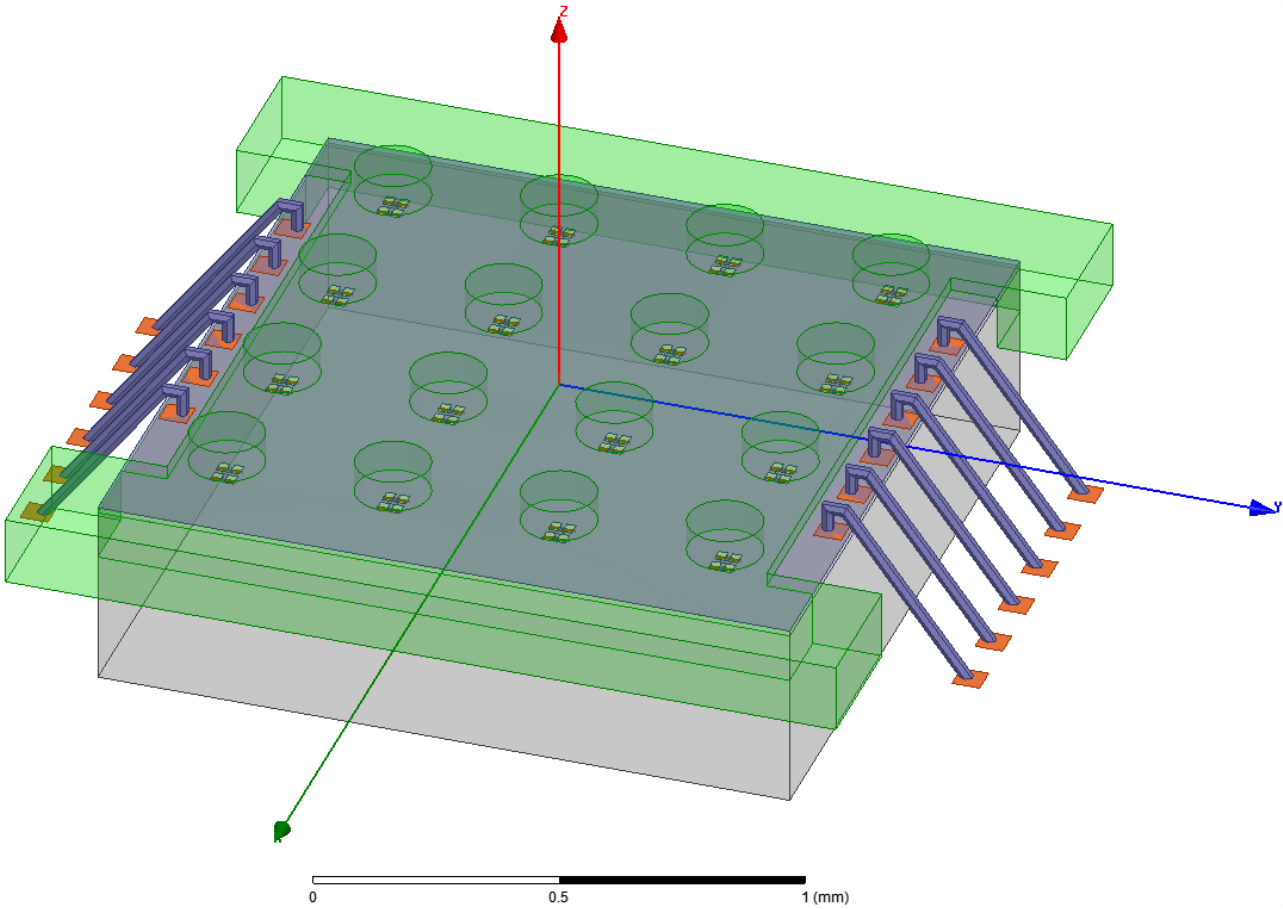
Fig. 4.25. DRA Array Module (DRAAM). DRAAM is a DRAAT plus the added alignment features for assembling on top of an active die.
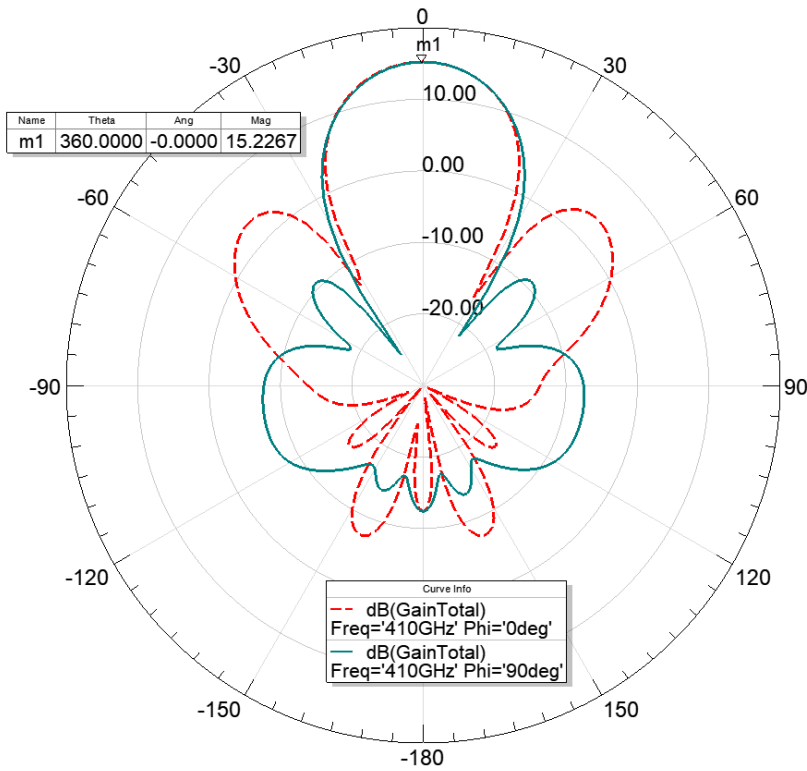
Fig. 4.26. DRAAM total gain radiation pattern
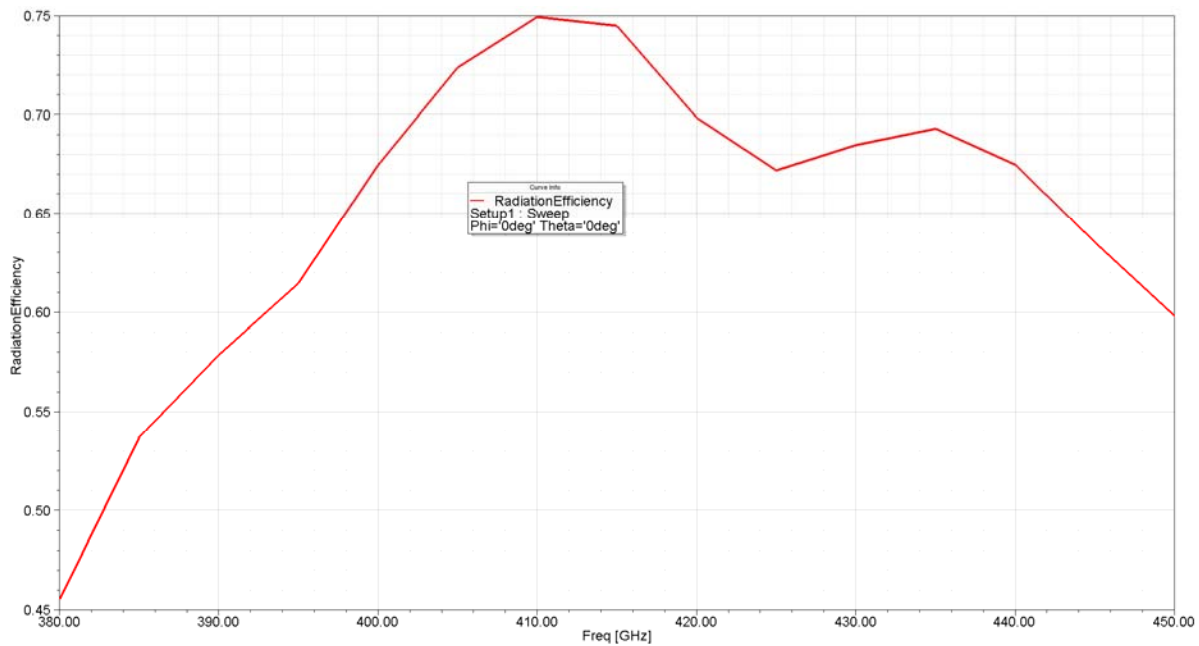
Fig. 4.27. Radiation efficiency of DRAAM versus frequency

CHAPTER 5   420 GHz Source with 4×4 DRA Array Module (DRAAM)

Harmonic generation by nonlinearity is a conventional way to create signal frequencies above the f_{max} of a given technology. Higher order harmonics of the fundamental frequency are generated when an active device is biased to work in a non-linear regime. Circuit simulators use the most accurate high frequency models of the devices provided by the foundry. Therefore, the best way to optimize the bias point for generating the maximum power of a desired harmonic is through the simulation. This work targets a 420 GHz transmitter. It focuses on 3rd harmonic signal generation from an oscillator with a 140 GHz fundamental oscillation frequency. Chapter 2 covered the implementation of a 140 GHz oscillator. In this Chapter, an active tripler circuit that follows the 140 GHz oscillator is described. Then the implementation of the injection locking circuit that connects each individual signal source to the H-tree network of Chapter 3, is explained. In Section 5.3 the network of 32 injection locked signal sources and the final active die layout and implementation is presented.

5.1   Tripler Circuit

Tuned circuit topologies are well known for providing a large gain over a narrow bandwidth. In this work the tripler is designed based on a tuned amplifier methodology but without using an actual inductor component in the drain. Since the tripler is directly driving a DRA, this work proposes to use the reactance of the input port of the DRA to tune the tripler circuit. Specifically, the antenna feed circuit is a part of the tripler circuit acting as an inductor load. The input impedance of the DRA is tunable through the dimension of the slot, $W_S \times L_S$, as well as the width of the feed line W_f as shown in Fig. 5.1.

The tripler circuit proposed in this work is shown in Fig. 5.2. The g_m of an nMOS device is proportional to the square root of bias current (I_D) as well as the width of the device (W_Q). In order to maximize the output power of the tripler, the width of the device and I_D must be increased as much as possible. However, there are two main factors that limit the increase of the device size.

One is the increase in the C_{gs} which is limited by the driving capability of the preceding block which is the 140 GHz oscillator buffer. Another is the increase in the amount of parasitic C_{ds} and C_{gd} when W_Q increases which decrees the harmonic power by limiting the bandwidth. Through Spice simulation, 7 figures for Q_5 and Q_6 at total $W_Q = 5.6$ μm resulted in the highest harmonic power achievable when loaded with a 30 pH inductance. Sweeps of input impedance of DRA ports versus L_S and W_S was shown in Fig. 4.21 and Fig. 4.22 plots. A $W_S \times L_S$ of 25×25 μm with $W_f = 5$ μm for feed line results an input impedance of about $Z_{dra} = 5 + 80j$ Ω (as shown in Fig. 5.2) at 420 GHz for each of the DRA input ports. The interconnecting line between FBO and the tripler Q_5 and Q_6 deceives shows 5.2 pH parasitic inductance in simulation. AC coupling capacitor of C_C is set to 167 fF and R_b of tripler is 4.4 KΩ.
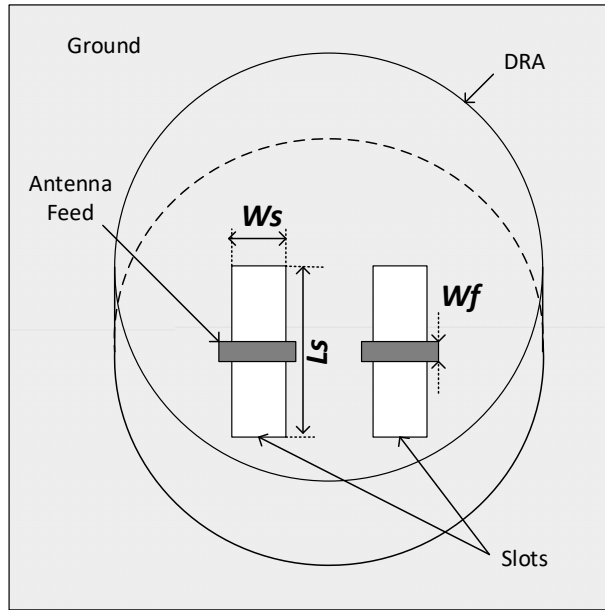
Fig. 5.1. Input impedance of DRA ports is tunable by changing W_S, L_S or W_f
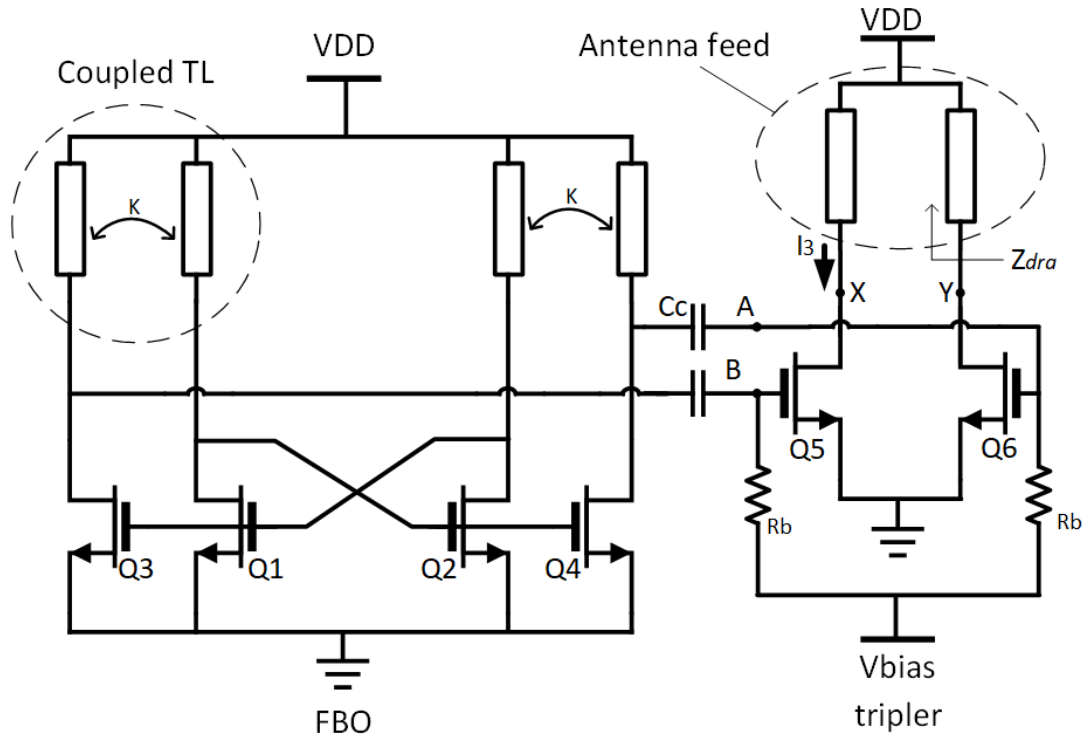
Fig. 5.2. Tripler circuit follows the 140 GHz feedback oscillator

The FBO generates an output voltage swing of 2 V_{pp} on the *AB* node as shown in Fig. 5.3. V_{bias} of 120 mV for tripler results maximum output power of -7.4 dBm on the differential antenna feed indicated as *XY* node. The tripler drain current (I_3) waveform at this optimum bias point for 3rd harmonic power is shown in Fig. 5.4. The tripler circuit consumes 10 uW of DC-power. The combination of the FBO and tripler have a DC-to-RF efficiency of 0.7 % at 420 GHz.
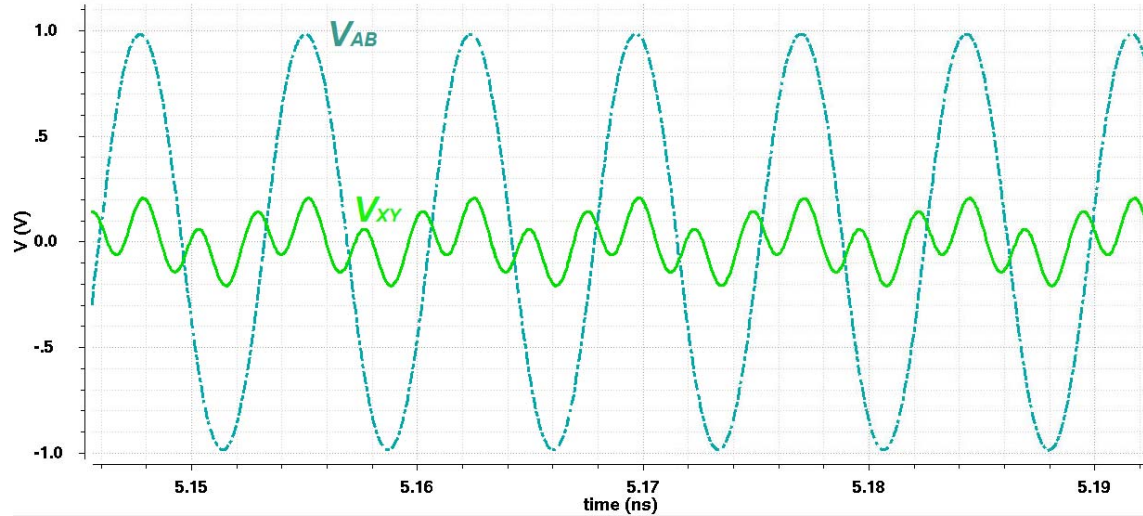
Fig. 5.3. Input (V_{AB}) and output (V_{XY}) Voltage waveforms of tripler
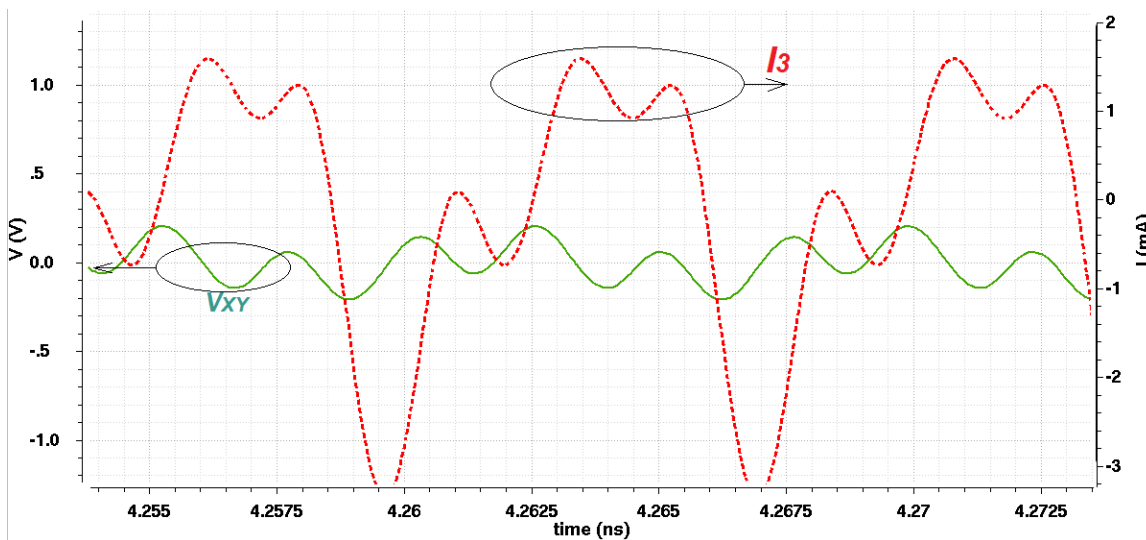
Fig. 5.4. Current waveform and output voltage of Tripler (I_{3})

As explained in Section 4.7, this work proposes a loss-less power combining mechanism inside a DRA. Therefore, two separate FBO circuits followed by two triplers drive a single DRA. This combination is referred to as FBO-Cell as shown in Fig. 5.5. The complete layout of FBO-Cell is shown in Fig. 5.6 and Fig. 5.7.

.
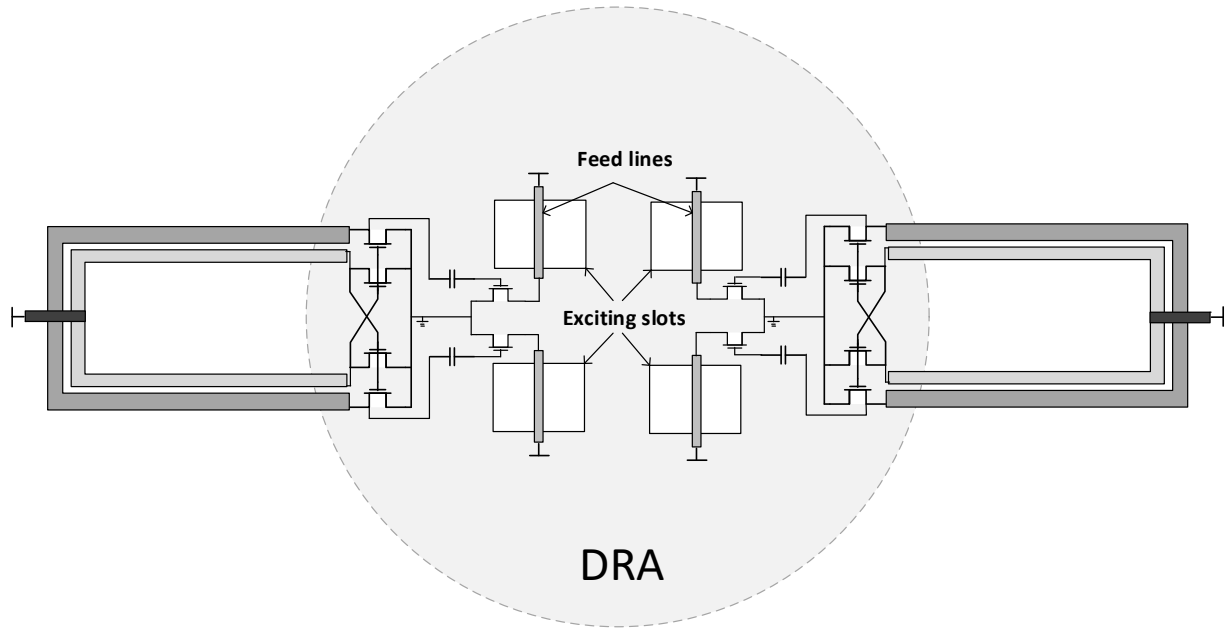
Fig. 5.5. FBO-Cell is composed of two FBOs and two following triplers driving a single DRA
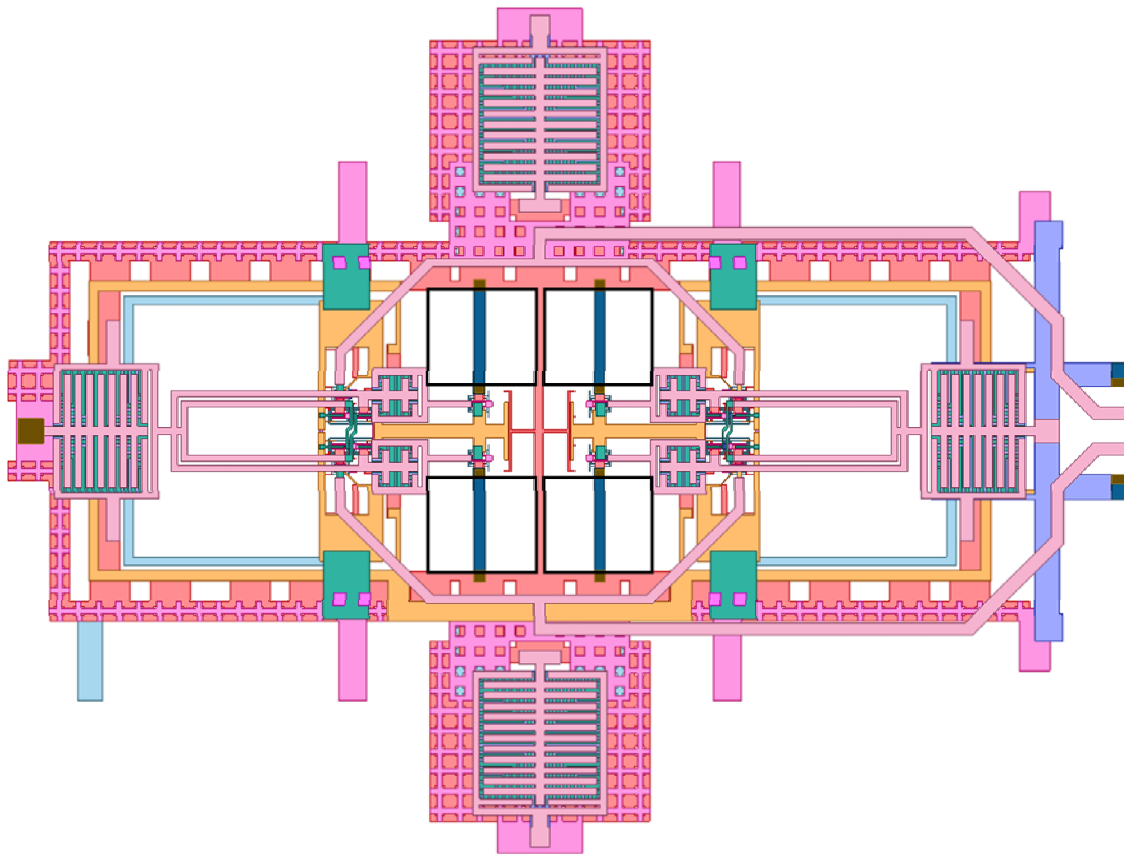
Fig. 5.6. Layout of FBO-cell in TSMC65nm. Top *AP* (ground) layer that contains the 4 ground slots is invisible

59
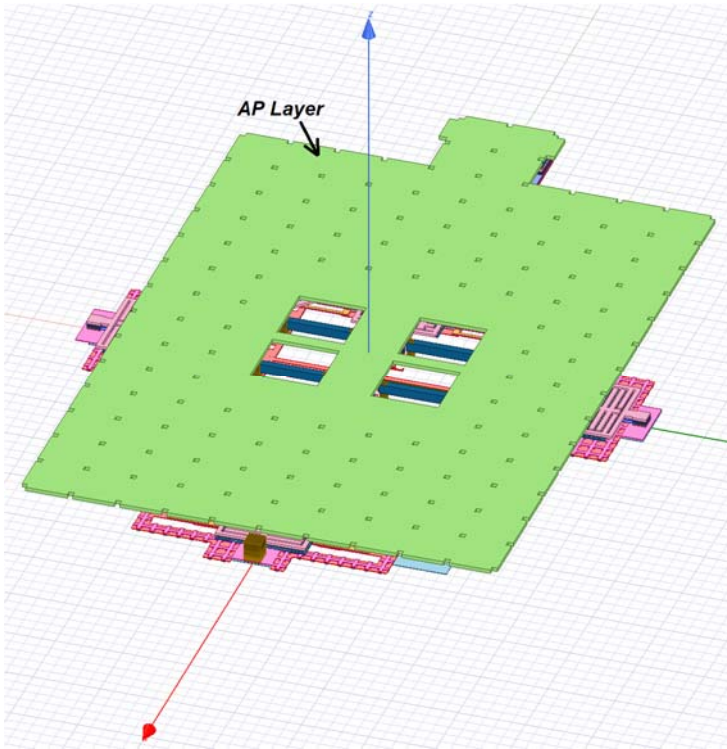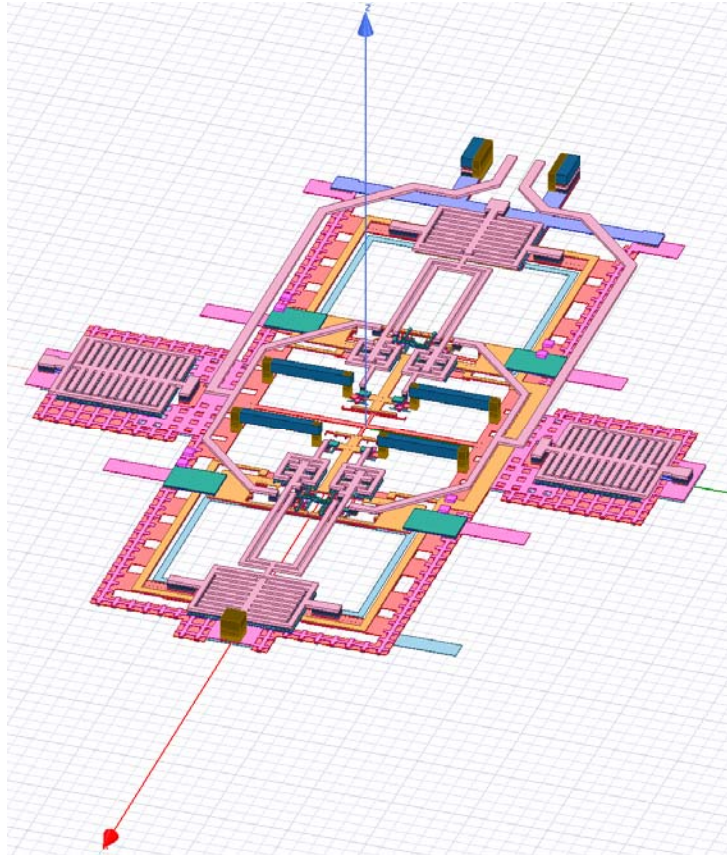
Fig. 5.7. 3D view of FBO-cell layout

60

5.2 Injection Locking Circuit

Consider a free-running oscillator which consists of an ideal positive feedback amplifier and an LC tank. If a signal is injected into the circuit, then the tank current would become a sum of the injected and transistor current. If the injected signal has the same frequency as the oscillator, it will push the oscillation phase to shift according to the phase of the injected signal as the loop gain must have exactly 2π phase shift (or multiples) to sustain the oscillation. The injection locking mechanism is implemented by adding devices Q_7 and Q_8 to the FBO circuit as shown in Fig. 5.8. $Q_{7,8}$ are driven by the differential CPWG from an on chip 140 GHz source. The central oscillator is AC coupled to $Q_{7,8}$. R_1 resistors are 4.4 KΩ for biasing. A degeneration resistor R_s of 70 Ω with a piece of 15 pH transmission line match the input impedance of the two injection ports to 50 Ω for connecting to the H-tree network.
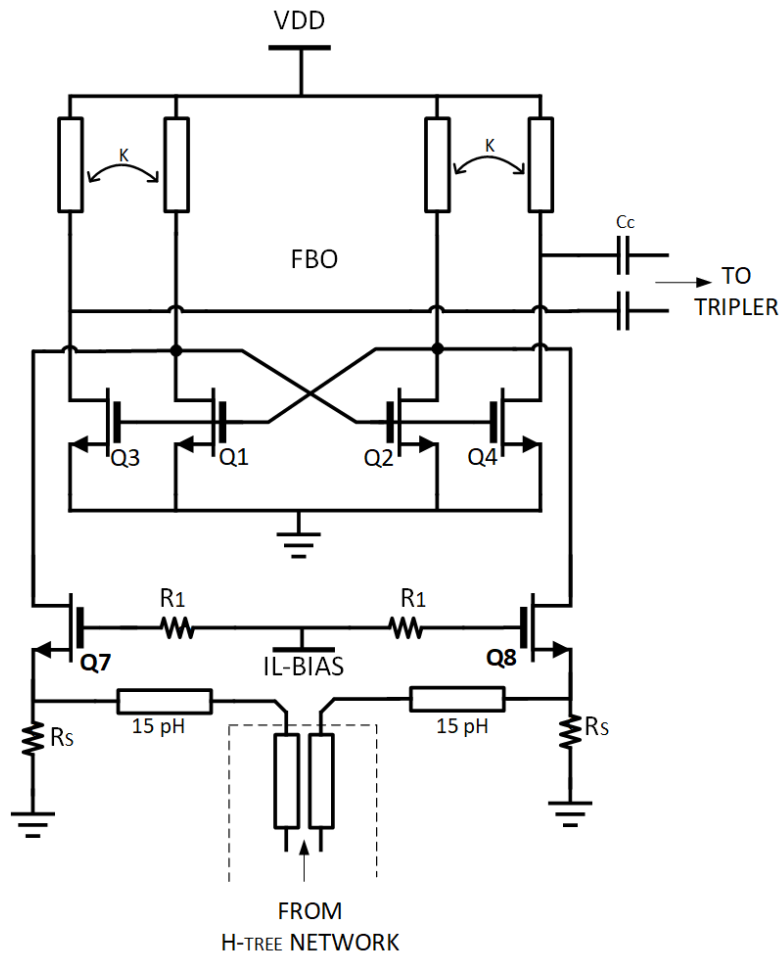
Fig. 5.8. Injection locking circuit added to FBO

5.3   Thirty-two Injection Locked Oscillator Network

The active die is composed of 32 injection locked oscillators as shown in Fig. 5.9. A central oscillator drives the H-tree and generates a 140 GHz reference signal for all the local oscillators. The central oscillator generates 8 dBm of output power. Including all the inter-connecting losses, each local FBO-cell receives a -9 dBm reference signal for injection locking through the H-tree network. An RF input pad is implemented on the die to provide an external route for the central oscillator to lock it to an off-chip source. In this case, the central oscillator will function as an amplifier. FBO-cells are grouped into three power domains as shown in Fig. 5.9. This power up mechanism is implemented to verify the power combining performance of the integrated transmitter. Power domain #1 powers up 4 FBO-cells to form a 2×2 array section. Power domain #2 powers up half of the chip which would result a 2×4 array. Finally, power domain #3 powers up the entire chip.
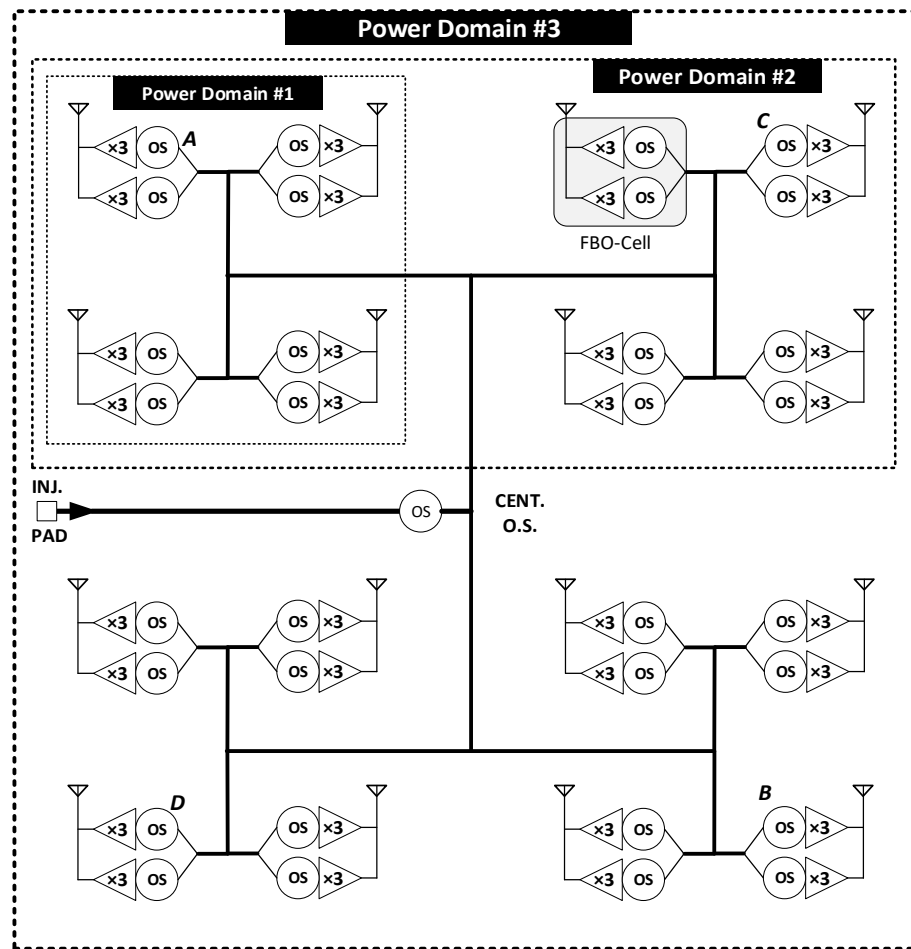
Fig. 5.9. Block diagram of the transmitter chip where 32 injection locked oscillators driving the 4×4 DRAAM
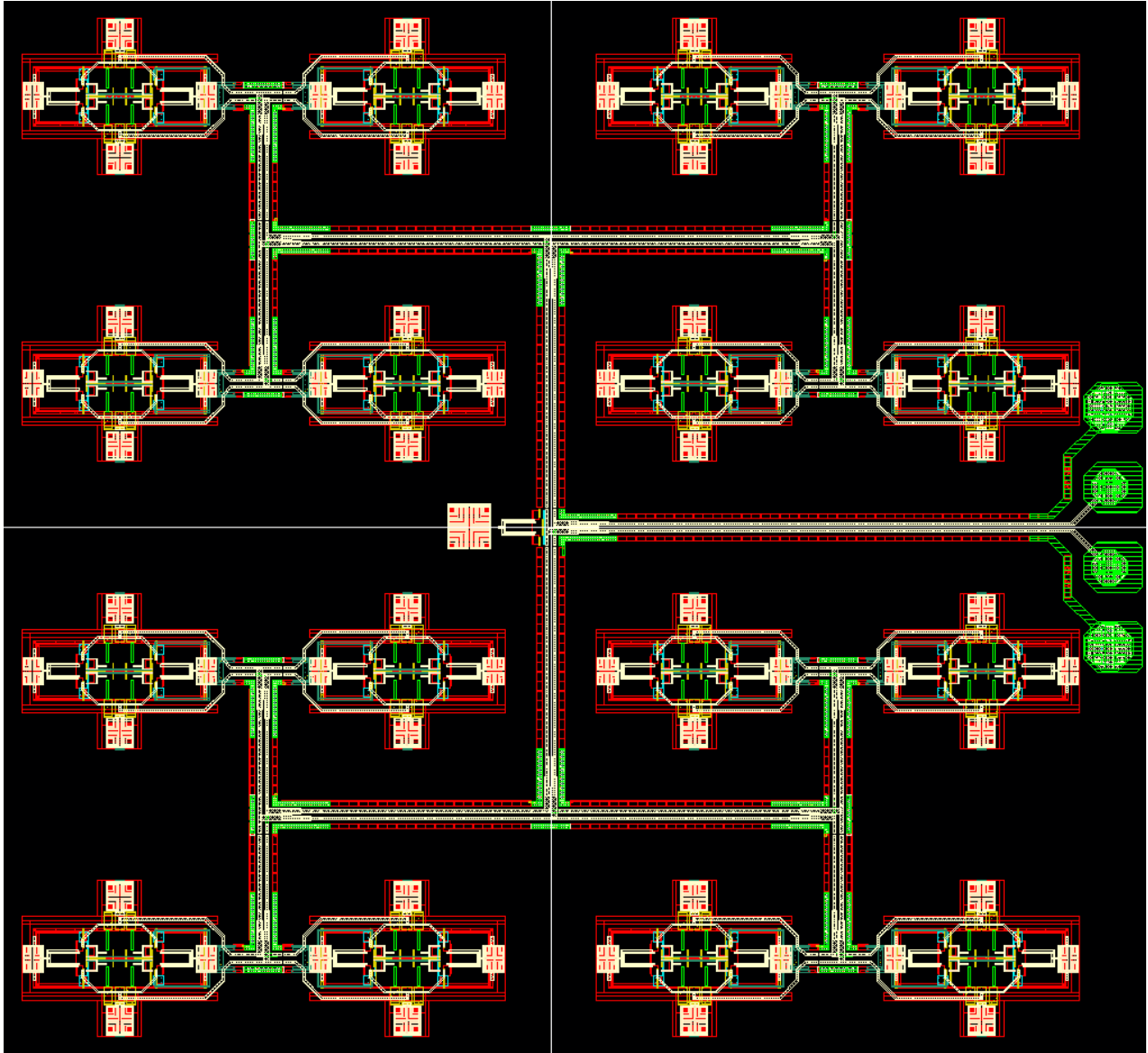
Fig. 5.10. Layout of the transmitter chip

Fig. 5.10 shows the top chip layout. A post layout transient simulation was performed to verify the injection locking network performance. Fig. 5.11 shows the voltage waveforms from the output of four oscillators placed at the farthest corners of the chip. These four oscillators are indicated as *A*, *B*, *C* and *D* on the circuit shown in Fig. 5.9. The output waveforms of these oscillators will be in-phase after 0.9 ns from start up.

Chip draws 161 mA of current from a 1.1 V supply, when power domain #1 is turned on. The current consumption increases to 305 mA in power domain #2 mode and when half of the chip

is powered up. The full 4×4 transmitter array when powered up (power domain #3), consumes 709 mW DC power from a 1.2 V supply. The central oscillator is turned on in all three power domains. A consistent increase in the power consumption when stepping through the three power domains, is an effective indicator of the chip functionality.
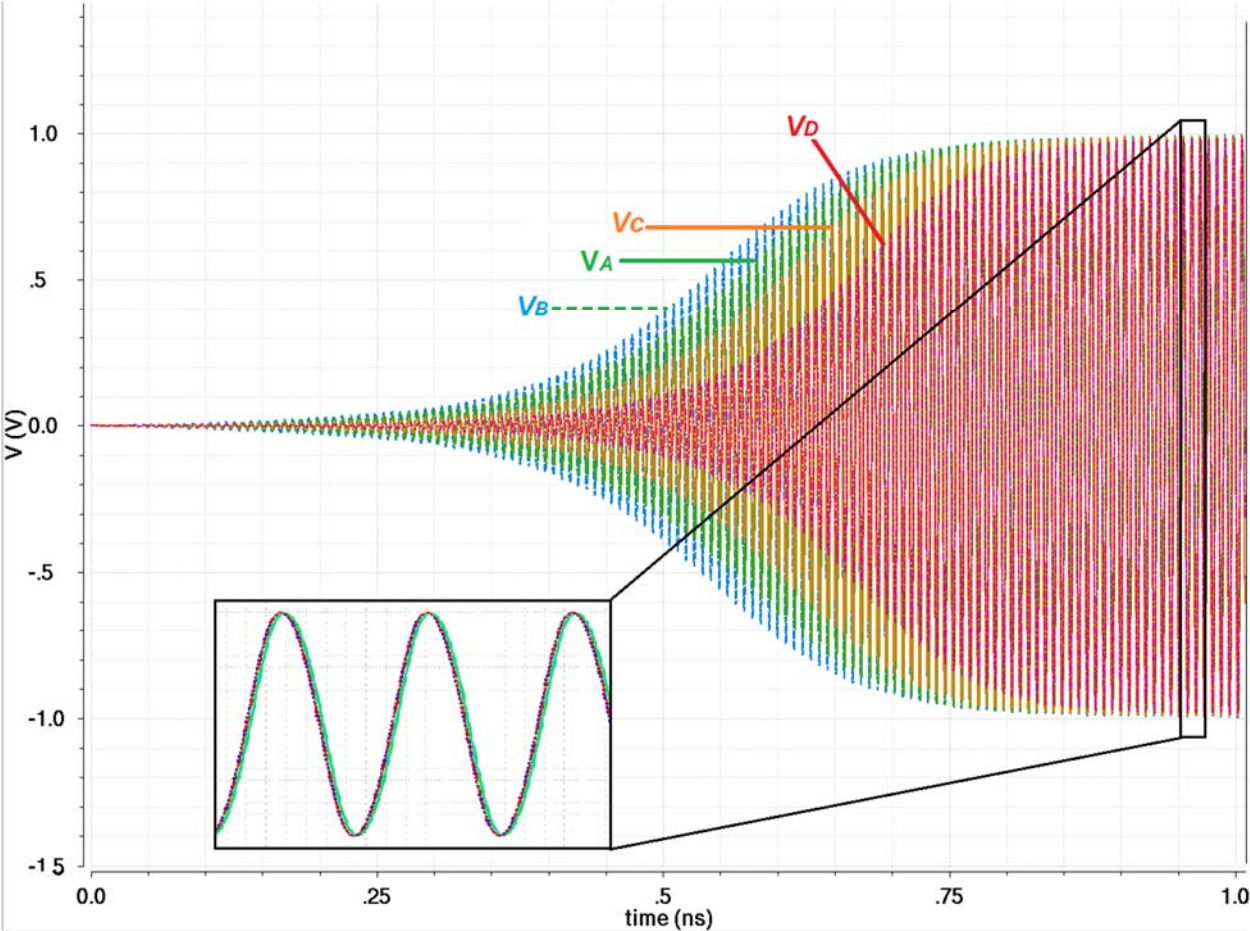
Fig. 5.11. Output waveforms of four injection locked oscillators

CHAPTER 6 Fabrication and Test

In this chapter the DRAAM fabrication process is explained in detail. DRAAM is made of HRS with features on both sides. The top side has cylindrical DRAs and the bottom side has a cavity to accommodate the MMIC. DRAs heights are 120 μm and the cavity depth can be made in the range of 100 to 200 μm to securely pocket the MMIC. The Bosch DRIE is an ideal fabrication process for creating deep etching, steep-sided holes and trenches in wafers and substrates.

6.1 DRAAM Fabrication

DRAAM is fabricated through two phases of the Bosch DRIE process. The first phase forms DRAs on the top side of a silicon wafer and the second one etches the cavity on the bottom side. A 4″ HRS wafer with resistance of 20 K to 40 K Ω/cm and 300 μm thickness is used for fabrication. The Si wafer was Intrinsic/FZ type, double side polished, and had (111) crystal orientation.

In DRIE, the chemical agent removes the upper-most layer of the substrate in areas that are not protected by photoresist (PR). Therefore, the surface needs to be patterned prior to DRIE. I used an exposure system and a proximity lithography approach to produce an image on the wafer using a photomask. The resolution in proximity lithography is approximately the square root of the product of the wavelength and the gap distance. For an i-line source (λ = 365 nm) and a gap less than 10 μm this resolution limit is approximately 2 μm. Since the DRA diameter is 180 μm, resolution of 2 μm is tolerable and it is verified by simulation. I used AZ P4620 series PR for this work. The AZ P4000 series PR provide capabilities in applications requiring film thicknesses up to 60 μm. The recipe that is followed for lithography is described below:

1. **Priming**: The wafer is placed in an HMDS (hexamethyldisilazane) oven. HMDS promotes adhesion of photoresist to wafer.

2. **Spin Coating**: Spin coating is done in two steps. The first step is dispensing or spreading the PR. This is done through spinning the wafer for 5 seconds at 500 RPM and 100 RPM/s ramping profile. The second step is the actual Spin-Coating. In order to obtain a 12 μm thick PR coat on the wafer, the wafer was spun for 30 seconds at 2000 RPM with 200

RPM/s ramping profile. This spin coating recipe results in a consistent PR coating with 12μm thickness.

3. **Soft-Baking**: The wafer is placed on the hot-plate at 115 ºC for 3 minutes. Based on the AZ4620 PR datasheet, this is sufficient time to reduce the solvent concentration in the PR to less than 4% when PR thickness is 12 μm.

4. **Rehydration**: The PR coated wafer is left for 2 hours at room temperature to rehydrate through the clean room air circulation. This step is essential for the PR coat to regain the amount of water it has lost during the soft-baking process. This is a very important step, which would result in a reasonable development rate in approximately 4 minutes.

5. **Exposure**: The MA6-SUSS mask aligner is used for UV exposure. The proximity setting was set to 6 μm and time of exposure to 29.5 sec. The exposure time was calculated based on the exposure energy at 730 mJ/cm^2.

6. **Development**: The AZ 400K series developer, as instructed on the PR datasheet, is used to develop the exposed PR. UV-exposed wafer is poured in a petri dish filled with AZ 400K solvent and shaken gently for 3 minutes. Fig. 6.1 shows the lithography result under the microscope.
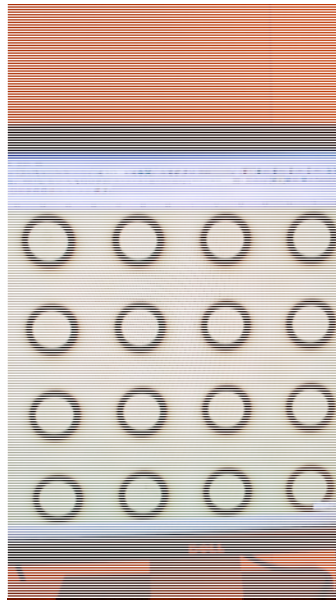
Fig. 6.1. Result of lithography on top side of the wafer where the PR is patterned with the shape of DRAs prior to DRIE

After successful lithography, the DRIE phase on top side of the wafer starts. This side of the wafer needs to be etched 120 μm to create cylindrical DRA features. If all 120 μm is etched in a single run, the wafer will over heat during the process which will burn out the PR coat and will ruin the sample. Fig. 6.2 shows this effect.
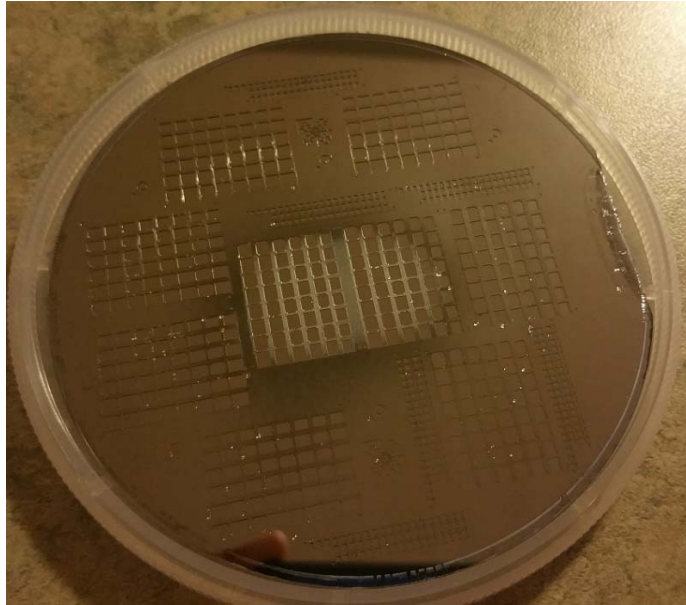
Fig. 6.2. Silicon wafer is burned at the centre due to a long DRIE run

I divided the process into to three shorter runs. At each run, the wafer is etched 40 μm and then placed in the room to cool down to room temperature. After successfully creating top side DRA features on Si wafer, the bottom side needs to be etched for 150 μm to form the MMIC-housing cavity. This side also needs to be patterned with PR through lithography prior to etching. Therefore, the wafer is HMDS primed and spin coated with the same AZ4620 PR using the same recipe as described for the top side lithography except in the soft-baking phase. The difference is that the baking temperature is reduced by 5 degrees to 110 but continued for 6 minutes longer for soft-baking. This was due to the non-uniformed surface on the other side of the wafer and use of a hot plate for baking which would prevent the heat to propagate evenly everywhere on the wafer in a shorter time. Exposure and development steps were performed similarly to the top side. One extra step for this side was mask alignment before the exposure. The top and bottom side masks should include a set of complimentary alignment marks so that the features built on the top and bottom side of the wafer become aligned with each other. High precision features that are built on

top of the wafer in the first DRIE phase, are used as the reference for alignment of the bottom side mask when positioned on the wafer for UV-exposure.

DRIE process on the bottom side starts after the bottom side lithography. Since our wafer thickness is 300 μm, the bottom side needs to be etched for 150 μm in order to leave 30 μm of silicon as the carrier layer for DRAs shown in Fig. 6.3. Similar to the top side etching process, the 150 μm etching is done through 4 shorter run intervals of 37.5 μm etching and cooling off periods.
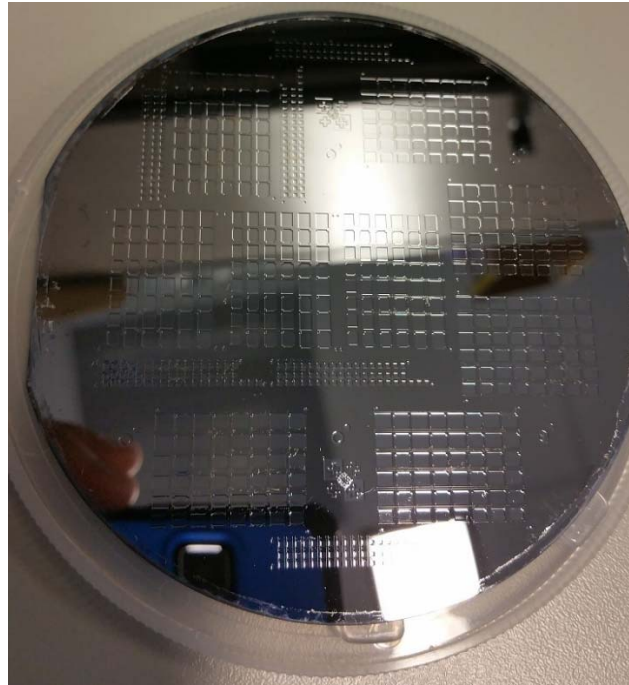
Fig. 6.3. Si wafer after successfully finishing the DRIE on the bottom side

The final step of the DRAAM fabrication is laser cutting the outer boundary of the array module from the wafer. Due to the irregular shape of the DRAAM boundary, use of a dicing saw machine was not an option. However, a side effect of using a laser for cutting, is that it leaves debris on the surface around the cutting line. These melted debris and the sample are fused during the cut and are not removable by using a solvent or Plasma Asher. Fig. 6.4 shows a sample with the cut debris indicated as white spots on the surface. In order to mitigate this problem, both sides of the wafer are coated with a thin layer of PR for protection, prior to laser cut. This thin protective PR layer is then removed with solvent after the cut. Samples that are cut using this approach carry a significantly lesser amount of cutting debris around the perimeter. In summary, the two phases

of Bosch DRIE etching process, and one phase of laser micro machining to build a DRRAM are depicted in Fig. 6.5.
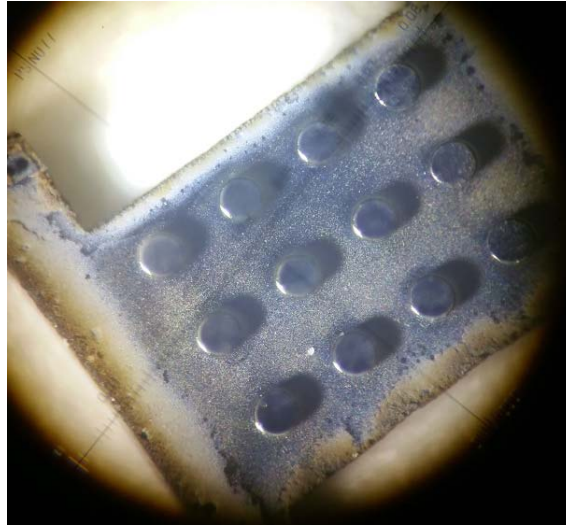
Fig. 6.4. laser cut leaves debris around the cut line
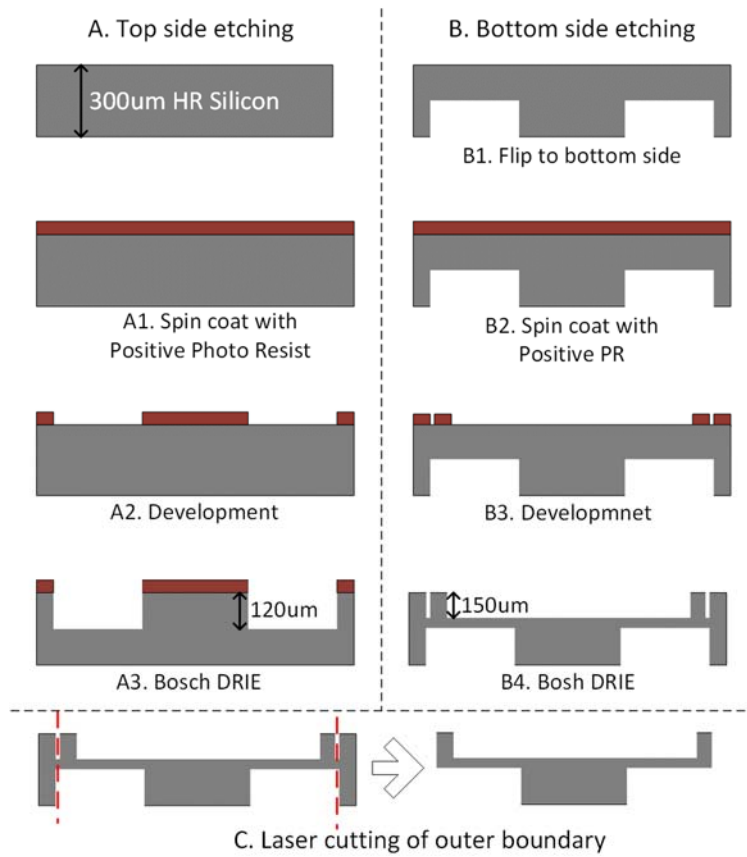
Fig. 6.5. DRAAM fabrication process through two DRIE phases and one last phase of laser cutting
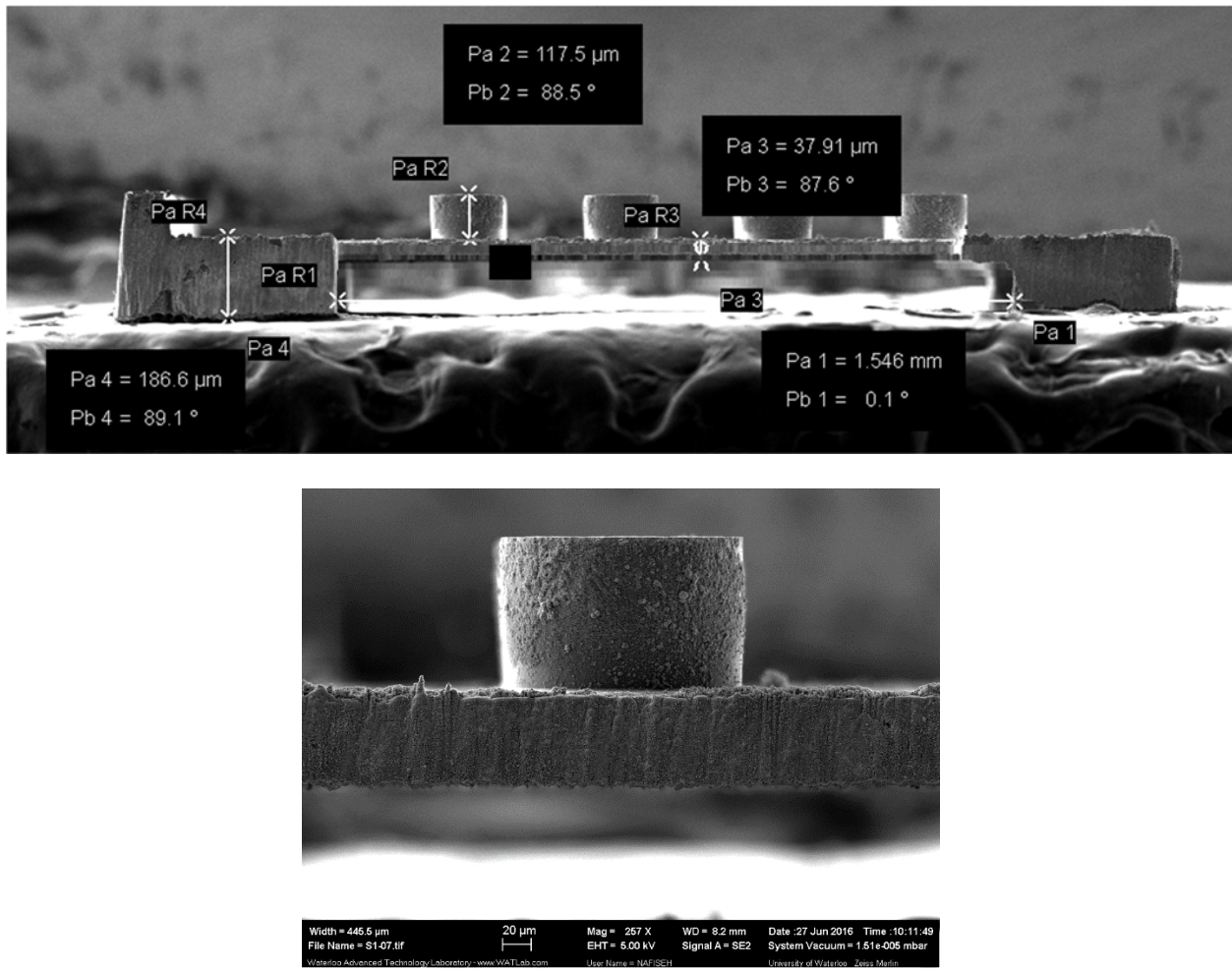
Fig. 6.6. SEM photo of a prototyped sample. Dimensions shows better than 3 µm fabrication accuracy

6.2 Assembly Methodology

The MMIC silicon dies that come from the foundry are already diced and packaged in a gel pack. All dies have the same circuit and design. However almost none of the dies are symmetrically cut around the circuit horizontal and vertical centre lines. In other words, width and length of the dies do not match with each other and different dies have a different square area. Therefore, a single cavity dimension would not work for different dies. In order to address this problem, a range of different size cavities having different width and length in 5 µm step size are drawn on the DRAAM bottom mask and fabricated on the HRS wafer. After fabrication and creating of features on the bottom side of the DRAAM wafer, the dimensions of an active die are measured and then placed into a matching cavity on the DRAMM wafer which has the dimensions that tightly fit the

70

die. Fig. 6.7 shows an example of a cavity pocketing a MMIC. A cavity, numbered as '105' in this example is the match found for a random die. Now that the right size sample is found, we proceed to cut out the DRAAM from the whole wafer as explained in Section 6.1.
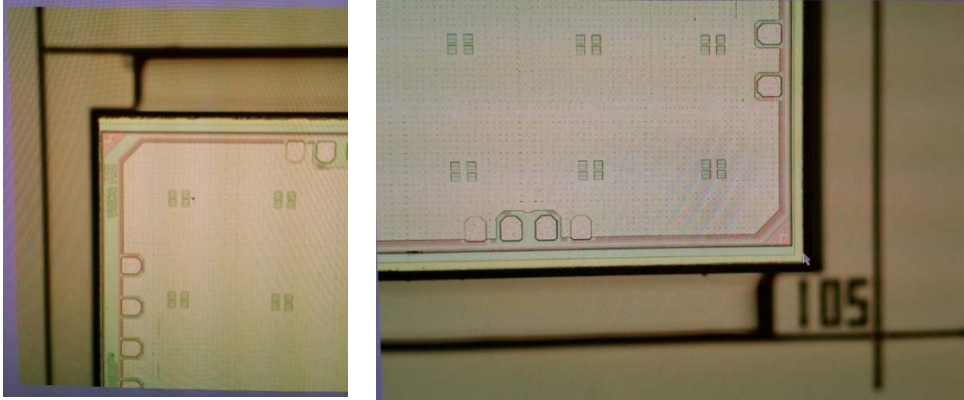
Fig. 6.7. A cavity matched to the chip in dimensions.

The MMIC active die is positioned and glued in the middle of a ceramic substrate which has gold plated pads suitable for wire-bonding. DC pads of the MMIC are then wire-bonded to the substrate pads. DRAAM is placed on top of the MMIC, so that the MMIC die snugs inside the cavity underneath the DRAAM. The maximum error observed and measured in this proposed integration technique is 2 μm. Fig. 6.8 shows simulation results with a maximum loss of 1.5 dB in broad side gain in the case of 10 μm misalignment of all 64 antenna apertures on top of MMIC with the DRAAM. Fig. 6.9 shows a fully assembled sample.
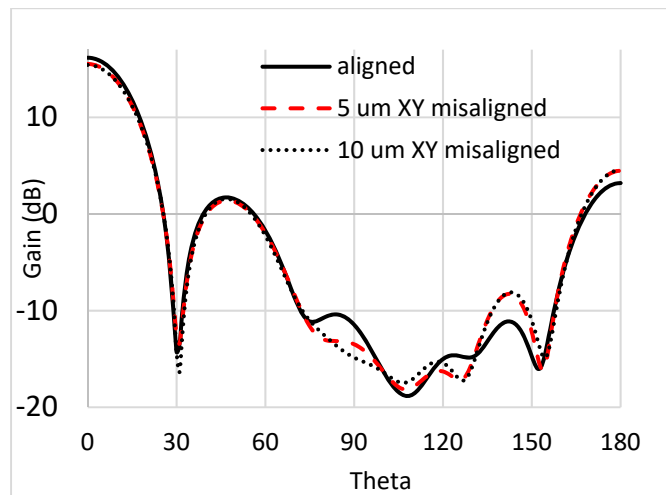
Fig. 6.8. Analysis of the sensitivity of the antenna gain pattern to DRAAM-MMIC assembly misalignment

71
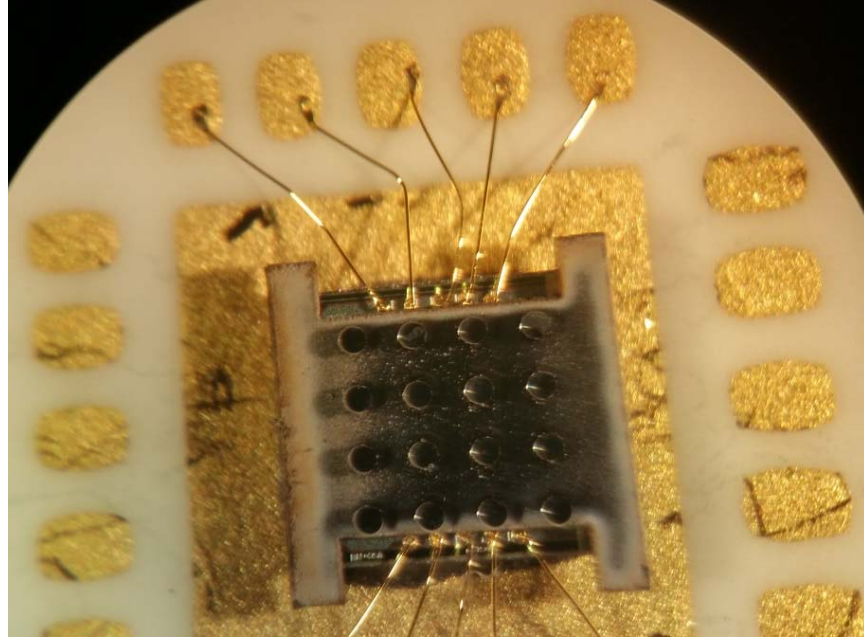
Fig. 6.9. Wirebonded active die with the assembled DRAAM

Wire-bonding the die and antenna assembly is done for the purpose of a feasibility study and demonstration of the proposed integration methodology. For performance test and verification, a sub-THz probing and radiation pattern measurement setup is used. Fig. 6.10 shows the MMIC-DRAAM under test. Fig. 6.11 shows the measurement system.
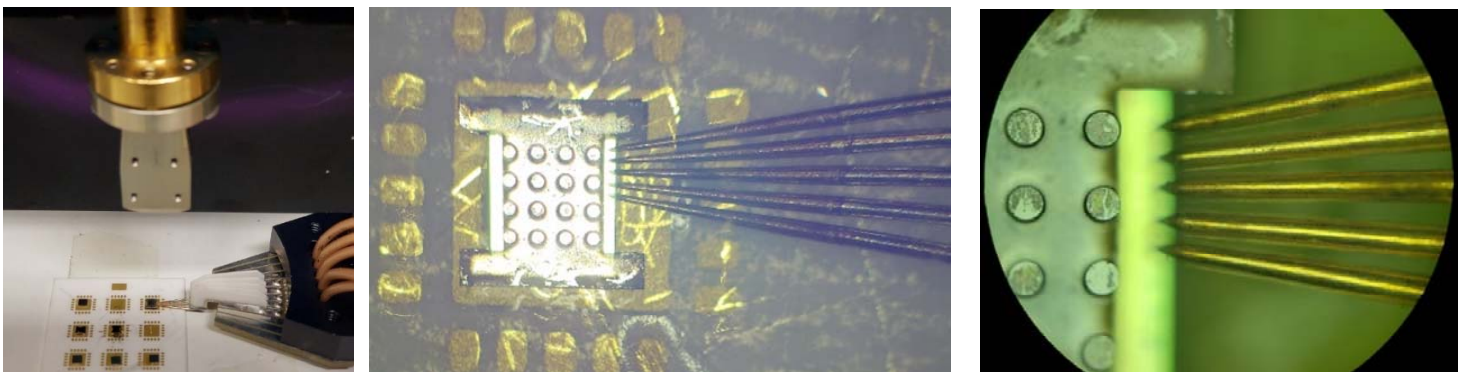
Fig. 6.10. Design under test: DC probing and power up the transmitter
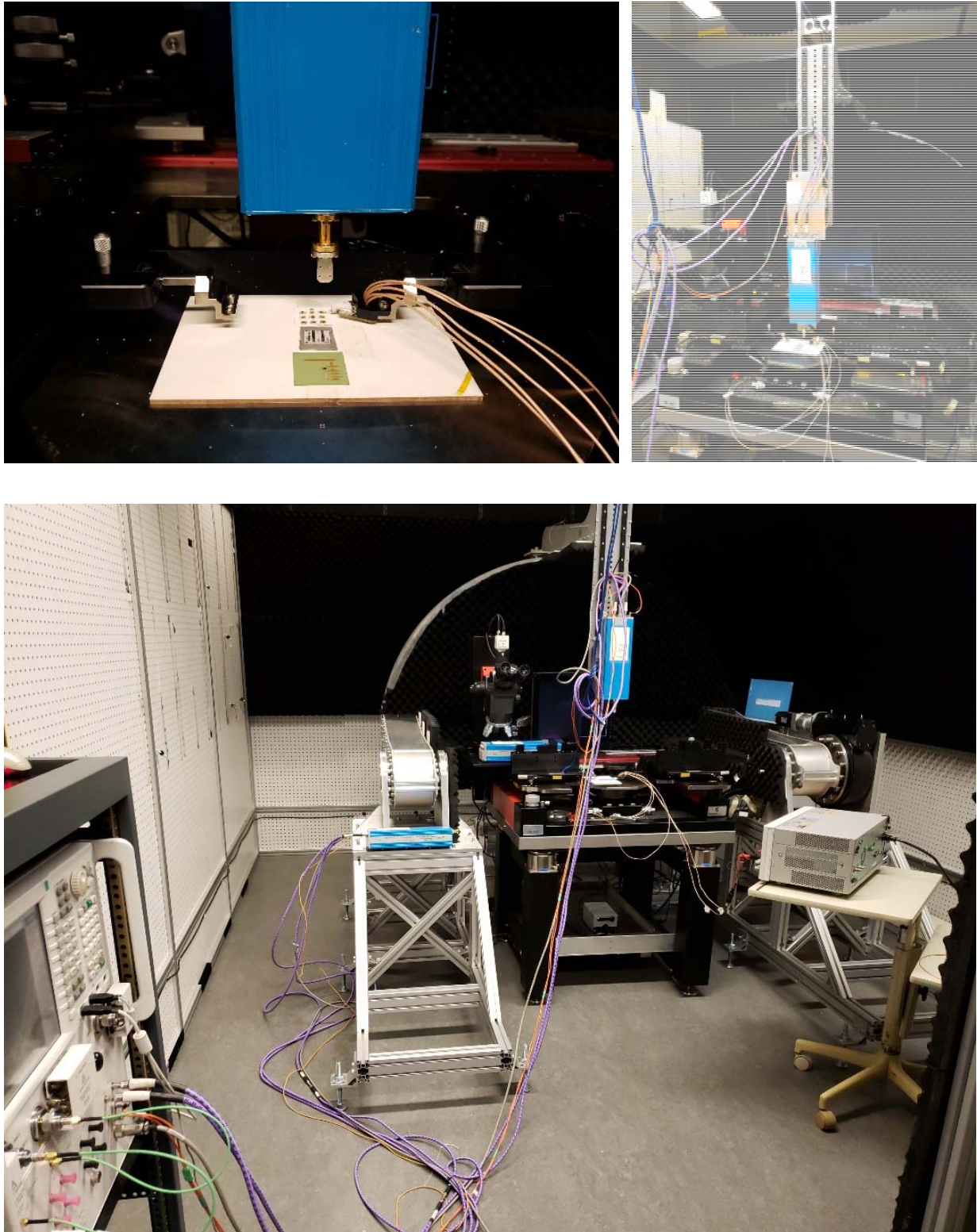
Fig. 6.11. sub-THz probing station equipped with antenna radiation measurement system

6.3   Radiation Pattern Measurement

Two 300-500 GHz OML harmonic mixer modules connected to Keysight-Technologies PNAX used in the measurement. The PNAX was configured to sweep from 410 to 411 GHz with IF bandwidth of 1 KHz and 16001 number of points. The OML that was connected to the port 2 of The PNAX was placed on the ground and covered with absorbers. The other OML, connoted to the port 1 of PNAX, was placed on the swing arm above the MMIC-DRAAM under the test. The S21 readings then resulted in the normalized radiation powered of the test chip when the theta and phi were swept. Three sets of measurements were performed. In the first run, MMIC was power up in the quarter mode (power domain #1) where just a 2×2 array of FBO-cells was powered on. In the second test, half the transmitters were powered up (power domain #2), resulting in a 2×4 array configuration. And in the last test, the full chip was powered up to create a 4×4 array transmitter. Radiation pattern of both the elevation and azimuth planes at 410.1 GHz are shown for all the three sets of measurements in Fig. 6.12, Fig. 6.13 and Fig. 6.14, and compared with their corresponding simulation result.
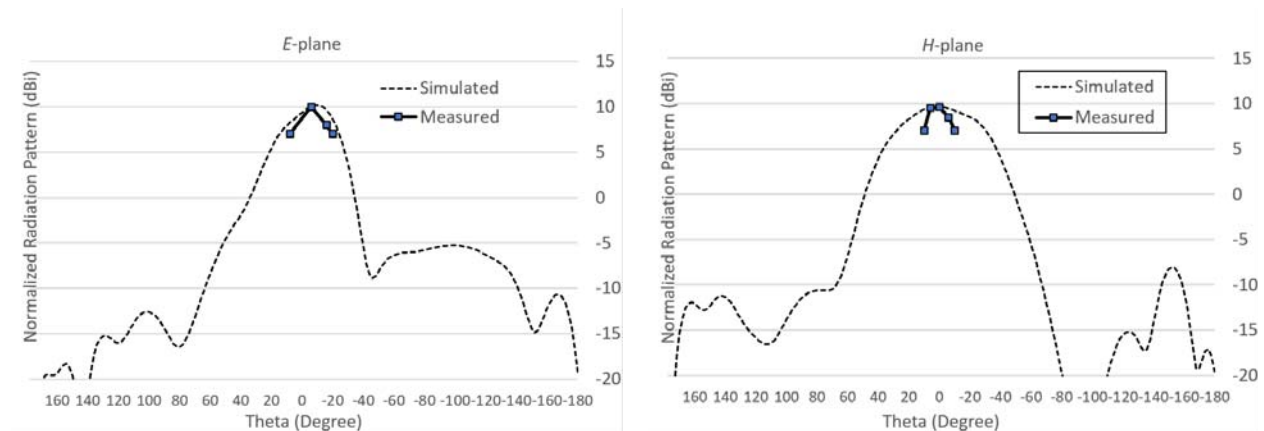
Fig. 6.12. Quarter array radiation pattern. The 0.41 THz transmitter in 2×2 configuration
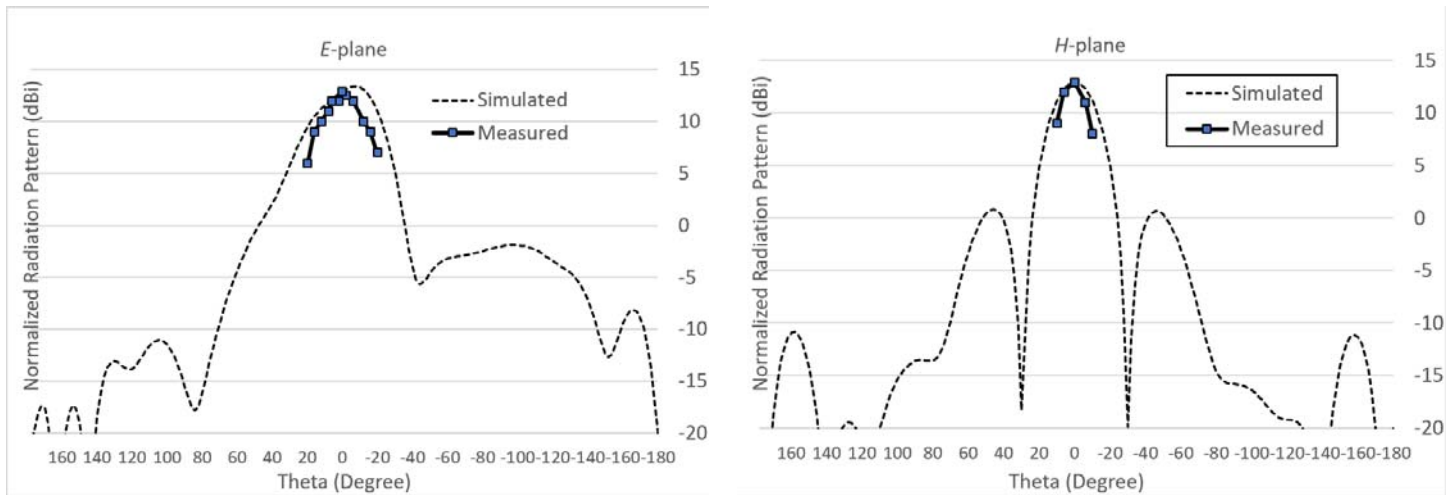
Fig. 6.13. Half array radiation pattern. The 0.41 THz transmitter in 2×4 configuration
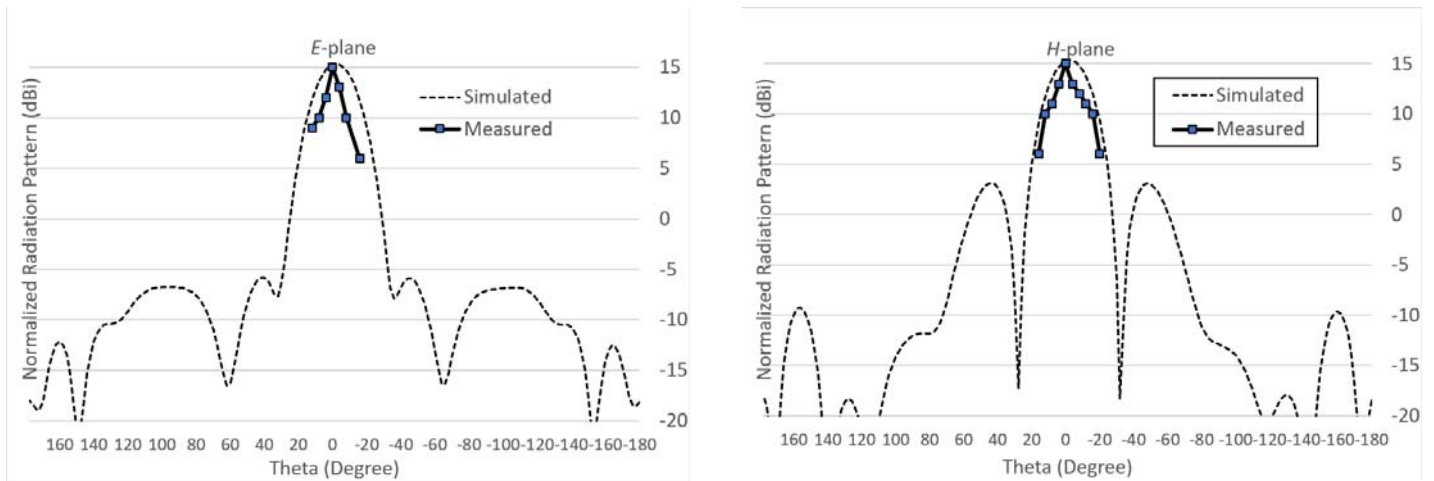
Fig. 6.14. Full array radiation pattern. The 0.41 THz transmitter in the full 4×4 configuration

The maximum received power between quarter, half and full array configuration were compared to verify the power combining functionality of the transmitter. S21 of half-array at peak power (theta = 0º and phi = 0º) showed 4.1 dB less S21 than the full-array. S21 of the quarter array at peak power was 3.3 dB less than half-array.

The 4×4 transmitter which is composed of 32 injection locked oscillators and drives a 4×4 DRAAM achieves 22.8 dBm EIRP.

75

CHAPTER 7 Conclusions and Future Work

With the fact that fully on-chip antenna suffers from low radiation efficiency mainly due to substrate losses, this research was focused to propose new solutions for integration of sub-THz MMICs with off-chip antennas. The main objective was to minimize the loss of sub-THz signal transmission from MMIC to the off-chip antennas. Therefore, I started by investigating an off-chip High Resistivity Silicon-Dielectric Resonator Antenna to achieve one of the most efficient radiating elements for sub-THz applications. Key methods developed for efficient integration of this type of antennas, DRAs, with MMIC are as follows:

1. Using the top metal layer of the MMIC for aperture coupling to the DRA.

2. Combining the antenna feeding structure with a fundamental circuit component, inductor, in the MMIC.

3. Utilizing the antenna also as a power combiner component in the front-end circuit.

4. Differential excitation of the antenna.

5. Structuring the antenna array module, DRAAM, which featured self-aligning design for low-loss and low-cost integration with MMIC.

All the above solutions were successfully implemented and verified in the form of a 420 GHz transmitter MMIC with a 4×4 HRS-DRAAM. The MMIC was composed of 32 injection locked 140 GHz buffer-feedback oscillators followed by triplers. Each tripler generated -8 dBm output power at 420 GHz in simulation. Every two tripler drive and transform their output power into a single DRA in the DRAAM through aperture coupling. Differential excitation was provided to directly deliver the differential output signal of the tripler to the antenna, eliminating the additional loss of an extra Ballun. Therefore, power combining of the two triplers inside a DRA, were achieved through two differentially driven apertures.

In order to realize the DRAAM 3-dimensional structural features, an elaborate micro fabrication recipe for prototyping the samples was proposed. The realized accuracy of 3 μm for

the features on the built DRAAM samples, and less than 10 µm for alignment, confirmed our proposed antenna-MMIC integration technology.

Every tripler showed a simulated output power of -8 dBm using the rigorous S-parameter model of the DRAAM. Therefore, +7 dBm combined output power from all the 32 signal sources with 15.8 dB broadside gain for the DRAAM, translates in to 22.8 dBm EIRP for the 4×4 transmitter.

The transmitter when emitting at full power in 4×4 configuration consumes 709 mW of DC power. Considering, +7 dBm combined output power from all the 32 signal sources and the DRAAM simulated efficiency of 0.85 in simulation, the DC to radiated power efficiency of the 4×4 transmitter is estimated as 0.7 %.

Radiation pattern measurement showed a consistent correlation with the design and array factor. A steady increase of approximately 3 dB in the radiation power when doubling the size of the array, confirmed the spatial power combining functionality of the transmitter. This result was verified twice when switching the transmitter from a 2×2 configuration to 2×4 and then from a 2×4 to a full 4×4 configuration,

We showed how the ground metal layer between the MMIC and the DRAAM for aperture coupling, will not affect the performance of passive components. We proposed a new up-side down arrangement for implementing the transmission line utilizing the imposed ground layer as the signal return path. The high performance of the passive components implemented in this research, for example the differential CPWG, the MTL, and the 140 GHz Transformer, verified that our proposed integration solution will not trade off the performance of the MMIC passive components.

An important achievement of this research was to validate the feasibility of the proposed techniques for off-chip antenna integration at sub-THz frequencies.

7.1 Future Work

In order to improve the performance of the proposed integration methodology, the loss associated with every component in the signal path needs to be measured separately. In this research I measured the output of a stand-alone 140 GHz oscillator. However, I was not able to measure the output power of the tripler. As the tripler was directly connected to the antenna feed, I needed to rely on the measurement of the absolute radiated power from the antenna to calculate the performance of the tripler. Furthermore, probing the output signal of the tripler at 420 GHz would require a Y-band (325-500GHz) probe and a special probe station system which was not easily available at the time of this research. In order to measure the absolute radiated power at 420 GHz, I installed the VDI power meter (from Virginia Diodes) on the swing arm above the chip under the test. However, the power readings from this instrument were not consistent. I speculated that the temperature of the die due to its large current consumption, at 590 mA was affecting my measurement. I attempted to power cycle the chip with precise timing through software to mitigate the problem. However, later I also observed that the VDI device was not calibrated and not showing a correct value even from a source with a known power which was the PNAX in my test. Since the VDI calibration process had to be performed by its manufacturer this part of the measurement is planned to be completed in the future.

As the efficiency of the antenna needs to be measured, I designed and implemented a passive test chip representing the MMIC as shown in Fig. 7.1. This passive die has a single ended input and a 50Ω transmission line corporate feed to excite a 2×4 DRAAM through aperture coupling. In order to exclude the loss of the feed network from the antenna efficiency, a separate transmission line with the same characteristics of the antenna feed network, implemented on the same die, as shown in Fig. 7.1. This measurement also required a Y-band (325-500GHz) probe and a custom-built positioner to connect an off-chip 420 GHz source to the die. In future, I am planning to set up this probe and the proper positioner system to complete this measurement.

Microstrip line for de-embedding the feed circuit
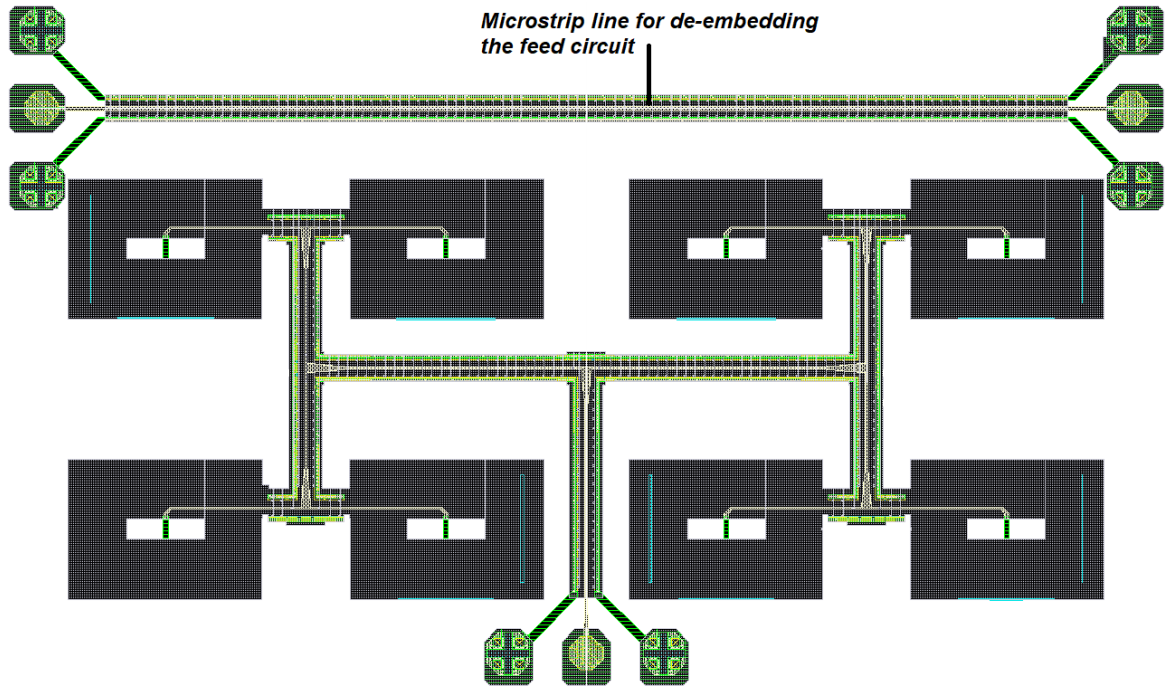
Fig. 7.1. MMIC Test chip. A single-ended corporate input feeds a 2×4 DRAAM

The DRAAM needs to be physically attached to the die. One idea is to coat the top of the MMIC die with a low-loss material like Benzocyclobutene (BCB) and place the DRAAM in position on top of the MMIC and then cure the BCB. I am expecting that this approach would bond the two substrates together. The effect of adding this BCB layer between the MMIC and DRAAM needs to be investigated and studied in future.

Most practical applications of a THz device would require radiated power in the range of 50mW [1][2][3]. The circuit topology proposed in this research featured an input pad for injection locking the central oscillator, and as a result the entire 32 triplers to an output reference 140 GHz signal. This scheme opens up the path to scale up the 4×4 transmitter to a larger size array using multiple dies and to achieve higher radiated power.

References

[1] R. Al Hadi, H. Sherry, J. Grzyb, Y. Zhao, W. Forster, H. M. Keller, A. Cathelin, A. Kaiser and U. R. Pfeiffer, "A 1 k-pixel video camera for 0.7–1.1 terahertz imaging applications in 65-nm CMOS," *IEEE J. Solid-State Circuits,* vol. 47, no. 12, p. 2999–3012, 2012.

[2] T. Globus and e. al., "Sub-terahertz vibrational spectroscopy for microRNA based diagnostic of ovarian cancer," *Convergent Sci. Phys. Oncol.,* vol. 2, no. 4, p. 045001, Oct. 2016.

[3] M. M. Assefzadeh and e. al., "Terahertz trace gas spectroscopy based on a fully-electronic frequency-comb radiating array in silicon," in *Proc. CLEO, Sci. Innov*, Washington, 2016.

[4] C. Wang and R. Han, "Rapid and energy-efficient molecular sensing using dual mm-Wave combs in 65 nm CMOS: A 220-to-320 GHz spectrometer with 5.2 mW radiated power and 14.6-to-19.5 dB noise figure," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. papers*, San Francisco, 2017.

[5] J. C. Chen and S. Kaushik, "Terahertz interferometer that senses vibrations behind barriers," *IEEE Photon. Technol. Lett.,* vol. 19, no. 7, p. 486–488, 2007.

[6] A. Blain, R. J. Smail, J. Ivison, P. Kneib and D. Frayer, "Submillimetre galaxies," *Phys. Rep. 369,* p. 111–176, 2002.

[7] T. Phillips and J. Keene, "Submillimeter astronomy," *Proc. IEEE 80,* p. 1662–1678, 1992.

[8] J.-D. Park, S. Kang and A. Niknejad, "A 0.38 THz Fully Integrated Transceiver Utilizing a Quadrature Push-Push Harmonic Circuitry in SiGe BiCMOS," *Journal of Solid-State Circuits,* vol. 47, no. 10, pp. 2344 - 2354, 2012.

[9] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen and P. Heydari, "A 210GHz fully integrated differential transceiver with fundamental-frequency VCO in 32nm SOI CMOS," 2013.

[10] J.-D. Park, S. Kang, S. Thyagarajan, E. Alon and A. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," in *VLSI Circuits (VLSIC)*, 2012.

[11] K. Sengupta and A. Hajimiri, "A 0.28 THz Power-Generation and Beam-Steering Array in CMOS Based on Distributed Active Radiators," *Solid-State Circuits,* vol. 47, no. 12, 2012.

[12] W. Shin, B.-H. Ku, O. Inac, Y.-C. Ou and G. Rebeiz, "A 108–114 GHz 4x4 Wafer-Scale Phased Array Transmitter With High-Efficiency On-Chip Antennas," *Journal of Solid-State Circuits,* vol. 48, no. 9, pp. 2041- 2055 , 2013.

[13] U. Pfeiffer, J. Grzyb, D. Liu, B. Gaucher, T. Beukema, B. Floyd and S. Reynolds, "A 60GHz radio chipset fully-integrated in a low-cost packaging technology," in *Electronic Components and Technology Conference*, 2006.

[14] Y. Tsutsumi, M. Nishio, S. Sekine, H. Shoki and T. Morooka, "A triangular loop antenna mounted adjacent to a lossy Si substrate for millimeter-wave wireless PAN," in *Antennas and Propagation Society International Symposium*, 2007.

[15] K. Schmalz, R. Wang, J. Borngraber, W. Debski, W. Winkler and C. Meliani, "245 GHz SiGe transmitter with integrated antenna and external PLL," in *2013 IEEE MTT-S International Microwave Symposium Digest (IMS)*, 2013.

[16] S. Shopov, A. Balteanu and S. Voinigescu, "A 19 dBm, 15 Gbaud, 9 bit SOI CMOS Power-DAC Cell for High-Order QAM W-Band Transmitters," *Solid-State Circuits,* vol. 49, no. 7, pp. 1653-1664, 2014.

[17] M. Elkhouly, Y. Mao, C. Meliani, J. Scheytt and F. Ellinger, "A G -Band Four-Element Butler Matrix in 0.13 µm SiGe BiCMOS Technology," *IEEE Journal of Solid-State Circuits,* vol. 49, no. 9, pp. 1916- 1926, 2014 .

[18] M. Elkhouly, S. Glisic, C. Meliani, F. Ellinger and J. Scheytt, "220 - 250-GHz Phased-Array Circuits in 0.13um SiGe BiCMOS Technology," *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. 8, pp. 3115- 3127, 2013.

[19] H. Jalili and O. Momeni, "A 318-to-370 GHz standing-wave 2D phased array in 0.13 µm BiCMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech.*, San Francisco, 2017.

[20] Y. Tousi and E. Afshari, "A high-power and scalable 2-D phased array for terahertz CMOS integrated systems," *IEEE J. Solid-State Circuits,* vol. 50, no. 2, p. 597–609, 2015.

[21] Y. Yang, O. D. Gurbuz and G. M. Rebeiz, "An eight-element 370–410-GHz phased-array transmitter in 45-nm CMOS SOI with peak EIRP of 8–8.5 dBm," *IEEE Trans. Microw. Theory Techn.,* vol. 64, no. 12, p. 4241–4249, 2016.

[22] S. Mason, "Power gain in feedback amplifier," *Circuit Theory, Transactions of the IRE Professional Group,* Vols. CT-1, no. 2, p. 20–25, June 1954.

[23] U. R. Pfeiffer and e. al., "A 0.53 THz reconfigurable source module with up to 1 mW radiated power for diffuse illumination in terahertz imaging applications," *IEEE J. Solid-State Circuits,* vol. 49, no. 12, p. 2938–2950, 2014.

[24] Y. Zhao and e. al., "A 0.56 THz phase-locked frequency synthesizer in 65 nm CMOS technology," *IEEE J. Solid-State Circuits,* vol. 51, no. 12, p. 3005–3019, 2016.

[25] Y. Zhao and e. al., "A 0.54–0.55 THz 2×4 coherent source array with EIRP of 24.4 dBm in 65 nm CMOS technology," in *IEEE MTT-S Int. Microw Symp. Dig.*, Phoenix, 2015.

[26] P. Hillger, J. Grzyb, S. Malz, B. Heinemann and U. Pfeiffer, "A lensintegrated 430 GHz SiGe HBT source with up to −6.3 dBm radiated," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Honolulu, 2017.

[27] Z. Hu, M. Kaynak and R. Han, "High-power radiation at 1 THz in silicon: A fully scalable array using a multi-functional radiating mesh structure," *IEEE J. Solid-State Circuits,* vol. 53, no. 5, p. 1313–1327, 2018.

[28] K. Guo, A. Standaert and P. Reynaert, "A 525–556-GHz radiating source with a dielectric lens antenna in 28-nm CMOS," *IEEE Trans. THz Sci. Technol.,* vol. 8, no. 3, p. 340–349, 2018.

[29] H. Jalili and M. O., "A standing-wave architecture for scalable and wideband millimeter-wave and terahertz coherent radiator arrays," *IEEE Trans. Microw. Theory Techn,* vol. 66, no. 3, p. 1597–1609, 2018.

[30] B. Ginsburg, S. Ramaswamy, V. Rentala, E. Seok, S. Sankaran and B. Haroun, "A 160 GHz Pulsed Radar Transceiver in 65 nm CMOS," vol. 49, no. 4, pp. 984- 995, 2014.

[31] A. Tang, G. Virbila, D. Murphy, F. Hsiao, Y. Wang, Q. Gu, Z. Xu, Y. Wu, M. Zhu and M.-C. Chang, "A 144GHz 0.76cm-resolution sub-carrier SAR phase radar for 3D imaging in 65nm CMOS," in *Solid-State Circuits Conference (ISSCC)*, 2012.

[32] E. Afshari and O. Momeni, "High power terahertz and millimeterwave oscillator design: A systematic approach," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 3, p. 583–597, March 2011.

[33] B. Razavi and J. Sung, "A 6-GHz 60-mW BiCMOS phase-locked loop," *IEEE J. Solid-State Circuits,* vol. 29, p. 1560–1565, 1994.

[34] D. Huang and e. al., "A 324 GHz CMOS frequency generator using a linear superposition technique," in *ISSCC Dig. Tech. Papers*, 2008.

[35] B. Catli and M. Hella, "Triple-push operation for combined oscillation/division functionality in millimeter-wave frequency synthesizers," *IEEE J. Solid-State Circuits,* vol. 45, p. 1575–1589, 2010.

[36] O. Momeni and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 3, pp. 583 - 597, 2011.

[37] R. Han and E. Afshari, "A high-power broadband passive terahertz frequency doubler in cmos," *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. 3, p. 1150–1160, March 2013.

[38] M. Adnan and E. Afshari, "A 247-to-263.5 GHz VCO with 2.6mW peak output power and 1.14% DC-to-RF efficiency in 65nm bulk CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014.

[39] S. Voinigescu, A. Tomkins, E. Dacquay, P. Chevalier, J. Hasch, A. Chantre and B. Sautreuil, "A Study of SiGe HBT Signal Sources in the 220–330-GHz Range," *IEEE Journal of Solid-State Circuits,* vol. 48, no. 9, pp. 2011 - 2021 , 2013.

[40] O. Momeni and E. Afshari, "A Broadband mm-Wave and Terahertz Traveling-Wave Frequency Multiplier on CMOS," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 12, pp. 2966 - 2976, 2011.

[41] O. Momeni and E. Afshari, "A 220-to-275GHz Traveling-Wave Frequency Doubler with -6.6dBm Power at 244GHz in 65nm CMOS," in *ISSCC*, 2011.

[42] E. Ojefors, B. Heinemann and U. Pfeiffer, "Active 220- and 325-GHz Frequency Multiplier Chains in an SiGe HBT Technology," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, no. 5, pp. 1311 - 1318, 2011.

[43] E. Ojefors, J. Grzyb, Y. Zhao, B. Heinemann, B. Tillack and U. Pfeiffer, "A 820GHz SiGe chipset for terahertz active imaging applications," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2011.

[44] X. Mei and e. al, "First demonstration of amplification at 1 THz using 25-nm InP high electron mobility transistor process," *Electron Device Lett.,* vol. 36, no. 4, p. 327–329, 2015.

[45] D.-H. Kim and J. A. del Alamo, "30-nm InAs PHEMTs with fT=644 GHz and fmax=681 GHz," *IEEE Electron Device Lett.,,* vol. 31, no. 8, p. 806–808, 2010.

[46] D. H. Kim, B. Brar and J. A. del Alamo, "fT =688 GHz and fmax=800 GHz in Lg=40 nm In0.7Ga0.3As MHEMTs with gm_max>2.7 mS/μm," in *319–322*, Washington, 2011.

[47] M. Seo, M. Urteaga, J. Hacker, A. Young, Z. Griffith, V. Jain, R. Pierson, P. Rowell, A. Skalare, A. Peralta, R. Lin, D. Pukala and M. Rodwell, "InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 10, pp. 2203 - 2214 , 2011.

[48] M. Abbasi, R. Kozhuharov, C. Karnfelt, I. Angelov, I. Kallfass, P. Leuther and H. Zirath, "Single-chip frequency multiplier chains for millimeter-wave signal generation," *IEEE Transactions on Microwave Theory and Techniques,* vol. 57, no. 12, pp. 3134- 3142, 2009.

[49] T. Merkle and e. al., "Testbed for phased array communications from 275 to 325 GHz," in *IEEE Compound Semiconductor Integr. Circuit Symp.*, Miami, 2017.

[50] T. Nagatsuma and J. Song, "Present and future of terahertz communications," *IEEE Transaction THz Sci. Technology,* vol. 1, no. 1, p. 256–263, Sep. 2011.

[51] D. Titz, R. Pilard, F. Gianesello, F. Ferrero, C. Luxey, P. Brachat, G. Jacquemod and D. Gloria, "Industrial HTCC Antenna-Module SiP for 60-GHz Applications," *IEEE Antennas and Wireless Propagation Letters,* vol. 11, pp. 576-579, 2012.

[52] D. G. Kam, D. Liu, A. Natarajan, S. Reynolds, H.-C. Chen and B. Floyd, "LTCC Packages With Embedded Phased-Array Antennas for 60 GHz Communications," *IEE Microwave and Wireless Components Letters,* vol. 21, no. 3, pp. 142-144 , 2010.

[53] D. G. Kam, D. Liu, A. Natarajan, S. Reynolds and B. Floyd, "Organic Packages With Embedded Phased-Array Antennas for 60-GHz Wireless Chipsets," *IEEE Transaction on Components, Packaging and Manufacturing Technology,* vol. 1, no. 11, pp. 1806-1814 , 2011.

[54] A. Amadjikpe, A. Vera, D. Choudhury and J. Papapolymerou, "Study of a 60 GHz rectangular patch antenna on a flexible LCP substrate for mobile applications," in *Antennas and Propagation Society International Symposium*, 2008.

[55] S.-J. Huang, Y.-L. Chen, H.-Y. Chu, P.-N. Chen, H.-Y. Chang, C.-Y. Kuo, C. Kao and J. Lee, "A Fully-Integrated 77GHz phase-array radar system with 1TX/4RX frontend and digital beamforming technique," in *VLSI Circuits (VLSIC)*, 2013.

[56] E. Cohen, M. Ruberto, M. Cohen, O. Degani, S. Ravid and D. Ritter, "A CMOS bidirectional 32-element phased-array transceiver at 60GHz with LTCC antenna," in *Radio Frequency Integrated Circuits Symposium (RFIC)*, 2012.

[57] B. Ginsburg, S. Ramaswamy, V. Rentala, E. Seok, S. Sankaran and B. Haroun, "A 160 GHz Pulsed Radar Transceiver in 65 nm CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 49, no. 4, pp. 984-995, 2014.

[58] G. Gentile, V. Jovanovic, M. Pelk, L. Jiang, R. Dekker, P. de Graaf, B. Rejaei, L. de Vreede, L. Nanver and M. Spirito, "Silicon-Filled Rectangular Waveguides and Frequency Scanning Antennas for mm-Wave Integrated Systems," *, IEEE Transactions on Antennas and Propagation,* vol. 61, no. 12, pp. 5893 - 5901, 2013.

[59] N. Ranjkesh, A. Taeb, S. Gigoyan and M. Basha, "Millimeter-Wave Silicon-on-Glass Integrated Tapered Antenna," *Antennas and Wireless Propagation Letters,* vol. 13, pp. 1425 - 1428, 2014.

[60] N. Ranjkesh, A. Taeb, S. Gigoyan, S. Safavi-Naeini and M. A. Basha, "High-gain integrated tapered dielectric antenna for millimeter-wave applications," in *Antennas and Propagation Society International Symposium*, 2014.

[61] A. Abdellatif, M. Basha and S. Safavi-Naeini, "Low-Cost and High-Efficiency Multibeam Antenna for Millimeter-Wave Applications," *Antennas and Wireless Propagation Letters,* vol. 11, pp. 141 - 143 , 2012 .

[62] B. Razavi, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology," *Solid-State Circuits ,* vol. 46, no. 4, pp. 894 - 903, 2011.

[63] S. P. Voinigescu and e. al., "CMOS SOCs at 100 GHz: System architectures, device characterization, and IC design examples," in *ISCAS*, May 2007.

[64] B. Razavi, R. H. Yan and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans. Circuits and Systems—Part I,* p. 750–754, Nov. 1994.

[65] B. Razavi, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 4, 2011.

[66] S. A. Long, M. W. McAllister and L. C. Shen, "The Resonant Cylindrical Dielectric Cavity Antennas," *IEEE Trans. Antennas Propagation.*

[67] R. Kumar Mongia and A. Ittipiboon, "Theoretical and experimental investigations on rectangular dielectric resonator antennas," *IEEE Transactions on Antennas and Propagation,* vol. 45, no. 9, pp. 1348 - 1356, 1997.

[68] A. Petosa, A. Ittipiboon, Y. Antar, D. Roscoe and M. Cuhaci, "Recent Advances in Dielectric Resonator Antenna Technology," *IEEE Antennas and Propagation Magazine,* vol. 40, no. 3, pp. 35-48, 1998.

[69] S. Safavi-Naini and H. Ameri, "Modal analysis of dielectric loaded coaxial probe fed circular waveguide radiator," in *Antennas and Propagation Society International Symposium*, 1991.

[70] A. Petosa, Dielectric Resonator Antenna Handbook, Boston/London: Artech House, 2007.

[71] R. Chair, A. A. Kishk and K. F. Lee, "Wideband Stair-Shaped Dielectric Resonator Antennas," *IET Microwaves, Antennas & Propagation,* vol. 1, no. 2, pp. 299-305, April 2007.

[72] W. Huang and A. A. Kishk, "Compact Wideband Multi-Layer Cylindrical Dielectric Resonator Antenna," *IET Microwave Antenna and Propagation,* vol. 1, no. 5, pp. 998-1005, October 2007.

[73] R. Chair, A. A. Kishk and K. F. Lee, "Low Profile Wideband Embedded Dielectric Resonator Antenna," *IET Microwaves, Antennas & Propagation,* vol. 1, no. 2, pp. 294-298, April 2007.

[74] Z. Fan and Y. M. M. Antar, "Slot-Coupled DR Antenna for Dual-Frequency Operation," *IEEE Trans. Antennas and Propagation,* vol. 45, no. 2, pp. 306-308, Feb. 1997.

[75] H. Y. Yee, "Natural resonant frequencies of microwave dielectric resonators," *IEEE Trans. Microwave Theory Tech.,* Vols. MIT-13, p. 256, 1965.

[76] A. A. Kishk, A. Ittipiboon, Y. M. M. Antar and M. Cuhaci, "Slot excitation of the dielectric disk radiator," *IEEE Trans. Antennas Propagat.,* vol. 43, pp. 198-201, 1995.

[77] P. Bijumon, Y. Antar, A. Freundorfer and M. Sayer, "Dielectric Resonator Antenna on Silicon Substrate for System On-Chip Applications," *IEEE Transactions on Antennas and Propagation,* vol. 56, no. 11, pp. 3404 - 3410, 2008.

[78] B. Kormanyos and G. Rebeiz, "Oscillator design for maximum," *Microwave and Guided Wave Letters,* vol. 4, no. 6, p. 205–207, June 1994.

[79] B. Razavi, R. H. Yan and K. F. Lee, Impact of distributed gate resistance on the performance of MOS devices.

[80] Y. Tousi, O. Momeni and E. Afshari, "A 283-to-296GHz VCO with 0.76mW peak output power in 65nm CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012.

[81] A. Zandieh, A. Abdellatif, A. Taeb and S. Safavi-Naeini, "Low-Cost and High-Efficiency Antenna for Millimeter-Wave Frequency-Scanning Applications," *Antennas and Wireless Propagation Letters, IEEE ,* vol. 12, pp. 116 - 119, 2013.

[82] L. Wu, S. Liao and Q. Xue, "A 312-GHz CMOS injection-locked radiator with chip-and-package distributed antenna," *IEEE J. Solid-State Circuits,* vol. 52, no. 11, p. 2920–2933, 2017.

[83] H. Aghasi, A. Cathelin and E. Afshari, "A 0.92-THz SiGe power radiator based on a nonlinear theory for harmonic generation," *IEEE J. Solid-State Circuits,* vol. 52, no. 2, p. 406–422, 2017.

[84] Y. Zhao and e. al., "A 0.54–0.55 THz 2×4 coherent source array with EIRP of 24.4 dBm in 65 nm CMOS technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Phoenix, 2015.

[85] Y. Zhao, E. Ojefors, K. Aufinger, T. Meister and U. R. Pfeiffer, "A 160-GHz Subharmonic Transmitter and Receiver Chipset in an SiGe HBT Technology," *Microwave Theory and Techniques,* vol. 60, no. 10, pp. 3286- 3299, 2012.

[86] Y. Tousi, O. Momeni and E. Afshari, "A novel CMOS highpower terahertz VCO based on coupled oscillators: Theory and implementation," *IEEE Journal of Solid-State Circuits,* vol. 47, no. 12, p. 3032–3042, Dec 2012.

[87] O. Momeni and E. Afshari, "A broadband mm-wave and terahertz traveling-wave frequency multiplier on cmos," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 12, p. 2966–2976, Dec 2011.