Backplane Circuit Design with Amorphous Silicon Thin-Film Transistors for Flexible Displays

by

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Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.
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Abstract

In recent years, rapid advancement in LED fabrication has enabled the possibility of using GaN μLEDs to be the light media in a display panel. It has superior performance in many aspects when compared with OLED technology, such as high contrast, wide viewing angle, and low power consumption. These advantages have enabled a possibility of using μLED technology to realize flexible displays. Currently, OLEDs need high mobility low-temperature-poly-silicon (LTPS) TFTs to be the backplane driving circuit material because lower mobility TFTs are inadequate to drive OLEDs. However, LTPS TFTs have poor uniformity over a large area due to unpredictable grain sizes and require additional fabrication processes which prevent it from being integrated onto a large-area flexible platform. On the other hand, conventional amorphous silicon (a-Si:H) technology used on LCD panels have an edge in terms of uniformity over large-area and low-cost fabrication. Even though the field-effect mobility of a-Si:H TFTs is much less than LTPS technology, it is sufficient to power up μLEDs with decent pixel density, which is impossible with OLEDs. However, the nature of amorphous materials gives rise to electrical instability issues. The output current of a-Si:H TFTs gradually decreases over time under electrical stress, which results in dimmer μLEDs in pixels. Moreover, the lack of complementary p-type TFTs in a-Si:H limits the integration of driver and control circuits onto the flexible platform to realize a full "system-on-flex". To overcome such shortcomings of a-Si:H technologies, this thesis makes a contribution in providing a solution to compensate the output current degradation by a novel pixel circuit with simple control scheme, as well as bootstrapped logic circuits that can be used as row driver and control circuits on flexible substrates. The proposed compensation pixel and row driver circuits can be combined to facilitate the realization of a "system-on-flex" backplane for a display panel with a-Si:H and μLED technologies.

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The last, but the most valuable support comes from my wife Shanshan, who has to take up the burden of keeping up the family and raising our young daughter Grace. None of my achievements would have been possible without her love, tolerance and trust. Besides, I am deeply grateful to my parents, and my parents-in-laws for their generous support and endless encouragement. Especially, my mom, who has always driven me to achieve better in whatever I do since I was a kid, sadly passed away just before the completion of my degree in the uncertain corona virus pandemic time. She will forever be remembered as a generous and encouraging parent.

Dedication

To my mom.

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Chapter 1

Introduction

1.1 A brief history of display technologies

Display technologies have come a long way since the inception of monochrome cathode-ray-tubes (CRTs) in the late 1890s [1]. The idea of CRTs is relatively simple. It operates on the principle that electrons, when fired at a high speed onto a screen coated with fluorescent materials can produce light. By changing the voltage, and subsequently the amount of electrons and their positions, it became possible to realize complex patterns. For a long period of time, CRTs were only used in laboratory environment. However in early 1900s, early development has explored the commercial viability of CRTs. With a tremendous amount of efforts, the first television came to the market in 1923. Even though its images were monochrome, blurry and slow, it still captured humanity's fascination of images.

However, people were not satisfied by monochrome images moving on their screens. The world of CRTs continued to evolve, and in the 1950s the first tri-color (red, green, and blue, i.e. RGB) CRT was shown to the market. Then, it enjoyed a successful commercial longevity all the way into the 1980s.

While CRTs were being purchased for every living room in ordinary families, the industry did not pause its pace. In the 1960s, the first light-emitting diodes (LEDs) were invented as well as plasma displays and liquid-crystal displays (LCDs). The first

LCD displays were only used in simple devices such as calculators and watches due to fabrication limitations [2].

The next revolution in the world of display technology was triggered by the arrival of personal computers (PCs). Screens had to be made with higher resolutions and easier to handle. Fortunately, by the advent of amorphous silicon (a-Si) thin-film transistors (TFTs), when integrated with liquid-crystals, a new generation of TFT-LCD displays were fitted onto the first large scale commercial PCs and laptops. These displays offered a much wider range of vivid colors and faster refresh rates. The fundamental idea behind the TFT-LCD is also not difficult. Using an array of TFTs to alter the voltage behind the liquid-crystals causing them to block portions of RGB light, it made gray-scale possible so that images can be formed.

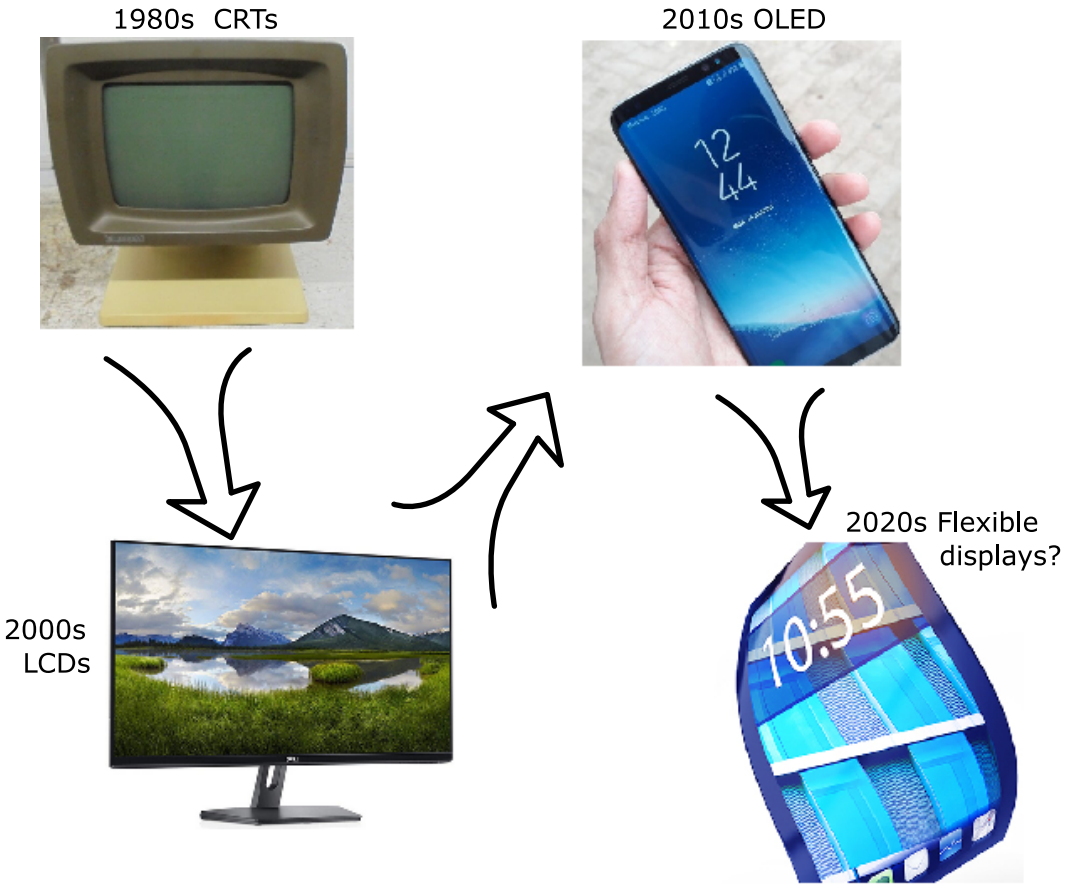


Figure 1.1: Evolution of the display technologies.

The LCD displays have made a high impact on the display industry as well as

the society during their popularity of the PC era. In the past decade, the world has witnessed a rise of another form of consumer electronics, the handheld devices in which more and more functionalities of the PCs have been integrated. As a result, the demand of a better display has increased tremendously due to the smaller size and higher resolution requirements. Driven by this demand, the development on low-temperature-poly-silicon (LTPS) TFTs and organic light-emitting diodes (OLEDs) have enabled high-contrast and high-resolution small size displays suitable for smartphones. Since their inception, they have been popular on the market till now [3, 4, 5, 6].

In the past few years, the focus on the Internet-of-Things (IoT) has spurred research activities on wearable electronics, which require curved or flexible displays for conformable shaping as well as high-brightness feature for outdoor use. As a result, the OLED displays started to show some challenges to cope with these requirements [7, 8]. In addition, these flexible displays will be powered by batteries, so a new solution with low power consumption and high brightness will be the key to the realization of this type of displays [9].

In the following sections, several key components in a modern display panel will be introduced.

1.2 Display panel components

Using a modern LCD panel as a demonstration, shown in Fig. 1.2, there is a number of components required to make a display.

The shown glass panel contains the TFT array, liquid-crystal layer, color filter, polarizer, and transparent electrodes. Then, the off-panel components, which may include power management integrated circuits (ICs), data source generator, row-select signal generator, interface connectors and other required connections to the glass panel. Shown on Fig. 1.2, a number of black ribbon cables (highlighted within

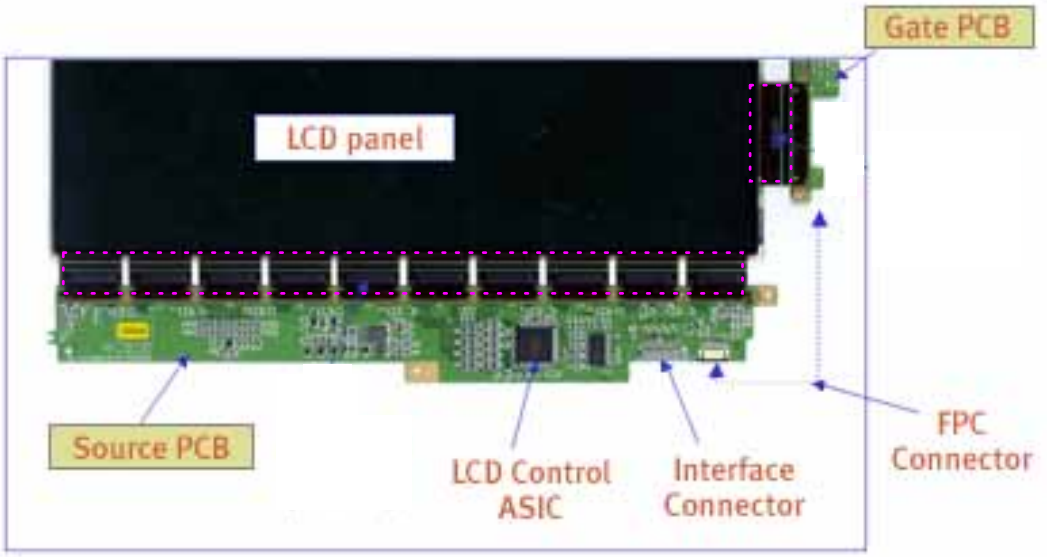


Figure 1.2: The PCB components and the panel of an LCD display.

dashed pink lines) are used to realize such connections. These connections require a complex and precise bonding process to secure links between the glass panel and external printed-circuit boards (PCBs) [10].

The cost of external components are comparatively high, and there is motivation to integrate functionality onto the display panel. Additionally, adding functionality on panel can make display energy efficient.

1.3 Comparison of light media

In most of the modern displays, the panel is made by glass which houses the light media and the backplane circuits, as well as filters and other optical components [8].

For a conventional LCD display shown in Fig. 1.3(a), there is a constant-on back-light, which is the source of all the illumination. The function of TFT array and liquid crystal is to block portions of light coming out of the back-light to achieve a range of gradient scales. Then, the color filter is to provide the combination of RGB since back-light is only white color.

Next, shown in Fig. 1.3(b), OLED displays do not require a back-light because

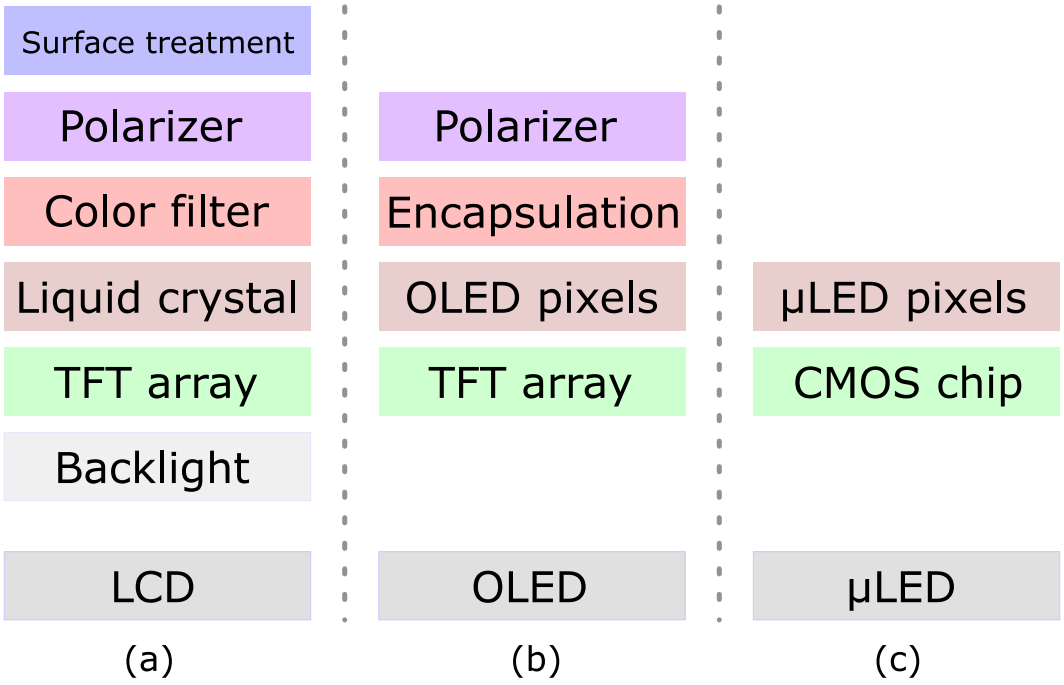


Figure 1.3: Schematic comparison of light media on rigid panels.

they are self-emissive. The TFT array delivers power to each OLED pixel directly so that there is no need of having a constant-on light source. As a result, the color contrast ratio is almost infinite because when pixels are not glowing they are completely dark. However OLEDs suffer from burn-in effect and low electro-luminescence efficiency problems. It also requires a high quality encapsulation layer to isolate the pixels from the environment to extend the life-span.

The shortcomings of OLED devices have led to the development of µLEDs, which are in-organic GaN LEDs processed at µm scale [11]. Conventionally GaN LEDs are used in interior or automobile lighting applications where their high-brightness and high electro-luminescence efficiency properties are exploited. They seem to be the ideal solution to display applications, however, difficulties in mass-transferring pixelated µLED arrays to large TFT backplanes has been the bottleneck. This is the reason that most demonstrations of µLED displays are CMOS driven small-size micro-displays shown in Fig. 1.3(c). With significant advancement in process development, the integration of µLED with TFT backplanes has become possible.

A comparison is provided in Table 1.1 which outlines the characteristics of LCD, OLED and μLEDs. It can be seen that the μLED media are the most attractive due to high output efficiency and long operational life-time [12].

Table 1.1: Comparison of light media

	LCD	OLED	μLED
Mechanism	Color filter/backlight	Self-emissive	Self-emissive
Luminous efficiency	Low	Medium	High
Luminance (cd/m^2)	$\sim 3 \times 10^2$ (full-color)	$\sim 5 \times 10^2$ (full-color)	$\sim 3 \times 10^5$ (full-color)
Contrast ratio	Low	High	High
Response time	ms	μs	ns
Power consumption	Medium	Medium	Low
Operating temperature	$-20 \sim 80°C$	$-30 \sim 70°C$	$-100 \sim 120°C$
Life span	Long	Medium	Long

1.4 Comparison of backplane circuit technologies

Beside the light media, backplane circuit technologies are also the determining factor for a display [13, 14]. There are several implementations on the market suited for different types of displays shown in Table 1.2.

Crystalline-silicon based CMOS backplane technology is being applied for ultra-high resolution small-area devices used in virtual-reality (VR) or augmented-reality

Table 1.2: Comparison of backplane technologies

	Crystalline silicon	Low-temperature poly-silicon	Amorphous silicon	Transition metal-oxide
Mobility (cm^2/Vs)	$\sim 10^3$	$\sim 10^2$	~ 1	~ 10
Device type	p- and n-	p- and n-	n- only	n- only
Fabrication area diagonal length	Very small 1”	Small $\sim 10''$	Very large $\sim 100''$	Large $\sim 10''$
Electrical stability	High	Medium	Low	Low
Device uniformity	High	Very low	High	High
Substrate flexibility	No	Medium	High	High
Cost	Very High	High	Low	High

(AR) gears. Since CMOS transistors possess very high carrier mobility at $\sim$ 1000 cm^2/Vs, they can accommodate a very small pixel down to a dimension of $5\,\mu m \times 5\,\mu m$, which is crucial for the near-eye VR displays [15, 16]. However, CMOS chips are known for their high fabrication cost and rigidity. Recently, there has been demonstrations on thinning the CMOS wafers and achieve some degree of flexibility, but the area limitation is still the major concern for making larger displays with crystalline CMOS backplane [17].

Next, the low-temperature poly-silicon (LTPS) TFTs have a carrier mobility around $\sim 100\,cm^2/Vs$ and can also be complementary [18]. They are mostly used on phone-sized displays driving OLEDs [19, 20]. The fabrication of LTPS TFTs requires a laser crystallization process on the amorphous silicon channel region. This procedure causes the TFTs to have poor large-area uniformity so that the display panels

struggle to reach tens of inches in size.

Then, hydrogenated amorphous silicon (a-Si:H) TFTs which have a low mobility of $\sim 1\,cm^2/Vs$ are conventionally used on TFT-LCD display panels [21]. Because of the constant-on back-light, the TFTs are only acting as switches to control the liquid-crystals. Therefore, these low performing TFTs are sufficient for this purpose [22]. However, due to the random nature of the amorphous material, the large-area uniformity of these TFTs are relatively high. In addition, they can be deposited with low temperature which is suitable for transparent plastic substrate enabling the potential to realize flexible displays.

Lastly, transition-metal-oxide TFTs are also deposited with the amorphous structure [23]. They resemble similar uniformity and flexibility features of a-Si:H TFTs, but with at least one order of magnitude higher carrier mobility [24]. However, their fabrication cost is higher than a-Si:H TFTs and the technology is not yet mature.

1.5 Motivations

Driven by the rapid growing demand of IoT and wearable devices, flexible displays have become a crucial component in shaping the display technology of the future. Market analysis have predicted a multi-billion dollar market on flexible electronics in the next decade. This research work was carried out with the goal of realizing a flexible display system ("system-on-flex" shown in Fig. 1.4), which is capable of providing high-brightness, low power consumption and high reliability displays.

Shown in the previous introduction, μLEDs appear to be the best choice as the light medium for flexible displays due to its high luminescence efficiency and long life span. On the other hand, a-Si:H TFTs which have excellent large-area uniformity and low cost may emerge as the backplane circuit choice.

After the successful demonstration of μLED integrated onto plastic substrate, it becomes crucial to design reliable a-Si:H backplane circuits to realize flexible displays.

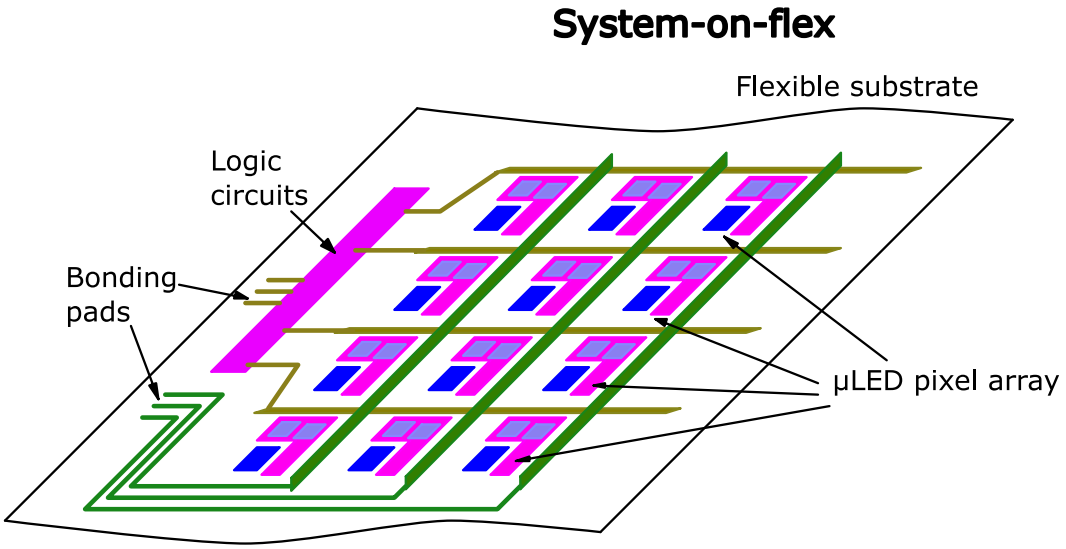


Figure 1.4: The diagram of a flexible µLED+a-Si:H TFT backplane.

Due to the nature of amorphous material, the electrical instability of the TFTs is a major disadvantage, especially in the case of µLED displays. Because these displays are self-emissive, so the TFTs need to supply power unlike their functions of being only switches in the conventional TFT-LCD displays. With this constraint, the well-known mobility degradation of a-Si:H TFTs can cause a display to lose brightness over-time. In addition, the lack of a complementary transistor type further complicates design of additional functionalities on the flexible panel.

With above mentioned challenges in mind, the thesis makes an attempt to provide circuit solutions. In particular, a novel compensation pixel circuit is demonstrated that is able to provide stable brightness despite changing threshold-voltage of the driver transistor on a flexible substrate. In addition, realization of multistage logic circuit with only n-type transistor is demonstrated that has CMOS-like properties.

With these challenges in mind for a-Si:H backplane, this thesis has provided several solutions to tackle the problems, such as compensation pixel circuits to retain µLED brightness over-time and full-swing low-power logic gates to realize complex digital circuits on flexible substrate. All these solutions are to facilitate the realization of flexible displays with the combination of µLED and a-Si:H TFTs.

1.6 Thesis outline

This thesis is organized in the following manner:

Chapter 1 provides a brief introduction of the display technologies for the past half a century and compared the light media and backplane technologies. It also brings up the motivation and goal of the research work.

Chapter 2 discusses background information on existing pixel driving scheme and amorphous silicon TFT properties to prepare readers for the core analysis of the thesis.

Chapter 3 shows a successful integration of μLEDs onto a-Si:H TFT pixel circuit on flexible substrate which demonstrates high-brightness and low-power features.

Chapter 4 proposes a novel compensation pixel circuit on flexible substrate to tackle the electrical instability of the TFTs with mathematical derivation, circuit simulation and measurement results.

Chapter 5 proposes novel logic gates with full-swing and low static leakage current suitable for peripheral circuits that controls pixel arrays on flexible substrate. Also, a demonstration of "system-on-flex" has been realized.

Chapter 6 concludes the thesis and lists suggested future work.

Chapter 2

Background

2.1 Display architectures

The majority of the area on the backplane of a display panel is occupied by the pixels. There are two types of display pixel architectures in the existing market, they are passive-matrix and active-matrix methods.

2.1.1 Passive-matrix architecture

In the passive-matrix (PM) addressing scheme shown in Fig. 2.1, there is no transistor backplane involved, only the light media [25]. The LED array is addressed row by row from an external driver. When a row of LEDs is selected, the voltage of the row line turns to ground and individual column driver is set to the desired current to represent the image information of all the LEDs. Because there is no transistor or storage component to maintain the image information, all the LEDs turn off when the next row is being addressed [26].

Even though PM architecture is known for its simplicity of only requiring light media on the display panel without backplane circuits, it is not capable of delivering the needs for large-area and high-resolution displays. Because in order to form any

still image or video on a PM display panel, the LEDs need to be driven at a much higher refresh rate. In addition, the column data drivers have to cope with accurate and high-levels of instant current density during the very short ON period of a display cycle which is very difficult to achieve. Therefore, PM architecture is only suitable for small-area and low-resolution digital displays typically less than 200 rows to maintain a standard refresh rate of 60 Hz [26, 27].

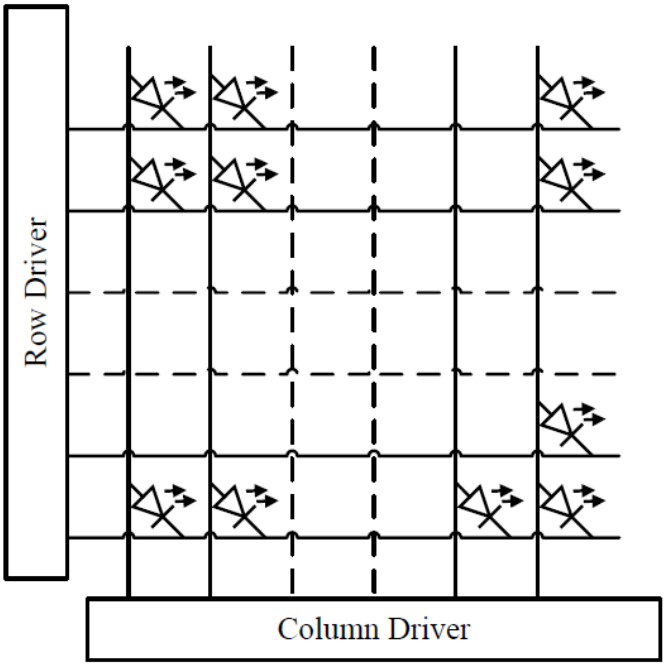


Figure 2.1: Backplane circuit example of an LCD display panel.

2.1.2 Active-matrix architecture

Considering the disadvantages of PM architecture, the active-matrix (AM) addressing was invented (shown in Fig. 2.2) and have been widely used since its inception [28]. In AM display panels, TFTs are used to control each pixel. There are typically two phases of operation. During programming phase, the data is stored in the pixel circuit. Next, in the emitting phase, the LED will glow proportionately to the stored data in the pixel circuit. The programming operation is carried out row by row through an external IC driver and traverses through the entire display panel. In addition,

the instant peak current density is much reduced compared to the PM architecture because of the continuous emission from the LEDs. Therefore, AM architecture is widely used in flat-panel displays. It is also the method used in this research work.

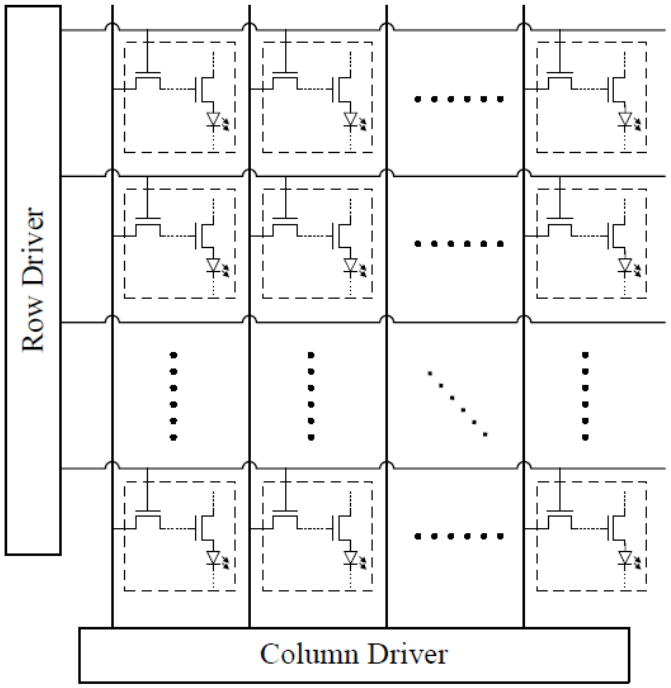


Figure 2.2: Backplane circuit example of an LCD display panel.

2.2 TFT families for display backplane

After comparing the display architecture and choosing the AM scheme, it is important to understand the differences among existing backplane technologies. The two main ones are low-temperature-poly-silicon (LTPS) and hydrogenated amorphous silicon (a-Si:H).

LTPS TFTs have excellent carrier mobility of $\sim 100\,cm^2/Vs$ as well as complementary device types, i.e. p- and n-. In addition, the electrical stability of LTPS TFTs is superior compared to a-Si:H ones because of the higher degree of crystallization in the channel region. However, a major drawback of LTPS TFTs is the poor spatial uniformity, i.e. high device variation in a large area. This is due to the non-

uniform crystallization during the laser annealing process which forms the poly-silicon active layer. These spatial variations cause poor pixel performance and result in low image quality. Therefore, LTPS TFT backplane is mostly used for OLED smartphone displays which requires high current and small fabrication area.

Owing to the superior performance of μLEDs against OLEDs, a-Si:H TFTs has emerged to be a viable backplane material solution. Even though the mobility of a-Si:H TFT is just around $\sim 1\,cm^2/Vs$, it is sufficient to drive μLEDs with excellent brightness. In addition, a-Si:H TFTs have been used in the TFT-LCD panels for such a long time, the fabrication cost of these backplanes are much lower compared to LTPS panels.

2.2.1 The structure of a-Si:H TFT

Fig. 2.3 depicts four typical device structure of a-Si:H TFTs, i.e. staggered, inverted staggered, co-planar and inverted co-planar. Co-planer (inverted co-planer) devices are fabricated with the semiconductor layer being the first (last). These fabrication techniques are typically used for printed organic TFTs because the printing step does not use a conventional deposition chamber and require all other layers to be made prior to the printing. On the other hand, co-planer devices have sub-optimal contact resistance resulting in lower carrier mobility [29]. The other device category is staggered structure where the semiconductor and gate dielectric layers are sandwiched between the gate and source/drain electrodes. Such configurations can reduce contact resistance which leads to higher carrier mobility. Moreover, the gate dielectric and semiconductor layers could be deposited sequentially without breaking vacuum from the chamber, so that the quality of the material interface is higher [30]. With these considerations, the TFT devices used in this research work are based on the staggered structure.

In the detailed layer-by-layer view of a-Si:H TFTs with inverted staggered struc-

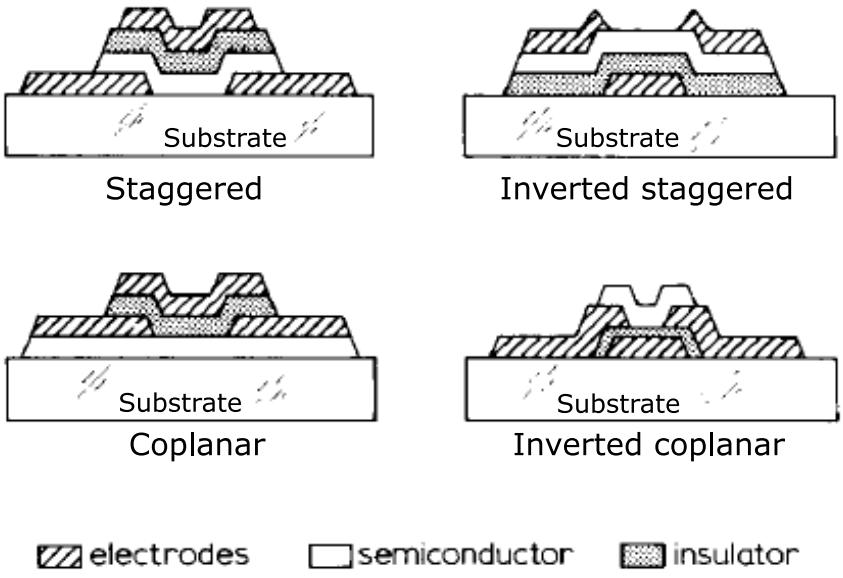


Figure 2.3: Four device structures for a-Si:H TFTs.

ture shown in Fig. 2.4, metal gate is at the bottom of the stack and directly fabricated on top of the substrate. Then, a tri-layer of amorphous silicon nitride (a-SiNx:H), intrinsic a-Si:H and doped n^+ are deposited sequentially on top of the gate metal using a plasma-enhanced chemical-vapor deposition (PECVD) system. Afterwards, the source/drain metal is patterned and the tri-layer is etched back to expose the intrinsic a-Si:H layer as the channel of the transistor. After these process steps a-Si:H TFTs can be formed.

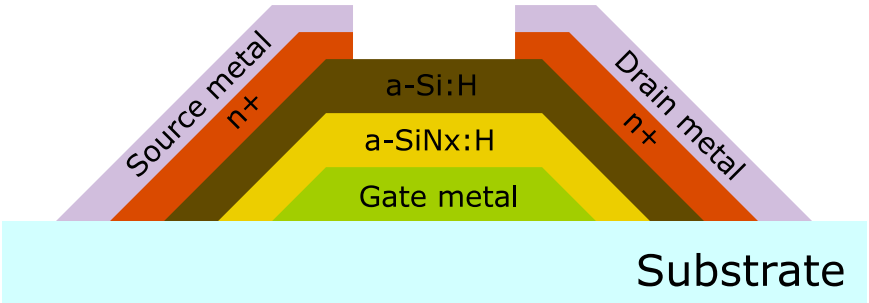


Figure 2.4: Fabricated layers of inverted staggered a-Si:H TFTs.

The deposition of a-Si:H layer uses a low-temperature process (typically less than $300°C$) which is very different from the high-temperature growth conditions used in crystalline-silicon CMOS fabrication. Shown in Fig. 2.5, the density of state vs.

energy level of amorphous silicon material is presented. Different from the clearly defined band edges of crystalline-silicon, amorphous silicon has broadened tail states extending into the forbidden band-gap caused by localized energy states. In addition, the defects from broken Si-Si bonds contribute to the states in the middle of the band-gap. The high concentration of defects and the slightly n-type nature of amorphous silicon material have made the realization of p-type a-Si:H TFTs difficult [31, 32].

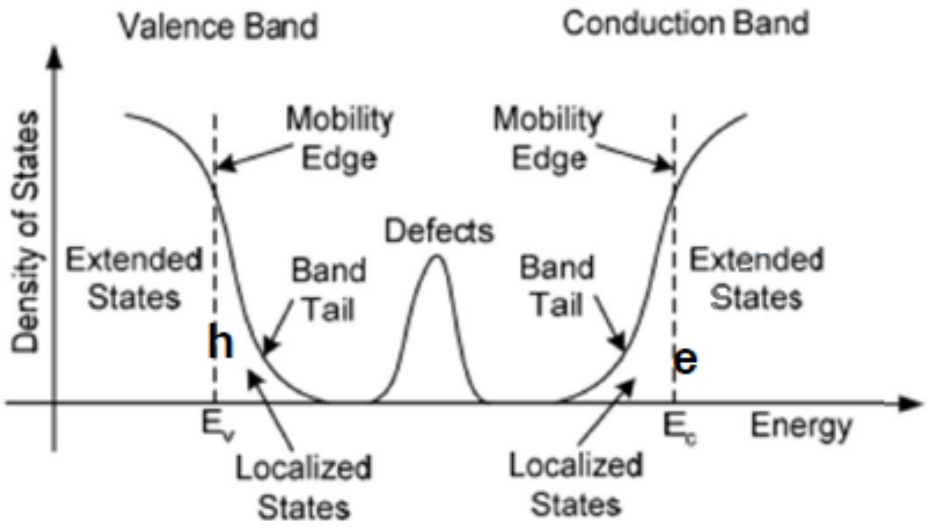


Figure 2.5: The band diagram of intrinsic a-Si:H.

The presence of high density of defects contributes to the low carrier mobility of a-Si:H TFTs [32]. In addition, voltage bias induced degradation may occur under different circumstances [33, 34, 35]. When stressed with a positive gate voltage, there could be more defect states formed in the channel or dielectric layers manifesting as a threshold-voltage (V_T) shift on the I-V curve. When a-Si:H TFTs are used as the pixel circuits for displays, this degradation can cause the brightness to go down resulting in a short life-span. Therefore, providing a method to compensate for such degradation is a focus of this research work. Furthermore, when considering applied mechanical strain, the electrical instability may behave differently under various strain conditions. Such effect is also studied in this work in details.

2.3 Peripheral control circuits

Traditionally, display panels consist of large array of pixel circuits as illustrated in Fig. 2.6, and several other components such as data and control drivers are outside the panel implemented in expensive CMOS technologies. However, there is growing motivation to integrate some of these components to make displays cheaper, energy-efficient and reliable [36, 37, 38].

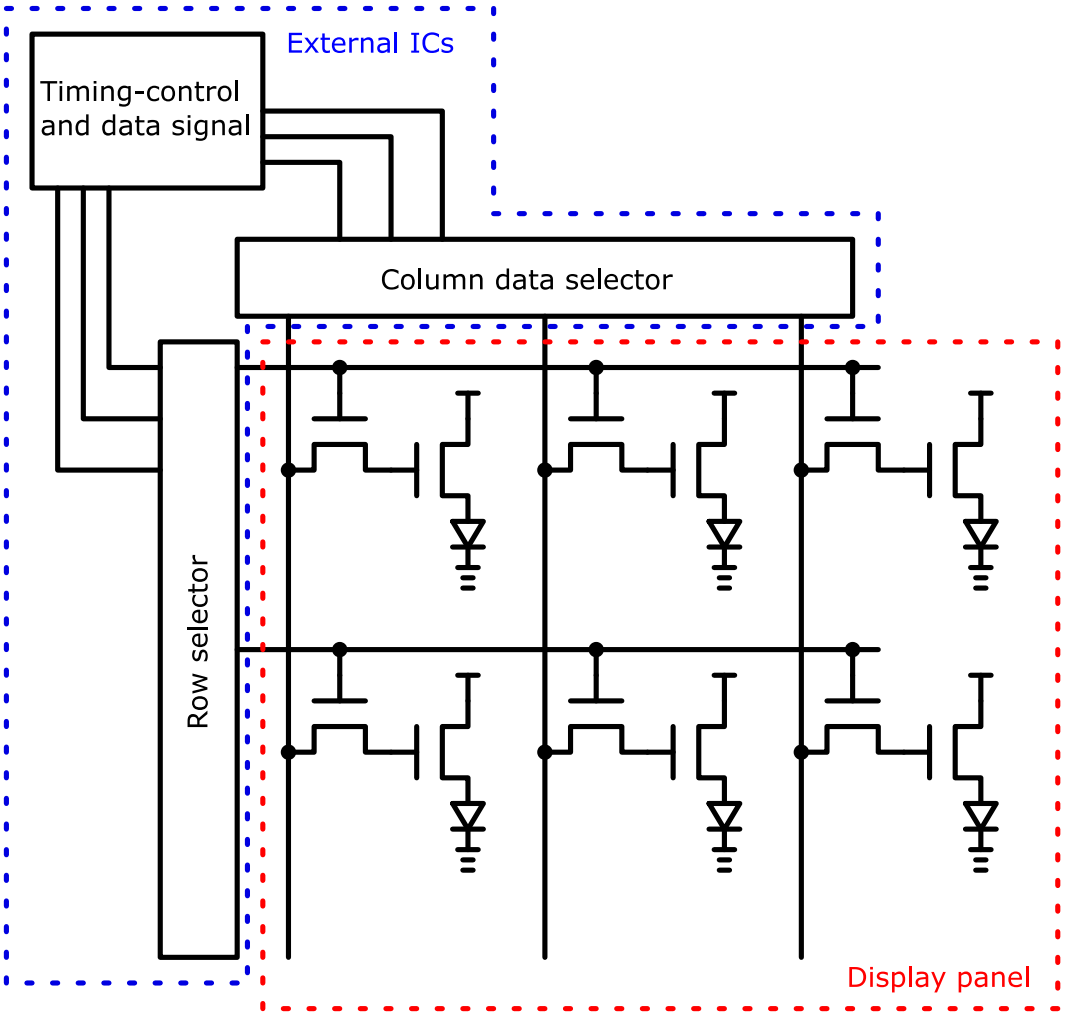


Figure 2.6: Backplane and external IC components of a display.

In CMOS technologies, both p- and n- type transistors are available which are efficient for conducting logic "1" and "0", respectively. Unfortunately, this is not the case for a-Si:H TFT technology. Often only n-type device is available for circuit

designers which makes realization of full-swing, energy-efficient, logic circuit a challenging task. Prior solutions mainly focus on fabrication improvement or exploiting external power supply to realize full swing logic gates which is costly and complex. Therefore, circuit solution would be the ideal method to tackle this problem. In this research work, novel circuit solutions to realize full-swing and low-power logic gates are proposed and verified to prove the feasibility of integrating circuit components on panel.

2.4 Summary

This chapter provides the readers with relevant background knowledge on the display architectures and TFT devices.

It outlines the benefit of AM addressing scheme and the benefits of using a-Si:H TFTs in the backplane circuit on flexible substrate. It also explains the shortcomings of a-Si:H TFTs, such as electrical instability under bending and the lack of a complementary device type. Solving those challenges is the focus of this research work and will be presented thoroughly in the following chapters.

Chapter 3

Power-efficient pixel circuit

In recent years, micrometer sized light-emitting diodes (μLEDs) have been extensively researched as potential light media for the next-generation of flat-panel as well as flexible emissive displays. μLEDs possess many benefits when compared with organic-light-emitting diodes (OLEDs) such as brightness, operational life-time, and luminescence efficiency [39]. In the past few years, there have been multiple technologies developed for integrating μLEDs onto different substrates such as transfer-printing, epitaxial lift-off, and laser-induced transfer [40]. These methods have attained varying degrees of success. For flexible displays, passive matrix (PM) addressing is still the popular implementation method owing to its simplicity [41]. However, it has several well-known drawbacks such as low resolution and high instant power consumption and etc. Consequently, active-matrix (AM) addressing scheme is needed if the display were to scale to a higher resolution and refresh rate.

At present, the display of choice includes low-temperature poly-silicon (LTPS) TFTs with OLEDs. However, if μLEDs were to become a reality for flexible displays, additional considerations such as cost, scalability, and mechanical stability needs to be investigated.

As mentioned in the previous chapter, the LTPS technology has superior carrier mobility and higher current drive compared to a-Si:H TFT technology. However, it

suffers from poorer uniformity over large display area. On the other hand, μLEDs are more power and energy efficient compared to OLEDs. Arguably, μLEDs together with a-Si:H TFTs can be a viable alternative to power-hungry OLED and LTPS panels. This was the motivation for the research described in this chapter. Two pixel circuit configurations with μLEDs are presented and analyzed.

3.1 Source-anode configured conventional pixel

[1] The first method to realize μLED with a-Si:H TFT pixel circuit is to mimic the LTPS+OLED configuration in which the anode of the μLED is placed at the source side of the driving TFT shown in Fig. 3.1. In the pixel circuit, the switch TFT (T_1) controls the charging and discharging of the storage capacitor in the programming phase and the driving TFT (T_0) supplies current to the μLED in the emitting phase [42].

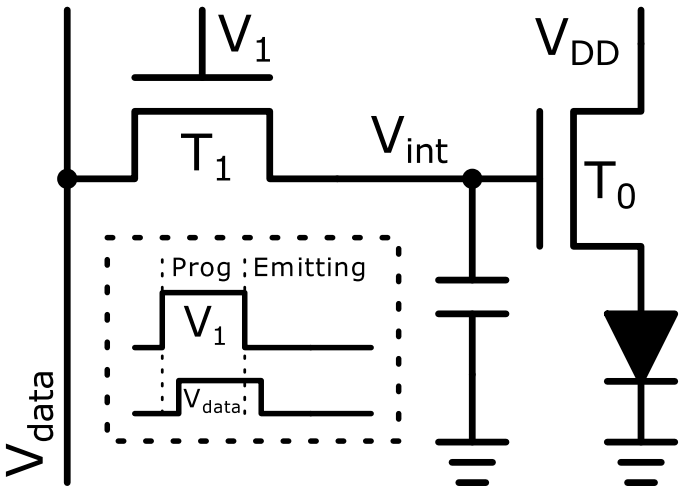


Figure 3.1: The conventional 2T pixel circuit with timing-control signals.

The integration process is divided into three major parts. Fig. 3.2(a) to (c) show the preparation of the surface after a-Si:H TFT pixel circuits have been fabricated

[1] This chapter is an amended version of "Integration of GaN light-emitting diodes with a-Si:H thin-film transistors for flexible displays", including modified figures and tables, by M. Asad, Q. Li, C.-H. Lee, W. S. Wong, M. Sachdev, published in Nanotechnology, with ©IOP Publishing 2019. If citing any figure or table, please refer to the original publication.

onto flexible substrate. These steps expose "a landing pad" on the source terminal of T_0 and also coat a bonding metal (BM). (d) to (f) show the process to obtain individual μLEDs from the sapphire substrate. Lastly, (g) and (h) show the final steps of bonding with a laser-lift-off process [43].

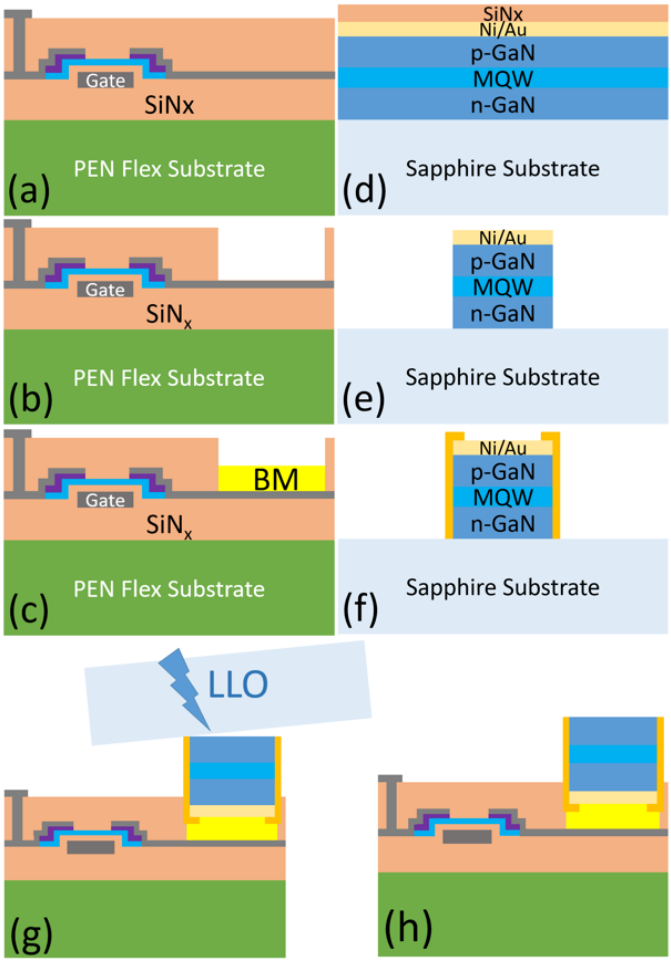


Figure 3.2: The single-transfer laser-lift-off process to integrate the μLED onto 2T pixel circuit in a source-anode configuration. (a) to (c) represent the preparation process after the a-Si:H TFT pixel circuit has been fabricated onto a flexible PEN substrate (BM = bonding metal). (d) to (f) show the process steps to fabricate individual μLEDs from a sapphire wafer. (g) to (h) is the bonding and laser-lift-off process to integrate the two parts to form full pixels.

In this experiment, the μLED had a geometry of $90\,\mu m \times 90\,\mu m$. From the I-V curve and electro-luminescence performance of the μLED, the TFTs in the pixel are designed to have a W/L of $100\,\mu m/20\,\mu m$ and $1000\,\mu m/20\,\mu m$ for T_1 and T_0 respectively. The layout of T_0 uses an inter-digitation style to make the pixel square-

shape. The extracted measurement results showed that the TFTs have an effective carrier mobility μ_{eff} of $\sim 0.9\,cm^2/Vs$ and a threshold-voltage of $\sim 3\,V$. The µLED has an on-voltage of $\sim 2.4\,V$. When using $20\,V$ as the supply (V_{DD}) and $5 \sim 15\,V$ as the V_{data} range, the pixel circuit could supply a current from $0\,\mu A$ to $\sim 17\,\mu A$. The post-fabrication micro-graph of the 2T pixel circuit before and after µLED integration is shown in Fig. 3.3(a) and (b), respectively. The transient voltage and current waveform of the full pixel is shown in Fig. 3.3(c) and the current/electro-luminescence vs. V_{data} is shown in (d).

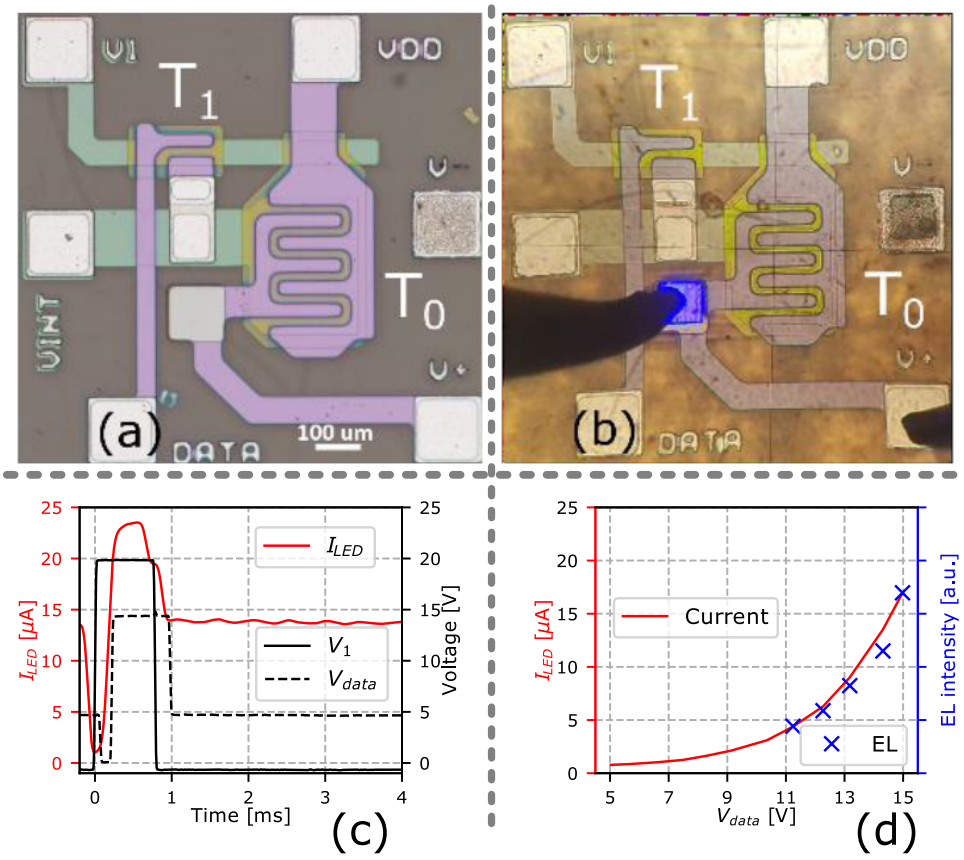


Figure 3.3: The micro-graph of the 2T pixel circuit (a) before and (b) after µLED bonding. (c) The transient voltage (black) and current (red) waveform of the full pixel circuit when $V_{data} = 14\,V$. (d) The current (red) and relative electro-luminescence (crosses) vs. V_{data}.

3.2 Power-efficient pixel circuit

With the advancement of μLED transfer and bonding technology, there is a distinct advantage of μLED over OLED media which is the ability to create drain-cathode inverted μLED structures shown in Fig. 3.4(b). Unlike the conventional OLED process, where a drain-cathode structure is impractical due to the environmental instability of the electron injection layer [44, 45], μLED devices may be integrated onto the pixel circuit with diode on the drain-side of the driving TFT. This configuration provides much higher dynamic range for the display due to the lower overdrive voltage needed to bias the μLED.

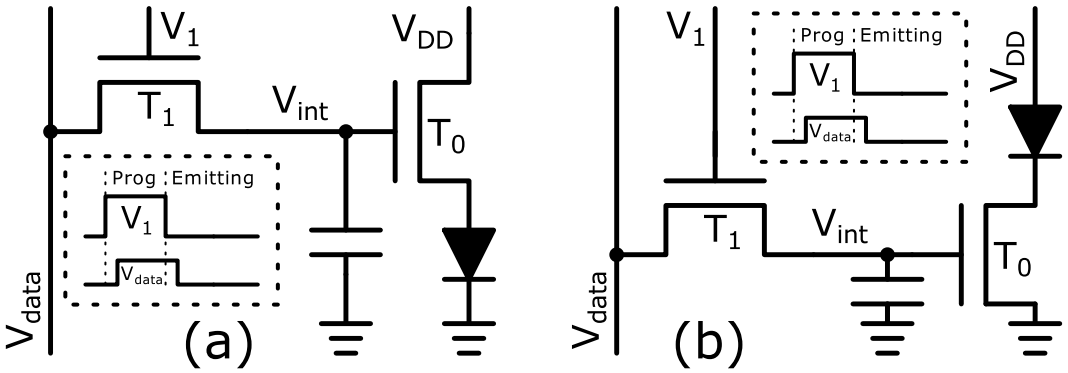


Figure 3.4: (a) The conventional source-anode and (b) proposed drain-cathode 2T pixel circuit.

Using a level-61 a-Si:H TFT model [46], the conventional and proposed pixel circuits have been simulated and the transient current waveform is shown in Fig. 3.5(a) and (b), respectively. In the simulation, V_{data} was set to be between $5\,V$ to $15\,V$ with $2\,V$ intervals to demonstrate the advantages of the proposed drain-cathode configuration.

The improvement of the proposed drain-anode pixel circuit could be explained as follows. Assume TFTs only turn on after threshold-voltage is reached and channel-length-modulation (λ) is negligible. In the conventional pixel circuit, the lower bound of the V_{data} needs to be at least the sum of the on-voltage of the μLED (V_{ON}) and the threshold-voltage of the driving TFT (V_T), so that T_0 can light up the μLED. On

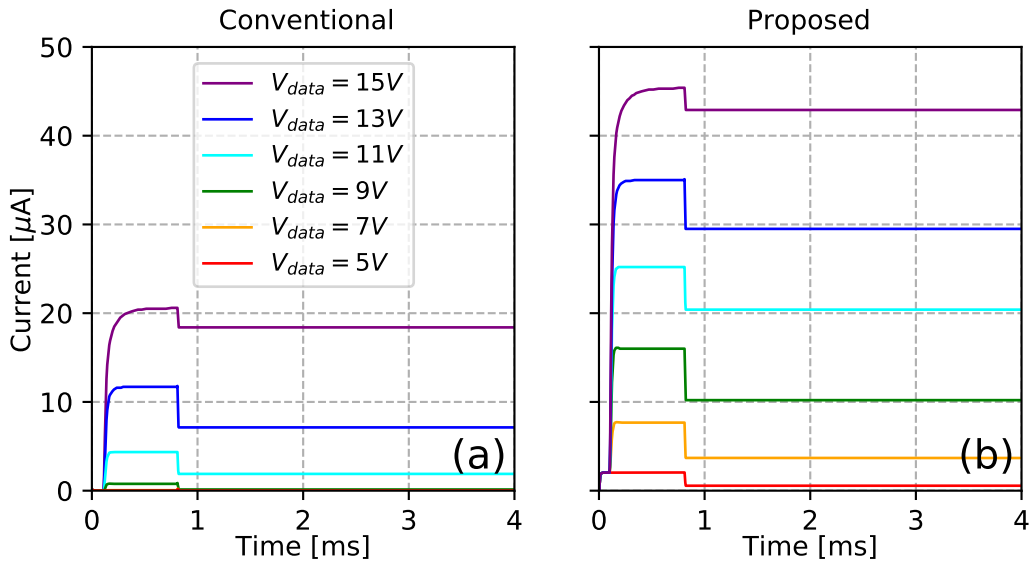


Figure 3.5: Simulated transient current at different V_{data} of the (a) conventional and (b) proposed pixel circuits.

the other hand, the upper bound of the V_{data} needs to be one V_T less of the on-state voltage of V_1 (in this case it is V_{DD}).

On the other hand, with the proposed pixel circuit, the μLED is moved to the drain side of T_0 so that the lower bound of V_{data} only needs to be V_T while the upper bound remains the same. Therefore, the dynamic range of V_{data} has been increased from $V_{DD} - 2V_T - V_{ON}$ to $V_{DD} - 2V_T$. The comparison is visually demonstrated in Fig. 3.6.

The first order field-effective transistor equation is used to demonstrate current-voltage relationship for the driving TFT (T_0) in saturation mode.

$$I_{DS} = \frac{1}{2}\mu_{eff} C_{nitride} \frac{W_0}{L_0} \left(V_{int} - V_T\right)^2 \tag{3.1}$$

The impact of voltage on the drain-source current is squared so that a dynamic range increase on the V_{data} can drastically increase the current output and the pixel brightness without raising the power supply voltage. On the other hand, if the brightness level remains the same, the proposed pixel circuit would require a much lower

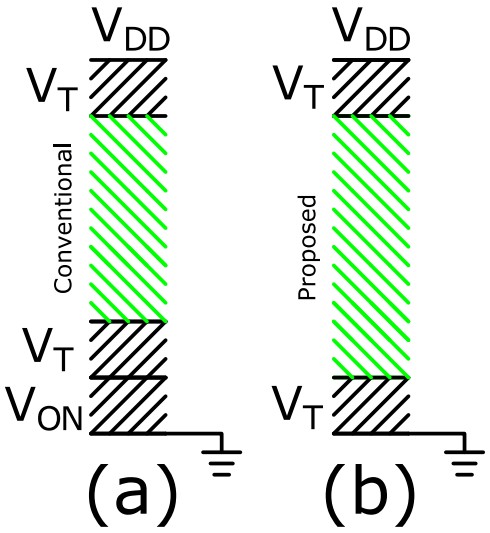


Figure 3.6: The dynamic range comparison on V_{data} of the (a) conventional and (b) proposed pixel circuits. The green shaded region indicates the dynamic range.

V_{data} signal to program the storage capacitor resulting in low-power consumption on the external column data driver.

In summary, the proposed drain-cathode pixel circuit could provide higher dynamic range and lower power consumption on the external data driver. It is preferred over the conventional source-anode pixel circuit.

3.3 Realization of the drain-cathode pixel circuit

The fabrication of the proposed drain-cathode pixel circuit has a distinct difference from the conventional one. The procedure included a double-transfer step which is necessary to temporarily hold the pixelated μLEDs onto a handler substrate. Only in this way, the cathode side of the μLED can be exposed and bonded to the drain contact pad of the driving TFT. The final schematic of the fabricated pixels are shown in Fig. 3.7. It can be seen that the TFT layers had no difference and the only the μLED is flipped.

The micro-graphs of the bonded and lit-up pixels with drain-cathode configuration are shown in Fig. 3.8.

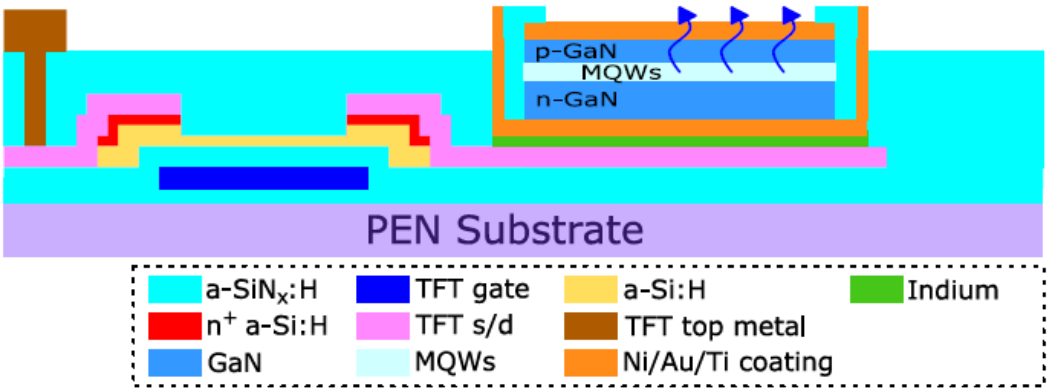


Figure 3.7: The schematic view of the fabricated layers using the double-transfer laser-lift-off process to integrate the μLED onto 2T pixel circuit in a drain-cathode configuration.

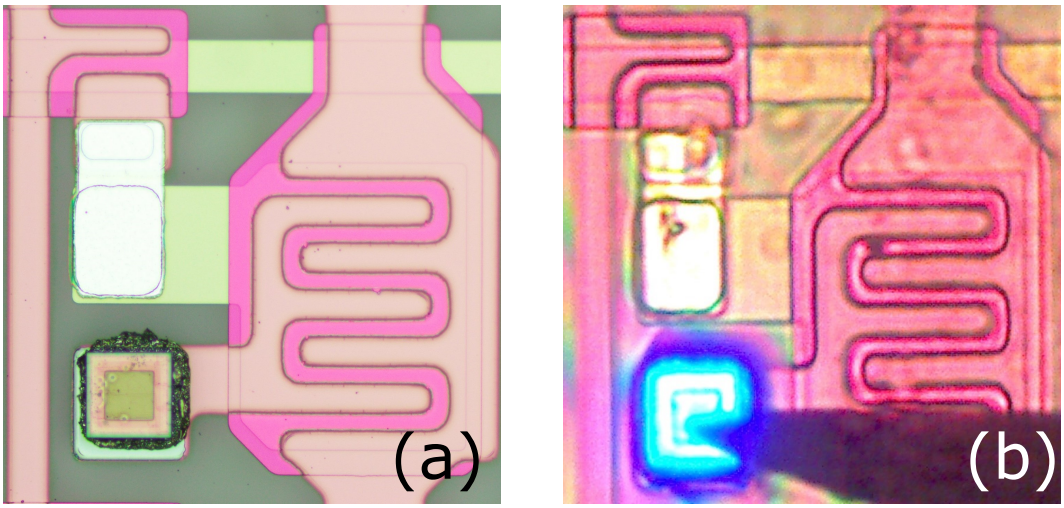


Figure 3.8: The micro-graph of the 2T pixel circuit (a) before and (b) after μLED bonding with the proposed drain-cathode configuration.

Both the conventional and proposed pixel circuits have been characterized under the same $V_{DD} = 20\,V$ and $V_{data} = 5\,V \sim 15\,V$ conditions and the results are illustrated in Fig. 3.9. The proposed pixel circuit could provide a maximum output current of $\sim 40\,\mu A$ and the conventional one was only $\sim 17\,\mu A$, this is a 2.4x improvement. Such increase in dynamic range is also reflected in the electro-luminescence data shown as blue crosses in the figure.

Meanwhile, the proposed pixel circuit only required $\sim 11\,V$ on the V_{data} signal to achieve the same brightness as the conventional pixel when V_{data} was equal to $15\,V$. Assume each V_{data} has equal probability during normal display operation, the energy

saving could be up to 38% on the column data driver.

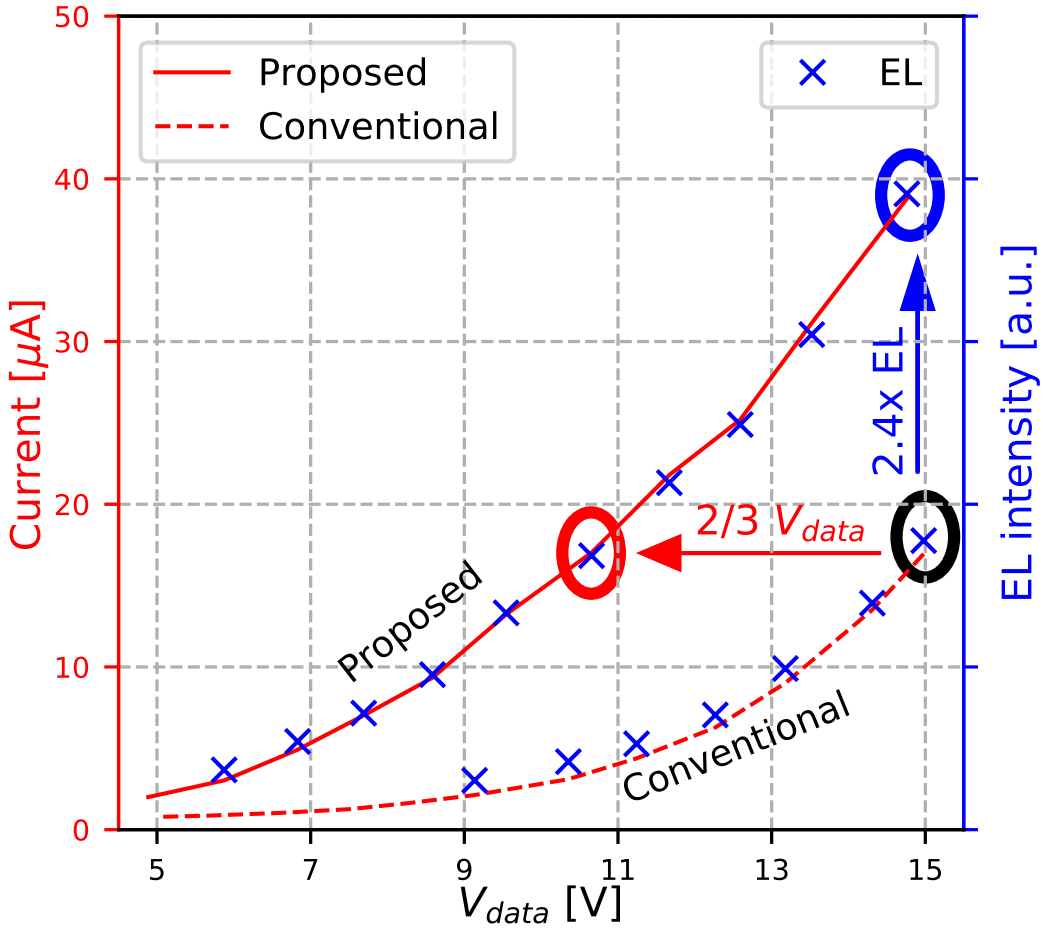


Figure 3.9: Current and EL intensity comparison of the conventional and proposed pixel circuits.

In conclusion, the proposed drain-cathode pixel circuit using high-performance μLEDs and a-Si:H TFTs have been demonstrated, it provides advantages of high dynamic range and low power consumption. Such benefits may lead to the realization of next-generation flexible displays.

However, this integration is not problem free. Even though μLEDs do not demonstrate drastic differences under long-term electrical stress or mechanical strain, a-Si:H TFTs do suffer from these shortcomings. It is well known that amorphous silicon with its random nature degrades under voltage-bias induced stress and applied bending. Therefore, it is crucial to find a solution to tackle these problems so that the back-

plane TFT circuits could function reliably on a flexible substrate. These concerns lead to a solution that will be presented in the next chapter in which a compensation pixel circuit is proposed and its operating principle and effectiveness under bending are thoroughly discussed and analyzed.

Chapter 4

Compensation pixel circuits for flexible displays

Hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) technology is a popular and inexpensive technology of choice to realize active-matrix liquid-crystal displays (AM-LCDs) [42, 47]. The technology has its advantages in low-temperature processing and excellent device uniformity in large-area fabrication. These advantages may facilitate the realization of next-generation flexible displays. Recent advancements in micro-light-emitting-diode (μLED) fabrication and transfer have enabled the possibility of integrating μLED onto a-Si:H TFT backplane to achieve low-power and flexible emissive displays [48, 49]. Unlike organic-LEDs (OLEDs), μLEDs are inorganic devices with much lower power consumption to reach equivalent brightness [50]. Thus, a-Si:H technology with relatively lower carrier mobility compared to low-temperature poly-silicon (LTPS) which is commonly used in OLED display for smart-phones, becomes a potent candidate for the backplane circuits.

The previous chapter has proven that the integration of μLED onto flexible PEN substrate with a-Si:H TFTs is feasible. The combination may provide a low-cost and mechanical flexible solution to next-generation displays.

Even though a-Si:H technology possesses great advantages to realize flexible back-

plane circuits, its shortcomings are also well known. The voltage-bias induced degradation of electrical stability causes a reduction of output current over-time. This behavior is mainly due to defect-creation and charge-trapping in the a-Si:H channel and the gate dielectric layers, respectively [51]. The degradation is usually modeled as a threshold-voltage shift (ΔV_T) [52, 53]. If left uncompensated, the degradation can result in brightness loss over-time and lead to shortened life-time of a display panel. A number of circuit solutions have been proposed to tackle this issue including reverse-bias annealing of the emitting TFT [45], sensing the ΔV_T of the emitting TFT using external ICs [54], internally sensing the ΔV_T using feedback TFTs [55], and charge-transfer using a correlation between driving and compensation TFTs [46]. All these methods have compensation capabilities to varying degrees. Their drawbacks include: complex control signals, added pixel circuit complexity, high cost of external CMOS circuits, and slower operating speed due to internal sensing and reverse annealing.

Furthermore, when fabricated onto flexible substrates, a-Si:H TFTs have another degree of variation due to applied mechanical strain. Tensile and compressive strains cause a-Si:H TFTs to degrade differently under constant voltage bias [56]. The orientation of the TFT also affects the degradation under bending [57, 58]. This additional factor should be taken into account when designing pixel circuits on flexible substrates.

This chapter first discusses prior compensation schemes, and then presents a charge-transfer self-compensating 6-TFT (6T) pixel circuit with only two control signals implemented on a flexible substrate. The proposed 6T pixel circuit provides reliable compensation performance when laid flat or even under mechanical strain. The proposed pixel circuit operates under an enhanced charge-transfer method to provide stable output current to the display media. The layout of the pixel is also specifically designed to mitigate the impact of bending on the circuit performance. Moreover, detailed operation of the 6T pixel circuit with various bending simulation and measurement results are thoroughly investigated.

4.1 Introduction to compensation schemes

4.1.1 Conventional 2T pixel circuit

The simplest active-matrix pixel circuit involves two TFTs, one functions a switch (T_1) and the other one functions as a driver (T_0) that supplies power to the light medium, such as an OLED or a μLED shown in Fig. 4.1(a). The pixel circuit also contains a storage capacitor realized by metal-insulator-metal (MIM) layers. The operation of the pixel circuit is divided into two phases, programming and emitting shown in Fig. 4.1(b). During programming phase, T_1 is switches on by a high control signal V_1 and immediately afterwards V_{data} programs the storage capacitor with the desired brightness voltage level. After allowing sufficient time for the storage capacitor to be fully charged, V_1 is turned low to switch T_1 off, the pixel enters the emitting phase, in which the pixel glows with the programmed brightness until the next refresh cycle begins.

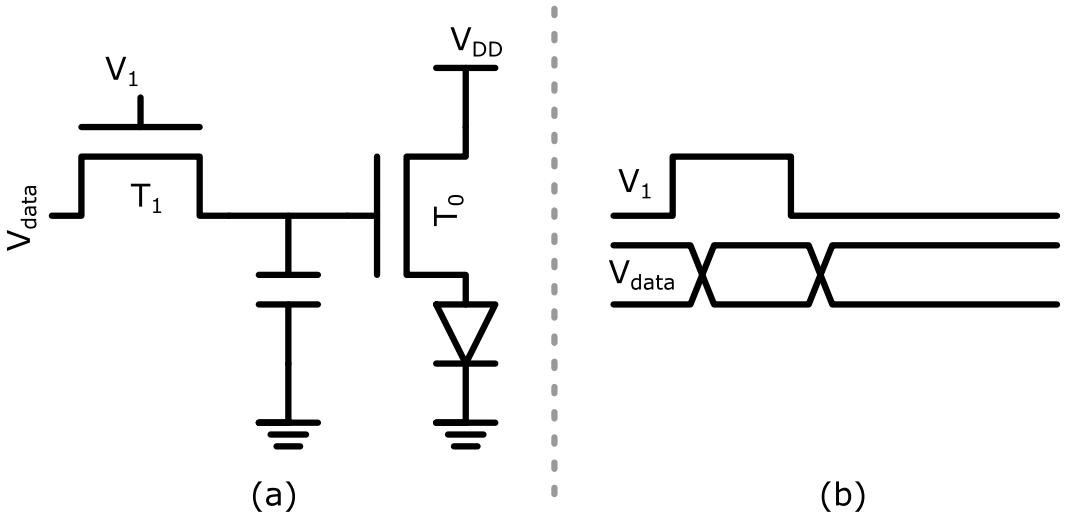


Figure 4.1: The (a) schematic and (b) control signals of the proposed 2T pixel circuit.

During the normal operation of a display panel, the TFTs are constantly under voltage-bias induced stress and their performance degrade over-time, especially the driving TFTs because they are operating in saturation mode nearly all the time. In

the case of a-Si:H TFTs, the degradation could be generally modeled by a threshold-voltage shift (ΔV_T) [59, 51, 56] given by the equation below:

$$\Delta V_T(t) = (V_{GS} - V_T) \times \left[1 - e^{-(\frac{t}{\tau})^{\beta}}\right] \tag{4.1}$$

The τ and β are process parameters related to the fabrication condition of the TFTs, and "t" is the time under which the TFTs are bias stressed. An example of output current (I_{DS}) decay under constant voltage bias is shown in Fig. 4.2. In this example, the parameters values were $\tau = 116000$ and $\beta = 0.3053$, the drain voltage V_{DD} was $20\,V$ and the V_{data} was $15\,V$.

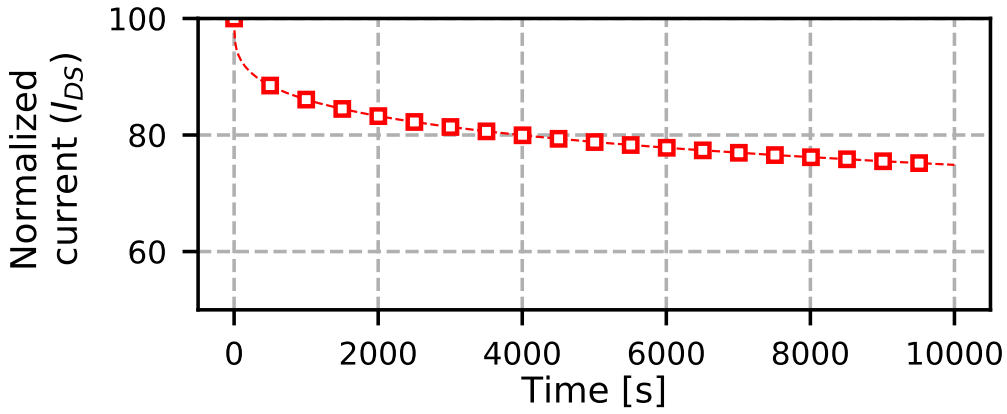


Figure 4.2: An example of I_{DS} degradation under constant voltage-bias over-time.

It is noticed that without any designated compensation mechanism, the 2T pixel circuit alone is not suitable for any display product due to a very short life-time. The output current decreases by 20% even within the first hour of operation.

Therefore, in order to utilize a-Si:H TFTs as the backplane circuit devices for display panels, compensation scheme is required. The following sections will briefly introduce several prior compensation schemes and list their pros and cons to facilitate a well-rounded understanding of the compensation concept.

4.1.2 Compensation scheme - external detection

One intuitive method for compensation is to engage external CMOS ICs to detect the threshold-voltage shift in the pixel circuit. Amiri et al. has proposed a simple pixel circuit with off-panel ICs to achieve this goal [60].

The full compensation scheme is shown in Fig. 4.3. It consists of a 3-TFTs and 1-capacitor (3T+1C) pixel circuit shown in Fig. 4.3(a) and an external cyclic digital-to-analog converter (DAC) with its associated switches and capacitors shown in Fig. 4.3(c). The timing-control signals of the pixel circuit and the external switches are presented in Fig. 4.3(b).

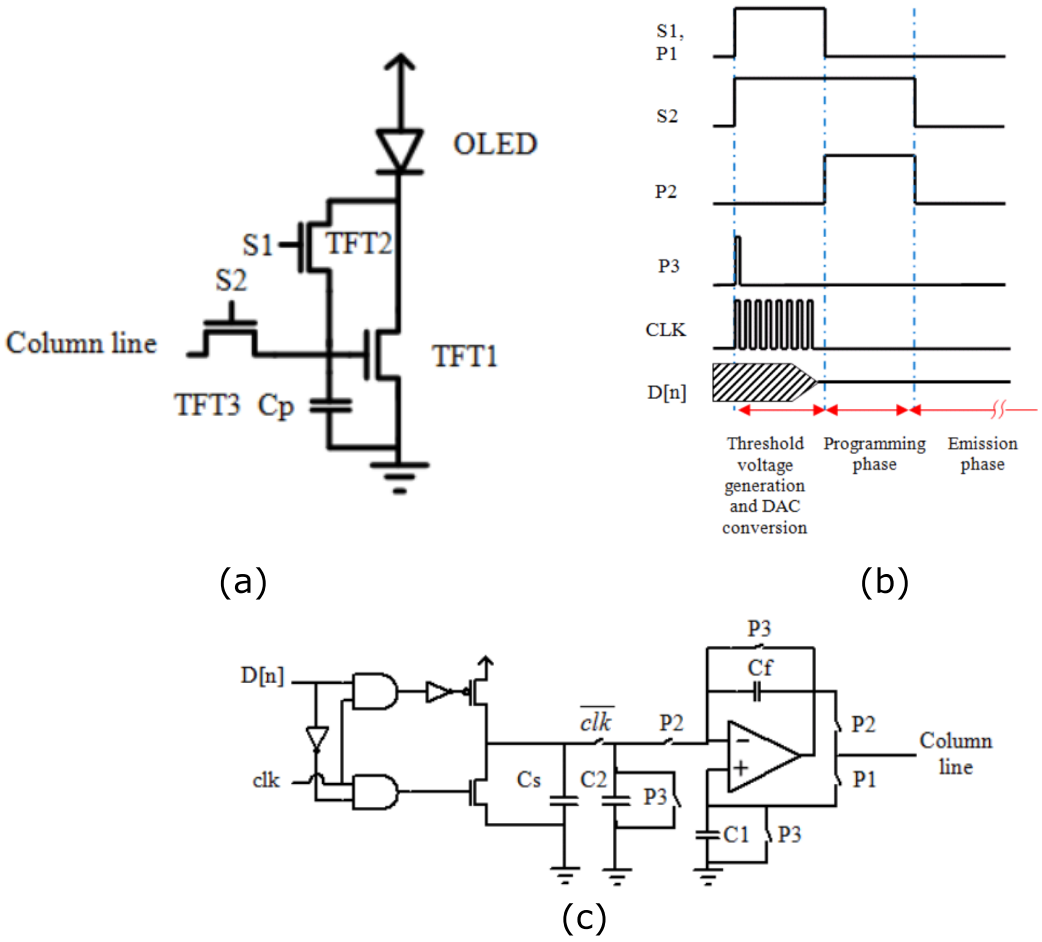


Figure 4.3: An external compensation method using (a) a 3T+1C pixel circuit. The control signals and off-panel IC schematic are shown in (b) and (c), respectively [60].

The operating principle of the proposed compensation scheme relies on the correct

generation and extraction of the threshold-voltage on the driving TFT (TFT_1). In the first phase of operation, both S_1 and S_2 switches are set to high so that TFT_1 is in a diode-connected mode. At the same time, the DAC is sampling the voltage on the column line which has a direct relationship with the threshold-voltage of TFT_1. As soon as the sampling phase ends, the DAC has obtained the threshold-voltage information and the weighted sum of the data voltage, threshold-voltage and the overdrive voltage of TFT_1. It then outputs this lumped sum voltage to the column line which subsequently programs the pixel circuit. The last phase is the emission in which the compensated data value has been stored on the capacitor, and the pixel is supplying the desired current to the LED.

The advantageous side of the external compensation method is that it could provide accurate output-current corrections for up to $5\,V$ of ΔV_T within a narrow variation of only 3% [60]. In addition, the simple 3T+1C pixel circuit with only two timing-control signals are also beneficial. However, there are several drawbacks about the scheme. First, the speed of operation is limited because the external DAC has to perform the sequence of sense-correct-program for every single pixel in a row of a display panel. For example, if a $60\,Hz$ RGB HD display with a resolution of 1920×1080 were to be compensated, there needs to be at least $1920 \times 3 = 5760$ sense-correct-program sequences carried out in a single display cycle of $16.67\,ms$ for a single row of tri-color pixels. The calculated sense-correct-program time for each pixel is less than $3\,\mu s$ which is a strict timing requirement for the external ICs. As a result, this scheme consumes a substantial amount of power due to its high operating speed. In addition, the V_{data} lines are being charged and discharged by serially connected transistors which may impact the speed and limit the refresh rate of the display. Moreover, threshold-voltage degradation may also occur on the other two TFTs in the pixel circuit causing inaccurate compensation.

In summary, the external compensation scheme could provide accurate output

current to a certain degree for pixels with high values of ΔV_T, but its scaling capability to accommodate higher resolution display panels is limited due to demanding off-panel hardware components, high power consumption and implementation complexity.

4.1.3 Compensation scheme - reverse annealing

Beside external compensation scheme, there are also several methods that use slightly complex pixel circuits to tackle the ΔV_T within each pixel. One of the methods uses a reverse annealing scheme to partially rectify the ΔV_T on the driving TFT.

Lee et al. has proposed a 6-TFT and 1-capacitor (6T+1C) pixel circuit using this concept [61]. The full pixel circuit and the timing-control signals are shown in Fig. 4.4(a) and (b), respectively. This pixel circuit uses a portion of the display cycle to apply a negative overdrive voltage on the driving TFT (T_3), in this case, a 2.7 ms recovery time has been taken off the full display cycle of 16.67 ms to facilitate the reverse annealing procedure.

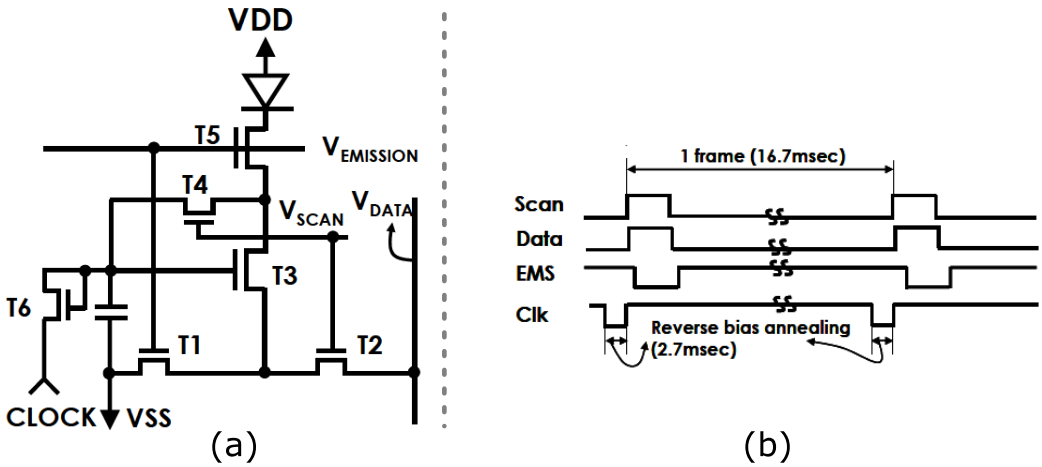


Figure 4.4: A reverse annealing compensation method [61] using (a) a 6T+1C pixel circuit. The control signals schematic shown in (b).

The ΔV_T behavior of a-Si:H TFTs have been well investigated and it is known that positive (negative) gate-bias stress will result in positive (negative) ΔV_T [53]. The 6T+1C pixel circuit exploits this idea. At the end of the emission phase, the external

clock signal applies a negative value lasting $2.7\,ms$ shown in 4.5(a). The resulting voltage-bias stress on the gate of the driving TFT is $-10\,V$ during the $2.7\,ms$.

After a 42-hour accelerated test, the result shows that the compensated output current could maintain approximately 70% of the original current while the uncompensated value dropped to 55% shown in 4.5(b). The measured threshold-voltage on the driving TFT has shifted by $0.48\,V$ compared to the uncompensated value of $0.75\,V$.

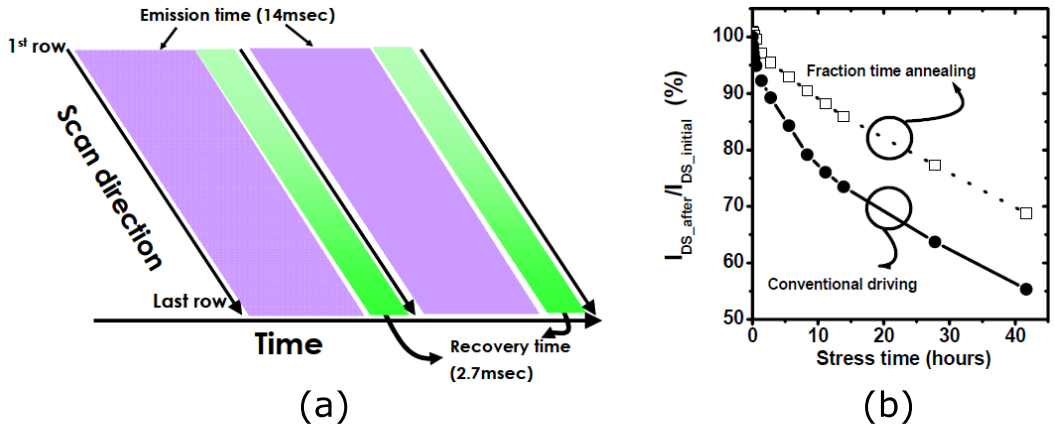


Figure 4.5: (a) The schematic of the reverse-annealing time frame with respect to the full display cycle. (b) The compensation performance by the reverse annealing compensation method [61]. The solid circles represent normalized output current degradation without compensation and the hollow squares are for reverse annealing method.

The benefit of the reverse annealing method is that the compensation is applied on the individual pixels. It does not involve complex external detection circuits. The shortcomings of this method is also obvious: the compensation could never fully recover all the ΔV_T because the reverse annealing is only slowing down the degradation on the TFT but not rectifying it. Furthermore, the loss of emission phase due to the required recovery period may cause flickering during display operation. Since the $2.7\,ms$ recovery time is a significant portion (16.2%) of the full display cycle, the pixel can not glow during this phase which may cause negative viewer experience.

Therefore, the reverse annealing compensation scheme attempts to solve the ΔV_T by slowing down the degradation of the driving TFT, however, it suffers from non-

optimal compensation performance and potentially poor viewer experience.

4.1.4 Compensation scheme - internal detection

Since the external detection method shows promising result at pixel level, there has been much efforts to incorporate the V_T detection within each pixel so that the dependence on external ICs could be potentially relieved.

Ashitiani et al. has proposed a 5-TFT and 1-capacitor (5T+1C) pixel circuit [55] with three timing-control signals to tackle the ΔV_T problem. The schematic and control signals are shown in Fig. 4.6(a) and (b), respectively.

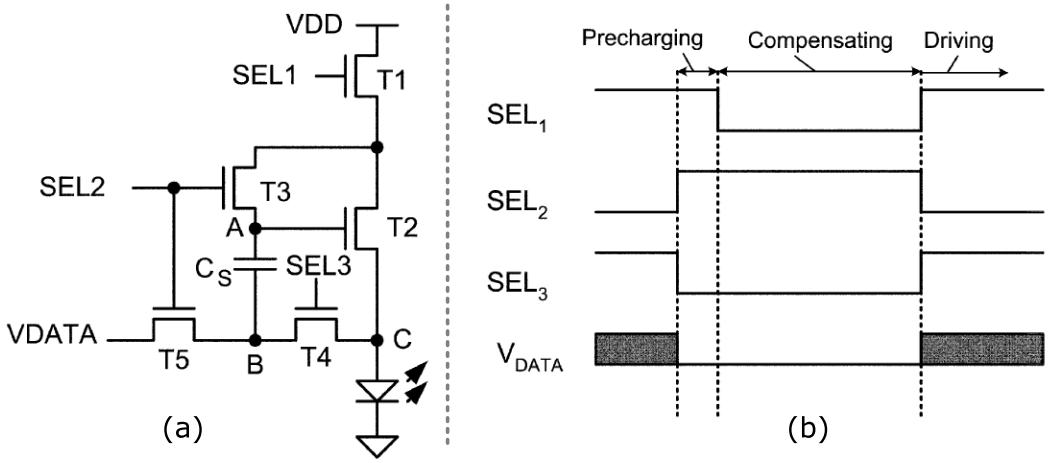


Figure 4.6: (a) The schematic and (b) timing-control signals of the 5T+1C pixel circuit engaging an internal V_T detection scheme [55].

This compensation scheme divides each display cycle into pre-charging, compensating, and driving/emitting phases. During pre-charging phase, the gate (node A) of the driving TFT (T_2) is charged close to V_{DD} while the data line voltage is also charged to the desired value. Then, in the compensating phase, T_2 is draining current in a diode-configured mode such that node A voltage eventually reaches around the threshold-voltage of T_2 ($V_{T,2}$). In the last phase, the sum of the data voltage and $V_{T,2}$ is pumped on to the gate of T_2 to achieve compensation. Since the ΔV_T of T_2 will constantly go up due to the operation of the pixel, the voltage at node A will also rise accordingly to mitigate the ΔV_T on T_2.

The transient node A voltage, output current and the compensation performance vs. increasing ΔV_T are shown in Fig. 4.7(a), (b) and (c). The node A voltage is able to rise according to the ΔV_T shown in Fig. 4.7(a) from $0\,V$ to $1\,V$. The overall compensation result also achieved a 90% output current retention rate with a $4\,V$ threshold-voltage shift.

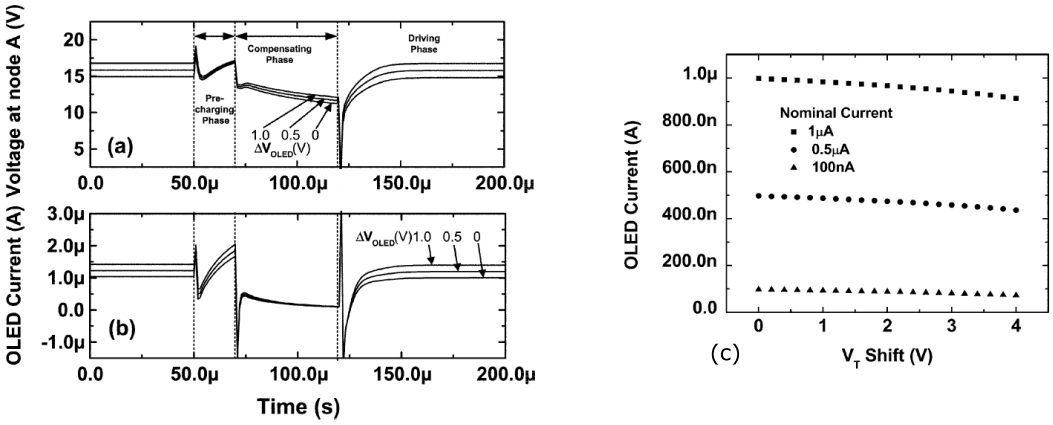


Figure 4.7: (a) The transient voltage at node A and (b) OLED current during a display cycle. (c) Compensation performance at different output current with increasing ΔV_T [55].

The internal detection compensation scheme has provided another approach to tackle the threshold-voltage shift. The advantages of this design is its self-contained nature and relative better compensation result because there is no need to involve additional circuitries to extract the threshold-voltage and the output current retention rate is higher than the reverse annealing method. However, the complex timing-control signals could be difficult to generate and the ΔV_T on T_1 is not accounted for which could also contribute to the non-ideal compensation results.

4.1.5 Compensation scheme - charge transfer

Beside the internal detection compensation method, Yang et al. has proposed another approach of a charge-transfer mechanism along with a 4-TFT (4T) pixel circuit with its three timing-control signals shown in Fig. 4.8(a) and (b), respectively.

The 4T pixel circuit uses a correlation between difference of ΔV_T in either linear

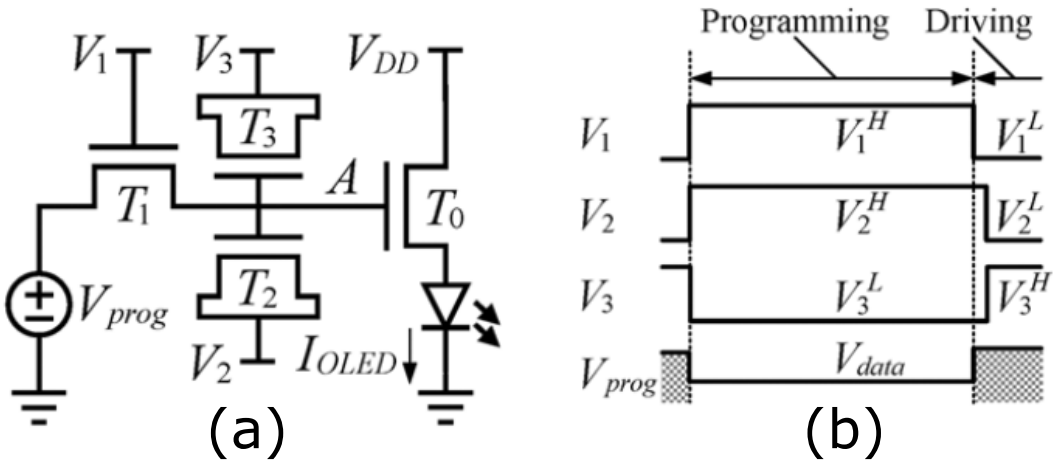


Figure 4.8: (a) The schematic and (b) timing-control signals of the charge-transfer 4T pixel circuit [46].

and saturation mode of a TFT to compensate the output current by raising voltage at node A. The simulated node A voltage and output current at different V_{data} are shown in Fig. 4.9(a) and (b), respectively. It can be seen that when ΔV_T rises from $0\,V$ to $5\,V$, node A voltage goes up accordingly to compensate.

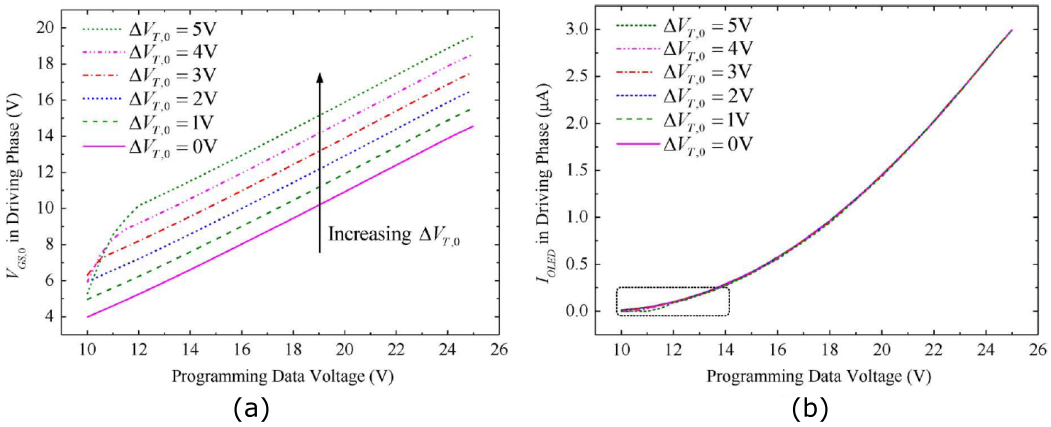


Figure 4.9: (a) The transient voltage at node A ($V_{GS,0}$) in the driving phase of a display cycle. (b) Compensation performance at different output current with increasing ΔV_T [46].

The charge-transfer method provides good compensation results. However, the complex timing-control signals and gaps in degradation between the two correlation TFTs are its disadvantages. The charge-transfer method leads to the proposed novel 6-TFT pixel circuit with simplified timing-control signals, which will be thoroughly introduced and analyzed in the next sections.

4.2 The proposed 6T pixel circuit and compensation method

Prior work discussed previously has laid out different pathways to the compensation of pixel circuits. The most effective method is the charge-transfer method, however, the 4T pixel circuit previously proposed by [46] has its deficiencies. To overcome those shortcomings, A novel 6T pixel circuit has been proposed to mitigate the impact of electrical instability of flexible a-Si:H TFTs based on the specific ratio of TFT degradation in linear and saturation modes [62]. It provides enhanced compensation performance through a self-compensating charge-transfer process. In addition, special consideration to the layout of TFTs has been given to ensure the correct behavior of the pixel circuit under different bending conditions. Furthermore, only a pair of timing signals is sufficient to control a row of such pixels, which reduces the complexity of external drivers compared to prior solutions [54, 55, 46] [1] .

4.2.1 Circuit operation

The schematic and control signals of the 6T pixel circuit are shown in Fig. 4.10(a) and (b), respectively. T_0 is the driving TFT that supplies current to the LED. Since the drain-cathode configuration has proven its feasibility, the μLED in this pixel circuit is placed in this method. The compensation TFT (T_2), which has its source and drain shorted to form a metal-insulator-semiconductor (MIS) capacitor, is connected between the gate and source terminals of T_0 electrically and provides compensation during the charge-transfer process. Another MIS capacitor (T_3) is used to store data prior to the emitting phase. The remaining TFTs (T_1, T_4, and T_5) are designed to act as switches. The control signal V_1 is the row-select signal which is the same as

[1] This chapter is an amended version of "A 6-TFT charge-transfer self-compensating pixel circuit for flexible displays", including modified figures and tables, by Q. Li, C.-H. Lee, M. Asad, W. S. Wong, M. Sachdev, published in Journal of the Electron Devices Society, with ©IEEE 2019

a conventional 2T pixel circuit. The only additional signal V_2 acts as a boost to pump charge to T_0. The operation of the pixel circuit is divided into two phases: programming and emitting, which are explained below.

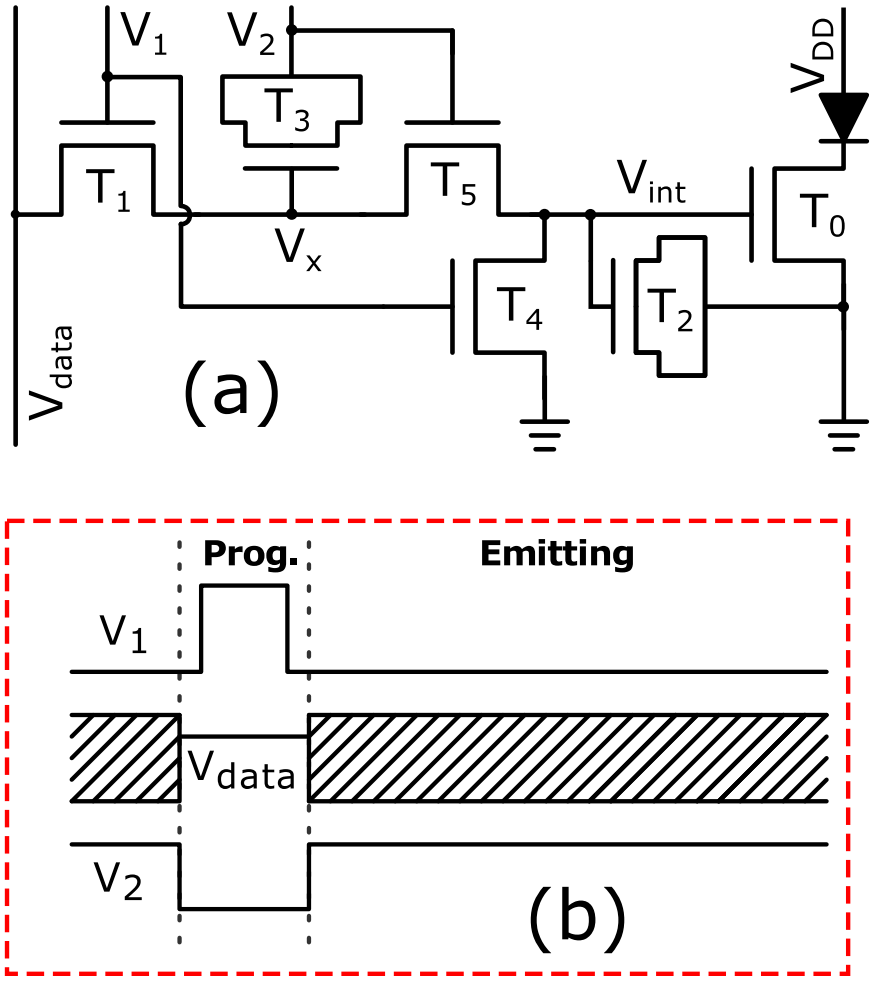


Figure 4.10: The (a) schematic and (b) control signals of the proposed 6T pixel circuit.

4.2.1.1 The programming phase

In the programming phase shown in Fig. 4.11, control signal V_2 is set to low first so that T_5 is in high impedance mode which isolates the internal node V_{int} from the constantly toggling V_{data} line. At the same time, the gate voltage (V_x) of the storage capacitor T_3 is lowered and waiting for the new V_{data} to arrive. After a short delay, which is necessary to eliminate a V_{data} and ground short situation, V_1 is set to high

such that T_1 and T_4 are conducting. As a result, the V_{int} node is drained through T_4 to clear the brightness level information from the previous display cycle. When V_{int} reaches zero, T_0 is shut off and no current is flowing through the μLED. Then, there will be no residual luminescence impact from the previous display cycle. Meanwhile, T_3 has acquired charge based on the new V_{data} value through T_1. In this phase, the reset of previous state and the acquisition of the new data are carried out without any cross-talk to neighboring pixels and power/ground rails.

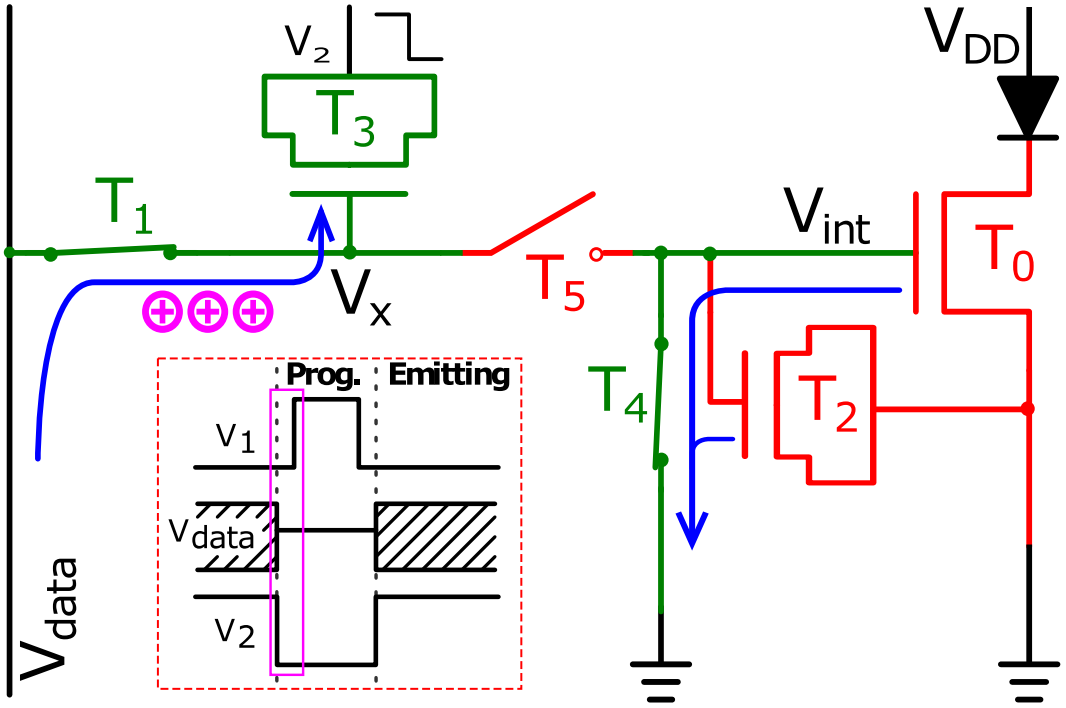


Figure 4.11: The switching behavior of TFTs and charge flow in the 6T pixel circuit in the programming phase. TFTs shown in red are turned off and shown in green are on. The charge flow is shown with blue arrows.

4.2.1.2 The emitting phase

After the programming phase ends, the pixel enters the emitting phase, shown in Fig. 4.12, by switching the polarity of control signals V_1 and V_2 sequentially. This operation makes T_1 and T_4 in high impedance mode and T_5 conducting. Consequently, V_{int} is isolated from the interference of the toggling V_{data} signal and ground. Then,

the majority of the charge on T_3 is injected to V_{int} and is stored on T_2, while a small portion is shared among parasitic capacitances of other TFTs.

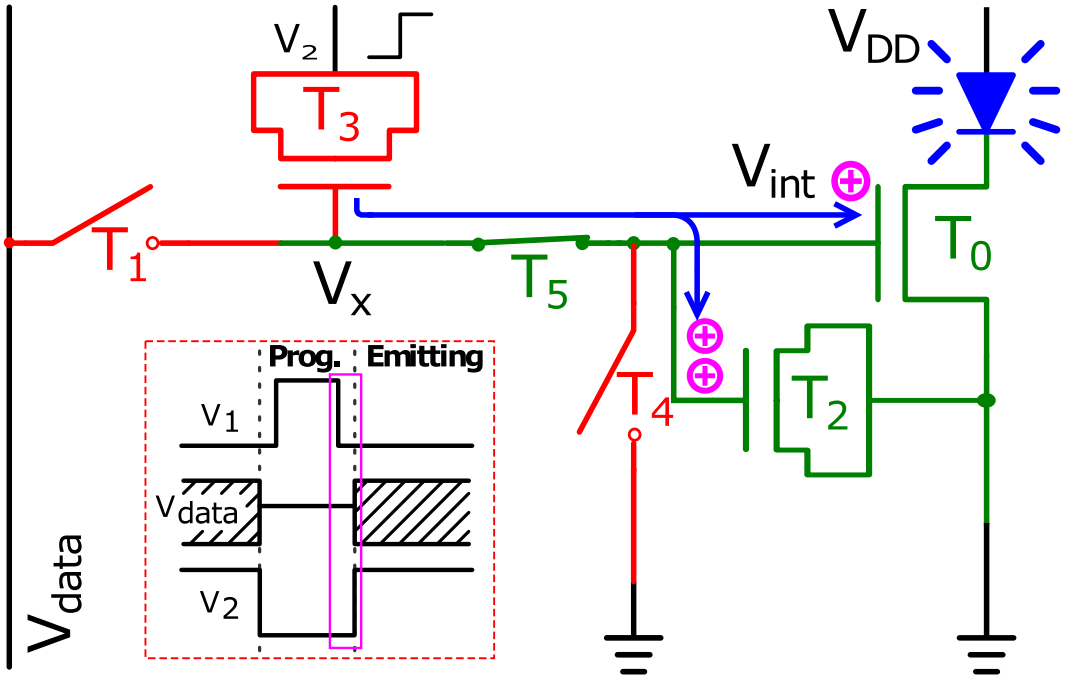


Figure 4.12: The switching behavior of TFTs and charge flow in the 6T pixel circuit in the emitting phase. TFTs shown in red are turned off and shown in green are on. The charge flow is shown with blue arrows.

4.2.1.3 The charge-transfer self-compensating mechanism

The self-compensating charge-transfer mechanism of the proposed 6T pixel circuit is governed by balancing charge components and utilizing the ΔV_T ratio between T_2 and T_0. In the following analysis, the μLED is neglected to ease the calculation because it has negligible impact on the compensation capability of the pixel circuit.

The derivation is to demonstrate that under the same V_{data} voltage, the pixel circuit is always providing the constant current to the μLED in spite of increasing $\Delta V_{T,0}$ conditions. Since the μLED only glows in the emitting phase, all charge equations are based on transistor behaviors in this phase.

In the emitting phase, T_2 is operating in linear mode and T_0 in saturation mode, so that before any long-term voltage-bias stress (ΔV_T has not occurred and all TFTs

are in their fresh state), the initial charge components in the channels of T_2 and T_0 are expressed as:

$$Q_{ch,2}^{initial} = C_{ch,2} \times (V_{int}^{initial} - V_{T,2}) \tag{4.2}$$

$$Q_{ch,0}^{initial} = \frac{2}{3} C_{ch,0} \times (V_{int}^{initial} - V_{T,0}) \tag{4.3}$$

In the above equations, $Q_{ch,2}^{initial}$ and $Q_{ch,0}^{initial}$ are the total charge in the channel of T_2 and T_0 at their initial state, respectively. $C_{ch,2}$ and $C_{ch,0}$ are the channel capacitance of these two TFTs. The applied gate-source voltage and initial threshold-voltages are expressed as $V_{int}^{initial}$ and $V_{T,2}$, $V_{T,0}$, respectively.

After the pixel circuit has been operated under voltage-bias stress, both T_2 and T_0 are degrading due to the disordered nature of the amorphous material [42, 59]. Consequently, the degradation causes ΔV_T on both T_2 and T_0. After biased-induced stress, the resulting new channel charge equations become:

$$Q_{ch,2}^{stressed} = C_{ch,2} \times (V_{int}^{stressed} - V_{T,2} - \Delta V_{T,2}) \tag{4.4}$$

$$Q_{ch,0}^{stressed} = \frac{2}{3} C_{ch,0} \times (V_{int}^{stressed} - V_{T,0} - \Delta V_{T,0}) \tag{4.5}$$

The degradation of T_2 and T_0 still follows the correlation rule [62], where the degradation of a TFT in linear mode is 1.5 times faster than saturation mode when the gate bias voltage is the same. The correlation is then expressed as:

$$\Delta V_{T,2} = \frac{3}{2} \Delta V_{T,0} \tag{4.6}$$

To achieve the self-compensating mechanism, $V_{int}^{stressed}$ should rise by the amount of $\Delta V_{T,0}$ from $V_{int}^{initial}$ automatically in the emitting phase. This relationship is expressed

as:

$$V_{int}^{stressed} = V_{int}^{initial} + \Delta V_{T,0} \tag{4.7}$$

In order to realize the above relationship, the geometry of all TFTs needs to be designed correctly by balancing charge components in the emitting phase. As a result, all the parasitic overlap capacitance that affects V_{int} node has to be also taken into account. The capacitor network in the emitting phase is shown in Fig. 4.13. It is assumed that the on-state of signal V_2 is equal to the supply voltage V_{DD}. The channel capacitance of T_5 is also neglected because its channel length is designed as minimum size to allow a fast charge-transfer from the programming to the emitting phase. It is also assumed that the possible degradation of T_5 has minimal impact on the compensation due to its small channel region comparing to T_2.

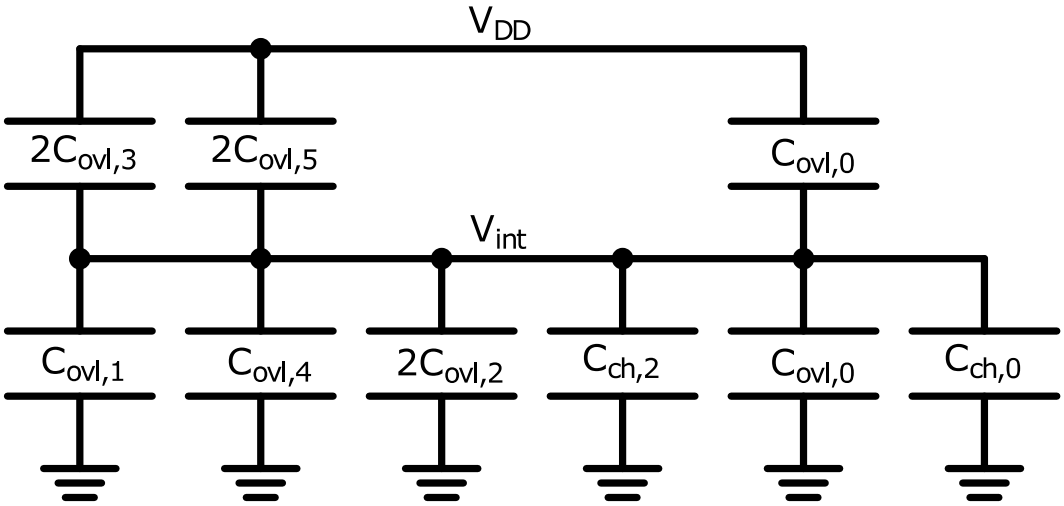


Figure 4.13: The channel and overlap capacitances that share charge in the emitting phase.

All the overlap capacitances between V_{DD} and V_{int} ($C_{ovl,top}$) from Fig. 4.13 are expressed as:

$$C_{ovl,top} = C_{ovl,0} + 2C_{ovl,3} + 2C_{ovl,5} \tag{4.8}$$

In addition, all the overlap capacitances between V_{int} and ground ($C_{ovl,bottom}$) from

Fig. 4.13 are expressed as:

$$C_{ovl,bottom} = C_{ovl,0} + C_{ovl,1} + 2C_{ovl,2} + C_{ovl,4} \tag{4.9}$$

According to the law of charge conservation, the charge equations in the top and bottom capacitor network are expressed as:

$$\begin{aligned} C_{ovl,top} \times (V_{DD} - V_{int}) &= C_{ovl,bottom} \times V_{int} \\ &\quad + Q_{ch,2} + Q_{ch,0} \end{aligned} \tag{4.10}$$

$$\begin{aligned} C_{ovl,top} \times V_{DD} &= (C_{ovl,top} + C_{ovl,bottom}) \times V_{int} \\ &\quad + Q_{ch,2} + Q_{ch,0} \end{aligned} \tag{4.11}$$

It is assumed that only the channel capacitances are affected by the threshold-voltage but not the overlap. Also, due to the close proximity of T_2 and T_0 on the layout, their initial threshold-voltages $V_{T,2}$ and $V_{T,0}$ are assumed equal. After substituting Eqs. (4.2) and (4.3) into in Eq. (4.11), the initial charge balance before any bias-stress can be expressed as:

$$\begin{aligned} C_{ovl,top} \times V_{DD} &= (C_{ovl,top} + C_{ovl,bottom}) \times V_{int}^{initial} \\ &\quad + C_{ch,2} \times (V_{int}^{initial} - V_{T,0}) \\ &\quad + \frac{2}{3} C_{ch,0} \times (V_{int}^{initial} - V_{T,0}) \end{aligned} \tag{4.12}$$

After substituting Eqs. (4.4), (4.5), and (4.6) into Eq. (4.11), the charge-balance

Eq. after the bias-stress of the pixel circuit, becomes:

$$\begin{aligned} C_{ovl,top} \times V_{DD} = (C_{ovl,top} + C_{ovl,bottom}) \times V_{int}^{stressed} \\ + C_{ch,2} \times (V_{int}^{stressed} - V_{T,0} - \frac{3}{2}\Delta V_{T,0}) \\ + \frac{2}{3}C_{ch,0} \times (V_{int}^{stressed} - V_{T,0} - \Delta V_{T,0}) \end{aligned} \tag{4.13}$$

A new relationship after substituting Eqs. (4.12) and (4.13) into Eq. (4.7), is then obtained, which describes the relationship between capacitors. It is expressed as:

$$\frac{1}{2}C_{ch,2} = C_{ovl,top} + C_{ovl,bottom} \tag{4.14}$$

$$\begin{aligned} \frac{1}{2}C_{ch,2} = 2C_{ovl,0} + C_{ovl,1} + 2C_{ovl,2} \\ + 2C_{ovl,3} + C_{ovl,4} + 2C_{ovl,5} \end{aligned} \tag{4.15}$$

Here, Eq. (4.15) indicates that the geometry of the compensating TFT (T_2) is determined by the sum of overlap capacitances in TFTs (T_0, T_1, T_2, T_3, T_4, and T_5). Then, the capacitance values are substituted by the widths and lengths of relevant TFTs. In addition, the process parameters including the unit-square sheet capacitance of the channel (C_{ch}) and the overlap capacitance (C_{ovl}) are inserted in the Eq. (4.15). Lastly, the minimum overlap length L_{ovl} is dictated by the fabrication process.

The relationship of capacitances shown in Eq. (4.15) is expressed as the channel width and length (W and L) of TFTs shown below:

$$\begin{aligned} \frac{1}{2}C_{ch,2} = 2W_0L_{ovl} + W_1L_{ovl} + 2W_2L_{ovl} \\ + 2W_3L_{ovl} + W_4C_{ovl} + 2W_5L_{ovl} \end{aligned} \tag{4.16}$$

$$\begin{aligned} \frac{1}{2}W_2L_2C_{ch} = 2W_0L_{ovl} + W_1L_{ovl} + 2W_2L_{ovl} \\ + 2W_3L_{ovl} + W_4C_{ovl} + 2W_5L_{ovl} \end{aligned} \tag{4.17}$$

The simplified Eq. (4.18) below serves the purpose to determine the sizes of TFTs in the 6T pixel circuit.

$$W_2 = \frac{2C_{ovl}(2W_0 + W_1 + 2W_3 + W_4 + 2W_5)}{\frac{C_{ch}L_2}{L_{ovl}} - 4C_{ovl}} \tag{4.18}$$

The mathematical analysis has suggested that, with correct sizing, the circuit is capable to maintain the ΔV_T of correlating T_2 and T_0 with a shift of the fixed 3 : 2 ratio. Therefore, the self-compensating mechanism is achieved by raising V_{int} with an amount equal to $\Delta V_{T,0}$ in the emitting phase. As a result, the output current is not affected by the bias-induced degradation of a-Si:H TFTs. The following sections will demonstrate the effectiveness of the pixel circuit with SPICE simulations.

4.2.2 Circuit simulation

In order to simulate the charge behavior of a-Si:H TFTs under various ΔV_T values, the conventional level-61 HSPICE model is not suitable because it is predominantly based on the current-voltage relationship. Then, a modified charged-based level-61 a-Si:H TFT model [46, 57] was developed to simulate the behavior of the 6T pixel circuit with increasing electrical instability. The circuit and its test-bench have been implemented in Cadence Virtuoso environment with parameters listed in Table 4.1. The process parameters (μ_{eff}, C_{ch}, and C_{ovl}) were obtained by extracting data from current-voltage (I-V) and capacitance-voltage (C-V) curves of test TFTs with known geometries. The L_{ovl} was set to 5 μm according to the foundry specification. The W/L of T_0 was set to 100 μm/20 μm as a reference to size all other TFTs. Switches T_4 and T_5 were chosen to be 25 μm/20 μm and 25 μm/10 μm, respectively, to minimize the pixel area guided by Eq. (4.18). Then, the size of T_2 was calculated to be 99.2 μm/100 μm, so that it was set to be 100 μm/100 μm. Lastly, T_3 was chosen to match the size of

T_2 to restore charge needed by T_2 in the emitting phase. Note that the maximum V_{data} needs to be less than the difference between the on-state of V_2 and the V_T of T_5 ($V_2^{high} - V_{T,5} = V_{DD} - V_{T,5}$). This condition was to guarantee that the V_{data} is always fully transferred onto V_{int} in the emitting phase without being clipped off by the threshold-voltage of T_5.

Table 4.1: Device and process parameters used in the simulation

Parameter	Value	Parameter	Value
$W_0/L_0\,(\mu m/\mu m)$	100/20	$V_{data}\,(V)$	$5 \sim 15$
$W_1/L_1\,(\mu m/\mu m)$	50/20	$V_{DD}\,(V)$	20
$W_2/L_2\,(\mu m/\mu m)$	100/100	$V_1\,(V)$	$0 \sim 20$
$W_3/L_3\,(\mu m/\mu m)$	100/100	$V_2\,(V)$	$20 \sim 0$
$W_4/L_4\,(\mu m/\mu m)$	25/20	$\mu_{eff}\,(cm^2/Vs)$	1.0
$W_5/L_5\,(\mu m/\mu m)$	25/10	$C_{ch}\,(fF/\mu m^2)$	0.16
$L_{ovl}\,(\mu m)$	5	$C_{ovl}\,(fF/\mu m^2)$	0.22

4.2.2.1 Functional simulation of the 6T pixel circuit

First, to investigate the effectiveness of the self-compensating circuit on a flat substrate without any applied mechanical strain, $\Delta V_{T,2}$ was varied from $0\,V$ to $4.5\,V$ and $\Delta V_{T,0}$ from $0\,V$ to $3\,V$ to represent increasing electrical instability of the correlating TFTs while maintaining the $3:2$ ratio. Fig. 4.14(a) has demonstrated the rise of V_{int} voltages when $\Delta V_{T,0}$ and $\Delta V_{T,2}$ are applied under the entire data range. The incremental V_{int} at each V_{data} is always $\sim 1\,V$ as desired. Using $V_{data} = 12\,V$ as an example shown in Fig. 4.14(b), the initial V_{int} before any stress is $10.42\,V$. After $3\,V$ of $\Delta V_{T,0}$ is applied, the resulting V_{int} is equal to $13.39\,V$ which is $2.97\,V$ (99%) compared to the expected voltage rise of $3\,V$.

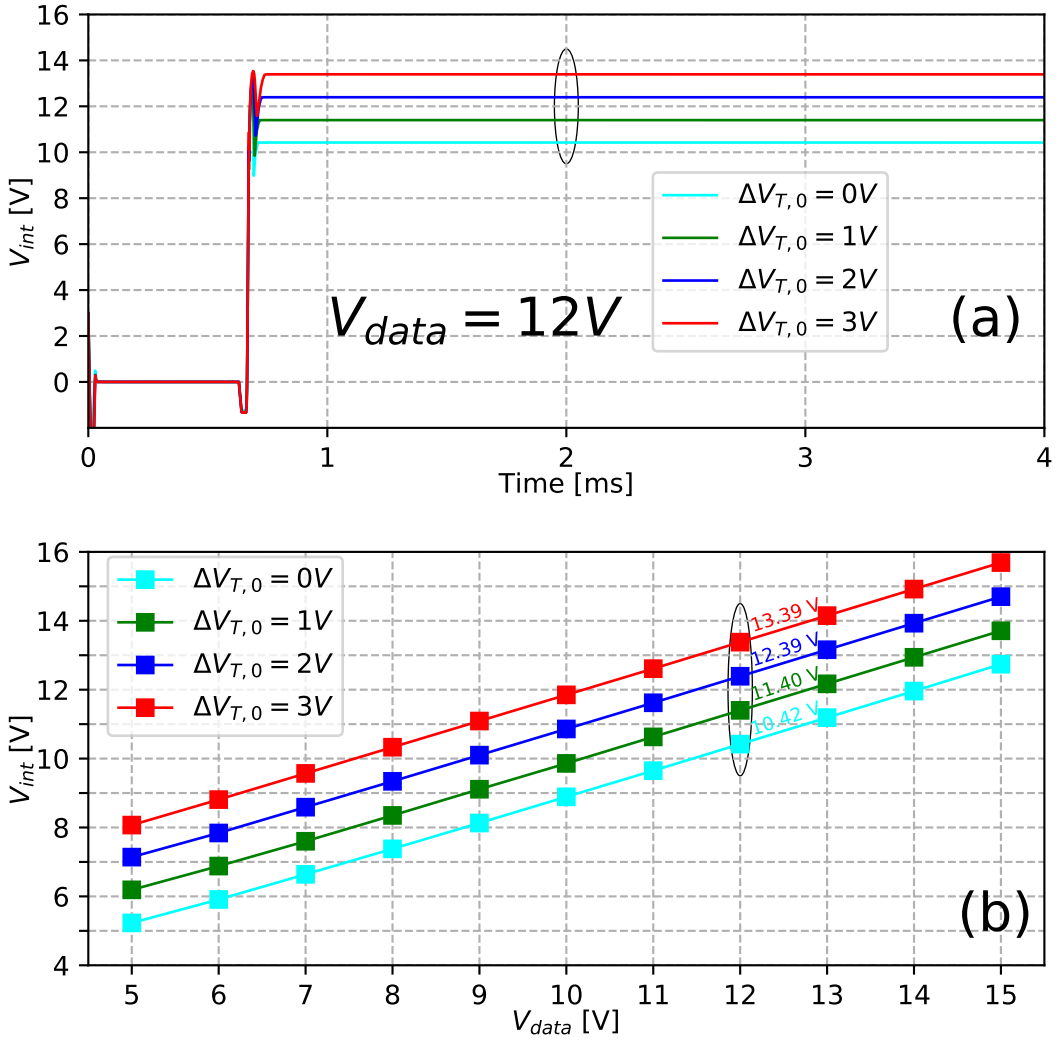


Figure 4.14: (a) The voltage of V_{int} of the 6T pixel circuit with increasing $\Delta V_{T,0}$ from $0\,V$ to $3\,V$ in the entire range of V_{data}. The circled dots with corresponding values represent the V_{int} values at $V_{data} = 12\,V$ with increasing $\Delta V_{T,0}$. (b) The transient waveform of V_{int} when $V_{data} = 12\,V$ under increasing $\Delta V_{T,0}$ from $0\,V$ to $3\,V$.

Next, the output current was simulated. The transient waveform of the output current in the entire V_{data} range is shown in Fig. 4.15(a). In addition, the extracted output current is normalized under each V_{data} point and summarized in Fig. 4.15(b). The simulation results indicated that the output current in the entire data range was able to retain more than 96% of its initial value with the worse case $\Delta V_{T,0} = 3\,V$. Therefore, the simulation results have demonstrated closely matched output current under increasing ΔV_T in the entire range of V_{data} proving the effectiveness of the

charge-transfer compensation method.

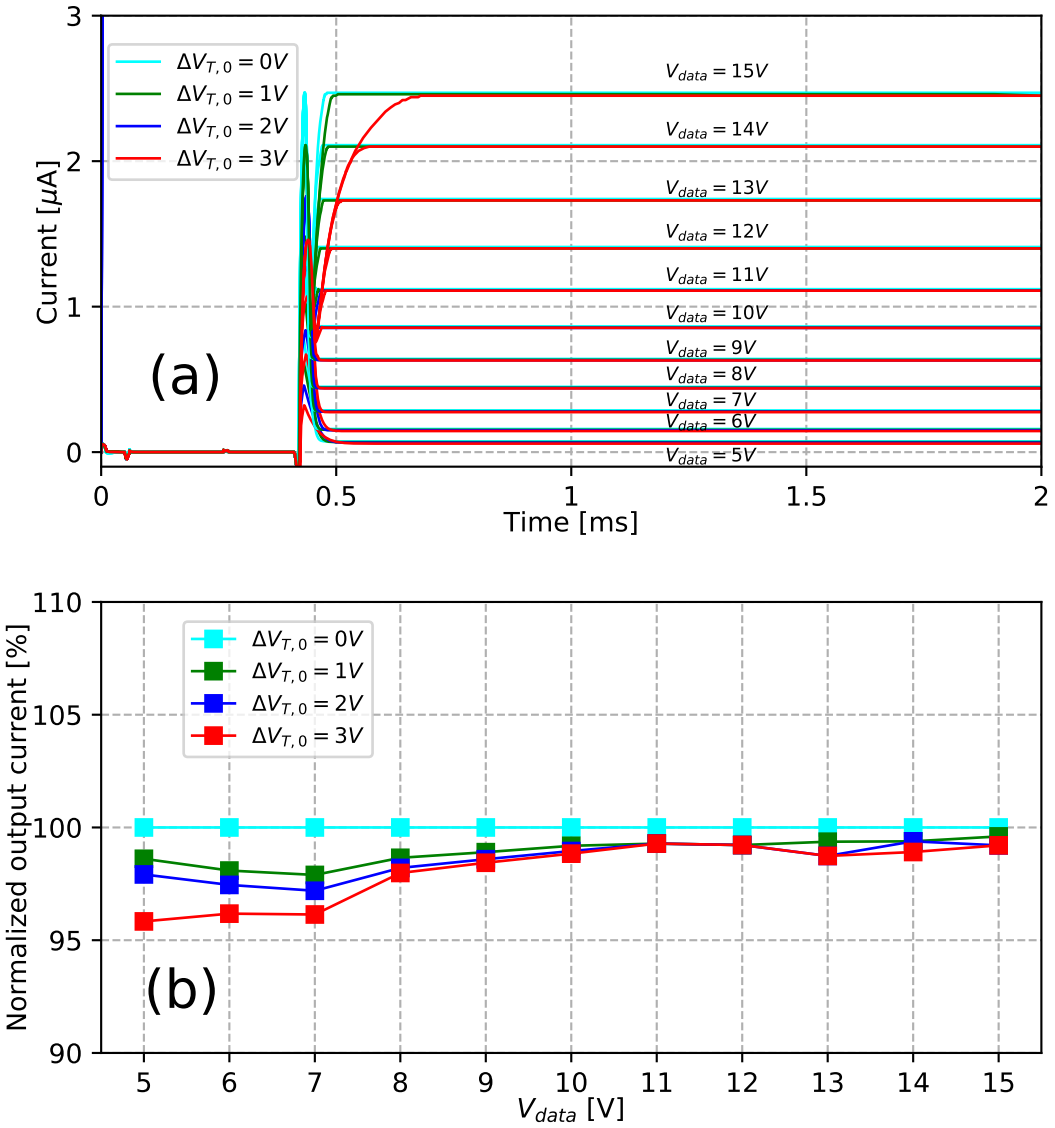


Figure 4.15: (a) The transient waveforms of the 6T pixel circuit under the entire range of V_{data}. The first 2 ms of a display cycle is shown. (b) The normalized output current in the V_{data} range under increasing $\Delta V_{T,0}$

By further investigating Eq. 4.18, it also indicates that only the channel capacitance of T_2 ($C_{ch,2}$) contributes to the overall compensation because of its V_T dependence and the rest of the gate capacitance, overlap capacitances, act as parasitic which should be minimized. Since switching TFTs (T_4 and T_5) are already set as the minimum, there exists another design parameter on the width and length ratio of

T_2, i.e. the total channel capacitance vs. the overlap capacitance which is capable of altering the compensation capability. Assume all the TFTs except T_2 maintain their geometries and only the width and length of T_2 vary, the compensation should perform better with a higher $C_{ch,2}/C_{ovl,2}$ ratio. The simulation results are summarized in Table. 4.2. Note that the initial output current is $2.52\,\mu A$ before any stress. Fig. 4.16 also demonstrates the results that with increasing W/L ratio of T_2 the compensation rises as expected to be over 100%. Therefore, this ratio could also be a design variable when considering the layout of the pixel circuit. For instance, when the ratio is 50, the pixel circuit can over-compensate by almost 8%. As a result, if the device floor-plan of the pixel circuit allows a long channel but short width T_2 structure, such configuration can be used to reduce the overall pixel area achieving higher fill factor.

Table 4.2: Comparison of compensation with different geometries of T_2.

T_2 Width (μm)	200	100	80	50	40	25	20
T_2 Length (μm)	50	100	125	200	250	400	500
Ratio of $C_{ch,2}/C_{ovl,2}$	5:1	10:1	12.5:1	20:1	25:1	40:1	50:1
Output current (μA) at $\Delta V_{T,0} = 1\,V$	2.43	2.51	2.52	2.55	2.56	2.58	2.58
Output current (μA) at $\Delta V_{T,0} = 2\,V$	2.37	2.51	2.54	2.59	2.61	2.64	2.65
Output current (μA) at $\Delta V_{T,0} = 3\,V$	2.31	2.50	2.55	2.63	2.66	2.71	2.72

Moreover, Eq. 4.18 also provides information on L_{ovl} in terms of downsizing TFTs. If a less overlap or a self-aligned process is available, the size of pixel TFTs , particularly T_2 and T_3 which are the largest TFTs in the pixel circuit, can be reduced. As

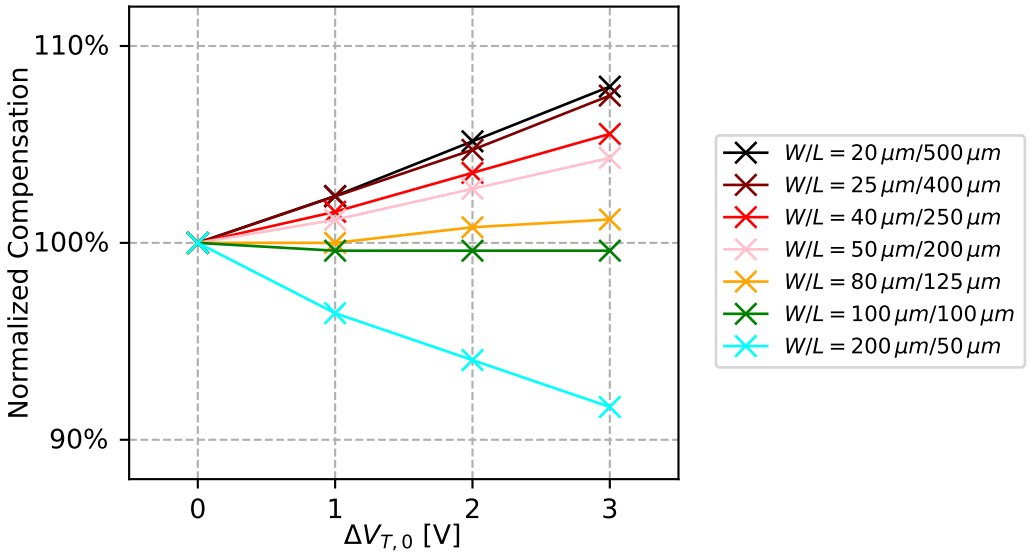


Figure 4.16: Normalized compensation with various geometries of T_2. The x-axis represents $\Delta V_{T,0}$ on the driving TFT. The color gradient of the lines from dark to light represents increasing W/L ratio or decreasing $C_{ch,2}/C_{ovl,2}$ ratio.

a result, a reduction in size can shrink the area occupied by the pixel circuit, thereby achieving a better fill factor and a higher display resolution.

All the above analysis and simulation have provided a thorough understanding of the operation and compensation capability of the 6T pixel circuit. The circuit is able to maintain an output current that retains more than 97% of the original value on a flat substrate with a very high ΔV_T of $3\,V$. Next, the performance of the pixel circuit under applied mechanical strain will be investigated.

4.2.2.2 The impact of mechanical strain

Previous reports [63, 56] have shown that, under tensile strain, the TFTs have slightly higher carrier mobility and much slower bias-induced degradation. On the other hand, when the TFTs are bent under compressive strain, they have slightly lower mobility and relatively faster bias-induced degradation.

Such behavior of the TFT under bending could be explained by the defect-creation model where the external strain is relieving or deteriorating the weak Si-Si bonds

[56, 64]. Several reports [57, 58, 64] have further investigated the impact of orientation of TFTs under the applied mechanical strain. It has been found that when the bending direction is parallel to the current flow, *i.e.* the TFT length direction, the impact of bending is at the highest, especially to the long-term biased-induced instability. When the bending direction is perpendicular to the current flow, the impact of mechanical strain is relatively less. As such, the layout of the pixel circuit should be given special consideration such that the correlating T_2 and T_0 are required to be in the same orientation and placed in close proximity. In this way, both TFTs experience the same mechanical strain so that their relative degradation ratio of $3:2$ will be always maintained.

Then, to simulate the impact of mechanical strain onto the flexible substrate, a higher $\Delta V_{T,0}$ value of $4\,V$ was chosen to represent a compressive stress and a lower $\Delta V_{T,0}$ value of $2\,V$ was chosen to represent a tensile stress. The mobility of the TFTs was also slightly adjusted due to bending. When placed under tensile strain, 0.3% is added to the TFT mobility, and when under compressive strain, 0.3% is subtracted from the original value [63, 64]. In order to maintain the desired correlation between $\Delta V_{T,2}$ and $\Delta V_{T,0}$, both T_2 and T_0 were assumed to have the same orientation and placed in close proximity in the layout. Therefore, their degradation could still have the $3:2$ relationship. The pixel circuit was able to maintain $\sim$ 96% of its initial current under tensile and compressive stain tests shown in Fig. 4.17.

Additionally, simulations with T_2 and T_0 having perpendicular orientation were conducted: the strain was applied in parallel to the length direction of T_0 and perpendicular to the length of T_2. When tensile strain was applied, the pixel circuit exhibited over-compensation, showing that the output current was $\sim$ 112% compared to the initial value shown as the green dashed line in Fig. 4.17. This is due to $\Delta V_{T,2} : \Delta V_{T,0} > 3:2$, so that T_2 was providing more charge which raised V_{int} higher than expected. On the other hand, when compressive strain was applied, the pixel

circuit demonstrated under-compensation. The output current only retained $\sim 92\%$ of its initial value due to $\Delta V_{T,2} : \Delta V_{T,0} < 3 : 2$ shown in as the brown dashed line in Fig. 4.17. The reason is that T_2 provided insufficient charge during the emitting phase, so that $V_{int}^{stressed}$ did not reach the correct value.

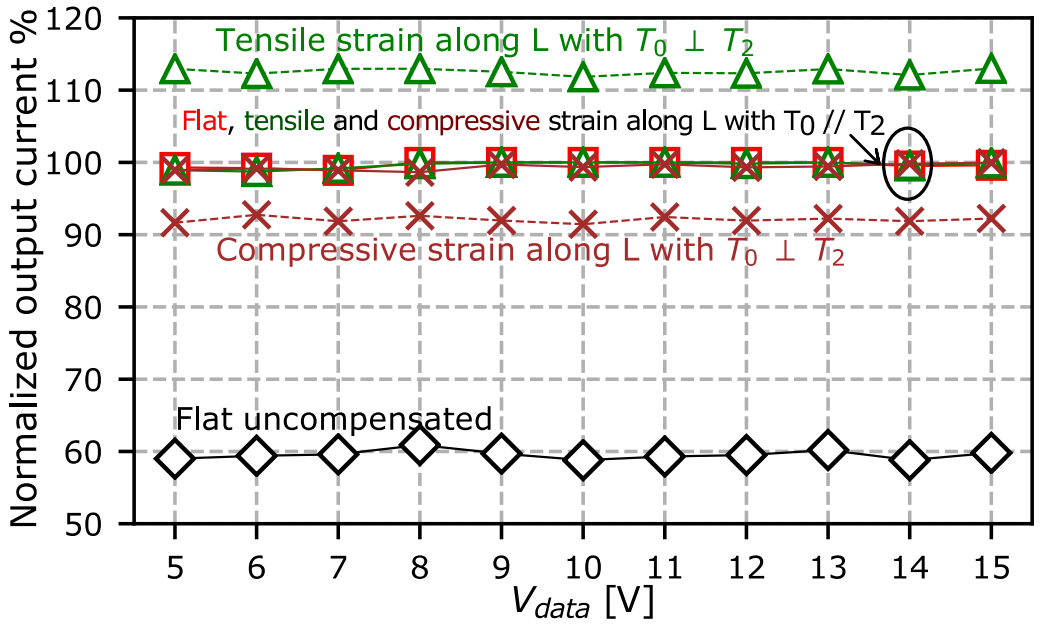


Figure 4.17: The simulation of normalized output current of the 6T pixel circuit in the entire V_{data} range under various bending conditions. The red, green, and brown solid lines show the compensation percentages under flat, tensile strain, and compressive strain conditions, respectively, when T_0 and T_2 are placed in parallel. The green and brown dashed lines represent the compensation under tensile and compressive strains, respectively, when T_0 and T_2 are placed perpendicularly. The black line shows a pixel circuit without compensation when placed flat.

The behavior of TFTs under mechanical bending is closely related to the initial strain of the a-Si:H semiconductor layer after its deposition. In this work, the initial strain of the TFT channel layer is compressive, so an applied tensile strain would cause the mobility of the TFT to rise and vise versa. However, if the initial strain of the TFT channel layer is tensile, the applied bending may cause a completely opposite result. Therefore, the effect of mechanical strain on TFT behaviors can not be generalized for all flexible circuits, it is dependent on the initial state of the film.

4.2.3 Fabrication and measurement results

The 6T pixel circuits were fabricated using the conventional 5-mask back-channel-etched (BCE) a-Si:H TFT process on flexible 3-inch polyethylene naphthalate (PEN) substrates at the maximum process temperature of $170°C$ [57]. The cross-sectional schematic of the fabricated a-Si:H TFT is shown in Fig. 4.18(a). Before the full TFT process began, a 500 nm a-SiN$_x$:H buffer layer was deposited on top of the PEN wafer to suppress out-diffusion from the substrate and minimize stress-induced strain deformation of the substrates that improved the adhesion of the TFT layers to the PEN. The device processing began with a 70 nm Mo deposition at room temperature by DC-sputtering on top of the 500 nm a-SiN$_x$:H buffer layer. Then the Mo layer was patterned to form the gate metal of all the TFTs. Afterwards, a tri-layer of 350 nm a-SiN$_x$:H gate dielectric, 200 nm a-Si:H channel, and 40 nm n^+ a-Si:H source/drain ohmic contact layer was sequentially deposited at $170°C$ using 13.56 MHz plasma-enhanced chemical-vapor deposition (PECVD) system.

After fabrication, the measured I_{DS} vs. V_{GS} curves are captured by pulsing a combination of Keithley 2430 and 6400 femto-amp source meters. The results are shown in Fig. 4.18(b). The test TFT showed carrier mobility (μ_{eff}) of $\sim 1\,cm^2/Vs$, sub-threshold slope (SS) $\sim 0.76\,V/dec$, and $V_T \sim 2.5\,V$.

4.2.4 Characterization of TFT stability under bending

The voltage-biased bending experiments of individual TFTs with four different modes have been conducted for three hours. The TFT was placed in tensile or compressive strain as well as in parallel or perpendicular to the length direction shown in Fig. 4.18(c). The output current was logged periodically and the result was compared with a flat TFT as reference.

The normalized drain-source current (I_{DS}) of test TFTs with the same geometry ($W/L = 100\,\mu m/20\,\mu m$) under four bending modes in saturation ($V_{DS} = 20\,V$ and

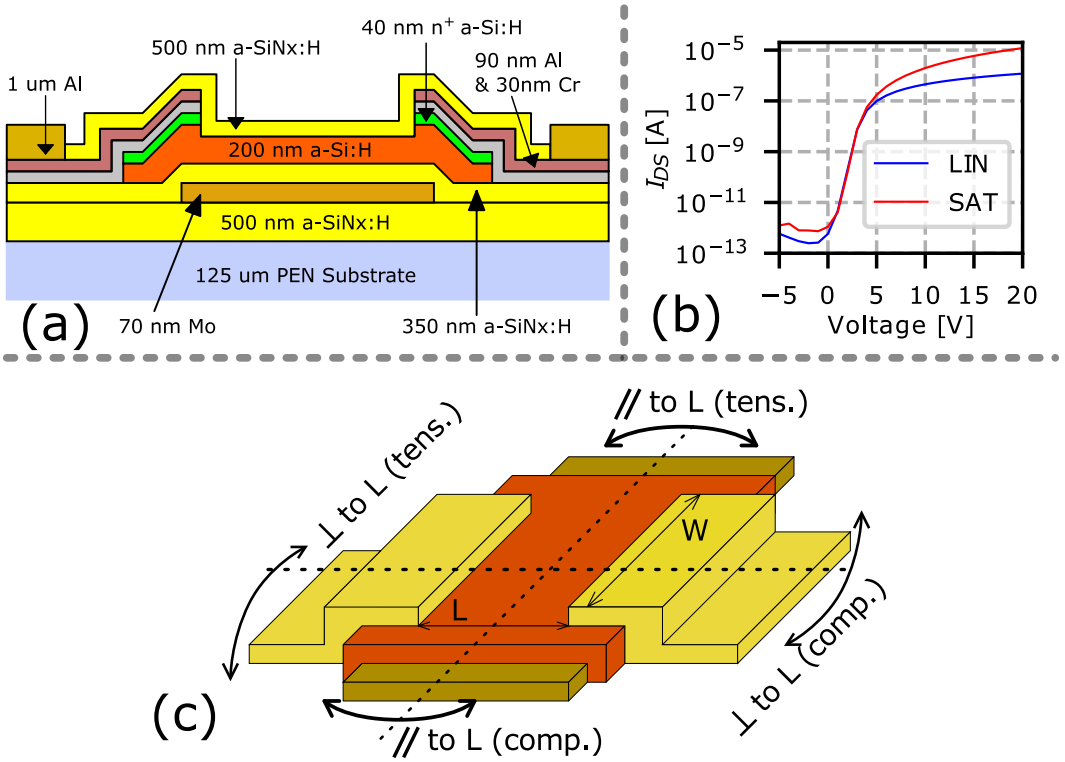


Figure 4.18: (a) The cross-section schematic of the TFT on flexible PEN substrate, (b) The I_{DS} vs. V_{GS} curves of the TFT ($W/L = 100\,\mu m/20\,\mu m$) in linear ($V_{DS} = 1\,V$) and saturation ($V_{DS} = 20\,V$) modes when laid flat, and (c) The schematic of various mechanical strain conditions applied to the TFT.

$V_{GS} = 20\,V$) or linear ($V_{DS} = 1\,V$ and $V_{GS} = 20\,V$) voltage-bias condition is shown in Fig. 4.19. The bending radius was $\approx 40\,mm$ over the PEN substrate with a thickness of $\sim 130\,\mu m$, so that the calculated strain was $\varepsilon = \pm 0.3\%$. TFTs under tensile strain showed lower bias-induced degradation compared to the reference flat TFT. On the other hand, compressive strain caused TFTs to degrade more under the same voltage bias. When the bending direction was in parallel with the length of TFTs, the impact of strain on degradation was generally more than the case of TFTs with strain perpendicular to L. Moreover, in all experiments, TFTs under linear mode were observed to degrade faster than in saturation mode under the same V_{GS}. The degradation ratio of linear to saturation modes was also confirmed to closely follow 3 : 2 [62] which is the crucial design parameter for the 6T compensation pixel circuit.

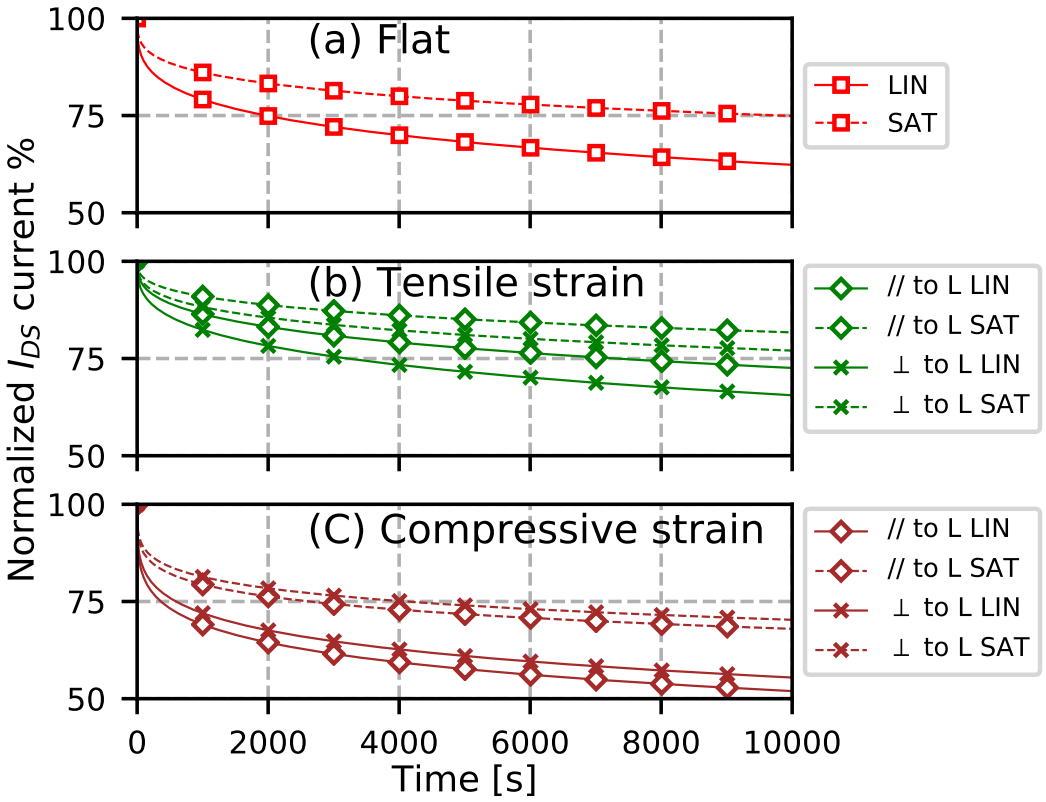


Figure 4.19: The normalized I_{DS} of a TFT ($W/L = 100\,\mu m/20\,\mu m$) under linear (LIN) and saturation (SAT) voltage-bias stress conditions for three hours when (a) laid flat, and under (b) tensile strain and (c) compressive strain. The bending experiments contain both configurations where the applied strain was parallel (//) and perpendicular (⊥) to L.

4.2.5 Measurement results of the 6T pixel circuit

The optical micro-graph of the fabricated 6T pixel circuit is shown in Fig. 4.20(a). The bending experiments were conducted by taping the substrate onto a convex (Fig. 4.20(b)) or a concave (Fig. 4.20(c)) metal sample holder with the same radius to obtain tensile or compressive strain, respectively. The power-supply voltage, data input, and control signals were generated according to Table. 4.1 by an Arduino-Mega micro-controller with external digital-to-analog converters and operational amplifiers shown in Fig. 4.20(d).

The pixel circuit on the same PEN substrate was driven at the maximum $V_{data} = 15\,V$ to mimic a worst-case TFT degradation while laid flat and bent with tensile or compressive strain of ±0.3% for 24 hours under 60 Hz frequency. Note that the bend-

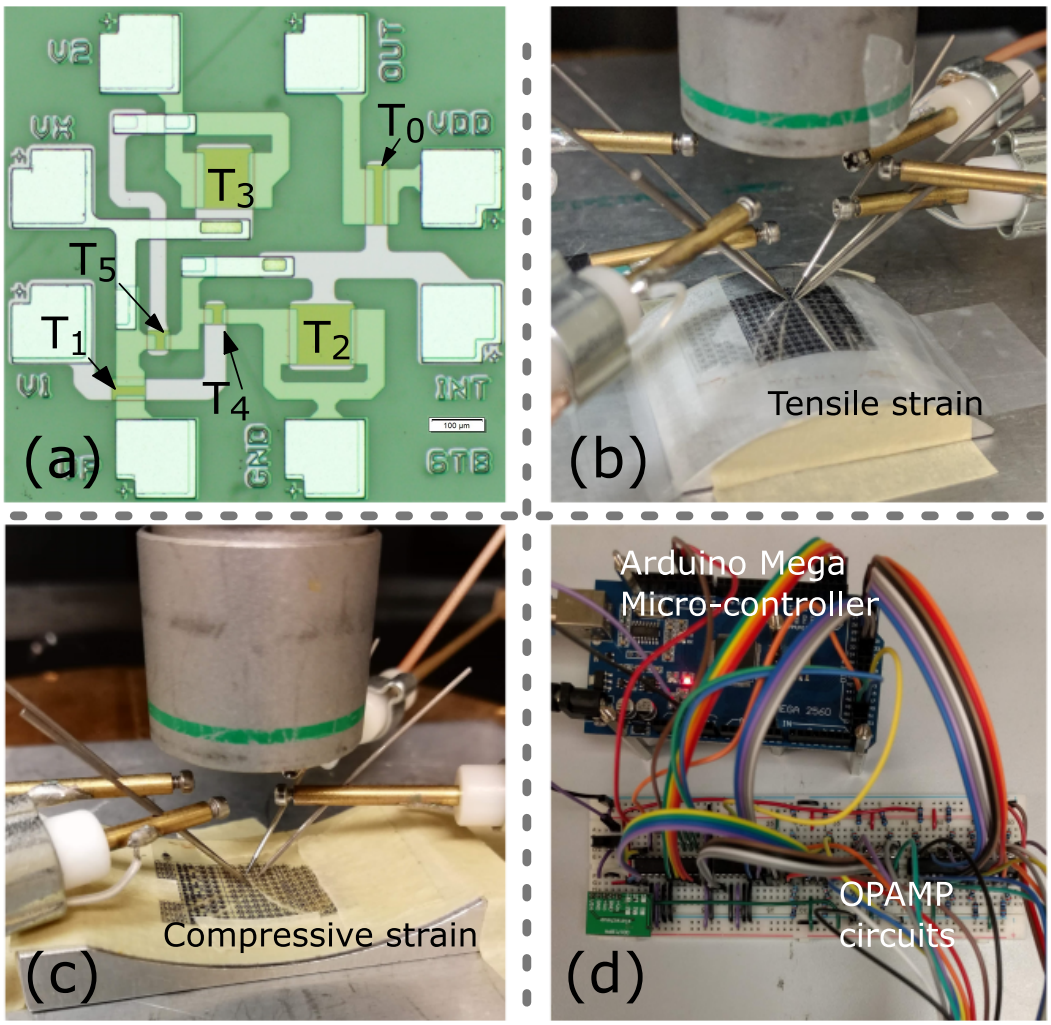


Figure 4.20: (a) A micro-graph of the pixel circuit, (b) The bending test setup with tensile strain, (c) The bending test setup with compressive strain, and (d) The Arduino Mega micro-controller and external IC components for control-signal generation and data logging.

ing direction was parallel to the length of T_0 and T_2 so that the impact of mechanical strain was at its maximum [56, 57]. The output current of the pixel circuit was logged every 10 minutes through an analog-to-digital converter on-board the Arduino-Mega micro-controller.

Fig. 4.21(a) shows the control signals of V_1, V_2, and V_{data}. The initial output current waveforms during a display cycle (60 Hz refresh rate) of the 6T pixel circuit are shown in Fig. 4.21(b). All three cases with the pixel circuit being laid flat, and under tensile strain and compressive strain showed a slight variation in the initial

output current values due to mobility change under bending [63, 65]. After 24-hour bias stress, all the pixel circuits demonstrated the correct compensation behavior with less than ±2% variation (Fig. 4.21c)) compared to the initial output current values with the same strain conditions in Fig. 4.21(b). In contrast, the output current of a 2T uncompensated pixel circuit with the same initial current experienced more than 40% loss when placed flat (not shown here).

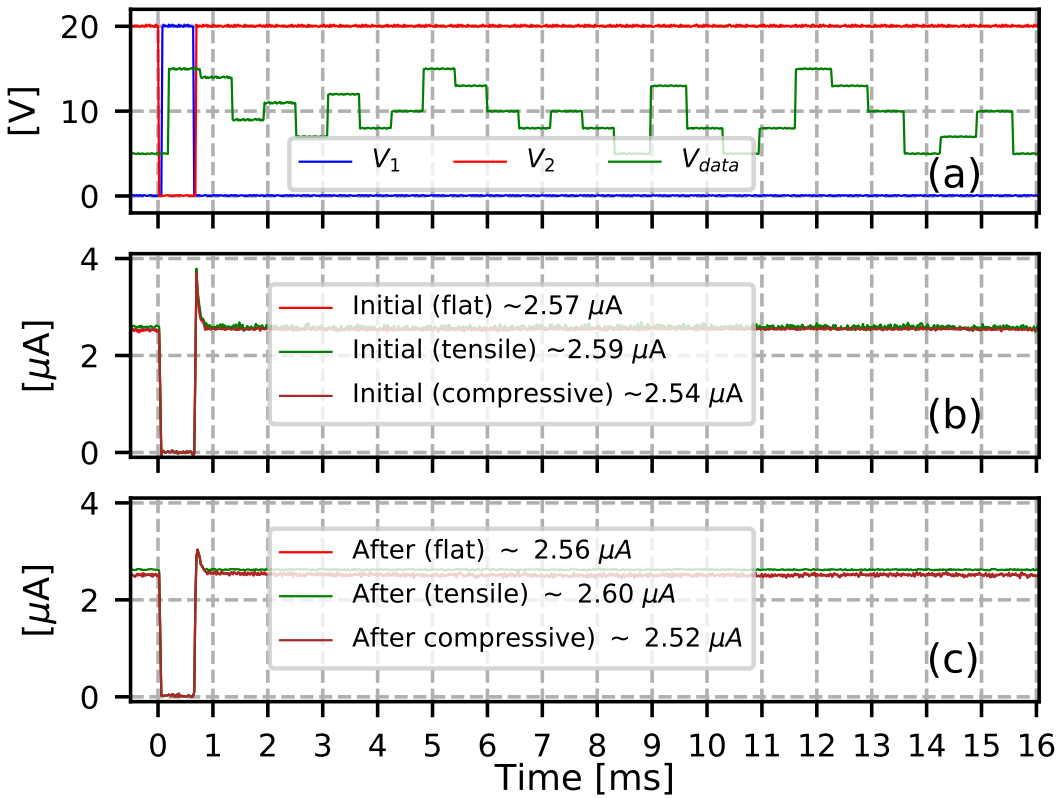


Figure 4.21: The measured transient waveforms of (a) the input signals. (b) The output current of the 6T pixel circuit at the initial time before bias stress. (c) The output current after 24 hours of bias stress test with maximum V_{data} when the pixel was laid flat, and under tensile and compressive strains.

To investigate the effectiveness of the self-compensating charge-transfer mechanism of the 6T pixel circuit, C-V measurements were also performed on the correlating TFTs (T_2 and T_0). All the terminals of T_2 and T_0 were made available for probing in the pixel circuit shown in Fig. 4.20(a). According to Eq. (4.6), the correlation ratio should be $\Delta V_{T,2} : \Delta V_{T,0} = 3 : 2$ [62]. In the experimental results shown in Fig. 4.22

(a) and (b), when the pixel circuit was laid flat during the test, $\Delta V_{T,2} = 3.15\,V$ and $\Delta V_{T,0} = 2.08\,V$, and the correlation value was 1.51. When under tensile strain, the measured C-V curves showed $\Delta V_{T,2} = 1.78\,V$ and $\Delta V_{T,0} = 1.16\,V$, and the correlation value was 1.53. When under compressive strain, the C-V curves showed $\Delta V_{T,2} = 4.17\,V$ and $\Delta V_{T,0} = 2.80\,V$, and the correlation value was 1.49. As a result, in all three long-term bias stress experiments, the 6T pixel circuit demonstrated the correct correlation between T_2 and T_0, which provided the desired compensation behavior regardless of strain situations.

Table 4.3: Summary of $\Delta V_{T,2}$ and $\Delta V_{T,0}$ under various stress conditions.

	$\Delta V_{T,2}$ (V)	$\Delta V_{T,0}$ (V)	Correlation ratio
Flat	3.15	2.08	1.51
Tensile	1.78	1.16	1.53
Compressive	4.17	2.80	1.49

Three additional experiments with random V_{data} were also conducted with flat, tensile strain, and compressive strain conditions on the pixel circuit to verify the compensation capability in the entire data range after bias-stress for 24 hours. Fig. 4.23 shows the results of the 6T pixel circuit in comparison with the 2T uncompensated pixel circuit under flat condition. Note that the proposed pixel circuit exhibited less than $\pm 3\%$ of variation for all the situations while the output current of the uncompensated 2T pixel circuit was reduced by $\sim 40\%$.

4.2.6 Analysis of the lifetime and overlap capacitance

To further investigate the limitation of the 6T compensation pixel circuit, higher $\Delta V_{T,2}$ and $\Delta V_{T,0}$ values were applied to the simulation test-bench, while keeping the correlation ratio of 3 : 2. Fig. 4.24 shows the simulation of normalized output current of the 6T compensated and 2T uncompensated pixel circuits with a $\Delta V_{T,0}$ range from

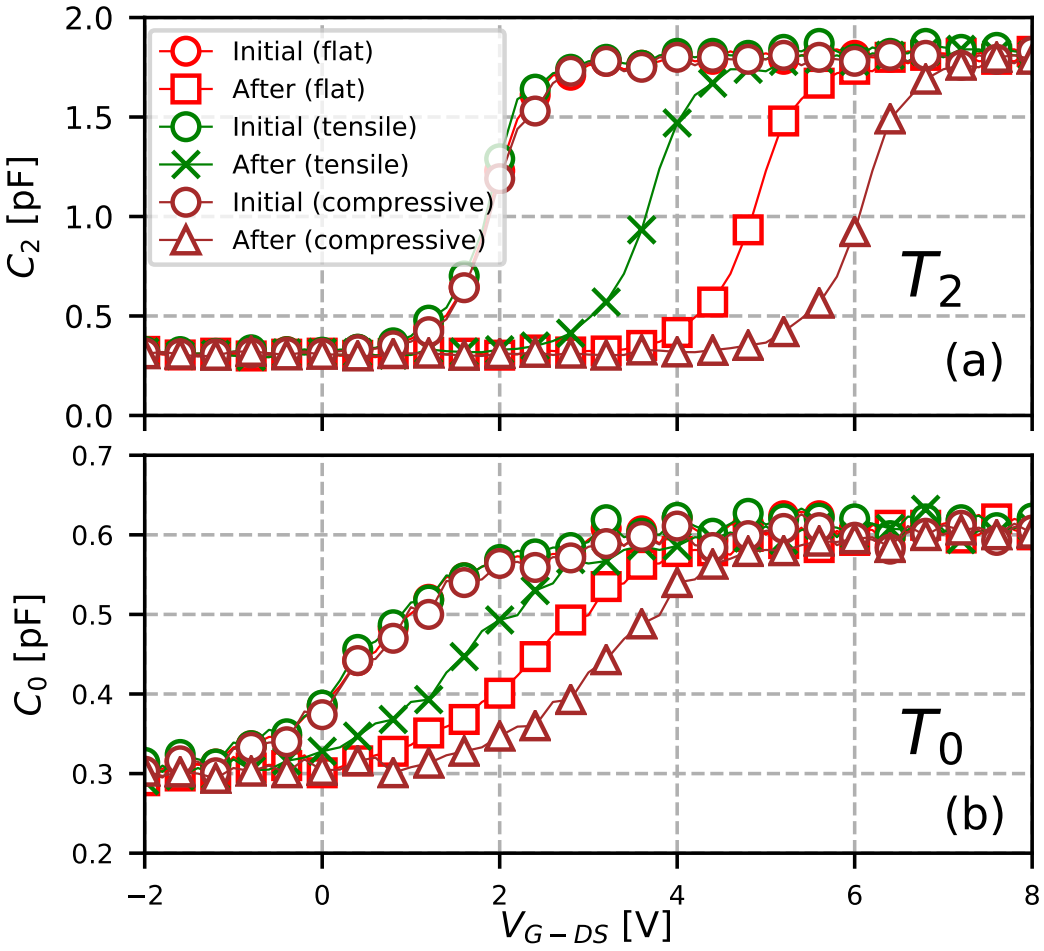


Figure 4.22: The C-V curves of the correlating TFTs (a) T_2 and (b) T_0 measured initially and after long-term (24 hours) bias-stress test under flat (red), tensile (green), and compressive (brown) strain conditions.

$0\,V$ to $7\,V$ under flat condition. The simulation assumed a maximum $V_{data} = 15\,V$ in continuous operation to mimic the worst-case degradation. It is observed that the compensation starts to lose its effectiveness above $\Delta V_{T,0} = 5\,V$. This phenomenon can be explained by the charge-transfer mechanism of the correlating TFTs. Since the proposed compensation mechanism is to raise $V_{int}^{stressed}$ according to $\Delta V_{T,0}$, $V_{int}^{stressed}$ from Eq. (4.7) becomes $20\,V$ at $\Delta V_{T,0} = 5\,V$. This has made the difference between gate and drain terminals of T_0 almost zero. As a result, T_0 is no longer in saturation mode when $\Delta V_{T,0}$ is beyond $5\,V$. Therefore, the correlation of $\Delta V_{T,2} : \Delta V_{T,0}$ becomes less than $3 : 2$, reducing the compensation capability and causing the output

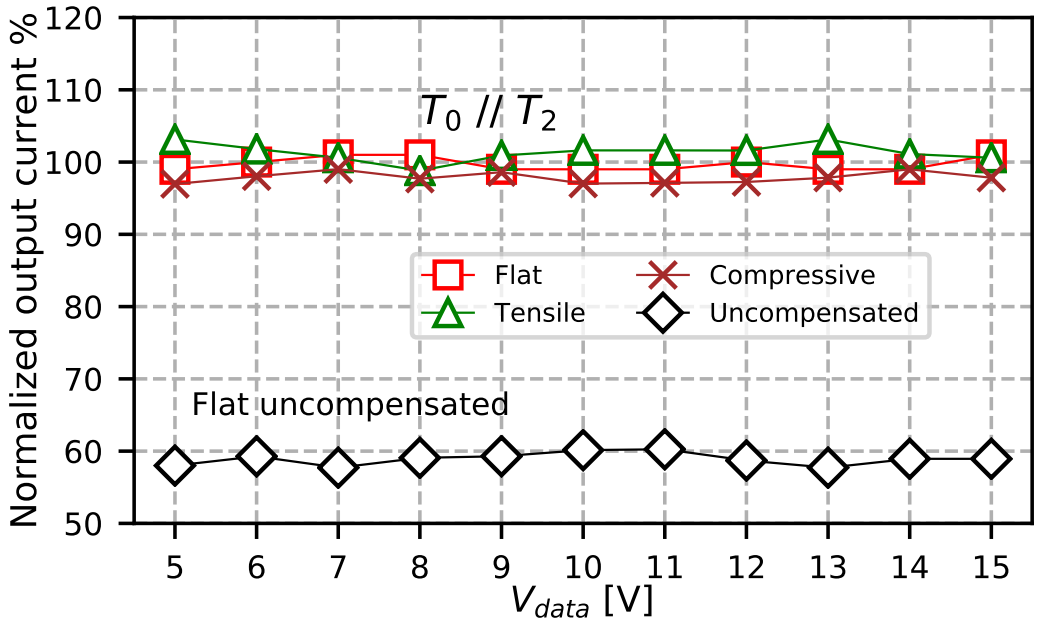


Figure 4.23: The normalized output current of the 6T pixel circuit for the entire V_{data} range after bias-stressed for 24 hours under flat (red), tensile strain (green), and compressive strain (brown) conditions along with the 2T uncompensated pixel circuit under flat condition.

current to deteriorate. Using the stretched-exponential relationship in Eq. (4.1), it is calculated that to reach $\Delta V_{T,0} = 7\,V$, it will take around 1400 hours of continuous display operation under the highest V_{data}. Therefore, more realistically, if the display is operating 3 hours a day showing videos, the time to reach $\Delta V_{T,0} = 7\,V$ is more than two and a half years. In addition, a portion of the material degradation in amorphous silicon and nitride materials is not permanent [66, 67]. When the display is not active, i.e. the TFTs are not being electrically stressed, the trapped charges in the disordered semiconductor layer and the semiconductor/dielectric interface may de-trap and restore some of the shifted V_T extending the life-time [52]. Furthermore, in a real product, there are multi-layers of fail-safe mechanism to enhance the reliability. In this case, when the degradation in the TFT becomes high and the pixel circuit is struggling to maintain a constant output current, there can be external detection method and software monitor system off the panel to correct the behavior. For example, increasing V_2 during the emitting phase allows T_3 to boost more charge to V_{int}

when $V_{T,0}$ is beyond $7\,V$. This can be a global solution that applies to all the pixels. The exact voltage increased on V_2 can be decided by the control software which logs the total operation time of the display.

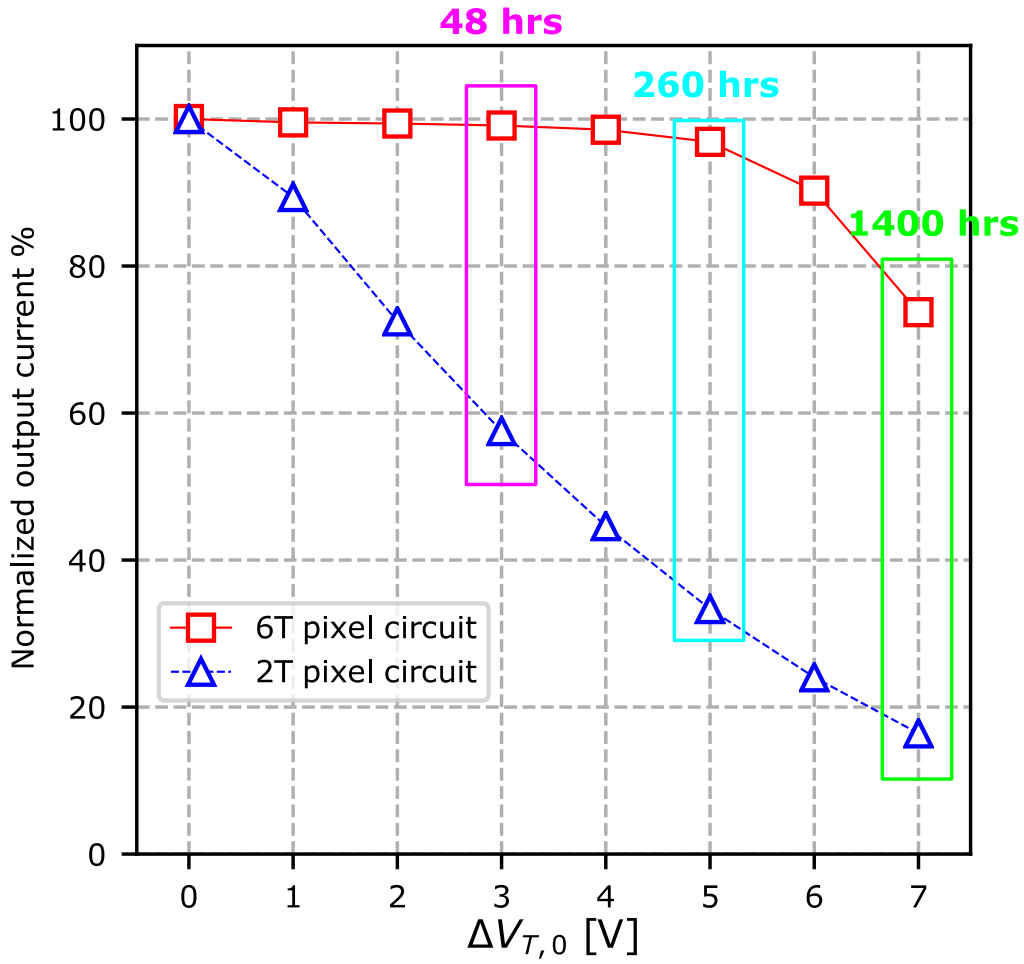


Figure 4.24: The simulation of normalized output current of the 6T pixel circuit and 2T uncompensated pixel circuit with increasing $\Delta V_{T,0}$ under flat condition at maximum $V_{data} = 15\,V$.

In addition to the consideration of the $\Delta V_{T,0}$ limitation, the change of correlation ratio has impact on the design of the 6T pixel circuit. When the correlation ratio is more than $3:2$, the size of T_2 and T_3 can be reduced because more charge from T_2 is supplied to facilitate the compensation. However, if the correlation ratio is less than $3:2$, the size of T_2 and T_3 should be increased to reach the desired compensation based on Eq. (4.18). In this case, the allowed area of the pixel circuit on the display

panel dictates the size of T_2 and T_3.

On the other hand, interests in 4K display, augment-reality (AR), and virtual-reality (VR) equipment have been recently growing, which requires faster operating speed and denser pixel displays. Despite the low carrier mobility of the a-Si:H TFTs, if they can be fabricated with design rules of $L_{ovl} = 1\,\mu m$ and a minimum length of $5\,\mu m$, the footprint can be reduced to $\sim 1070\,\mu m^2$, which is less than 5% of the original size. The simulation assumed that the W/L of T_0 remains the same, while other TFTs were sized according to Eq. (4.18). Moreover, the significant reduction in L_{ovl} can allow the pixel circuit to be operated at a higher frequency. In the proposed 6T pixel circuit, the speed is determined by the RC time constant when T_1 is charging the storage capacitor T_3. If a $1\,\mu m$ overlap design rule is assumed, the simulated worst-case charging time is less than $3\,\mu s$ satisfying the requirement for $200\,Hz$ refresh rate in a 2K display panel. However, if used in a $400\,Hz$ 4K display with more demanding requirements, a-Si:H technology would not be the ideal solution. In this case, high-mobility TFTs made by metal-oxide or LTPS technologies [68] could reduce the size of pixels and increase the operating speed, which satisfy the requirement for high-resolution displays.

4.3 Comparison of pixel circuits

4.3.1 Comparison between charge-transfer pixel circuits

Since the pixel circuit reported in [46, 57] also uses the same charge-transfer compensation method, a detailed comparison can be made between the 6T and 4T pixel circuits. First, the 6T pixel circuit has two small extra TFT switches (T_4 and T_5) but one less control signal. The reduction in control signals could significantly alleviate the complexity on the external row-control ICs, that outweighs the slight addition of the transistor increase.

The correlation ratio between T_2 and T_0 is crucial for the compensation method to perform correctly. However, the 4T circuit could not guarantee such correlation due to the following reasons.

(a) In the 4T circuit shown in 4.25(b), during the programming phase, T_2 is turned off by a high signal from V_2 while T_0 is turned on by V_{data}. As a result, there is a slight discrepancy between the degradation time of T_2 and T_0 which is proportional to the duration of the programming phase and the emitting phase.

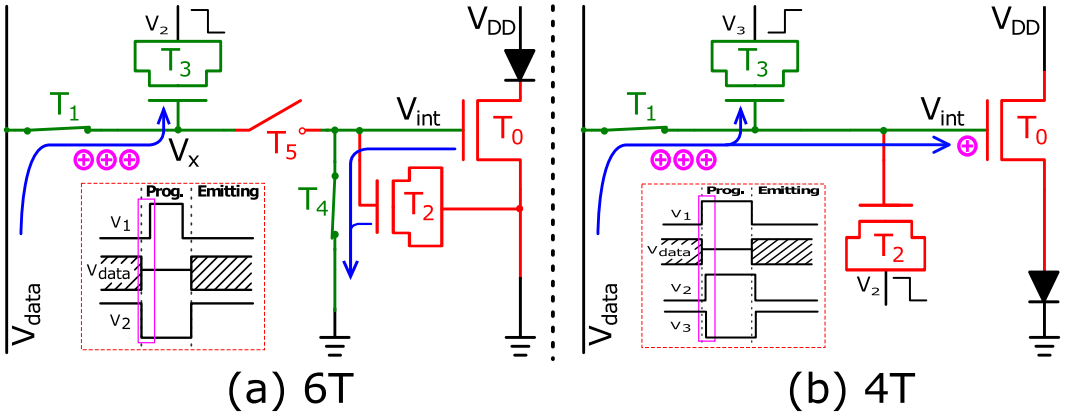


Figure 4.25: The schematic of (a) 6T and (b) 4T pixel circuits in programming phase.

(b) Moreover, since the LED is placed on the source terminal of T_0, there exists a difference in voltage bias between T_2 and T_0 depending on the on-voltage of the LED. Then, T_2 would degrade slower than expected, causing the 4T pixel circuit to under-compensation.

On the other hand, the speed of operation also plays an important role for a pixel circuit because it leads to higher display resolution or refresh rate. In the 4T circuit, the column data driver has to fully charge both T_3 and T_0 to V_{data}, while in the 6T circuit, it only needs to charge up T_3 and a small switch T_5. Based on the device sizes used in both circuits, the input capacitance in the 4T circuit is:

$$C_{4T} = C_{T_0} + C_{T_3} \tag{4.19}$$

$$C_{4T} = 100 \times 5 \times C_{ovl} + 100 \times 20 \times C_{ch} \tag{4.20}$$

$$+ 100 \times 5 \times 2 \times C_{ovl} + 100 \times 100 \times C_{ch} \tag{4.21}$$

$$C_{4T} = 2.25\,pF \tag{4.22}$$

Meanwhile, the input capacitance in 6T pixel circuit in the column is:

$$C_{6T} = C_{T_3} + C_{T_5} \tag{4.23}$$

$$C_{6T} = 100 \times 5 \times 2 \times C_{ovl} + 100 \times 100 \times C_{ch} \tag{4.24}$$

$$+ 20 \times 5 \times C_{ovl} \tag{4.25}$$

$$C_{6T} = 1.84\,pF \tag{4.26}$$

Seen from the calculations above, the 6T pixel circuit has 18.2% less input capacitance for the column driver to charge, which could potentially result in a higher operating speed.

From all the analysis presented above, it can be concluded that the 6T pixel circuit can provide superior compensation capability by always maintaining the same bias stress on T_2 and T_0, so that the 3 : 2 correlation is always kept. Meanwhile, the reduction of one control signal and input capacitance could alleviate the complexity of external ICs and improve operating speed, thus facilitating the realization of a higher resolution display.

4.3.2 Comparison of existing compensation pixel circuits

The proposed 6T pixel circuit was compared with existing compensation methods in terms of number of TFTs, control signals, and performance. The result is summarized

in Table 4.4. The 6T pixel circuit has the least amount of control signals and average TFT count. Its footprint is also comparable to other charge-transfer pixel circuits and much less than the ones using other compensation methods. The compensation performance under flat and bending situations is superior to the previously reported solutions, demonstrating the efficacy of the proposed self-compensating pixel circuit for flexible displays.

Table 4.4: Comparison of a-Si:H compensation pixel circuits

	This Work	Lee [2017]	Yang [2012]	Oh [2012]	Ashtiani [2007]	Lee [2005]
Technology	**a-Si:H**	a-Si:H	a-Si:H	a-Si:H	a-Si:H	a-Si:H
Substrate	**PEN**	PEN	Glass	Glass	Glass	Glass
Compensation Method	**Charge transfer**	Charge transfer	Charge transfer	External detection	Internal detection	Reverse anneal
# of TFTs	**6**	4	4	4	5	7
# of signals	**2**	3	3	4	3	3
Footprint (mm^2)	**0.024**	0.021	0.023	0.054	0.036	0.058
Flat	±**2**%	±5%	±3%	±2%	±5%	±6%
Bending	±**3**%	±10%	N/A	N/A	N/A	N/A

4.4 Summary

In this chapter, the challenges of using a-Si:H TFTs as the backplane to drive μLEDs have been exposed. Due to material degradation, pixel circuits made by a-Si:H TFTs struggle to supply a stable current to the light media. Several prior compensation schemes have been introduced and an in-pixel compensation circuit has been proposed and thoroughly analyzed, simulated and measured for its performance in compensation capability on a flexible substrate.

The proposed 6T pixel circuit requires only two digital timing-control signals along with the data input to operate, just one extra than the conventional 2T pixel circuit. The 6T pixel circuit engages a specific correlation between two degrading TFTs in linear and saturation modes to realize compensation which can provide a near constant output current to the light media over-time. Furthermore, based on prior reports and in-house experiment results, the orientation of two correlating TFTs can also play an important role in compensation, that could be exploited for flexible display applications. When compared with other compensation methods, the charge-transfer method proves to be very effective and the 6T pixel circuit has demonstrated excellent compensation results under bending with ease of control.

After having a simple and reliable pixel circuit to tackle the electrical instability of the TFTs, it is intuitive to come up with logic circuits that could address those timing-control signals properly so that the flexible display panels could achieve higher integration levels to reduce fabrication cost. In the next chapter, low-power and full-swing logic circuits realized by unipolar a-Si:H TFTs will be presented to achieve this goal.

Chapter 5

CMOS-like logic circuits for flexible displays

With rapid growing interests in Internet-of-Things, wearable devices, and virtual-reality gadgets, demand in flexible electronics is rising owing to its low-cost and mass-production capabilities [69]. Unlike single-crystalline CMOS process, low thermal-budget thin-film technology is used to fabricate transistors on non-rigid substrate on which flexible display panels could be realized [42]. Conventionally, TFTs on display backplane only form pixel arrays while the peripheral control and data circuits are realized from off-panel integrated circuits (ICs). Consequently, every row and column signal needs to be driven externally, resulting in a large number of bonding pads. The schematic of an LCD backplane as well as a micro-graph is shown in Fig. 5.1 which indicates the high count of bonding pads.

With the growing demand for higher resolution displays, pixel density is reaching beyond 4K. As a result, the number of pads is increasing proportionally and reducing pad pitch is becoming increasingly difficult to accommodate growing pad requirement. To alleviate this problem, peripheral digital circuits should be realized alongside the pixel array on the same substrate. However, there are challenges to design complex logic circuits with unipolar TFTs because of the unavailability of both p- and n-type

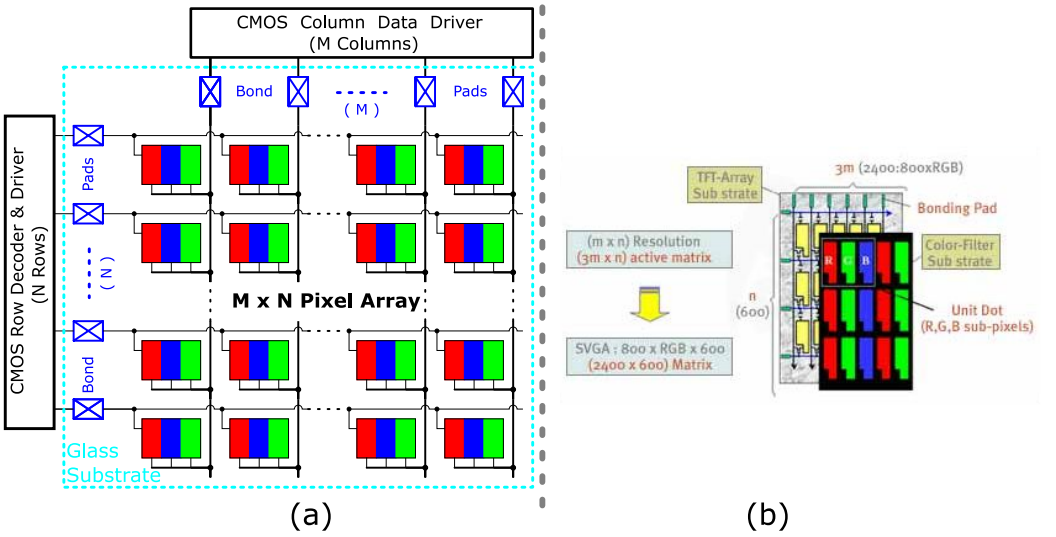


Figure 5.1: (a) The schematic and (b) layout views of a conventional LCD display panel showing the number of bonding pads.

devices.

In the display industry, handheld applications with smaller screens can overcome this problem by using low-temperature-poly-silicon (LTPS) TFTs which undergo laser and ion-implantation treatments to achieve both types of devices on rigid substrates [70, 71, 72]. However, such technique would not be feasible for large-area displays because of the poor uniformity of LTPS TFTs and the additional fabrication complexity. With these aforementioned constraints, the solution to realize CMOS-like digital circuits on panel has to come from innovative circuit design.

This chapter will introduce the challenges to design logic circuits with unipolar TFTs. It will also discuss prior circuit implementations. Followed by that, a bootstrapped logic gate style will be analyzed, it promises unity stage-to-stage gain and low static leakage current. Then, a multi-stage logic circuit example of a 1-to-2 decoder is demonstrated with such logic gates on flexible substrate. Next, an area efficient improvement of the bootstrapped logic gates is proposed with a more complex 3-to-8 decoder design to prove its effectiveness.

5.1 Introduction to TFT logic gates

5.1.1 Conventional unipolar logic gates

Logic gates such as inverter, NAND, and NOR are the fundamental building blocks to accomplish complex circuits. Conventionally, using only n-type TFTs, an inverter can be realized with two TFTs: the diode-connected load and the pull-down TFT shown in Fig. 5.2. This 2T configuration has two major drawbacks: one being not able to deliver rail-to-rail output swing (ΔV_{out}) and the other being power hungry. The reason is explained as follows with the aid of a transient simulation shown in Fig. 5.2(b). When the input signal is low, the diode-connected pull-up TFT tries to charge the load capacitor to high, however the maximum V_{out} (V_H) that can reach is only $V_{DD} - V_T$ with the V_T being the threshold-voltage of the load TFT. On the other hand, when the input signal is high, both TFTs are on, resulting in a voltage division at the output. As such, the minimum output voltage (V_L) can not reach zero either.

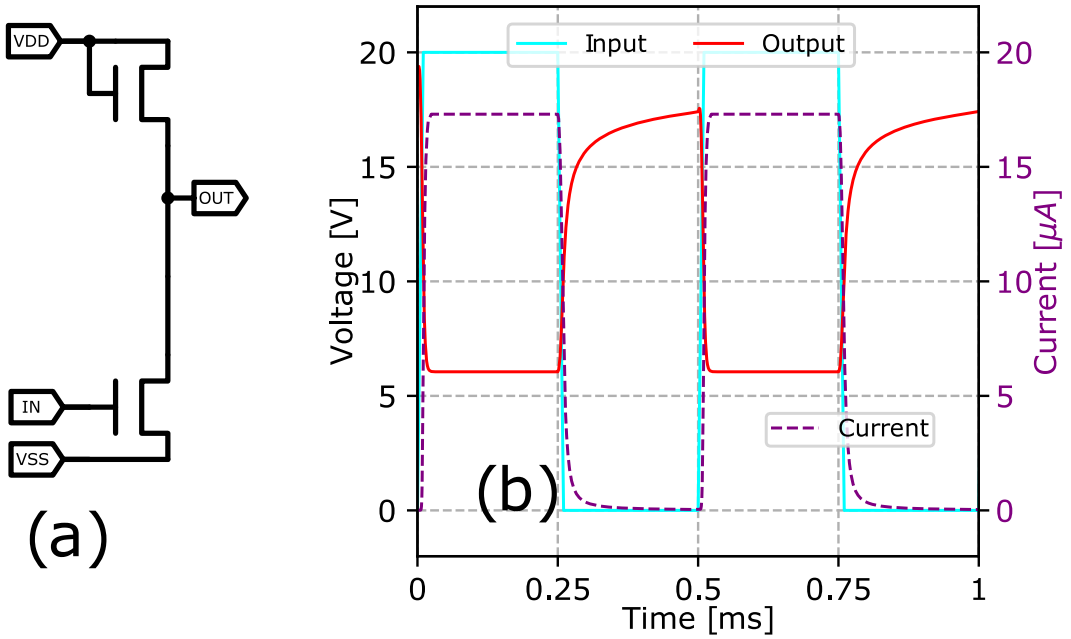


Figure 5.2: (a) The schematic of the conventional 2T inverter and (b) the input/output voltage waveform and the transient current behavior.

In another example, the 2-input NAND gate made by 3-TFTs is shown in Fig.

5.3(a) along with the transient behavior shown in (b).

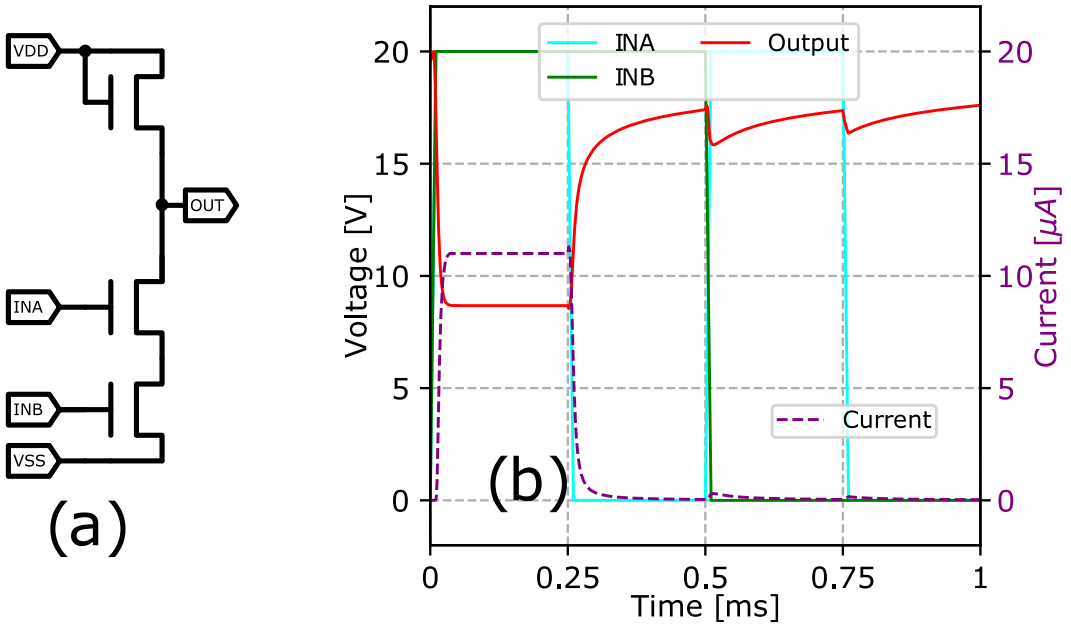


Figure 5.3: (a) The schematic of the conventional 3T NAND and (b) the input/output voltage waveform and the transient current behavior.

It can be concluded that the conventional diode-connected configuration of the logic gates causes the static leakage current to be high from inability to shut off non-conducting TFTs completely. Consequently, these conventional logic gates are not able to achieve the CMOS-like features that a complex circuit needs.

There have been several circuit solutions to tackle the deficiencies caused by unipolar TFTs with varying degrees of success. They will be briefly introduced for the readers to understand the prior art.

5.1.2 Prior solution - 4-TFT inverter

Prior work [73, 74] has first attempted to tackle the high static leakage current problem by inventing a 4-TFT (4T) inverter which has an additional stage compared to the 2T one. Shown in Fig. 5.4(a) the gate (node A) of the pseudo p-type load TFT (T_0) is now connected to the source of a diode-configured TFT (T_3) and on the same node, another TFT (T_2) shorts it to V_{SS}.

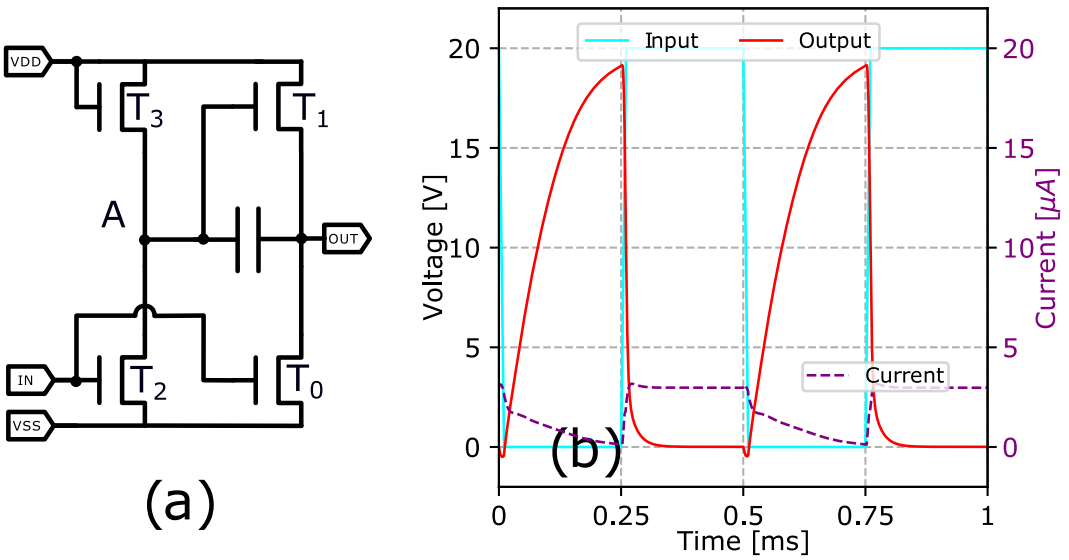


Figure 5.4: (a) The schematic of the 4T inverter and (b) the input/output voltage waveform and the transient current behavior.

In this 4T configuration, when input is high, T_0 and T_2 are fully turned on causing node A and the output to be both drained. Since T_3 is a diode connected load so that it is always in saturation mode. The channel width ratio of T_3 and T_2 has to be heavily skewed so that T_3 is only leaking minimal current while T_2 is large and the on-resistance (R_{ON}) is very low. In this way, node A voltage is kept low enough so that T_1 is not turned on and the output voltage can be successfully lowered to V_{SS}.

On the other hand, when the input signal is low, the capacitor boost charge to help T_1 raise the output voltage, so the output swing is higher compared the 2T inverter. However, the leakage current is almost eliminated in this phase. Overall the 4T inverter is a much better design considering the output swing and leakage current.

5.1.3 Prior solution - 7-TFT and 1-capacitor inverter

Hwang et al. has proposed a 7-TFT and 1-capacitor (7T+1C) inverter to tackle the challenges [75]. The schematic of the inverter is shown in Fig. 5.5.

The operation of this inverter is described as follows. When the input signal (IN) is switched to V_{DD}, TFTs N_2, N_4, and N_6 are turned on and at the mean time, the gates

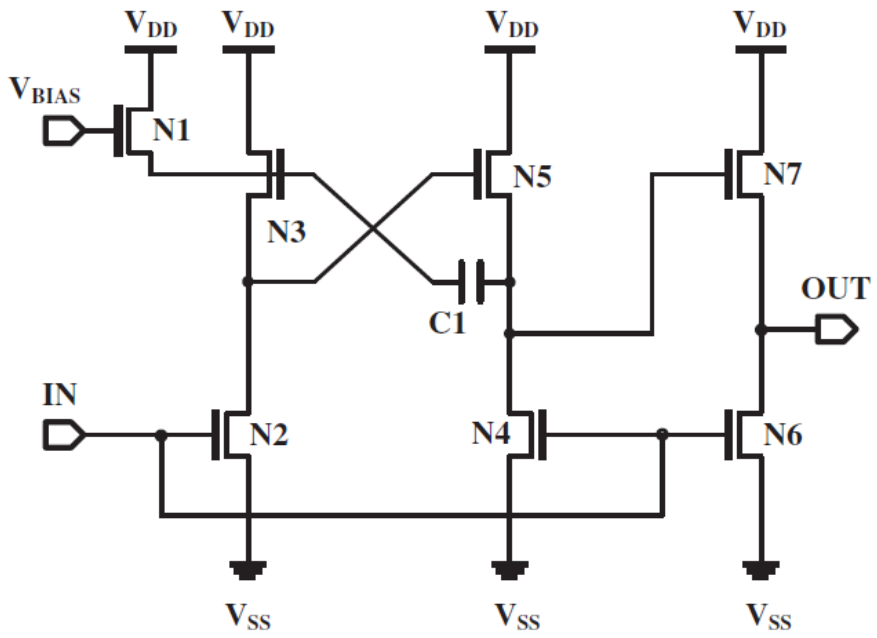


Figure 5.5: The schematic of the 7T+1C inverter [75].

of N_3, N_5, and N_7 are fully discharged, such that the output node is also discharged to ground. In the next phase when the input signal switches to ground, TFTs N_2, N_4, and N_6 are turned off. Subsequently, the gate of N_5 is raised due to the drain current supplied by N_3. Then, the gate voltage of both N_3 and N_5 increase to V_{DD} from the feedback loop. The function of V_{BIAS} is to aid in storing charge on C_1 which maintains the overdrive voltage of N_3. The V_{BIAS} signal is crucial in the operation of the inverter because it helps the output signal to reach full swing. However, this extra signal makes it not truly CMOS-like because it complicates logic circuit design in terms of routing and area overhead.

5.2 Bootstrapped logic gates

Fig. 5.6(a) and (b) show the bootstrapped 7-TFT (7T) inverter and 10-TFT (10T) NAND gate, respectively [76, 77]. The main difference between the prior implementations and the bootstrapped logic gates is the addition of a feedback loop consisting of four TFTs (T_1, T_3, T_4, and T_5) and one metal-insulator-metal (MIM) capacitor

(C_{fb}) configured in the bootstrapped inverter and NAND gate as shown in dashed red boxes in Fig. 5.6(a) and (b) [1].

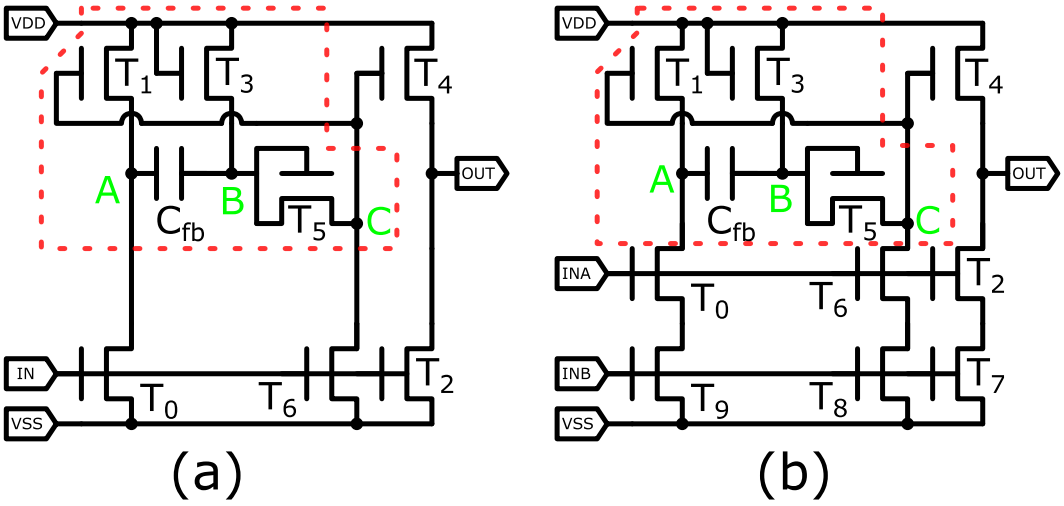


Figure 5.6: The bootstrapped (a) 7T inverter and (b) 10T NAND gate. The dashed red boxes contain the feedback loops.

5.2.1 Mathematical analysis of the feedback loop

The 7T inverter is used as an example to illustrate the bootstrapped technique. The following analysis is divided into two parts, output pull-up (when input switches to low state) and pull-down (when input switches to high state) operations.

When the input signal is high, the voltage at node A (V_A) is drained to zero. Node B (V_B) and C (V_C) voltages are fractions of V_{DD} in a resistor network formed by diode-configured TFTs (T_3 and T_5) as well as T_6 operating in the linear mode. As a result, V_B is $\sim \frac{1}{2}V_{DD}$. Since the resistance of T_6 is much smaller than T_3 and T_5, V_C is close to $0\,V$ which turns off T_4. However, the non-zero leakage current flowing through T_3, T_5, and T_6 is notably low owing to the smaller TFT width of T_3. As a result, V_L can reach close to zero. The nodal voltages and leakage current path are shown in Fig. 5.7.

[1] This chapter is an amended version of "CMOS-like logic circuits with unipolar thin-film transistors on flexible substrate", including modified figures and tables, by Q. Li, C.-H. Lee, M. Asad, W. S. Wong, M. Sachdev, published in the Transactions of Electron Devices, with ©IEEE 2019. If citing any figure or table, please refer to the original publication.

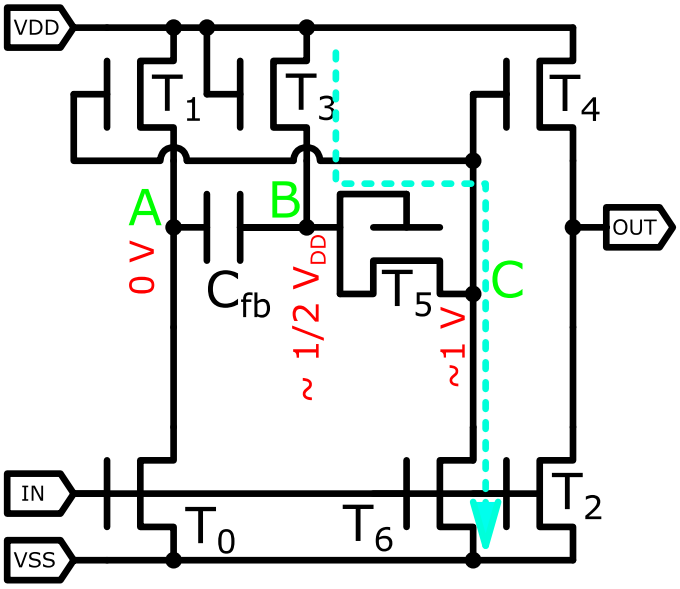


Figure 5.7: The internal nodal voltages of the 7T inverter after reaching steady-state during output pull-down operation. The dashed line indicates leakage current flow that limits the node C voltage to be low.

Assuming T_2 is in saturation mode for the majority of the pull-down transition, the discharging time "t" could be estimated by a first-order MOSFET equation shown in Eq. (5.1). The parameters μ_n and C_{SiN} represent the field-effect mobility and the capacitance of the a-SiN$_x$:H gate dielectric of the a-Si:H TFTs, respectively.

$$\frac{1}{2}\mu_n C_{SiN}\frac{W_2}{L_2}[V_{DD}-V_T]^2 = \frac{C_{load}V_{DD}}{t} \tag{5.1}$$

Next, assuming that the input signal switches to zero at "$t = 0$", TFTs (T_0, T_6 and T_2) are turned off, which prevents all leakage paths to ground. Then, the feedback loop begins to raise V_C, which subsequently turns on T_1 and causes V_A to rise. This charging behavior reaches steady-state when V_A, V_B, and V_C attain approximately V_{DD}, $\frac{3}{2}V_{DD}$, and $\frac{3}{2}V_{DD} - V_T$, respectively.

Fig. 5.8(a) illustrates the feedback network portion of the inverter. All devices, parasitic capacitors, and current flow directions are labeled accordingly. To simplify the analysis, diode-configured T_3 is not included.

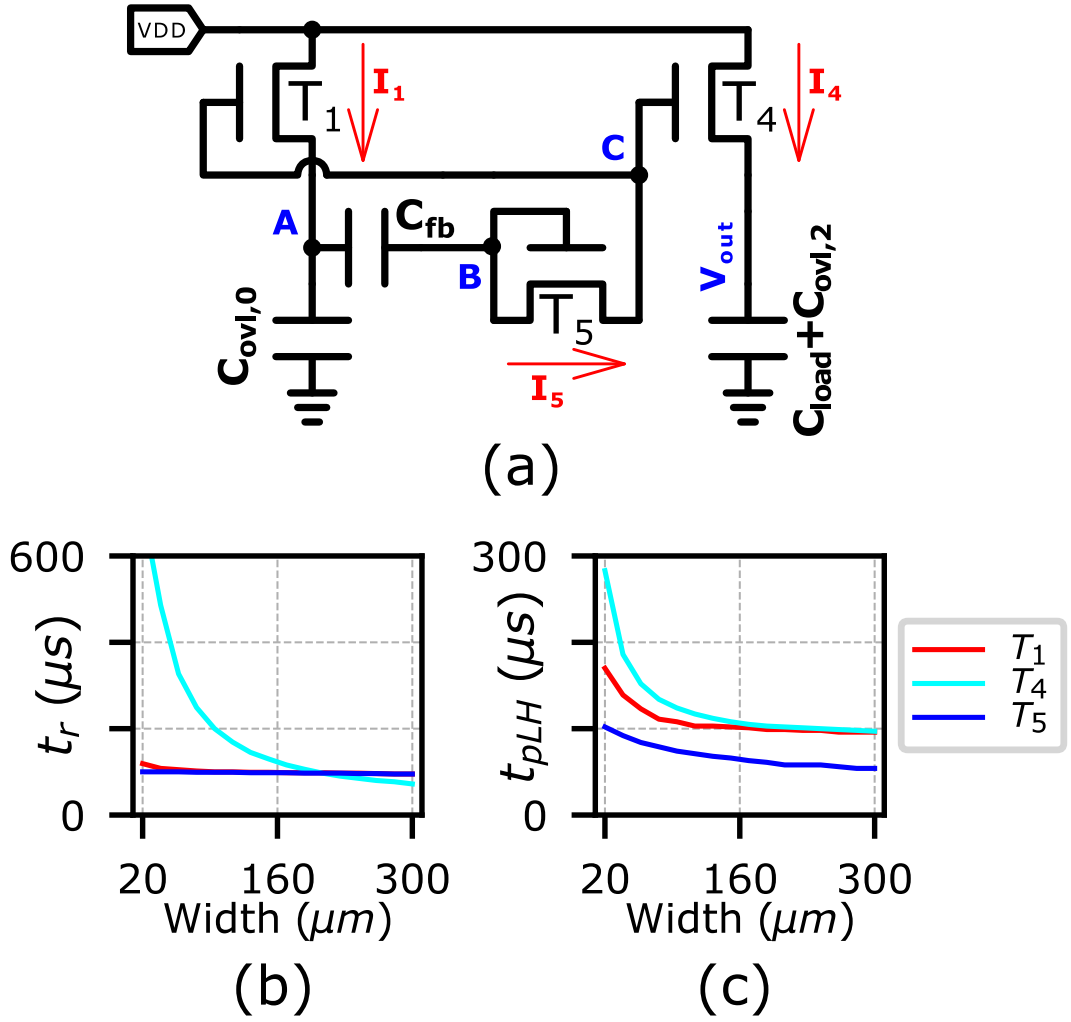


Figure 5.8: (a) The feedback network portion of the inverter when input is zero. The output (b) rise-time (t_r) and (c) low-to-high propagation delay (t_{pLH}) of the 7T inverter when varying the width of T_1 (red line), T_4 (cyan line), and T_5 (blue line) individually using derived equations.

The transient current-voltage relationship for each TFT and internal nodes are derived as follows:

At node A, T_1 is used to raise V_A to V_{DD}. Assuming that T_1 is in saturation mode for the majority of the duration before V_A reaches V_{DD}, its output current at given time "t" is shown below:

$$I_1(t) = \frac{1}{2}\mu_n C_{SiN}\frac{W_1}{L_1}[V_C(t) - V_A(t) - V_T]^2 \tag{5.2}$$

The capacitance at node A that T_1 has to charge up is shown as:

$$C_A = C_{fb} + C_{ovl,0} \tag{5.3}$$

At node B, V_B rises as V_A goes higher, and the stored charge in C_{fb} ($Q_{fb} = \frac{1}{2}C_{fb}V_{DD}$) when input is $0\,V$ is pushed into V_C. Assuming that C_{fb} is an ideal capacitor, there exists a relationship between $V_B(t)$ and $V_A(t)$ shown below:

$$V_B(t) = V_A(t) + \frac{1}{2}V_{DD} \tag{5.4}$$

$I_5(t)$ is the current charging C_C and can be expressed as:

$$I_5(t) = \frac{1}{2}\mu_n C_{SiN}\frac{W_5}{L_5}[V_B(t) - V_C(t) - V_T]^2 \tag{5.5}$$

where C_C is given as:

$$C_C = C_{ovl,4} + C_{ovl,6} \tag{5.6}$$

Lastly, V_{out} reaches V_{DD} through the current supplied by T_4 with a lumped capacitance (C_{out}). The current provided by T_4 at time "t" equals to:

$$I_4(t) = \frac{1}{2}\mu_n C_{SiN}\frac{W_4}{L_4}[V_C(t) - V_{out}(t) - V_T]^2 \tag{5.7}$$

And C_{out} is expressed as:

$$C_{out} = C_{load} + C_{ovl,2} \tag{5.8}$$

After combining all the equations above using Kirchhoff's current law, a first-order estimation can be calculated to find out the t_{pLH} and t_r for V_{out} to reach V_{DD} by performing a time-domain integration using the general charge-current equation:

$$C_{out}V_{out}(t) = \int \Big\{ I_1(t), I_5(t), I_4(t) \Big\} dt \tag{5.9}$$

To obtain numerical solution to the Eq. (5.9), the size of T_2 is chosen to be $W/L = 200\,\mu m/20\,\mu m$ as a reference. Then, after varying the widths of T_1, T_4, and T_5 from $20\,\mu m$ to $300\,\mu m$ one at a time, the resulting t_r and t_{pLH} are shown in Fig. 5.8(b) and (c), respectively. It is seen that the main TFT (T_4) that charges the output load has the strongest influence on the transient behavior. However, its impact starts to saturate when W_4 approaches $200\,\mu m$. It is also noticeable that T_5 can further reduce the propagation delay by $40 \sim 50\%$ because it directly affects the charging of V_C, yet such gain in speed comes at a cost of increased leakage current.

5.2.2 Simulation of the bootstrapped 7T inverter

From the circuit analysis and mathematical derivations, it is observed that t_r and t_{pLH} are large because as V_{out} is increased, the over-drive voltage of T_4 ($V_C - V_{out} - V_T$) is proportionately reduced. On the other hand, t_f and t_{pHL} are lower because the maximum over-drive voltage on T_2 is always maintained when the input is high. To determine the geometries of TFTs in the pull-up network, transient and power simulations were carried out with a modified charge-based level-61 a-Si:H model [46] in the Cadence Virtuoso environment. The model globally defined a source/drain

overlap of 15 μm and a minimum channel length of 20 μm to comply with fabrication specifications. In addition, the model used a V_T of 4.5 V, a field-effect mobility of 0.7 cm^2/Vs, and a sub-threshold slope of 0.65 V/dec. Simulations swept the width of T_1, T_3, T_4, T_5, and C_{fb} from 20 μm to 300 μm individually, while keeping the geometry of all other TFTs constant. The V_{DD} was set to 20 V and the input signal had a frequency of 1 KHz and t_r and t_f of 10 μs.

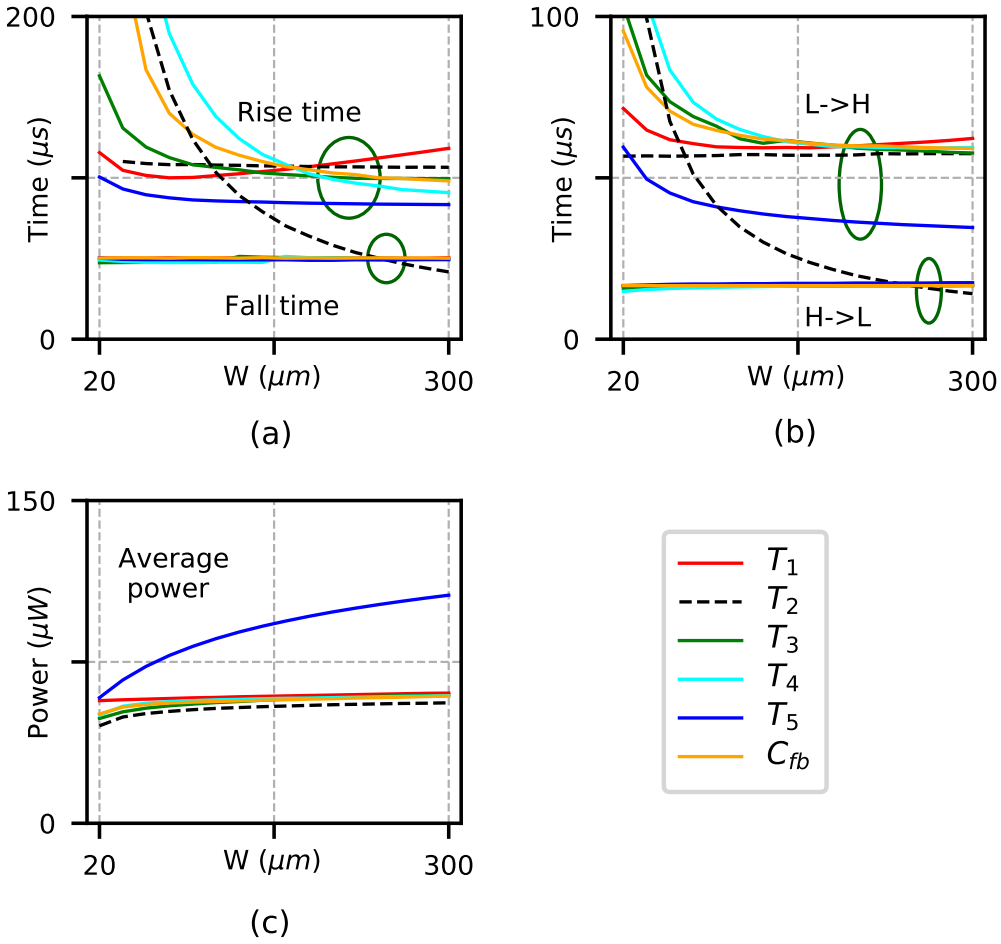


Figure 5.9: The comparison of (a) t_r and t_f, (b) t_{pLH} and t_{pHL}, and (c) P_{avg} of the 7T inverter when varying the sizes of T_1, T_2, T_3, T_4, T_5, and C_{fb}, individually.

Fig. 5.9 illustrates simulation results. Shown in Fig. 5.9(a) and (b), t_r and t_{pLH} are critically affected by T_4 because it directly charges the load capacitor, as predicted in the derivation. Moreover, C_{fb} is also a contributor to the switching speed because the charge stored in C_{fb} raises V_B and subsequently V_C. In addition, the size impact

from T_5 is also consistent with the prediction. When its width increases from 20 μm to 300 μm, t_{pLH} drops from 59.5 μs to 34.6 μs, which is a 42% reduction. Meanwhile, such increase in the width of T_5 results in the static leakage current to be higher, causing the average power consumption to rise by $\sim$ 80% shown in Fig. 5.9(c).

On the other hand, when the input signal is high, t_f and t_{pHL} have minimal impact from the size variation of the devices in the feedback loop (T_1, T_3, T_4, T_5, C_{fb}) as shown in Fig. 5.9(a) and (b). However, predominantly, the size of T_2 determines the t_f and t_{pHL} which monolithically decrease while the width of T_2 increases. During this pull-down transition of the inverter operation, T_2 can be viewed as a common-source amplifier. The calculated unity-gain frequency of T_2 is approximately 40 KHz. The overlap capacitance between gate and drain is 420 fF which acts as a Miller capacitance. From the target operating speed of the inverter at less than 10 KHz, the impact of Miller effect could be safely neglected.

The final transient simulation waveform of the 7T inverter showing all its internal nodes are illustrated in Fig. 5.10.

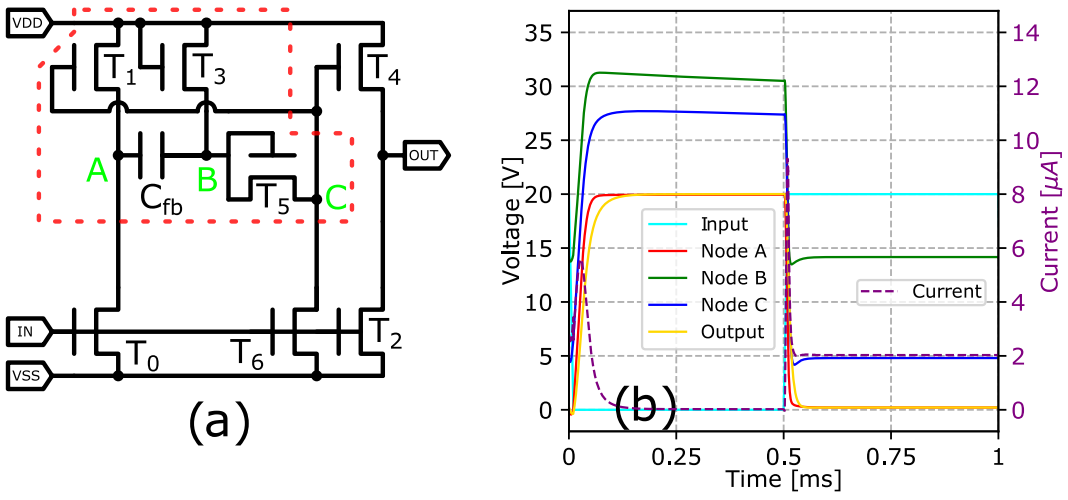


Figure 5.10: (a) The schematic of the 7T inverter. (b) The transient simulation of all the nodal voltages.

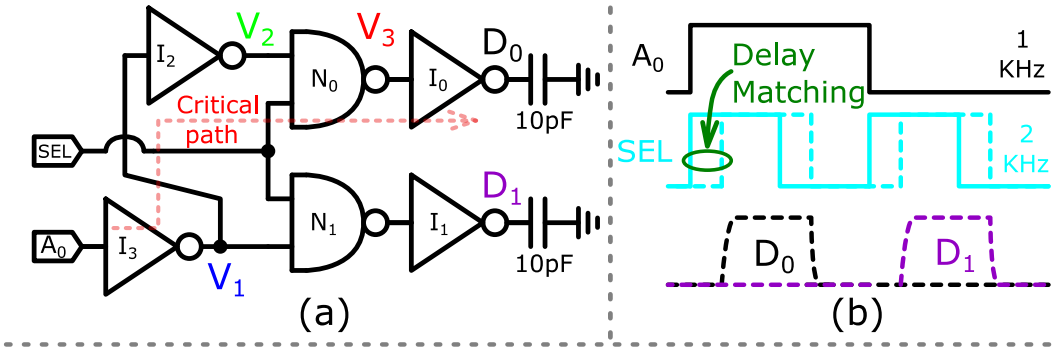
5.3 Multi-stage logic circuits with bootstrapped gates

From the analysis in the last section, bootstrapped logic gates demonstrate CMOS-like properties which have the potential to address the low stage-to-stage gain and high static leakage current problems associated with previous implementations. When cascaded into multiple stages, complex logic can be realized on the panel. In addition, the benefit of low-temperature fabrication capability of a-Si:H TFTs has enabled the possibility to realize flexible displays [42, 57]. Multiple groups have showed reliable pixel circuits on flexible substrate [78, 79, 57]. If bootstrapped logic circuits could be combined with the pixels onto the same substrate, an integrated low-cost display system may be realized. To demonstrate the feasibility, a decoder implemented on flexible substrate with low-temperature a-Si:H TFTs is proposed. The decoder is used to deliver row-scanning signals for the pixel array. For example, a display panel with a resolution of $m \times n$ has n row-select pads. If a decoder is used, it could drastically reduce the number of bonding pads between the panel and external ICs from n to only $\lfloor log_2^n \rfloor + 1$, which lowers the cost and increases the integration level. The detailed circuit design, simulation, and measurement results are provided in the following sections.

5.3.1 Design and simulation of a 1-to-2 decoder

The gate-level schematic of a 1-to-2 decoder, which contains six logic gates, is illustrated in Fig. 5.11(a). The load capacitance is set to be $10\,pF$ to represent a row of pixels on the display panel of a typical hand-held device [80]. The two input signal (A_0 and SEL) and output signal of (D_0 and D_1) waveforms are shown in Fig. 5.11(b). The geometries of devices in the gates are summarized in Fig. 5.11(c).

Both conventional and bootstrapped logic gates were used to construct the same



(c)

Device	T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	C_{fb}
W (μm)	100	100	200	200	200	40	20	200	20	100	300
L (μm)	20	20	20	20	20	20	20	20	20	20	300

Figure 5.11: (a) The gate-level schematic of a 1-to-2 decoder with node voltages and the critical path labeled. (b) The input signal waveforms of A_0 and SEL, as well as the output signals D_0 and D_1. (c) The geometries of the devices in the logic gates.

decoder to compare their performance. Fig. 5.12(a) and (b) show the transient voltage and current response of the decoder using conventional and bootstrapped logic gates, respectively. The average current (I_{avg}) dropped from $38.2\,\mu A$ to $6.18\,\mu A$ with the bootstrapped logic gates, which is an 80% reduction in average power consumption. Fig. 5.12(c) shows that the stage-to-stage voltage-swing deteriorated from $14.9\,V$ at V_1 to $3.68\,V$ at V_{out} with the conventional logic gates, causing a 75% loss in only four stages. Meanwhile, the decoder with bootstrapped gates had a constant voltage-swing of $20\,V$ throughout all four stages. Therefore, the comparison results have clearly demonstrated the advantages of the bootstrapped logic gates in maintaining stage-to-stage gain and reducing power consumption.

However, realization of multi-stage logic requires careful balancing of delays in the re-converging signal paths. Failure to comply with this may result in unintended glitch as shown in D_0 signal in Fig. 5.12(b). Such behavior is the result of different signal arrival time to the two NAND gates (N_0 and N_1), causing undesired cross-talk between two rows. It could be corrected by delaying the SEL signal with an inverter

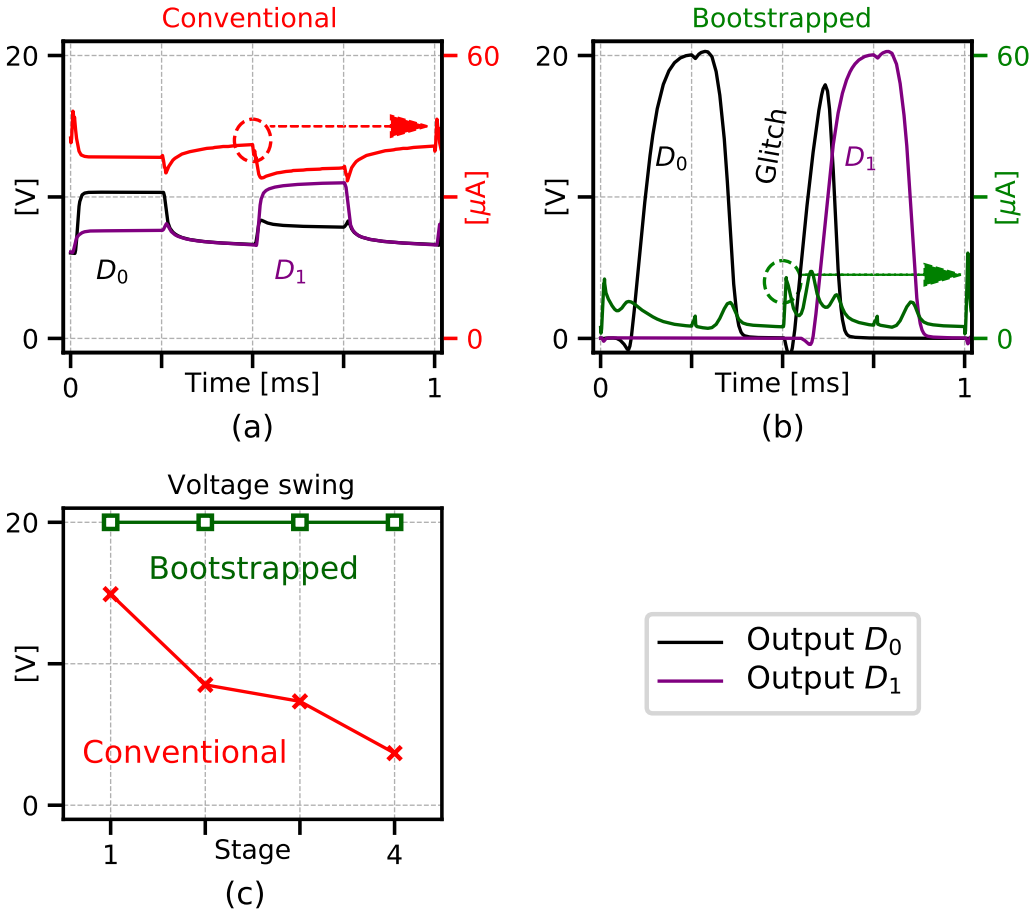


Figure 5.12: The transient voltage and current waveforms of the decoder with (a) conventional and (b) bootstrapped logic gates. (c) The stage-to-stage voltage swing of both decoders.

delay.

5.3.2 The impact of the ΔV_T degradation of a-Si:H TFTs

Simulation results in previous sub-section show a feasibility of realizing multistage row decoder with desirable characteristics. However, the disordered properties of the a-Si:H channel and a-SiN$_x$:H gate dielectric layers can introduce voltage-bias induced degradation which has been commonly modeled as a threshold-voltage shift (ΔV_T) [59, 52]. Therefore, it is necessary to investigate its impact on the performance of complex logic logic circuit such as decoder. It has been shown that the ΔV_T can be approximated by a stretched-exponential relationship [56] shown in Eq. (5.10).

$$\Delta V_T(t) = (V_{GS} - V_T) \times \left\{1 - exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{5.10}$$

The characteristic time constant τ and dispersion parameter β are specific to fabrication conditions which can be extracted by measuring bias-stress performance of individual TFTs.

Higher ΔV_T results in poor t_r and t_{pLH}. Consequently, the SEL signal should also be adjusted to match the increased gate delay to avoid aforementioned glitch. The Eq. (5.10) can be also utilized to estimate the increase in delay. In a continuous row-scanning operation of a display panel, the input buffers (inverters I_2 and I_3 in Fig. 5.11(a)) have a 50% duty cycle. Then, for some logic gates in the decoder, the accumulate ΔV_T could be approximated as half of the time that the display is on. The simulated maximum glitch level vs. SEL delay under progressive ΔV_T is shown in Fig. 5.13(a). For instance, if the ΔV_T reaches $2\,V$, the initial $50\,\mu s$ SEL delay is not sufficient to limit the glitch shown in Fig. 5.13(b). According to Fig. 5.13(a), a minimum of $70\,\mu s$ SEL delay is required to eliminate the glitch as illustrated in Fig. 5.13(c). Therefore, the sizing of TFTs in the decoder should consider the maximum ΔV_T that TFTs would accumulate during their expected life-time and the maximum allowed programmable delay of the SEL signal.

5.3.3 Impact of applied mechanical strain

Prior reports [58, 56, 63] have demonstrated that mechanical strain has an effect on the mobility of the TFTs. When the applied strain is tensile (compressive), the μ_n is increased (decreased). Moreover, the mobility deviation is higher when the bending direction is parallel to the channel length [57, 78, 64].

The applied strain affects the ΔV_T during bias-stress, as compressive strain results in the worst TFT degradation. These behaviors may be explained with the defect-

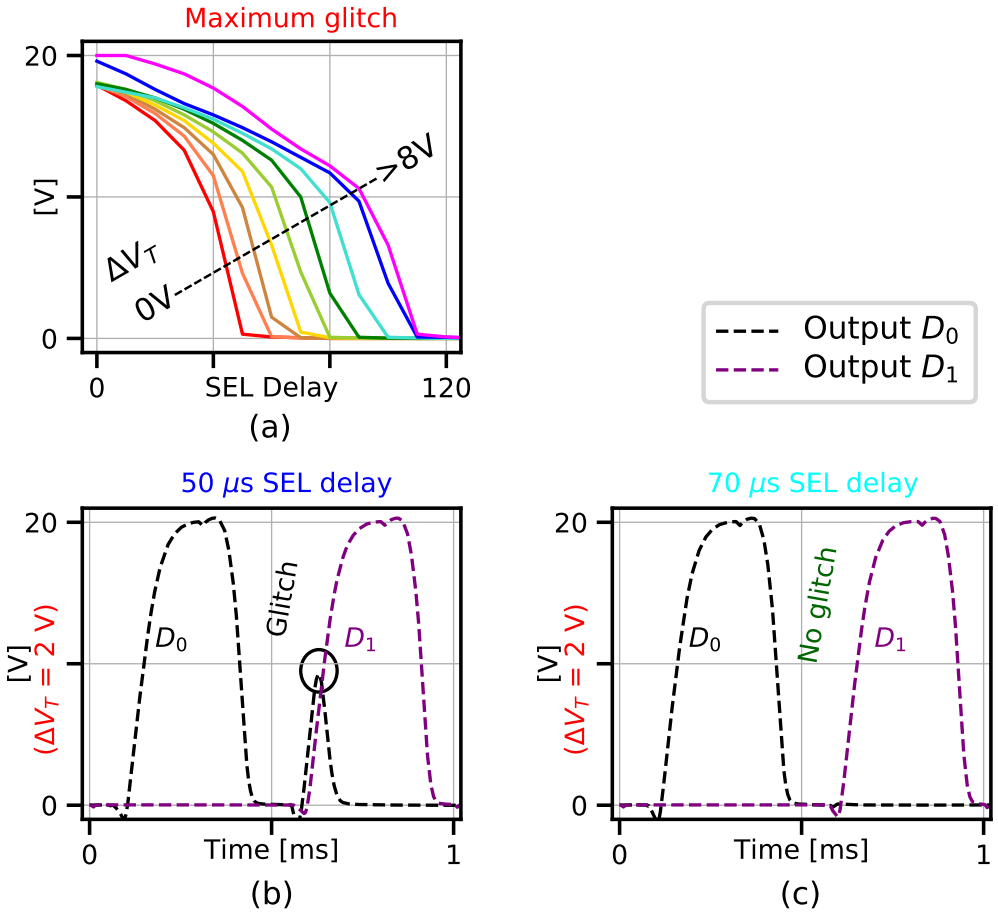


Figure 5.13: (a) The simulated maximum glitch level vs. SEL signal delay with increasing ΔV_T from $0\,V$ to $8\,V$ (b) The output signals with $50\,\mu s$ SEL signal delay at $\Delta V_T = 2\,V$ showing the glitch (c) The output signals with $70\,\mu s$ SEL delay showing no glitches at $\Delta V_T = 2\,V$.

pool model where the tensile or compressive strain is either healing or breaking the weak silicon-silicon bonds in the a-Si:H channel layer [56, 64]. A simulation of ΔV_T vs. stress time under flat, tensile, and compressive strain conditions is shown in Fig. 5.14(a) using Eq. (5.10).

Assuming that the decoder operates for 48 hours under compressive strain, the accumulated ΔV_T is roughly $2\,V$ estimated from Eq. (5.10). As indicated in Fig. 5.14(a), a $70\,\mu s$ delay in SEL signal is required to suppress the glitching. To demonstrate the delay-matching results, output waveforms are shown in Fig. 5.14(b) and (c), demonstrating a glitch-free decoding operation.

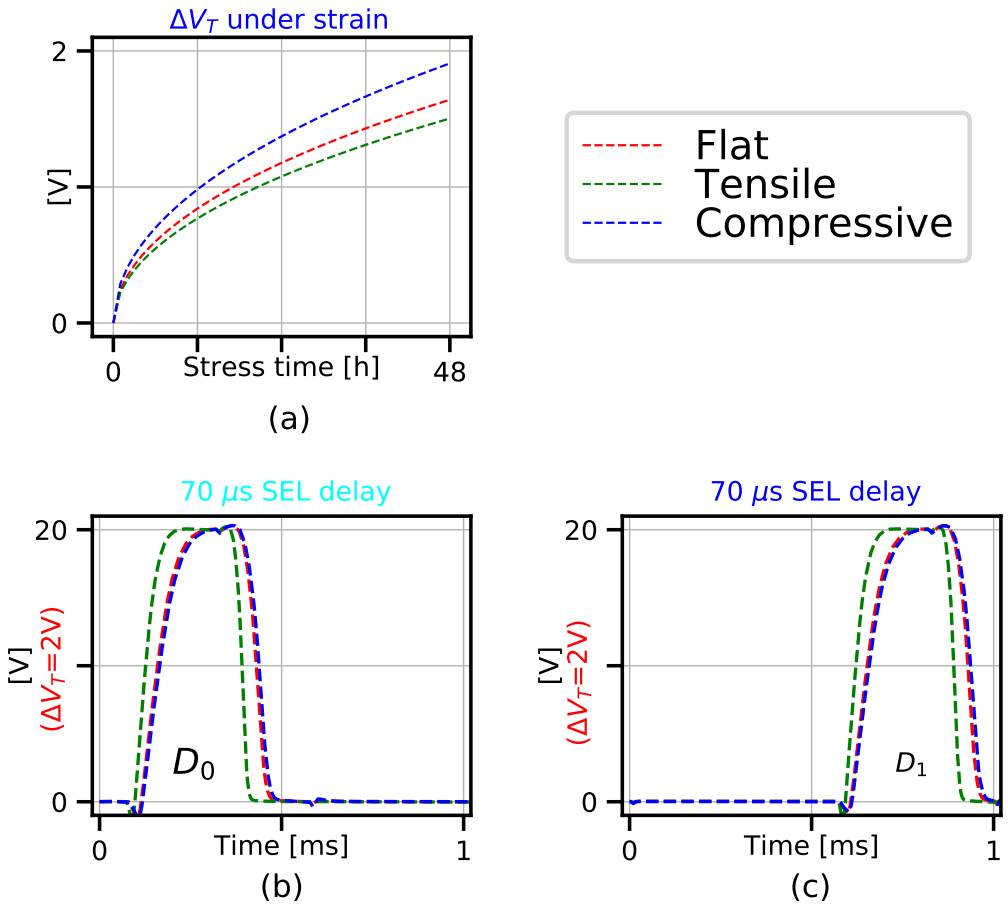


Figure 5.14: The comparison of (a) simulated ΔV_T and output voltages (b) D_0 and (c) D_1 of the 7T inverter under flat (red), tensile (green), and compressive (blue) strain conditions.

From the detailed analysis and simulations above, it becomes necessary to consider μ_n variation and ΔV_T differences under bending when designing flexible circuits with TFTs. These design parameters could impact the life-time of the circuits if not chosen properly.

5.3.4 Fabrication and experimental results

To verify the performance of flexible a-Si:H TFT circuits, a 1-to-2 decoder with bootstrapped logic gates has been fabricated on a plastic substrate (PEN) along with test TFTs for process parameter extraction. The minimum overlap design rule and channel length were 15 μm and 20 μm, respectively. The TFTs were laid-out with a conven-

tional invert-staggered back-channel-etch (BCE) structure shown in Fig. 5.15(a). The a-Si:H and a-SiN$_x$:H layers were deposited using PECVD processes with a maximum temperature of 170°C. The detailed fabrication process can be found in [57]. Measured I_{DS} vs. V_{GS} curves of a test a-Si:H TFT ($W/L = 100\,\mu m/20\,\mu m$) under flat, tensile, and compressive strain conditions are shown in Fig. 5.15(b). The inset of Fig. 5.15(b) shows that the tensile strain caused the TFT to have slightly higher mobility (+2.5%) and the opposite for compressive strain (−2.9%), which was consistent with the theoretical model. The applied strain conditions were conducted by taping the PEN substrate onto a convex or concave metal sample holder shown in Fig. 5.15(c) and (d). The bending radius was $\sim 40\,mm$ corresponding to a calculated strain of ±0.3%. The test TFT showed a field-effect mobility (μ_n) of $0.71\,cm^2/Vs$, sub-threshold slope (SS) of $0.64\,V/dec$, and $V_T \sim 4.54\,V$.

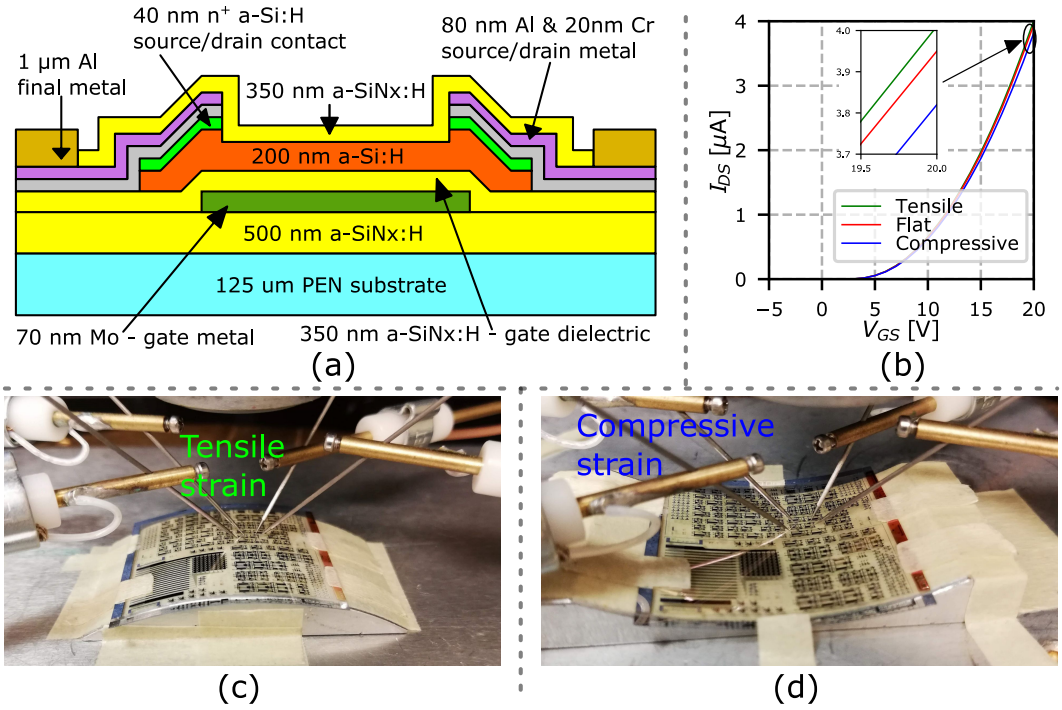


Figure 5.15: (a) The cross-sectional schematic of the a-Si:H TFT logic circuits on PEN substrate. (b) The I_{DS} vs. V_{GS} curves of a TFT with $W/L = 100\,\mu m/20\,\mu m$ under flat, tensile, and compressive strain conditions. The inset shows the deviation in I_{DS} near $20\,V$. The experimental setup of the flexible circuits under applied (c) tensile strain and (d) compressive strain.

The micro-graph of the 1-to-2 decoder and the test-bench setup is shown in Fig. 5.16(a) and (b), respectively. All the TFTs were oriented the same way so that they experience the same mechanical strain conditions [78, 57, 64]. Moreover, the layout followed the conventional standard-cell style with shared power and ground rails to minimize area. The input signals were generated by an ArduinoMega micro-controller and amplified to $0\,V - 20\,V$ range. The output signals of the decoder were first connected to high-precision unity-gain amplifiers (TLE2144) with the load capacitor ($10\,pF$) attached. Then, the outputs of the unity-gain amplifiers were connected to an oscilloscope for waveform capturing. The role of the unity-gain amplifier is to mitigate the resistive coupling effect of the probes ($1\,M\Omega$) in series with the high output resistance (hundreds of $K\Omega$) of a-Si:H TFTs.

Fig. 5.17(a) shows the measured (solid lines) and simulated (dashed lines) ΔV_T of a TFT for a 48-hour continuous operation test under flat and bending conditions. The output waveforms with a $50\,\mu s$ delay in SEL signal are shown in Fig. 5.17(b). Because the increase in ΔV_T was not compensated sufficiently, a glitch was clearly observed in the D_0 signal. According to Fig. 5.17(a), the worst-case ΔV_T of approximately $2\,V$ had occurred for the TFTs under compressive strain. Therefore, using Eqs. (5.2)-(5.10), a calculated delay of $70\,\mu s$ was set from the beginning of the decoder stress test to avoid circuit malfunction during the entire operational life-time. After the $70\,\mu s$ delay was applied, the decoder could operate without any glitch throughout the 48 hours as shown in Fig. 5.17(c). Variations in μ_n and ΔV_T caused by different mechanical strain conditions were also observed and the results were consistent with simulations. As a result, the programmable delay-matching method is effective in controlling undesired cross-talk by mitigating the glitching behavior. The decoder was able to maintain full output-swing throughout the stress-test period. Based on measurement results, the extrapolated maximum operating frequency of this decoder could reach $4.9\,KHz$, which is capable of refreshing the rows of a QVGA display under

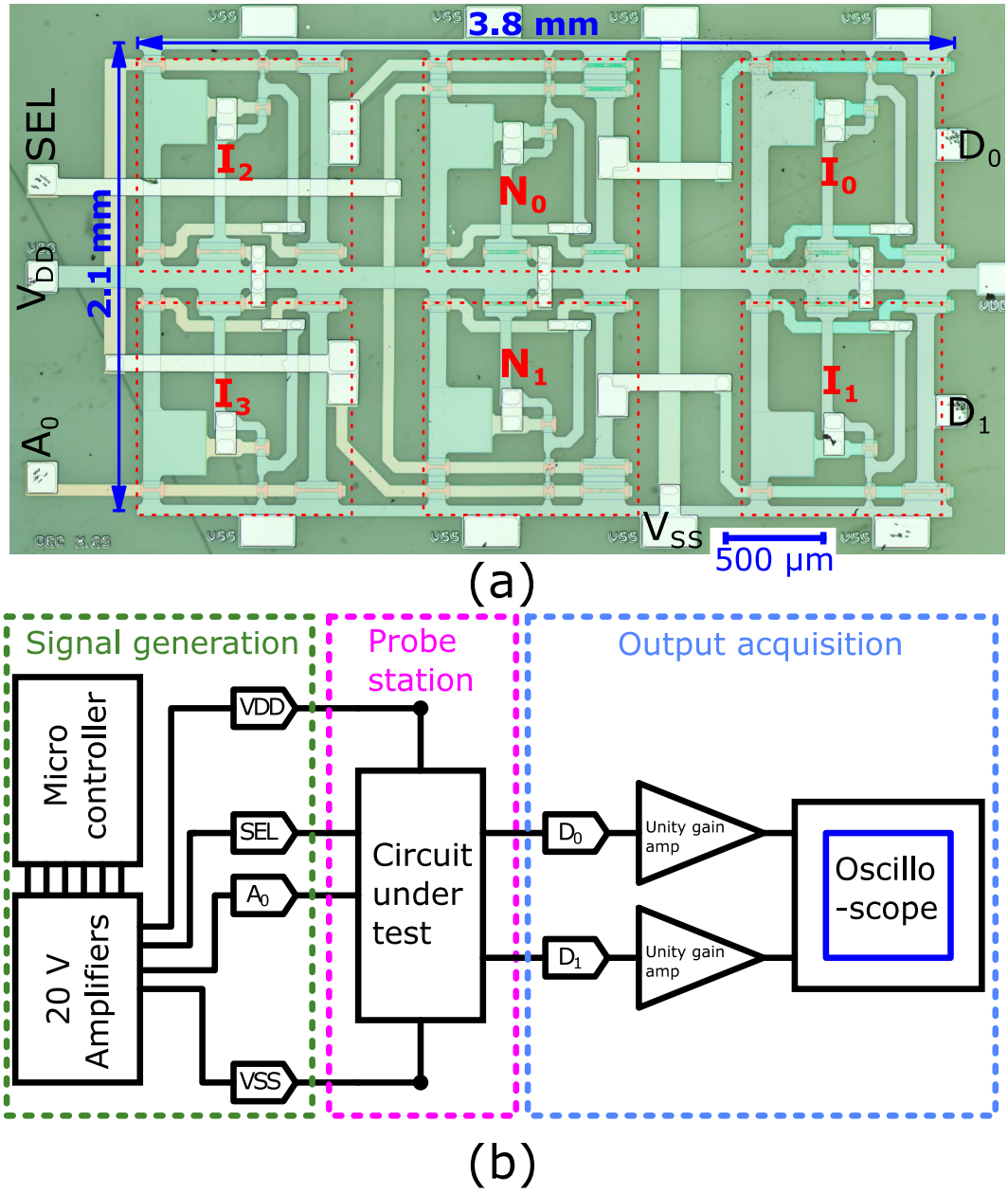


Figure 5.16: (a) The a micro-graph and (b) the test-bench of the 1-to-2 decoder.

compressive strain condition. The operating frequency could increase to suit higher resolution displays after sizing the TFTs appropriately.

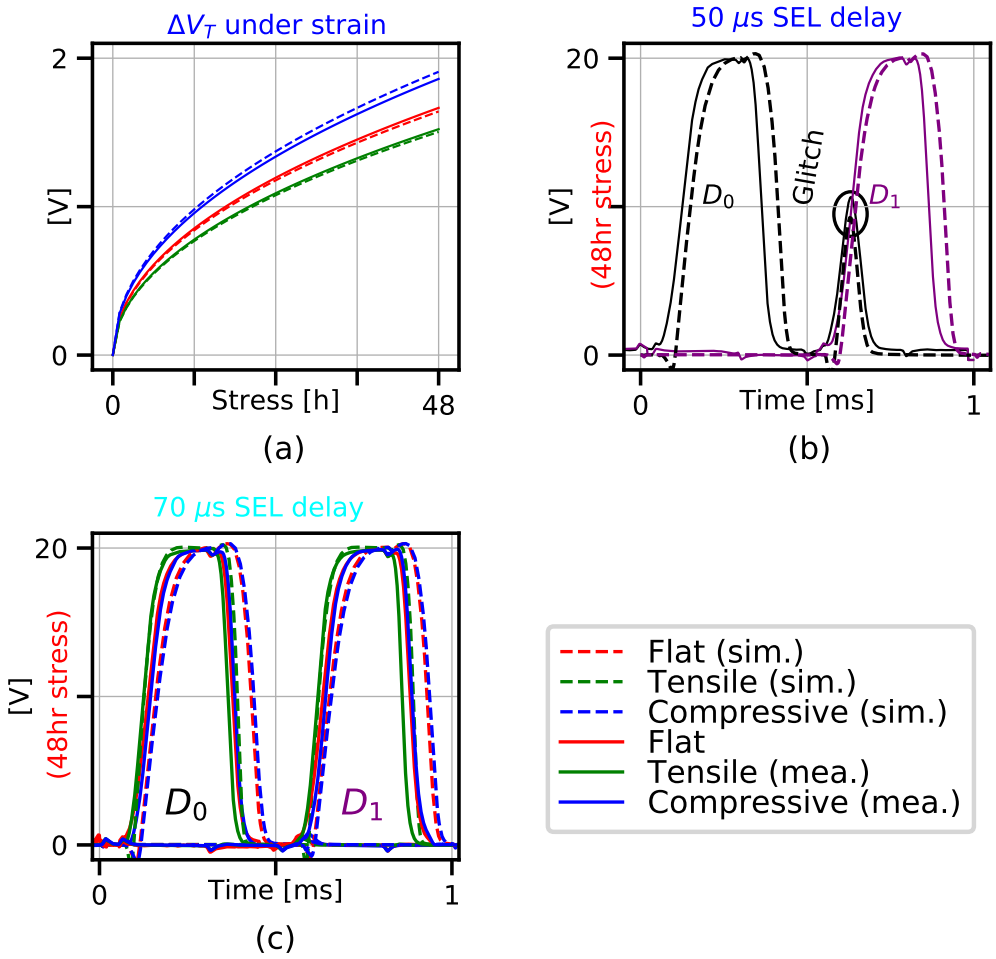


Figure 5.17: (a) The measured (solid lines) and simulated (dashed lines) ΔV_T of the decoder under flat and bending conditions. (b) The output waveforms after operating for 48 hours with a 50 μs delay on SEL signal. Glitch in D_0 is clearly observed. (c) The output waveforms after operating for 48 hours with a 70 μs delay on SEL signal. Glitch is not observed.

5.4 Area-efficient bootstrapped logic gates

From the successful demonstration of flexible multi-stage logic circuits with bootstrapped logic gates presented in the previous sections, there is great potential to use such logic style to realize more complex logic circuits [2].

However, to form macro-sized circuits, the number of gates goes up and the footprint on the substrate rises drastically. It becomes crucial to design gates with less

[2]This chapter is an amended version of "Realization of an Energy-Efficient and Full-Swing Decoder with Unipolar TFT Technology", including modified figures and tables, by Q. Li, C.-H. Lee, M. Asad, W. S. Wong, M. Sachdev, published in the proceedings of Custom Integrated Circuits Conference 2020, with ©IEEE 2020. If citing any figure or table, please refer to the original publication.

area consumption, so that they can be packed much denser.

By observing the internal node-voltage behavior of the 7T inverter shown in Fig. 5.10, it can be seen that node A closely resembles the output which leads to the possible reduction of 2 TFTs (T_2 and T_4).

Then, novel area-efficient bootstrapped logic gates are proposed, the schematics of 5T inverter, 7T NAND, and 7T NOR gates are shown in Fig. 5.18(b), (c) and (d), respectively.

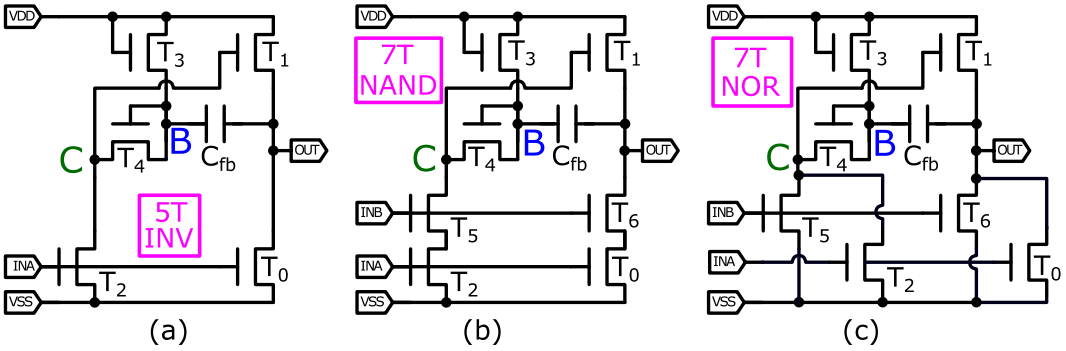


Figure 5.18: The schematic of (a) the conventional 2T inverter and the proposed (b) 5T inverter, (c) 7T NAND, and (d) 7T NOR gates.

The ability of the proposed logic gates to achieve full swing comes from the same bootstrapped feedback loop formed by T_1, T_3, T_4 and C_{fb} as the previous implementation. Using the 5T inverter as an example, the detailed operation of these gates are explained with simulation results on the side [81].

5.4.1 When input switches from ground to V_{DD}:

Shown in Fig. 5.19, pull-down TFTs (T_0 and T_2) become conductive and start draining V_{out} and node C. Meanwhile, a leakage current path (the green dashed line) is formed by two diode-connected TFTs (T_3 and T_4) and T_2 operating in linear mode. This direct path keeps node C voltage to be slightly above ground level and much lower than the threshold-voltage so T_1 remains off. As a result, V_{out} could be lowered to ground level. At the same time, node B is held at approximately half of V_{DD} due to

voltage division on the leakage path. This voltage difference between node B and C would function as a trigger for the feedback loop in the second half of the inverter operation.

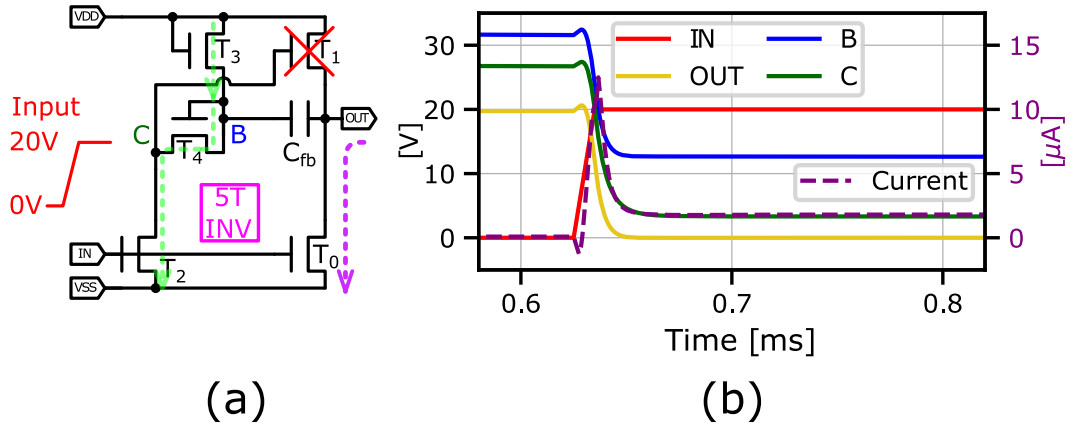


Figure 5.19: The (a) schematic and (b) the waveform including input, output, internal node B and C of the 5T inverter during output pull-down transition. (TFTs marked with red crosses are turned off. The dashed pink lines represent current flow to charge and discharge the output.)

5.4.2 When input switches from V_{DD} to ground:

Shown in Fig. 5.20, pull-down TFTs (T_0 and T_2) are turned off blocking all leakage paths to ground. Since there already exists a voltage difference between node B and C from the first half of the operation, current supplied by V_{DD} rail then starts to flow into node C which gradually turns on T_1. Next, T_1 begins to raise V_{out} which also pushes node B voltage to be higher. This positive feedback loop (the blue dashed line) formed by T_1, T_4, and C_{fb} eventually leads to $V_B \approx \frac{3}{2}V_{DD}$, $V_C \approx \frac{3}{2}V_{DD} - V_T$, and $V_{out} = V_{DD}$ after reaching steady-state. It is observed that that the pull-up speed is generally slower compared to pull-down. This is due to the reducing over-drive voltage (V_{OV}) of T_1 when V_{out} rises.

Next, to further investigate the pull-up operation of the inverter, propagation delay (t_{pLH}) and rise time (t_r) were simulated. The results are shown in Fig. 5.21 which demonstrates the impact from each device, including T_1, T_2, T_3, T_4, and C_{fb} when their

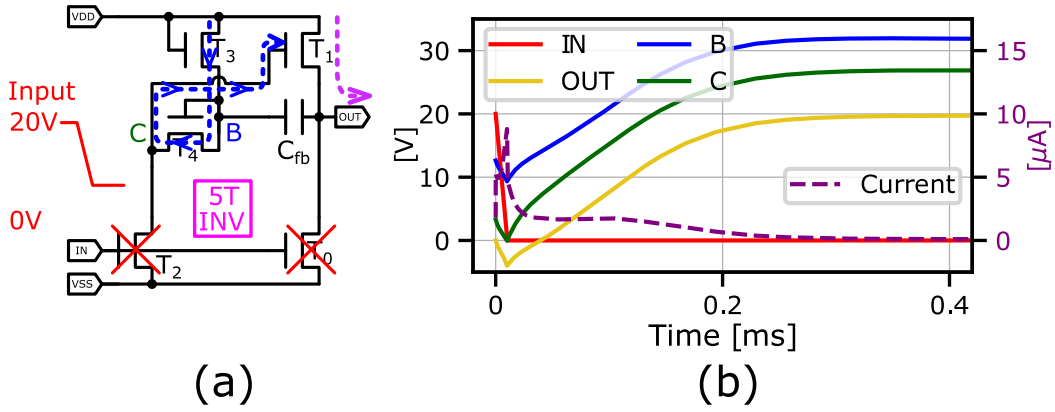


Figure 5.20: The (a) schematic and (b) the waveform including input, output, internal node B and C of the 5T inverter during output pull-up transitions. (TFTs marked with red crosses are turned off. The dashed pink lines represent current flow to charge and discharge the output. The blue dashed line is the current path of the bootstrapped feedback loop.)

individual sizes vary. Here, the geometry of T_0 was kept at $W/L = 100\,\mu m/20\,\mu m$ as a constant and all the other devices were set to have the same channel length of $20\,\mu m$. The load capacitance was set to be $10\,pF$. The results show that increasing geometry of T_1, T_3, T_4, and C_{fb} generally lead to lower t_{pLH} and t_r values since all these devices contribute positively to the feedback loop. However, T_2 acts in the opposite way. The reason is that T_2 is turned off when input is low, therefore, it does not contribute any current to accelerate the feedback. However, with an increase in the geometry of T_2, the parasitic capacitance at node C becomes higher resulting in slower pull-up transition. Moreover, when T_2 is larger, the leakage path could drain more static current when input is high. Thus, T_2 should be designed to the minimum size to have better pull-up speed and lower leakage current.

After multiple cycles of simulations and optimization that balance operating speed

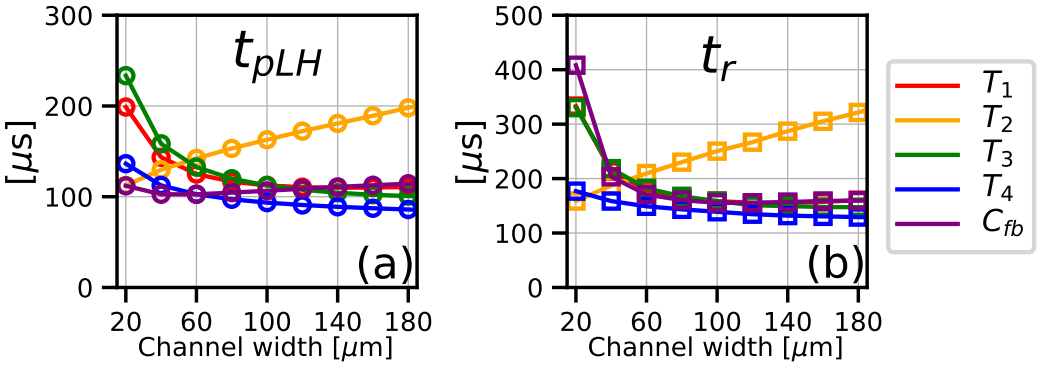


Figure 5.21: (a) The t_{pLH} and (b) t_r of the inverter output when varying the width of T_1, T_2, T_3, T_4 and C_{fb}.

and footprint. The device geometries were determined and summarized in Table 5.1. Subsequently, device sizes of NAND and NOR gates could be generated by using logical effort analysis.

Table 5.1: Device geometries of the 5T inverter

	T_0	T_1	T_2	T_3	T_4
Width (μm)	100	100	20	100	40

Then, the 5T inverter is put into a circuit environment to test its capability along with the conventional 2T and 7T inverters.

5.4.3 Comparison of 2T, 4T, 5T and 7T inverters

A six-inverter buffer chain shown in Fig. 5.22, has been constructed to demonstrate transient stage-to-stage behavior of the 2T, 4T, 5T, and 7T inverters.

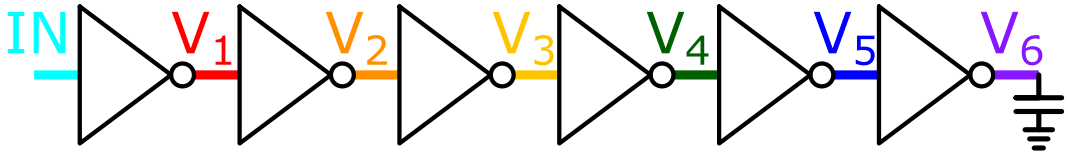


Figure 5.22: A six-inverter delay chain used to simulate the stage-to-stage behavior of 2T, 4T, 5T and 7T inverters.

Fig. 5.23(a), (b), (c) and (d) show the stage-to-stage output voltage swing of

four delay chains formed by the 2T, 4T, 5T and 7T inverters, respectively. The 4T inverter was designed with the same TFT widths for T_0, T_1, T_2 and T_3 and capacitor values as the 5T inverter to compare the new design with a more conventional TFT ivnerter circuit. The 5T and 7T inverters maintained a $20\,V$ swing at each stage as expected, while the 4T and 2T inverters had decreased swing of $17.6\,V$ (88% of supply) and $3.2\,V$ (16.0% of supply), respectively. The lower stage-to-stage gain of the 2T and 4T inverter-style logic gates would cause circuits to malfunction. In addition, the transient current for the 5T inverter chain is $6.5\,\mu A$ compared to $25\,\mu A$ for the 2T configuration (Fig. 5.23(e)), demonstrating the considerable power savings of the former. This low-power performance is also superior to the 4T and 7T inverter chains, which consumed an average transient current of $9.16\,\mu A$ and $10.5\,\mu A$, respectively, over the same period.

The analysis and simulation results have demonstrated the effectiveness of the proposed area-efficient logic gates which are capable of providing unity stage-to-stage gain and minimizing leakage current.

5.4.4 Fabrication and measurement results of logic gates

The proposed 5T inverter and 7T NAND gate have been fabricated on glass substrate with an industry standard 5-mask a-Si:H process. The cross-sectional view of the layers is shown in Fig. 5.24(a). The deposition temperature in the PECVD chamber was set at 170° maximum for the a-Si:H channel and a-SiN_x:H gate dielectric layers.

From the measured I-V curves in Fig. 5.24(b) and (c), device parameters were extracted. Carrier mobility, threshold voltage and sub-threshold slope values are $0.92\,cm^2/Vs$, $3.86\,V$ and $0.66\,V/dec$, respectively.

Measured transient waveform of the 5T inverter and 7T NAND gate were overlaid with simulation results shown in Fig. 5.25. The standard cells performed as proposed with full-swing output signals and much lower static leakage current.

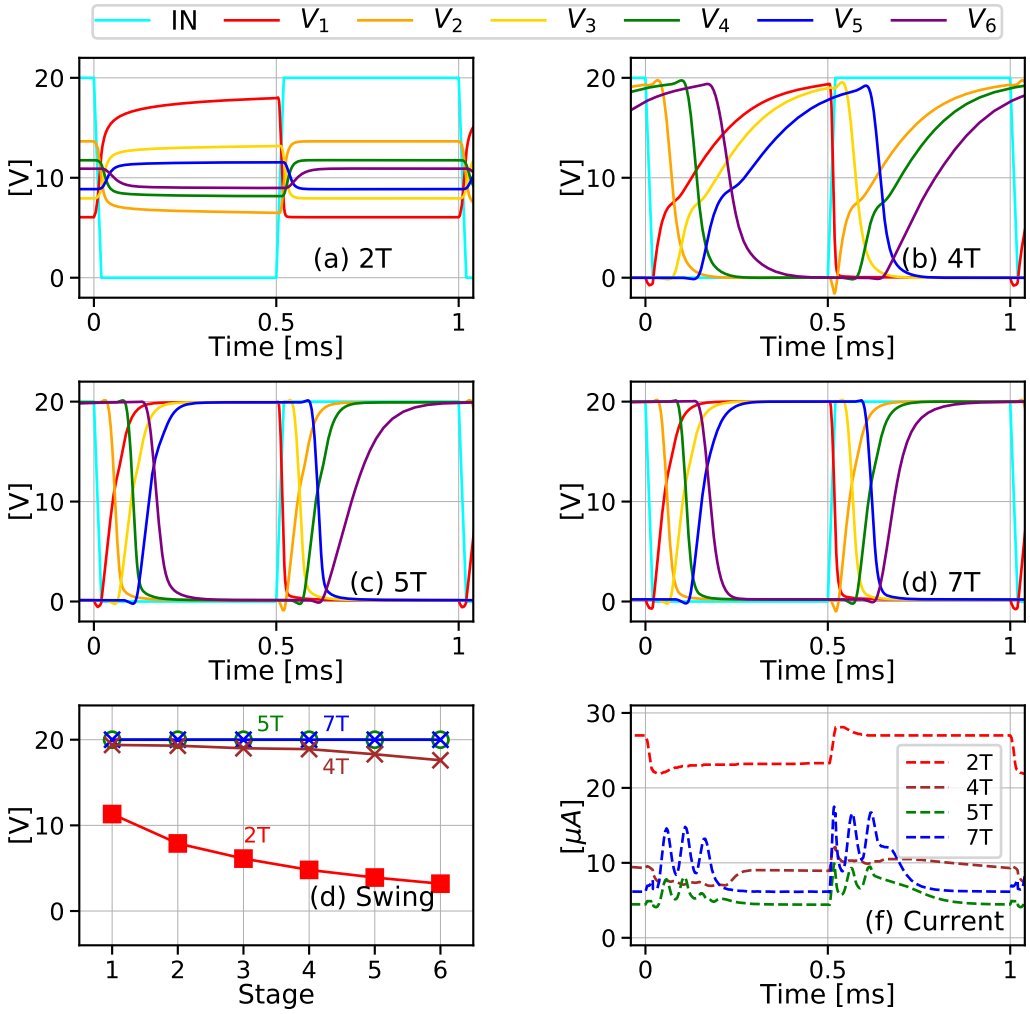


Figure 5.23: (a), (b), (c) and (d) show the transient voltage waveform of the buffers formed by 2T, 4T, 5T, and 7T invertes. (e) The comparison of the stage-to-stage voltage swing. (f) The comparison of transient current of the delay chains.

Fig. 5.26 summarizes the static leakage current and area reduction reduction of the proposed standard cells. More than 85% of static leakage current is achieved by all the standard cells when compared with conventional gates. Meanwhile, the footprint of the 5T inverter was 11% less than the one demonstrated in prior art [76]. The footprint of NAND and NOR gates with two to four input signals shown in Fig. 5.26(b) were also smaller than the ones presented in [76] with a reduction ranging from 12% to 32%.

In summary, the measurement and comparison results have proven the effective-

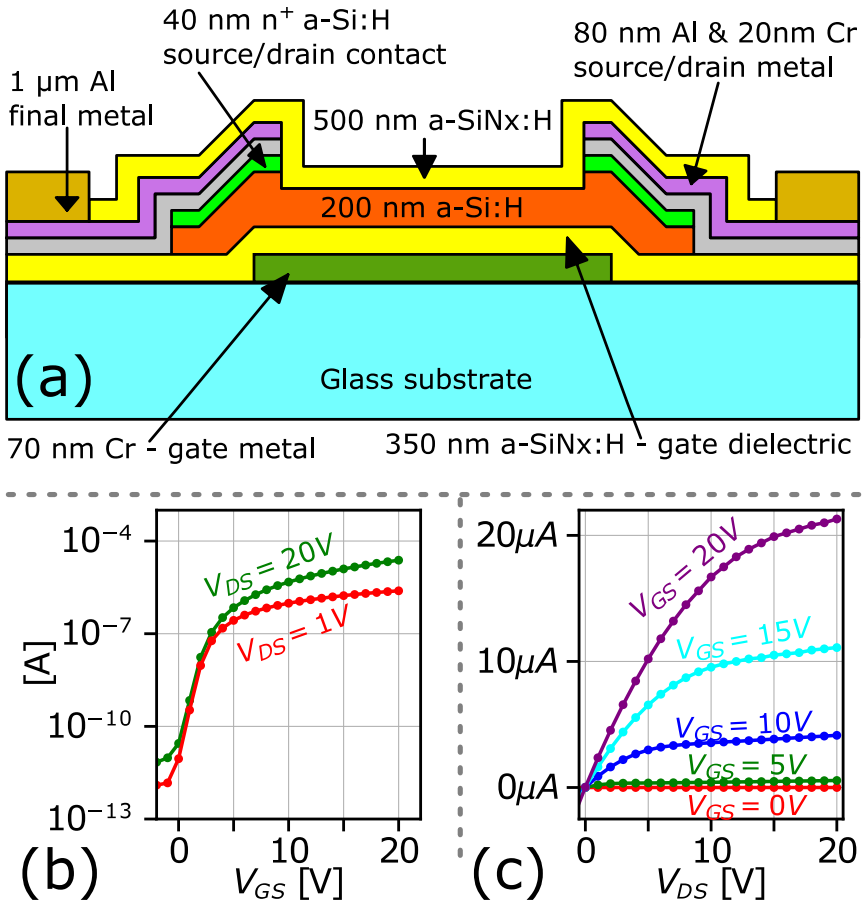


Figure 5.24: (a) The fabricated layers of a-Si:H TFTs on glass substrate. (b) The transfer (I_{DS} vs. V_{GS}) and output (I_{DS} vs. V_{DS}) curves of a TFT with the geometry of $W/L = 200\,\mu m/20\,\mu m$.

ness of the proposed standard cells in minimizing energy consumption and footprint.

5.5 Multi-stage logic circuit demonstration

To test the proposed standard cells in a multi-stage configuration, a 3-to-8 decoder has been designed and fabricated. The schematic and input/output waveform are shown in Fig. 5.27(a) and the optical micro-graph is shown in (b). The design is consisted of fourteen 5T inverters and eight 4-input NAND gates totaling 126 TFTs. The layout followed CMOS standard cell style with shared power supply and ground rails. The load capacitance of the decoder was approximately $10\,pF$. The total area of the decoder is $3.6\,mm \times 6.1\,mm$.

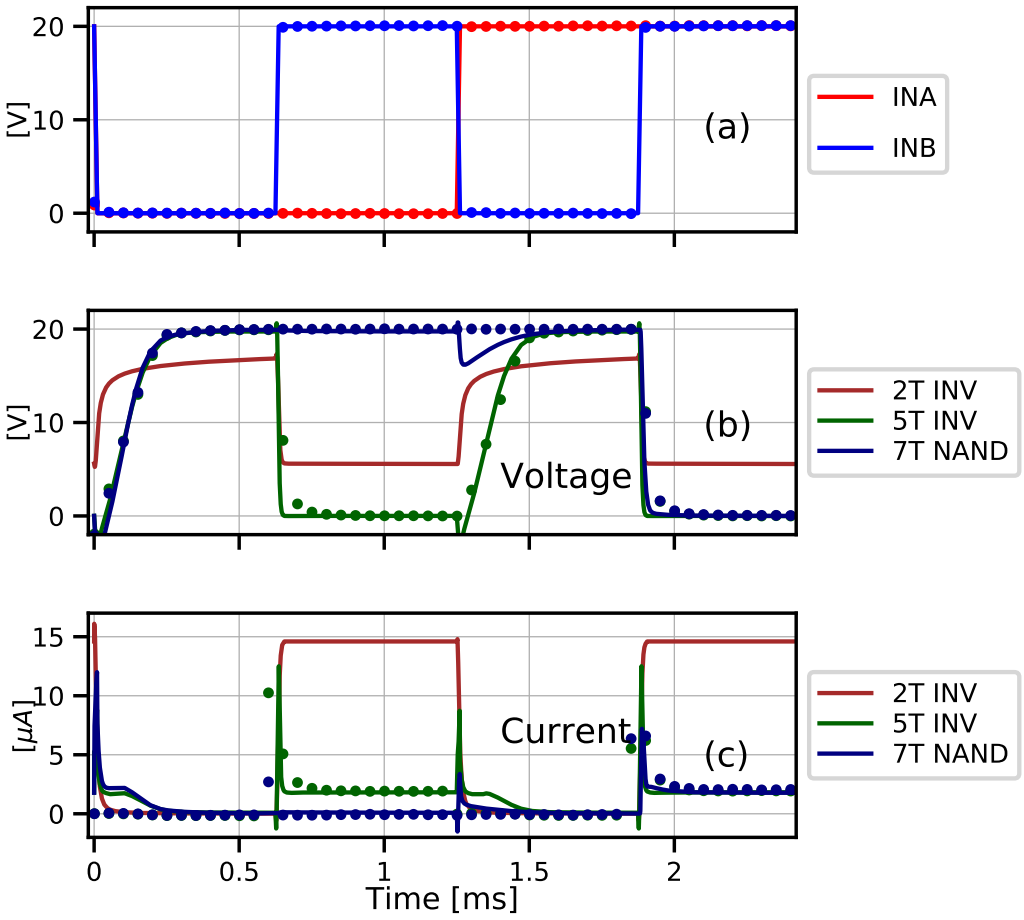


Figure 5.25: Overlaid transient voltage and current waveform of the 2T, 5T inverter and the NAND gate. Simulations are shown with lines and measurements are represented by dots.

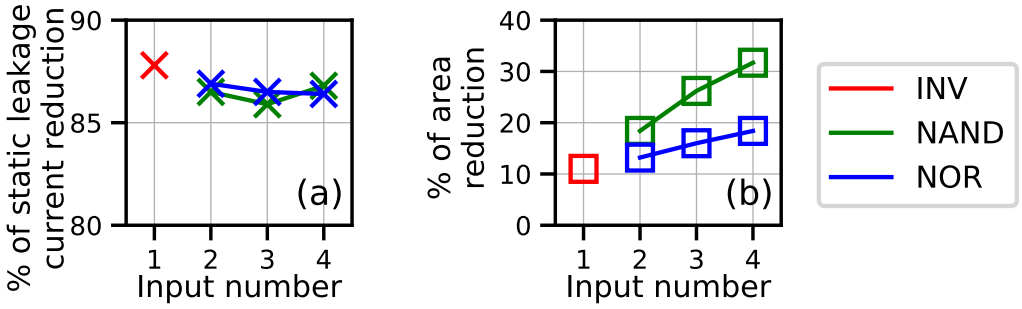


Figure 5.26: (a) The percentage of static leakage current reduction against conventional logic gates (b) The percentage of area reduction compared to prior art [76].

The decoder was characterized using the same test-bench as previous measurements. Shown in Fig. 5.28(b), the decoder is able to achieve rail-to-rail output swing as designed while running at 1.6 *KHz*. However, there were voltage glitches higher

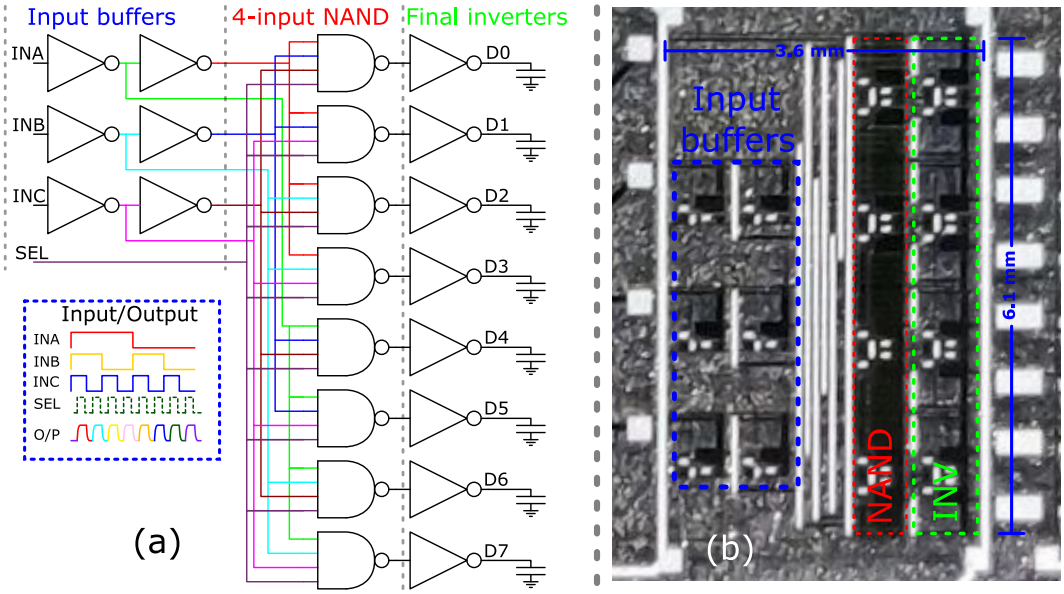


Figure 5.27: (a) The gate-level schematic with input/output waveform and (b) the micrograph of a 3-to-8 decoder.

than $12\,V$. Such undesired behavior is due to the different arrival time of the re-converging signals after the input buffer stage. These glitches have the potential to interfere the normal operation of a memory or display array.

By introducing a skew into the SEL signal could alleviate this problem. Shown in Fig. 5.28(a), a delay matching of $300\,\mu s$ has been inserted into the SEL signal. Then as demonstrated in Fig. 5.28(c), all the output signals have demonstrated low glitches less than the threshold voltage of the TFTs.

The average current was also measured to be $20.4\,\mu A$, which is an 85% reduction if the decoder was implemented by conventional logic gates. At the same time, the area is approximately 20% less if the gates were realized by the initial implementation of bootstrapped ones.

5.6 Comparison of TFT logic circuits

Table. 5.2 compares this work with other logic-circuit realizations with TFTs. Note that the proposed circuits in this work demonstrate full-swing over multiple stages

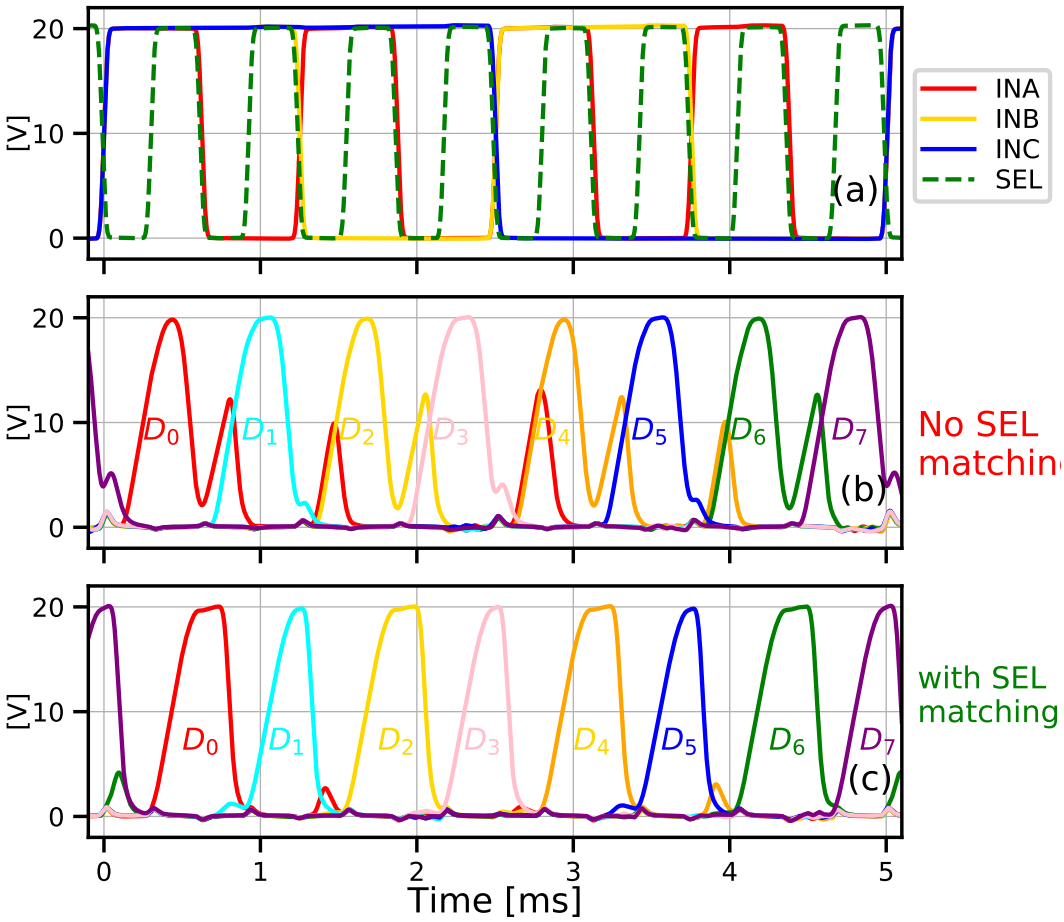


Figure 5.28: (a) Input signals of the 3-to-8 decoder. The dashed SEL signal is delayed to match other re-converging signals after the input buffer. (b) and (c) are the waveform of the eight output signals without and with SEL signal matching.

while maintaining low power consumption.

The proposed area-efficient logic gates has the best overall performance in terms of the full-swing and low-power features on top of area-reduction when compared to prior implementations of bootstrapped logic gates.

5.7 Realization of a flexible display backplane

From the detailed analysis and successful experimental results shown above, the proposed area-efficient, full-swing and low-power logic circuits can be integrated with a pixel array to demonstrate its effectiveness. The decoders controlling a column of 2T

Table 5.2: Comparison of logic circuits with thin-film transistors

	This work		Ref. [76]	Ref. [71]	Ref. [72]	Ref. [75]
Technology	**a-Si:H**	**a-Si:H**	a-Si:H	Dual-gate a-IGZO	Dual-gate a-IGZO	a-IGZO
Substrate	**Glass**	**Flex**	Glass	Glass	Glass	Glass
CMOS-like	**Yes**	**Yes**	Yes	No	No	No
Full swing	**Yes**	**Yes**	Yes	No	No	Yes[1]
Low power	**Yes**	**Yes**	Yes	No	No	Yes
Inverter Devices	**5T**	**7T**	7T	2T	2T	7T+1C
Circuits realized	**INV NAND 3-to-8 Decoder**	**INV NAND 1-to-2 Decoder**	INV	INV R.O.	INV NOR	INV

[1] The inverter requires an additional bias voltage signal to make it full-swing.

and 6T pixel arrays have been demonstrated as follows:

5.7.1 Row decoder + 2T pixel array

The overall schematic of the display backplane is shown in Fig. 5.29. The 3-to-8 decoder is used as the row-select function so that there would be only four control signals instead of eight.

The fabrication of the flexible wafer followed the same procedures and the deposition temperature was at $150°C$. The bending experiments were also carried out with the same aluminum sample holder with a radius of $40\,mm$ and the resulting strain of $\varepsilon = \pm 3\%$. The mobility of the a-Si:H TFTs have changed slightly during bending which can be seen from the variations of the rise/fall time and propagation delay

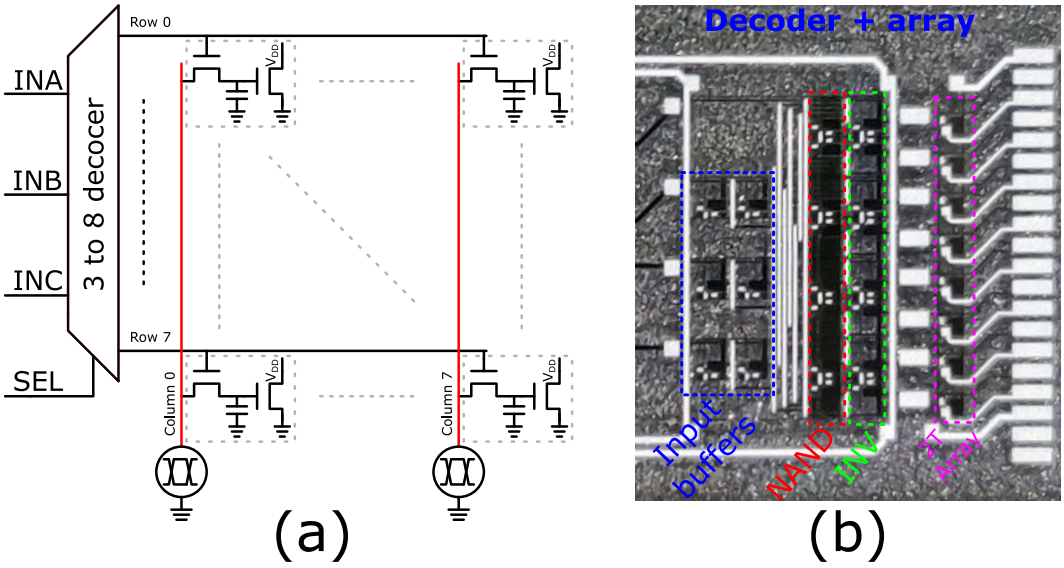


Figure 5.29: (a) The schematic of a 3-to-8 decoder controlling the row signals of a 2T pixel array. (b) The micro-graph of a fabricated decoder with one column of 2T pixel circuits.

shown in Fig. 5.30.

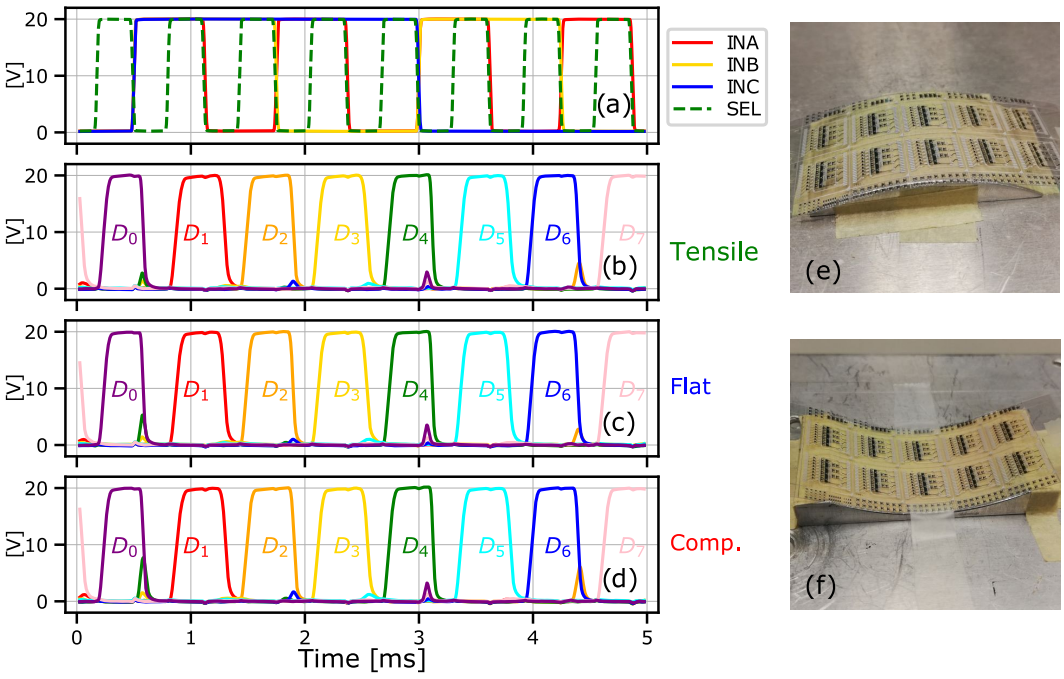


Figure 5.30: (a) Transient waveform of the input signals of the 3-to-8 decoder. (b) (c) and (d) The measured output waveform of the decoder under tensile, flat and compressive strain conditions. (e) and (f) The bending setup of the flexible decoder wafer.

Meanwhile, a 8×1 column of 2T pixels were attached to the decoder to verify the row-selecting capability. The output current of each pixel could be probed individually

to collect data. Fig. 5.31(a) shows transient waveform of the output current when V_{data} scans from $8\,V$ to $15\,V$ under flat situation. In addition, the summary of current vs. V_{data} is shown in (b) under various bending conditions.

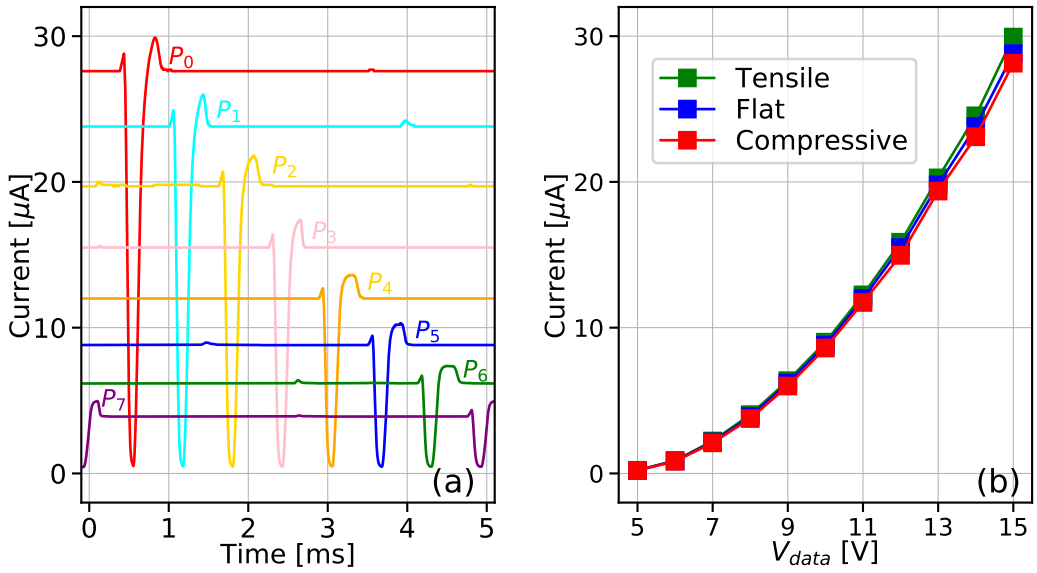


Figure 5.31: (a) Transient waveform of the output current at a V_{data} range of $5\,V \sim 15\,V$ (b) The current vs. V_{data} curve of the 2T pixels.

5.7.2 Row decoders + 6T pixel array

After the simple 2T array addressing has been realized, it is possible to design row-select circuits for the 6T compensation pixel array. In order to control both the V_1 and V_2 timing signals for every row, two separate decoders are required. Shown in Fig. 5.32, the schematic of the 6T pixel array addressing has been provided. The number of row-select pads required becomes twice as much as the 2T array implementation.

The input timing-control signals and the individual output of the two decoders are shown in Fig. 5.33. It can be seen that all the V_1 and V_2 signals can be generated properly.

Then, the compensation performance of the 6T pixel driven by decoders has also been investigated. Under progressive ΔV_T values, the output current shows less than 3% variation from the initial state in the full V_{data} range in Fig. 5.34.

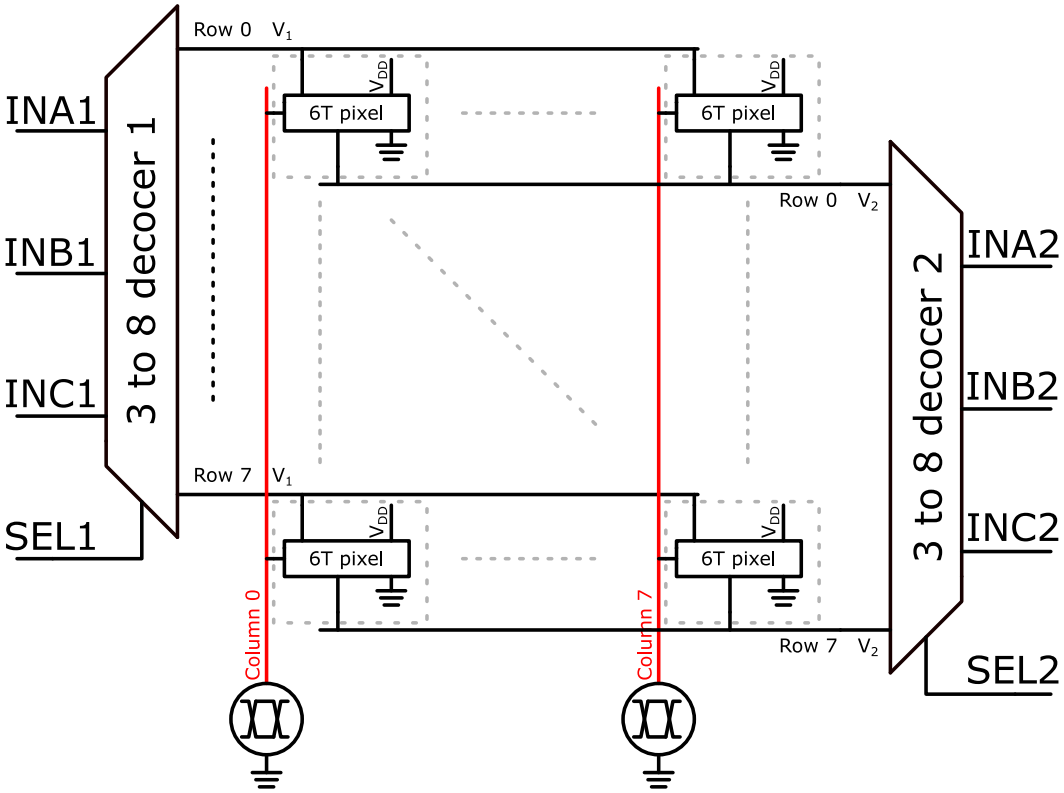


Figure 5.32: The schematic of two decoders driving a 6T pixel array.

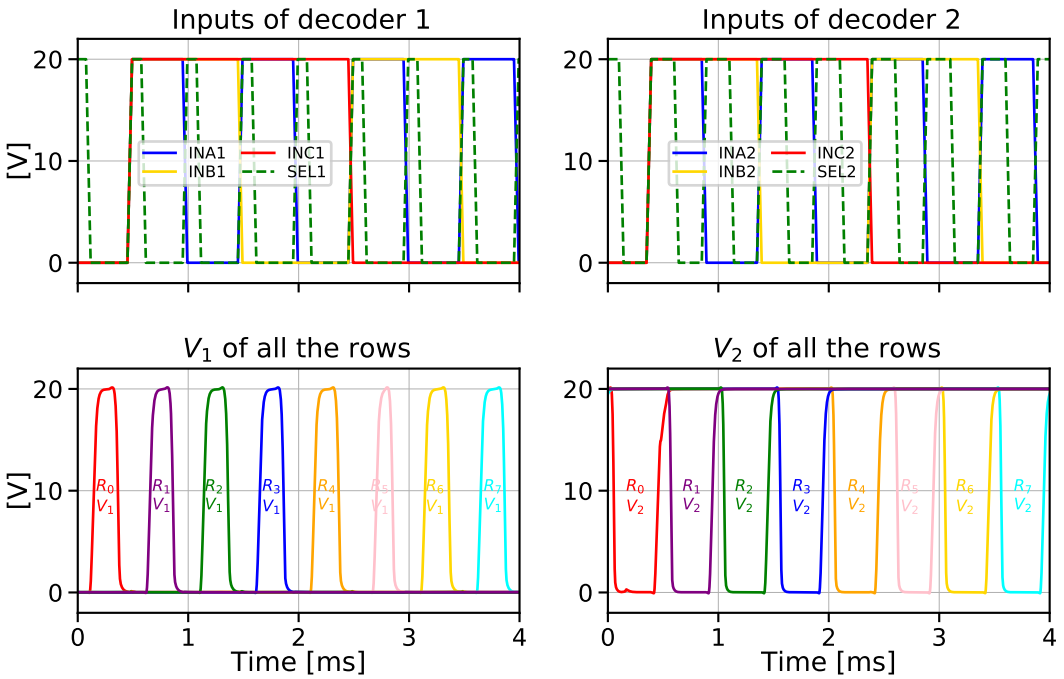


Figure 5.33: The input and output signals of the two decoders generating the V_1 and V_2 signals for a 6T pixel array.

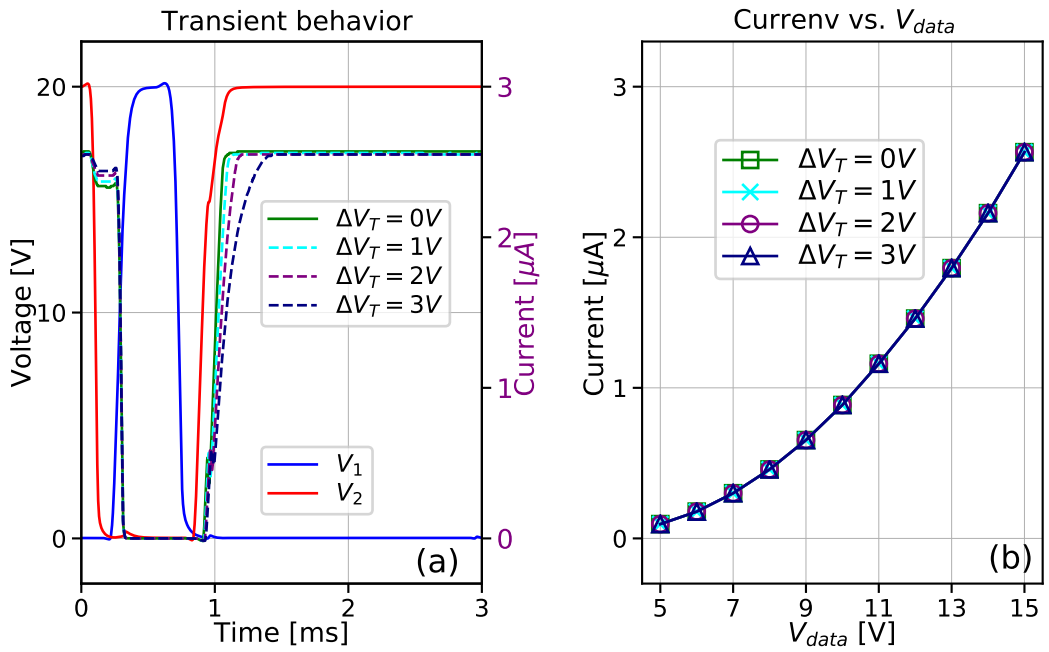


Figure 5.34: (a) V_1 and V_2 signals and the transient output current with progressive ΔV_T of the 6T pixel circuit. (b) The output current vs. V_{data} of 6T pixel array with progressive ΔV_T.

5.8 Summary

In summary, this chapter has demonstrated full-swing and low-power logic gates using the bootstrapped technique so that CMOS-like logic circuits can be successfully realized by unipolar n-type only a-Si:H TFT technology. The proposed area-efficient gates has been integrated into a 3-to-8 decoder which is capable of selecting rows of a display array. Its performance has been verified through simulation and measurement. Then, the realization of a scaled-down display panel was also achieved by attaching a column of 2T pixel array to the decoder. It demonstrated correct behavior as desired. Moreover, by combining two decoders, it is also possible to address the 6T compensation pixel circuit proposed in the previous chapter. Simulation results have shown the correct timing signals and compensation capability is also maintained.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The realization of low-cost flexible displays as a "system-on-flex" requires low-power light media, reliable pixel circuits and peripheral on-flex control circuits. Novel solutions to all these challenges have been addressed in this thesis.

The first major contribution presented in the thesis is a power-efficient pixel circuit using amorphous silicon TFTs and μLEDs configured in a novel method. Conventionally, the anode terminal of the OLED has be connected to the source of the driving TFT due a fabrication constraint. With a novel fabrication technique, μLEDs which possess much higher electro-luminescence efficiency, can be bonded with their cathode terminals to the drain of the TFT. In this novel pixel configuration, the display dynamic range is extended from eliminating the on-voltage of the diode. The analysis and experimental results have demonstrated significant increase of dynamic range and low-power features.

The second contribution is a novel 6-TFT compensation pixel circuit. Due to the well-known mobility degradation of amorphous silicon TFTs under voltage bias, pixel circuits supply less current to the light media over-time. The proposed 6-TFT pixel circuit uses a charge-transfer technique which utilizes a specific degradation

ratio between TFTs biased in linear and saturation modes. Two MIS capacitors form the core of the compensation mechanism. By balancing the capacitor components among the 6 TFTs, the output current of the pixel circuit remains the same under the same data voltage. In addition, when the pixel circuit operates under applied mechanical strain, the layout of the TFTs also plays a role in the compensation capability. When the TFTs are oriented the same way, the compensation remains consistent, otherwise, over- and under- compensation can be observed. Theoretical and experimental analysis has proved the effectiveness of the proposed 6-TFT pixel circuit.

The third contribution of the thesis is to provide a logic-gate-level solution to realize low-power and full-swing digital circuits on flexible substrate with amorphous silicon TFTs. Such digital logic circuits can be used as row/column drivers resulting in much less input signals required from the external ICs. Using a bootstrapped feedback network, primary logic gates, such as inverter, NAND, and NOR gates can be realized with full-swing output and low static leakage current. Using 5 TFTs and a capacitor, a bootstrapped inverter can be realized, as well as 7 TFT NAND and NOR gates. These novel logic gates provide desirable CMOS-like features and are area-efficient in the mean time compared to prior TFT logic implementations. As a proof of concept, a 3-to-8 decoder has been designed and fabricated on flexible substrate and its performance closely matched the simulations. Furthermore, a miniature "system-on-flex" has been realized by the decoder and a column of pixel circuits. The results have demonstrated the effectiveness of the novel logic circuit implementations.

6.2 Future work

To extend on the research work performed in this thesis, further investigations can be continued on all three aspects. For the topic on power-efficient pixel circuits, the proposed drain-cathode configuration with μLED can be applied onto other platforms,

such as CMOS and LTPS backplanes. While down-sizing the μLEDs to reach higher display resolutions, the uniformity of electro-luminescence across a large area should be further studied. The solution may come from novel circuit design or more advanced fabrication techniques.

For the aspect of compensation pixel circuits, the proposed method uses six TFTs and two control signals. Since the overlap capacitance negatively impacts the compensation performance, a self-aligned TFT fabrication process should be experimented to verify the performance of the proposed pixel circuit. Also, the repeated bending measurements should be carried out to find out the limits of the pixel circuit. In terms of materials, metal-oxide TFTs and printed organic TFTs can also be used to validate the compensation concept. Last but not the lease, future studies should always aim to reduce the TFT count so that the fill factor may improve to provide better visual quality.

For circuit implementations on flexible substrate with unipolar TFTs, more functions should be realized, such as memory, data conversion, power harvesting and etc. Only by integrating more functions on the same substrate, can the cost of flexible electronics go down. The proposed low-power and full-swing logic gates have enabled the realization of digital circuits, while much future work can be investigated with analog and mixed-signal circuits.

6.3 Contributions

Journal articles

1. **Q. Li**, C.-H. Lee, M. Asad, W. S. Wong, M. Sachdev, "Energy-efficient and full-swing logic circuits with unipolar TFTs on flexible substrate", in preparation

2. M. Asad*, **Q. Li***, C.-H. Lee, M. Sachdev, W. S. Wong, "Design and demonstration of high-brightness, power-efficient flexible micro-LED pixel circuits",

submitted to Nano Energy, (*equal contribution)

3. **Q. Li**, C.-H. Lee, M. Asad, W. S. Wong, M. Sachdev, "CMOS-like logic circuits with unipolar thin-film transistors on flexible substrate", IEEE Transactions on Electron Devices, volume 67, issue 2, page 512-517

4. M. Asad, **Q. Li**, M. Sachdev, W. S. Wong, "Size-dependent optoelectrical properties of 365 nm ultraviolet light-emitting diodes", Nanotechnology, volume 30, issue 50, page 4001

5. M. Asad, **Q. Li**, C.-H. Lee, M. Sachdev, W. S. Wong, "Integration of GaN light-emitting diodes with a-Si:H TFTs for flexible displays", Nanotechnology, volume 30, issue 32, page 4003

6. **Q. Li**, C.-H. Lee, M. Asad, W. S. Wong, M. Sachdev, "A 6-TFT charge-transfer self-compensating pixel circuit for flexible displays", IEEE Journal of the Electron Devices Society, volume 7, page 792-800

7. S. Sanjeevi, **Q. Li**, C.-H. Lee, W. S. Wong, M. Sachdev, "Effect of charge-retention of non-volatile memory TFTs under multiple read cycles", IEEE Journal of the Electron Devices Society, volume 5, issue 4, page 266-270

Conference publications (selected)

1. **Q. Li**, C.-H. Lee, W. S. Wong, M. Sachdev, "Realization of an energy-efficient and full-swing decoder with unipolar TFT technology", IEEE Custom Integrated Circuits Conference (CICC 2020), March 2020, Boston, MA, USA (held virtually)

2. **Q. Li**, C.-H. Lee, M. Asad, W. S. Wong, M. Sachdev, "Operation and control of flexible display pixel circuits under mechanical bending", IEEE International

Flexible Electronics Technology Conference (IFECT 2018), Aug 2018, Ottawa, ON, Canada

3. **Q. Li**, M. Asad, C.-H. Lee, W. S. Wong, M. Sachdev, "Flexible inverted InGaN micro-LEDs addressed by a-Si:H TFT pixel circuits", 61st Electronic Materials Conference (EMC 2019), June 2019, Ann Arbor, MI, USA

References

[1] T. R. H. Wheeler and M. G. Clark, *CRT Technology*. Boston, MA: Springer US, 1992, pp. 221–256, doi:10.1007/978-1-4757-9754-1.

[2] Y. Ishii, "The world of liquid-crystal display TVs—past, present, and future," *Journal of Display Technology*, vol. 3, no. 4, pp. 351–360, Dec 2007, doi:10.1109/JDT.2007.909381.

[3] J. N. Bardsley, "International OLED technology roadmap," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 10, no. 1, pp. 3–9, Jan 2004, doi:10.1109/JSTQE.2004.824077.

[4] M. Koden, *History of OLEDs*. IEEE, 2017, pp. 1–11, doi:10.1002/9781119040477.

[5] L. Hung and C. Chen, "Recent progress of molecular organic electroluminescent materials and devices," *Materials Science and Engineering: R: Reports*, vol. 39, no. 5, pp. 143 – 222, 2002, doi:10.1016/S0927-796X(02)00093-1.

[6] D. Barnes, "5.1: Invited Paper: LCD or OLED: Who Wins?" *SID Symposium Digest of Technical Papers*, vol. 44, no. 1, pp. 26–27, 2013. doi: 10.1002/j.2168-0159.2013.tb06130.x

[7] Z. R. Li, *Transparent Electrode for OLEDs*. CRC Press, 2017.

[8] "Liquid crystal display and organic light-emitting diode display: present status and future perspectives," *Light Science and Applications*, vol. 7, p. 17168, 2018.

[9] S. Park, K. Chung, and S. Jayaraman, "Chapter 1.1 - wearables: Fundamentals, advancements, and a roadmap for the future," in *Wearable Sensors*, E. Sazonov and M. R. Neuman, Eds. Oxford: Academic Press, 2014, pp. 1 – 23. ISBN 978-0-12-418662-0

[10] R. Mitsui, J. Sato, S. Takahashi, and S.-i. Nakajima, "Electrical reliability of a film-type connection during bending," *Electronics*, vol. 4, no. 4, pp. 827–846, 2015.

[11] T. Wu, C.-W. Sher, Y. Lin, C.-F. Lee, S. Liang, Y. Lu, S.-W. Huang Chen, W. Guo, H.-C. Kuo, and Z. Chen, "Mini-led and micro-led: Promising candidates for the next generation display technology," *Applied Sciences*, vol. 8, no. 9, 2018.

[12] C. e. a. Tian, "Effects of unit size on current density and illuminance of micro-led-array," *Optoelectronics Letters*, vol. 13, pp. 84–89, April 2017.

[13] J.-J. Lih, C.-F. Sung, C.-H. Li, T.-H. Hsiao, and H.-H. Lee, "Comparison of a-si and poly-si for amoled displays," *Journal of the Society for Information Display*, vol. 12, no. 4, pp. 367–371, 2004. doi: 10.1889/1.1847734

[14] J. F. Wager, "Flat-panel-display backplanes: Ltps or igzo for amlcds or amoled displays?" *Information Display*, vol. 30, no. 2, pp. 26–29, 2014. doi: 10.1002/j.2637-496X.2014.tb00698.x

[15] A. Teramoto, T. Hamada, M. Yamamoto, P. Gaubert, H. Akahori, K. Nii, M. Hirayama, K. Arima, K. Endo, S. Sugawa, and T. Ohmi, "Very high carrier mobility for high-performance cmos on a si(110) surface," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1438–1445, June 2007. doi: 10.1109/TED.2007.896372

[16] G. B. Levy, W. Evans, J. Ebner, P. Farrell, M. Hufford, B. H. Allison, D. Wheeler, Haiqing Lin, O. Prache, and E. Naviasky, "An 852/spl times/600 pixel oled-on-silicon color microdisplay using cmos subthreshold-voltage-scaling current drivers," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1879–1889, Dec 2002. doi: 10.1109/JSSC.2002.804344

[17] J. N. Burghartz, G. Alavi, B. Albrecht, T. Deuble, M. Elsobky, S. Ferwana, C. Harendt, Y. Mahsereci, H. Richter, and Z. Yu, "Hybrid systems-in-foil—combining the merits of thin chips and of large-area electronics," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 776–783, 2019. doi: 10.1109/JEDS.2019.2896188

[18] K. Yoneda, R. Yokoyama, and T. Yamada, "Development trends of ltps tft lcds for mobile applications," in *2001 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No.01CH37185)*, June 2001. doi: 10.1109/VLSIC.2001.934204. ISSN null pp. 85–90.

[19] C. Lin, P. Chen, M. Cheng, Y. Liu, and F. Chen, "A three-transistor pixel circuit to compensate for threshold voltage variations of ltps tfts for amoled displays," *Journal of Display Technology*, vol. 11, no. 2, pp. 146–148, Feb 2015. doi: 10.1109/JDT.2014.2383434

[20] C. Lin, P. Chen, M. Deng, C. Wu, W. Chiu, and Y. Lin, "Uhd amoled driving scheme of compensation pixel and gate driver circuits achieving high-speed operation," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 26–33, 2018. doi: 10.1109/JEDS.2017.2763601

[21] C. Liao, C. He, T. Chen, D. Dai, S. Chung, T. Jen, and S. Zhang, "Design of integrated amorphous-silicon thin-film transistor gate driver," *J. Display Technol.*, vol. 9, no. 1, pp. 7–16, Jan 2013.

[22] G.-T. Zheng, P.-T. Liu, M.-C. Wu, L.-W. Chu, and M.-C. Yang, "Design of bidirectional and low power consumption gate driver in amorphous silicon technology for tft-lcd application," *J. Display Technol.*, vol. 9, no. 2, pp. 91–99, Feb 2013.

[23] J. K. Um, S. Lee, S. Jin, M. Mativenga, S. Yun Oh, C. H. Lee, and J. Jang, "High-performance homojunction a-igzo tfts with selectively defined low-resistive a-igzo source/drain electrodes," *IEEE Transactions on Electron Devices*, vol. 62, no. 7, pp. 2212–2218, July 2015. doi: 10.1109/TED.2015.2431073

[24] H. Wu and C. Chien, "Highly transparent, high-performance igzo-tfts using the selective formation of igzo source and drain electrodes," *IEEE Electron Device Letters*, vol. 35, no. 6, pp. 645–647, June 2014. doi: 10.1109/LED.2014.2317943

[25] J. Hughes, R. Bannister, A. Graham, D. McDonnell, H. Pedlingham, D. Scattergood, and C. Smith, "A high-resolution ferroelectric liquid crystal display," *Displays*, vol. 15, no. 2, pp. 117 – 123, 1994. doi: https://doi.org/10.1016/0141-9382(94)90066-3

[26] D. J. Cristaldi, S. Pennisi, and F. Pulvirenti, *Passive LCDs and Their Addressing Techniques*. Dordrecht: Springer Netherlands, 2009, pp. 75–108. ISBN 978-90-481-2255-4

[27] M. Yang, Ph.D. dissertation, 2014.

[28] Si Yujuan, Zhao Yi, Chen Xinfa, and Liu Shiyong, "A simple and effective ac pixel driving circuit for active matrix oled," *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 1137–1141, April 2003. doi: 10.1109/TED.2003.812100

[29] T. P. Brody, "The thin film transistor—a late flowering bloom," *IEEE Transactions on Electron Devices*, vol. 31, no. 11, pp. 1614–1628, Nov 1984. doi: 10.1109/T-ED.1984.21762

[30] Wen-Jian Lin and Hsiung-Kuang Tsai, "A new process of fabricating inverted-staggered tri-layer thin-film transistors," *IEEE Electron Device Letters*, vol. 16, no. 4, pp. 133–135, April 1995. doi: 10.1109/55.372492

[31] S. Oda, N. Adachi, S. Katoh, and M. Matsumura, "p-channel amorphous silicon tfts with high hole mobility," *IEEE Transactions on Electron Devices*, vol. 35, no. 12, pp. 2448–, Dec 1988. doi: 10.1109/16.8877

[32] N. Ibaraki, K. Fukuda, and H. Takata, "The effect of interface states on amorphous-silicon transistors," *IEEE Transactions on Electron Devices*, vol. 36, no. 12, pp. 2971–2972, Dec 1989. doi: 10.1109/16.40965

[33] M. J. Powell and D. H. Nicholls, "Stability of amorphous-silicon thin-film transistors," *IEE Proceedings I - Solid-State and Electron Devices*, vol. 130, no. 1, pp. 2–4, February 1983.

[34] K. Long, A. Z. Kattamis, I. . Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, "Stability of amorphous-silicon tfts deposited on clear plastic substrates at 250°c to 280°c," *IEEE Electron Device Letters*, vol. 27, no. 2, pp. 111–113, Feb 2006. doi: 10.1109/LED.2005.863147

[35] M. J. Powell and D. H. Nicholls, "Stability of amorphous-silicon thin-film transistors," *IEE Proceedings I - Solid-State and Electron Devices*, vol. 130, no. 1, pp. 2–4, February 1983. doi: 10.1049/ip-i-1.1983.0002

[36] J. W. Choi, J. I. Kim, S. H. Kim, and J. Jang, "Highly reliable amorphous silicon gate driver using stable center-offset thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 57, no. 9, pp. 2330–2334, Sep. 2010. doi: 10.1109/TED.2010.2054453

[37] J. Yoo, S. Jung, Y. Kim, S. Byun, J. Kim, N. Choi, S. Yoon, C. Kim, Y. Hwang, and I. Chung, "Highly flexible am-oled display with integrated gate driver using

amorphous silicon tft on ultrathin metal foil," *Journal of Display Technology*, vol. 6, no. 11, pp. 565–570, Nov 2010. doi: 10.1109/JDT.2010.2048998

[38] C. Lin, F. Chen, M. Wang, P. Lai, and C. Tseng, "Gate driver based on a-si:h thin-film transistors with two-step-bootstrapping structure for high-resolution and high-frame-rate displays," *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3494–3497, Aug 2017. doi: 10.1109/TED.2017.2710180

[39] A. Paranjpe, J. Montgomery, S. M. Lee, and C. Morath, "45-2: Invited paper: Micro-led displays: Key manufacturing challenges and solutions," *SID Symposium Digest of Technical Papers*, vol. 49, no. 1, pp. 597–600, 2018. doi: 10.1002/sdtp.12414

[40] H. W. Choi, C. W. Jeon, M. D. Dawson, P. R. Edwards, and R. W. Martin, "Fabrication and performance of parallel-addressed ingan micro-led arrays," *IEEE Photonics Technology Letters*, vol. 15, no. 4, pp. 510–512, April 2003. doi: 10.1109/LPT.2003.809257

[41] C.-M. Kang, D.-J. Kong, J.-P. Shim, S. Kim, S.-B. Choi, J.-Y. Lee, J.-H. Min, D.-J. Seo, S.-Y. Choi, and D.-S. Lee, "Fabrication of a vertically-stacked passive-matrix micro-led array structure for a dual color display," *Optics Express*, vol. 25, no. 3, pp. 2489–2495, Feb 2017. doi: 10.1364/OE.25.002489

[42] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, "Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1477–1486, Sept 2004, doi:10.1109/JSSC.2004.829373.

[43] M. Asad, Q. Li, C.-H. Lee, M. Sachdev, and W. S. Wong, "Integration of GaN light-emitting diodes with a-si:h thin-film transistors for flexible displays," *Nanotechnology*, vol. 30, no. 32, p. 324003, may 2019. doi: 10.1088/1361-6528/ab1a5e

[44] H. Hosono, J. Kim, Y. Toda, T. Kamiya, and S. Watanabe, "Transparent amorphous oxide semiconductors for organic electronics: Application to inverted oleds," *Proceedings of the National Academy of Sciences*, vol. 114, no. 2, pp. 233–238, 2017. doi: 10.1073/PNAS.1617186114

[45] J.-H. Lee, B.-H. You, C.-W. Han, K.-S. Shin, and M.-K. Han, "A new a-Si:H TFT pixel circuit suppressing OLED current error caused by the hysteresis and threshold voltage shift for active matrix organic light emitting diode," *SID Int. Symp. Dig. Tech.*, vol. 36, no. 1, pp. 228–231, 2005, doi:10.1889/1.2036410.

[46] M. Yang, N. P. Papadopoulos, W. S. Wong, and M. Sachdev, "A novel voltage-programmed pixel circuit utilizing V_T-dependent charge-transfer to improve stability of AMOLED display," *J. Display Technol.*, vol. 9, no. 12, pp. 957–964, Dec 2013, doi:10.1109/JDT.2013.2275172.

[47] Y. Kuo, "Thin film transistor technology - past, present and future," *Electrochem. Soc. Interface*, vol. 22, no. 1, pp. 55–64, 2013.

[48] C. An, M. Wu, Y. Huang, T. Chen, C. Chao, and W. Yeh, "Study on flip chip assembly of high density micro-LED array," in *2011 6th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, Oct 2011, pp. 336–338, doi:10.1109/IMPACT.2011.6117235.

[49] M. Asad, R. Wang, Y.-H. Ra, W. S. Wong, and Z. Mi, "Electrical and optical properties of flexible nanowire blue light-emitting diodes under mechanical bending," in *Proc. SPIE*, 2017, p. 10104, doi:10.1117/12.2254543.

[50] C. W. Jeon, H. W. Choi, and M. D. Dawson, "Fabrication of matrix-addressable InGaN-based microdisplays of high array density," *IEEE Photonics Technology Letters*, vol. 15, no. 11, pp. 1516–1518, Nov 2003, doi:10.1109/LPT.2003.818643.

[51] R. Shringarpure, S. Venugopal, L. T. Clark, D. R. Allee, and E. Bawolek, "Localization of gate bias induced threshold voltage degradation in a-Si:H TFTs," *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 93–95, Jan 2008, doi:10.1109/LED.2007.911609.

[52] C.-S. Yang, L. L. Smith, C. B. Arthur, and G. N. Parsons, "Stability of low-temperature amorphous silicon thin film transistors formed on glass and transparent plastic substrates," *J. Vac. Sci. Technol. B*, vol. 18, no. 2, pp. 683–689, April 2000, doi:10.1116/1.591259.

[53] D. R. Allee, L. T. Clark, B. D. Vogt, R. Shringarpure, S. M. Venugopal, S. G. Uppili, K. Kaftanoglu, H. Shivalingaiah, Z. P. Li, J. J. R. Fernando, E. J. Bawolek, and S. M. O'Rourke, "Circuit-level impact of a-Si:H thin-film-transistor degradation effects," *IEEE Transactions on Electron Devices*, vol. 56, no. 6, pp. 1166–1176, June 2009, doi:10.1109/TED.2009.2019387.

[54] K. Oh and O.-K. Kwon, "Threshold-voltage-shift compensation and suppression method using hydrogenated amorphous silicon thin-film transistors for large active matrix organic light-emitting diode displays," *Jpn. J. Appl. Phys.*, vol. 51, no. 3S, pp. 03CD01–04, 2012, doi:10.1143/JJAP.51.03CD01.

[55] S. J. Ashtiani, G. R. Chaji, and A. Nathan, "AMOLED pixel circuit with electronic compensation of luminance degradation," *J. Display Technol.*, vol. 3, no. 1, pp. 36–39, March 2007, doi:10.1109/JDT.2006.890711.

[56] M. J. Chow, A. A. Fomani, M. Moradi, G. Chaji, R. A. Lujan, and W. S. Wong, "Effects of mechanical strain on amorphous silicon thin-film transistor electrical stability," *Applied Physics Letters*, vol. 102, no. 23, p. 233509, 2013, doi:10.1063/1.4811271.

[57] C.-H. Lee, N. P. Papadopoulos, M. Sachdev, and W. S. Wong, "Effect of mechanical strain on hydrogenated amorphous silicon thin-film transistors and compensation circuits on flexible substrates," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2016–2021, May 2017, doi:10.1109/TED.2017.2682881.

[58] P. Servati and A. Nathan, "Functional pixel circuits for elastic AMOLED displays," *Proceedings of the IEEE*, vol. 93, no. 7, pp. 1257–1264, July 2005, doi:10.1109/JPROC.2005.851534.

[59] J. B. Choi, D. C. Yun, Y. I. Park, and J. H. Kim, "Properties of hydrogenated amorphous silicon thin film transistors fabricated at 150°C," *Journal of Non-Crystalline Solids*, vol. 266-269, pp. 1315 – 1319, 2000, doi:10.1016/S0022-3093(99)00943-6.

[60] M. Amiri, A. R. Zamir, S. Shahin, and S. J. Ashtiani, "A novel 3-tft amoled pixel driver for threshold voltage shift compensation," in *2012 IEEE International Conference on Electronics Design, Systems and Applications (ICEDSA)*, Nov 2012. doi: 10.1109/ICEDSA.2012.6507779. ISSN 2159-2047 pp. 121–124.

[61] Jae-Hoon Lee, Ji-Hoon Kim, and Min-Koo Han, "A new a-si:h tft pixel circuit compensating the threshold voltage shift of a-si:h tft and oled for active matrix oled," *IEEE Electron Device Letters*, vol. 26, no. 12, pp. 897–899, Dec 2005. doi: 10.1109/LED.2005.859674

[62] K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 188–190, April 2004, doi:10.1109/LED.2004.825154.

[63] W. M. H. bin Wan Zaidi, J. Costa, A. Pouryazdan, W. F. H. Abdullah, and N. Münzenrieder, "Flexible IGZO TFT SPICE model and design of active strain-

compensation circuits for bendable active matrix arrays," *IEEE Electron Device Letters*, vol. 39, no. 9, pp. 1314–1317, Sept 2018, doi:10.1109/LED.2018.2854541.

[64] P. Servati and A. Nathan, "Orientation-dependent strain tolerance of amorphous silicon transistors and pixel circuits for elastic organic light-emitting diode displays," *Applied Physics Letters*, vol. 86, no. 3, p. 033504, 2005, doi:10.1063/1.1852729.

[65] M. Bagheri, S. J. Ashtiani, and A. N. Nathan, "Fast voltage-programmed pixel architecture for AMOLED displays," *Journal of Display Technology*, vol. 6, no. 5, pp. 191–195, May 2010, doi:10.1109/JDT.2010.2044015.

[66] Z. Hu, L. L. Wang, C. Liao, L. Zeng, C. Lee, A. Lien, and S. Zhang, "Threshold voltage shift effect of a-si:h tfts under bipolar pulse bias," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4037–4043, 2015.

[67] Z. Hu, C. Liao, W. Li, L. Zeng, C. Lee, and S. Zhang, "Integrated a-si:h gate driver with low-level holding tfts biased under bipolar pulses," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4044–4050, 2015.

[68] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous in–ga–zn–o thin-film transistors," *Science and Technology of Advanced Materials*, vol. 11, no. 4, p. 044305, 2010, doi = 10.1088/1468-6996/11/4/044305.

[69] K. Myny, "The development of flexible integrated circuits based on thin-film transistors," *Nature Electronics*, vol. 1, no. 1, p. 30, Jan 2018, doi:10.1038/s41928-017-0008-6.

[70] S. Y. Yoon, Y. H. Jang, B. Kim, M. D. Chun, H. N. Cho, N. W. Cho, C. Y. Sohn, S. H. Jo, C.-D. Kim, and I.-J. Chung, "Highly stable integrated gate driver circuit using a-Si TFT with dual pull-down structure," *SID Int. Symp. Dig. Tec.*, vol. 36, no. 1, pp. 348–351, July 2012, doi:10.1889/1.2036443.

[71] X. Li, D. Geng, M. Mativenga, Y. Chen, and J. Jang, "Effect of bulk-accumulation on switching speed of dual-gate a-IGZO TFT-based circuits," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1242–1244, Dec 2014, doi:10.1109/LED.2014.2362992.

[72] S. H. Nam, P. J. Jeon, Y. T. Lee, S. R. A. Raza, and S. Im, "NOT and NOR logic circuits using passivation dielectric involved dual gate in a-InGaZnO TFTs," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1527–1529, Dec 2013, doi:10.1109/LED.2013.2285185.

[73] Q. Zhao, W. Sun, J. Zhao, L. Feng, X. Xu, W. Liu, X. Guo, Y. Liu, and H. Yang, "Noise margin, delay, and power model for pseudo-CMOS TFT logic circuits," *IEEE Trans. Electron Devices*, vol. 64, no. 6, pp. 2635–2642, June 2017, doi:10.1109/TED.2017.2695527.

[74] B. Tiwari, P. G. Bahubalindruni, A. Santa, J. Martins, P. Mittal, J. Goes, R. Martins, E. Fortunato, and P. Barquinha, "Oxide TFT rectifiers on flexible substrates operating at NFC frequency range," vol. 7, pp. 329–334, Feb 2019, doi:10.1109/JEDS.2019.2897642.

[75] T.-H. Hwang, I.-S. Yang, O.-K. Kwon, M.-K. Ryu, C.-W. Byun, C.-S. Hwang, and S.-H. K. Park, "Inverters using only N-type indium gallium zinc oxide thin film transistors for flat panel display applications," *Jpn. J. Appl. Phys.*, vol. 50, no. 3, p. 03CB06, Mar 2011, doi:10.1143/jjap.50.03cb06.

[76] N. P. Papadopoulos, C.-H. Lee, A. Tari, W. S. Wong, and M. Sachdev, "Low-power bootstrapped rail-to-rail logic gates for thin-film applications," *IEEE/OSA J. Display Technol.*, vol. 12, no. 12, pp. 1539–1546, Dec 2016, doi:10.1109/JDT.2016.2561841.

[77] Q. Li, C. Lee, M. Asad, W. S. Wong, and M. Sachdev, "CMOS-like logic circuits with unipolar thin-film transistors on flexible substrate," *IEEE Transactions on Electron Devices*, vol. 67, no. 2, pp. 512–517, Feb 2020. doi: 10.1109/TED.2019.2956890

[78] Q. Li, C.-H. Lee, M. Asad, W. S. Wong, and M. Sachdev, "A 6-TFT charge-transfer self-compensating pixel circuit for flexible displays," vol. 7, pp. 1–9, Mar 2019, doi:10.1109/JEDS.2019.2903541.

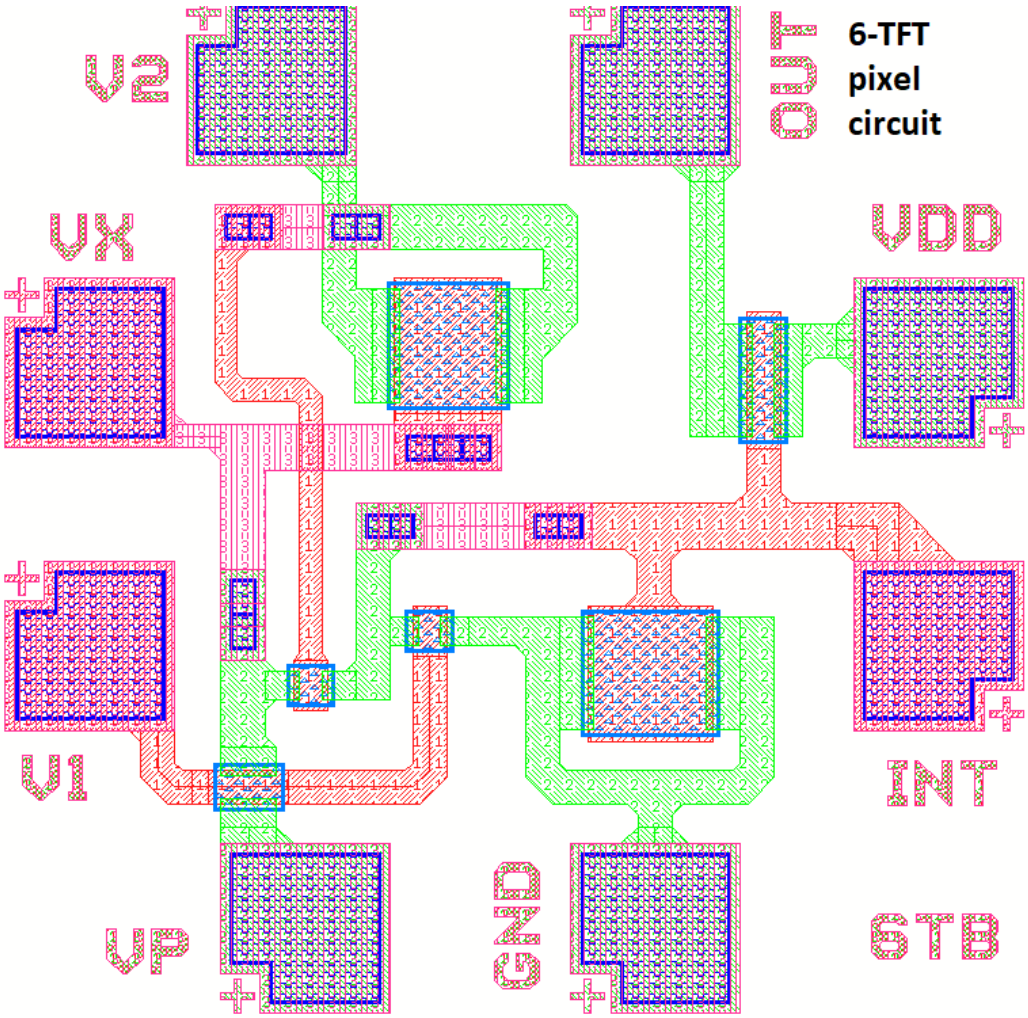
[79] Q. Li, C.-H. Lee, M. Asad, M. Sachdev, and W. S. Wong, "Operation and control of flexible display pixel circuits under mechanical bending," in *2018 Int. Flex. Elec. Tec. Conf. (IFETC)*, Aug 2018, pp. 1–4, doi:10.1109/IFETC.2018.8583886.

[80] J. Genoe, K. Obata, M. Ameys, K. Myny, T. H. Ke, M. Nag, S. Steudel, S. Schols, J. Maas, A. Tripathi, J. P. J. van der Steen, T. Ellis, G. H. Gelinck, and P. Heremans, "Integrated line driver for digital pulse-width modulation driven AMOLED displays on flex," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 282–290, Jan 2015, doi:10.1109/JSSC.2014.2364268.

[81] Q. Li, C.-H. Lee, W. S. Wong, and M. Sachdev, "Realization of an energy-efficient, full-swing decoder with unipolar TFT technology," in *2020 Custom Integrated Circuits Conference (CICC 2020)*, March 2020, accepted.

APPENDICES

A - The layout of the 6-TFT pixel circuit



B - The layout of the 5-TFT inverter