Design of SRAM Based Dosimetry Used for Neutron and Proton Detection

by

Kai Jiang

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Radiation causes soft errors in memory devices, and a variety of research has been focused on techniques to reduce these soft errors. In this thesis, instead of mitigating soft errors, we present an SRAM based dosimeter which uses the soft error susceptible nature of SRAMs as a means of measuring radiation fluence. This cost effective, real-time dosimeter can be used to calibrate and characterize neutron and proton beams with wide-range spectra.

The design of the SRAM dosimeter includes both hardware and software. An array of thirty 16-Mbit off-the-shelf 65 nm SRAMs are used as sensors directly exposed to radiation. An FPGA is used as a processor to analyze the sensor data and communicate with a PC. Finally, a graphical user interface is provided for interacting with the dosimeter.

The dosimeter device has been validated at the TRIUMF proton and neutron irradiation facility, and has been used by the facility to carry out various calibration and measurement activities such as proton and neutron beam characterization, beam profile measurements, collimator design and shielding effects measurements.

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Abbreviations

CMOS Complementary Metal Oxide Semiconductor 8

ECC Error Correction Code 7, 21

FIT Failure in Time 20, 43

FPGA Field Programmable Gate Array 19

FTDI Future Technology Devices International 19, 25

GUI Graphical User Interface 3, 24, 25, 27

IC Integrated Circuit 1, 3

JEDEC Joint Electron Device Engineering Council 35

MBU Multi Bit Upset 7, 21

MOSFET Metal Oxide Semiconductor Field Effect Transistor 2

NIF Neutron Irradiation Facilities x, 30–32, 35

NMOS *N-type* Metal Oxide Semiconductor 13

PCB Printed Circuit Board 19

PIF Proton Irradiation Facilities x, 30–32, 35

PMOS *P-type* Metal Oxide Semiconductor 15

PMT Photo Multiplier Tubes 6

SBU Single Bit Upset 7

SEB Single Event Burnout 8, 21

SEE Single Event Effects 7

SEGR Single Event Gate Rupture 8, 21

SEL Single Event Latch-up 7, 21

SER Soft Error Rate 1, 16

SEU Single Event Upsets 1–3, 7, 19–21

SRAM Static Random Access Memory 1, 2

TID Total Ionizing Dose 7

TLD Thermo Luminescent Dosimeter 2

TMR Triple Modular Redundancy 7

TRIUMF Tri-University Meson Facility 30, 41, 45

UART Universal Asynchronous Receiver-Transmitter 20, 25

Chapter 1

Introduction

Year over year, integrated circuits continue to increase in complexity and decrease in feature size. Contemporary applications, such as machine learning, graph acceleration and search engine optimization, require compute-intensive systems that not only include traditional CPUs but also consist of various high-speed interfaces, I/O links, gigabytes of on-chip memories and complex arithmetic accelerators. For such hybrid and dense systems, exposure to surrounding radiation can significantly alter the performance and even damage the systems.

Ionizing radiation poses a direct threat to microelectronics because it can change the stored values in memory elements, an action known as Single Event Upsets (SEU). SEUs are usually non-destructive but can be a dominant factor affecting the reliability of Integrated Circuit (IC)s [4]. Flow of neutrons are the primary causes of SEUs in the terrestrial environment. Although neutrons are not directly ionizing, if their energy is high enough they can cause nuclear interactions in the silicon, resulting in ion recoils, which produce electron-hole pairs in semiconductors. The charges induced by the electron-hole pairs could change the stored values, i.e., SEUs occur, if the voltage variation is large enough. The Soft Error Rate (SER)s within a system exposed to ionizing radiation are proportional to the radiation fluence. A Static Random Access Memory (SRAM) storage cell is an example of a radiation-susceptible circuit. An SRAM will remain operational after SEUs, however its data could become corrupted.

Extensive research has studied the effects of SEUs on circuits [11, 12] and suggested that as transistor sizing continues to decrease, the number of neutron-induced upsets have increased dramatically. Thus, it is crucial to develop radiation-hardened designs, which requires methods of measuring the radiation exposure of electronics.

Dosimeters are the devices that are used to measure the dose uptake of external ionizing radiation. These devices are useful to detect excessive radiation that can have detrimental effects on the circuit. Over the past several decades, different kinds of dosimeters have been developed to measure neutron beam fluence, such as ionization chamber dosimeter, Thermo Luminescent Dosimeter (TLD), and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) dosimeter [13, 14]. All these types of dosimeters use different types of material or methods to measure radiation. For example, ionization chamber dosimeter uses a gas-filled chamber to measure the charge produced by radiation. TLD uses phosphur crystals which absorb the radiation energy to detect its intensity. MOSFET based dosimeters monitor the shift in the threshold voltage due to radiation exposure. More details on these dosimeters are provided in the background section.

1.1 Research Objective

The research objective of this thesis is to develop a new type of dosimeter used to characterize broadband neutron and proton beams. We postulate that the rate of SRAM SEUs may be used as a measure of neutron/proton fluence. SRAM SEUs have been characterized in radiation environments, mostly by microelectronics companies seeking to improve the robustness of their next-generation electronics products. However, using SRAMs as radiation fluence measurement devices for radiation testing facilities has not gathered much attention, with exceptions in [15, 16]. Our goal is to design an advanced, fast and sensitive dosimeter using an array of SRAMs. Our dosimeter makes use of the correlation between SEU rate and the radiation fluence. There are six relevant performance criteria for the dosimeter:

1. **Real-time monitor -** Real-time SRAM sensor information should be available to the user through read-out circuitry. Read-out data should contain SEU rate

and accumulative SEUs, which can be used to further calculate SEU cross sections, radiation fluence and to measure beam profile.

2. **Sensitivity -** The SRAM sensor should be sensitive to different radiation energies, especially those within the range of typical broad-spectrum neutron beams.

3. **Reusable -** The dosimeter should be reusable for multiple measurements. The SEU cross section of the sensor needs to be reasonably constant.

4. **Portable -** The device should be portable. The dimension of the device should be small to accommodate for different beam spot sizes.

5. **Easy to operate -** The system should be easy to setup and use. A Graphical User Interface (GUI) should be implemented for users to access data from the dosimeter system and control the system.

6. **Cost efficient -** The system should be inexpensive to produce, use and maintain as compared to the existing solutions.

1.2 Thesis Organization

The outline of this thesis is as follows:

- In Chapter 2, existing radiation measurement methods are reviewed.
- In Chapter 3, the background of radiation effects on semiconductor devices is presented. A breakdown of the most commonly known radiation sources for soft errors is discussed, followed by the respective failure mechanisms for ICs, specifically SRAMs and DRAMs. We conclude the chapter with a discussion about the increasing importance of radiation testing as technology scales.
- In Chapter 4, the design methodology of the SRAM based dosimeter is presented. The chapter explains, in details, the implementation considerations for each subsystem of the device.

- In Chapter 5, measurement results and comparisons are discussed.
- Finally, Chapter 6 presents the conclusion and outlines future work directions.

Chapter 2

Background

2.1 Current Dosimetry Methods

We review three types of widely used and studied dosimeters. Each uses different material and detection methods to measure radiation.

2.1.1 Gaseous Ionization Detectors

Gaseous ionization detectors use ionising effects of gas sensors to detect radiation. There are three types of detectors: ionization chambers, proportional counters, and Geiger-Muller counters.

The ionization chamber is a type of gas-filled chamber that measures the direct ionization charges generated when radiation strikes the gas. The current generated in the chamber is directly proportional to the absorbed radiation, and the absorption is determined by the type of gas fill and the pressure. The ionization process can only occur when the energy transferred by the particle is equal to the ionization energy of the gas molecule, which is between 10 and 25 eV for most gases used for the detector.

Ionization chambers offer immediate readout and can be used for beam calibrations. However, the drawbacks are 1) they are large and thus less portable; 2) they need high

supply voltage.

2.1.2 Thermoluminescent Dosimeter

TLDs use phosphor as a radiation detector. When a TLD is exposed to neutron radiation, its phosphor crystals absorb the energy, causing their electrons to leave the ground state. The electrons remain trapped until heat is applied, which releases the stored energy as photons. The intensity of the light released is determined by Photo Multiplier Tubes (PMT) and is directly related to the amount of ionizing radiation to which the system is exposed. Compared to ionization chambers, TLDs are much smaller in size, typically worn as badges [17]. However, they are passive devices which provide results only after each exposure. The readout procedure is tedious and does not reflect real-time dose change.

2.1.3 MOSFET Dosimeter

MOSFET-based dosimeters work by measuring and correlating the shift of the threshold voltage as a function of the absorbed dose. The gate oxide traps the charge from electron-hole pairs generated by ionizing radiation, creating a shift in the threshold voltage [18]. MOSFET dosimeters have the capability of real-time readout and are much smaller than both ionization chambers and TLDs, can be in micro-meter scale as shown in [19]. However, the main drawback of MOSFET dosimeters is their limited irradiation life span due to the decrease in radiation sensitivity as the cumulative dose increases [18]. The dosimeter needs to be annealed to release the trapped charges to restore the threshold voltage. Another drawback is that the sensitivity of threshold voltage is subject to temperature variation [20].

2.2 Radiation Effects on Semiconductor Devices

In this chapter, we discuss the radiation sources and effects on various semiconductor devices.

2.2.1 Radiation Faults

Radiation-induced faults can be classified into two categories: cumulative dose damages, and single event effects. Both can cause either permanent or temporary faults on semiconductor devices.

The long term cumulative damage is called Total Ionizing Dose (TID) effect. TID damage happens when the device has a continuous exposure to the radiation source, causing lattice displacement damage. As a device is exposed to the radiation source, trapped charges start to build-up in the insulating layer, Si/SiO_2 interface, and the bulk of the device. The built-up charges would increase the threshold voltage, alter the amount of *on* current and leakage current, and also affect the transconductance of the device. The cumulative irradiation on the semiconductor may permanently alter the intrinsic properties of the semiconductor device, depending on the total dosage.

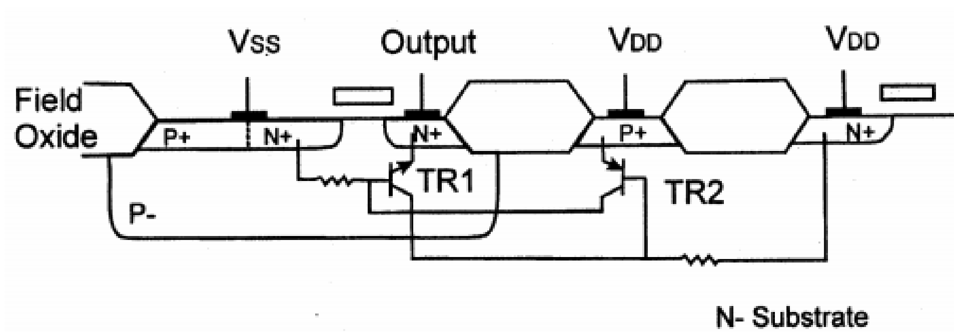
Other than cumulative effects, short-time pulses of radiation can also induce destructive or non-destructive events on a semiconductor device. This phenomenon is known as Single Event Effects (SEE) [21]. Some of the main events are listed below.

- A non-destructive event is commonly referred to as an SEU, where a radiation event would strike a memory cell, flipping the content stored within, causing the data to be corrupted. SEUs do not cause permanent failures to the cell, i.e., when the device is reset or the new content is written to the cell, the fault would disappear. SEUs are usually Single Bit Upset (SBU)s. However, if the radiation energy is strong enough, failures can also be Multi Bit Upset (MBU)s. To mitigate the effects of SEUs, most memory devices nowadays use Error Correction Code (ECC) to detect and/or correct upset events. To further enhance the device, hardened hardware decision logic such as Triple Modular Redundancy (TMR) [22] is used.
- Single Event Latch-up (SEL) refers to an event where a low resistance path forms from the power line to the ground on a device. It is usually caused by heavy ions or protons from cosmic rays or solar flares passing the sensitive region of the device. When a device is latched up, it will remain in this high current state until a new

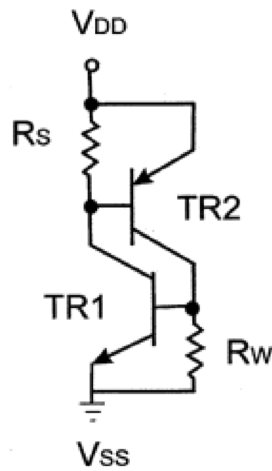
power cycle, or the device becoming permanently damaged. Figure 2.1a shows a bulk Complementary Metal Oxide Semiconductor (CMOS) structure that is latch-up susceptible. A parasitic *p-n-p-n* device acts as a *PNP* and an *NPN* transistor stacked next to each other. In Figure 2.1a the four-layer *p-n-p-n* device is formed by the *p*+ diffusions, the *n*- substrate, the *p*-well regions, and the *n*+ diffusions respectively. An equivalent circuit representation is shown in Figure 2.1b. When either one of the bipolar transistors becomes forward biased, the conducting transistor will feed the current to the base of the other transistor causing it to conduct, hence driving the first transistor harder. Although the initiation is caused by a transient event, this positive loop would continue to latch the device until the device burns out or the power is removed. Multiple methods have been proposed to decrease the device latch-up rate [23]. Some popular techniques include reducing the substrate resistance to improve *p*-well trapping, and adding deep *n*-well on *p*-substrate to form a triple well.

- Single Event Burnout (SEB) is initiated when heavy ions strike a device at *off* state. The induced current creates a forward biased condition for the parasitic bipolar transistor, which makes it conductive. If the device drain-source is holding a high voltage, this sudden turn-on will result in a massive current flow, immediately causing permanent damage to the device. SEB typically occurs in power MOSFET for space systems [24].

- Single Event Gate Rupture (SEGR) is initiated when particles strike a device, resulting in a dielectric breakdown, forming a conducting path in the gate oxide. This event will also result in a destructive burnout for the device.



(a) Cross section view of bulk CMOS technology



(b) Equivalent circuit representation

Figure 2.1: Latch-up structure [3]

2.2.2 Soft Error Radiation Sources

Soft errors in semiconductor are mainly induced by three types of radiation: alpha particles, high energy cosmic neutrons and neutron induced boron fission [4].

2.2.2.1 Alpha Particles

Alpha particles mostly come from the wafer, the packaging material, and the solder bumps used for semiconductor devices. An alpha particle is a double ionized helium atom consisting of two neutrons and two protons. Alpha particles from the most common source have energy ranging from 4 to 9 MeV [21]. In a silicon substrate, each creation of electron-hole pair requires 3.6 eV from the particle. This means that each alpha particle can cause a burst of a million electron-hole pairs as it travels in silicon. The higher the energy of an alpha particle, the more distance it can travel in the substrate.

2.2.2.2 High Energy Cosmic Neutron

Cosmic radiation mainly consists of two types of particles, the galactic particles that enter the solar system with energy $\gg$1 GeV, and particles from the solar wind, with energies $<$1 GeV. Those particles include 89% protons, 10% alpha particles, and 1% heavier nuclei [5]. When these primary cosmic particles hit the earth's atmosphere, a shower of secondary particles, called cascade particles, is produced. Since the earth's atmosphere is very thick, many collisions occur as the particles travel through. The actual particles that penetrate to the earth's terrestrial level are the further cascaded particles. The primary particles are fewer than 1%. At sea level, the dominating particles are pions, muons, neutrons, electrons, and photons. Since more than 97% of the particle flux is from neutrons at sea level [25], neutrons are known as the main contributor for devices' soft errors. Figure 2.2 shows the cosmic neutron flux at sea level (New York City). The neutron flux is a function of latitude, longitude, altitude and solar activities. Altitude is the most important factor. For example, at an altitude of 10,000 feet, the flux from cosmic rays is ten times more than that at sea level.

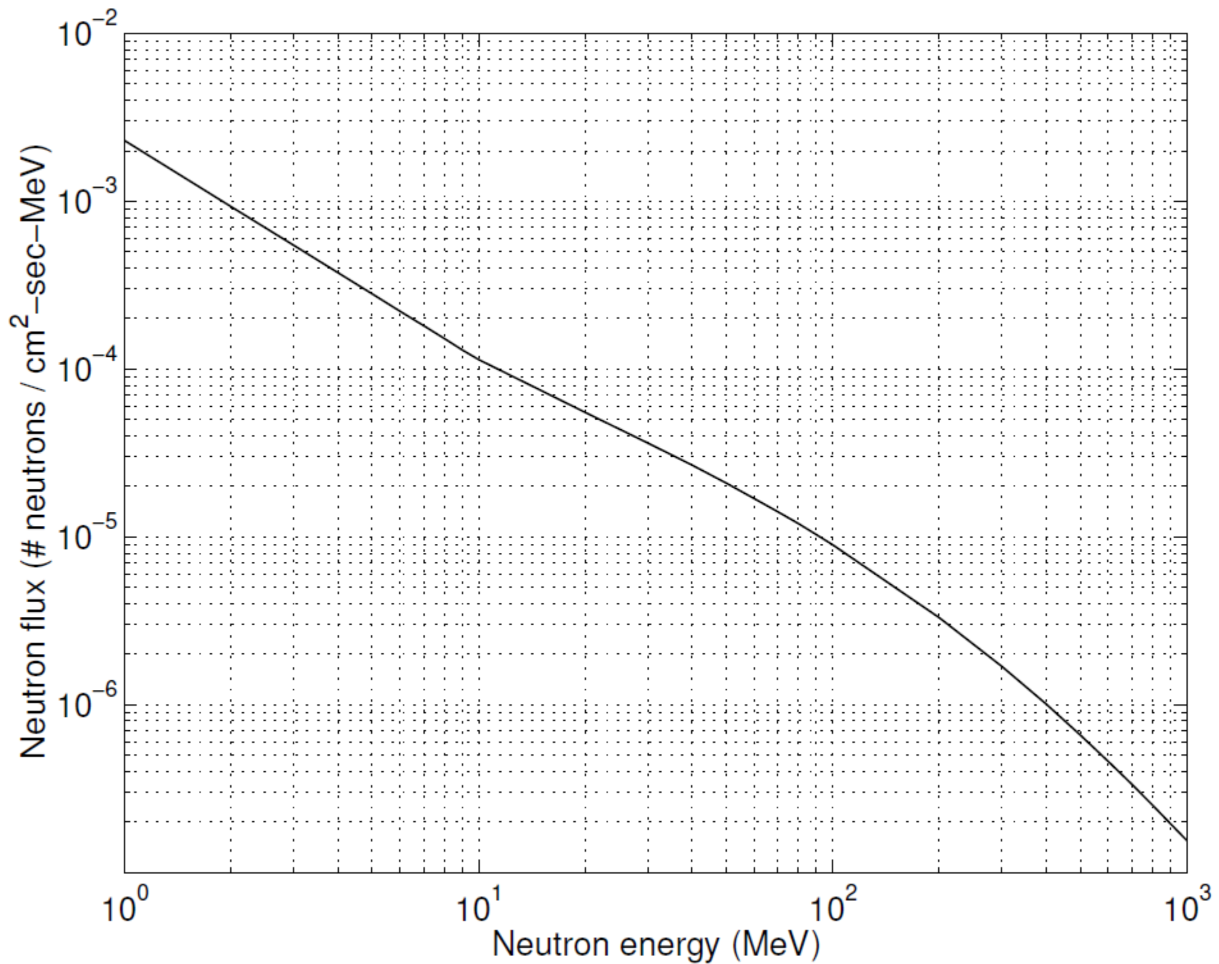


Figure 2.2: Cosmic neutron flux at sea level [4, 5]

Since neutrons are uncharged, they are not directly ionizing. However, if their energy is high enough, they can cause nuclear interactions in the silicon, resulting in ion recoils, which produce electron-hole pairs in semiconductors. Neutrons can also be absorbed by the nucleus to produce secondary particles. Unlike other lightly charged particles, which produce a single ion track in the direction of strike, neutron tracks are formed inside the device and they can start in any direction. This means that the sensitive region can be a lot larger than other ionizing particles. Cosmic neutrons have a high penetration rate for concretes. One foot of concrete reduces neutron radiation only by approximately 30% [26].

Chip-level shielding on consumer electronics can have little to no effect on reducing cosmic neutrons.

2.2.2.3 Low Energy Neutron

Other than the direct impact from cosmic neutrons to the semiconductor, another source of the ionizing particles is the interaction between low energy cosmic neutrons (thermal neutrons) and boron. Boron is used as a p-type dopant in silicon. It has two isotopes, ^{11}B and ^{10}B. The ^{10}B isotope, which is 19.9% in abundance, is highly unstable when exposed to neutrons [21].

Figure 2.3 shows ^{10}B fission: first, it captures a thermal neutron; then, after the neutron is absorbed, ^{10}B fissions and releases a ^{7}Li recoil and an alpha particle in the opposite directions. Both of the alpha particle and the lithium recoil are charged, and they are capable of inducing soft errors on semiconductor devices.

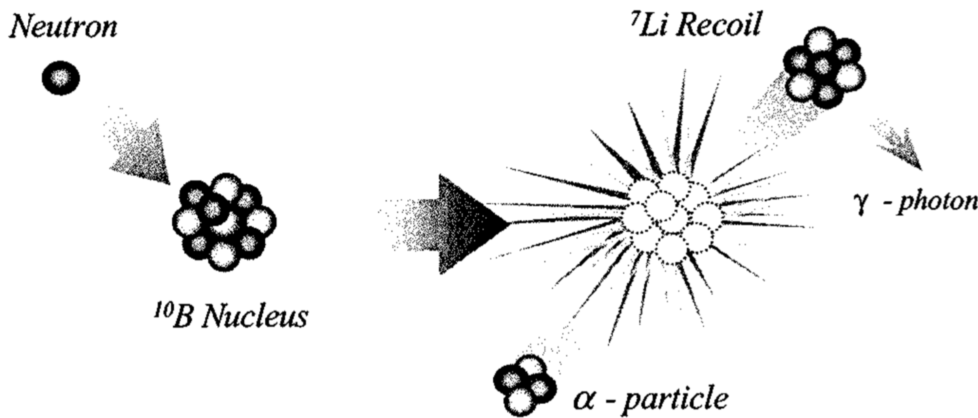


Figure 2.3: ^{10}B Fission [4]

2.2.3 Soft Errors in Memory Devices

Soft errors could corrupt data stored within memory cells without damaging the device, thus making soft errors hard to detect.

2.2.3.1 Soft Errors in SRAM

In a typical 6-transistor SRAM cell, data is stored inside a latch type structure formed by a cross-coupled CMOS inverter pair, and two additional access transistors are used for read/write operations. If a particle strikes the *N-type* Metal Oxide Semiconductor (NMOS) at the *off* position, for example the bottom left NMOS indicated in Figure 2.4a, the excess charge produced in the junction would result in a high current pulse, turning the MOSFET *on*. The now turned-on NMOS will start conducting current through its channel, pulling the *HIGH* nodes to *GND*, as indicated in Figure 2.4b. Figure 2.4c shows the propagation effect, once the *HIGH* nodes get pulled to *GND*, the right inverters toggle, starting to charge up the output node to *HIGH*, which also turns off the left inverter. This feedback loop will eventually flip the bit stored inside the SRAM cell, and lock the cell into a stable condition (Figure 2.4d). This transient current pulse produced by particle strikes works similarly as the write operation during normal operations.

(a) A particle hits an *off* transistor and turns it *on*

(b) The drain node gets pulled down to 0 by the *on* NMOS

(c) Right transistor turns *on*

(d) Stable state where bit flipped [27]

Figure 2.4: 6T SRAM

2.2.3.2 Soft Errors in DRAM

A 1-transistor design DRAM cell consists of an access transistor and a storage capacitor. Unlike an SRAM cell where the data is stored using an active feedback circuit which guarantees the node to be either *HIGH* or *LOW*. A DRAM cell relies on a passive storage component to keep the charge during a refresh cycle. This means that if a particle strikes a DRAM cell, the charge stored inside the capacitor can be degraded to anywhere between the supply voltage and the ground. The data remains disturbed until corrected by an external circuitry [6]. Figure 2.5 shows a DRAM cell under aparticle strike.

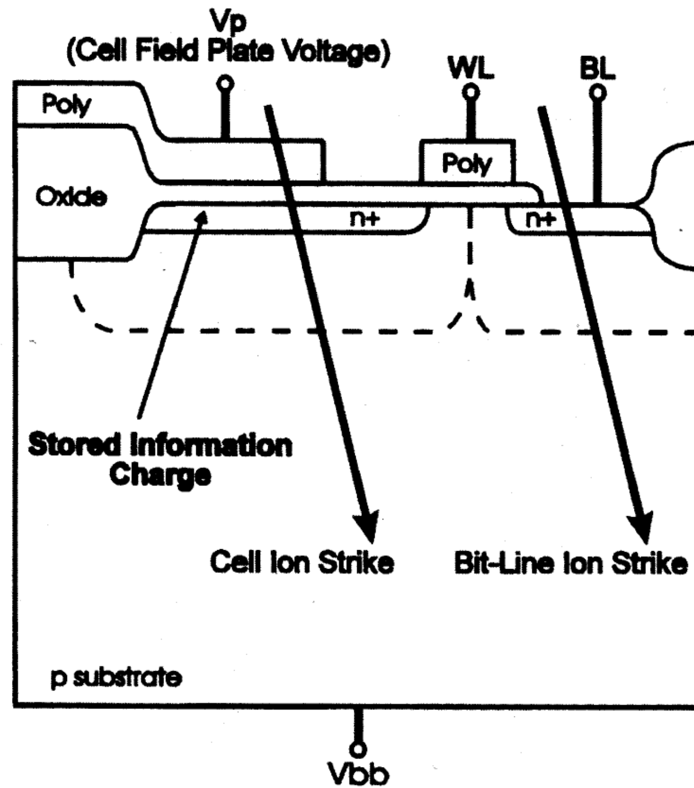


Figure 2.5: The layout of a DRAM cell under ion strike [6]

The strike can happen either close to the storage capacitor, or at a bitline of the storage array. A strike near the storage would directly impact the data stored, and if the data disturbance is larger than the noise margin of the circuit, an upset could occur. For strikes at a bitline, soft errors are possible only when the bitline is in a floating voltage state, or during pre-charge or at the sensing stage [6].

2.2.3.3 Technology Impact

Critical charge (Q_{crit}) is defined as the total amount charge required to cause a bit upset inside a memory cell.

Inside an SRAM cell, Q_{crit} can be expressed as equation 2.1. C_{node} is the node capacitance. V_{DD} is the supplied voltage. I_{D_P} is the conduction current for the *P-type* Metal

Oxide Semiconductor (PMOS) pull-up transistors, and the T_F is the time for the cell to flip [28]. C_{node} and I_{D_P} can be further expanded into equations 2.2 and 2.3 respectively [29].

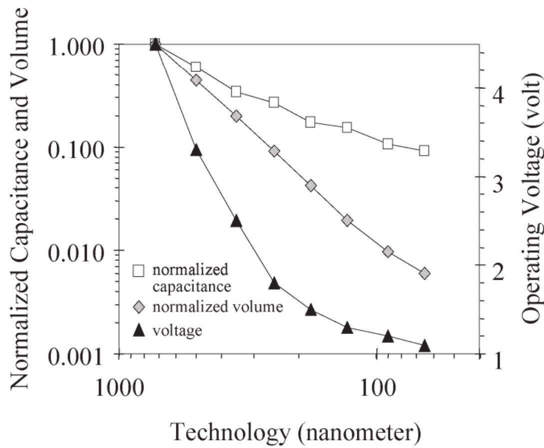
$$Q_{crit} = C_{node}V_{DD} + I_{D_P}T_F \tag{2.1}$$

$$C_{\text{node}} = WL\frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} + C_{\text{j}} + C_{\text{parasitics}} \tag{2.2}$$

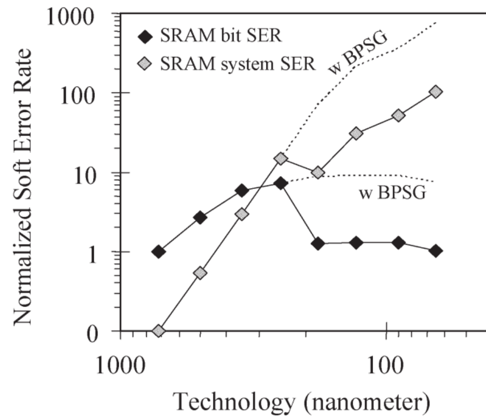
$$I_{\text{D}_\text{P}} = |\frac{\varepsilon}{t_{\text{ox}}}\frac{W}{L}(V_{\text{GS}} - V_{\text{T,P}})V_{\text{DS}}| \tag{2.3}$$

The supply voltage is a dominant factor in deciding the critical charge of an SRAM cell. As can be seen from equation 2.1, decreasing V_{DD} will decrease the critical charge at the sensitive nodes. Based on equation 2.3, decreasing V_{DD} also decreases the drive strength of the stabilizing pull-up transistors, which again leads to smaller Q_{crit}. Equation 2.2 shows the nodal capacitance is a function of width, length, junction capacitance, and parasitic capacitance. As the process becomes more advanced, the transistor size shrinks, resulting in the reduction of the overall nodal capacitance.

Besides Q_{crit}, SER also depends on the radiation sensitive volume of the devices. Shown in Figure 2.6a), the radiation sensitive volume decreases with technology scaling down. A smaller sensitive volume makes it harder for particles to generate more than Q_{crit} charges. However, recall that Q_{crit} decreases with technology. As a result, as shown in Figure 2.6b), the per bit SER remains almost flat with technology scaling [30, 31]. But the per system SER increases with technology because of the increase in density (Figure 2.6b).



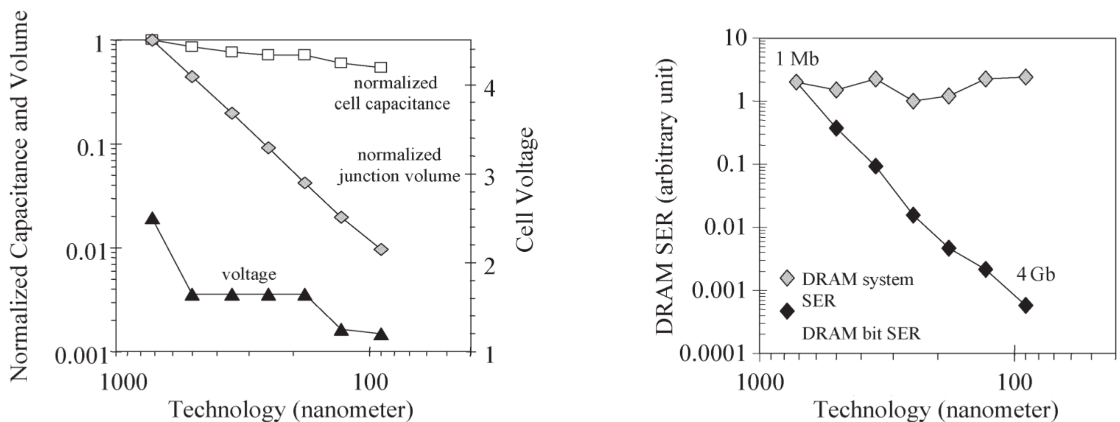
(a) Normalized node capacitance, supply voltage, and junction volume as a function of technology nodes



(b) Normalized bit SER and system SER as a function of technology nodes [21]

Figure 2.6: Technology effects on SRAM

As opposite to SRAMs, the per bit SER for a DRAM is decreasing with technology scaling, shown in Figure 2.7b. Figure 2.7a shows how the capacitance and the junction volume of the DRAM change with technology. Unlike the active feedback approach used in SRAMs to store data, DRAMs have passive cell capacitors. The capacitance has little dependency on technology, and to maintain a robust read margin, the value is constant at 30 fF [30]. The supply voltage does decrease with technology, which decreases the Q_{crit}. But with junction volume decreasing on a much steeper slope, the collected charge is significantly reduced. Combining all these factors, the DRAM bit SER decreases significantly with each process generation. The system level SER remains flat due to that the memory density increases at the same rate as bit SER decreases.



(a) Normalized cell capacitance, supply voltage, and junction volume as a function of technology nodes

(b) Normalized bit SER and system SER as a function of technology nodes [21]

Figure 2.7: Technology effects on DRAM

Particle strikes could also induce failures of more than one bit, known as Multi-Bit Upset (MCU)s. Other than Q_{crit} and the sensitive volume, MCU also depends on the density of the memory array. MCU accounts for only a small percentage of the total faults in older technologies: for a 0.18 um process, 99.9% of failures are single bit failures [5]. In contrast to bit SER, the accumulated MCU probabilities increase per technology generation [32].

Chapter 3

Methodology

We design a custom Printed Circuit Board (PCB) populated with off-the-shelf SRAMs. A separate Field Programmable Gate Array (FPGA) is used to control the SRAMs. This configuration allows the SRAMs to experience SEUs while the FPGA processing of those SEUs does not suffer corruption from radiation. The system is designed to be modular, where each main component can be easily replaced for system upgrade. Figure 3.1 shows the architecture of the dosimeter, which includes four main components:

- a Future Technology Devices International (FTDI) breakout board,
- an FPGA development board,
- a custom interface PCB, and
- an SRAM PCB

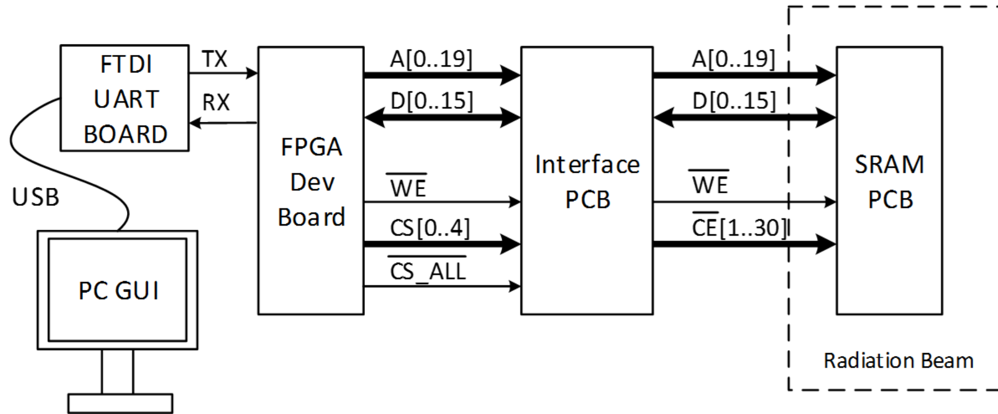


Figure 3.1: The SRAM-based dosimeter architecture showing connectivity and relevant signals

The FPGA is a Terasic Altera development kit and it mounts directly to the interface PCB via headers. The interface PCB decodes the chip select signals (CS) into chip enable signals (CE) to save FPGA I/Os. The SRAM PCB has shared data and address buses, so the interface PCB also contains logic to prevent bus contention and floating inputs. Furthermore, it enables simultaneous writing to all SRAMs through the CS_ALL signal. The FPGA development board and the interface PCB are mounted out of the beam and are connected via ribbon cable to the SRAM PCB. A SparkFun FTDI breakout board is connected to the FPGA to allow communication between the FPGA and the computer using Universal Asynchronous Receiver-Transmitter (UART) protocol.

3.1 SRAM Sensor Design

The biggest challenge of the SRAM-based dosimeter is the design of the SRAM sensor. The soft error rate is usually expressed as Failure in Time (FIT): 1 FIT equals to 1 upset in 10^9 hours of operation, which is about 114,000 years. The system considers each bit flip as a SEU and counts the total number of bit flips per read cycle to predict the radiation fluence. This means SRAM sensor needs to have a measurable FIT rate when in contact

with particles. However, the SRAMs can not be too susceptible to the radiation either, for the following reasons: 1) A single particle strike could also cause MBUs. When an MBU happens, the system will incorrectly count it as several SEUs. If the percentage of MBU becomes non-negligible in the total bit errors, the number of bit flips will not give a clear picture of how many particle strikes happened. 2) If the bit flip probability is very high, one cell would likely encounter multiple bit flips before a single readout occurs, which makes the measured fluence number questionable. 3) The sensors also need to have protection against SEL, SEB, and SEGR. These effects will directly interrupt the operation of the dosimeter, and could cause permanent damage to the dosimeter sensors.

Taking those factors into consideration, thirty 65 nm technology Cypress Semiconductor `CY62167GE30` asynchronous SRAMs are arranged in a close-packed array on a PCB, acting as the sensor of the dosimeter. Each SRAM contains 16 Mb memory (16-bit data line, 1-Mb address line). 30 SRAMS are used to increase the sensitivity of the sensor. Figure 3.2 shows the internal organization of each `CY62167GE30` SRAM chip. The SRAM chip has a built-in ECC scheme which is activated by default to mitigate most of the SEUs in the system. ECC is also a valuable feature to separate SBU from MBU. However, it is necessary to disable the ECC because the purpose of ECC is to eliminate the impact of SEUs, whereas we want to increase SEUs for sensitivity consideration when using SRAMs as dosimeter sensors. Cypress Semiconductor has provided confidential company data to program the SRAM into testing mode and deactivate the ECC function. Other internal data has shown that the SRAM has a suitable FIT rate and MCU to SEU ratio. For example, as will be shown in Chapter 4, irradiation under ¿10 MeV proton beam will cause more than 1000 FIT per Mb for the SRAM.

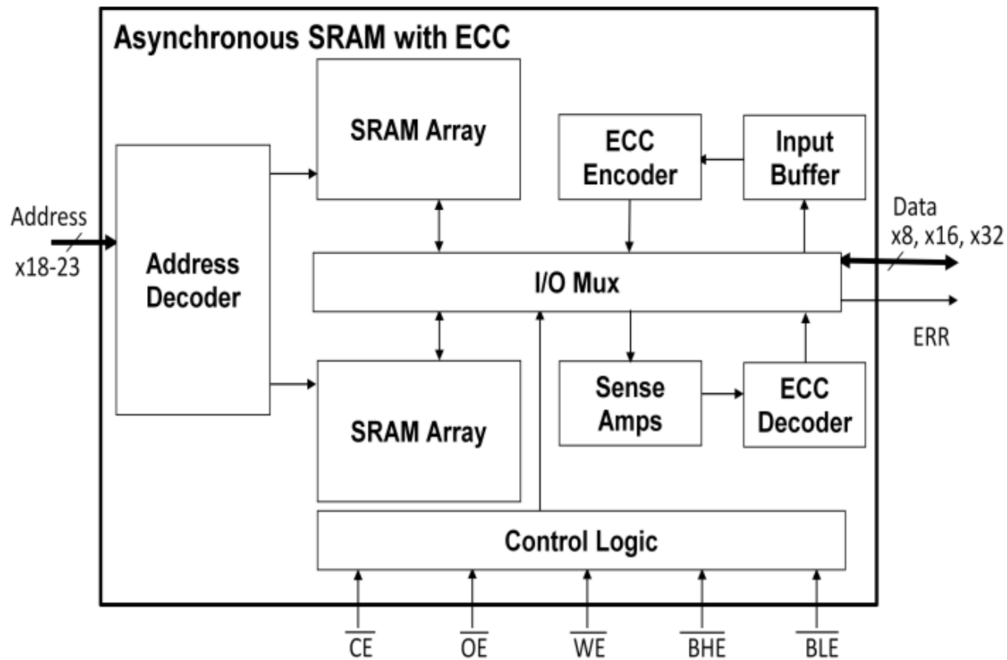


Figure 3.2: Internal organization of the 65 nm Cypress asynchronous SRAM [7]

Figure 3.3 shows the final design of the SRAM sensor board. The eight-layer PCB has footprints for 30 SRAMs, passives, connection headers, and power supply pins. The SRAMs ICs are in 6 mm × 8 mm `VFBGA` packages. The 30 SRAM sensors occupy 41.7 mm × 44.1 mm in total. The CE header provides connections to the chip enable signal of each SRAM. The main header provides connections to power, address pins, data pins and peripheral control logic. A separate power connector is designed on board, offering freedom to change the sensitivity of the system by adjusting the supply voltage of the SRAM sensors. The sensor board is designed to be modular. It can be swapped out from the dosimeter system and replaced with another sensor board. Each SRAM chip is also independently populated, the amount of SRAMs can be reduced to desensitize the system.

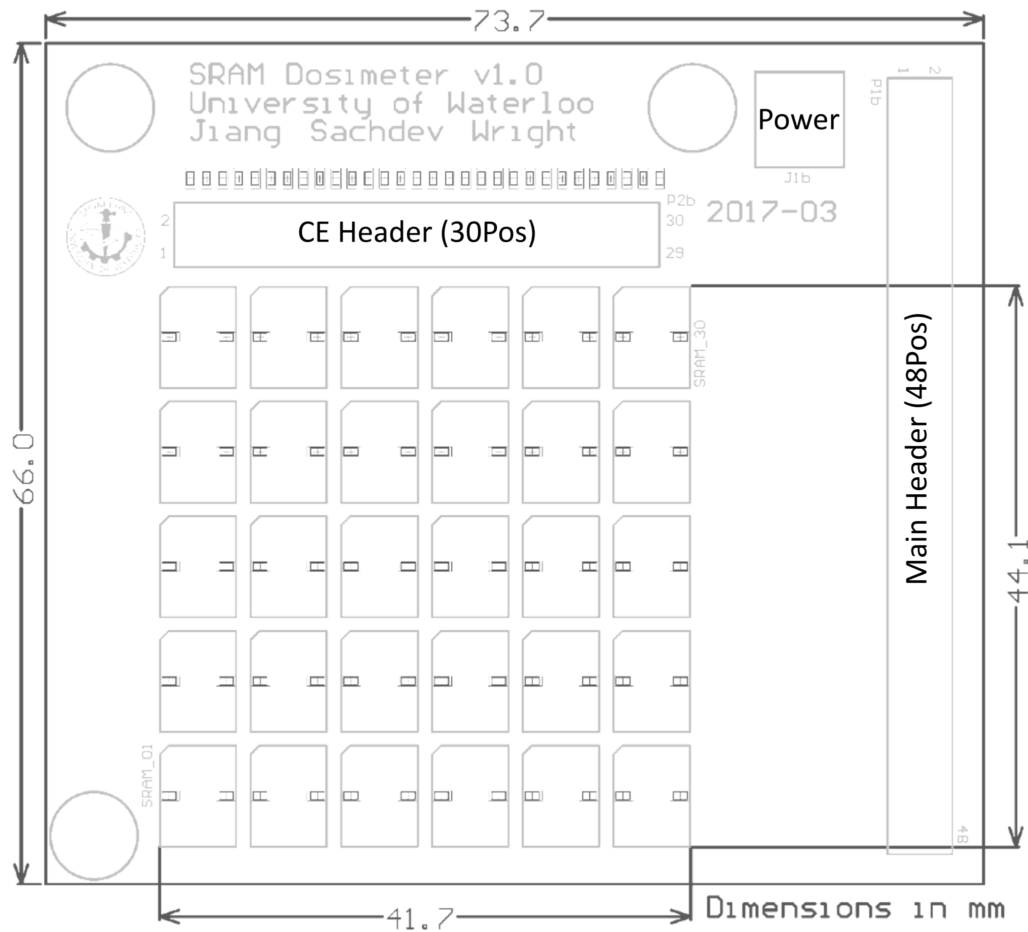


Figure 3.3: Dosimeter PCB diagram showing the active area consisting of 30 SRAM sensors

3.2 Processing Unit

A Terasic DE0-Nano development and education board[33] (Figure 3.4) is selected to be the processing unit of the SRAM sensors. The DE0-Nano contains an Altera Cyclone IV FPGA containing 22,320 logic elements and 64 Mb of serial configuration memory, which can be programmed using the on-board USB-Blaster circuit. Two 40-pin headers are soldered on board providing direct connections to 72 extended pins of the FPGA chip. The headers also include 5V supply, 3.3V supply, and GND pins. Power can be provided

to the board via the USB connector (5V) or the 2-pin power headers. A 50 MHz oscillator is directly connected to the clock input pin of the FPGA, used as the clock source to drive the phase lock loops. Since the dosimeter is not a time critical device, the clock speed is sufficient for our application.

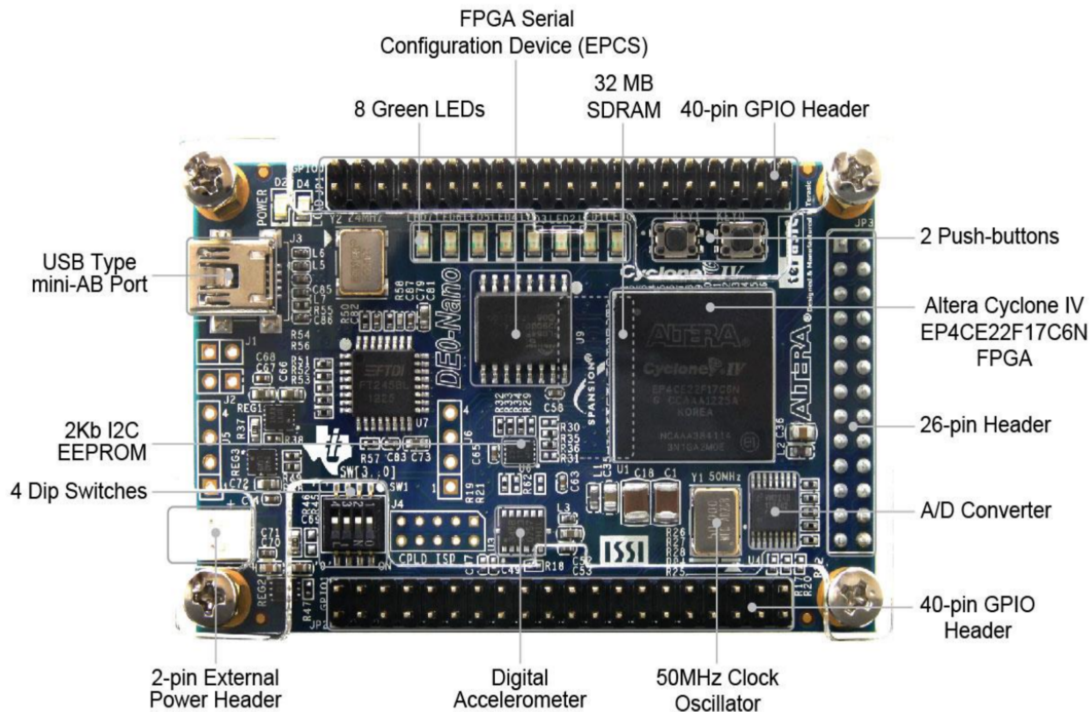


Figure 3.4: DE0-Nano development and education board layout [8]

The FPGA is programmed to control the SRAM sensors and communicate with the GUI installed on a laptop via a USB cable. First, the software will either disable or enable the built-in ECC on SRAMs based on the user's input and then write a user-defined 16-bit data pattern to all the active SRAM sensors. Then, the entire memory space of the active SRAMs is read in sequence and compared with the default pattern. A bit flip indicates one occurrence of a radiation induced soft error. There is a separate error counter associated with each SRAM, allowing the dosimeter to determine the spatial distribution of the radiation beam fluence.

If a bit flip occurs at a particular memory location, the FPGA increments the counter and immediately writes back the default pattern to the memory address. This dynamic writing back reduces the likelihood of miss-counting when a bit double flips, which can be a concern under high fluence. After a complete read cycle is finished, a new read cycle is commenced. In the meanwhile, the counter data from the completed cycle is transferred to the GUI using the 115200 bits-per-second UART protocol through the FTDI breakout board. A complete read cycle of 30 SRAMs takes 3 to 6 seconds, depending on the number bit flips triggered. The state machine diagram of the FPGA processor is in Figure 3.5.

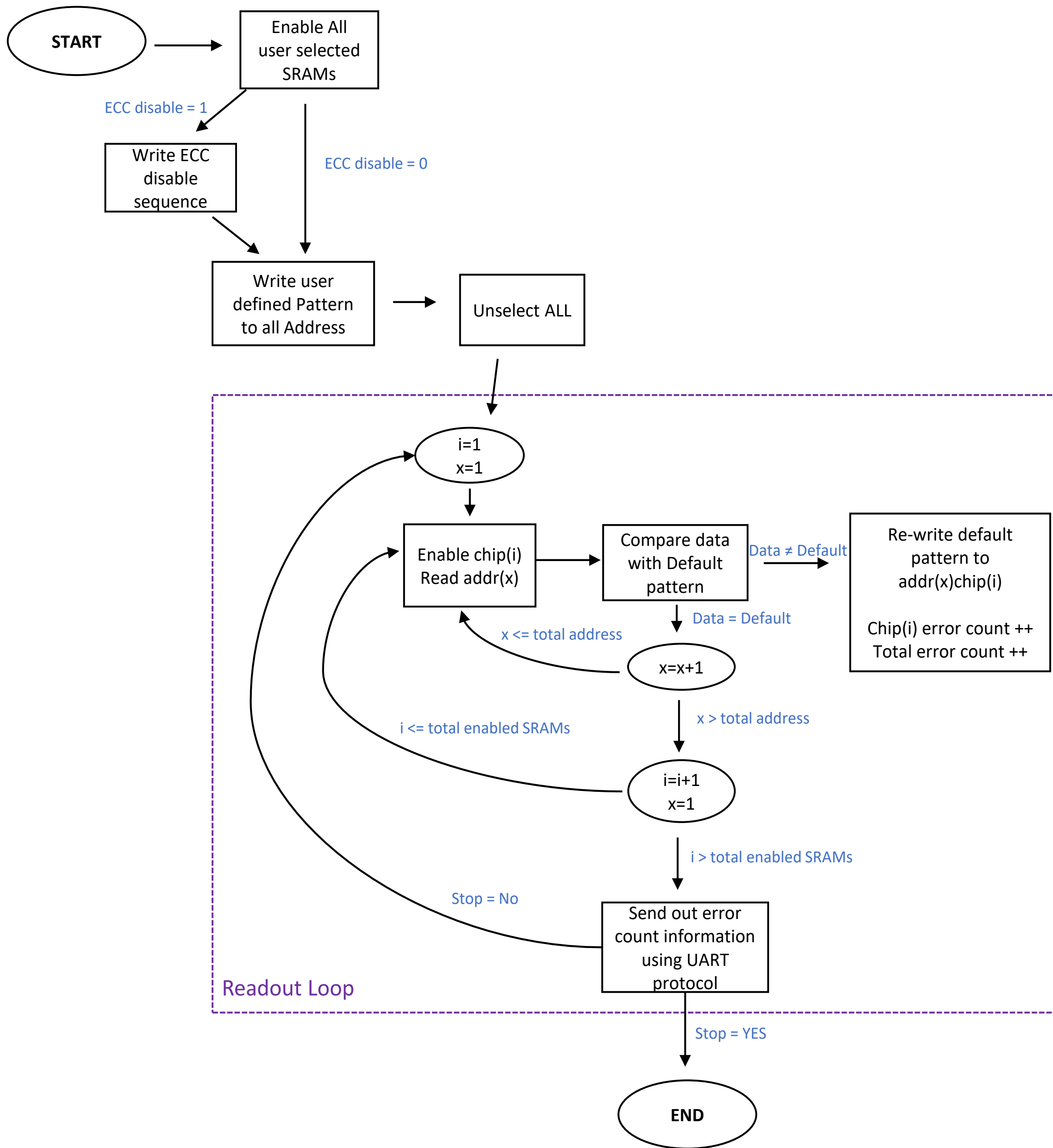


Figure 3.5: State machine of the processing unit

3.3 User Interface

An interactive GUI is coded in `python`. The user can activate and deactivate each of the 30 SRAMs separately, based on the size and intensity of the radiation beam. Several pattern choices, including all 0s, all 1s, checkerboard, and random patterns, are available to choose from. The default supply voltage to the SRAM sensors is 3.3 V. Users have the ability to adjust the voltage from 1 V to 5 V to control the sensitivity of the sensors. ECC is disabled by default, however it can be enabled directly from the GUI. A power cycle to the SRAM sensors is needed for this change. When START button is clicked, the GUI will send user defined information to the FPGA and kick off the FPGA data flow cycle. Users have the ability to pause or stop the acquisition at the end of each readout cycle.

Figure 3.6: Dosimeter GUI during operation

Figure 3.6 shows an example of the GUI when the system is in operation. In this figure,

a checkerboard pattern has been programmed to the sensor chips with a total of 27 sensors activated. Over the course, results can be exported to Excel files without interrupting the operation. Two types of plots are displayed: time view and spatial view. Time view shows the total number of SEUs triggered on the device per read cycle over time, allowing the user to see the consistency of the beam over time. The spatial view displays the cumulative SEUs per chip, which measures the spatial uniformity of the beam.

3.4 The Dosimeter System Setup

Figure 3.7 shows the setup of the SRAM dosimeter system used for testing. The dosimeter was fastened to an aluminium mounting plate, and only the sensor board was in the beam. An SRAM sensor board was populated for the test with 28 SRAM ICs, because out of the 30 ICs, two ICs experienced malfunctions during the population process and were removed from the board to ensure the accuracy of the sensors. It was found during testing that a third IC had a loose connection and was disabled for the remainder of the tests. A laptop running the Windows operating system was used to control the test operations via the proprietary python GUI. For testing simplicity, no external power was used other than the USB port from the laptop. The 5 V USB power is stepped down to 3.3 V on the FTDI breakout board and supplies the entire system. Since no external supply was used, the SRAM sensor board had a fixed 3.3 V supply and the user-controlled voltage function was disabled on the GUI. If an external variable voltage supply is used, the user can set a desired voltage by adjusting the voltage slider on the GUI. The GUI sends the value to the FPGA to adjust the voltage regulator.

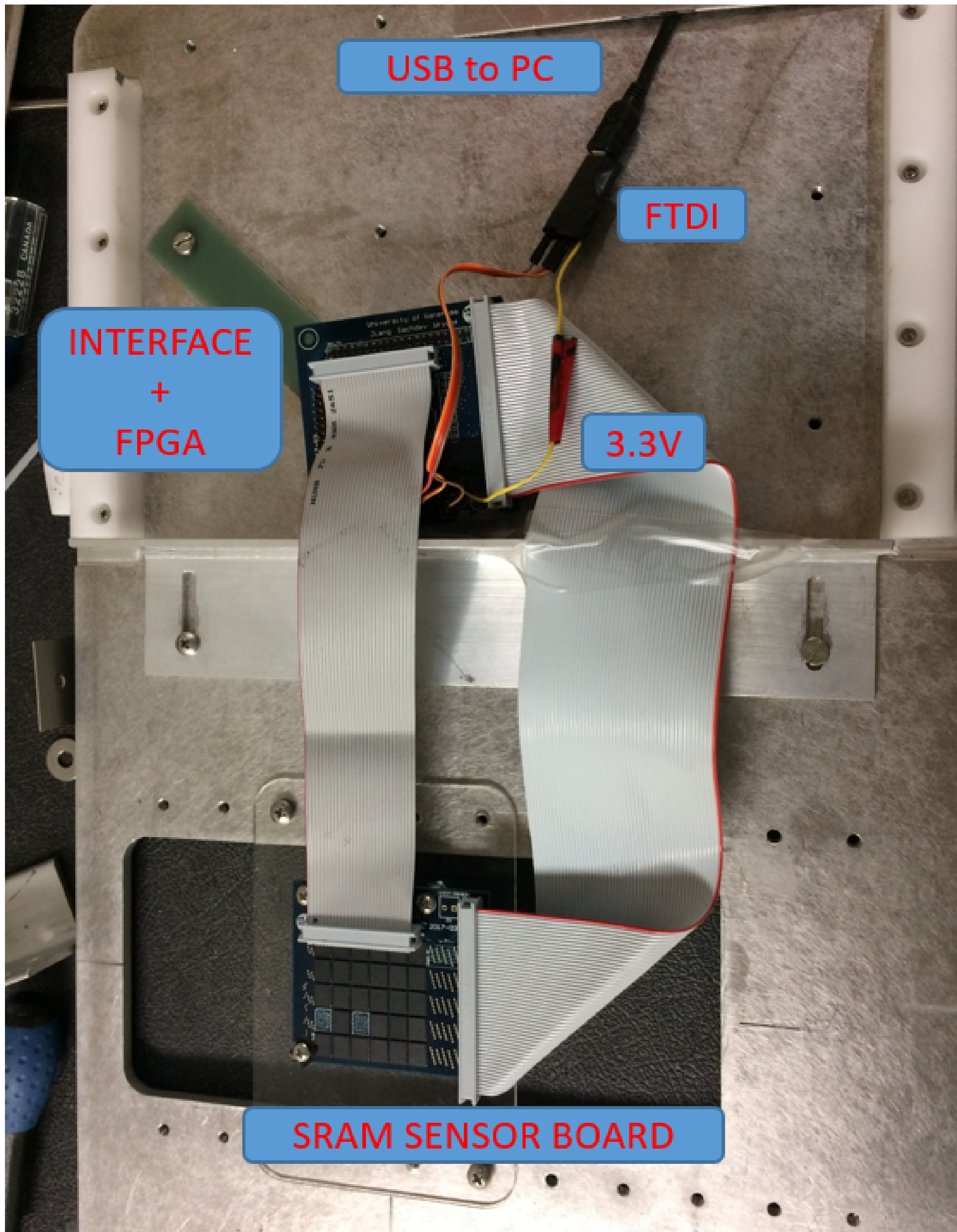


Figure 3.7: Physical setup of the SRAM dosimeter system, including SRAM sensor board and FPGA readout system

Chapter 4

Measurement Results

The accuracy and effectiveness of this SRAM based dosimeter system was tested and validated at Tri-University Meson Facility (TRIUMF) particle accelerator centre by the author of the thesis and other researchers at TRIUMF. In this chapter, we will first introduce the testing facility. Then we will present the results of the measurements done for the proton and neutron beams under different settings that vary in energy (or energy spectrum), fluence, the material and the dimension of the collimator, beam spot sizes, testing locations, etc. The initial measurements were done by the author in October 2017, while the others were done with the help of the author. Many results in this chapter can also be found in our published journal paper [10].

4.1 Testing Facility

Results were measured at TRIUMF particle accelerator centre. TRIUMF's PIF & NIF [34, 13] uses beams of protons and neutrons many times greater than the background radiation, which simulates either prolonged use in the standard environment or uses in radiation-rich environment, like space.

4.1.1 Proton Beam Specifications

PIF & NIF is able to generate mono-energetic proton beams from 65 to 500 MeV. Degraders can be added to degrade energy down to 20 MeV [13, 35]. Two separate beams are used in the facility: BL2C [35] beam which provides energies from 5 to 120 MeV, and the higher energy BL1B [36] beamline which provides energies from 180 to 500 MeV. The protons are extracted from the TRIUMF 500 MeV cyclotron, and transported to the test room where they are collimated and scattered to provide a beam of the desired dimension and flux. An ionization chamber consisting of a total plate and quadrant plates is used to center the beam and measure the proton flux. The BL2C protons extracted from the TRIUMF 500 MeV cyclotron are typically at 116 MeV or 70 MeV. Table 4.1 provides a summary of the characteristics of the proton beams from PIF.

Table 4.1: Proton Beam Characteristics [1]

	BL1B protons	**BL2C protons**
Energy	350 or 480 MeV Some other energies with a degrader	63 or 105 MeV Some other energies with a degrader
Flux (protons/cm^2/s)	Standard location: 10^5 to 4×10^7 (10^2 possible) Upstream location: 7×10^8 max	Standard location: 10^5 to 1×10^8 (10^2 possible) Upstream location: 2×10^9 max
Spot Size	Standard location: 3×3 cm to 7.5×7.5 cm Upstream location: 1 to 2 cm diameter	Standard location: 1×1 cm to 5×5 cm or 7.5 cm diameter Upstream location: 0.5 to 2 cm diameter
Spot Homogeneity	Standard location: ±5% Upstream location: ±10%	Standard location: ±5% Upstream location: ±10%
Beam Counting and Monitoring System	Ion Chamber or Scintillator	Ion Chamber, Scintillator, or Faraday Cup
Device-Positioning System	Remote-controlled X-Y platform with laser alignment	Remote-controlled X-Y platform with laser alignment
Access Conditions	20 m cable length to Control Area	20 m cable length to Control Area

4.1.2 Neutron Beam Specifications

PIF & NIF has three neutron beams: TNF [13], BL1B and BL2C.

The TNF beam can produce neutrons with energies ranging from thermal to 400 MeV. The spectrum of the TNF neutron beam [13] is similar to the spectrum of terrestrial neutrons, with an acceleration factor of 7E+09 based on the JEDEC standards >10 MeV [37]. As shown in Figure 4.1, neutrons are produced by stopping high intensity protons of 450 MeV in a series of aluminum plates (20cm in diameter and 57cm long) immersed in a cylindrical water tank (73cm in diameter). The designed beam power is up to 50 kW. The neutrons, produced in the beam stop, proceed down to a beam channel that is at 60° angle to the incoming proton beam. The neutron channel is accessible from a vertical access hole that intersects with this beam at a location that is 3.6 m from the beam stop. A moderated BF_3 neutron detector is placed after the test location and shielded by 60 cm of steel to ensure the desired counting rate. The TNF has a very high flux of $3 \text{ x } 10^6$ neutrons/cm^2/s for neutrons with energy >1 MeV. It has an irradiation spot of 5×12 cm. While the BF_3 counter is sensitive to thermal neutrons, the interaction decreases as energy goes up. The moderator material and nearby shielding slow down the higher energy neutrons to thermalize them so they can be detected. The BF_3 proportional counters are used for the neutron calibration or normalization. But it does not give any information about the energy spectrum. To calculate the neutron energy spectrum, a nuclear Monte-Carlo FLUKA [38, 39] simulation code is used. Then, a series of activation foil measurements is done to get an absolute flux measurement in different energy regions [13].

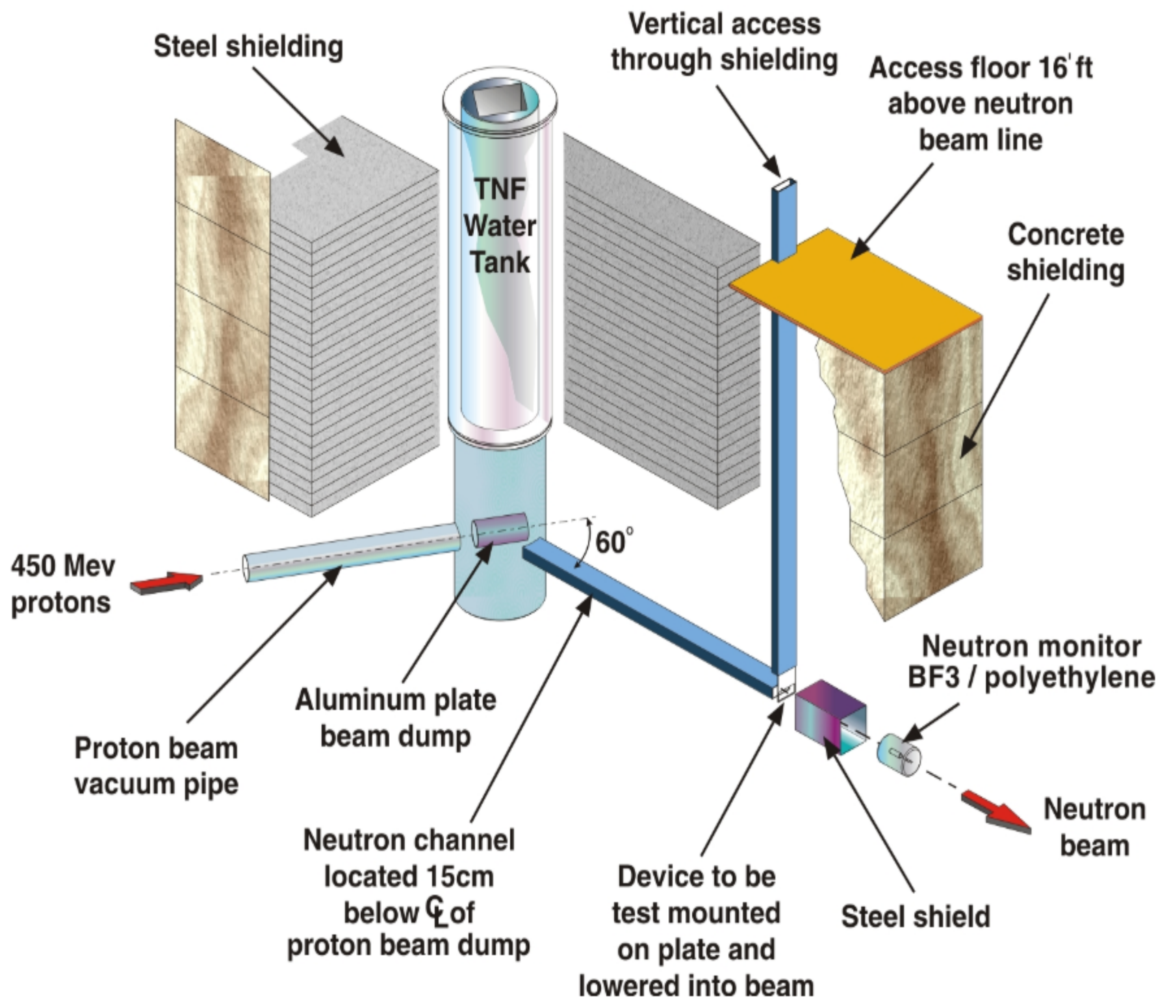


Figure 4.1: TNF plan view [9]

To generate BL1B and BL2C neutron irradiation, protons from BL1B (500 MeV) and BL2C (116 MeV) are completely stopped by a 20 mm lead absorber. The neutron flux and spectrum are measured using Bonner spheres and carbon activation. Neutrons are generated in the forward direction after the absorber. BL1B and BL2C have larger neutron

beams than TNF, but lower neutron flux >10 MeV than TNF. The maximum diameters are 60cm and 150 cm respectively for BL1B and BL2C. Figure 4.2 shows the spectra of the three neutron beams generated at PIF & NIF. The beam spectra are similar to Joint Electron Device Engineering Council (JEDEC) atmospheric neutron reference spectrum [2], with BL1B being the closest. Since terrestrial neutrons have a broad energy spectrum from thermal energies $\approx 0.025eV$ to more than 1 GeV, it is necessary to determine the flux as a function of energy. Table 4.2 provides a summary of the neutron beams' characteristics at TRIUMF.

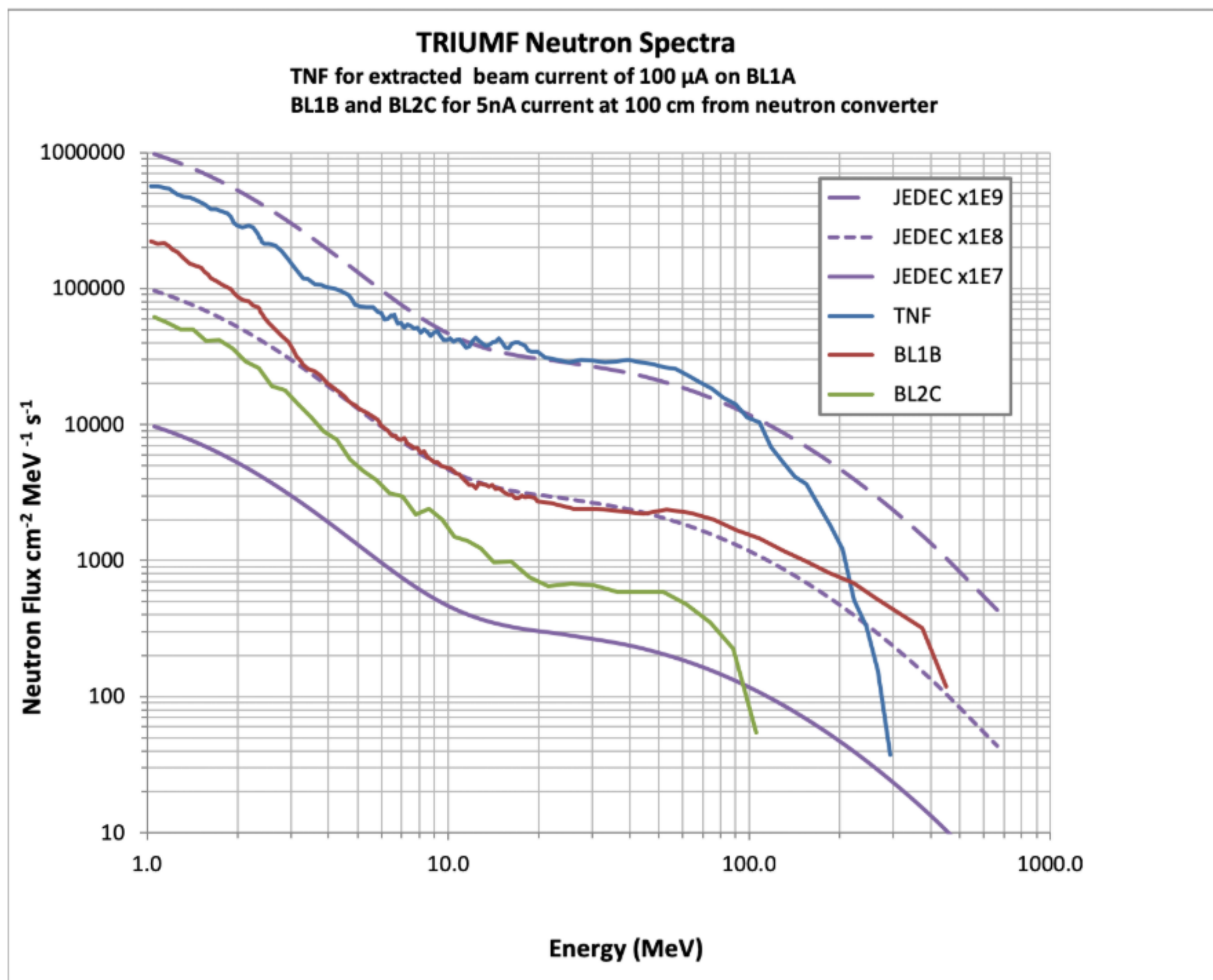


Figure 4.2: PIF & NIF Neutron Spectra [2]

Table 4.2: Neutron Beam Characteristics [2]

	TNF	**BL1B Neutron**	**BL2C Neutron**
Energy	Thermal to 400MeV	1/E spectrum to 480MeV	1/E spectrum to 120MeV
Flux ($n/cm^2/s$)	2×10^6 to 3×10^6 above 10 MeV $5x10^5$ thermal energies	10^3 to 5×10^5 above 10 MeV	10^3 to 5×10^5 above 10 MeV
Spot Size	5×12 cm	4 to 60 cm diameter	30 to 150 cm diameter
Spot Homogeneity	±10%	±10%	±10%
Beam Counting and Monitoring System	BF_3 Counter and Activation Foils	BF_3 Counter and Activation Foils	BF_3 Counter and Activation Foils
Device-Positioning System	Movable Trolley with positive stop	Remote-controlled X-Y platform with laser alignment	Remote-controlled X-Y platform with laser alignment
Access Conditions	6 m cable length to Control Area	20 m cable length to Control Area	20 m cable length to Control Area

4.2 Proton Beam Measurements

4.2.1 BL2C Proton Beam Profile

The BL2C proton beam is extracted at 116 MeV. A thin lead foil is used to scatter the beam to provide a uniform beam of 50 mm $\times$ 50 mm. The proton beam energy is degraded during this process, and the actual energy on the DUT is 105 MeV.

A test to demonstrate the spatial distribution of the radiation flux was conducted using a square brass collimator placed in the beam. The square collimator is 20 mm thick and has a 30 mm $\times$ 30 mm opening. By installing the collimator, the proton beam is confined within the 30 mm $\times$ 30 mm square shape. Ideally, no additional proton radiation should be received outside of this area on the SRAM sensor. The SRAM card is placed in the usual test position, which is 25 cm downstream from the collimator. First, the SRAM dosimeter is directly irradiated under the beam by aligning the center of the dosimeter to the center of the square collimator. Then, shifting in the X-direction of -30 mm (green triangle in Figure 4.3) and 30 mm (red square in Figure 4.3) is performed to map the profile of the proton beam and look for any anomaly. Figure 4.3 shows the normalized SEU rate of the square beam in the X-direction. The SEU rate directly corresponds to the beam intensity. From -15 mm to $+15$ mm, the normalized SEU rate is almost uniform. Figure 4.3 shows that there was a small amount of SEUs triggered outside of the proton beam, which is likely caused by neutrons produced in the collimator when stopping the protons. There are overlap in data points among center position, left position and right position, because the dimension of the dosimeter is 41.7 mm $\times$ 44.1 mm which is longer than the shifting distance of 15 mm.

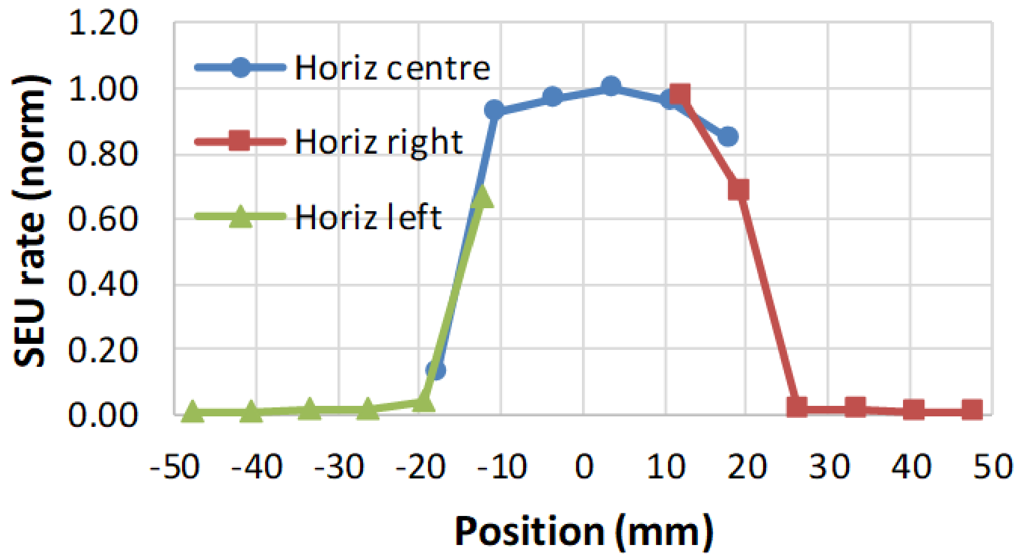


Figure 4.3: BL2C proton beam profile

Figure 4.4 shows the color-map SEU distribution of the dosimeter when a circle collimator with a diameter of 30 mm is placed and aligned with the center of the sensor board. For each SRAM sensor, the accumulative number of SEUs triggered by the proton irradiation is directly displayed in the figure. As expected, the majority of the errors was triggered at the center of the circle. The few SEUs on the corner outside of the circle were again likely caused by the neutrons produced in the collimator, or caused by the beam divergence after exiting the collimator.

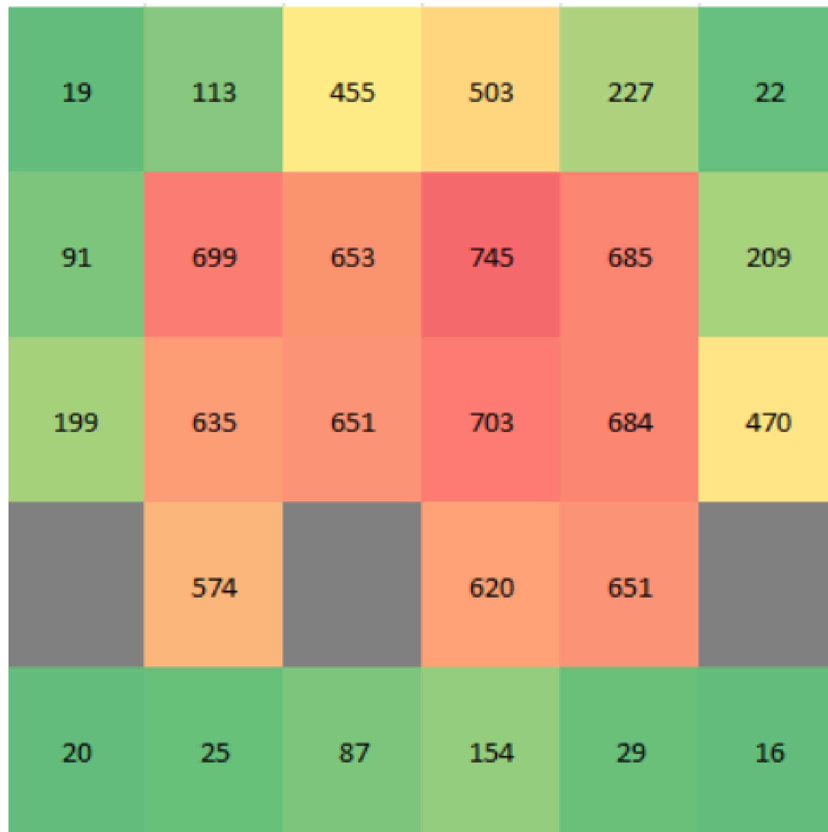


Figure 4.4: SEU distribution for the SRAM sensor ICs when a 30mm diameter circle collimator is installed in front of the BL2C proton beam

Since physical address on the SRAM die for each SRAM is not extracted by the FPGA, the SRAM dosimeter currently has a coarse granularity, that is at the level of each SRAM. Two options could be employed to achieve a finer grained spatial beam profile: 1) use more and smaller SRAMs. 2) use the proprietary SRAM information provided by Cypress Semiconductor to translate the address into an approximate on-die physical location.

4.2.2 Additional BL2C Beam Profile Study

Figure 4.5 shows a more detailed BL2C beam profile study that has been conducted in the paper [10]. The normalized SEU rates are plotted in both linear and log scales.

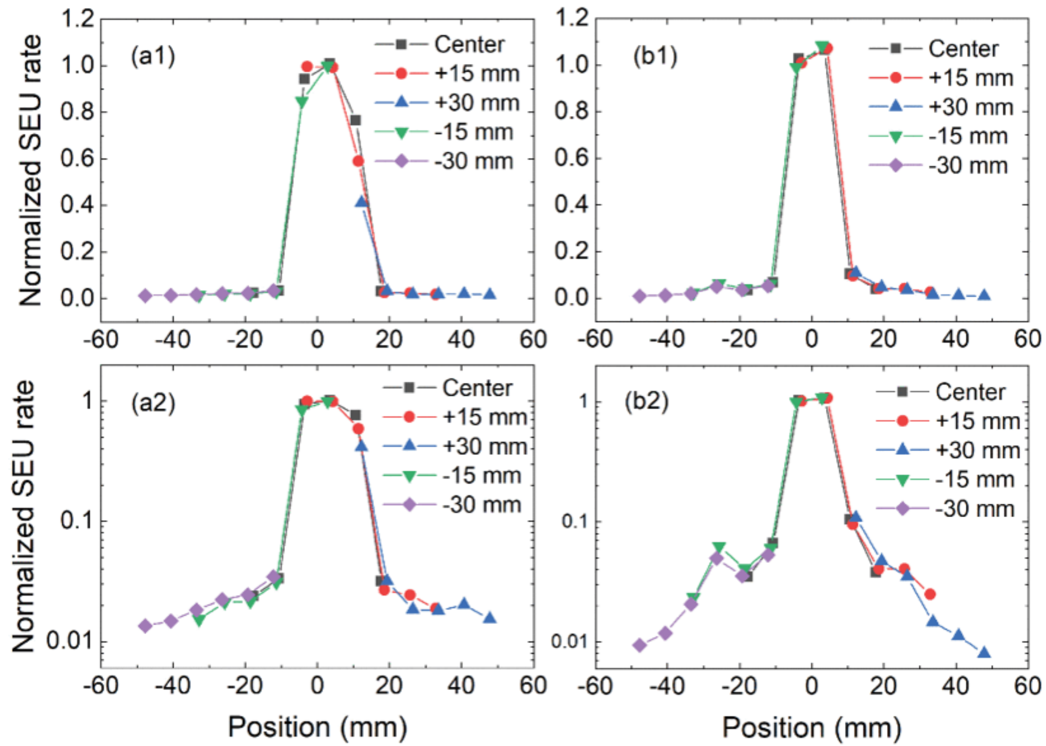


Figure 4.5: BL2C proton beam profiles with 15 mm × 15 mm collimator a1) 25 cm downstream a2) 25 cm downstream, log scale on Y-axis b1) 2.5 cm downstream b2) 2.5 cm downstream, log scale on Y-axis [10]

The 105 MeV proton beam was collimated to 15 mm × 15 mm using a brass collimator. The SRAM dosimeter SEU rate was measured at both 25 cm downstream and 2.5 cm downstream. The dosimeter was first measured at the center of the beam, then scanned across the X-axis from −30 mm to +30 mm, with 15 mm steps. The measurements show a 1-2 % SEU rate outside of the collimated beam at the standard testing location (25 cm downstream). At the 25 cm downstream position, Figure 4.5 shows that the proton beam is wider compared to the 2.5 cm location. This is due to the natural proton beam shaping from the scattering foil.

4.2.3 Sensitivity and Reproducibility

Figure 4.6 shows the dosimeter SEU cross section for BL2C and BL1B proton beams on a log scale. It is noticed that the dosimeter has a much higher sensitivity to low energy protons. For example, in the figure, the peak SEU cross section happens at around 5 MeV. Previous studies [40, 41] have shown that the SEUs triggered by low energy protons are caused by proton direct ionization. In contrast high energy protons, the SEUs are mainly triggered by nuclear reactions. The proton direct ionization strongly depends on the manufacture technology and the angle of irradiation [40], which makes the placement of the dosimeter critical when conducting these type of measurements. The different SEU trigger mechanisms explain the different SEU cross section across the proton energy.

Repeated BL2C SEU cross section measurements are taken one month after the original measurements. They show less than 1% change. The cross section change over the 6 month usage at TRIUMF is reported being between 1% and 2% [10], making the dosimeter a reliable source for beam measurements.

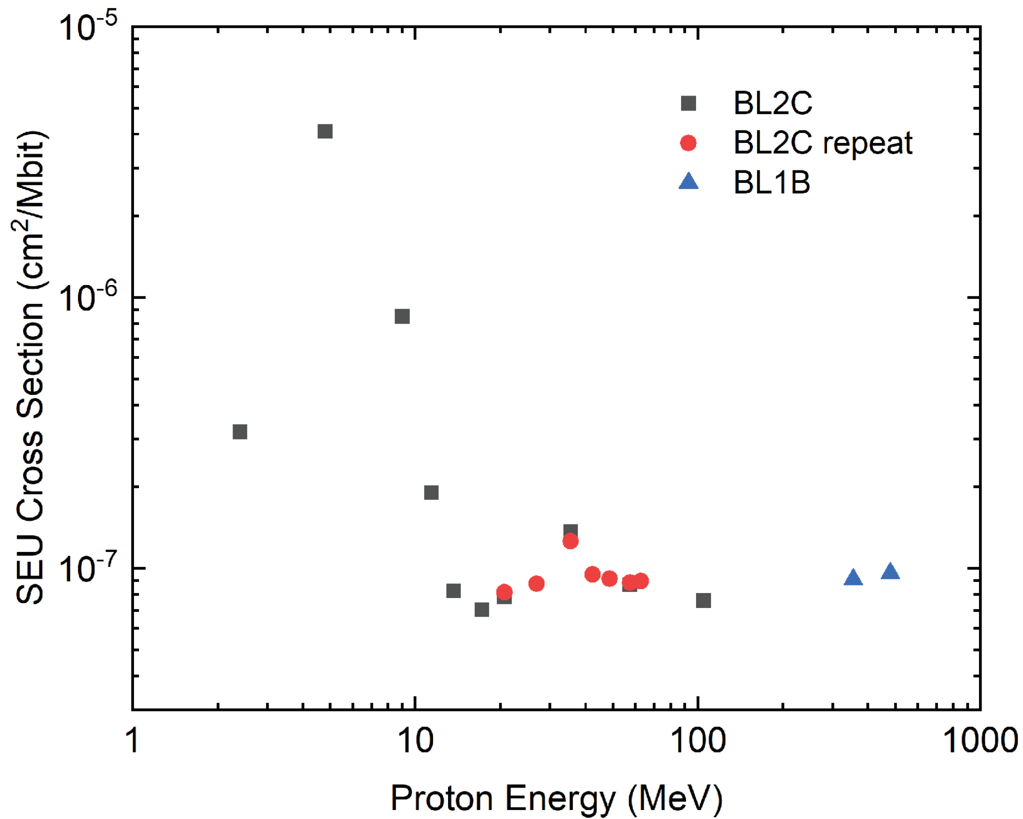


Figure 4.6: Proton SEU cross sections as a function of proton energy, BL2C repeat is taken one month after original BL2C measurements [10]

4.3 Neutron Beam Measurements

4.3.1 SRAM Sensor Default Pattern Study

Table 4.3 shows the performance of the SRAM dosimeter when directly irradiated under the TNF neutron beam > 10 MeV for 8 minutes. The SRAM sensors are placed at the centre position of the beam to ensure uniform irradiation. Twenty-eight ICs were activated during the test, adding up to a total memory size of 448 Mb. Neutron fluence was measured by the neutron counter system provided by the TRIUMF facility. The bit SEU cross section

is calculated as the total number of induced errors divided by the total number of bits and neutron fluence. To calculate the FIT rate, which is the number of failures per 10^9 hours for ground-level neutrons, we need to use the acceleration factor between the TNF neutrons and ground-level neutrons.

Table 4.3: TNF > 10 MeV Neutron Beam Direct Irradiation Results

Default Pattern	Induced Errors	Fluence (n/cm^2)	Cross section (cm^2/bit)	FIT/Mb
All 0s	93,955	2.541E+09	7.870E-14	1101.8
All 0s	91,058	2.475E+09	7.832E-14	1096.5
All 1s	82,666	2.220E+09	7.927E-14	1109.8
All 1s	88,757	2.398E+09	7.878E-14	1102.9
Checkerboard	87,027	2.388E+09	7.757E-14	1086.0
Checkerboard	87,474	2.541E+09	7.870E-14	1084.6

The SRAM dosimeter was tested with three different pre-programmed test patterns: all 0s, all 1s, and checkerboard patterns (alternating ones and zeros). The different SRAM test patterns did not have a noticeable effect on the dosimeter FIT rate. The dosimeter FIT rate is uniform across all six runs under the same beam condition, and averages to 1096.8 FIT/Mb with a maximum absolute percent deviation of 1.1%. Tests with different durations were performed on the SRAM dosimeter with the TNF beam. From Table 4.3, it is noted that:

- The dosimeter is very sensitive to the neutron beam. Over 90,000 irradiation-induced errors are counted within eight minutes. With each three second read cycle the

dosimeter is able to capture > 300 errors, which justifies the dosimeters real-time performance, returning valid measurement results within seconds.

- The results are highly reproducible.

To further understand the cross section of the SRAM, repeated measurements were taken with the sensor board moved ±12.5 mm vertically from the original position with 3.1 mm steps. It was found that the card was originally placed too low where the top row of the SRAM sensors was not irradiated properly. The sensor board was moved 6.2 mm higher from the original position for further studies. The misplacement has resulted in under-estimating the FIT/Mb by 10%, while the actual average FIT/Mb being 1267.

4.3.2 Sensor Uniformity

Figure 4.7 shows the percent error of each SRAM sensor with respect to the mean of all 27 active SRAMs. A long exposure to the neutron beam was used for this test to ensure that each SRAM was exposed to a uniform amount of radiation. The dosimeter was irradiated for 27.6 minutes under the TNF neutron beam, corresponding to 470 complete cycles of data captures. 313,971 errors occurred. Each SRAM had a slightly different soft error rate (SER), with 8.4% maximum absolute error. The percent deviation of the dosimeter is 3%. The TNF neutron beam has been profiled by radiochromic film, where some non-uniformity was found across the beam spots [13]. Some of the deviations among the SRAMs could be due to the non-uniformity of the beam.

If spatial beam irradiation is a point of interest, each SRAM should be calibrated separately at the same location in a plane normal to the beam's axis to mitigate any difference in the beam profile.

-8.4	-2.7	-5.2	-1.5	4.7	0.1
-0.3	-3.7	-1.2	-0.2	0.9	4.8
-1.6	3.3	1.4	1.1	1.4	1.8
N/A	4.1	N/A	-0.6	1.6	N/A
1.8	-0.9	-5.0	1.0	1.4	2.0

Figure 4.7: Percent error of each SRAM sensor using TNF neutron beam

4.3.3 Beam Profile

The neutron beam profiling was done for both the TNF beam and BL1B beam. Figure 4.8 shows the TNF beam profile. The SRAM dosimeter was shifted both horizontally and vertically to map the 2D profile of the beam. The results show a 5 cm $\times$ 12 cm beam profile, which is in alignment with TRIUMF's beam specification as well as the previous measurements conducted using radiochromic films [13].

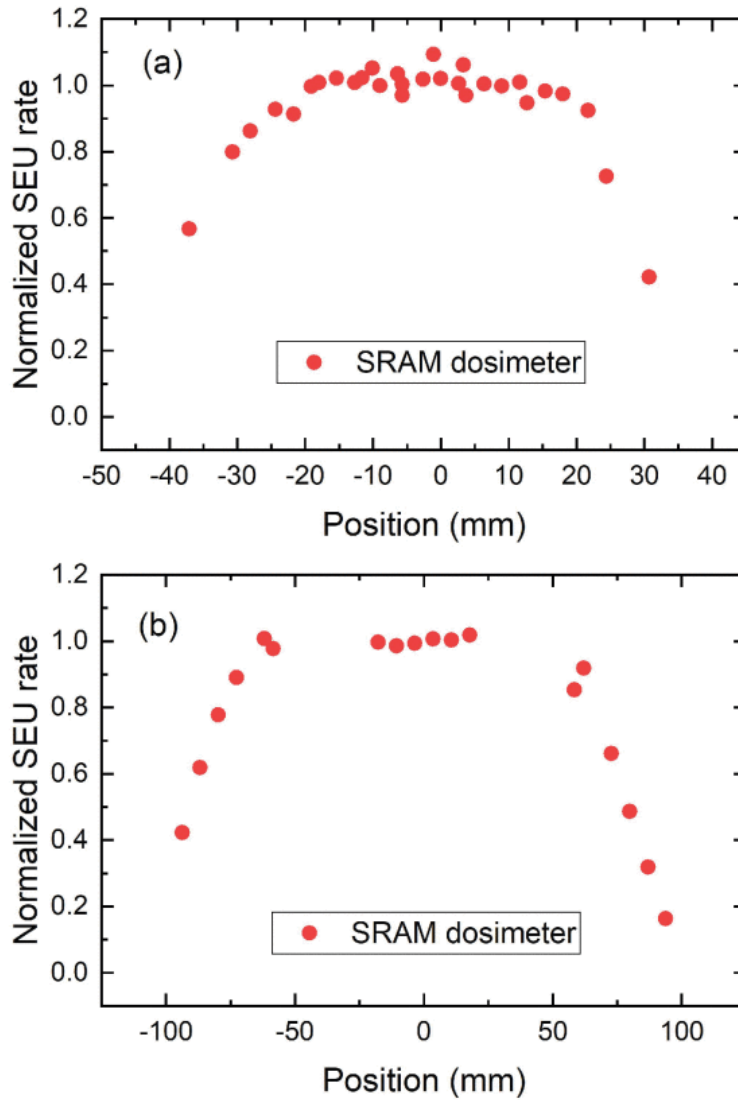


Figure 4.8: TNF neutron beam profile [10] a) Vertical b) Horizontal

Figure 4.9 shows the uncollimated BL1B beam profile measured with the SRAM dosimeter positioned at 150.5 cm from the lead converter. The dosimeter was moved at 6 cm step to the left or right from the centre to map the horizontal beam profile up to ±14 cm. Since the sensor is about 4 cm wide, a 2 cm data point is missing between consecutive moves.

Using the beam diameter calculator provided by TRIUMF [42], the beam diameter should be around 25 cm, which agrees with the beam profile measured by the SRAM dosimeter.

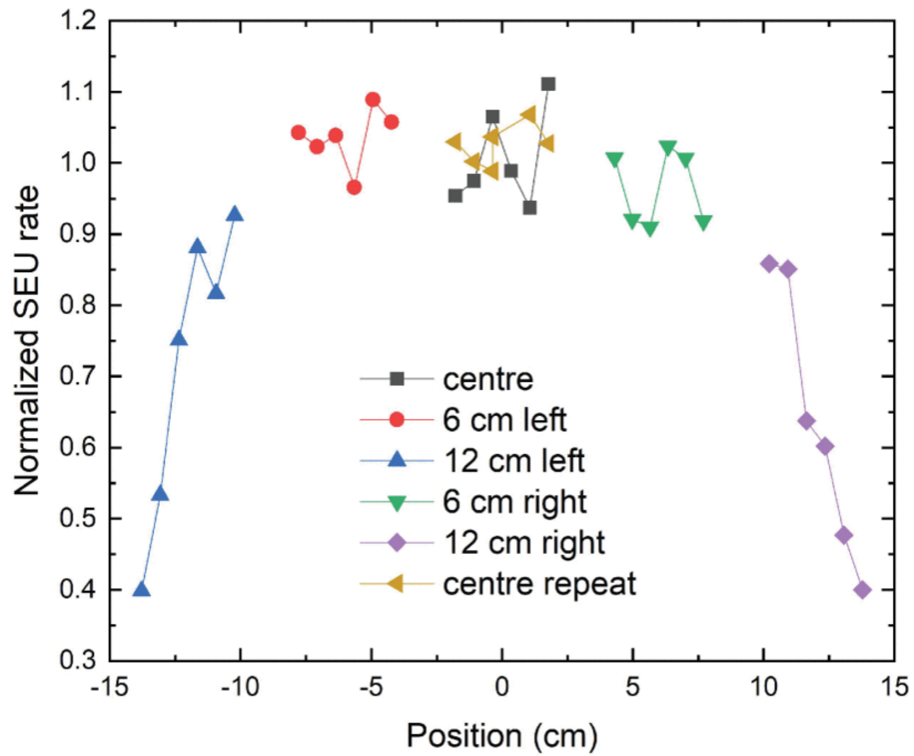


Figure 4.9: BL1B neutron uncollimated horizontal beam profile [10]

Chapter 5

Conclusion

As technology scaling progresses, electronic devices have become increasingly susceptible to radiation, which in turn increases the importance of accurately measuring radiation exposure. In this thesis, an SRAM based dosimeter has been designed and implemented. The dosimeter uses its susceptibility to ionizing radiation as a means of measuring the radiation fluence. The dosimeter has been used at TRIUMF proton and neutron facility under multiple tests. The key results for the SRAM dosimeter from the measurements at TRIUMF that the author participated are:

- All thirty SRAM sensors have a uniform cross section, making the device easy to calibrate. The percent deviation for the sensors is 3%.
- The SRAM dosimeter is able to accurately map the beam profile (real-time) for all the measured proton and neutron beams (TNF neutron beam, BL1B neutron beam, BL2C proton beam, BL1B proton beam).
- Repeated measurements were taken on the BL2C proton beam one month after the original measurements. The difference was less than 1%. After six month of usage, the difference was only 1% to 2%.
- The dosimeter shows high sensitivity to > 10 MeV neutrons/protons. An 8-minute test under TNF > 10 MeV neutron beam will induce $> 80,000$ errors.

- Collimated proton beam measurements have shown that the brass collimator unintentionally produces neutrons while stopping the proton beam.

The test results obtained at TRIUMF validate the conjecture that this SRAM dosimeter can be used as a neutron and proton beam dosimeter in radiation testing facilities. Moreover, the device has been adopted by TRIUMF as radiation beam characterization tool. More recently, at the TRIUMF facility, the measured beam profile using this dosimeter over a spatial range much larger than the collimated beam size was compared against the simulated beam profile, and the results showed good general agreement [43].

5.1 Future Work

- More tests should be conducted with ECC enabled to understand the increasing error rate observed in the measurements.
- Beams with >1 MeV were measured with the dosimeter. Lower energy beams have yet to be measured with the dosimeter. More measurements can be done for lower energy proton and neutron beams.
- An external power supply can be used to adjust the sensitivity of the dosimeter. Adjusting the supply voltage to the SRAM sensor could potentially increase the dosimeter's sensitivity to low energy protons and neutrons.
- SRAM sensors with a technology other than the 65 nm can be used to study the implications of technology scaling.
- New SRAM sensor PCBs can be designed for beams with low energy or ultra high energy.
- Wireless transceiver can be used instead of long USB cables for the communication between the SRAM dosimeter and user computer. The wireless design would make the dosimeter truly portable.

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