Development of Ultrasonic Devices for Non-destructive Testing: Ultrasonic Vibro-tactile Sensor and FPGA-Based Research Platform

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

This thesis is focused on the development of ultrasonic devices for industrial non-destructive testing (NDT). Ultrasound is generated from mechanical vibrations and then propagates through the medium. Ultrasonic devices can make use of the ultrasound in both aspects, vibrations and propagations, to perform inspections of the objects. To this end, two devices were developed in this research, each pertaining to NDT of the objects.

The first device is the vibro-tactile sensor which aims to estimate the elastic modules of soft materials with minimally invasive technique. Inspired by load sensitivity studies in the high-power ultrasonic applications, vibration characteristics in resonance were utilized to perform the inspection. Only a minimal force to ensure contact with the object surface needs to be applied for a vibro-tactile sensor to perform inspection of the object; hence, it can be used for in-vivo measurement of the soft materials' elastic moduli without causing severe surface deformation. The design and analysis of the device were carried out using the electro-mechanical analogy to address the electro-mechanical nature of piezoelectric devices. The designed vibro-tactile sensor resonates at ~40 kHz and can be applied to differentiate the elastic modulus of isotropic soft samples with a range from 10 kPa to 70 kPa.

The second device developed is a field-programmable development platform for ultrasonic pulse-echo testing. Ultrasonic testing, utilizing sound wave propagation, is a widely used technique in the industry. The commercially available equipment for industrial NDT is highly dependent on the competence of the inspector and rarely provides the access to raw data. For successful transition from traditional labor-intensive manufacturing to the next generation "smart factory" where intelligent machines replace human labor, inspection equipment with automated in-line data collection and processing capability is highly needed. To this end, a flexible platform which provides the access to raw data for algorithm development and implementation should be established. Therefore, an affordable, versatile, and researcher-friendly development platform based on field-programmable gate array (FPGA) was developed in the research. Both hardware and software development tools and procedures were discussed. In the lab experiment, the developed prototype exhibited its competence in NDT

applications and successfully carried out hardware-based auto-detection algorithm for mm-level defects on steel and aluminum specimens. Comparisons with commercial systems were provided to guide future development.

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Dedication

This thesis is dedicated to

My parents and family members

All lab members

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Nomenclature

AC	Alternating current
ACAN	Advanced contract award notice
AD/DA	Analog-to-digital/digital-to-analog
ADC	Analog-to-digital converter
AFE	Analog front end
AHB	Advanced High-performance Bus
AI	Artificial Intelligence
ALM	Adaptive Logic Module
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
API	Application programming interface
APT	Advanced packaging tool
ARM	Advanced RISC Machine / Acorn RISC Machine
ASIC	Application-specified integrated circuit
AXI	Advanced eXtensible Interface
BNC	Bayonet Neill-Concelman
BOM	Bill of materials
BPF	Band-pass filter
BT	Bismuth titanate
BVD	Butterworth-Van Dyke
CLB	Configurable Logic Block
CPU	Central processing unit
CV	Coefficient of variation
DAC	Digital-to-analog converter
DC	Direct current
DHCP	Dynamic host configuration protocol
DSP	Digital signal processor

EDA	Electronic design automation
EMI	Electro-magnetic interference
ESO	Evolutionary structural optimization
FEA	Finite element analysis
FF	Flip-flop
FIFO	First-in first-out
FPGA	Field-programmable gate array
FSM	Finite state machine
FTP	File transfer protocol
GPIO	General purpose input/output
GPU	Graphics processing unit
GUI	Graphical user interface
HDL	Hardware description language
HLS	High-Level Synthesis
HPS	Hard processor system
HSMC	High-speed mezzanine card
HV	High voltage
I/O	Input/Output
IC	Integrated circuit
IP	Intellectual property
JTAG	Joint test action group
KVL	Kirchhoff's Voltage Law
LN/VGA	Low noise/variable gain amplifier
LPF	Low-pass filter
LUT	Look-up table
LV	Low voltage
MAC	Multiply-accumulate
MEMS	Micro-electro-mechanical systems
MOSFET	Metal-oxide-semiconductor field-effect transistor

NDT	Non-destructive testing
NRE	Non-recurring engineering
PA	Phased array
PCB	Printed circuit board
PIO	Parallel input/output
PLL	Phase-Locked Loop
PRF	Pulse repetition frequency
PVDF	Polyvinylidene fluoride/difluoride
PZT	Lead zirconate titanate (Pb[Zr(x)Ti(1-x)]O3)
R&D	Research and development
RAM	Random-access memory
RCL	Resistor, capacitor, and inductor
RF	Radio frequency
RISC	Reduced instruction set computer
ROM	Read-only memory
RTL	Register-transfer level
SDC	Synopsys design constraints
SDRAM	Synchronous dynamic random-access memory
SFTP	Secure file transfer protocol
SIMP	Solid isotropic material with penalization
SMT	Surface mount technology
SoC	System-on-Chip
SPC	Statistical process control
SRAM	Static random-access memory
SSH	Secure shell protocol
TOFD	Time-of-flight diffraction
UART	Universal Asynchronous Receiver/Transmitter
UT	Pulse-echo ultrasonic testing
VCO	Voltage-controlled oscillator

VGA	Video graphics array
VNC	Virtual network computing

Chapter 1
Introduction

1.1 Thesis Outline

This thesis describes two research projects:

The first project is the design and analysis on an ultrasonic vibro-tactile sensor. A prototype was developed with a technique combining the analytical derivation and successive finite element analysis (FEA). Both the design and analysis were conducted with electro-mechanical analogy and the electrical behavior of the sensor was analyzed and adopted as a sensing reference for applications. The second project is the development of an FPGA-based research platform which can implement hardware-based algorithm. The research platform is configured into an ultrasonic pulse-echo inspection system to test the performance.

The thesis is composed of five chapters. The first chapter introduces the overall background, related technology, and objectives of the projects. The second chapter discusses the methodology to tackle the problems. The third chapter details the development and analysis of the ultrasonic vibro-tactile sensor. The fourth chapter focuses on the prototyping and experiment of the FPGA-based research platform. Finally, the fifth chapter gives conclusions and discussions for future work.

1.2 Backgrounds

Non-destructive Testing (NDT) is an examination technique to evaluate the integrity of a material, a mechanical component, or other parts without causing physical damage [1]. Ultrasound has been used for NDT for decades. The long history of the ultrasonic NDT made the technology popular in the industry but also stereotyped as an application utilizing wave propagation.

1.2.1 Vibro-tactile Sensor

Ultrasound is the result of mechanical vibrations. However, when an ultrasonic testing is mentioned, it is instinctive to picture the time-of-flight diffraction (TOFD) applications where the underlain physics is wave propagation. The aspect of mechanical vibrations is

over-shadowed by the former's success and seldom referred to in NDT applications, although it has flourished in the high-power applications like ultrasonic cleaning and ultrasonic welding. In normal ultrasonic testing where wave propagation is used, the requirement for impedance matching demands special care to be paid in probe selections regarding the object under test. Similarly, the load sensitivity is problematic in high-power ultrasonic applications as it can cause the equipment to underperform in a shifted frequency; thus, vibration behaviors should be closely monitored and controlled. Inspired by the load sensitivity, it can be deduced that the vibration characteristics can be used to differentiate the characteristics of the object in contact with the probe.

Probes which perform measurements by physical contact can be categorized as tactile sensors. When the physics behind the tactile measurement is vibration at ultrasonic frequencies, it becomes an ultrasonic vibro-tactile sensor. The sensitivity given by the nature of vibrations is not only an exceptional asset in terms of detection threshold but also a big challenge in implementation, as the process should be carefully controlled to allow the change reflecting only the effect of loading from test objects. Although less popular than the other ultrasonic NDT methods, there were some ultrasonic vibro-tactile sensors proposed and developed over the years. Those sensors demonstrated their potential as a tool for tissue measurement [2–4] and non-solid (gas, water) identification [5]; however, they still need further improvements in the design for practical applications.

1.2.2 Non-destructive Testing

On the other hand, the conventional ultrasonic NDT is popular in the industry for quality assurance; however, the use of the technology still relies heavily on trained specialists. Ultrasonic NDT systems available on the market can provide good measurement results, but trustworthy interpretation of the data can only be expected from qualified personnel. One severe limitation is the lengthy period of training that is required for an individual to become fully qualified [6], as it is important to ensure a full understanding of the technique's limitations and capabilities but is an expensive burden for the industry. In critical applications such as inspections for nuclear power plants, where time and cost are not

prioritized, the inspector can take enough time for the inspection and interpretation to derive a sound conclusion with care. However, in case of mass-production line such as automotive industries, it is almost impossible for human to perform in-line inspection, let alone the fact that human can fatigue under intense workload [7]. To facilitate the manufacturing, screening inspection is only included during the establishing phase of the production line. In the production phase (when the production line matures), the process will be monitored with statistical process control (SPC), meaning that the inspections are done only on sampled products. The control limits are usually set within the design specification limits. If any abnormality is found in the sample out of the control limit, the production line will be interrupted and the whole batch will be disposed due to the fact that item-wise inspection is impossible [7–9]. This huge waste and uncertainty can be avoided if in-line inspection can be facilitated so that the problem can be detected on spot. Incorporating the automated inspection into the manufacturing helps successful transition from traditional labour-based manufacturing to the next generation "smart factory" where full industrial automation is commencing. Human error can be minimized and/or excluded from the manufacturing and inspection process. It all depends on the viability of the trusted measurement and proper interpretation of data.

Under the current ultrasonic inspection philosophy, the commercial measurement systems are highly dependent on the competence of inspectors by providing standardized cooked data and are very stingy in granting access to raw data. The human interaction with commercial systems closes the inspection loop. For automated inspection process, the data should be processed in a way that the on-board algorithm can "comprehend"; hence, it requires the access to raw data and a platform to implement and adjust the algorithm easily. The existing commercial platforms for research in ultrasound are expensive, bulky, and aiming at providing closed hardware solutions to signal acquisition [10]; The basic concept of such development platform confines the methodology to only software approaches which deprived researchers of opportunities to solve the problem with hardware implemented algorithm. The in-line inspection poses challenges to system's portability and processing speed. Because ultrasonic data processing or even the implementation of artificial intelligence (AI) interface

does not require advanced computing functions [11], the pure hardware realization is perfectly doable [12]. The speed of hardware processing can surpass its software comparator which is getting more and more complex over the years [13,14]. At the meantime, the increasing versatility of field-programmable gate array (FPGA) packages paves the way to portability.

1.3 Literature Reviews

1.3.1 Ultrasound and Piezoelectric Materials

The nominal human hearing range is 20 Hz to 20 kHz [15]. Ultrasound is thereby defined as sound waves that have frequency beyond 20 kHz, inaudible to the human ear. Ultrasound is the result of mechanical vibrations and requires a medium to propagate. There have been many applications developed in science, industry or medicine utilizing ultrasound [16–18]. To generate the ultrasound, two different physics can be utilized: magnetostriction and piezoelectricity. The argument on the better technology to generate the ultrasound between these two has been almost resolved with the development of piezoelectric materials. With the improvement of the quality of piezoelectric composites over the years, the inherent advantages such as short response time (capable of producing higher frequency signals), lower loss in the system, and ease of customization make the piezoelectric effect preferable in most cases [19–21].

As a burgeoning research topic ever since the discovery of direct piezoelectric effect in 1880 by Curie brothers, many different piezoelectric materials were developed over the centuries [21]. Other than the piezoelectric perovskite (like PZTs), piezoelectric polymers (e.g. PVDF) were also synthesized and found useful in medical applications because their low acoustic impedance is advantageous for soft biological objects [22]. Since the synthesis of a piezoelectric material is not in the scope of this research, rather than evaluating various piezoelectric materials individually, understanding the characteristics and the common definition on the properties of the currently prevailing piezoelectric materials have the priority in the study. Technical information provided by individual manufacturer is usually enough to select a suitable material for conducting a practical design of the system. Through

the preliminary R&D process, it was found that the piezoelectric standard provided by IEEE [23] is useful in finding the relationship between parameters defined by various researchers. The standard is beneficial to the theoretical modeling of the piezoelectric devices (usually by constructing the equivalent circuit of the mechanical system), especially for the analytical analysis on transducers [24].

It is worth noting that the piezoelectric materials are not isotropic due to its crystal structure for ceramics or compound for polymer, so that the mechanical properties, such as compliance of the material, should be given in 2D tensors [23,25,26]. But, since most practical designs of a piezoelectric device utilize only one isolated vibration mode, single value definition is commonly acceptable with clear indications of the direction of the property [27]. A conventional definition of the indices on the direction is shown in Figure 1.1.

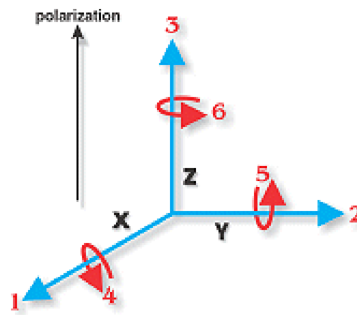


Figure 1.1: Directions defined for piezoelectric materials [27].

In the definition of the electrical properties of a piezoelectric material, the relative dielectric constant and the dissipation factor tangent, or loss tangent ($\tan\delta$), are usually given. Inherently, the piezoelectric material acts like a capacitance in the circuit. The dielectric constant (K^T) shows how easily the electricity can penetrate the material. It is defined as

$$K^T = \frac{C_{01\mathrm{K}}h}{\varepsilon_0 A} \tag{1.1}$$

where $C_{01\mathrm{K}}$ is the measured capacitance at 1 kHz, h is the distance between the electrodes (thickness of the piece), ε_0 is the relative permittivity of free space (8.854×10-12 F/m) and A is the area of the electrodes [25]. The lower the K^T value is, the harder the material is to break down when subjecting to intense electric fields. $\tan\delta$, on the other hand, describes the electrical loss of the material.

As an interface between the mechanical and electrical systems, a piece of piezoelectric material has an important parameter: coupling factor, which is denoted in tensor form as k_{ij}. Normally, i represents the direction of the electric field and j shows the mechanical vibration direction. The number assigned to each direction can be reviewed in Figure 1.1. It is an indicator of the efficiency with which a piece of piezoelectric material converts electrical energy into mechanical energy, or vice versa [23,25,27].

Piezoelectric charge constant (defined on mechanical strain) and piezoelectric voltage constant are denoted in tensor form as d_{ij} and g_{ij}, respectively. The charge constant shows the strain generated by the material when subjecting to a certain electrical field, which is an indicator of material's suitability for actuator applications. On the other hand, the voltage constant demonstrates the induced electrical displacement due to the mechanical stress applied to the material, which makes it an indicator of a material's suitability for sensing applications. Given the material's modulus of elasticity (at a constant electrical field) c_{ij}, the charge constant related to the strain d_{ij} can be transformed into charge constant related to stress denoted by e_{ij} following the equation [23,26],

$$e = dc \tag{1.2}$$

For a piece of piezoelectric material which is poled in its thickness direction, the charge constant can be expressed as (1.3),

$$d = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & d_{15} \\ 0 & 0 & 0 & 0 & d_{15} & 0 \\ d_{31} & d_{31} & d_{33} & 0 & 0 & 0 \end{bmatrix} \tag{1.3}$$

where d_{31}, d_{33}, and d_{15} are parameters commonly provided by the manufactures [26–28]. The voltage constant g_{ij} is defined with tensor form in the similar manner.

The quality factor of the piezoelectric material is also useful during the design. It shows the sharpness of the electromechanical response spectrum and is a good indicator of the bandwidth of the system. It can be calculated from the equivalent circuit (Figure 1.2) using (1.4) [23].

$$Q = \frac{1}{R_1}\sqrt{\frac{L_1}{C_1}} \tag{1.4}$$

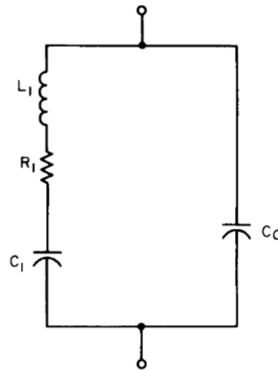


Figure 1.2: Equivalent circuit for piezoelectric materials [23].

A piezoelectric device with a higher quality factor has a higher frequency selectivity (smaller bandwidth) and lower mechanical loss. In the high power ultrasonic applications, a higher quality factor is preferable; meanwhile, for applications like energy harvesting in which broad bandwidth is a merit to the system, there is a trade-off between bandwidth and signal intensity [29–31].

The resonance frequency of an isolated mode of a piezoelectric material relates closely to the material's dimension. In the material properties given by the manufacturer, frequency-related property is usually defined as a frequency constant N (Hz·m) with indices showing the relevant direction in that vibration mode. The conventional definitions of the indices are: "1" for radial mode; "2" for length mode (plate); "3" for length mode (cylinder); "4" for thickness mode (plate/disc) and "5" for shear mode, and the definition of the dimensions are on diameter, length, length, thickness and thickness, respectively [25,27]. The resonance frequency (F) of the element in that particular mode can thus be calculated based on

$$F_i = \frac{N_i}{t_i} \tag{1.5}$$

where t is the associated dimension to that vibration mode.

Last but not the least, it is common to show material's Curie temperature in a data sheet. The material will lose its piezoelectric properties when operated in the temperature above that, which is a concern in high-temperature applications. In that situation, and materials with better thermostability, such as bismuth titanate (BT), should be considered [32,33].

Since there exists a military standard (MIL-STD-1376B Rev. B [34]) for the piezoelectric materials, no matter what names in the catalogue of a material provider are, there is always an equivalent in the standard to be compared to. For detailed information on different types of the piezoelectric materials, one can refer to the material type defined in the standard or directly from the manufacturer's catalogues. Nevertheless, the material properties for a piezoelectric material should contain mechanical, electrical, and electro-mechanical aspects. Piezoelectric materials of each kind have strengths in different aspects, and there is no material that can cover all the angles. As an example, the material properties between soft (Naval type II, V or VI) and hard (Naval type I, III) piezoelectric ceramics are presented in Table 1.1.

Table 1.1: Comparison between the soft and hard piezoelectric materials [27]

Characteristics	Soft Ceramic	Hard Ceramic
Piezoelectric Constants	larger	smaller
Permittivity	higher	lower
Dielectric Constants	larger	smaller
Dielectric Losses	higher	lower
Electromechanical Coupling Factors	larger	smaller
Electrical Resistance	very high	lower
Mechanical Quality Factors	low	high
Coercive Field	low	higher
Linearity	poor	better
Polarization / Depolarization	easier	more difficult

From Table 1.1, it can be inferred that the soft ceramics are generally good in receiver applications and the hard ceramics are preferable in power ultrasounds. Therefore, it is very case-dependent to choose a suitable material for a certain application.

1.3.2 Tactile Sensor and Vibro-tactile Sensor

A tactile sensor is a device that measures material information from the physical interaction with the object material. It may be useful for medical diagnostic applications, as pathological changes in the tissues, such as tumors, affect mechanical properties of the tissues. Malignant tissues are usually 5-20 times stiffer than normal ones [35], thus clinicians have used palpation [36,37] to feel the stiffness of tissues and determine the malignancy of them. While palpation is simple, it is just a qualitative assessment and the results are widely open to user interpretation. To imitate the diagnostic process in more objective and quantifiable manner, various types of tactile sensors have been developed. The efforts have mainly focused on integrating sensing mechanisms into the tactile probe to convert haptic responses from the object into digitizable signals such as current or voltage, and analyze them on computers using modern signal processing techniques to help accurate diagnosis [36,37].

The most common types of tactile sensors are force-based ones which measure the load associated with the displacement as a direct imitation of palpation. A typical setup for the force-based tactile sensor can be found in the work by Sangpradit et al. [38], They employed a robotic positioning mechanism to control the sensing position and compression depths, while forces were measured with a load cell. Combining the force and the displacement information, they were able to estimate the stiffness of inclusions inside a soft phantom. The sensing mechanism is straight-forward, and the raw data are easy to comprehend. However, it causes a severe local deformation on the surface of the object to acquire data, which makes the method inappropriate for deformation-sensitive practices such as neurosurgery. Besides, unlike the lab phantom, the geometries of biomedical objects, such as tissues and organs, are usually irregular and rough, which brings tremendous challenges to the precise displacement control. Furthermore, the raw data should be further processed to compensate for the probe geometry to derive the elastic modulus [39].

To address these challenges, various indirect measurement methods, which can induce minimal deformation in the objects, have been proposed. One of the promising solutions is to use mechanical vibrations. Vibro-tactile sensors utilize mechanical vibrations at their resonance for measurement [40]. In case of solid target medium, only minimal level of force needs to be applied to secure the contact with the object; hence, no excessive pressure on the target surfaces is required. One successful design of the vibro-tactile sensor for solids was developed in 1992 by S. Omata and Y. Terunuma (Figure 1.3) [41].

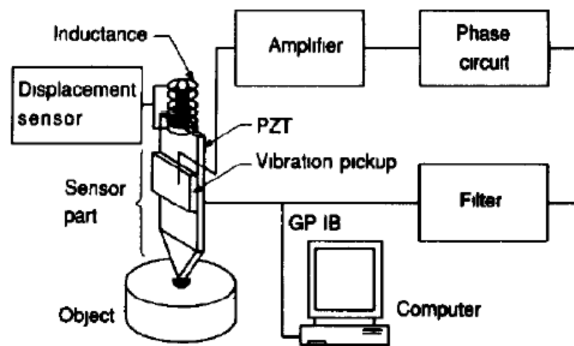
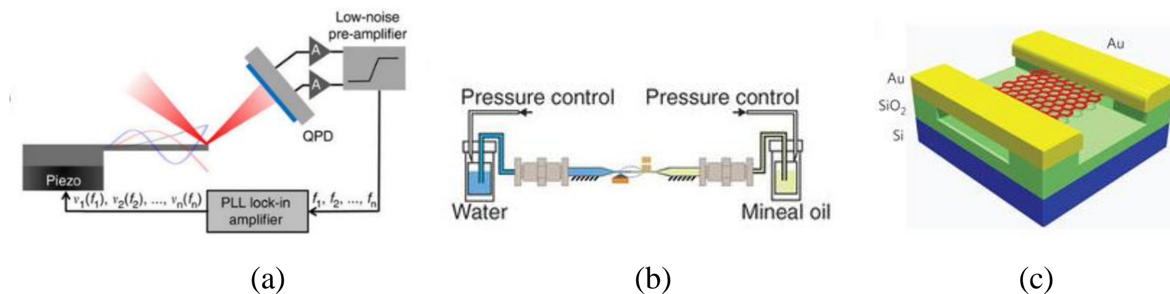


Figure 1.3: A vibro-tactile sensor developed by Omata and Terunuma [41].

The key components of the sensor are a piezoelectric transducer that generates vibration and a pickup transducer that senses the vibration signal. The resonance frequency is monitored with a circuit connecting to the computer. Under a constant contact force controlled by the spring deformation, frequency changes can be observed when the sensor head is applied to the objects with different stiffness. The shift in the resonance frequency was proposed as the measure of the mechanical property of the object. The test results on the gelatin samples revealed that the resonance frequency shift has a linear relationship with the shear modulus of the sample. Later, in 1995, the device showed the potential for applications in medicine, such as oedema measurement, by O.A Lindahl and S. Omata [42]. In the lab experiment on the silicone rubber phantoms and rat tissues, the device was capable of discriminating hardness of the object by resonance frequency shifts. The device was further improved for medical applications on human skins [2]. Afterward, in the past two decades, various types of vibro-tactile sensors have been developed and applied to silicone rubber phantoms, animal

tissue samples, and human tissue samples, in vivo or in vitro [3,4,43–46]. However, the primary principle of the device, adopting the mechanical resonance frequency shift as the indicator for material properties of an object, has remained the same.

There are other vibration sensors which operate like tactile sensors by exposing themselves to the mediums other than solids such as gas and liquid, where deformation data are not readily available. When the vibrating sensor end is immersed in the target medium, the change in boundary conditions due to mass loading affects sensor's vibration behavior. In 2003, A. Vidic et al. developed a cantilever vibration system for the identification of gas and liquid [5]. The resonance frequency changed because of the different mass loadings of the medium to which the cantilever was exposed. Similar concept can be found in the development of MEMS systems for nano-scale applications, where limitations in dimensions and requirement in sensitivity are extraordinary. Depending on the emphasis of the applications, the sensor can be manufactured into different shapes, such as microcantilever type (Figure 1.4(a)) [47], hollow tube type (Figure 1.4(b)) [48], or monolayer graphene type (Figure 1.4(c)) [49].



(a) (b) (c)

Figure 1.4: Examples of vibro-sensor designs in MEMS systems: (a) microcantilever type [47]; (b) hollow tube type [48]; (c) monolayer graphene type [49].

Note that the principle has been established regarding such sensors as a mechanical vibration system. Most of the researchers have analyzed the system from a pure mechanical perspective in the development of the vibro-tactile sensors [40,50–52]. The analytical analysis in [53] demonstrated that a linear relationship between Δf (the mechanical resonance frequency shift) and F (the contact force) concerning the material properties of the object (elastic modulus E and density ρ) could be established as $\Delta f \propto \rho E^{-1} F$. However,

when the frequency shift was measured as the indicator of the stiffness in actual experiments, the measured value was very small compared to the reference frequency. For example, the maximum frequency shift observed in [2] was less than 500 Hz, which is less than 1% of the working resonance frequency of the device (~ 61 kHz). As a result, the signal can be easily contaminated by noise. Therefore, there is a crucial need to improve the sensitivity of the device to estimate the stiffness of soft materials for critical applications. This has been partly addressed by manipulating the mechanical design of the sensor. For example, Y. Murayama and O.A. Lindahl [54] replaced the tactile part with a tapered glass needle to improve the sensitivity. Although not explicitly mentioned in [54], the glass needle functioned as an ultrasonic vibration concentrator, which increased the mechanical quality factor of the device, i.e., increase the conversion efficiency from electrical energy to mechanical energy. Therefore, when the sensor contacted the object, sensitivity increased by transmitting more energy. However, no theoretical derivation was presented for the design of such vibration concentrator.

1.3.3 Field-Programmable Gate Array

Field-programmable gate array (FPGA) is an integrated circuit that can be reconfigured after being manufactured. In 1984, FPGA was first introduced by Ross Freeman, a co-founder of Xilinx, with the name “Logic Cell Array” in pursuit of the market demands. Prior to mid-1980s, chip manufacturer from US dominated the market and most of the them only targeted the market where massively produced chip can make profit by selling in large quantities. But as the global competition became fierce since mid-1980s, especially with the rise of the Japanese semiconductor manufacturers, the US manufactures soon lost its technological advantage and had to share the market with other international companies. At the meantime, the market demand for application-specific circuits increased significantly. It fueled the idea of building a versatile chip which can be reprogrammed by the customer. This idea was eventually materialized as a technology known as “field-programmable gate array” which is gaining popularity over the years [55,56].

Basic elements within an FPGA are look-up tables (LUT), flip-flops (FF), wires, and input/output (I/O) blocks [13]. The LUT is basically a truth table that represents the output values based on different combinations of its input. The LUT can facilitate different digital logics. The results can be stored as "states" in registers, which are made up of FFs. Wires are used to connect the elements. The I/O blocks controls the data transfer between the FPGA and the peripheral circuits. Usually the I/O blocks are general-purpose input/output (GPIO) pins and pads. The elementary building block inside an FPGA is a configurable logic block (CLB). It is a combination of LUTs, FFs, and multiplexers. The structure of the CLB is defined by the FPGA provider. Currently, two big companies dominate the market. They are Xilinx, the inventor of the FPGA, and Intel which acquired Altera (the previous comparator of Xilinx) [57]. In Xilinx FPGAs, the elementary block is either referred to as CLB or Slice [58]; while in Intel FPGAs, it is called adaptive logic module (ALM) [59]. Combining CLB, wires, and I/O ports, the architecture of the FPGA can be established (Figure 1.5).

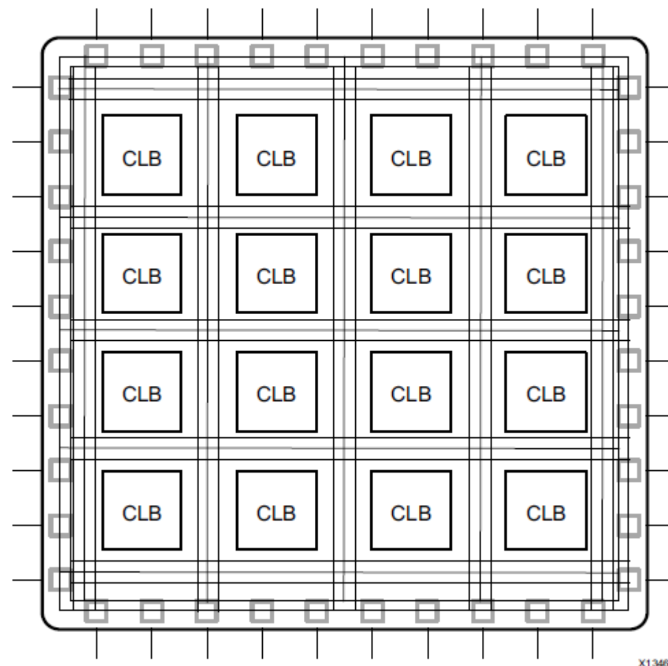


Figure 1.5: Basic FPGA architecture (CLB: configurable logic block) [13].

Programming an FPGA is a process to define interconnections between the logic blocks to fulfill specific circuit logic. Since the connections in the electrical circuits are basically “1” for conduct or “0” for open, the configuration for the FPGA interconnections is stored as a bitstream. Based on how the bitstream is applied to the FPGA, there are different kinds of FPGA fabric [60,61]:

1. SRAM-based FPGA

   The configuration data is stored in the static random-access memory (SRAM). The SRAM is volatile, meaning that it cannot hold data without power; therefore, this type of FPGA should be reprogrammed upon boot. The FPGA can be programmed either by reading the external memory chip (master mode) or fed with the programming bitstream (slave mode). In slave mode, the master device can be a processor, or other dedicated interface, such as a boundary scan device like JTAG.

2. SRAM-based FPGA with an internal flash memory

   Similar to the previous one, except that internal flash memory blocks are included in the FPGA fabric to store the data. Other than the advantage of preserving the program during power-off, the additional non-volatile memory can prevent unauthorized bitstream copying and thus increase the safety.

3. Flash-based FPGA

   The flash memory in SRAM based FPGA only functions for storing the boot-up configurations. But in the true flash-based FPGA, it uses flash as primary on-board resource. A true flash-based FPGA can “remember” the configuration even after reboot. It has the advantage of less power consumption and is more tolerant to radiation effects. Like the second FPGA fabric, it can also prevent unauthorized bitstream copying.

4. Antifuse-based FPGA

   Antifuses are opposite to the fuse. The antifuse does not conduct current initially, but it will allow the current flow after being burnt down. This process is permanent,

which means that this type of FPGA can be programmed only once after being manufactured.

An FPGA design is a synthesis of various functional circuits. Sometimes, the functions needed have already been developed and packaged as an application-specified integrated circuit (ASIC). For example, a SRAM chip for data storage. ASIC is an integrated circuit with its functionality defined and cannot be modified after being manufactured. Compared to FPGA, ASIC acts as a specialist who is the most suitable agent for a specified task rather than focusing on flexibility. The manufacturing of ASIC requires customers to pay for the mask tooling with an up-front non-recurring engineering (NRE) charge, but the successive cost in development is lower than that for FPGA [55]; Therefore, ASIC is usually preferred in producing massively produced ICs, while FPGA shines in lower production volume [55]. The flexibility of the FPGA is powerful in defining specific task where no other replacement IC can perform and eliminate the entry-barrier of customizing IC in terms of NRE cost and manufacturing difficulties. At the same time, the FPGA trades in the power-consumption efficiency and the maximum frequency of operation for its versatility. The efficiency of a temporary solution on FPGA may not be comparable to that of a well-developed ASIC. During the development of hardware, if an ASIC exists for the required function, it is neither necessary nor economical to configure FPGA to adopt that function with its basic building blocks. An FPGA can be configured into any digital circuit, however the analog functions, like power-amplifier or analog interfaces, are hard to be accommodated. To address these issues, in modern FPGA chips, it is common to integrate various ASICs into the fabric [13,61]. Figure 1.6 shows the architecture of a contemporary FPGA [13]. The embedded memories, phase-locked loop (PLL) clock generators, high-speed serial transceivers, off-chip memory controllers, and multiply-accumulate (MAC) blocks are additional ASICs to enhance the FPGA and allow it to function as a “processor”.

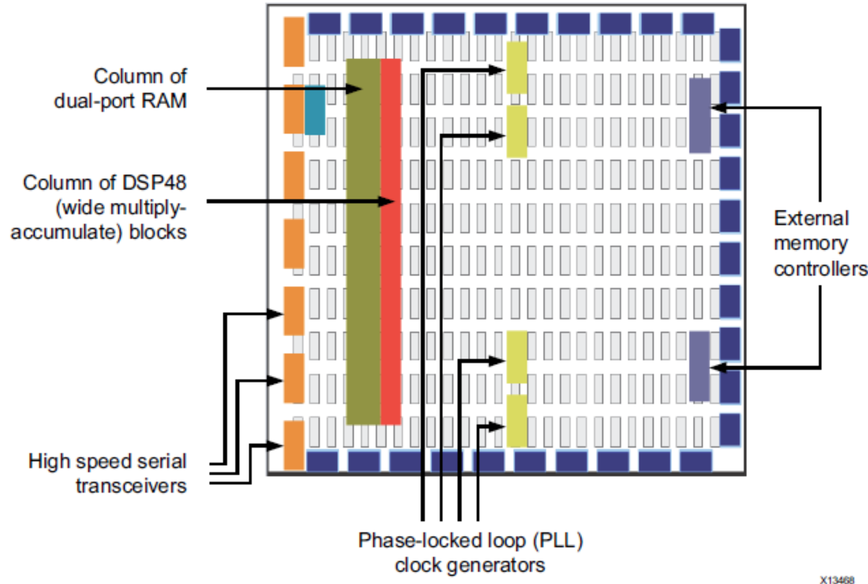


Figure 1.6: Contemporary FPGA Architecture [13].

In some FPGA fabric, even a hard-implemented processor chip is included. These types of FPGA are called SoC FPGA, where SoC stands for system on chip [62]. As inferred by its name, SoC is an IC which integrates a central processing unit (CPU), I/O ports, memory, and other microchips into the chip without the need of motherboard as in traditional computer system. The advantages of including a hard-embedded SoC in an FPGA is that it allows software to run on the FPGA-based system more efficiently. The inclusion of SoC also greatly facilitates the interactions between the chip and peripheral electronic components. The most used "hardened" processor in the chip is an ARM Cortex-A processor [62], which leverages the performance with optimal power consumption [63]. The ARM processor is a processing unit based on a modified reduced instruction set computer (RISC) architecture. It strips out unnecessary complex instructions supported by normal CPU and increase the efficiency of its operations by pipelining the single clock cycle command executions. The compact design for the supported instructions bring about smaller size, simpler design, and lower power consumption compared to the traditional but powerful CPUs. It is a superior solution to embedded system and thus popularized in many SoC development or mobile

platforms [64]. Figure 1.7 illustrates a typical design where ARM chip is the core of the embedded system to control various peripherals.

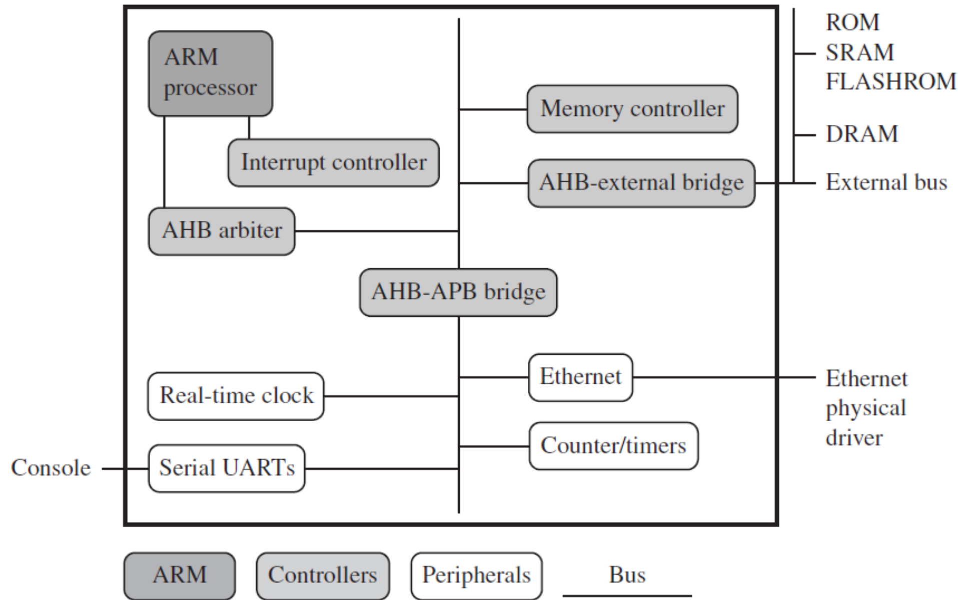
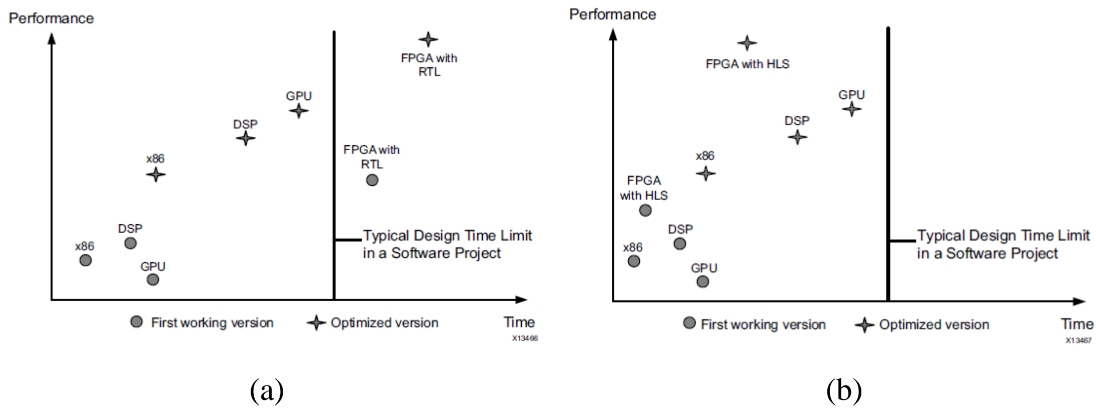


Figure 1.7: An example of an ARM-based embedded device [64].

Combining FPGA and the ARM chip, a complete solution for sensor platform can be built, and its functions can be reconfigured in the field.

Together with all the advantages provided by an FPGA, it brings about challenges in the actual development process. The programming model for the FPGA and normal processor is different. On FPGA, the algorithms or the logics are fulfilled by defining a suitable circuit, which means that the design should be defined in very low level. This increases the difficulty of a high-level algorithm implementation because the operations that can be defined in hardware are just transferring states in registers through wires. Therefore, the development difficulty results in a huge lag in the lead time of the project as shown in Figure 1.8(a). However, the performance of the final product may be superior once it is optimized properly because of the high efficiency of operations at hardware level.



(a) (b)

Figure 1.8: Development time and performance comparison for different computational platforms: FPGA development with (a) RTL entry; (b) with specific development tools [13].

To improve the efficiency in the development of hardware-based algorithm, Xilinx offered a development tool named High-Level Synthesis (HLS) in its development suite Vivado for all versions [13]. The HLS can synthesize the circuit logic defined by high-level language, such as C, and convert it into register-transfer level (RTL) designs. The overall development time can be shortened without compromises in the performance (Figure 1.8(b)). Intel also provides their installation of HLS in their development suite Quartus Prime, but only in the standard and pro versions which require a subscription fee. HLS is a useful tool for algorithm development but may not be necessary for elementary level functions. The development without HLS does not necessarily start from the very bottom level for RTL programming. High-level abstraction of a circuit can be coded with hardware description language (HDL). The most used HDLs are Verilog and VHDL [57]. Although HDL partially alleviated the workload in programming, the difficulty in realizing popular sequential software algorithms with HDL persists, due to the programming model difference mentioned previously.

The performance advantage of an FPGA illustrated in Figure 1.8 comes from synchronous operations of FPGA, which implies that multiple operations can be conducted in massive parallel at the same time. It is realized by referencing to clock signals. In FPGA, a clock signal is a square wave signal with typically 50% duty cycle given at a certain frequency. A logic block in FPGA will react to the rising or falling edge of its input clock signal. Similar to the RISC where "short" instructions are used to facilitate the pipelining, the logic blocks in

FPGA can pipeline the parallel processes because individual operation shall finish the state change in one clock cycle. Therefore, the speed of the process is based on the clock speed/frequency. A clock tree will be established in the FPGA to ensure the clock signal reach each component at the same time to help logics keep timing constraints. An example of a clock tree is shown in Figure 1.9.

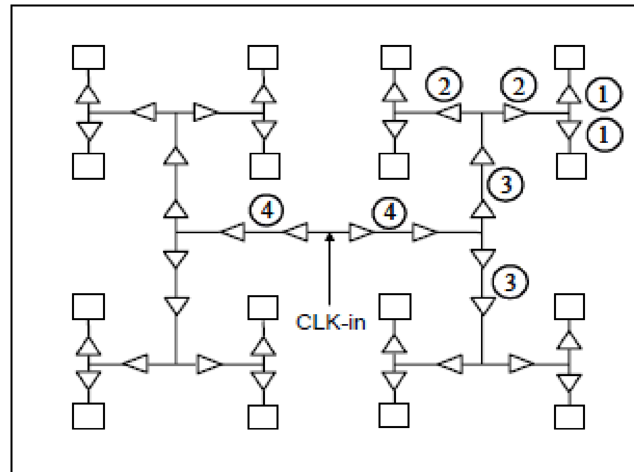


Figure 1.9: An H-tree clock distribution network; and the index of each level is indicated with the circled number [65].

For developers, the clock distribution is handled by the development suite during the program synthesis and routing. It is not uncommon to have modules in the circuit working at different clock speed; therefore, different stable clock source should be generated for these modules. The most used method is phase-locked loops (PLLs). Figure 1.10 shows the system diagram of the PLL.

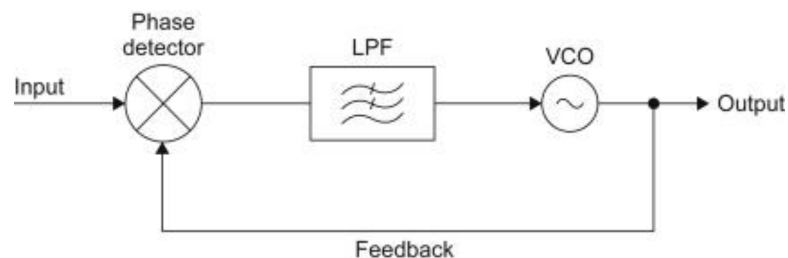


Figure 1.10: Phase-locked loop diagram [66].

The core of a PLL consists of three major components. They are a phase detector, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO). The crystal inside a VCO can oscillate at a very high frequency, and the applied voltage on the crystal can change the output frequency of the VCO. The input signal to the PLL is compared with the output from VCO to generate an error signal. The error signal is filtered by LPF and used by the VCO to optimize the voltage control on the oscillator until the desired frequency is achieved. Because the voltage adjustment is a control process, the convergence on the expected output frequency is not instantaneous. So, usually there is a signal derived from the PLL module to indicate whether the phase has been locked in. With modifications to PLL in Figure 1.10, frequency multiplier (higher frequency) or divider (lower frequency) can be implemented if a known reference frequency is given. The modified PLL circuit is called a PLL synthesizer. An example for a PLL synthesizer design is shown in Figure 1.11.

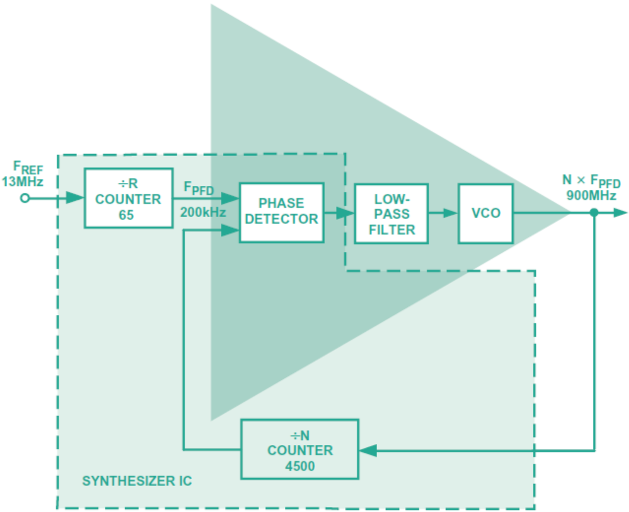


Figure 1.11: PLL synthesizer diagram [67].

From a PLL synthesizer, different output frequencies can be achieved. However, due to the nature of the divider, not all the requested frequency can be achieved exactly.

In summary, FPGA can use very high clock frequency to achieve fast processing speed thanks to the synchronous operation and massive parallel processing. It takes a different route to solve the problem compared to a typical asynchronous processor like CPU. The

development in FPGA demands more knowledge in electrical engineering than pure software development as it is hardware-based design. Alongside the challenges, the abundant I/O, reprogrammable feature, and evolving development suites facilitate the initial prototyping for mechatronics devices. The performance benefits and versatility can be good reasons to investigate the feasibility with FPGA and eventually come up with a prototype for the versatile ultrasound research platform.

1.3.4 Ultrasonic Transducers

Ultrasonic NDT uses high frequency sound waves for the detection of flaws inside the structure. The method, which proposed by Sokolovin in 1935 and later applied by Firestone in 1940, was soon developed to be a viable option for material testing [68] after World War II. Over the decades, the technology has been applied extensively across diverse areas. Many products have been commercialized worldwide, and they are based on a similar “pulse-echo” principle. The ultrasonic transducer converts high frequency electrical signals provided by a pulser into the mechanical pulse waves. The waves propagate through the test material until they meet a discontinuity in the material. It can be a defect within the material or very end of the material. A reflection wave is bounced back at the discontinuity and will be picked up by the same transducer. The transducer converts the reflected stress waves into electrical signals and a receiver circuit will capture them. A diagram illustrates the received signals can be acquired after signal processing (Figure 1.12).

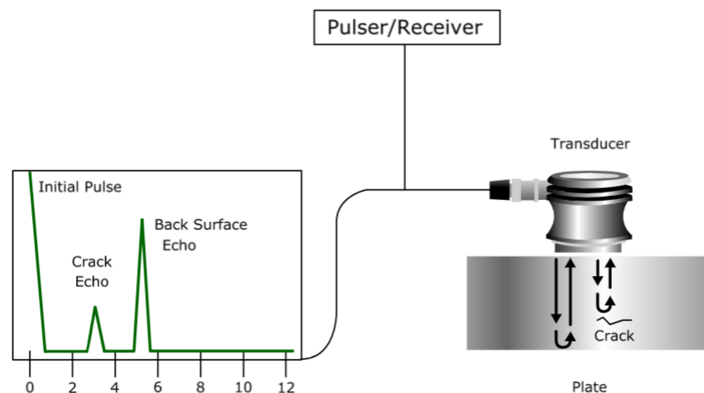


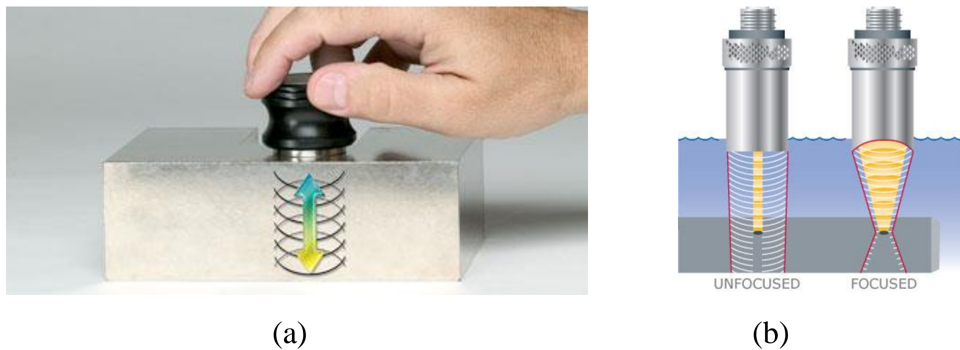
Figure 1.12: Diagram in ultrasonic NDT by pulse-echo sensing [69].

The depth of the crack within the material can be calculated based on the speed of sound in the material and the time delay between the incident and echo pulse. Similarly, the delay time of the back-surface echo can be utilized to calculate the thickness of the material.

The frequency in ultrasonic NDT determines the resolution in the measurement, because the wavelength of ultrasonic waves which propagate through a material can be calculated based on

$$\lambda = \frac{c}{f} \tag{1.6}$$

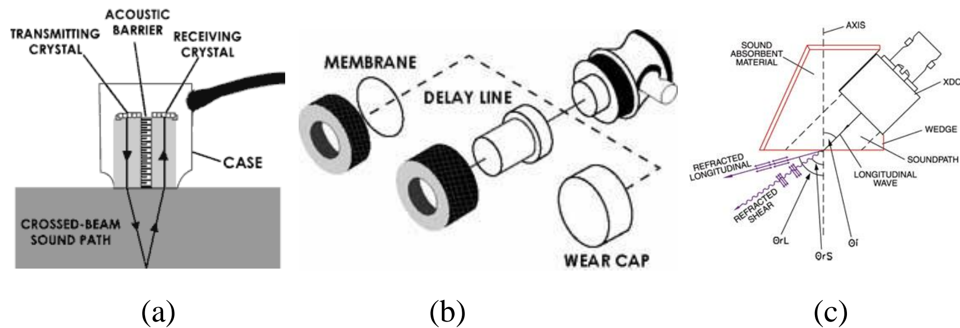
where c is the speed of sound in the material and f is the frequency of sound waves. The higher frequency the sound wave is, the better depth resolution in the test can achieve. The speed of sound can vary dramatically depending on the propagated material (Appendix A). The frequency range of a typical ultrasonic NDT device can be anywhere between 0.5 MHz and 25 MHz to achieve a mm-level wavelength [68]. However, the choice of the frequency is also a compromise on the penetration depths. Higher frequency provides better interpretation of smaller flaws inside the material but shorter penetration depth due to the severer energy attenuation [70]. As shown in Figure 1.12, an ultrasonic transducer is a probe which serves as the interface between the electrical signals and mechanical vibrations. Over the years, many transducers for ultrasonic pulse-echo testing have been developed. The transducers can be categorized into two major groups [71]: contact type and immersion type (Figure 1.13).



(a) (b)

Figure 1.13: Two groups of ultrasonic probes: (a) contact type [72]; (b) immersion type [73].

The contact type transducers make direct contact with the objects for flaw detection and thickness measurement. Based on the concept shown in Figure 1.13(a), contact type transducers can be further evolved into three variations for improved sensibility and compatibility to the applications: dual element transducers, delay line transducers, and angled beam transducers (Figure 1.14) [71].



(a) (b) (c)

Figure 1.14: Contact type ultrasonic transducers: (a) dual element transducer [71]; (b) delay line transducer [71]; (c) angled beam transducer [74].

A dual element transducer is composed of two independently operated elements inside. It is designed for applications in which the reflector is near the surface of the test specimen. For a single element transducer design, the “ring down effect” can jeopardize the measurement in thin material: When only one element is included in the design, it oversees both sending the pulse and receiving the echo. If the echo reaches the element before it stops sending the pulse (still ringing), the measurement cannot be fulfilled [71]. Besides, in the cases where the medium for the application is too lossy, if the intensity of the echo signal is less than the self-noise of the pulser, then a clean echo signal cannot be picked up [75]. Therefore, to address these problems, two pieces of piezoelectric material should be included in the system to take care of one of these two tasks individually. To ensure the echo signal being successfully picked up by the receiver piezoelectric element, the elements are angled towards each other as portrayed in Figure 1.14(a).

A delay line transducer includes a piece of additional “delay” material between the head and piezoelectric element. Two advantages can be provided by this design: 1) The time delay caused by the additional material can buy enough time for the piezoelectric element to finish

the ringing process and be ready to receive the echo, i.e., a different approach from the dual element design in eliminating the ring down effect to increase the accuracy of the measurement; 2) Materials with desired properties, such as heat isolation, corrosion resistance or increased durability, can be introduced into the system for the delay line part to increase the survivability of the device in extreme conditions. So, this type of transducer is widely used for precise thickness measurement or applications requiring thermal isolations [33,71]. The disadvantage of including a delay line is that it increases the energy loss of the system and requires more effort in designing.

An angle-beam transducer includes a wedge (red block in Figure 1.14(c)) in its design. Since the refraction of the sound wave is material dependent, the usage of the transducer is very case specific, i.e., it is accurate only for a particular type of material (usually steel) [71]. The angled sound wave can find perpendicular cracks inside the material. The angles of refraction shown in Figure 1.14(c) follow the Snell's law [76],

$$\frac{\sin(\theta_1)}{\sin(\theta_2)} = \frac{V_1}{V_2} \tag{1.7}$$

where θ_1 is the incident angle in first material, θ_2 is the refracted angle in second material, V_1 is the speed of sound in first material, and V_2 is the speed of sound in second material. Furthermore, the typical design of the angle-beam transducer utilizes the mode conversion to convert the longitudinal waves into the shear waves at an angle of 30, 45, 60 or 70 degrees [77]. As the angle between the longitudinal wave and the surface (normal vector) increases, more proportion of the wave being converted into shear wave [76]. Besides the usual parts of a contact sensor, the wedge can be made of special materials; hence, it is possible to use materials with better durability than other parts for the design to improve the endurance and extend the applications.

Despite all the improvement mentioned in the contact type transducers' development, the wave propagation in different mediums is an inherent problem in ultrasonic NDT. To ensure the conductivity of the sound waves, it is necessary to apply ultrasonic couplants (for example, coupling gel) between the transducer and the object, because the air gap between

the transducer and the test object can result in attenuation of sound waves due to the severe acoustic impedance mismatch [78]. The coupling problem can be addressed otherwise with immersion sensors (Figure 1.13(b)). They are used to conduct tests in immersed condition when applicable. Because the object and part of the sensor are immersed in a pre-defined medium such as water [79–81] or oil [82,83], the wave propagation is much more predictable than that in the air with couplant. The elimination of the uncertainty in the medium change and the avoidance of contact problems grant immersion NDT the following advantages [84]:

1. The coupling between the sensor and the test specimen is uniform.
2. The process can be automated when robotic system is added.
3. It is easier to customize a different output shape (usually a curvature like a focusing lens with user-defined focal point) than contact type.

However, since the transducer is immersed (entirely or partially depending on different design) inside liquid, it brings more concerns to the design competence, like waterproofing and corrosion resistance. For example, as indicated by OLYMPUS, one of major transducer manufacturers, their immersion sensors are not supposed to be submerged for periods exceeding 8 hours and need be dried out when put out of the service to ensure the life span of the unit. The immersion also set limitations on the test specimen since not all of them can be tested inside a liquid. Although, methods like using sealed vacuum bag to cover the object were proposed to help solve this problem [85], it invites additional burdens to operations.

A typical design of an ultrasonic transducer is shown in Figure 1.15. As the core of the electro-mechanical transducer, the active element is made of piezoelectric materials. It can be a single element or an array of elements. Small element has a better compatibility to the curved shape than the large elements, but the scanning speed should be lower since it covers less surface area than the big element [86]. The electrodes were applied to both sides of the active element to supply the AC electrical signals.

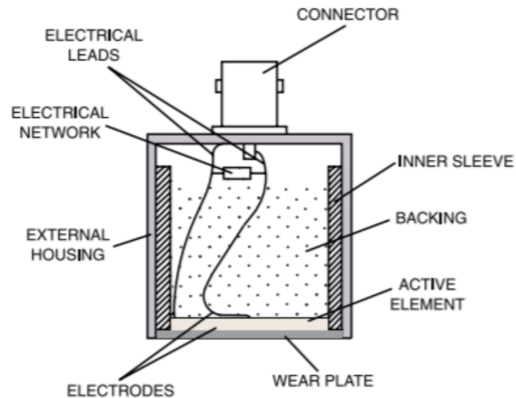


Figure 1.15: Typical design of an ultrasonic transducer [84].

Wiring and manufacturing become difficult problems when the frequency of the design is high because the dimension of piezoelectric elements is inversely proportional to the resonance frequency [27]. If phased-array technique is considered, the design criteria can be even stricter, because [87]:

1. Each element should be driven individually and independently without inducing vibration in its nearby elements by the mechanical or electrical coupling.
2. Properties of each element should be identical so that homogeneous beams can be formed.

Fortunately, both the invention of 1-3 composite (Figure 1.16) in late 1970s [88] and the dice and fill technique, which is useful in controlling a uniform characteristics among all elements [89–91], contributed to the manufacturing of piezoelectric elements capable of phased-array scanning in their thickness vibrations.

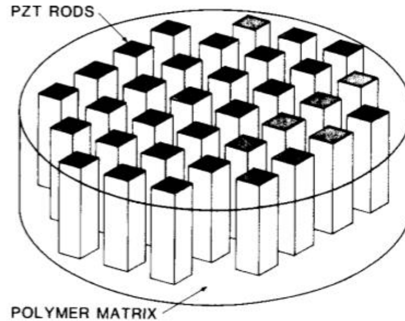


Figure 1.16: Schematic of a 1-3 composite made from PZT rods in a polymer matrix [92] (“1-3” defines the connectivity of the material).

The wear plate makes direct contact to the surface of the object through couplants in a contact sensor, or it makes contact to the coupling liquid in an immersion sensor. In either case, the concern of impedance matching regulates the thickness of it. In normal design, a $\lambda/4$ design for the matching layer is adopted [93,94]. The design brings about challenges in manufacturing. Based on the wavelength calculated with (1.6), the matching layer thickness should be controlled with um accuracy if a transducer is to be matched with common metallic materials such as steel or aluminum.

To ensure the accuracy of the measurement, a backing layer needs to be included to absorb (damp out) the vibration energy to avoid unnecessary reflection of the sound waves inside the transducer. In the meantime, the backing layer also secures the wiring and add some rigidity to the sensor. Usually, composites or other materials with heavy acoustic damping are used for the backing layer [95–97].

1.3.5 Ultrasonic Systems

Ultrasonic transducers are merely agents to interact with the samples. The driving system for the transducers is equally important. A typical composition of an ultrasonic system can be presented with a block diagram in Figure 1.17. It can be divided into three major parts: the peripherals dealing with analog signals, a pure digital part for signal acquisition and processing, and an analog front end (AFE) which interfaces the previous two parts. Based on the transducer type (single-element or phased-array), the AFE may be configured differently.

The major difference is due to the channel counts and the timing requirement in sending out the pulses. The multiplexer for directing and receiving signals in the phased-array testing requires a very accurate timing for the concept to work. Then, a beamformer which can coordinate multiple channels is necessary.

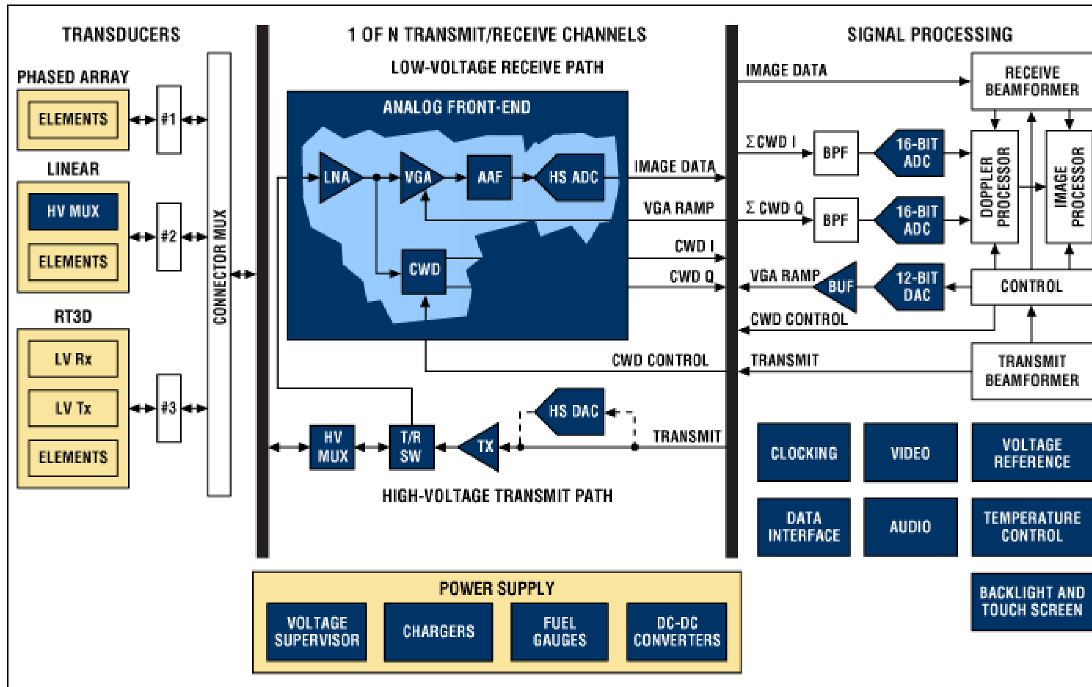


Figure 1.17: Functional block diagram of an ultrasound imaging system [98].

Beamforming can be done with analog circuits (Figure 1.18(a)) or digital circuits (Figure 1.18(b)). Because of the advantages in performance and flexibility, the latter one is gaining popularity, although it takes multiple high-speed digital components to realize [99]. With the continuous development in flexible ICs such as FPGA and the cost reduction in massively produced ASICs like ADC and FIFO, the digital beamformers are now dominating.

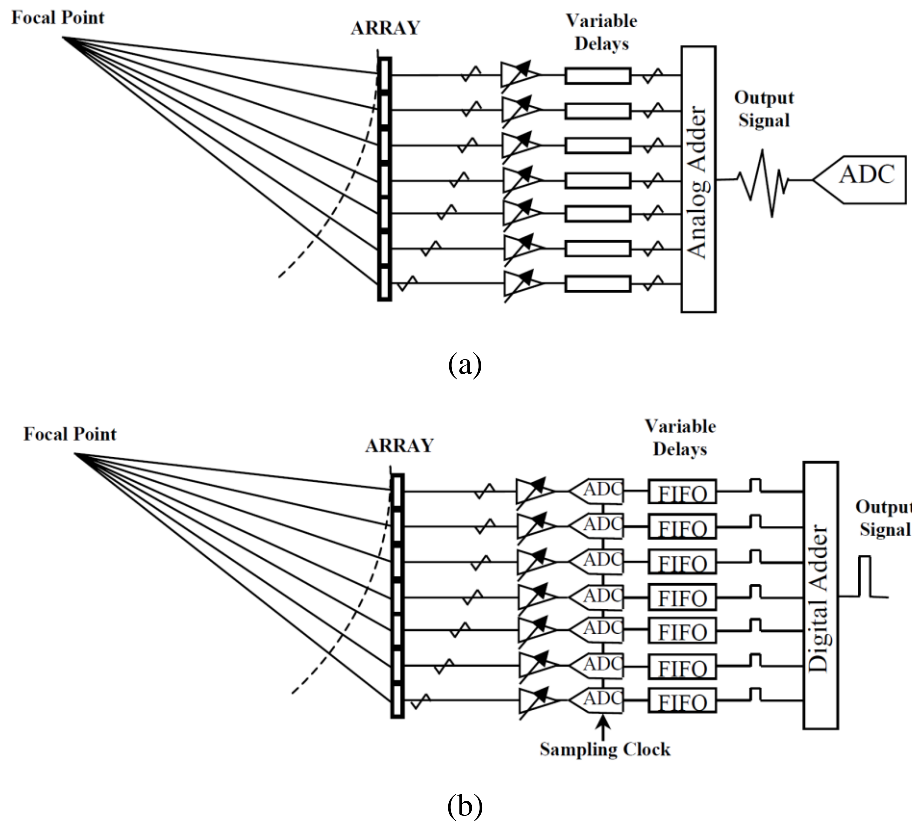


Figure 1.18: Beamforming in (a) analog; (b) digital [99,100].

Note that multiple channels are needed to drive and listen to the elements in the array as demonstrated in Figure 1.18. Moreover, these electrical circuits after the analog-to-digital converters (ADCs) are pure digital circuits. The multichannel and flexibility requirement of the ultrasonic imaging system, especially the beamformer component, can be addressed very well by an FPGA. It is not surprising that many researchers have decided to use FPGA to develop the ultrasonic imaging system. Some examples can be found in [101–105], although the flexibility of FPGA is mainly utilized to apply the digital delay line, which makes the FPGA a beamformer specialist. The high-level signal processing was still done with upper machine. In 2013, S. Gilliland et al. [106] investigated the performance of using hard-embedded SoC chip inside the FPGA fabric for signal processing in ultrasonic imaging. Their study showed that the embedded system performance was better than the conventional hardware-software co-design, which demonstrated the great potential of the embedded

processing. However, as mentioned in Section 1.3.3, it takes time for professionals to perform RTL programming in FPGA. It is not easy to perform a pure hardware processing to replace the prevailing software algorithms. Therefore, with all the system developed in the past, very few of them decided to address the signal processing in hardware directly [107,108], and they took place quite recently (after 2015). It is worth noting that the improvement of the development tool really contributed to the successful implementation of the algorithm in hardware. One recent paper [12] addressing the signal processing for ultrasonic imaging not only demonstrated the possibility of a pure hardware processing, but also showed the importance of a user-friendly development environment. It should also be pointed out that a continuous effort in familiarizing the hardware development is also necessary as the first author of [12] has been developing the FPGA systems for years. With the current development tools available for FPGA, which has been improved over the years, the establishment of a prototype for ultrasonic system in FPGA can be achievable for the ones who are even not familiar with the hardware. However, the new developer should focus more on the possibility of evolving the system to better use the powerful hardware potential. To this end, the first prototype with function-wise realization was developed in this research.

1.3.6 State-of-art Commercial Ultrasonic Systems

The commercial ultrasonic systems for industrial inspections can be found from many sources. One of famous suppliers is OLYMPUS (Tokyo, Japan). The OmniScan series is one of the products in their NDT flaw detection solutions. It supports ultrasonic testing functions like pulse-echo (UT) sensing and phased-array (PA) inspections. It is a complete phased array toolbox (W:335 mm, H:221 mm, D:151 mm, 5.7 kg) and has a 1280x768 display to allow data viewing on-site. The outfit of the device is shown in Figure 1.19.

Figure 1.19: OmniScanX3 from Olympus [109].

The device supports up to 25 GB storage space. It can digitize signals with a sampling frequency up to 100 MHz with 16-bit accuracy. Maximum voltage output is 115V for PA channels and 295 V for UT channels. The best model can support 32 elements as pulsing aperture and 128 elements for receiving. The data can be reviewed with the display on-board or use the software provided by OLYMPUS to perform defined signal processing [109]. Users need to be educated before properly using the system. The mobile version of the OmniScan is MX series, and the representitive model is OmniScan MX2. Compared to the X version, it is smaller (W:325mm, H:235mm, D:130mm) and lighter (3.2 kg). It chops down the system with slightly inferior display, battery, storage, and less I/O ports. The PA testing function is not as good as that in X series because less focal laws are supported. There are some limitations in choosing aperture and receiving channel combination for the product. The price is not directly available in the website, but a refurbished Omniscan MX2 32/128 in second-hand market usually ask for ~$30,000 to $40,000 USD before tax (Feb. 2020).

An alternative for these expansive OLYMPUS devices can be found from the product line by SIUI (Shantou, China). The system is called SyncScan [110]. A representative model is SyncScan 2. The product basically resembles OLYMPUS OmniScan. Despite the same number of channels supported, almost all other specifications are less competitive. It is worth noting that the resolution for ADC is 12 bits, but it has a higher sampling rate (170 MHz) in UT testing. The price for SyncScan also varies based on configurations details of the model. The one in our lab (Figure 1.20) purchased in 2017 is a compact version of SyncScan 1

which supports only dual channel UT testing and a 16-channel PA measurement. It was included in a ~5000 CAD bundle alongside a 16-channel PA transducer. As for the data communication, like the products from OLYMPUS, it only supports the online monitoring through the on-board display or through customized-software-based data interpret package. The raw RF data is not accessible in commercial version.

Figure 1.20: SyncScan 1 from SIUI.

In the area of research ultrasound platforms, most famous supplier is Verasonics (Seattle, USA). Verasonics was founded in 2001 by a team of scientists, engineers and technical staff who are ultrasonic experts. They provide standalone solutions for ultrasonic research platforms [111]. VANTAGE™ (Figure 1.21) is their state-of-art research platform which not only provides customized-software-based data intepretation, but also grants access to the raw ultrasound data from each channel in real time. It supports multi-channel and beamforming techniques with customized transducer array. The supported output frequency is up to 50 MHz. The sampling rate of ADCs is 62.5 MHz with 14-bit resolution. Pulser voltage can reach up to 190V. The single channel power can rise up to 100 Watts peak and 8 Watts on average (for 50 Ohms).

The system is designed and released for researchers who want to carry out research in software environment to improve the ultrasonic signal processing techniques. A MATLAB scripting environment is provided to cater to those who are familiar with it and line up with the existing training in the education institutions [10]. The performance and convenience

come with a cost. From an Advanced Contract Award Notice (ACAN 16-024-CW) found online [112], the price for Verasonics Vantage 64 LE was roughly over 100,000 CAD before tax in 2016 for the standalone unit without any accessories.

Figure 1.21: Verasonics VANTAGE research ultrasound system [10].

1.4 Problem Statement and Research Scope

1.4.1 Ultrasonic Vibro-tactile Sensor

Based on the literature review on the vibro-tactile sensors, it is certain that those sensors have great potentials as tools in various fields to help differentiate the mechanical properties of the object with minimal contact force. Since the emphasis of such devices has been switched to MEMS system with the growing interest in nanotechnology, the research on the refinement of the structure in meso-scale is less popular. Considering there are still demands in measuring the soft material properties in-vivo with non-destructive methods, such as measurement of the mechanical properties of the hydrogels and biomedical tissues [113], it is still valuable to investigate the possibility of applying deliberate refinement to the device's structure in pursuit of improving its detection accuracy so that the method can be applied in-vivo without making testing specimens, and fill the gap in the current meso-scale measurement techniques.

Furthermore, it is worth noting that most of the vibro-tactile sensors which are driven by piezoelectric elements should have both mechanical and electrical aspects; therefore, such

devices can be studied mechanically via direct amplitude measurement followed by spectrum analysis, or electrically by analyzing its electrical characteristics [29]. For the latter, it is common to convert the mechanical structure into electrical circuits following the electro-mechanical analogies to facilitate the analyses using well-established electrical principles [29,114], [115]. Current investigations on vibro-tactile devices rely on the mechanical vibration responses extensively, but seldom pay attention to the electrical readouts of the system. The overlook on the electrical readouts also resulted in a design requiring an additional vibration pick-up to acquire the mechanical response [41]. Some researchers observed the electrical responses, but they did not recognize the value of processing electrical signals in electrical analysis to relate back to the mechanical properties. Therefore, the proposed research will attempt to establish the relationships between electrical and mechanical parameters and search for electrical parameters that reflect the mechanical properties. So, based on the similar principle to [41], a vibro-tactile sensor resonating in the ultrasonic regime but with one piezoelectric material only to provide vibration source will be developed with the following specific objectives:

1. Make a working prototype and provide design scheme for ultrasonic vibration concentrator which can be used with generic ultrasonic Langevin transducer
2. Establish new object evaluation parameters instead of the conventional mechanical frequency shift
3. Elucidate the limitations (measurement range, resolution, reliability) of the sensor.

1.4.2 Field-programmable Ultrasonic System

Based on the literature review, transducer manufacturing requires special facilities to accurately control the process to reach the sub-micron level precision demanded for a working design. With resources available in this project, it is not possible to include the design and manufacturing of the transducer into the research scope. Therefore, the commercially available ultrasonic transducers were purchased from SIUI (Shantou, China) for the NDT system.

As for the system integration, existing systems have limitations. The industrial ultrasonic systems are trustworthy inspection tools for trained specialists but not suitable for research. The system modifications may be possible by the manufacturer, but it is very costly and not flexible. As for the commercial research platform, the price is a huge barrier for most researchers. Moreover, the research platform is good in hardware performance, but it is impossible to bring the expansive and bulky system on-site (like factories) for experiment. The system design for the ultrasonic integrated automation should be more portable and versatile. Furthermore, the ultrasonic research platform is more focused on providing data ports for users to access the data and supporting APIs for software development [10]. It can help research in pursuit for a better processing algorithm, but it contributes little to the automation integration. However, software algorithms will be bottlenecked by the limitations in hardware eventually. The current commercially available setups become very limited if the algorithm is to be improved in a hardware realization. Due to the different programming models, the same algorithm may be implemented in the software and hardware environment in different approach. Therefore, a new platform to support all these requirements should be developed.

The advancement in FPGA technology opened the gate for hardware algorithms, which can be more efficient compared to the software realization. The SoC FPGA provides additional versatility to the hardware integration. The proposed FPGA system by others did not show details in development, and they used FPGA mostly as a multiplexer instead of a processor. Therefore, the development of a new research platform focus on the potential in the processing with FPGA is the first step toward the automation of in-line NDT. The following objectives are set for the project:

1. Develop a prototype with FPGA which can conduct ultrasonic testing
2. Develop analog circuits which interface with the commercial ultrasonic transducers
3. Develop digital circuits with FPGA to perform data acquisition and on-board processing
4. Provide technical design references to the lab for future use

Chapter 2
Models and Methods

2.1 Electro-Mechanical Analogy

Electro-mechanical analogies are frequently used to analyze the characteristics of mechanical system by establishing the relationship between the mechanical system and electrical networks. The key aspect of applying the analogy is, instead of dealing with difficult differential equations in mechanical analysis (e.g. (2.1)), working with the symbolic representations in electrical analysis to take advantage of well-established electric circuit theories [116].

$$F = M\frac{d^2x}{dt^2} + C_m\frac{dx}{dt} + K_m x \tag{2.1}$$

Two types of analogies are widely used: impedance analogy and mobility analogy. In the impedance analogy, force (effort) and velocity (flow) are regarded equivalent to voltage and current respectively, which is an intuitive way to convert the system to a different representation. Impedance analogy maintains the analogy between the electrical and mechanical impedance, although it fails to preserve the topology of the system. The resemblance between the mechanical components and the electrical ones can be express in (2.2) – (2.4),

$$F = C_m u \Leftrightarrow v = Ri \tag{2.2}$$

$$F = M\frac{du}{dt} \Leftrightarrow v = L\frac{di}{dt} \tag{2.3}$$

$$F = K_m \int u dt \Leftrightarrow v = C\int i dt \tag{2.4}$$

where mechanical notations F, u, $\mathrm{C_m}$, M and K_m are force, velocity, viscous damping coefficient, mass and spring constant, respectively; and electrical notations v, i, R, L and C are voltage, current, resistance, inductance and capacitance, respectively. On the other hand, in the mobility analogy, the analogies are force vs. current and velocity vs. voltage, which

eventually lead to the change of the resemblance relations from (2.2) – (2.4) to (2.5) – (2.7), where the notations have the same meanings as previous.

$$F = C_m u \Leftrightarrow i = \frac{1}{R} v \tag{2.5}$$

$$F = M \frac{du}{dt} \Leftrightarrow i = C \frac{dv}{dt} \tag{2.6}$$

$$u = \frac{1}{K_m} \frac{dF}{dt} \Leftrightarrow v = L \frac{di}{dt} \tag{2.7}$$

The topology of the system remains intact at the cost of losing the analogy between the electrical and mechanical impedance, because the force equilibrium is the connection between the boundaries of the mechanical components.

Adopting either the impedance analogy or mobility analogy depends on the system being analyzed. The impedance analogy is commonly used in filter modelling to determine the frequency selectivity from the system model for various purposes, such as noise predictions [117] and electro-mechanical filter design [118]. Impedance analogy is a common choice for the mechanical filter design [116], because the important design features, like the amplification ratios, can be observed easily in the transmission line models. Meanwhile, in the design phase, the structure of the mechanical filter is usually predetermined; hence, the topology is not a major concern. Therefore, it is advantageous to keep impedance analogy between the mechanical and electrical models, as the resonance problem can be solved by finding the minimum impedance. The mobility analogy is suitable for describing the vibration source characteristics and its coupling to the dynamic load [119], like in [29]. The mobility analogy is also preferred in the analysis in this project because the additional load can be modelled mathematically as an RCL circuit connecting to the original mechanical circuit branch in series, which provides the possibility to distinguish the load components from the sensor model when measuring the response in an electrical manner, i.e., through the impedance analysis from the electrical ports of the electro-mechanical system.

2.1.1 Impedance Analogy in Design

Table 2.1 gives a list of the important notations that are used in the derivation for the impedance analogy established between the electrical circuits and mechanical filter. The adopted analogy for this research is between an arbitrary-diameter cylinder (Figure 2.1) and a two-port electrical transmission line model (Figure 2.2).

Table 2.1: Basic notations for the analytical model

Notation	Meanings
E	Young's Modulus
ρ	Density
$\xi = \xi(x)$	Displacement of the cross section along the axis
$\dot{\xi} = \frac{\partial \xi}{\partial t} = j\omega\xi$	Particle velocity
$\sigma = \sigma(x) = E \cdot \frac{\partial \xi}{\partial x}$	Stress on the cross section along the axis
$S = S(x)$	Cross-sectional area along the axis
$k = \frac{\omega}{c}$	Wave number, where $c = \sqrt{\frac{E}{\rho}}$ is longitudinal wave speed in solid

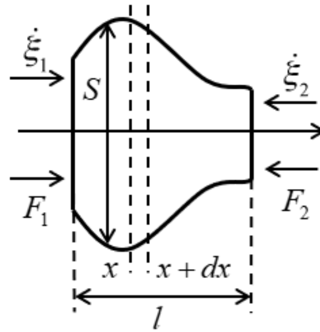


Figure 2.1: Cylindrical rod with varied diameter with boundary conditions applied.

Based on the schematic shown in Figure 2.1, the following equation can be derived from the force equilibrium (see Appendix B),

$$\frac{\partial^2 \xi}{\partial x^2} + \frac{1}{S}\frac{\partial S}{\partial x}\frac{\partial \xi}{\partial x} + k^2 \xi = 0 \tag{2.8}$$

By letting $K^2 = k^2 - \frac{1}{\sqrt{S}}\frac{\partial^2 \sqrt{S}}{\partial x^2}$ and $y = \sqrt{S}\xi$, (2.8) can be rewritten as (see Appendix C)

$$\frac{\partial^2 y}{\partial x^2} + K^2 y = 0 \tag{2.9}$$

In order to get the harmonic solution, $K^2 > 0$ is required [120]. Some discussions on this inequality is provided in Appendix D. Solving (2.9) gives displacement distribution along the axis as

$$y = A \sin Kx + B \cos Kx \Rightarrow \xi = \frac{1}{\sqrt{S}}(A \sin Kx + B \cos Kx) \tag{2.10}$$

where A and B are determined by the boundary conditions. Note that the complete form of the solution to the wave equation should have the time-dependent terms as

$$\xi(x,t) = (A \cos Kx + B \sin Kx) \cdot (A' \cos \omega t + B' \sin \omega t) \tag{2.11}$$

where A' and B' are determined by the initial conditions. As for the analysis on a general case of the harmonic vibration, the following form is used

$$\xi(x,t) = (A \cos Kx + B \sin Kx)e^{jwt} \tag{2.12}$$

Applying boundary conditions $\begin{cases} x = 0 & \dot{\xi} = \dot{\xi}_1 & S = S_1 \\ x = l & \dot{\xi} = -\dot{\xi}_2 & S = S_2 \end{cases}$ to (2.12), constants can be solved as

$$\begin{cases} A = -\dfrac{\sqrt{S_2}\dot{\xi}_2 + \sqrt{S_1}\dot{\xi}_1 \cos Kl}{j\omega \sin Kl} \\ B = \dfrac{\sqrt{S_1}\dot{\xi}_1}{j\omega} \end{cases} \tag{2.13}$$

Force equilibrium gives us

$$F = -S\sigma = -SE\epsilon = -SE\frac{\partial \xi}{\partial x} \tag{2.14}$$

The partial derivative in (2.15) can be found by taking partial derivative of (2.10) with respect to x,

$$\frac{\partial \xi}{\partial x} = -\frac{1}{2S\sqrt{S}}\frac{\partial S}{\partial x}(A\sin Kx + B\cos Kx) + \frac{K}{\sqrt{S}}(A\sin Kx - B\cos Kx) \tag{2.15}$$

Applying the boundary conditions $\begin{cases} x = 0 & F = -F_1 & S = S_1 \\ x = l & F = -F_2 & S = S_2 \end{cases}$ and (2.13) to (2.15), the following equations can be derived (Appendix E).

$$\begin{cases} F_1 = \dfrac{\rho c}{2jk}\left(\dfrac{\partial S}{\partial x}\right)_{x=0}\dot{\xi}_1 + \dfrac{\rho c K S_1}{jk}\cot Kl\,\dot{\xi}_1 + \dfrac{\rho c K\sqrt{S_1 S_2}}{jk\sin Kl}\dot{\xi}_2 \\ F_2 = -\dfrac{\rho c}{2jk}\left(\dfrac{\partial S}{\partial x}\right)_{x=l}\dot{\xi}_2 + \dfrac{\rho c K S_2}{jk}\cot Kl\,\dot{\xi}_2 + \dfrac{\rho c K\sqrt{S_1 S_2}}{jk\sin Kl}\dot{\xi}_1 \end{cases} \tag{2.16}$$

In impedance analogy, force is equivalent to voltage and velocity is equivalent to current. Then, a T-network can be established as the circuit shown in Figure 2.2.

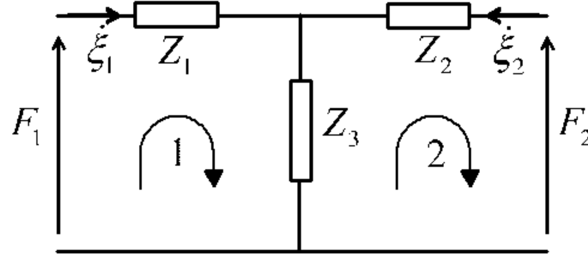


Figure 2.2: T-network equivalent circuit with mechanical boundary conditions applied.

Applying Kirchhoff's voltage law (KVL) on mesh 1,

$$F_1 = \dot{\xi}_1 Z_1 + (\dot{\xi}_1 + \dot{\xi}_2)Z_3 = (Z_1 + Z_3)\dot{\xi}_1 + Z_3\dot{\xi}_2 \tag{2.17}$$

Applying KVL on mesh 2,

$$F_2 = \dot{\xi}_2 Z_2 + (\dot{\xi}_1 + \dot{\xi}_2)Z_3 = (Z_2 + Z_3)\dot{\xi}_2 + Z_3\dot{\xi}_1 \tag{2.18}$$

Comparing these equations to (2.16), the impedances can be found as

$$
\begin{cases}
Z_1 = \frac{\rho c}{2jk}\left(\frac{\partial S}{\partial x}\right)_{x=0} + \frac{\rho c K S_1}{jk}\cot Kl - \frac{\rho c K\sqrt{S_1 S_2}}{jk\sin Kl} \\
Z_2 = -\frac{\rho c}{2jk}\left(\frac{\partial S}{\partial x}\right)_{x=l} + \frac{\rho c K S_2}{jk}\cot Kl - \frac{\rho c K\sqrt{S_1 S_2}}{jk\sin Kl} \\
Z_3 = \frac{\rho c K\sqrt{S_1 S_2}}{jk\sin Kl}
\end{cases}
\tag{2.19}
$$

This concludes the impedance analogy between the mechanical cylinder (Figure 2.1) and equivalent electrical circuit network (Figure 2.2) [116,121,122].

A typical mechanical design problem using impedance analogy is the design of an ultrasonic vibration concentrator (also referred to as ultrasonic horn; a type of the mechanical filter that can focus the vibration and increase the amplitude of the input vibration at its output end). In the design process, the shape function S and the radius R at both ends should be defined. Based on the properties from the selected material and the desired operating frequency, the only parameter to be solved is the length l. The analytical solutions for these equations are extremely hard to derive, but they can be solved by numerical methods. Since more than one basic shape can be integrated into the design, precise analytical derivation is very challenging [116,121,122]. Hence, a hybrid design approach can be adopted for such requirement to facilitate the design process, i.e. first extract initial guesses from a simplified analytical model and then refine the parameters through iterative processes with the aid of FEA models.

As for the modeling of a piezoelectric component, due to the nature of mechanical and electrical coupling, more parameters are involved. Usually, it is sufficient to have stress T and strain S to illustrate the mechanical properties, and electric field density E and displacement D to describe the electrical ones. The coupling can be described with equations formed by these parameters and coefficients or constants that relate them [123]. Appendix F provides the information on the relations among the piezoelectric parameters and some detailed explanations and definitions for each coefficient tensor [124]. Two different types of electrical boundary conditions (i.e. short-circuit and open circuit) along with two different types of mechanical boundary conditions (i.e. stress-free and clamped) result in four sets of

piezoelectric equations describing the material properties (Table 2.2 [124]). The indices indicate the direction of the parameter (Figure 1.1). The equations are equivalent since the coefficients are mutually derivable. Although it is preferred to apply the most "convenient" one to solve the problem, it may not always be practical. Sometimes, there is no direct measurement method for a certain parameter due to limitations in material testing.

Table 2.2: Piezoelectric equations [124]

Name	**Boundary conditions and corresponding coefficients**	**Loading**	**Piezoelectric equations with shortened subscripts***
Type 1	Short-circuit compliance coefficients s_{ij}^E Stress-free dielectric constants ε_{nm}^T	T_j, E_m	$S_i = s_{ij}^E T_j + d_{mi} E_m$ $D_n = d_{nj} T_j + \varepsilon_{nm}^T E_m$
Type 2	Short-circuit stiffness coefficients c_{ji}^E Clamped dielectric constants ε_{nm}^S	S_i, E_m	$T_j = c_{ji}^E S_i - e_{jm} E_m$ $D_n = e_{mi} S_i + \varepsilon_{nm}^S E_m$
Type 3	Open-circuit compliance coefficients s_{ij}^D Stress-free impermittivity components β_{mn}^T	T_j, D_n	$S_i = s_{ij}^D T_j + g_{in} D_n$ $E_m = -g_{mj} T_j + \beta_{mn}^T D_n$
Type 4	Open-circuit stiffness coefficients c_{ji}^D Clamped impermittivity components β_{mn}^S	S_i, D_n	$T_j = c_{ji}^D S_i - h_{jn} D_n$ $E_m = -g_{mi} S_i + \beta_{mn}^S D_n$

*i, j = 1, 2, 3, 4, 5, 6; m, n= 1, 2, 3.

For piezoelectric element design in thickness vibration, it is common to start with Type 3 equation,

$$\begin{cases} S_3 = s_{33}^D T_3 + g_{33} D_3 \\ E_3 = \beta_{33}^T D_3 - g_{33} T_3 \end{cases} \tag{2.20}$$

By rearranging the equation, the relationship between stress T and electrical displacement D and strain S can be found,

$$T_3 = \frac{1}{s_{33}^D} S_3 - \frac{g_{33}}{s_{33}^D} D_3 \tag{2.21}$$

Inserting (2.21) to the second equation of (2.20), electrical displacement can be found,

$$E_3 = \beta_{33}^T \left(1 + \frac{g_{33}^2}{\beta_{33}^T s_{33}^D}\right) D_3 - \frac{g_{33}}{s_{33}^D} S_3 \tag{2.22}$$

Then, new wave equation can be derived (details provided in Appendix G) as

$$\frac{\partial^2 \xi}{\partial t^2} - \frac{1}{\rho s_{33}^D} \frac{\partial^2 \xi}{\partial x^2} = 0 \Rightarrow v = \sqrt{\frac{1}{\rho s_{33}^D}} \tag{2.23}$$

Solving the wave equation, the solution should take the form similar to (2.12) and given the boundary conditions as $\begin{cases} x = 0 & \dot{\xi} = \dot{\xi}_1 \\ x = l_0 & \dot{\xi} = -\dot{\xi}_2 \end{cases}$, one can find constants in the equation. Then, the displacement can be written as

$$\xi = \frac{-\dot{\xi}_2 \sin kx + \dot{\xi}_1 \sin k(l_0 - x)}{j\,\omega \sin kl_0} \tag{2.24}$$

Take the partial derivative of (2.24) with respect to x, the strain distribution is found as

$$\frac{\partial \xi}{\partial x} = \frac{-k\dot{\xi}_2 \cos kx - k\dot{\xi}_1 \cos k(l_0 - x)}{j\,\omega \sin kl_0} \tag{2.25}$$

From force equilibrium, the following equation can be found

$$F_1 = -ST|_{x=0} = \frac{Sk(\dot{\xi}_1 \cos kl + \dot{\xi}_2)}{s_{33}^D j\omega \sin kl} + S\frac{g_{33}}{s_{33}^D} D_3 \tag{2.26}$$

To establish the equivalent circuit, the relationship between the force F and the particle velocity $\dot{\xi}$ should be found; therefore, some work needs to be done on the right-hand side of (2.26). For the first part, the following transformation can be found (Appendix H)

$$\frac{Sk(\dot{\xi}_1 \cos kl + \dot{\xi}_2)}{s_{33}^D j\omega \sin kl} = j\rho c S \dot{\xi}_1 \tan\frac{kl}{2} + \frac{\rho c S}{j \sin kl}(\dot{\xi}_1 + \dot{\xi}_2) \tag{2.27}$$

Rearranging (2.20), we find Type 2 piezoelectric equation with parameters from Type 3 equation as

$$\begin{cases} T_3 = \dfrac{1}{S_{33}^D\left(1+\dfrac{g_{33}^2}{\beta_{33}^T s_{33}^D}\right)} S_3 - \dfrac{g_{33}}{s_{33}^D\beta_{33}^T\left(1+\dfrac{g_{33}^2}{\beta_{33}^T s_{33}^D}\right)} E_3 \\ D_3 = \dfrac{1}{\beta_{33}^T\left(1+\dfrac{g_{33}^2}{\beta_{33}^T s_{33}^D}\right)} E_3 + \dfrac{g_{33}}{s_{33}^D\beta_{33}^T\left(1+\dfrac{g_{33}^2}{\beta_{33}^T s_{33}^D}\right)} S_3 \end{cases} \tag{2.28}$$

Let

$$\beta_r = \varepsilon_{33}^S = \beta_{33}^T\left(1+\frac{g_{33}^2}{\beta_{33}^T s_{33}^D}\right) \tag{2.29}$$

and denote β_r as relative impermittivity of the material. This can be interpreted as the property of a parallel-plate capacitor. From Gauss Law, electric displacement D is independent of x and is equal to surface charge intensity, so

$$\oint_A D dA = d_{\text{free}} \Rightarrow D = \frac{Q}{A} \tag{2.30}$$

Then,

$$\begin{cases} I = \dot{q} = S\dot{D} \\ U = \int_0^l E\, dx \end{cases} \tag{2.31}$$

Note that S is the cross-sectional area of the piezoelectric element. Inserting the second equation for D_3 in (2.28) into the current equation in (2.31),

$$I = S\dot{D} = \frac{S}{\beta_r}\dot{E} + \frac{S g_{33}}{S_{33}^D \beta_r}\dot{S}_3 \tag{2.32}$$

Using the knowledge on the parallel-plate capacitor and the strain rate (provided in Appendix I), (2.32) can be written as

$$I = j\omega C_0 U - \eta(\dot{\xi}_1 + \dot{\xi}_2) \tag{2.33}$$

where $\eta = \frac{S g_{33}}{l S_{33}^D \beta_r}$ is defined as electromechanical coupling factor [122].

To derive the second term of the right-hand side of (2.26), first steps is to insert (2.22) into the voltage equation in (2.31),

$$U = \beta_r D l + \frac{g_{33}}{j\omega s_{33}^D}(\dot{\xi}_1 + \dot{\xi}_2) \tag{2.34}$$

Because,

$$\beta_r D l = \frac{\beta_r l q}{S} = \frac{\dot{q}}{j\omega C_0} = \frac{I}{j\omega C_0} \tag{2.35}$$

Then,

$$U = \frac{I}{j\omega C_0} + \frac{g_{33}}{j\omega s_{33}^D}(\dot{\xi}_1 + \dot{\xi}_2) \tag{2.36}$$

Combining (2.33) and (2.36),

$$U = U - \frac{\eta}{j\omega C_0}(\dot{\xi}_1 + \dot{\xi}_2) + \frac{g_{33}}{j\omega s_{33}^D}(\dot{\xi}_1 + \dot{\xi}_2) \Rightarrow \frac{g_{33}}{s_{33}^D} = \frac{\eta}{C_0} \tag{2.37}$$

Rearranging (2.34),

$$S\frac{g_{33}}{s_{33}^D}D = \eta U - \frac{\eta^2}{j\omega C_0}(\dot{\xi}_1 + \dot{\xi}_2) \tag{2.38}$$

which is the second term of the right-hand side of (2.26). Combining (2.26), (2.27), and (2.38)

$$F_1 = \left(\frac{\rho c S}{j\sin kl} - \frac{\eta^2}{j\omega C_0}\right)(\dot{\xi}_1 + \dot{\xi}_2) + \left(j\rho c S \tan\frac{kl}{2}\right)\dot{\xi}_1 + \eta U \tag{2.39}$$

Using the boundary conditions of the other end, $F_2 = -ST|_{x=l}$,

$$\begin{cases} F_1 = \left(\dfrac{\rho c S}{j\sin kl} - \dfrac{\eta^2}{j\omega C_0}\right)(\dot{\xi}_1 + \dot{\xi}_2) + \left(j\rho c S \tan\dfrac{kl}{2}\right)\dot{\xi}_1 + \eta U \\ F_2 = \left(\dfrac{\rho c S}{j\sin kl} - \dfrac{\eta^2}{j\omega C_0}\right)(\dot{\xi}_1 + \dot{\xi}_2) + \left(j\rho c S \tan\dfrac{kl}{2}\right)\dot{\xi}_2 + \eta U \end{cases} \tag{2.40}$$

where $\eta = \frac{Sg_{33}}{lS_{33}^D \beta_r}$ and $\beta_r = \beta_{33}^T \left(1 + \frac{g_{33}^2}{\beta_{33}^T s_{33}^D}\right)$. Then, the equivalent circuit can be developed as in Figure 2.3.

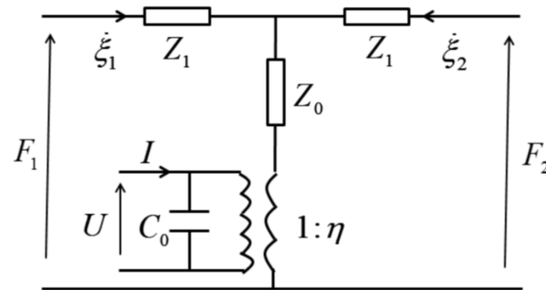


Figure 2.3: T-network equivalent circuit for piezoelectric materials.

The impedance shown in Figure 2.3 can be found by

$$\begin{cases} Z_0 = \dfrac{\rho c S}{j \sin kl} - \dfrac{\eta^2}{j\omega C_0} \\ Z_1 = j\rho c S \tan \dfrac{kl}{2} \end{cases} \tag{2.41}$$

This concludes the analogy for the piezoelectric materials [116,122].

As a complete piezoelectric vibrator, the front mass and back mass can be modeled by the circuit shown in Figure 2.2. The mechanical connection reflected in the electrical system is that the circuits are connected by its ports. An example can be found in Figure 2.4.

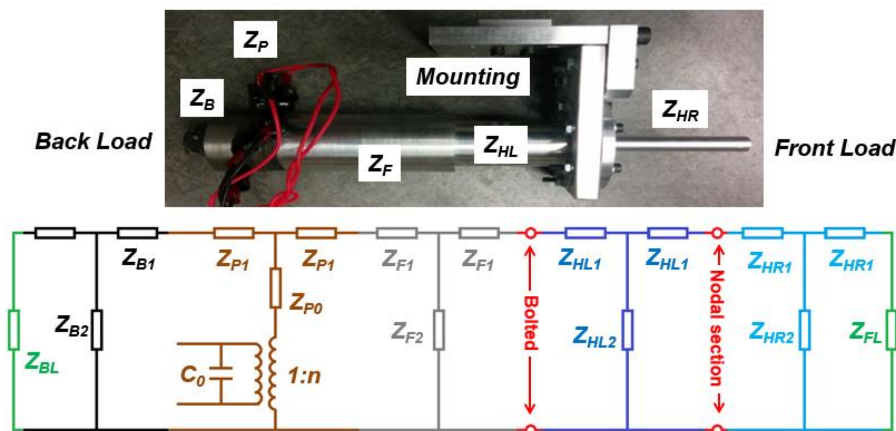


Figure 2.4: Example of connected equivalent circuits for mechanical structure.

2.1.2 Mobility Analogy in Analysis

The vibro-tactile sensor produces ultrasonic vibrations by converting the electrical AC signals into mechanical deformations by its transducer, and the whole structure resonates. So, the assembly can be considered as a resonator. The most representative equivalent circuit for resonators is the Butterworth-Van Dyke (BVD) circuit [29,115,125] (Figure 2.5). It is the same equivalent circuit adopted by IEEE standard for the piezoelectric element (Figure 1.2). In Figure 2.5, C_p represents the clamped capacitance of the piezoelectric material, and R_m, C_m, and L_m are derived equivalent electrical parameters representing mechanical resistance, capacitance, and inductance, respectively. The conductance (the inverse of the resistance R_m) is related to the dissipative component, the motional capacitance C_m represents the equivalent mass of the system, and the motional inductance L_m resembles the resultant mechanical compliance (the inverse of the stiffness) [126].

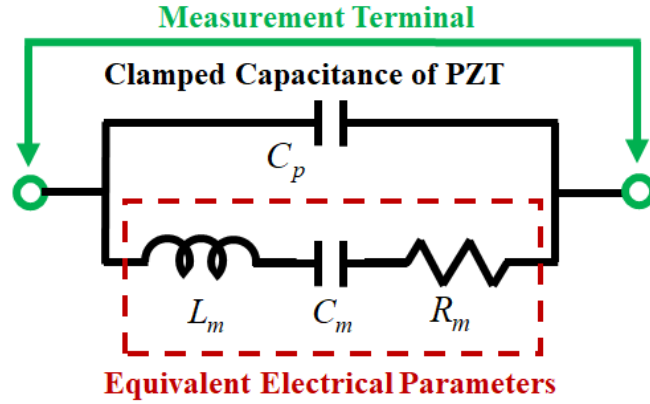


Figure 2.5: BVD model for the piezoelectric devices.

Given an impedance plot as shown in Figure 2.6, the components' values can be derived as (2.42) – (2.45) [29,114]. The quality factor (Q_m) of the mechanical structure, which is a measure of the damping in the resonant structure, is determined as (2.46).

$$C_p = \sqrt{\frac{Z_s^2(f_2^2 - f_1^2) + \sqrt{Z_s^4(f_2^2 - f_1^2)^2 + 4f_2^4 Z_s^2 Z_p^2}}{8\pi^2 f_2^4 Z_s^2 Z_p^2}} \tag{2.42}$$

$$R_m = \sqrt{\frac{Z_s^2}{1 - 4\pi^2 Z_s^2 f_1^2 C_p^2}} \tag{2.43}$$

$$C_m = \frac{f_2^2 - f_1^2}{f_1^2} C_p \tag{2.44}$$

$$L_m = \frac{1}{4\pi^2 C_m f_1^2} \tag{2.45}$$

$$Q_m = \frac{1}{R_m} \sqrt{\frac{L_m}{C_m}} \tag{2.46}$$

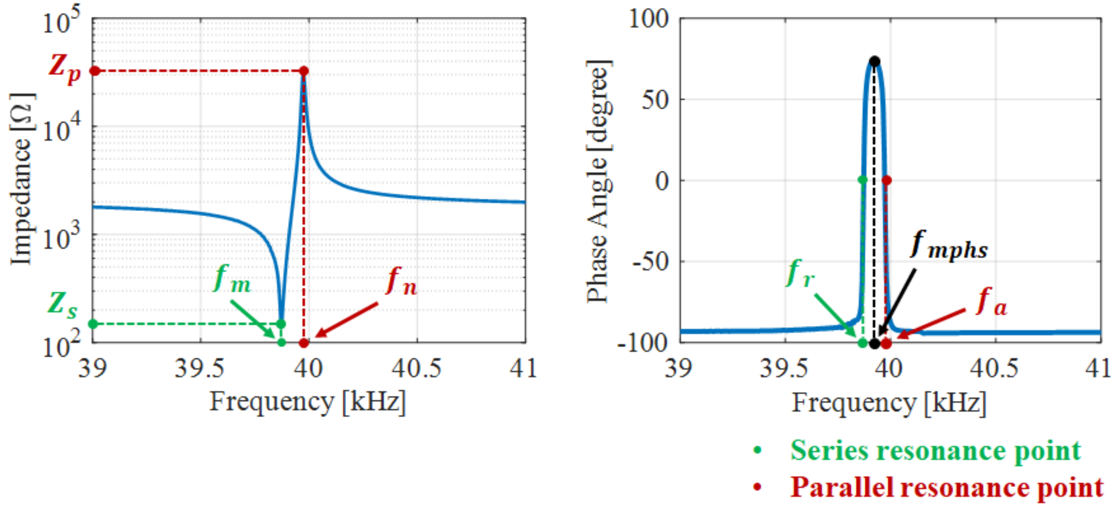


Figure 2.6: Characteristic data points in typical impedance vs. frequency and phase angle vs. frequency responses of a piezoelectric device.

In deriving these equations, it is usually assumed that the minimum impedance frequency (f_m), series motional mechanical resonance frequency (f_s), and series electrical zero phase frequency (f_r) are equal and can be regarded as f_1. Similarly, the maximum impedance frequency (f_n), parallel motional mechanical resonance frequency (f_p), and parallel electrical zero phase frequency (f_a) are assumed to be equal and regarded as f_2 [29,114]. Although these assumptions make the problem simpler, they also cause the discrepancy between analytical and the experimental results. As the mechanical quality factor decreases (loss in

the system increases), the gaps between the frequencies within the same frequency group become larger, which results in the weakening of the frequency-related assumptions, and finally leads to a noticeable difference between the analytical predictions and the actual measurement. To resolve this issue, initial electrical components' values were analytically found from (2.42) – (2.45) first, and then a non-linear multi-parameter regression was performed on the impedance vs. frequency signature curve as illustrated in Figure 2.6, using the nonlinear regression model ("nlinfit" function) in MATLAB. The impedance expression (|Z|) was the dependent variable, which can be derived from Figure 2.5 as (2.47).

$$|Z| = \sqrt{\frac{(4\pi^2 C_m L_m f^2 - 1)^2 + 4\pi^2 C_m^2 R_m^2 f}{\left(2\pi C_m f + 2\pi C_p f - 8\pi^3 C_m C_p L f^3\right)^2 + 16\pi^4 C_m^2 C_p^2 R_m^2 f^4}} \tag{2.47}$$

It is worth noting that typical values of these parameters are far apart each other in magnitudes; if measured in standard SI units, R_m, C_m, C_p, and L_m values have typical magnitudes of 10 (Ω), 10^{-11} (F), 10^{-9} (F) and 10^{-1} (H), respectively. In this case, direct regression adopting original parameters is improper because of the large differences in orders of magnitudes. To address this mathematical concern, while keeping the R_m and L_m values from the analytical solutions for the nonlinear regression, two pseudo-multipliers were assigned to capacitance values as agents for parameter tuning, i.e., the C_m and C_p in (2.47) were replaced by $k_1 C_0$ and $k_2 C_{0p}$ in regression process. k_1 and k_2 are the pseudo-multipliers, and C_0 and C_{0p} are constants found from the analytical solutions with the order of magnitude less than 10^{-10}. In doing so, the magnitude of each parameter in the curve-fitting was balanced between 10^{-2} and 10^{2} [114].

2.2 PCB Design Procedures

In this project, the analog front end (AFE) of the system has to be made from a customized printed circuit board (PCB). A free electronic design automation (EDA) software called KiCAD (available from https://kicad-pcb.org/) can be used to design the schematics and the PCB layout. Typical design procedures with KiCAD are as follows:

1. Create a project and setup a project folder to organize all the design files.

File extensions for important design files are listed in Table 2.3.

Table 2.3: Important files in KiCAD

File extension	Description
*.pro	Project file
*.sch	Schematic file
*.net	Netlist file
*.lib	Component library file
*.kicad_mod	Footprint file
*.kicad_pcb	PCB layout file

2. Build/import components and establish a schematic.

   This step concerns the tool Eeschma in KiCAD. KiCAD provides various generic symbols for frequently used electrical components or ICs. Since it is open source, many developers share their libraries of components on GitHub. Through internet connection, the library in the local installation can always be synchronized with new libraries available online. If a specific component is nowhere to be found, user can customize a new symbol by using the Library Editor provided by KiCAD.

3. Annotate all the components in the schematic and generate the netlist.

   This step is also done in Eeschma. The annotation is required for generating a netlist which describes the electrical connections defined in the schematic. The electrical rule check tool available in Eeschema can help diagnose the circuit as it will report the pin conflicts, missing drivers, and unconnected pins.

4. Assign footprints to all the components

   A footprint represents the actual physical arrangement of the pads for the components. An associated footprint must be assigned to the corresponding component before the component can be seen in the PCB layout design. Footprint Editor can be used to customize a footprint if needed. The footprint a component can be changed anytime during the development. Since it reflects the real dimensions and

connections of the IC packaging appears on the board, wrong selection for the footprint can ruin the design.

5. PCB layout design

   The PCB editor, “PCBnew”, is used to arrange the PCB layout. The netlist generated in step 3 should be read into the program so that the software can provide guidance on the required pin connections. It is a good practice to check if footprints assigned in step 4 are correct. Modifications can be made in the PCB editor if needed. The electrical design rules must be set for the design according to the requirement of the design and capacity of the manufacturer. The calculations for the design rules can be done with the help of the tool “pcb_calculator” in KiCAD. Normally, the PCB layout file (*.kicad_pcb) generated by the editor is enough for the manufacturer to work with. If needed, KiCAD also provides tools to export the design into other universal format like Gerber files.

2.3 FPGA Development Procedures

The development environment for FPGA is determined by the supplier of the chip selected. As mentioned in Section 1.3.3, there are two major suppliers, Intel and Xilinx. The development suite from Intel is Quartus Prime, and the one from Xilinx is Vivado. In this project, the system is based on an Intel FPGA chip, Cyclone V SoC FPGA. Therefore, the development procedure discussed here concerns Quartus Prime. There are three editions for Quartus Prime. The edition makes a difference in the FPGA chip families and software tools it supports [127]. The Lite edition (version 18.1) was chosen because it supports Cyclone V FPGA development. The user interface for Quartus Prime Lite 18.1 is shown in Figure 2.7.

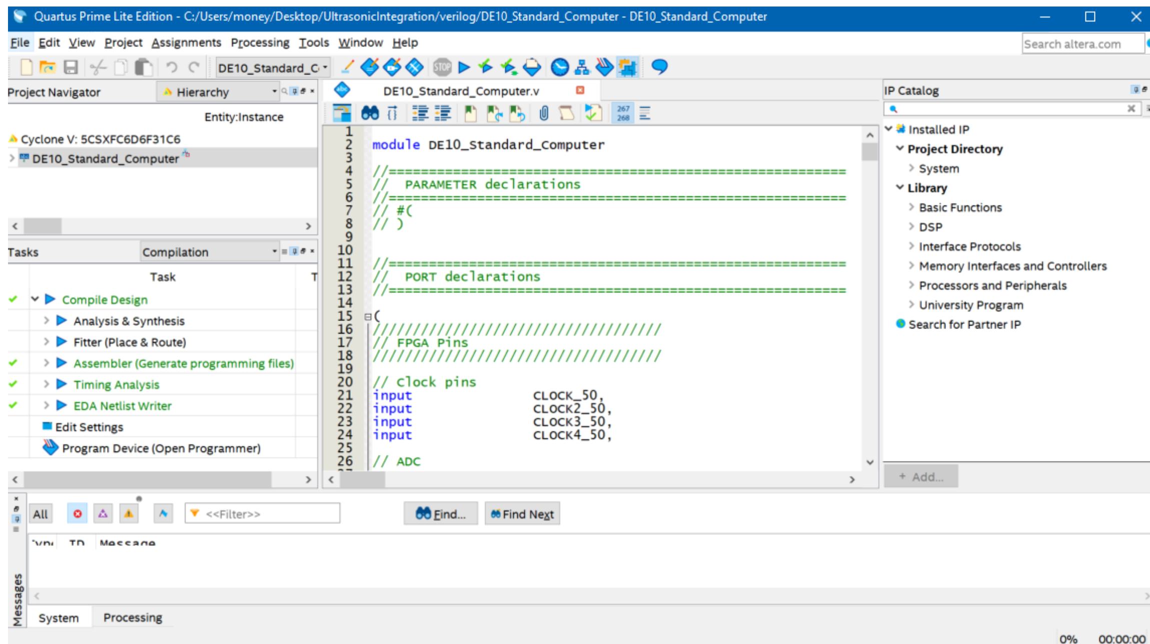


Figure 2.7: Quartus Prime Lite 18.1 user interface.

Quartus Prime helps the user organize their project, relate the HDL designs to the actual hardware I/O pins with the help of various tools. The complier will compile the design and conduct circuit and timing constraint optimization based on the analysis on the code. A brief design procedure using Quartus Prime is as follows:

1. Create a project and specify the chip to develop in the settings

2. Include all the relevant developed HDL design files (templates, function blocks, etc.) into the project

3. Use the Platform Designer (a graphical programming tool) to establish the interconnection between the hard processor system (HPS) and FPGA fabric and generate the top-level HDL template. Add the generated template to the top-level module and modify the I/O definitions to facilitate all the instantiated modules in the Platform Designer.

4. (If applicable) refine the top-level module with the code generated by the System Builder (a development tool, which will be introduced in Section 4.1.2, provided by a third-party distributor of the development board for FPGA)

5. (If applicable) run the Tool Command Language file (*.tcl) in some premade project files (it resembles command lines which execute operations based on script contents)
6. Develop and revise HDL codes as per user's needs
7. Conduct the compilation process and start debugging with the help of error/warning messages
8. Based on the timing analysis results, make adjustment in the Timing Analyzer to update the Synopsys Design Constraints (SDC) files. Some iterations in step 5 to 8 may be required until the design satisfy the need of the project.
9. Load the binary file (*.sof) generated after the compilation to the FPGA with the Programmer tool in the Quartus Prime or convert the binary file into other format for other programming methods.

In this project, the system was not built from scratch. It was a modified version of the DE10-Standard Computer template included in the Intel University Program. However, other than the development in HDL codes, there was still a large portion of the premade system which had to be modified or customized. The system interconnection layout, for example, was fully popularized in a convoluted manner, and therefore substantial modifications were needed to satisfy the need in the project. Other than the HDL templates, inside Quartus Prime, Intel provides Intellectual Property (IP) blocks for commonly used circuits [128]. The dual clock FIFO module and the dual port RAM are two IP blocks used in this project. Other functional block instances in FPGA were coded in Verilog HDL. The compiled project file was converted to the compressed raw binary file and loaded on the micro-SD card for later FPGA configuration through Linux installed on ARM powered HPS.

2.4 HDL Programming

The FPGA programming is basically defining circuits in hardware description language (HDL); hence, it is a part of hardware engineering. Coding in HDL is different from doing so in software language. In software, codes are executed line by line sequentially, while in HDL, codes do not infer an algorithm but defines a circuit. Circuits are inherently parallel as

the current will just flow if it is allowed. As mentioned in Section 1.3.3, FPGA is powerful in clocked operations. The massive parallelism with a design concept built on pipelined operations can defy the developers' intuition based on software development.

The one problem that resembles the multi-threading or parallelism issue in software is that the parallelism can possibly cause corruption of data. For example, if a conditional statement depends on a register's value to perform specific operations and those operations last several clock cycles, the outcome may not hold valid if the conditional statement is not applied on the same value. The reason is that the register value can be updated in each clock cycle. In these circumstances, delays (usually realized by shift registers) should be applied to hold the value until the end of the statement process. It is a way of realizing pipelined structure [13]. Another problem that is seldom an issue in software is that the signal can stay in a metastable state if a transition between clock domains is required. This is an inherent behavior of the asynchronous circuit operations because it can cause a register to change its digital state ("0" or "1") constantly. The rising and falling time of the voltage can cause the register fail to be locked in a stable state and thus generate unpredictable results. In order to address this issue, dual clock FIFO or a series of shift registers can be used to stabilize the data through a series of delays.

Despite the usefulness of the intentional delays, undesired ones can jeopardize the design easily due to the parallelism. The operations should be executed in parallel in every clock cycle, but a long data path, excessive circuit components, or complicated logic structures can delay the signal's appearance at the output. These kinds of delays are harmful to the timing of the signals. When multiple operations are conducted at the same time and the output is a combinatorial result of them all, it can infer a racing condition in which the outcome becomes unpredictable. Then, the "sequential logic" should be introduced to prevent this from happening. In order to safely implement "sequential logic" like in a software program, we must develop the hardware logic with finite state machines (FSM) [57] so that proper sequence of operations can be executed correctly by state changes. To make the FSM work, coherent internal signaling and sound hardware logics are essential.

Chapter 3

Electro-mechanical Design and Analysis of Vibro-tactile Sensor

3.1 Introduction

A hybrid approach was used to design an ultrasonic concentrator for vibro-tactile sensor. The approach is twofold: first, the base design was derived analytically using impedance analogy discussed in Section 2.1.1. Then, the design was refined by numerical simulation using a commercial finite element analysis (FEA) software, COMSOL Multiphysics. The impedance analogy was adopted for the concentrator design, because the structure of the filter was predefined before the design phase and the components are connected by the force boundary. Although electro-mechanical analogies can reduce the complexity of solving differential equations, the models used in the analogies are overly simplified and many details are neglected in the analytical derivations. Therefore, in addition to the impedance analogy, numerical (FEA) simulations were subsequently conducted to modify the parameters in the model so that a realistic design can be approached.

In this research, the shape was predefined based on the application considerations and was initially designed with analytical derivations, which made the sensitivity analysis for different design parameters possible. A graphical solution was used to analyze the sensitivity of tunable parameters. The following FEM refinement took advantage of the analysis and adjusted the design parameter accordingly to reach the design goal in an efficient way.

3.2 Design with Electro-mechanical Analogy

3.2.1 Design Overview

The base shape of an ultrasonic vibration concentrator is a cylindrical rod with varying diameter, which can be simplified into a 2D model as shown in Figure 2.1. When testing a soft sample with a tactile sensor, it is important to minimize the contact area to pinpoint the measurement position and avoid the influence of adhesion. In the meantime, the tactile end should not be too sharp to create excessive local stress concentration that can damage the surface. As a compromise, the tactile end of the vibration concentrator was designed to be a

hemispherical-shaped probe head with a diameter of 5 mm. Note that as a vibro-tactile sensor, the structure should be subjected to the resonance conditions of the whole system. Hence, the design of the vibration concentrator should be conducted considering the characteristics of the vibration source. In this study, the ultrasonic vibration concentrator was to pair with a commercial Langevin ultrasonic transducer (HEC-1340P4BF, Honda Electronics, Japan) that has an output end of 13 mm diameter. Note that the transducer was a commercial product, therefore the following tests and analysis treated it as a standalone unit, whose detailed mechanical and electrical properties can be reviewed in manufacturer's official website. Nevertheless, during the electrical test of the vibro-tactile sensor, the bare transducer was tested with an impedance analyzer (HP4194A, Hewlett Packard, USA) to confirm its in-situ performance. The input end of vibration concentrator should be tightly connected to the output end of the transducer with a stressed bolt. To maximize the wave propagation efficiency, the entire area of the output end of the transducer should be contacted with the input end of the concentrator. Therefore, the diameter for the input end of the vibration concentrator was set to be 20 mm, which resulted in a design of decreasing radius from the input end towards the probe head.

The working frequency of the Langevin transducer is rated as 40 kHz, which is the resonance frequency of the structure where the vibration amplitude of the unit increases dramatically when the frequency of the input signal approaches it. It can be identified in the vibration spectrum diagram as an isolated peak. In vibro-tactile sensing applications, frequency shift of that peak occurs when the sensor is in contact with the surface of the tested object. By introducing the vibration concentrator, it is expected that the bandwidth of the peak should be further reduced so that the frequency shift is more distinct in sensing operations. However, this effect is varied depending on the transitional shape of the vibration concentrator. Different shapes have their own limits, so there have been efforts delivering new designs adopting sophisticated mathematical functions [129]. In this design, instead of a continuous horn shape following a specific function, a combinational-shaped concentrator with a step and a taper was adopted for design simplicity. It will be shown later that this design does not sacrifice performance but greatly facilitates the fabrication.

3.2.2 Design Procedures

Analytical model of the concentrator was developed by applying impedance analogy discussed in Section 2.1.1. In this study, the ultrasonic concentrator was developed following the procedures exhibited in Figure 3.1. Initially, the concentrator was sketched out as a half-wavelength long stepped horn, which is a successive combination of two equally long cylinders of different diameters. Then, a tapered feature was introduced between the steps with different diameters for smooth transition. Next, a flange was added to the design to provide its mechanical support to fixtures. Note that the flange should be placed at the nodal section where the amplitude is zero to avoid the interaction with the environment. Therefore, the mid-plane of the flange divides the whole concentrator into two halves: The front half acted as a quarter-wavelength cantilever horn, and the rear half played as a quarter-wavelength cylinder. As a result, the resonance condition can be solved either for the minimum impedance of total structure, or for the maximum impedance of each half corresponding to quarter-wavelength. After the shape was defined, the lengths of major parts were assigned with parameters in favor of the numerical process programming and the parametric FEA simulation in the next phase.

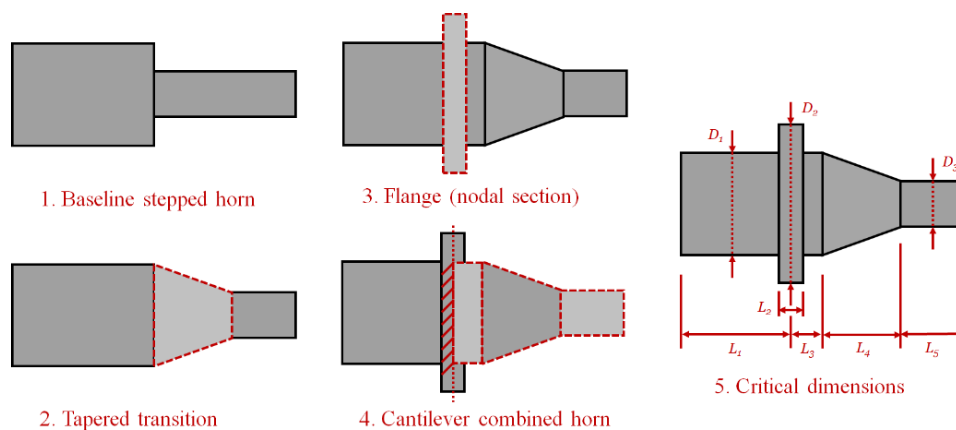


Figure 3.1: Design flow of an ultrasonic concentrator [39].

During the analytical derivation process, the mechanical design can be converted into the equivalent circuit as shown in Figure 3.2.

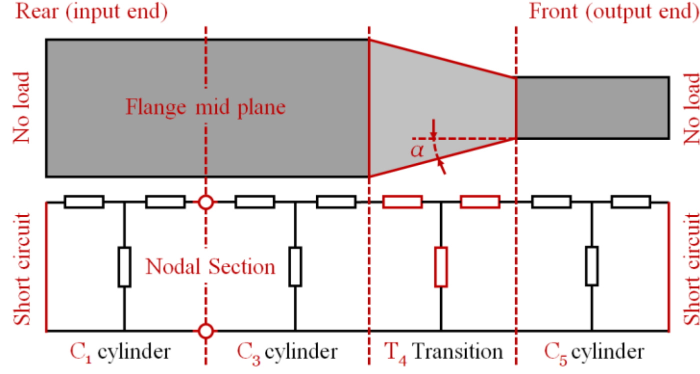


Figure 3.2: Equivalent circuit for the concentrator.

Note that the flange shape in Figure 3.1 was omitted in the equivalent circuit because the ideal flange should be as thin as possible to minimize the influence on structural vibration characteristics. However, it also should be sturdy enough to support the structure. As a compromise, the flange thickness (L_2) was designed to be 2 mm, which was added later in FEA simulation. There were two relevant geometries, the cylinder shape (C_1, C_3, and C_5) and circular truncated cone shape (T_4). In a 2D model, cut-plane views of cylinders and truncated cone are rectangular and isosceles trapezium, respectively, which can be translated into shape functions in (3.1) and (3.2).

$$S_C(x) = S = \frac{1}{4}\pi D^2 \quad \text{where } D = D_1 \text{ } or \text{ } D_3 \tag{3.1}$$

$$S_T(x) = S_1(1 - \alpha x)^2 = \frac{1}{4}\pi D_1^2(1 - \alpha x)^2 \quad \text{where } \alpha = \frac{D_1 - D_3}{D_1 l} \tag{3.2}$$

By substituting (3.1) and (3.2) into (2.19), impedance expressions for both shapes could be derived as (3.3) and (3.4).

$$\begin{cases} Z_{C1} = j\rho cS\tan\dfrac{kl}{2} \\ Z_{C2} = Z_{CL} \\ Z_{C3} = -\dfrac{j\rho cS}{\sin kl} \end{cases} \tag{3.3}$$

$$\begin{cases} Z_{T1} = j\rho cS_1\left[\tan\dfrac{kl}{2} + \left(1-\dfrac{D_3}{D_1}\right)\left(\dfrac{1}{kl}-\dfrac{1}{\sin kl}\right)\right] \\ Z_{T2} = \dfrac{D_3}{D_1}j\rho cS_1\left[\dfrac{D_3}{D_1}\tan\dfrac{kl}{2} + \left(1-\dfrac{D_3}{D_1}\right)\left(\dfrac{1}{\sin kl}-\dfrac{1}{kl}\right)\right] \\ Z_{T3} = -\dfrac{D_3}{D_1}\dfrac{j\rho cS_1}{\sin kl} \end{cases} \tag{3.4}$$

Based on (3.3) and (3.4) and referencing Figure 2.2 with both force terminals shorted, the total impedance for cylinder and truncated cone shape can be determined. By substituting different lengths (ranging from 0.01 mm to 80 mm with a step size of 0.01 mm), the impedance values for both shapes can be calculated and were plotted in Figure 3.3.

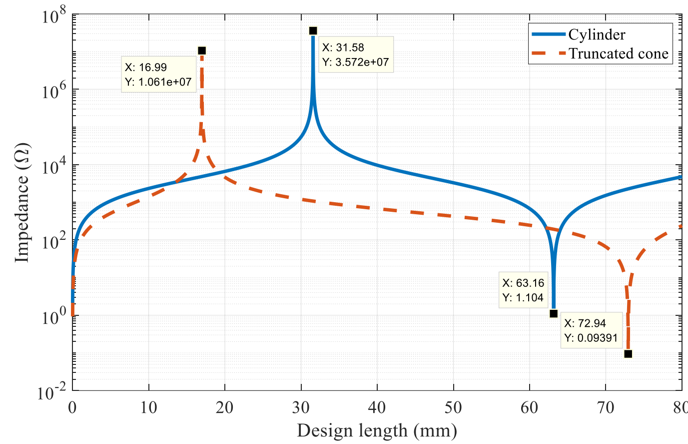


Figure 3.3: Impedance of cylinder and truncated cone with different design lengths.

In Figure 3.3, x-coordinates of the data points with maximum impedance are the quarter-wavelengths for the corresponding shapes, while the ones with minimum impedance are half-wavelengths. Therefore, L_1, the length of the rear half cylinder, should be designed to be 31.58 mm. Calculating the quarter-wavelength based on the material properties (Al 6061) and 40 kHz frequency yielded the same value, which shows the validity of equivalent circuit method.

It is worth mentioning that the wave propagation inside truncated cone (T_4 in Figure 3.2) is not uniformly distributed. This is reflected in (3.4) where the length parameter takes place outside the trigonometric functions of the impedance expression, which leads to an expression for total impedance being aperiodic. As a result, the quarter-wavelength of truncated cone is different from that of the cylinder. From Figure 3.3, it was estimated to be 16.99 mm. As for the front half, total length ($L_3 + L_4 + L_5$) should be equal to the quarter wavelength. Since the quarter-wavelength of truncated cone is 16.99 mm, L_4 should not exceed this value. In order to allow the room for L_3 and L_5, 13 mm was selected for L_4, which resulted in the half cone angle of 30°. As for L_3 and L_5, the total impedance expression for the parts in the right side of the nodal section in Figure 3.2 was established in MATLAB by following the electric circuit laws. Substituted the symbolic parameters with all the known values, the numeric results of the impedance with different combinations of L_3 and L_5 values (both ranging from 0.1 mm to 50 mm with a step size of 0.1 mm) were calculated. The results were converted into logarithmic scale and are presented in Figure 3.4.

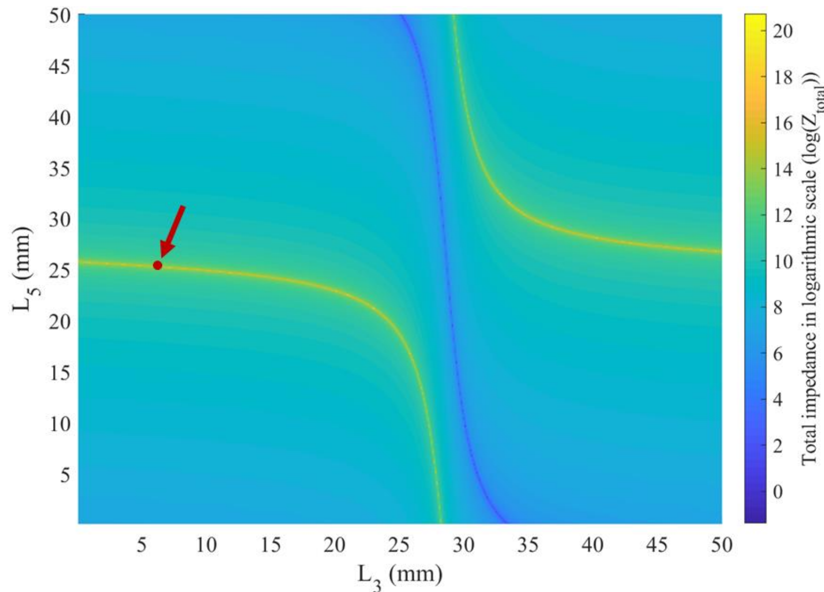


Figure 3.4: Map of Impedance (in logarithmic scale) as a function of L_3 and L_5.

Two light-colored curves in the top right and bottom left quarters of Figure 3.4 mark the maximum impedance locations and the dark-colored curve in the middle shows the minimum

impedance region. Parameters for quarter wavelength design should be selected from either of light-colored curves. In order to make a concise design, lengths were chosen from the left side region (pointed by an arrow in Figure 3.4). L_3 and L_5 corresponding to this point are 6 mm and 25.3 mm, respectively. The plateau-like curve around the chosen point suggests that the influence of L_5 on the impedance is much greater than that of L_3.

At this stage, all the dimensions were determined under the assumption of no energy loss in the system. The model also neglected detailed design features, such as bolt holes, flat surface pairs on the cylindrical body for clamping during assembling process, flange at the nodal section for connection to the external structures, and hemispherical tactile part. These simplifications accompanied by the 2D modeling resulted in errors in the calculation. Analytical considerations of all these features are almost impossible [130,131]. Therefore, base design derived from the equivalent circuit method was modelled with FEA, and all details were refined through iterative processes.

3.2.3 FEA and Final Design

The base 2D skeleton model was extended to a realistic 3D model with COMSOL Multiphysics, containing all detailed features, as shown in Figure 3.5.

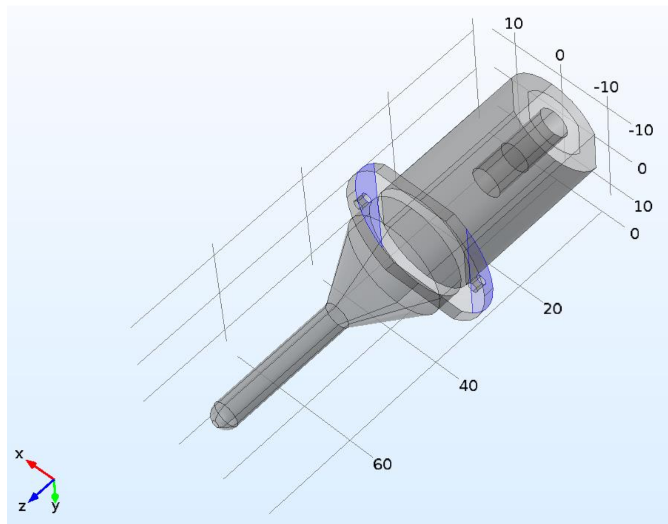


Figure 3.5: Realistic 3D FEA model in COMSOL with all design features (all dimensions in mm) and fixed boundary shown in purple.

Fixed constraint was imposed to the purple surfaces to mimic the mechanical restriction from installation in actual applications. The analysis steps were conducted under no-load condition on both ends. Other than the features that were mentioned in the previous section, a M6 threaded installation hole was added to the input end of the vibration concentrator, which was used to connect to the transducer with a stud. Two bolt holes were also made in the flange for the installation. A pair of parallel surfaces were milled on both sides of the concentrator input end to help apply pre-stress between the transducer and the concentrator with a calibrated torque wrench.

The dimensions of the FEA model was refined through iterative FEA simulation until the resonance frequency converged to 41 ± 1 kHz with a nodal section locating at the flange. The frequency was set slightly higher than the target frequency of 40 kHz because the numerical simulation with finite elements tends to overestimate the stiffness of the system. With all the design features implemented (mostly mass removal), the model-estimated resonance of the initial model was predictably higher than design target. First adjustment was happening in L_5 because the impedance was more sensitive to it (largest gradient) as illustrated in Figure 3.4. A parametric sweep was set up for L_5 with a step size of 0.1 mm ranging from 25.3 mm to 28 mm to search for an optimal design, and 27.5 mm was chosen. Then, based on the displacement distribution along the longitudinal direction of the surface, a new position (L_1) for flange was determined. Since the flange was only 2 mm in thickness and it was originally placed near the nodal section, the impact from L_1 adjustment on the frequency was negligible. For close values, for example, 0.1 mm difference in L_5, the resultant frequency difference was small (~100 Hz, or 0.3%), the final choice of value was opted for manufacturing considerations. The drawing of the refined model is presented in Figure 3.6, and the critical dimensions of the concentrator before and after the refinement are presented in Table 3.1.

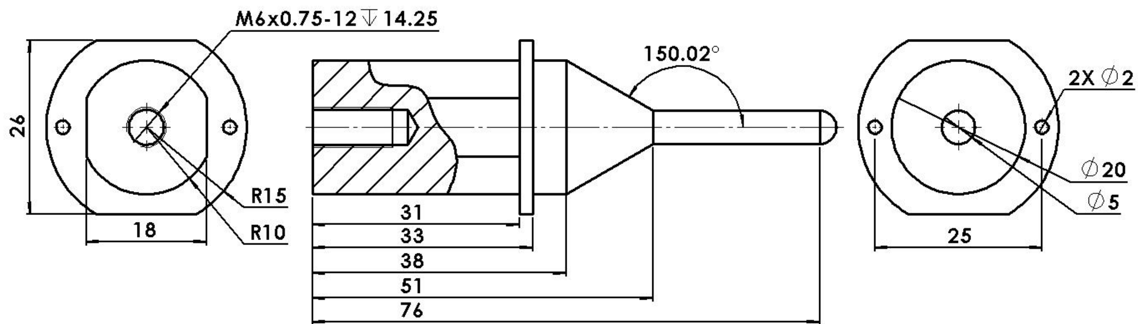


Figure 3.6: Final design of the concentrator (all dimensions in mm).

Table 3.1: Critical Dimensions of the Design before/after the refinement

Parameter	Description	Initial (mm)	Refined (mm)
L_1	Bottom to the nodal	31.6	32
L_2	Flange thickness	2	2
L_3	Nodal to the taper	6	6
L_4	Taper length	13	13
L_5	Taper to the tip	25.3	27.5
R_1	Input radius	10	10
R_2	Flange radius	15	15
R_3	Output radius	2.5	2.5

3.3 Electro-mechanical analysis of the tactile sensor

In this research, it is more important to model the load to derive the characteristics of the sample than to find a comprehensive model for the whole structure. Therefore, instead of using a convoluted model to fully describe the behavior of each component of our sensor, we can keep using the BVD model (Figure 2.5) to analyze the sensor assembly (including the transducer, the vibration concentrator, and the part of object under test) as a single vibrator operating at an isolated vibration mode. The analysis of the tactile sensor was conducted with the mobility analogy explained in Section 2.1.2. However, a modified model was proposed for analysis on the tactile sensor during applications (Figure 3.7).

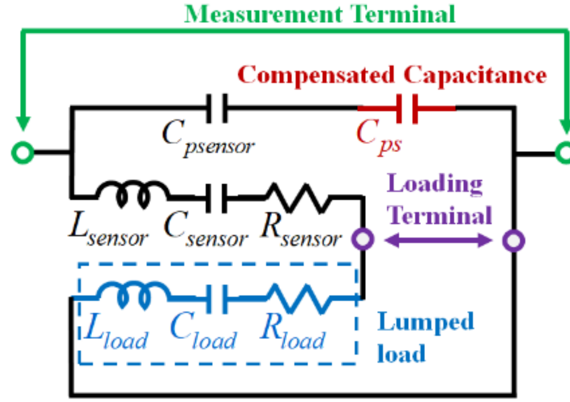


Figure 3.7: A modified BVD model for the tactile sensor.

Mechanically, the surface of the object in contact with the sensor tip is assumed to maintain a continuum condition; hence, the contact can be considered as a series connection mechanically. Since the mobility analogy preserves this topology by finding the equivalency between the force and current, the load can be modelled as another LCR circuit branch (lumped load as L_{load}, C_{load}, and R_{load}) connected to the equivalent circuit representing the mechanical behavior of the sensor (the branch with L_{sensor}, C_{sensor}, and R_{sensor}) in series. It is worth mentioning that the mechanical loading will also affect the characteristics and performance of the piezoelectric elements, which effectively changes C_p, at the electrical terminal. Adding more horns or boosters to the system will increase C_p; however, the increase of C_p due to external attachments is limited to be less than +50% [29]. So, due to the loading effect from the object to C_p, C_{ps} is added in series to the clamped capacitance to compensate for it. Thus, a modified equivalent circuit for loaded cases was established as Figure 3.7.

Following Figure 2.5, the total impedance (Z_m) of the mechanical equivalent circuit branch can be expressed as

$$Z_m = \frac{V}{I} = R_m + j\left(\omega L_m - \frac{1}{\omega C_m}\right) \tag{3.5}$$

where V is the supply voltage, I is the current. When electrical series resonance happens, the reactance from L_m and C_m cancels out; therefore, V and I become in phase, following Figure 3.7, (3.5) is reduced to

$$Z_{m@f_1} = \frac{V}{I} = R_m = R_{sensor} + R_{load} \tag{3.6}$$

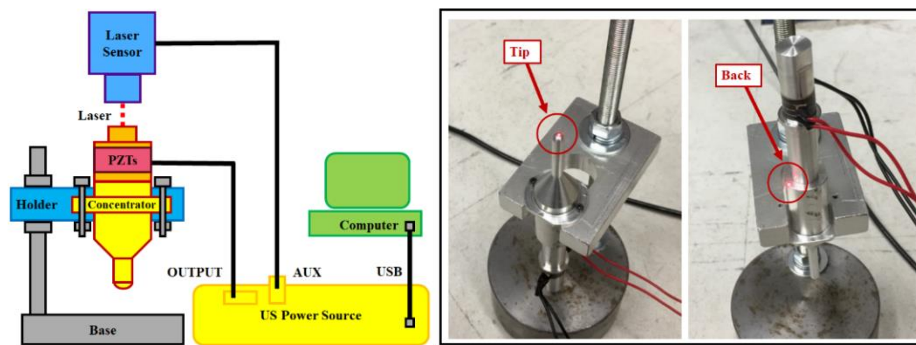
The electrical characteristics of the vibro-tactile sensor are assumed to be constant regardless of the samples tested; thus the equivalent resistance of the load R_{load} is the only term changing depending on the loading condition at f_1. In doing so, the electrical parameters for the load can be extracted from the original structure. When the electrical parameters for the vibro-tactile sensor at no-load condition were determined as the calibration data, the ones representing the lumped load can be calculated with the data found in loaded conditions.

3.4 Experiment with the Developed Tactile Sensor

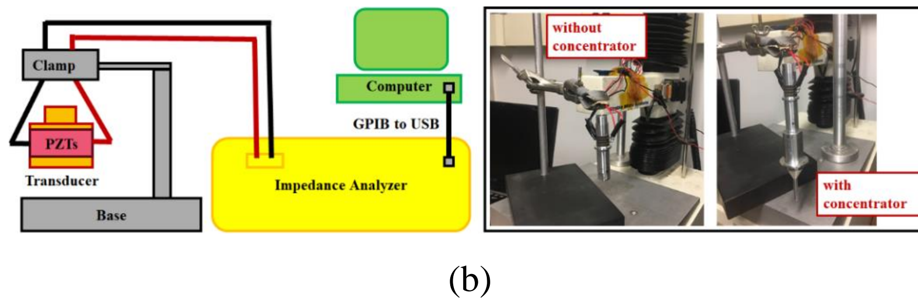
Two types of experiments were performed. Characteristic tests were conducted to confirm the competence of the design by measuring and analyzing the characteristics of the sensor. Tactile sensing tests on soft samples were carried out to evaluate sensor's performance and examine the equivalent electrical parameters as candidates for stiffness indicators.

3.4.1 Characteristic Tests

Since the ultrasonic tactile sensor has both electrical and mechanical aspects, a series of tests were conducted to identify the electrical and mechanical characteristics of the sensor. Test setups were presented in Figure 3.8.



(a)



(b)

Figure 3.8: Schematics and the real experiment setup for (a) mechanical characteristic tests, and (b) electrical characteristic tests.

Mechanical characteristic tests were conducted using laser Doppler vibrometer (OFV-505, Polytec, Germany). A stable holding mechanism was implemented to firmly fix the ultrasonic tactile sensor at its flange. The transducer was driven by the ultrasonic power source (PDUS200, Micromechatronics, USA) connected to its electrical terminals. The vibrometer fed the measured voltage into the auxiliary input of the power source. The AC electric signal level generated by the ultrasonic power source was set to 20 Vp-p, and the sensitivity of the laser Doppler vibrometer was tuned to 1 um/V. For each measurement, a complete cycle sweep was conducted, i.e., it swept and recorded the dynamic response from 38 kHz to 42 kHz frequency forward and then backwards. The measurement was taken on the tip and back of the concentrator as indicated by arrows in Figure 3.8(a). The synchronized data (driving voltage and concurrent vibration) were transmitted to the control computer for further comparisons. Electrical characteristic tests were conducted by an impedance analyzer (HP4194A, Hewlett Packard, USA), where frequency sweeps were performed with and without the concentrator. The range of frequency sweep was set to 39 kHz to 41 kHz and 38 kHz to 46 kHz for the tests with and without the concentrator, respectively, due to the shift of resonance frequency. During tests, the sensor was held in a suspended position with its powering cables clamped to a stable stand as indicated in Figure 3.8(b). The driving voltage from the analyzer was set to 1 Vrms. The impedance vs. frequency data were recorded by the impedance analyzer and transferred to the computer via GPIB connection under the supervision of a customized LabVIEW program. Then, the

equivalent electrical parameters of the data were derived using techniques discussed in Section 2.1.2.

3.4.2 Preparations for Tactile Sensing Tests

To evaluate the performance of the tactile sensor integrated with the vibration concentrator for soft materials, a set of experiments on the silicone samples with different stiffness (10 kPa < E < 150 kPa) was to be conducted with setup shown in Figure 3.9.

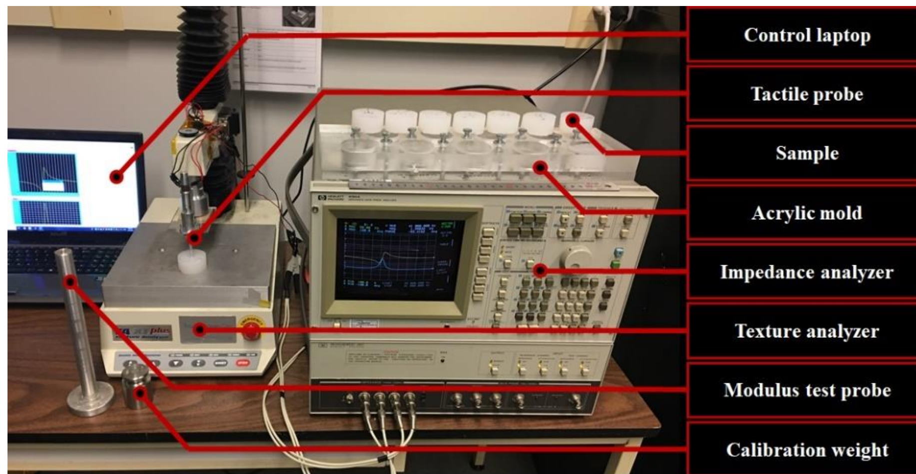


Figure 3.9: Experiment setup for tactile sensing tests.

The silicone samples were fabricated from the platinum cure silicone rubber (Ecoflex 00-30, Smooth-On, USA) and the stiffness of the samples was varied by adding different portion of thinner to the silicone compound. The weight of mixture for each sample was carefully controlled to be 40 ± 0.1g. The mixture was stirred for at least 3 min before pouring into an acrylic mold. The diameter and the depth of each mold hole were 44.5 mm and 25.4 mm, respectively. After curing for 24 hours in room temperature, the samples were taken out, and their height and mass were measured to calculate the density. Finally, six test positions were marked out for tactile sensing tests, as shown in Figure 3.10. All the test points were located within a circular area with less than 20 mm diameter.

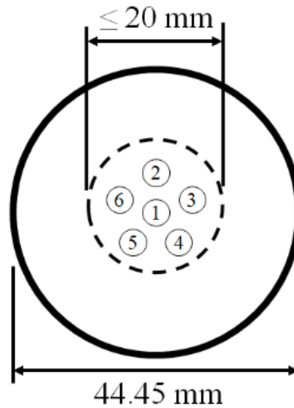


Figure 3.10: Test positions on the samples.

Elastic moduli (E) of the samples were measured by conducting compression tests using TA XT Plus texture analyzer (Stable Micro Systems, England). A compression probe with a 65 mm-diameter cylindrical surface (modulus test probe in Figure 3.9) was used to obtain the loading-unloading curves for each sample. Rate of compression was 0.3 mm/s and the maximum compression was set to 25%. The E for each sample was determined by the slope of unloading curve. The sample number, compound composition, ρ, and E of each sample are shown in Figure 3.11.

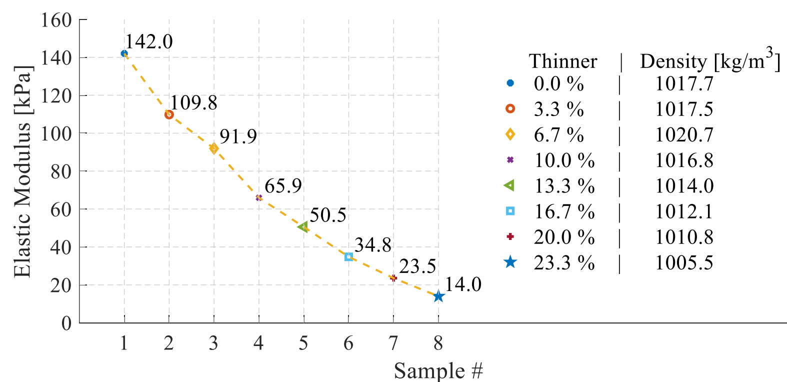


Figure 3.11: The compound composition and corresponding elastic modulus of the samples.

3.4.3 Tactile Sensing Tests

After the mechanical properties of the samples were determined, tactile sensing tests on each sample were conducted. The fabricated ultrasonic tactile sensor was fixed to the texture

analyzer that functioned as a Z-stage (1um resolution) with force feedback (5 kgf capacity with 0.1 gf sensitivity). Using this setup, a uniform compressive force of 20 gf was applied to the samples. The ultrasonic sweep signals were produced by the impedance analyzer. The impedance vs. frequency and phase angle vs. frequency data were recorded. The driving AC signal level was set to 1 Vp-p. Frequency sweep range was from 39 kHz to 41 kHz, and the number of measurement points was set to the maximum (401 points), which resulted in the frequency resolution of around 5 Hz. The elapsed time for each sweep was about 1 min. For each sample, tactile sensing was performed at six marked points, as illustrated in Figure 3.10. For each test point, five consecutive frequency sweeps were conducted with the impedance analyzer. The contact force was released and re-applied before each sweep to ensure the independence of each sweep test.

After the tactile sensing test at each test point, an indentation test was conducted at the same point without applying ultrasonic vibration to collect the relationship between the applied load and deformation. The indentation rate was set to 0.2 mm/s, the indentation depth was adjusted according to the stiffness of the sample to ensure the maximum force applied during the tests being > 22 gf. The calibration value (no-load condition) measurement was done intermittently throughout the whole test process with a minimum interval of 2 hours. Three electrical measurements in total were taken to derive the calibration values.

3.5 Results and Analyses

3.5.1 Mechanical Characteristics

In the mechanical characteristic test, the auxiliary transfer function (ratio between output voltage and auxiliary input voltage) was recorded by the control software of the ultrasonic power source. Combined with the calibration information from the laser Doppler vibrometer controller box, the transfer function could be converted into the ratio between the vibration magnitude (in [m]) and the input AC voltage (in [V]). Data collected from the experiments are plotted in Figure 3.12(a) and the amplification ratio (tip/back) derived from Figure 3.12(a) is plotted in Figure 3.12(b).

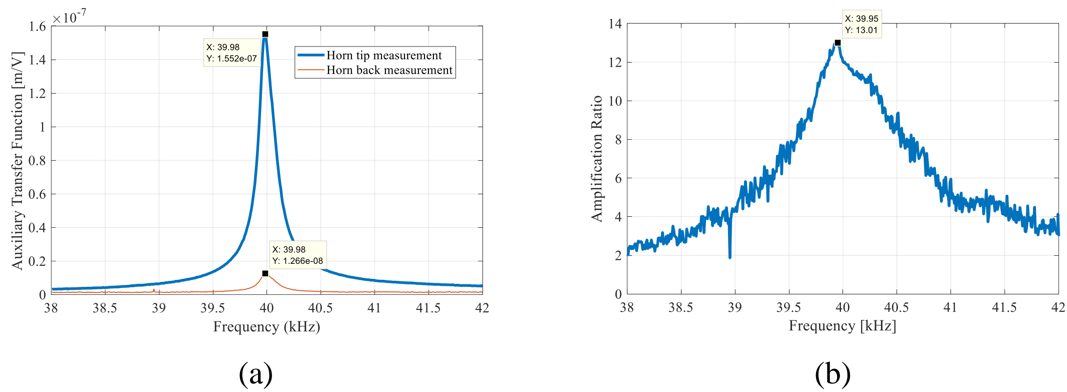


Figure 3.12: Mechanical characteristics: (a) auxiliary transfer function at the front tip and back end; (b) the amplification ratio of the vibration concentrator.

Figure 3.12(a) presents that the system had a clear mechanical resonance at 39.98 kHz. Amplification ratio shown in Figure 3.12(b) followed a similar trend, with a peak value of 13.01 at 39.95 kHz. The results of analytical calculation, numerical FEA, and the experiment are summarized in Table 3.2. According to analytical method, the resonance frequency was designed at 40 kHz with an amplification ratio being higher than 7.2. Refined model from FEA was deliberately tuned to have a ~600 Hz higher resonance frequency than the design target to compensate for the overestimation of the structural stiffness in FEA calculations. Resonance frequency acquired in the experiment was ~0.1% lower than the design target.

Table 3.2: Comparison of the results

Method	Resonance Frequency (kHz)	Amplification Ratio
Analytical	40.00	> 7.2
Numerical	40.61	11.2
Experimental	39.95	13.0

3.5.2 Electrical Characteristics

In the electrical characteristic tests, different frequency sweep range was chosen for the case with and without the concentrator. The test results are shown in the impedance response plot (Figure 3.13(a)) and phase angle response plot (Figure 3.13(b)).

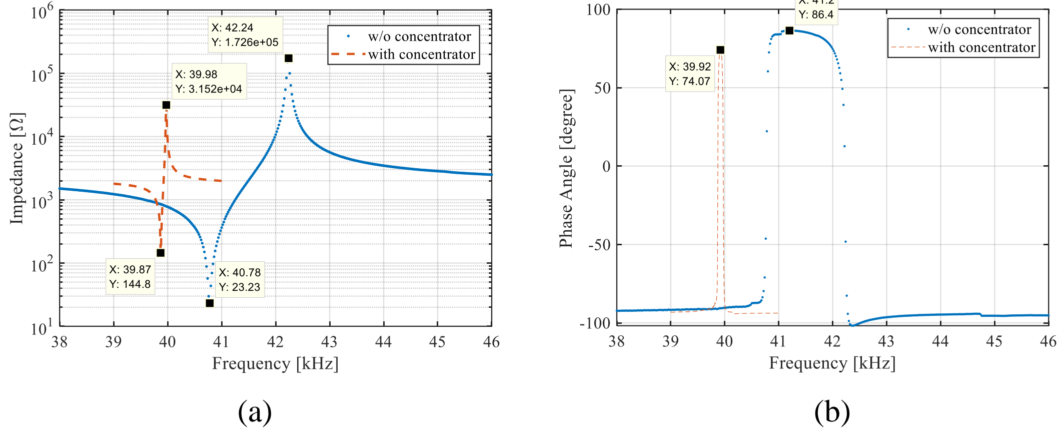


Figure 3.13: Electrical characteristics: (a) impedance responses; (b) phase angle responses.

In Figure 3.13(a), the series resonance point (f_1 in Figure 2.6) and the parallel resonance point (f_2 in Figure 2.6) diverged by ~1500 Hz without the concentrator with $f_1 = 40.78$ kHz and $f_2 = 42.24$ kHz; but when the concentrator was attached, they converged at 40 kHz with only a small gap of ~110 Hz ($f_1 = 39.87$ kHz and $f_2 = 39.98$ kHz). The corresponding phase angle plot in Figure 3.13(b) also showed similar behavior. In the case without a concentrator, a plateau-style response was generated; however, when the concentrator was attached to the transducer, a spike-style response was produced with two zero phase angle points almost coinciding each other (diverged by ~100 Hz) at ~39.9 kHz, which made the maximum phase angle frequency ($f_{m\phi}$) moved close to 39.92 kHz. These changes indicate that the designed concentrator improved frequency selectivity, and hence Q_m increased. However, the decrease in the range of the y axis values (the difference between the maximum and the minimum y values) in both plots for the cases with the concentrator also suggests that mechanical loss increased due to concentrator, which is an adverse effect brought by adding more mass to the system. Applying the BVD model (Figure 2.5) and the regression method discussed in Section 3.3, equivalent electrical parameters can be extracted. Q_m from both cases were calculated using (2.46). The results were presented in Table 3.3.

Table 3.3: Electrical parameters of the equivalent circuit based on BVD model

Parameters	without concentrator	with concentrator
C_p (pF)	1,865	2,095
R_m (Ω)	23.04	102.2
C_m (pF)	136.1	10.01
L_m (mH)	111.9	1,590
Q_m	1,244	3,896

Although the increase in R_m (represents the mechanical loss) had negative effect on Q_m, the influences from the frequency related components (C_m and L_m) were dominant, resulting in significant increase of Q_m by more than 3 times. Therefore, it can be concluded that the vibration concentrator fulfilled its design purpose to increase the frequency selectivity and quality factor of the sensing device.

3.5.3 Tactile Sensing Performance

There are 30 frequency sweep data associated with each sample (6 points per each sample x 5 sweeps per each point). Mean values of them with error bars (indicating standard error) are presented in Figure 10. In the impedance spectrum (Figure 3.14(a)), the impedance range (difference between Z_s and Z_p) became larger and the resonance frequencies shifted to the right as the sample stiffness increased. In the phase angle response (Figure 3.14(b)), the phase range and the resonance frequency followed the same trend as the impedance response. To quantitatively evaluate the results, frequency shifts were determined from Figure 3.14(a), and equivalent electrical parameters were derived with the method in Section 2.1.2 according to Figure 2.5. Table 3.4 presents the mean values and the associated coefficient of variation (CV) in parentheses of all data for each sample derived from the impedance vs. frequency curves in Figure 3.14(a). The last column in Table 3.4 gives the calibration values from no-load (NL) condition.

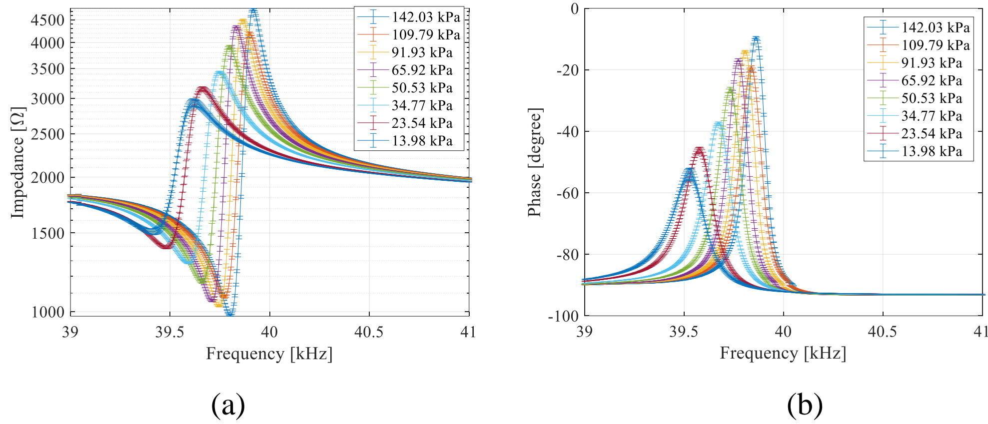


Figure 3.14: Sensing results: (a) impedance response; (b) phase response.

Table 3.4: Electrically determined parameters in tactile sensing tests (CV %)

Sample #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**NL**
Elastic modulus: determined from the compression tests									
E [kPa]	142.0 (0.28)	109.8 (0.13)	91.93 (0.55)	65.92 (0.83)	50.53 (0.79)	34.76 (1.95)	23.54 (1.80)	13.98 (0.31)	N/A
Measured frequency parameters									
f_1 [kHz]	39.82 (0.01)	39.79 (0.01)	39.77 (0.01)	39.73 (0.01)	39.68 (0.04)	39.60 (0.01)	39.49 (0.05)	39.41 (0.13)	39.93 (0.02)
f_2 [kHz]	39.92 (0.00)	39.91 (0.01)	39.87 (0.01)	39.84 (0.01)	39.80 (0.03)	39.74 (0.01)	39.66 (0.02)	39.63 (0.05)	40.00 (0.00)
$f_{m\phi}$ [kHz]	39.86 (0.01)	39.84 (0.01)	39.81 (0.01)	39.77 (0.01)	39.73 (0.02)	39.67 (0.01)	39.58 (0.03)	39.52 (0.04)	39.98 (0.02)
Equivalent electrical parameters									
C_p [pF]	2,047 (0.03)	2,048 (0.06)	2,049 (0.03)	2,051 (0.05)	2,043 (0.30)	2,036 (0.08)	2,036 (0.10)	2,030 (0.35)	2038 (0.31)
R_m [Ω]	1,014 (3.29)	1,216 (6.62)	1,103 (1.90)	1,164 (4.05)	1,349 (4.25)	1,693 (4.97)	2,108 (15.0)	2,801 (33.4)	450.0 (1.62)
C_m [pF]	7.396 (0.18)	7.356 (0.18)	7.328 (0.09)	7.292 (0.09)	7.332 (0.70)	7.328 (0.37)	7.195 (1.22)	6.998 (2.96)	8.123 (0.30)
L_m [mH]	2,158 (0.19)	2,172 (0.17)	2,184 (0.08)	2,198 (0.20)	2,192 (0.64)	2,200 (0.37)	2,252 (1.27)	2,323 (3.01)	1955 (0.27)

As mentioned above, the shifts of mechanical resonance frequencies have been used to estimate the stiffness of soft material. The results in Table 3.4 present that both electrical

resonance frequencies (f_1 and f_2) and the electrically determined maximum phase angle frequency ($f_{m\phi}$) have positive correlation with E of the samples. Furthermore, the frequency results are robust, because the CVs associated with frequencies are mostly less than 0.05% except one (Sample #8: 0.13% for f_1). On the other hand, Table 3.4 also suggests that the electrical parameters of the equivalent circuit diagram (Figure 2.5) can be correlated with the E for the samples from #4 to #8, where E is relatively low.

3.6 Discussions for Indicators of Elastic Modulus

3.6.1 Frequency Shifts vs. Elastic Modulus

According to [53], the relationship for the frequency shift can be found as $\Delta f \propto \rho E^{-1} F$, where Δf is the shift of mechanical resonance frequency. On the other hand, the equivalent circuit theory suggests that series resonance frequency f_1 should be very close to the mechanical resonance frequency. Therefore, it is worth investigating if Δf_1 also follow the similar trend as Δf. Since contact force was controlled to be 20 gf for all tests, the relationship for Δf_1 can be established as $\frac{\rho}{\Delta f_1} \propto E$, as plotted in Figure 3.15(a), which shows linear relationship with $R^2 = 0.9978$. According to Table 3.4, parallel resonance frequency f_2 has smaller standard errors than f_1, especially for the two softest samples. Therefore, the same procedures were attempted on Δf_2 to see if it also has the similar trend as Δf. Figure 3.15(b) indeed shows that $\frac{\rho}{\Delta f_2}$ has the linear relationship with E, although the linearity is a little degraded ($R^2 = 0.9848$). If the maximum phase angle frequency $f_{m\phi}$ is considered in the same manner, $\frac{\rho}{f_{m\phi}}$ also has the linear relationship with E ($R^2 = 0.9966$), as shown in Figure 3.15(c). However, according to Table 3.4, the absolute changes in the measured frequencies (f_1, f_2, and $f_{m\phi}$) were less than 1.2% with respect to the NL condition values. These small changes are accounted for the vibration characteristics of the sensor dominated by its metallic structure. When the sensor is applied to soft objects with low E (in the order of kPa), metallic structure is much stiffer (in the order of GPa), resulting in very small change in overall stiffness and mechanical vibration characteristics.

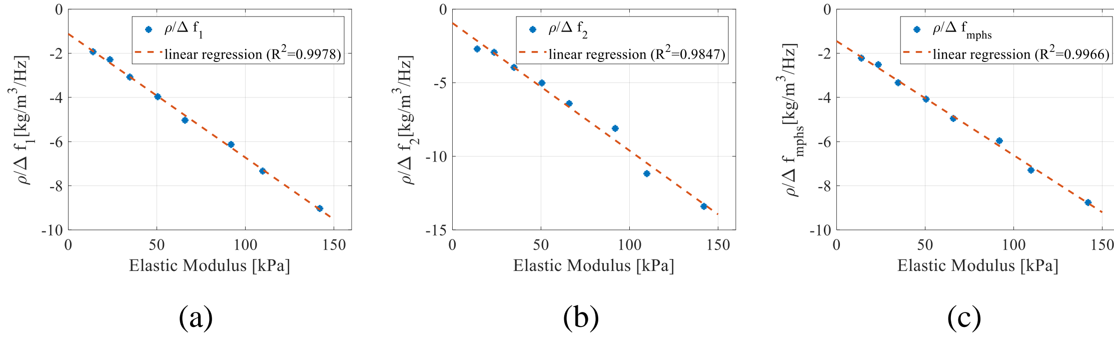


Figure 3.15: Linear regression analyses of the electrical frequency shift derived from tactile sensing data: (a) $\frac{\rho}{\Delta f_1}$ vs E, and (b) $\frac{\rho}{\Delta f_2}$ vs E, and (c) $\frac{\rho}{\Delta f_{m\phi}}$ vs E.

3.6.2 Equivalent Conductance vs. Elastic Modulus

As described in Section 3.3, The electrical characteristics of the vibro-tactile sensor can be determined from NL cases in Table 3.4. Then, the equivalent resistance of the load R_{load} for each sample can be determined by using (3.6) with the loaded case data in Table 3.4. If V is controlled to be constant, the voltage over the equivalent circuit of the lumped load will remain unchanged. Then, I, the contact force (F) in mechanical domain, should be linearly proportional to the reciprocal of the resistance of the load (i.e., conductance G_{load}) at resonance as

$$I \Leftrightarrow F \propto \frac{1}{R_{load}} = G_{load} \tag{3.7}$$

Force F can be split into the static contact load and the dynamic load from vibrations. The static load was constant in all tests, so that it merely caused a vertical shift of linear relationship. On the other hand, the dynamic load was responsible for the linear behavior. From the indentation tests described in Section 3.4.3, it was found that the force and displacement showed linear relationship with R^2 over 0.9945 within the tested load range (18 gf ~ 22 gf). Then, the slope of the force-displacement curve (k) at selected range around 20 gf contact force can be determined. Along with the voltage-displacement transfer function at tip end (A) and the supplied voltage (V), the amplitude of the dynamic force can be expressed as

$$\left|\tilde{F}\right| = kAV \tag{3.8}$$

Since A and V are parameters governed by the sensor system, k is derived from the sensing operations and can establish a direct link to E. Hence, a regression analysis was performed between k and E, and the linear relationship was found with $R^2 = 0.9967$ as shown in Figure 3.16, i.e., $k \propto E$.

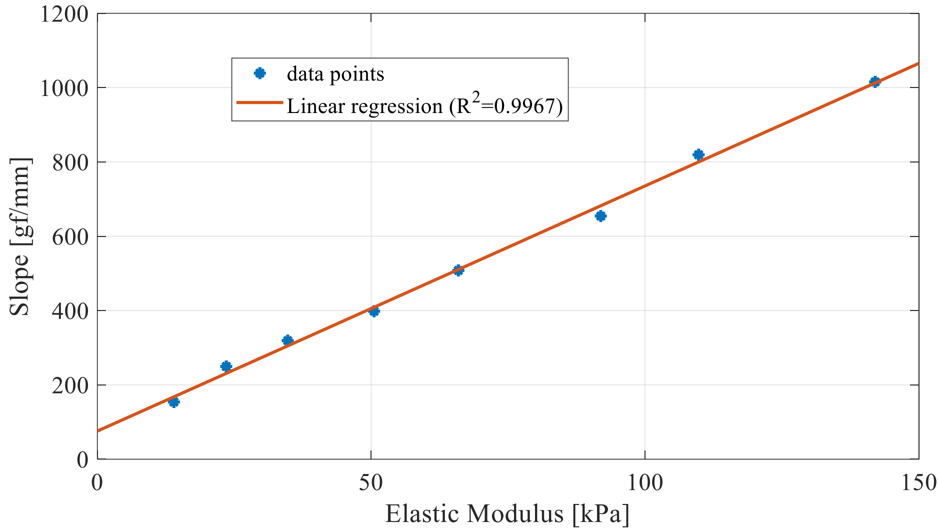


Figure 3.16: Linearity between the slope and elastic modulus of the samples.

As for A and V, they are parameters that determine the dynamic displacement. The sensor's capability of producing the dynamic displacement is directly related to the loading condition of the piezoelectric material. It can be evaluated from the variation of C_p, which is the clamped capacitance determined by curve fit in this isolated vibration mode. Figure 3.17 shows that C_p has a linear relationship ($R^2 = 0.9611$) with E for the soft samples with E up to 70 kPa (sample# 4 to 8). Beyond that range, the piezoelectric device cannot produce more power to generate enough displacement to maintain the linearity, as the driving voltage of 1 Vrms is too low. Therefore, combining all the information gathered from k, A, and V, the linear relationship between the conductance (G_{load}) and E of the sample can be established as $G_{load} \propto E$ for the samples with E less than 70 kPa (sample # 4 to 8) as in Figure 3.18. As expected, linearity ceased to be held beyond that range (sample #1 to #4). Comparing R^2 for

linearity in the range below 70 kPa (sample # 4 to #8), G_{load} arguably has a better linearity ($R^2 = 0.9998$) than frequency related parameters.

However, the above consideration also indicated that equivalent electrical parameters have the limitation that their linear relationships with E are expressed only in the valid sensing range specific to each piezoelectric device. Therefore, the valid range should be carefully estimated prior to the sensing application. To extend the range, a more efficient piezoelectric transducer or higher voltage input are required.

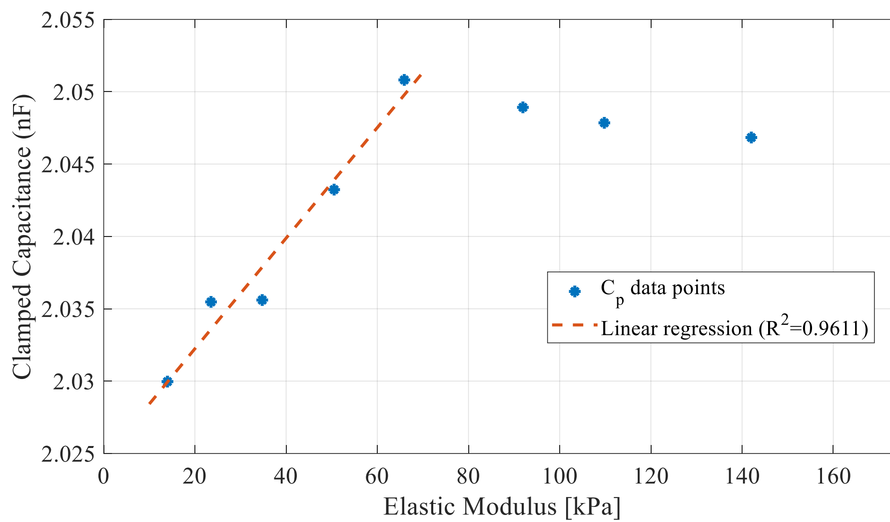


Figure 3.17: Relationship between C_p and E.

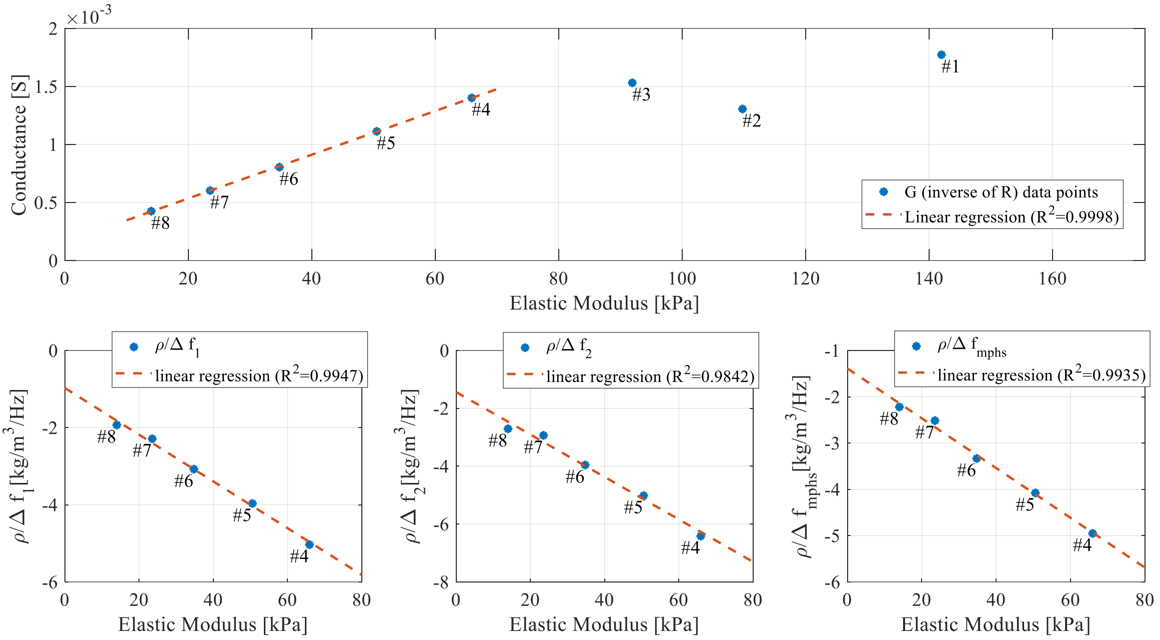


Figure 3.18: Linear regression within sample # 4 to 8 of the derived values: G_{load} vs. E, $\frac{\rho}{\Delta f_1}$ vs. E, $\frac{\rho}{\Delta f_2}$ vs. E, and $\frac{\rho}{\Delta f_{m\phi}}$ vs. E.

3.7 Conclusions

By using a hybrid design approach, an ultrasonic vibration concentrator was designed to enhance the performance of the sensor, and its design competency was verified by mechanical and electrical characteristic tests. By integrating the ultrasonic vibration concentrator into the system, the gap between the series resonance and parallel resonance frequencies was reduced from 1500 Hz to 90 Hz, which enabled the identification of the mechanical resonance frequency (located between two electrical resonance frequencies) more obvious and direct. This also led to the increase of the quality factor (Q_m) from 1,244 to 3,896, leading to the increase of frequency selectivity.

In the tactile sensing experiment, the electrically derived frequency shifts were robust (CV: coefficient of variation < 0.05% in most measurements) and applicable to the full sensing range available with the current samples (10 kPa to 140 kPa). The derived equivalent conductance of the load G_{load}, on the other hand, exhibited better linearity ($R^2 = 0.9998$)

than series resonance frequency shift Δf_1 ($R^2 = 0.9947$), parallel resonance frequency shift Δf_2 ($R^2 = 0.9842$), and the maximum phase angle frequency shift $\Delta f_{m\phi}$ ($R^2 = 0.9935$), in the valid sensing range (10 kPa and 70 kPa). However, the valid range needs to be carefully estimated for each piezoelectric device prior to the measurement test.

All electrical resonance frequency shifts have the potential of being directly adopted as the stiffness indicator for soft materials whose elastic modulus (E) is between 10 kPa and 70 kPa when the transducer was driven at 1 Vrms. However, it can be inferred from the reciprocal expression found in the linearity and the steep slope of the transfer function near mechanical resonance that the signal to noise ratio may be a problem when the resultant resonance frequency is getting closer to the mechanical resonance frequency at no load condition (i.e., when the frequency shift is approaching zero). The absolute value change in series resonance frequency shift was small (1% compared to reference value), but the CV values associated exhibited its robustness; while the equivalent conductance of the load, although had a larger change in its absolute values (can be more than 6 times as the reference value), was less robust, as suggested by its larger CV value (generally > 1.5%, and in some case spiked up to 33%).

In summary, the vibro-tactile sensor can identify the elastic modulus (E) of soft materials in a non-destructive manner in lab environment. However, the manipulation of the sensor should be carefully designed to ensure load conditions applied properly. Moreover, the absolute change in indicator values (for frequencies) and the large CV values (for electrical parameters) both shadowed the sensitivity advantage in vibration characteristics. Therefore, the vibro-tactile sensor developed is theoretically applicable to the measurement, but it requires further refinement and development to be practical in real applications.

Chapter 4
FPGA-based Versatile Research Platform

4.1 Introduction

4.1.1 Development Scope

There are two main objectives in the development of FPGA based ultrasonic system, the hardware engineering and the corresponding software development. Both should be addressed to reach a working prototype.

In hardware engineering, there were five key components. They were a DC high-voltage (HV) power source, an ultrasonic probe, an analog front end (AFE), an analog to digital interface (ADC), and a controller based on an SoC FPGA. Further, the hardware can be separated into analog and digital parts. The HV power source, ultrasonic probes, and AFE formed the analog part of the hardware. The HV power source used in this project is TENMA 72-8700A, a dual channel lab power source that can provide DC voltage up to ~32V/channel. Technically, it cannot be regarded as HV, but it allowed research to carry on and was enough to generate meaningful data in this project. As for probes, the system is supposed to work with generic ultrasonic probes with specified working frequencies. Therefore, standard probes (P2.5-20L and P10-10L) commercially available from SIUI (Shantou, China) were used in this research. The AFE used in the project was developed from scratch through a complete process of designing and making a prototype PCB. It is worth mentioning that the open-source ultrasound project [132] by Columbia University was very inspiring at the beginning stage of the development. Multiple iterations were taken to reach the working prototype, but only the final version is presented in this thesis. The details on the circuit design are presented in the following sections so that people with limited electric engineering background can use them as a reference to fabricate a working prototype.

For the digital part, commercially available FPGA development board (DE10-Standard) and its AD/DA interface daughter card (THDB-ADA) were employed. Both boards are from Terasic Technologies (Taiwan, China). Since an FPGA was used, the digital circuit part did

not require repetitive manufacturing processes. The FPGA can be programmed into different digital circuits with HDL. In this project, Verilog HDL was used. Other than building basic functions for the pulse-echo signal generating and receiving, a simple pulse detection algorithm was developed and implemented in the FPGA. This part of hardware definition was to demonstrate the capability of direct data processing using hardware logics. Since the algorithm was implemented with HDL codes, the algorithm can be altered to fulfill other tasks as well. If on-board resource allows, artificial intelligence technique can also be implemented with proper coding and fully exploit the inherent parallelism of FPGA. Thanks to the flexibility of FPGA and its hard-embedded SoC with an operating system, the configuration for the algorithm implementation can happen in field at ease.

In software development, the program was coded in C language. It was supposed to run on Linux installed on the SoC powered by an ARM processor. It aimed to provide a user-interface, which included display output for users to preview the data, data saving functions on users' requests, and data transferring capabilities.

4.1.2 DE10-Standard and THDB-ADA

As mentioned in the previous section, a DE10-Standard development board (Terasic Technologies) was chosen as the FPGA-SoC hardware platform for the project. This board is a part of the Intel University Program [133], which is supposed to be educational-friendly, i.e., tutorials and supporting documents are provided as teaching materials to allow beginner-level users to start the development smoothly. The choice of the FPGA also resulted in the following HDL development platform to be on the development suite (Quartus Prime) provided by Intel.

The detailed model of FPGA for the core of the development board is Intel's Cyclone V SoC FPGA. Other than the FPGA, it provides a hard implemented 925 MHz dual core ARM Cortex A9 MPCore processor. Therefore, the core of the chip is divided into two parts: the FPGA and hard processor system (HPS). As a development toolkit, numerous peripherals and I/O ports are provided by factory settings. The basic system block diagram is shown in Figure 4.1, which summarizes all the peripherals available. As indicated by the diagram, the

physical connections to the peripherals are managed by the FPGA and HPS side separately. These connections are hard-wired and thus not configurable. Although not directly wired, the peripheral from both sides can be visited by either device through the interconnections defined with a graphical programming language in the development suite. This matter will be covered in Section 4.3.4 when describing the system interconnection design. The layout of the DE10-Standard can be reviewed in Figure 4.2.

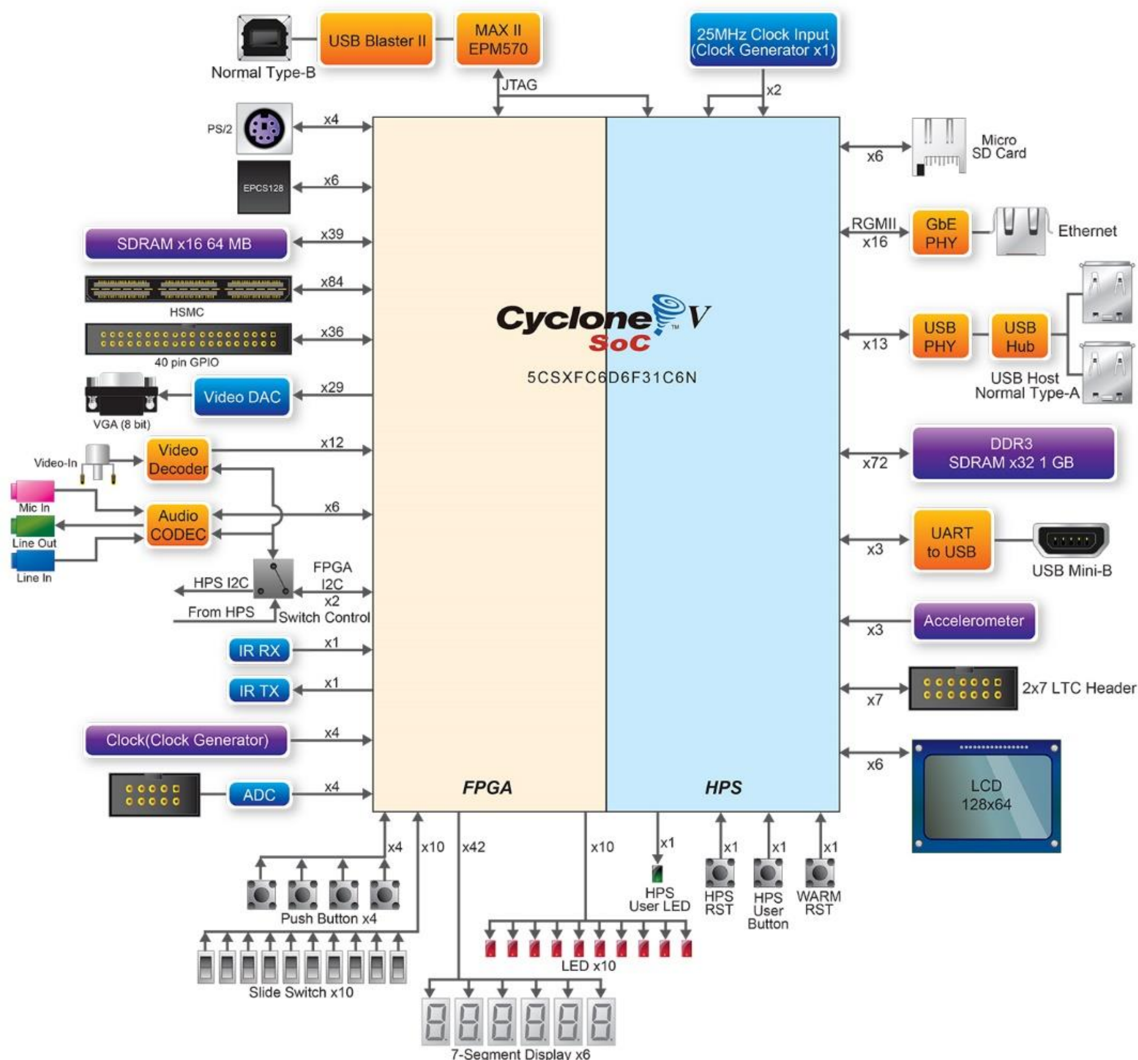


Figure 4.1: Block diagram of Cyclone V SoC [134].

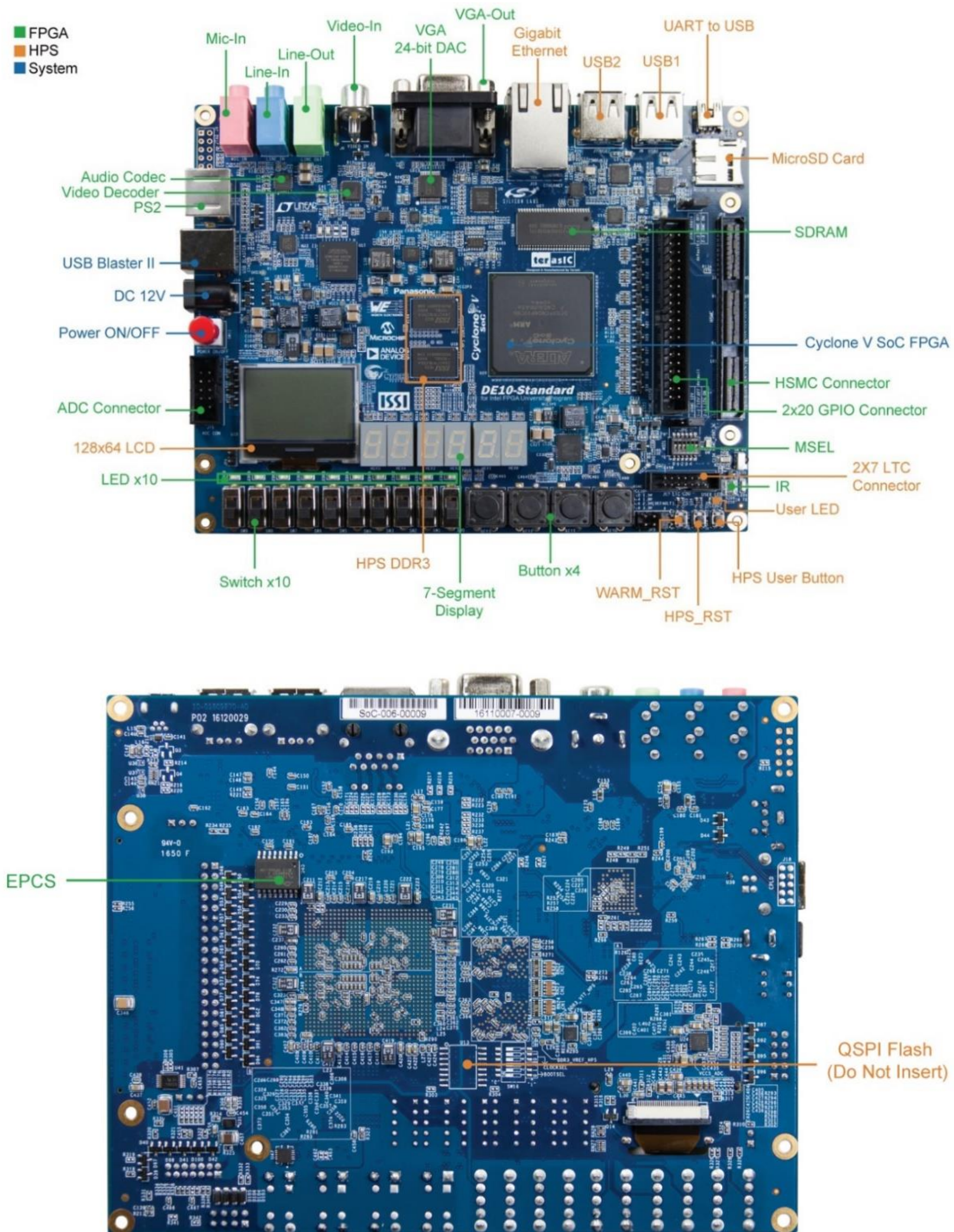


Figure 4.2: Layout of the DE10-Standard: the peripheral directly connected to the HPS is marked in orange and the peripherals directly connected to FPGA is shown in green [134].

Note that there is an HSMC connector available in the DE10-Standard. HSMC stands for Altera High Speed Mezzanine Card interface. Through this interface, the AD/DA interface daughter card, THDB-ADA (Figure 4.3), can be attached.

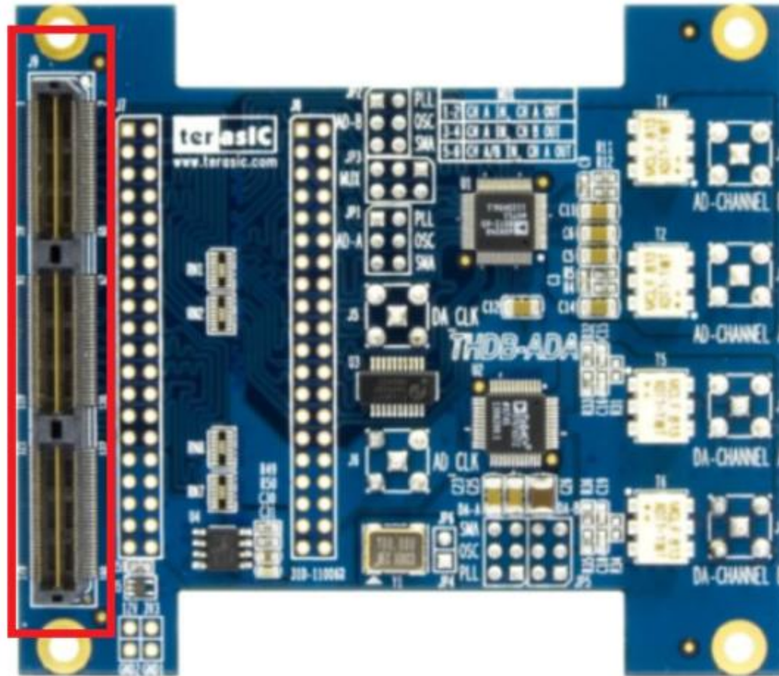


Figure 4.3: THDB-ADA (HSMC connector marked out in red) [135].

THDB-ADA is also developed by Terasic Technologies to expand the AD/DA capability of the development kit. It should be noted that the original DE10-Standard has its own ADCs and DACs (as indicated in Figure 4.1). Although eight ADC channels with 12-bit precision are implemented on the DE10-Standard, the sampling rate of these ADCs are too slow (500KSamples/S) for this project [134]. THDB-ADA, on the other hand, supports only two AD channels and two DA channels, but it supports AD conversion rate up to 65 MSamples/s with 14-bit precision. Based on the Nyquist sampling theorem, this sampling frequency can preserve frequency components up to 32.5 MHz, which is enough with respect to the probes' working frequency (2.5 MHz and 10 MHz) if only primary pulses are to be detected. Since at this moment only one AD channel is required, THDB-ADA can satisfy the need. The input

voltage range for its ADC is 2V p-p, and DC signaling is not supported [135]. Therefore, the voltage resolution is $2\mathrm{V}/(2^{14}-1)=0.122\ \mathrm{mV}$.

If a development board from Terasic Technologies is used, a software toolbox called "System Builder" is useful. The "System Builder" is board specific. Its user interface is shown in Figure 4.4. The "System Builder" is used to create a top-level module with pin assignments established. The related peripherals can be selected from the user interface and the builder will generate the HDL files as per request. In this project, the GPIO headers were initialized for the pulse signals to AFE and the HSMC header was also activated for THDB-ADA board ("ADA – High Speed ADC/DAC" in Figure 4.4). The pin assignments are generated inside the "*.qsf" file. An SDC file contains all the timing constraints that are related to the selected modules is also generated. Since it is not necessary to use these specific files generated by the System Builder, users can generate a full-scale system and copy the necessary code segments to the active project files.

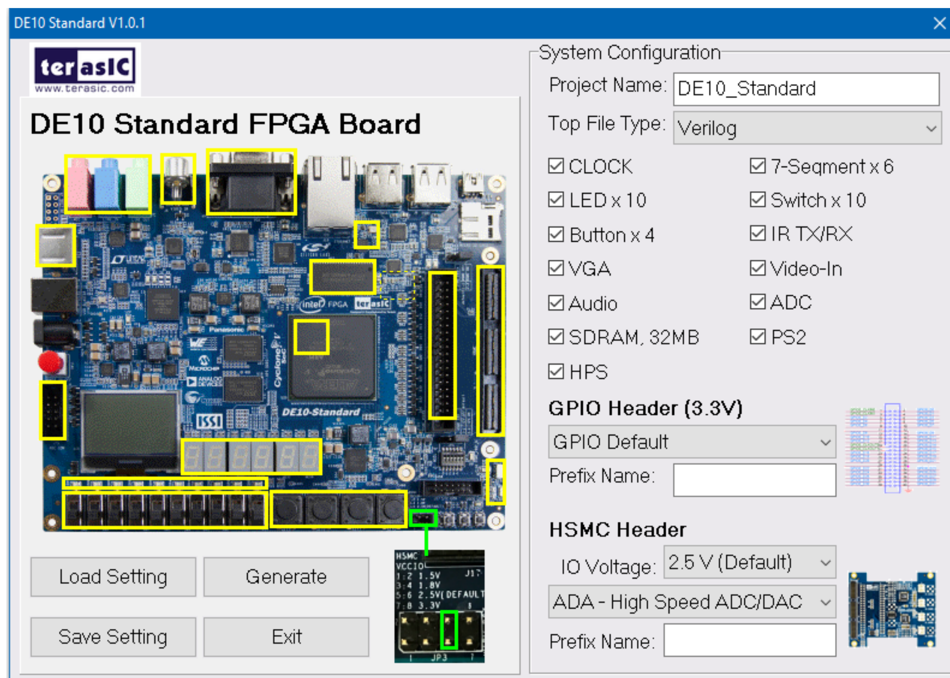


Figure 4.4: User interface of DE10-Standard System Builder (Note that the GPIO and HSMC headers are initialized).

More specification details for DE10-Standard and THDB-ADA can be found in the datasheets [134,135]. By choosing both commercial boards, the efforts to develop the AD interface and digital controller could be saved. But the FPGA still needed to be programmed to fulfill the tasks.

4.2 Analog Front End

No commercially available AFE board was available for this project. Therefore, the development for AFE started with the basic circuit design. Once the design was finished, the layout file was sent to an online based manufacture OSHPARK (USA) to make the prototype PCBs. All the electronic components were soldered by hand when the PCBs were received. The full electrical schematic can be found in Appendix J, and the bill of materials (BOM) list is in Appendix K.

4.2.1 Circuit Design

The AFE design plays a very important rule as it can greatly affect the signal quality. In this section, the circuit design will be explained. The technical specifications for all the components can be found in the corresponding datasheet.

4.2.1.1 Power Regulation Circuit

There are two main power sources to the board. One is the main power supply (12V) from the barrel jack (J2) to power up various ICs and circuits, and the other is the positive (VPP) and negative (VNN) HV inputs through screw connector (J5) to boost the output waveform to the ultrasonic probe. Figure 4.5 shows the schematic of the power regulation circuit.

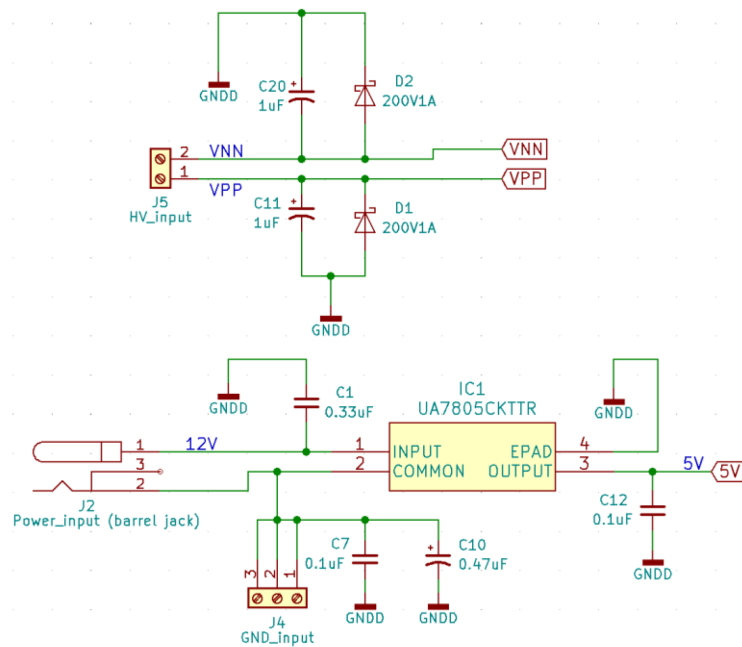


Figure 4.5: Power regulation circuits for AFE.

The barrel jack pairs with common 12V AC/DC power adaptor (2.1 mm x 5.5 mm). The VPP and VNN are supplied with lead wires connecting to the TENMA 72-8700A. The screw connector J4 provides terminals for proper grounding. The additional ports provided by J4 can be used to provide ground for analog circuit diagnosis.

The 12V input is fed into the voltage regulator UA7805CKTTR to get a regulated 5V voltage source for the rest of the circuits. Since the powering circuit deals with DC inputs, the C1, C7, C10, C11, C12, and C20 are all bypass capacitors or decoupling capacitors to counter the trace inductance and filter out the AC noise within the circuit. The values are chosen based on recommendations in the datasheet. The Schottky diodes, D1 and D2, are implemented to provide protection to reverse voltages.

4.2.1.2 Pulse Generation Circuit

The pulse generation circuit is demonstrated in Figure 4.6. The concept of pulsing in this AFE uses the MOSFET switch. The HV pulses are generated by activating the MOSFET gates at right frequencies. The low voltage (LV) high frequency signals can be amplified to a

reasonable amplitude (the same as externally provided VNN and VPP). Therefore, the MOSFET controller needs to be able to keep up with the frequency of the application. Since negative and positive gate are separate, to satisfy the need of driving a 10MHz probe, the gate switching time should be less than 500ns, which is very generous for most of the MOSFET gates designed for high frequency applications.

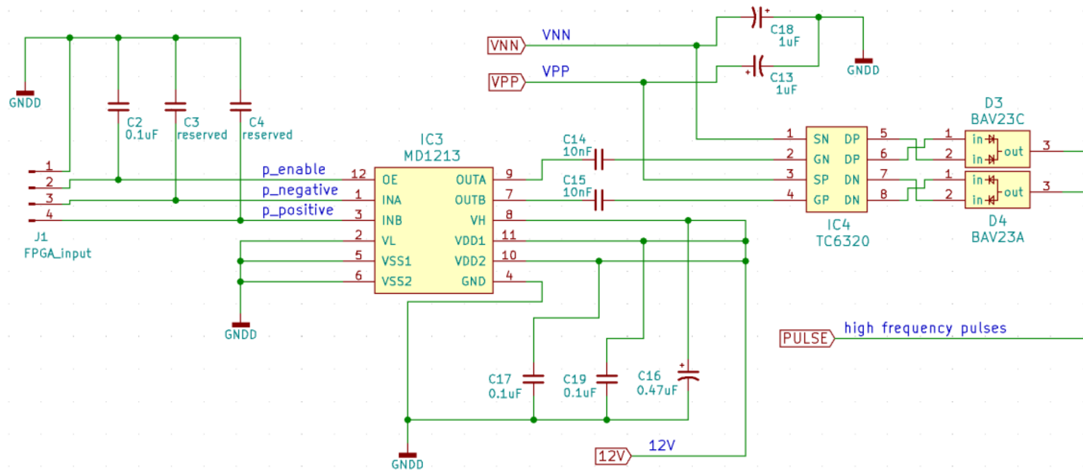


Figure 4.6: Pulse generation circuits for AFE.

In this design, MD1213, a dual channel MOSFET driving IC with 6ns in rise and fall time (1000 pF load) [136], is introduced to provide positive and negative gate activation. The input incidence pulses (p_negative and p_postive) come from GPIO pins of the FPGA. The FPGA GPIO pins work at 3.3V (as is shown in Figure 4.4) for digital high, which is within the voltage range (1.8V ~ 5V) supported by MD1213. The FPGA board sends in pulse activation signals (p_negative and p_positive) at right intervals via J1 to the MD1213 chip. The p_enable signal also comes from one of the GPIO pins and stays high (3.3V) so that MD1213 is kept operational. The actual MOSFET gates need to support both P-channel and N-channel to provide bi-polar signals. Referencing to the MD1213 datasheet [136], MOSFET pair IC TC6320 was employed. MD1213 activates the MOSFET gates in TC6320 to let HVs (VNN and VPP) pass through.

Because the output pulse is bi-polar, one should always keep an eye on the positive and negative voltage isolation. When either voltage is activated, it should not back flow to the

other side of the circuits, vice versa. Therefore, two diode rectifiers (BAV23C and BAV23A) are implemented. Furthermore, other than the usual decoupling capacitors (C2, C3, C4, C13, C16, C17, C18, C19), there are two essential isolation capacitors (C14 and C15) located between MD1213 and TC6320 to protect the LV circuits from HV DC inputs, meaning that the voltage rating for C14 and C15 should be selected based on the VNN and VPP levels. The drain-to-source breakdown voltages for P and N channel in TC6320 are 200V and -200V respectively. So, if only considering the pulse generation, the maximum voltage should not exceed ±200V.

4.2.1.3 Echo Receiver Circuit

The ultrasonic pulses towards the probe are HV (in the magnitude of 10 or 100 V), but the echo signals coming back from the tranducer are LV (in the magnitude of 0.01 or 0.1 mV). A voltage limiter needs to be implemented so that the HV and LV are isolated. T/R switch MD0100 was selected for easy implementation. It limits the voltage drop across its two terminals (A and B) within ± 2V so that it can allow reflected echo to pass the switch. But it has a limit to the maximum voltage between the terminals. It can withstand ±100V between its terminals [137]. Therefore, MD0100 further limited the voltage of VPP and VNN to ±100V for this design. The other components were added to complete the echo receiver circuit as shown in Figure 4.7.

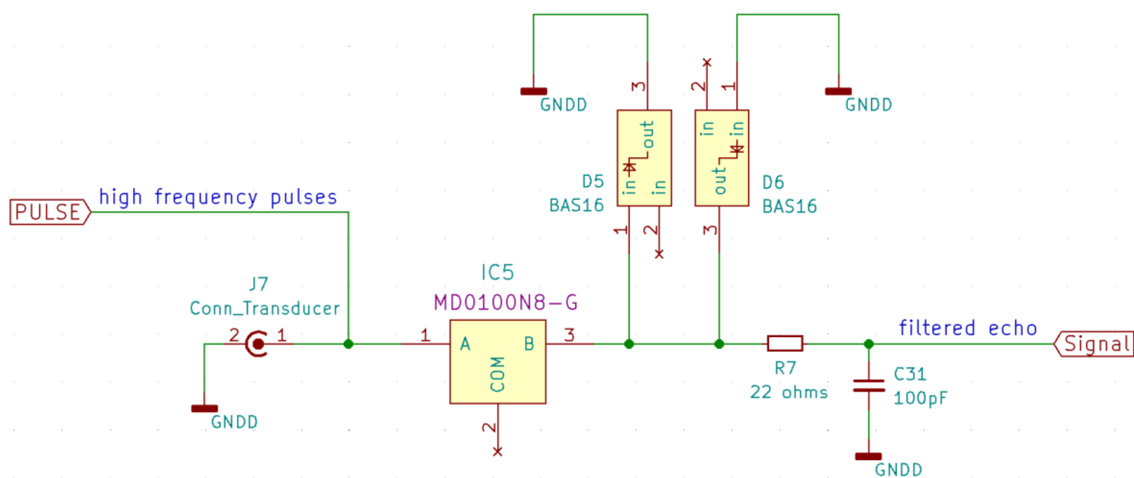


Figure 4.7: T/R switch and low-pass filter circuit for AFE.

The HV high frequency pulses are sent to the BNC connector (J7) which further passes the signal on to the ultrasonic probe. Note that the HV pulses also make their way to the MD0100 through the joint on the left of port A, but they are blocked. When the echo comes back from the transducer to J7, it will be allowed to pass MD0100. The LV echo then go pass two diodes (BAS16) that are facing opposite direction. These two diodes formed a voltage clipper which only allows maximum ± 1.25V (value of their forward voltage V_f) to go pass so that the remaining circuits are protected. Right before the signal is sent to the amplification circuit, it goes through an analog RC low-pass filter built by a series resistor and a bypass capacitor. The values of those two components are determined based on the desired frequency of the low-pass filter. In this design, the low-pass filter works at 72.34 MHz.

4.2.1.4 Post-receiver Amplifier Circuit

There are two ICs concerned in this circuit: AD8331 (Analog Devices) and LTC5507 (Linear Technology). They are the Low-Noise Variable Gain Amplifier (LN/VGA) chip and RF power detector chip, respectively. The schematic shown in Figure 4.8 was developed according to the recommended circuits provided in their datasheets (Figure 96 in [138] for AD8331 and Figure 3 in [139] for LTC5507).

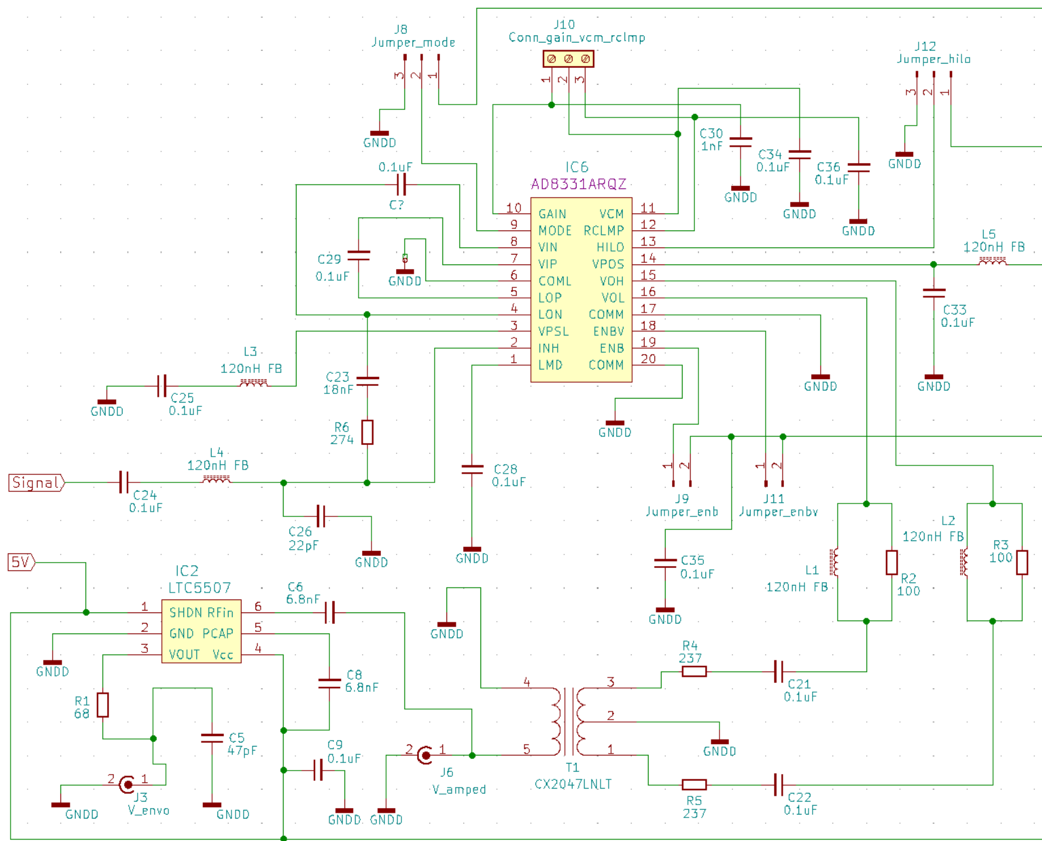
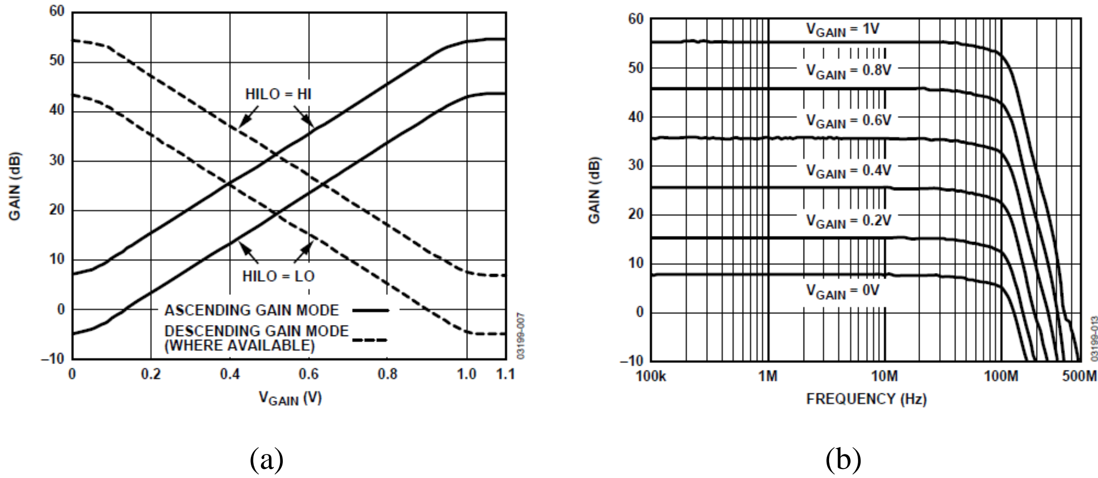


Figure 4.8: Echo amplifier and power detection circuits.

AD8331 chip provides different functional settings based on the inputs to specific pins. These settings can be accessed through the jumper positions at J8, J9, J11, J12, and the screw connector (J10). The functions of these input can be reviewed in the datasheet [138]. Because the purpose of this chip is to amplify the signal, the most important aspect is the amplification ratio that can be provided by the chip. The datasheet [138] provides thorough explanation on the chip's capability. With a quick glance, it can be found that it is possible to acquire ~55 dB gain through the maximum gain setting on the chip (Figure 4.9(a)). The amplification may be limited by working frequency (not until ~100 MHz as shown in Figure 4.9(b)), but it is not a concern in this project. The voltage of the echo can be expected to be raised to ~10 mV in magnitude.



(a) (b)

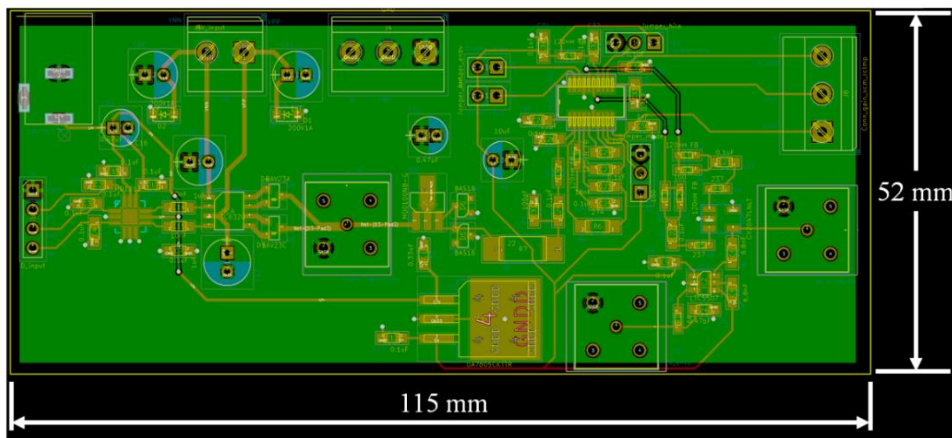
Figure 4.9: Gain settings for AD8331: (a) V_{gain} with different modes (Figure 7 in [138]); (b) Frequency response for the amplification in HI setting (Figure 13 in [138]).

It is common to investigate the envelope of raw RF data. Therefore, an RF power detection chip, LTC5507, was included to provide auxiliary functions on the AFE. In total, there are two outputs from this customized AFE. One is "V_amped" at J6, the other is "V_envo" at J3. The "V_amped" is the amplified echo signal, i.e. the raw RF signal, provided by the LN/VGA, and the "V_envo" is the envelope of the raw RF signal detected by LTC5507.

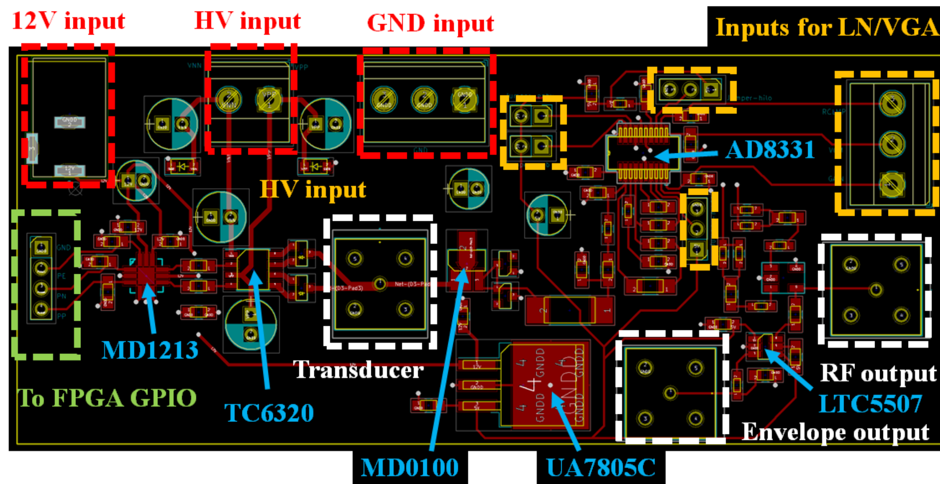
4.2.2 PCB Layout Development

After finalizing the schematics, a PCB layout is designed with selected components. The electrical components' manufacturers usually provide the same unit in different packages. To save the board space and reduce the unnecessary vias, surface-mount technology (SMT) packages are preferred. However, since only hand-soldering is possible with the soldering setup in the lab, some packages smaller than solderable size could not be selected. Also, when assigning the footprint of the components, hand-soldering possibility was a decisive factor. In order to fit all the components, a PCB layout shown in Figure 4.10 was designed. As shown in Figure 4.10(a), the board size is 115mm x 52mm, which is about 1/6 of a size of the DE10-Standard. In Figure 4.10(b), the placement for ICs and their supporting circuits are demonstrated. To minimize the trace length for the high frequency signals, the connection to the ultrasonic transducer is placed in the middle of the board. The electrical connections,

such as the power inputs, and the connections to FPGA GPIO pins are located on the left side of the board. The LN/VGA (AD8331) and the envelope detector (LTC5507) implemented to condition the echo signal before sending out to the receiver are located on the right side of the board. The outputs of the board are placed near the signal conditioners, and thus they are on the right side of the board. All bypass and decouple capacitances are placed as close to the source or sink of the signals as possible or otherwise follow the recommended layout in the specific IC's datasheet and application notes.



(a)



(b)

Figure 4.10: PCB layout of the customized AFE (a) design overview; (b) placement for the most important ICs.

The green-colored background in Figure 4.10 is the ground plane. A complete ground plane can improve the signal to noise ratio by minimizing the loop current, provide shortest return path, and reduce work in planning the ground connections. In order to keep the ground plane as intact as possible, most of the connection tracks were placed on the top layer (Figure 4.11(a)). The orientations and positions of electrical components are also deliberately arranged so that minimum vias and tracks for crossing the electrical planes (i.e., copper layers) are needed. In the cases where plane crossing is inevitable, the routing on the bottom layer (Figure 4.11(b)) has to minimize the crossing under the signal wires to reduce the electro-magnetic interference (EMI) to them. All the RF connectors used on the board are BNC connectors with 50 Ω terminal impedance.

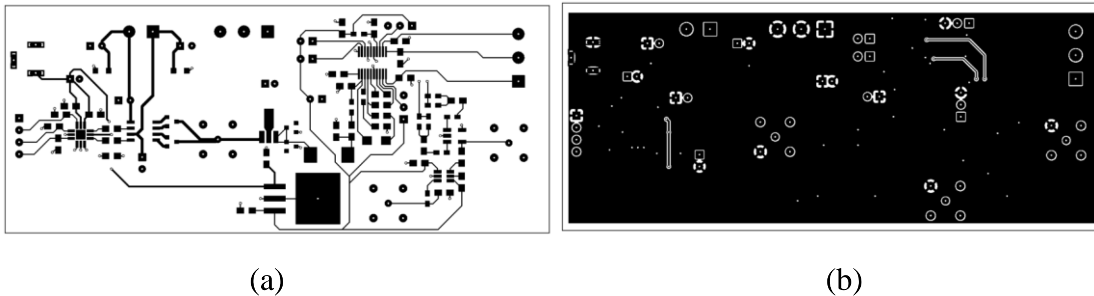


Figure 4.11: Copper layers in the PCB layout: (a) top layer; (b) bottom layer.

The fabricated prototype board is shown in Figure 4.12. The electrical components on the PCB were soldered by hand later. Note that the pin locations in Figure 4.11(b) and Figure 4.12(b) are mirrored because the PCB layout for copper layers in Figure 4.12 are all acquired from top view.

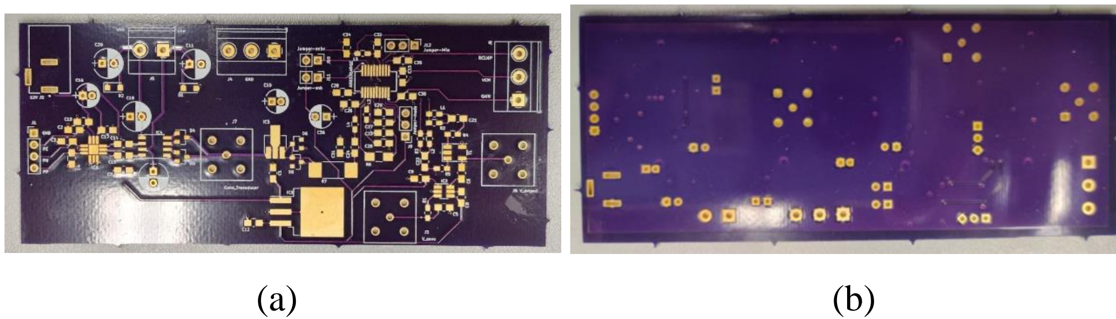


Figure 4.12: PCB prototype manufactured by OSHPARK (USA): (a) top view; (b) bottom view.

4.3 FPGA Based Signal Generator and Processor

As mentioned in Section 4.1.2, DE10-Standard and THDB-ADA were used. In this section, the detailed configuration and development procedures on those two commercial boards are presented.

4.3.1 Board Configuration and Communication

DE10-Standard allows users to program the FPGA with USB-BLASTER II connector through the Programmer tool in Quartus Prime or using the binary file through the ARM-based Linux system on the micro-SD card [134]. In this project, the Linux approach is the most preferred, because Linux can be used later in the software development. Linux is installed on the HPS, which is the SoC part of the Cyclone V. In this configuration, the FPGA works as a peripheral to the HPS. Software codes can be compiled and executed on Linux. A setup procedure identical to the one explained in DE1-SoC tutorial document [140] should be followed in order to allow the HPS to program the FPGA. The MSEL switches on the DE-10 Standard must be configured as in Figure 4.13.

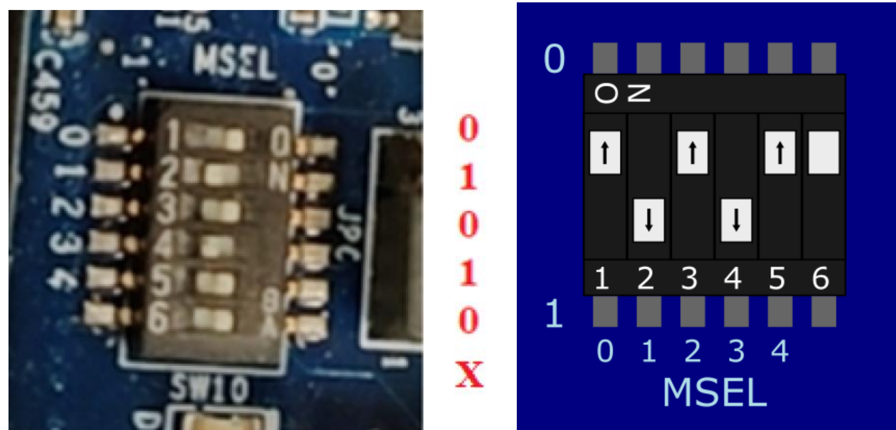


Figure 4.13: Configuration for the MSEL switches of the DE10-Standard to allow ARM program the FPGA (x means don't care).

To boot the Linux on ARM-based HPS, a bootable micro-SD card loaded with suitable Linux distribution should be prepared. After the card is inserted into the micro-SD card adaptor on

the HPS side, when Linux is booted, command line instructions will be used to program the FPGA with the binary programming files.

In order to gain access to the Linux command line from a host machine, the easiest way is to establish a serial communication with UART-to-USB connection (on HPS side) by a freeware called “PuTTY”. A cable is needed to connect the micro USB connector (USB mini-B) on the HPS side and a USB port on the host machine. Then, in PuTTY, as shown in Figure 4.14, under the “Serial” panel, the UART communication should be configured as: baud rate = 115200 bits per second, data bits = 8, stop bits = 1, and parity and flow control = none. The COM port number can be found in the Device Manager on a Windows-based host machine (Figure 4.15). A command line interface will pop-up once the connection is open.

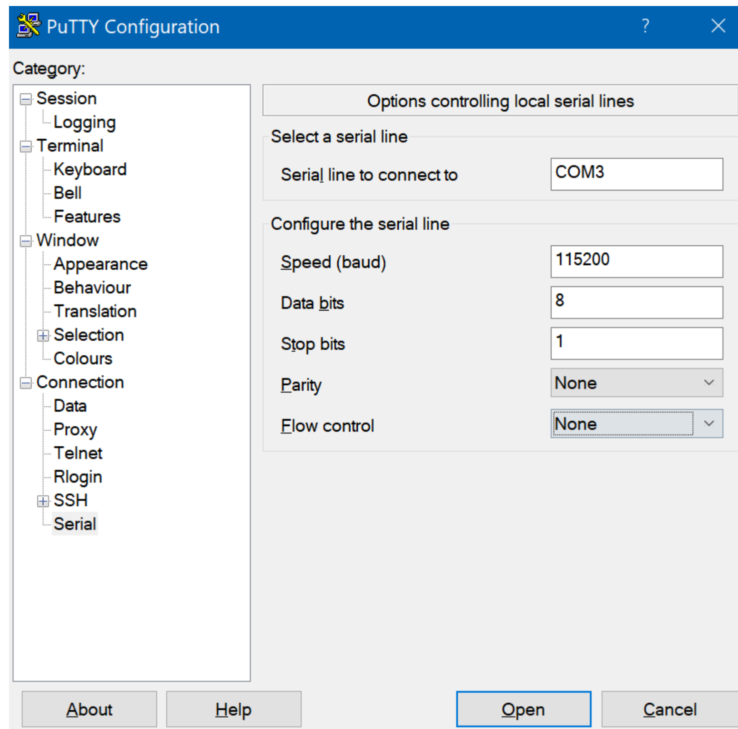


Figure 4.14: PuTTY configurations for serial communication.

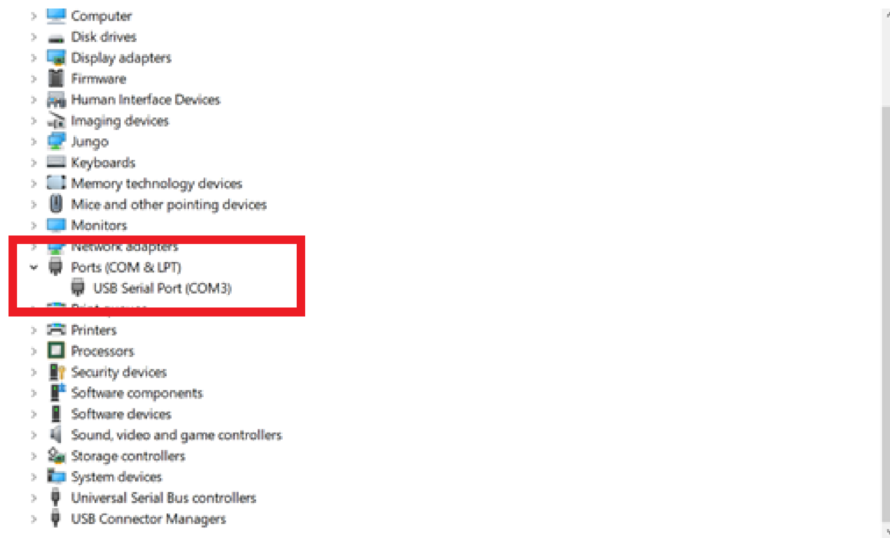


Figure 4.15: Look up for COM port in Device Manager in Windows.

4.3.2 System-level Integration and Working Principle

The system needs acquire the digitized ultrasonic RF signals during the NDT applications; hence, the FPGA is configured based on the signal routes. The system shown in Figure 4.16 was proposed and realized. The signal routes during operation are illustrated and numbered sequentially to provide a full image on how the system works.

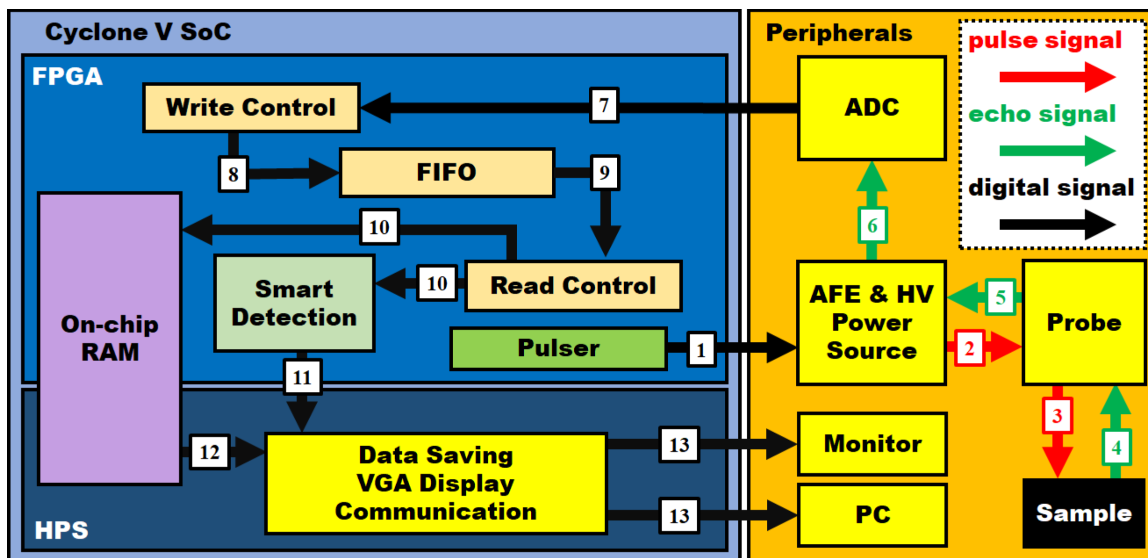


Figure 4.16: Ultrasonic T/R system signal related block diagram and signal routes.

The system diagram in Figure 4.16 is not thorough, because the sample control block in the FPGA and the Parallel I/O (PIO) ports (similar to the GPIO ports) between HPS and FPGA are not shown. The PIO ports are either used to control auxiliary hardware (such as LED, pushbuttons and switches) or transfer control signals between the FPGA and HPS. Therefore, they are crucial to the system but are miscellaneous and not directly concerned with the basic signal paths. For presentation clarity, they are omitted for the moment. The signal paths shown in Figure 4.16 can be interpreted as follows:

1. The pulser block in FPGA gives the activation pulses to the AFE.
2. The AFE sends out HV bi-polar pulses to the ultrasonic probe.
3. The probe converts the electrical energy into the mechanical deformation with its piezoelectric element and emits mechanical waves to the object under test.
4. The echo signal bounces back to the probe, and is converted to electrical disturbances.
5. The AFE extracts the echo signal and amplifies it with ~55 dB gain.
6. The ADC digitizes the amplified signal with 14-bit precision at a rate of 65 Msample/s.
7. The digitized signal is transferred to the FPGA through HSMC connector.
8. The write control block writes the data to the FIFO buffer.
9. The read control block takes the data out of the FIFO buffer.
10. The data is sent to both on-chip RAM for storage and smart detection block for hardware-based processing.
11. After the data of interest have been examined by the smart detection block, the results are sent to the HPS program.
12. When enough data points are gathered, the HPS program will inspect the memory.

13. The HPS program cooks the data into display information to drive the VGA compatible monitor. Upon request, the raw data will be saved to the micro-SD card and can be transferred to the host machine if necessary.

Based on the operation concept described above, the internal signaling of the system was established as in Figure 4.17.

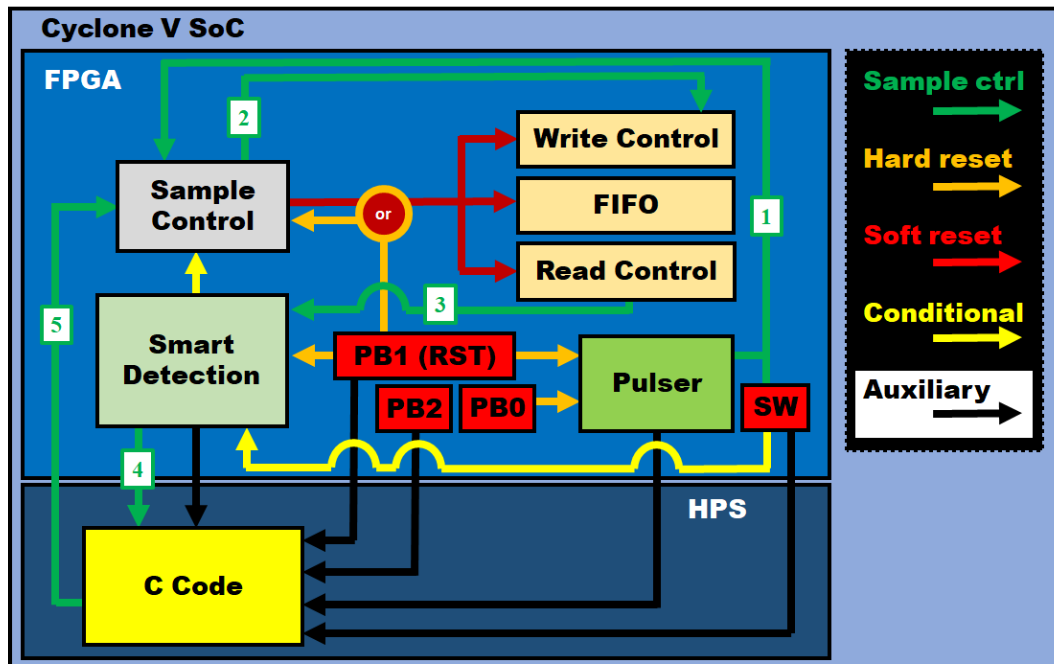


Figure 4.17: Control signal connections and control flows in the system.

Figure 4.16 and Figure 4.17 combined is the complete system-level design. In Figure 4.17, green paths indicate transitions in operation phases. Initially, the activation pulse generated by the pulser block is captured by the sample control block, which indicates the beginning of a testing/sampling cycle. Alongside the pulse activation, readings from the switches (SW) are also fed into the sample control block. The readings indicate a binary number which describes the length of a delay before the start of the cycle. The delay is a design attempt to implement the digital delay line. Once the activation pulse is detected and the delay condition is met, the sample control block will lift the soft resets (red paths) on FIFO related blocks. The write control block will start working which indicates the start of data acquisition.

During the data acquisition phase, the read control block will signal the smart detection block three times. The first time is when the data count in the read control block reaches the start of the data of interest. The second time is when the data count reaches the end of the data of interest. The smart detection block interprets the data between these two signals and forwards the detection result to the C code in HPS through a PIO port once done. During the interpretation period, the switch settings (yellow path from SW) are read by the smart detection block and it determines the length of data should be examined and whether the "defect" found in data should be pushed to the C code (black path from the smart detection block). Note that this data interpretation is carried out in parallel with the data acquisition. In the same acquisition phase, the final contact made by the read control block to smart detection block is when no data will ever appear in the FIFO which indicates the end of the data acquisition phase. The smart detection block will forward this message to the C code to initiate the software operations. At this moment, three FIFO related blocks and the smart detection block are remained in their own idle state.

Once the C Code acknowledges the signal from smart detection block, it will conduct a memory copy operation on the data in RAM. After the memory copy is done, the C Code will signal the sample control block to announce the end of the cycle. When the sample control block receives the signal, it will put the FIFO related blocks in soft reset and check if any defect needs to be reported (yellow path from smart detection block). If a defect is reported, the sample control block will put up a message in the on-board seven-segment displays and set the whole system on hold. Now, only hard reset (orange path to sample control block) can restart the process. If no detection operation has been done, the sample control block will start a new acquisition cycle all over again.

For other black paths that were not mentioned, the one from the reset button let C Code reset the display information on VGA display; the one from SW carries information on the delay and length of data of interest to C code; the one from PB2 (the push button labelled as KEY 2 on the development board) initialize a data saving process in C code; and finally the one from the pulser block tells C Code the current pulsing mode. The pulsing mode is set by PB0 (the push button labelled as KEY 0 on the development board). The hard reset (orange

paths) is conducted by PB1 (KEY 1 on the development board). It does all the reset for FPGA logic: It puts pulser block into the OFF state, clears the detection information in the smart detection block, restarts the sample control block, resets the FIFO related blocks, and resets all the counters.

4.3.3 Block Functions

Following the system diagrams (Figure 4.16 and Figure 4.17) in the previous section, individual function blocks have to be developed. Verilog codes are long and tedious to go through, so the HDL programming considerations and concepts for key functions are presented in the following sections.

4.3.3.1 Debouncing block

This block may never appear in any system level diagram, but it is essential for pushbutton related operations. Switch bouncing is a problem caused by hardware circuit. Figure 4.18 gives an impression on the bouncing issue.

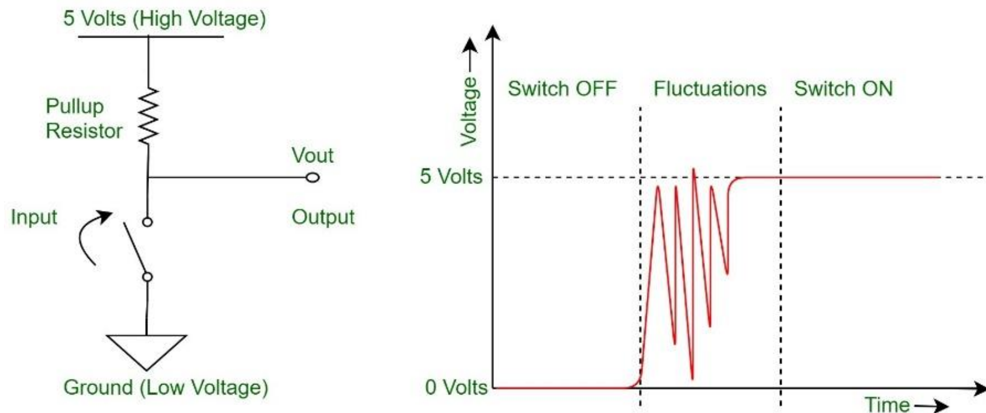


Figure 4.18: Switch bouncing [141].

The “bouncing effect” may cause instability in edge triggering behaviors. The debounce block is used to eliminate this hazard and convert button actions into a clocked operation. The key is to use a register to hold the value which tells the status of the button. No update for the value is needed unless an input for new value stays for a certain period which is longer than the fluctuation time. The period is controlled by a counter reacting to a clock. In

this way, the button output is stable, and the behavior is synchronized with clock. All the pushbutton related operations in this design used this debouncing technique to ensure stability.

4.3.3.2 Pulser block

The pulser block has three states: 10 MHz pulsing state, 2.5 MHz pulsing state, and an OFF state. The state machine changes the pulse enable and the frequency selected for the operation. The Pulse Repetition Frequency (PRF) is set to 1 kHz. It is realized by an internal counter in the pulser_core submodule. In the pulser_core submodule, the cycle length of the counter reacts to the change of the current driving frequency. Because a bi-polar pulse is made up of one positive pulse and one negative pulse while the clock operation can be activated by either positive or negative edge of the clock, the input clock should be doubled to provide the "half length". So, 20 MHz and 5 MHz are needed as clock inputs for 10 MHz and 2.5 MHz output bi-polar pulses. The selection between the input clock is done with a 2 to 1 multiplexer. There is also a switch input to the pulser block, because the last switch (switch 9) is used as an ON/OFF switch to the system. The pulse amplitude is a combinatorial result of the switch 9 position and a pulse enable signal, which promotes the ON/OFF switch with an overwrite privilege to the pulser.

4.3.3.3 FIFO Block and its Read/Write Control Block

The data are supposed to be logged into the RAM, but the RAM and ADC works in different clock domains; hence, a dual clock FIFO is needed for clock domain crossing and data preservation. Dual clock FIFO block in this project was modified from an Intel IP block. It should be used with read and write controls. The read control and write control blocks are modified from the examples provided in the FIFO IP manual [142]. The maximum number of samples in the write control were changed to 4096. Consequentially, the sizes of the registers in both the read and write controls were changed. It is worth noting that the write control has an INCARD state between its write cycles to allow the data to stabilize (prevent the metastable condition). Then, the frequency of the write control block should be exactly twice as fast as the ADC clock, otherwise data will be lost (if too slow) or oversampled (if

too fast). The read control works in a similar way. There is an INCARD state exists between the read cycles to submit the data to the RAM. Therefore, to cope with the read and write controls, the FIFO operations in this design are all clocked at 130 MHz. To synchronize with the FIFO read control and ensure stable data transfer, the RAM module is also clocked at 130 MHz with the same clock source.

The FIFO operation starts whenever it is pulled out of its reset. The operation will terminate automatically because the write control only writes a total 4096 words to FIFO before going idle. The FIFO will be drained eventually by the read control, and the reading process should end. In the design concept, a new cycle will not begin unless there comes a reset signal which brings the write control out of its IDLE state and resets all the parameters in FIFO and read controls.

4.3.3.4 Smart detection block

Other than the reset state, there are four normal states in the smart detection block, IDLE, TAKE_DATA, PROC_DATA, and DONE. In IDLE state, initial values are set, and the HPS is not allowed to take data from the shared memory. When the specific number of words have been read by the read control block, the smart detection block moves on to TAKE_DATA state. In this state, the smart detection block reads data from the output port of read control block disregarding the “read_enable” signal. But it still takes reference to the current data count from read control block. To synchronize with the FIFO operations, the smart detection block is also clocked at 130 MHz. Compared to the switch-mode operation due to the INCARD state in FIFO read/write control blocks, the continuous reading doubles the data rate in the smart detection block.

Smart detection block is implemented to demonstrate the hardware processing. As inferred by its name, the block is programmed to identify the premature echo pulse in the data of interest. The processing is done in the TAKE_DATA state. The concept is to identify the start of the “big bumps” in the raw RF signal disregarding the small fluctuations by setting a trigger level. It means that the signal should be filtered so that the high frequency components can be ruled out, and any distortions left in the processed signal should contain

valuable information. Therefore, the algorithm took reference to a basic RC low-pass filter circuit (Figure 4.19) [143].

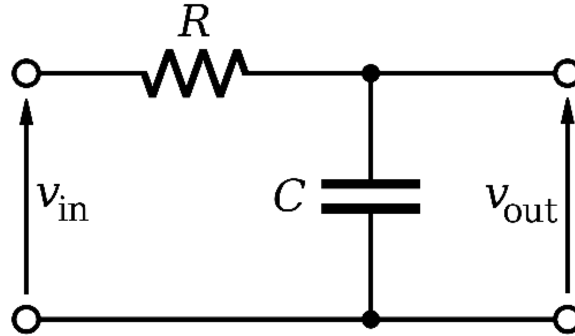


Figure 4.19: RC low-pass filter [143].

According to the Kirchhoff's circuit laws, the voltage relationship can be established as,

$$v_{in} + Ri(t) = v_{out} \tag{4.1}$$

Let the charge stored in the capacitance C at time t be $Q_c(t)$. Then,

$$C = \frac{Q_c(t)}{V_{out}} \tag{4.2}$$

$$i(t) = \frac{dQ_c(t)}{dt} \tag{4.3}$$

Plug (4.2) and (4.3) to (4.1), and rearrange, we have

$$v_{in}(t) - v_{out}(t) = RC\frac{dv_{out}}{dt} \tag{4.4}$$

Let $v_{in}(t)$ be the signal in and $v_{out}(t)$ be signal out, and write the continuous equation into discrete representation (sampling the signal is discrete), the equation becomes

$$x(i) - y(i) = RC\frac{y(i) - y(i-1)}{\Delta t} \tag{4.5}$$

where i is the sample count. x and y are signal series for input and output, respectively. Rearrange (4.5),

$$y(i) = \alpha\, x(i) + (1-\alpha)y(i-1)$$
$$\text{where } \alpha = \frac{\Delta t}{\Delta t + RC} \text{ is the smoothing facter, and } 0 \leq \alpha \leq 1 \quad (4.6)$$

(4.6) gives the equation for the low pass filtering on input signal.

Let α be very small, then $(1-\alpha)$ can be approximated to 1. In this case, the output of the current measurement will only be affected by a large enough input, and the previous output will carry on (hold the level if nothing is worth adding). To keep the level from dropping, the absolute value of the input value ($|x(i)|$) can be used. Then, whenever a comparative large impulse arrives, the level of the output will increase. By setting a proper threshold, a level detector can be created to identify the pulse location. Next step is to develop the hardware code to implement the algorithm. A trick used in the hardware implementation took advantage of the fact that the value assignment in non-blocking assignment will take effect in the next clock cycle. Therefore, assigning the current value $y(i)$ to a register effectively saves the $y(i-1)$ for the next cycle. The input $|x(i)|$ is the absolute value of the RF signal. The ADC latches data into 14-bit unsigned registers. Therefore, the acquired data should be subtracted by the offset value (213) before taking the absolute value. To help fit the data into the 16-bit storage space in RAM, the data size is expanded to 16 bits during the algorithmic operations. The deduction and absolute value finding procedure are done with the 2's compliment method:

1. Add the unsigned binary number with 2's compliment of decimal number 8192 in 16-bit representation (1110_0000_0000_0000)
2. If the result is equivalent to a negative value in a signed register (the most significant bit is 1), then the results is deducted by 1; Otherwise, preserve the current result.
3. Keep the condition branch followed in step 2, the current result preserved in positive value branch is the final output; As for the negative branch, flip all the bits in the register (0 to 1 and 1 to 0) and use the new value as the output.

By using the 2's compliment method, the conversion from an unsigned register to signed register is not required. Because there are 3 clock cycles between step 2 and the available

output, three parallel routes are established to hold the value in the conditional statement throughout the process so that the operation is coherent. The multiplication of the circuits is done with a for-loop. Multiple signal paths created a new challenge in initialization. To zero all the registers concerned in this logic in the IDLE state is a waste of resources if done individually. Therefore, three valid bits are introduced and evenly distributed to each route to mark the validity of the input data. Thus, the initializing process can be done on just three bits. After $|x(i)|$ is found, the level detection algorithm can be implemented. In hardware, (4.7) was used,

$$y(i) = |x(i)| \gg N + y(i-1) \tag{4.7}$$

where N denotes the repetition of right shift operations, and each right shift in register means a division by 2. N can be set based on the signal intensity. The pulse is detected once the output $y(i)$ equals to certain threshold. The threshold is also determined based on the application. N was set to 8 in this project, threshold to detect the pulse was set to 2. The data of interest range can be adjusted by the ON/OFF state of switch 6. The range is based on the read sample count, and is either 200 to 500, or 200 to 1000 in this project. Once $y(i)$ reaches the threshold, the current word count minus one will be recorded as the detected echo position. The pulse detection information will be forwarded to the HPS. When all the data of interest have been processed, the smart detection block will change its state to PROC_DATA.

In PROC_DATA state, the received pulse position is examined. If switch 8 is off, the current pulse position will be saved as a reference for the next cycle; otherwise, the comparison between the position of previously detected pulse and the current one will be made. The current pulse position will always be exported to the last four HEX display (HEX 0 ~ 3) for reference. Based on the difference, it can be determined whether the echo is from a premature reflection, i.e., the defect. In the implemented hardware, a minimum offset of 40 in word count should be fulfilled before the new value to be claimed as a “defect”. An additional piece of information will be handed over to the sample control block and HPS if the defect is found. This state will not end until the last word is read by the FIFO read

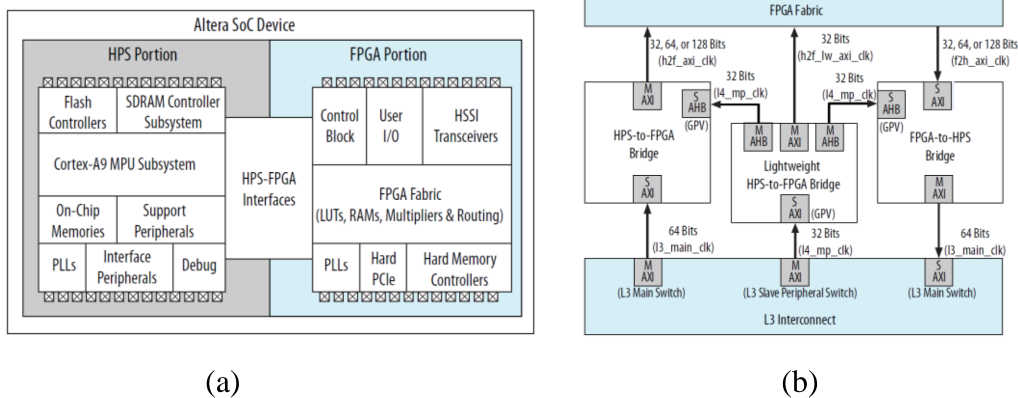
control. Once the state ends, it will change to state DONE and await the signal from sample control block to flip back to IDLE. The reset state controlled by the hard-reset button (KEY 1) will clear any memorized pulse position.

4.3.3.5 Sample control block

The sample control block oversees the whole operation. Other than the reset state, it has four working states. State 0 sets all the initial values for the counters and applies a two-second delay to the operation cycle which just comes out of reset. The first two HEX displays (HEX 4 ~ 5) will show the count-down for these 2 seconds and end with "GO" to notify the user. State 1 detects the positive edge of the pulser block's positive pulse activation signal. State 2 handles the delay condition set by the first 6 switches. The binary number represented by the switches are the multiples of 65 clock cycles, which means each increment in the binary number is an additional 0.5 us in the delay. State 3 gives "Go" command to the FIFO operations, which also puts smart detection block back to IDLE state from DONE state. If defect detecting function is activated, when the defect is detected, the sample control block will be stuck in this state and only applying reset (by KEY 1 or reboot the system) can get rid of it, and the first two HEX displays (HEX 4 ~ 5) will show "GG". During normal operations, when the finish signal from the smart detection block arrives, the sample control block will proceed to state 4 and await HPS signal to start a new cycle.

4.3.4 Platform Designer (Qsys) and System Interconnection

The design introduced in the previous section requires multiple data transfer and communication operations between the FPGA and HPS. Referring to the architecture in block diagram of the Intel SoC FPGA (Figure 4.20(a)), the operations should be realized by the HPS-FPGA interfaces. More specifically, three bridges between the HPS and FPGA take the burden ((Figure 4.20(b)).



(a) (b)

Figure 4.20: HPS to FPGA connections (a) Intel SoC block diagram (Figure 2-1 in [144]); (b) Three bridges between the FPGA and HPS fabric (Figure 9-1 in [144]).

The bridges use the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI) protocol, and are based on the AMBAS Network Interconnect (NIC-301) [144]. To define the interconnection through these bridges, the Platform Designer (Qsys) tool in the Quartus Prime Lite Development Suite is used. As mentioned in Section 2.3, the project was based on the DE10-Standard Computer project, so the Qsys layout has already been popularized with all demo instances for Intel University Program tutorials. The huge Qsys structure is comprehensive for most applications indeed, but it also unnecessarily soaks up valuable resources on the chip and increase the compilation time and fitting & routing difficulties for no meaningful return. Therefore, the system should be chopped down and reconfigured. The modified Qsys layout is shown in Figure 4.21. System_PLL and pll_0 are two PLL clock modules to provide stable clock signals for the system. The reference clock for both PLL clock modules were exported to the top-level module in the Verilog codes, and 50MHz clock source was assigned to these exported ports. The output clock from the sys_clk is 100 MHz. The output clocks from the pll_0 are 20 MHz, 5 MHz, 65 MHz, and 130 MHz successively for outclk number 0 to 3. The first LED (LED 0) on the development board shows the lock-in state (light on for locked-in) for pll_0 module. The clock outputs from both modules are assigned to inputs in various modules following the connections in Figure 4.21. ARM_A9_HPS is the HPS system instantiated in the Qsys to communicate with other parts of the system. The configuration for HPS is varied based on the SoC on board.

Because the original layout was made for DE10-Standard, no change was needed. The prefix on the ports “h2f” and “f2h” means “HPS to FPGA” and “FPGA to HPS”, respectively. For modules other than the system clock and HPS instance, a reset source must be specified. In this project, all the instantiated modules in the Qsys layout had their reset sources synchronized to the reset_source in System_PLL and h2f_reset in HPS. The SDRAM (acronym for Synchronous Dynamic Random-Access Memory) module refers to the SDRAM (64 MB in size) on the FPGA side. Although not intentionally used in this project, it was found during the development that the SDRAM is an always enabled I/O buffer for the DE10-Standard Computer System; hence, it is kept in the design for system stability. The LEDs, Slider_Switches, and Pushbuttons are PIO ports established between the HPS and FPGA to control the corresponding hardware on the development board. The edge_data, hps_signals, and sys_status are other sets of customized PIO ports used to exchange simple signals between the two fabrics. For PIO ports, they can be defined as Bidir, Input, Output, or Inout ports. In this design, they are defined as either Input or Output, and the direction of the ports is in the perspective of HPS. The clock bridge instance is used to import clocks from the FPGA side to Qsys interconnection. It is essential for dual port instances, such as the dual port RAM, because the clock for either port must be synchronized to their controller fabric. The dual port RAM, tmp_data, is the On-chip RAM block shared by both fabrics, and it is the memory block to store the digitized measurement data.

Figure 4.21: Qsys layout for the prototype system.

AV_config, Pixel_DMA_Addr_Translation, VGA_Subsystem, and On-chip_vga_buffer are all instances related to the 640x480 8bit VGA display. Instead of using SDRAM as the video buffer, the design employed the on-chip Static RAM (SRAM) for the speed. This optimization technique was adopted from the course material (GPU with FAST display from SRAM) available online [145]. The VGA_Subsystem is a high-level module which is a combination of several submodules. Drill into the system, another Qsys layout can be found. After the adjustment, a new VGA_Subsystem interconnection was established as in Figure 4.22. Some of the instance substitutions require users to have installed the add-on package from Intel University Program. Following Figure 4.22, the detailed configurations are as follows: In VGA_PLL, the VGA clock was enabled as the clock for VGA 640x480. The Clock frequency in Sys_Clk was set to “50,000,000 Hz”. The VGA pixel FIFO had its Color bits set to “8” and the Color Planes set to “1”. The incoming format for VGA_Pixel_RGB_Resampler was “8-bit RGB” and the Outgoing format was “30-bit RGB”. VGA_Alpha_Blender was set to “Normal” mode. In VGA_Dual_Clock_FIFO, the Color Bits was set to “10” and the color planes to “3”. In VGA_Controller, “DE10-Standard” was chosen as the DE-Series Board option. Video Out Device was set to “VGA connector”, and the VGA Resolution was configured as “VGA 640x480”. One of the most important configurations should be done in the VGA_Pixel_DMA. The Addressing Mode should be configured to “Consecutive”, because it can change the way the memory space being mapped to the pixels on the display. By configuring the address mode into consecutive, 30% of the SRAM needed for the video buffer can be saved compared to the “X-Y addressing” mode [145,146]. It is worth doing so because SRAM is an expansive resource on board.

System: Computer_System.VGA_Subsystem **Path:** VGA_PLL

Name	Description	Export	Clock	Base	End
VGA_PLL	Video Clocks for DE-series Boards				
ref_clk	Clock Input	**vga_pll_ref_clk**	***exported***		
ref_reset	Reset Input	**vga_pll_ref_reset**			
vga_clk	Clock Output	*Double-click to export*	VGA_PLL_vga_clk		
reset_source	Reset Output	*Double-click to export*			
Sys_Clk	Clock Source				
clk_in	Clock Input	**sys_clk**	***exported***		
clk_in_reset	Reset Input	**sys_reset**			
clk	Clock Output	*Double-click to export*	Sys_Clk		
clk_reset	Reset Output	*Double-click to export*			
VGA_Pixel_FIFO	Dual-Clock FIFO				
clock_stream_in	Clock Input	*Double-click to export*	**Sys_Clk**		
reset_stream_in	Reset Input	*Double-click to export*	[clock_stream_in]		
clock_stream_out	Clock Input	*Double-click to export*	**Sys_Clk**		
reset_stream_out	Reset Input	*Double-click to export*	[clock_stream_out]		
avalon_dc_buffer_sink	Avalon Streaming Sink	*Double-click to export*	[clock_stream_in]		
avalon_dc_buffer_source	Avalon Streaming Source	*Double-click to export*	[clock_stream_out]		
VGA_Pixel_RGB_Resampler	RGB Resampler				
clk	Clock Input	*Double-click to export*	**Sys_Clk**		
reset	Reset Input	*Double-click to export*	[clk]		
avalon_rgb_sink	Avalon Streaming Sink	*Double-click to export*	[clk]		
avalon_rgb_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]		
avalon_rgb_source	Avalon Streaming Source	*Double-click to export*	[clk]		
VGA_Alpha_Blender	Alpha Blender				
clk	Clock Input	*Double-click to export*	**Sys_Clk**		
reset	Reset Input	*Double-click to export*	[clk]		
avalon_foreground_sink	Avalon Streaming Sink	*Double-click to export*	[clk]		
avalon_background_sink	Avalon Streaming Sink	*Double-click to export*	[clk]		
avalon_blended_source	Avalon Streaming Source	*Double-click to export*	[clk]		
VGA_Dual_Clock_FIFO	Dual-Clock FIFO				
clock_stream_in	Clock Input	*Double-click to export*	**Sys_Clk**		
reset_stream_in	Reset Input	*Double-click to export*	[clock_stream_in]		
clock_stream_out	Clock Input	*Double-click to export*	**VGA_PLL_vga_clk**		
reset_stream_out	Reset Input	*Double-click to export*	[clock_stream_out]		
avalon_dc_buffer_sink	Avalon Streaming Sink	*Double-click to export*	[clock_stream_in]		
avalon_dc_buffer_source	Avalon Streaming Source	*Double-click to export*	[clock_stream_out]		
VGA_Controller	VGA Controller Intel FPGA IP				
clk	Clock Input	*Double-click to export*	**VGA_PLL_vga_clk**		
reset	Reset Input	*Double-click to export*	[clk]		
avalon_vga_sink	Avalon Streaming Sink	*Double-click to export*	[clk]		
external_interface	Conduit	**vga**			
VGA_Char_Buffer	Character Buffer for VGA Display				
clk	Clock Input	*Double-click to export*	**Sys_Clk**		
reset	Reset Input	*Double-click to export*	[clk]		
avalon_char_control_slave	Avalon Memory Mapped Slave	**char_buffer_control_slave**	[clk]		
avalon_char_buffer_slave	Avalon Memory Mapped Slave	**char_buffer_slave**	[clk]		
avalon_char_source	Avalon Streaming Source	*Double-click to export*	[clk]		
VGA_Pixel_DMA	Pixel Buffer DMA Controller				
clk	Clock Input	*Double-click to export*	**Sys_Clk**		
reset	Reset Input	*Double-click to export*	[clk]		
avalon_pixel_dma_master	Avalon Memory Mapped Master	**pixel_dma_master**	[clk]		
avalon_control_slave	Avalon Memory Mapped Slave	**pixel_dma_control_slave**	[clk]		
avalon_pixel_source	Avalon Streaming Source	*Double-click to export*	[clk]		

Figure 4.22: Qsys layout for VGA subsystem in the prototype system.

Other than the interconnection wires, the physical address assignment was also done in the Platform Designer. Following the connections shown in Figure 4.21, the modules were controlled by different buses. Figure 4.23 gives an impression on a common address map for the system interconnect masters. Those controlled by the low-weight AXI bus (h2f_lw_axi_master) have a base address at 0xFF200000, and those controlled by the full speed AXI bus (h2f_axi_master) have a base address at 0xC0000000.

Figure 4.23: System interconnection master address map (Figure 8-4 in [144]).

The defined values in the base column in Figure 4.21 are merely offset instead of the real "base" value. They should be noted and will play an important role in the software coding. Figure 4.24 shows a collective address map designed for this project. Any conflicts in the address will be marked out in red font by the Platform Designer.

Address Map

System: Computer_System **Path:** System_PLL

	ARM_A9_HPS.h2f_axi_master	ARM_A9_HPS.h2f_lw_axi_master	Pixel_DMA_Addr_T...	VGA_Subsystem.pixel_dma_mas...
LEDs.s1		0x0000 0000 – 0x0000 000f		
edge_data.s1		0x0000 0020 – 0x0000 002f		
hps_signals.s1		0x0000 0030 – 0x0000 003f		
Slider_Switches.s1		0x0000 0040 – 0x0000 004f		
Pushbuttons.s1		0x0000 0050 – 0x0000 005f		
sys_status.s1		0x0000 0060 – 0x0000 006f		
AV_Config.avalon_av...		0x0000 3000 – 0x0000 300f		
Pixel_DMA_Addr_Tra...		0x0000 3020 – 0x0000 302f		
VGA_Subsystem.char...		0x0000 3030 – 0x0000 3037		
SDRAM.s1	0x0000 0000 – 0x03ff ffff			
tmp_data.s2	0x0400 0000 – 0x0400 1fff			
Onchip_vga_buffer.s2	0x0800 0000 – 0x0804 afff			0x0800 0000 – 0x0804 afff
VGA_Subsystem.char...	0x0900 0000 – 0x0900 1fff			
ARM_A9_HPS.f2h_axi...				
Onchip_vga_buffer.s1				
VGA_Subsystem.pixel...			0x0000 – 0x000f	
tmp_data.s1				

Figure 4.24: Address map for the prototype system.

Once all the configurations in the Platform Designer are done, the HDL codes for the interconnections should be generated. This procedure is done through accessing the menu in the Platform Designer "generate -> generate HDL…". The instantiation template available in the same menu branch helps users build their own top-level module with the instantiated HDL template. The connections inside the template should be modified to I/O definitions according to the definitions in the project.

4.3.5 System Summary and Debugging

Until this point, the whole hardware system configuration for the FPGA is finished. After the compilation, a brief summary on the resource consumptions of the FPGA can be reviewed from the compilation report (Figure 4.25). The report indicated that only 11% logic elements and 6% of the DPS blocks were used in the project. There is still a large room for more complicated on-board signal processing techniques to be implemented. Although 47% of the block memory resources were taken, this situation can be alleviated by making use of other peripherals like SDRAM on FPGA side or DDR3 RAM on HPS side.

Revision Name	DE10_Standard_Computer
Top-level Entity Name	DE10_Standard_Computer
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	4,577 / 41,910 (11 %)
Total registers	5787
Total pins	373 / 499 (75 %)
Total virtual pins	0
Total block memory bits	2,659,840 / 5,662,720 (47 %)
Total DSP Blocks	7 / 112 (6 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	2 / 15 (13 %)
Total DLLs	1 / 4 (25 %)

Figure 4.25: Compilation report of the prototype system.

During the compilation, if no error messages were delivered, the compilation would eventually be successful. But the design could fail if some of the warnings, which do not interrupt compilation, were ignored. Two of the most likely causes in the warnings which can harm the design contain the keywords “latches” or “inferred” [147]. When a conditional statement or case statement is not fully defined, a latch can be inferred because the logic controlled by the statement can stay in the original state and thus halt the process. The solution to this is simply complete the definition for all the conditional statements. For case statement specifically, a “default” case should always be included so that the logic can respond to all possible inputs. For the keyword “inferred”, it usually implies that the register or wire components in the design are not declared and thus an “inferred” component has been created to fit the gap. Sometimes it works, but it can also cause serious problems without providing a clear clue, such as overflowing the connections or registers when a certain data width is required yet undefined. Speak of the data width, it is a good practice to check the width assignment for every register or wire in the design so that they are sufficient for the logic demands. As for the warnings in time constraints, most of them can be solved by proper settings in the Timing Analyzer tool provided in Quartus Prime or referring to the related SDC setup mentioned in the manuals or datasheets. Some of the timing issue may not affect the functionality of the program. In this project, the debugging process was basically keeping Trial & Error until the design worked.

A program file (*.sof) will be generated under the project directory once the design is compiled. It can be used for FPGA programming directly through the USB-Blaster II connection (normal type-B on the board) with the Programmer tool in the Quartus Prime. It is a handy way for a quick programming for debugging. It is a recommended way if Signal-Tap is used to monitor the FPGA program in real register-transfer level (RTL) simulation. Signal-Tap is a real-time analyzer tool provided in the Quartus Prime. Although called simulation, it is a test run performed with real hardware. Once a test program is created in the Signal-Tap, the tool will instantiate an interface on the FPGA to talk with the Analyzer; Therefore, the whole program needs to be recompiled and the FPGA should be programmed afterwards. During the testing, the link between the host machine and the board should be maintained by

the boundary scan circuitry via JTAG (in this case, USB-Blaster II connection). Figure 4.26 shows the Signal-Tap simulation during the early stage of the development. The setup was to test the performance of the AD interface card and confirm if the pulse activation concept would work in data acquisition.

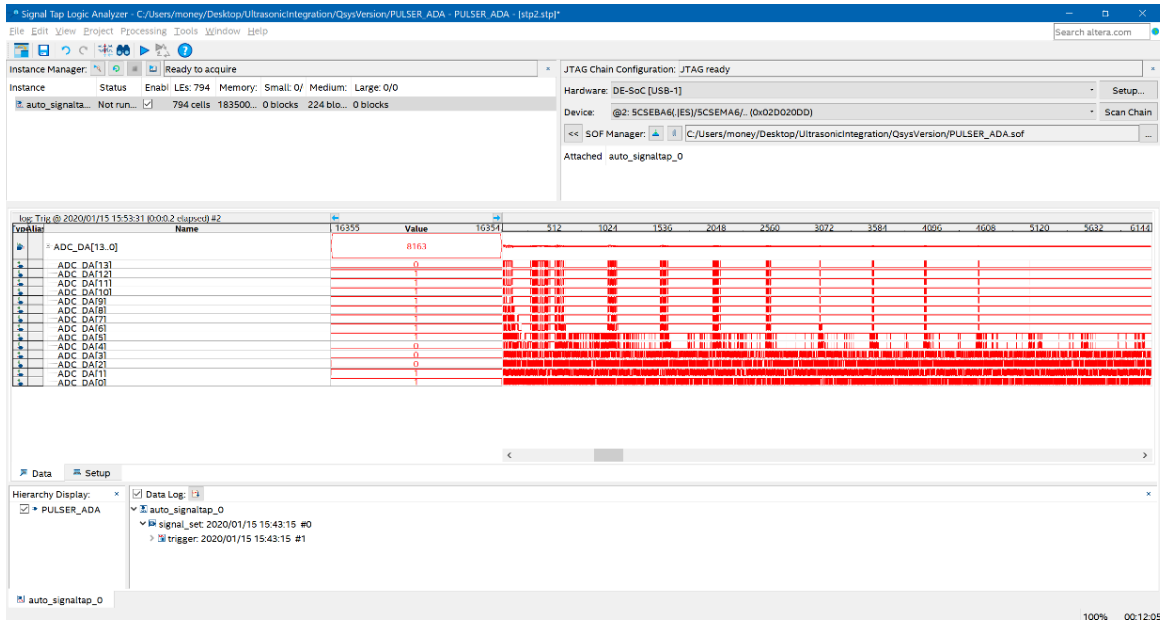


Figure 4.26: RTL test with Signal-Tap functions for AD channel.

In this project, instead of through the JTAG connection, the FPGA was programmed by ARM processor with Linux operating system. To do so, the program file must be converted into a compressed raw binary file (*.rbf) for Linux. There are two ways to do that. The first one is to use the GUI function in the Quartus Prime Lite program. It can be accessed through the main menu, “File -> Convert Programming Files…”. The procedures after in the pop-up window are shown in Figure 4.27.

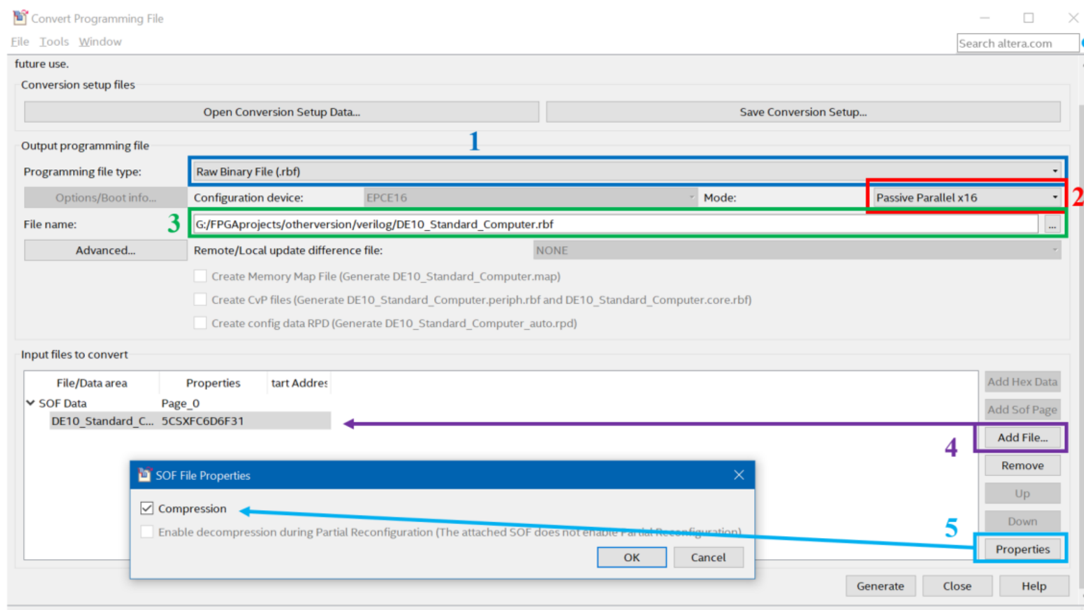


Figure 4.27: Program file conversion steps with GUI.

1. Select the programming file type as Raw Binary File (*.rbf)
2. Change mode to Passive Parallel x16
3. Add the output file name and path
4. Add the input file to the converter
5. Select the file and check Compression in the Properties setup window
6. Generate the raw binary file

The other way does it with command line script, but it still calls the conversion functions in the Quartus Prime installation. Create a Windows Batch file (*.bat) by any text editor, for example Notepad, and add the following script:

%QUARTUS_ROOTDIR%\\bin64\\quartus_cpf -c *.sof -o bitstream_compression=on *.rbf

Replace the "*" part of "*.sof" with the file name in the project and change the "*" part in "*.rbf" to the output file name. Save the file and place it in the same directory where the "*.sof" is located. Run the batch file and the command line in Windows will handle the rest.

After a while, the converted file will appear in the same directory. The programming file in compress raw binary file format is the ultimate output of FPGA programming.

4.4 Software Development

The first step in software development was to configure the environment. In this design, Linux system was installed in the ARM core as a platform for the code execution. Note that the platform for coding does not have to be on the Linux, but the codes should be compiled to binary files which can run on the Linux. C language is used in software development for its efficiency and low-level support.

4.4.1 Linux Distribution

A distribution of Linux should be selected. Both Intel and Terasic Technologies provide a few different Linux distributions. Based on our requirement, the selections can be narrowed down to either the console Linux with 4.5 kernel provided by Terasic Technologies (Version-A), or the DE10-Standard-UP-Linux-ROS with 3.18 kernel provided by Intel (Version-B).

Version-A is a modified kernel from Angstrom (http://wp.angstrom-distribution.org/). Angstrom is a distribution directly maintained by Altera, and the target application of the distribution is to embedded systems. To optimize for speed and size, it is made into a binary distribution. It works on a lightweight package management system: open package management (opkg) system. The management system allows users to install software distributed as opkg packages. This Linux distribution also ships with a Dynamic Host Configuration Protocol (DHCP) client software (udhcpc), so that the file transfer can be done using the Secure Shell protocol (SSH). To use the protocol, the host and the on-board system should login to the same DHCP server. Easiest way is to use a router which supports DHCP and connect both devices to it. Alternatively, for Windows based host machine, a free-to-use software “DHCP server for windows (https://www.dhcpserver.de/cms/)” can be used to establish the server on the host’s ethernet card. The on-board system can connect to the server directly through the ethernet cable connection to the host. Version-A can program the FPGA on boot-up with a specific compressed raw binary file (soc_system.rbf) in its root directory. The problem with Version-A is that it does not provide Linux Header files, which

are necessary to develop kernel modules. This creates difficulties in building interrupt handlers which are supposed to be inserted into the kernel. Even if generic header files for the distribution version are found, they do not guarantee the compatibility as the distribution is customized for the hardware. To rebuild a kernel with the specific header files, it takes effort to realize. Another drawback is that Version-A is a console-only distribution. For those engineers who have been trained with graphics operating systems, like Windows, it takes time to get used to. Nevertheless, Version-A is a Linux distribution that is space-efficient and fast but slightly not user-friendly.

Version-B, on the other hand, has a better support for user interface at a cost of disk space and boot up time (minor). Compared to the compact Version-A, it is more than 4 times bigger in the image file size (6.24 GB vs. 1.49 GB). Version-B does not include udhcpc in fresh installation. However, it provides Virtual Network Computing (VNC) support. It is a graphical desktop sharing system that allows users to access the target machine through network connection [148]. Similar to the DHCP, both the host machine and on-board system must work under the same local IP domain to use the connection. To transfer files between the host machine and on-board system, secure file transfer protocol (SFTP) can be used. Version-B also includes an FTP Server which uses Port 22 for the network connection. Username for the FTP server is “root”, and the password is “password”. On the Windows based host machine, a free-to-use software FileZilla (client version at https://filezilla-project.org/) can be used to establish the FTP. The Linux kernel in Version-B is based on Ubuntu (https://ubuntu.com/), which means that it resembles the Debian-based Linux distributions. The file management system is dpkg and users can use Ubuntu’s Advanced Packaging Tool (APT) to install new software packages. This is one of the major differences between Version-B and Version-A. Since Version-B is supposed to be a part of Intel University Program, all the examples in the educational program should work. Therefore, it naturally provides the Linux Header files for Kernel module development. ROS compatibility is also provided in the distribution, which is a nice feature to include considering the project may require coordination with robotics in the future. Boot-up FPGA programming with a specific compressed binary file (*.rbf) is also supported by Version-B. it

was found that the method described in [140] did not work well. Therefore, an alternative was followed to finish the task. In summary, Version-B is advantageous for beginners because it is user-friendly and comprehensive. The file size and the unnecessary features may be an issue in a performance oriented commercial system, but for educational and research purposes, it is not an issue given the fact that 64 GB or larger size micro-SD cards are commonly available.

Based on the above considerations, Version-B (the Intel version) was chosen for this project. The link to the image file (DE10-Standard-UP-Linux-ROS.img) can be found in the following online source:

https://www.intel.com/content/www/us/en/programmable/support/training/university/materials-software.html.

The Linux image file can be written to a micro-SD card with Win32 Disk Imager tool available in Windows. Note that most of the file system is not directly accessible in Windows, but there is a shared disk space formatted with FAT32 file system. If necessary, it can also be a way to transfer file between both systems. Although GUI is provided through VNC, most features in SoC design still rely on command line instructions.

Once the raw binary file is acquired following the procedures described in 4.3.5. and have migrated to the Linux file system on the micro-SD card, the FPGA can be programmed using the following commands (Figure 4.28) through the command line interface in PuTTY.

```
echo 0 > /sys/class/fpga-bridge/fpga2hps/enable
echo 0 > /sys/class/fpga-bridge/hps2fpga/enable
echo 0 > /sys/class/fpga-bridge/lwhps2fpga/enable
dd if=/home/root/soc_system.rbf of=/dev/fpga0 bs=1M
echo 1 > /sys/class/fpga-bridge/fpga2hps/enable
echo 1 > /sys/class/fpga-bridge/hps2fpga/enable
echo 1 > /sys/class/fpga-bridge/lwhps2fpga/enable
```

Figure 4.28: Commands to program the FPGA from Linux.

First three command lines in Figure 4.28 are used to disable the FPGA-HPS bridges to prevent unpredictable outcomes during programming. The actual command which programs the FPGA is in the fourth line. Linux is a file-based operating system; hence, all its

operations are based on manipulations on "files". The FPGA programming is conducted with the contents in file "/dev/fpga0". The command in the fourth line simply loads the compressed raw binary file (in this case soc_system.rbf) to the device file to have the FPGA programmed. After the programming, the FPGA-HPS bridges should be re-established for the program to run properly (last three lines of commands). In this project, the FPGA should always be programmed on boot-up. To realize that, all the necessary commands for FPGA programming were converted into Bash scripts (Figure 4.29) to run automatically after the boot-up of Linux.

```
#!/bin/sh
date -s "02/12/2020 11:11:11"
ifconfig eth0 169.254.1.2
echo 0 > /sys/class/fpga-bridge/fpga2hps/enable
echo 0 > /sys/class/fpga-bridge/hps2fpga/enable
echo 0 > /sys/class/fpga-bridge/lwhps2fpga/enable
dd if=/home/root/soc_system.rbf of=/dev/fpga0 bs=1M
echo 1 > /sys/class/fpga-bridge/fpga2hps/enable
echo 1 > /sys/class/fpga-bridge/hps2fpga/enable
echo 1 > /sys/class/fpga-bridge/lwhps2fpga/enable
```

Figure 4.29: Bash script to be executed immediately after Linux boot-up.

Note that in Figure 4.29, the first line indicates that the file is a Bash script. A Bash script contains commands need to be executed in a file. The name Bash is from GNU Bash, which is a Unix Shell and Command language (https://www.gnu.org/software/bash/). A Bash command can read and execute these commands from the file. The typical file extension for Bash files is "*.sh". Since the bash code is supposed to be executed right after boot, other boot-up configurations can also be inserted into the same bash script in a right order. The command in the second line in Figure 4.29 is used to set a date & time for Linux. The default time on boot-up in Linux is Jan 1, 1970. Usually it is not an issue. However, when compiling a file using "make" tool, it can cause a problem where the compilation tool judges the file being created "in the future", which will result in an error [140]. So, it is recommended to set a more realistic time on boot-up to help the tool work properly. The command in the third line is to assign a fixed IP address to the ethernet port. It is configured for the VNC connection and the FTP protocol, because the host machine in the project has an IP address at

169.254.1.1 with ethernet cable. The following steps should be taken so that this file can help in the boot-up configurations [149].

1. Move the .sh file into the directory /etc/init.d/
2. Execute “sudo chmod +x /etc/init.d/<script.sh>”
3. Execute “sudo update-rc.d <script.sh> defaults”

The first step joins the file to the boot-up files. The second step turns the Bash script executable. The third step installs the Bash code to all run levels as a service. The script can be stop/start/restart with code “sudo service <script.sh> stop/start/restart”. After these configurations, the FPGA will be programmed by the specified raw binary file right after the Linux is booted.

4.4.2 C Program

Before any algorithm can be developed, the hardware memory address should be mapped to the virtual memory space so that the software can access. All the data transfer, processing, and display are basically memory read and write operations on specific memory locations with the virtual pointers. The “mmap” function is used to map the address. The memory addresses defined in the Section 4.3.4 should be referenced. Any operations outside the allowed memory space can crash the program and result in a “segmentation error” in execution.

The ARM processor in the Cyclone V SoC is a 925 MHz dual core Cortex A9 MPCore processor [144]. The program in this project made use of the dual core feature and the program was coded into a dual thread process. The multi-threading was realized with “pthread” library. Two threads were created in the program. One handles the main system functions which contain data transfer, data saving, and plotting operations on the VGA display; and the other takes care of system controls which react to user inputs on the slider switches and push buttons. When the program receives the data acquisition finish signal from HPS, the data transfer process will begin. The data transfer between the RAM and HPS program is done using “memcpy” function. If a data saving request is made, a file contains

the copied memory contents will be saved on the micro-SD card. The file contains all 2048 data points which are formatted into one column, and they take the form of decimal numbers (converted from the 16bit unsigned register). Once all the data transfer & saving operations are done, the program will signal the FPGA to start a new cycle. The saved file can be read into MATLAB directly and parsed as a numeric vector for further data processing.

A software-based VGA display driver was coded to provide a rough graphical presentation of the acquired signal. To draw on the VGA display is to write to a specific series of memory addresses with 8-bit data which represent colors. A pixel on the display corresponds to one of these addresses. The VGA buffer in this project is instantiated into 640x480 resolution and encoded into a sequential representation (see Section 4.3.4); therefore, in order to write to a pixel which has x and y as its lateral and vertical coordinate on the screen, (4.8) should be used to determine the address offset from the base address of the pixel buffer.

$$\text{addr_offset} = y * 640 + x \tag{4.8}$$

The sampled data itself contains information on y value in (4.8). (4.9) is used to find y.

$$y = \text{floor}\left(\frac{8192 - \text{data}}{4.096} + 200\right) \tag{4.9}$$

The raw data read from the RAM are 16 bits unsigned binary numbers without the hardware processing discussed in Section 4.3.3.4. Therefore, it should be converted to a decimal number and deducted by 213 to compensate for the zero offset. Then, the number is divided by a multiple of the resolution calculated in Section 4.3.1 to create a height value in voltage. Note that the deduction is reversed in (4.9). It is because the VGA display scans from the top-left to bottom-right corner. So, a sign flip is needed to avoid the upside-down display. The y-axis span on VGA is set to ±70mV, because it was found during operation that the maximum absolute amplitude is around 50 mV. x is given by the associated time of that data point. The total data length in the project is 2048 for each acquisition cycle. It is not possible to display them all on a single x-axis under 640x480 resolution. Since the VGA display is just a reference, a resampling is done on the data to accommodate more information in time (the saved-out data remains intact; this process only affects the display). The display data is

picked as one out of every two data points in the memory, which allows the display window to show the trend for the first ~1200 data. The sampling rate in data acquisition is 65MSample/s, therefore, every 65 pixels in lateral direction on the display represent a 2us difference in time. Once the address is located, an 8-bit color will be assigned to it in consideration of readability.

To benchmark the performance of the system and the efficiency of the C code, three timestamps are recorded in the code. The first one is right after the signal from FPGA is acquired, the second one is after all the data operations are finished, and the third one is at the end of all the VGA drawing process, or the end of the software cycle. With these three timestamps, the elapsed time for data logging and the display refresh cycle can be determined.

The program uses math operations and the pthread functions, the C code compilation with gcc should include these two linker flags, "-lm" and "-lpthread". To compile the source code, the following command should be used:

"gcc -o <output file name> <file name.c> -lm -lpthread"

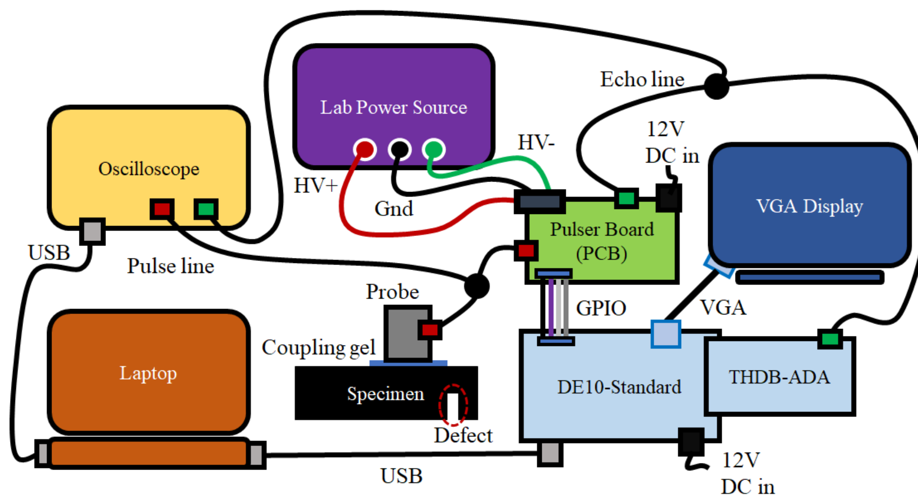
After compilation, a binary file will be generated in the same directory as the C source file. To execute the output file, use command "./<output file name>". The command to execute the binary file can also be attached to the boot script. If so, after the FPGA is automatically programmed on boot-up, the software will run.

4.5 Experiment with the prototype and evaluations

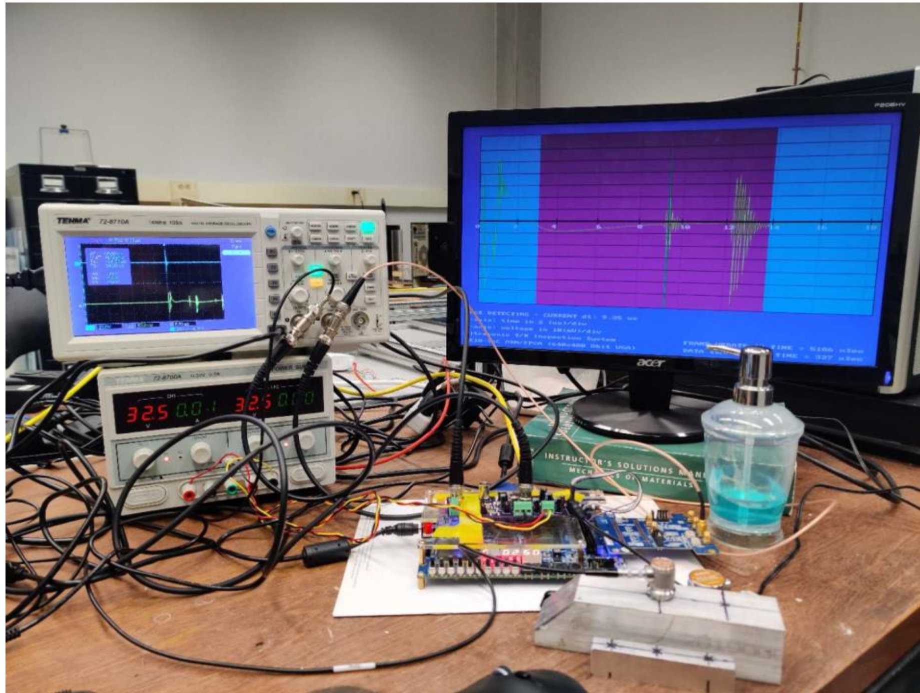
4.5.1 Data Validation Experiment

The aim of this experiment was to confirm the performance of the signal acquisition of the prototype system. A series of comparisons between the measurement from the oscilloscope and prototype are given. The schematic and corresponding real setup for the experiment are shown in Figure 4.30. An oscilloscope (TENMA 72-8710A) was included to provide benchmark data to evaluate the acquired signal. Note that the data were acquired simultaneously by the prototype system and oscilloscope. Using two T connectors, the pulse

signal from the AFE PCB was split to feed both the channel 1 on oscilloscope and transducer. Similarly, the echo signal from the AFE PCB was also split to connect to the channel 2 on oscilloscope and THDB-ADA AD channel A. Since the transducer used in the tests (SIUI P10-10L) is contact type, ultrasonic coupling gel must be applied for proper acoustic propagation. DE10-Standard board was controlled by a laptop with PuTTY through the serial USB connection. The data saved on the micro-SD card were transferred to the host laptop through the ethernet connection under SFTP protocol with Filezilla. The data from the oscilloscope were transmitted to the host computer through another serial USB connection, and they were logged by a program (DSO Monitor Controller V2.0) provided by TENMA.



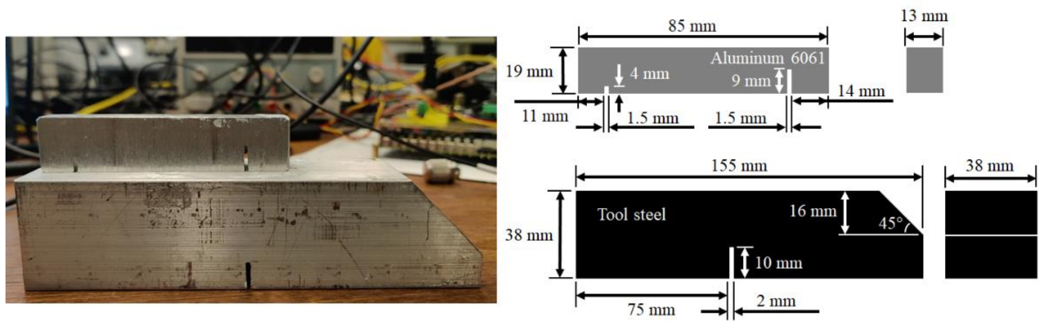
(a)



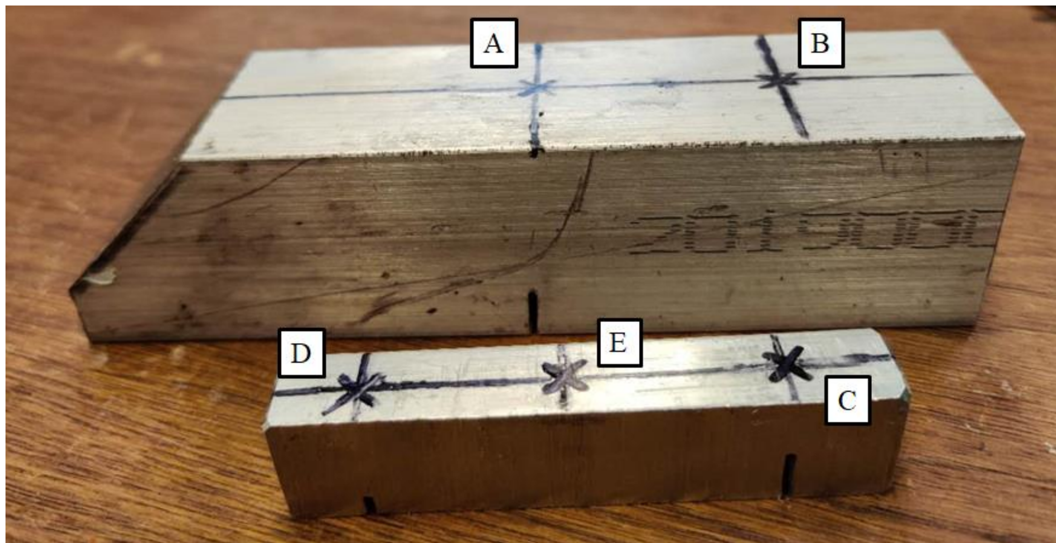
(b)

Figure 4.30: Experiment setup for validation tests (a) schematic; (b) real setup.

Specimens with known dimensions and artificial defects (Figure 4.31(a)) were prepared as samples under tests. The artificial defects were thin (1.5~2 mm) slots created with a bandsaw. The smaller specimen was made of aluminum and the bigger specimen was made of steel. Five signature test points (five black crosses marked by A, B, C, D, and E in Figure 4.31(b)) were picked on the specimens. A and B were picked on the centerline of the steel specimen. A was right above the center of the defect; and B had a 20 mm offset from A to the edge without chamfer. C, D, and E were picked on the centerline of the aluminum specimen. C was right above the center of the longer defect, D was right above the center of the smaller defect, and E had a 30 mm offset from C to D. In this experiment, the driving voltages from the lab power source were set to ±32.5V (maximum setting) for the positive and negative rail, respectively.



(a)

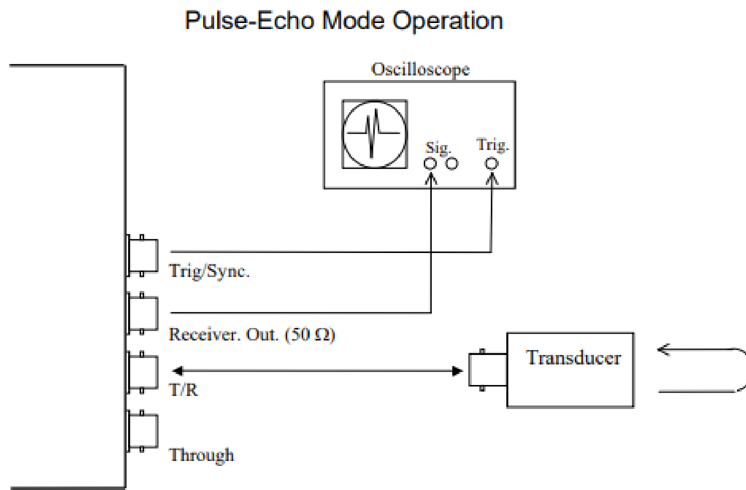


(b)

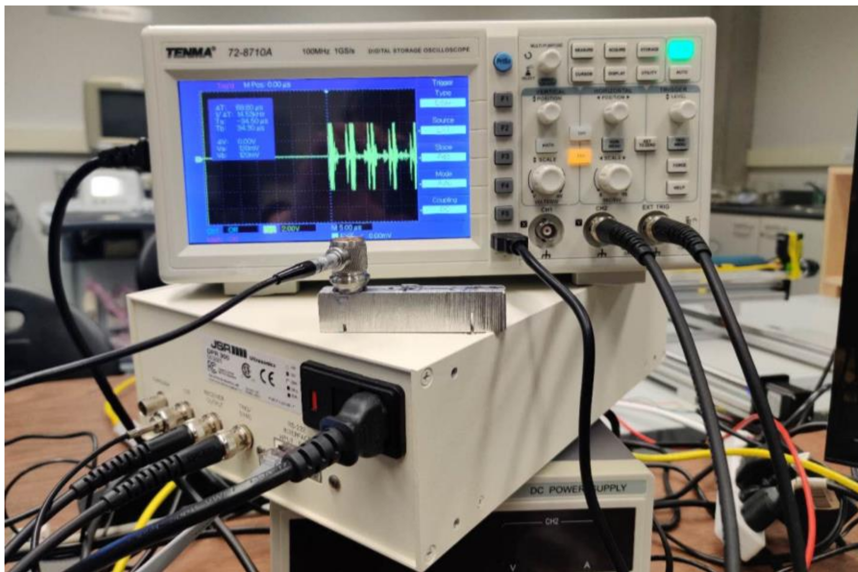
Figure 4.31: Specimens with artificial defects (a) dimensions; (b) test points (on black crosses).

4.5.2 Benchmark Experiment

The benchmark experiment was conducted with JSR DPR300 Pulser/Receiver unit. DPR300 is a commercially available ultrasonic pulser which can conduct T/R ultrasonic pulsing. The unit can be configured with a host computer by an interface software provided by JSR (JSR Control Panel). It has a 35MHz receiver bandwidth and an adjustable low-noise receiver gain up to 80 dB. High pass and low pass filter can be applied during the measurement [150]. Test setup and real configurations are shown in Figure 4.32.



(a)



(b)

Figure 4.32: Experiment setup for benchmark tests (a) schematic [150]; (b) real setup.

In this experiment, the data were acquired with the help of the oscilloscope (TENMA 72-8710A). The T/R measurements were performed on the same five positions as in the validation experiment. The detailed parameter setup can refer to Figure 4.33.

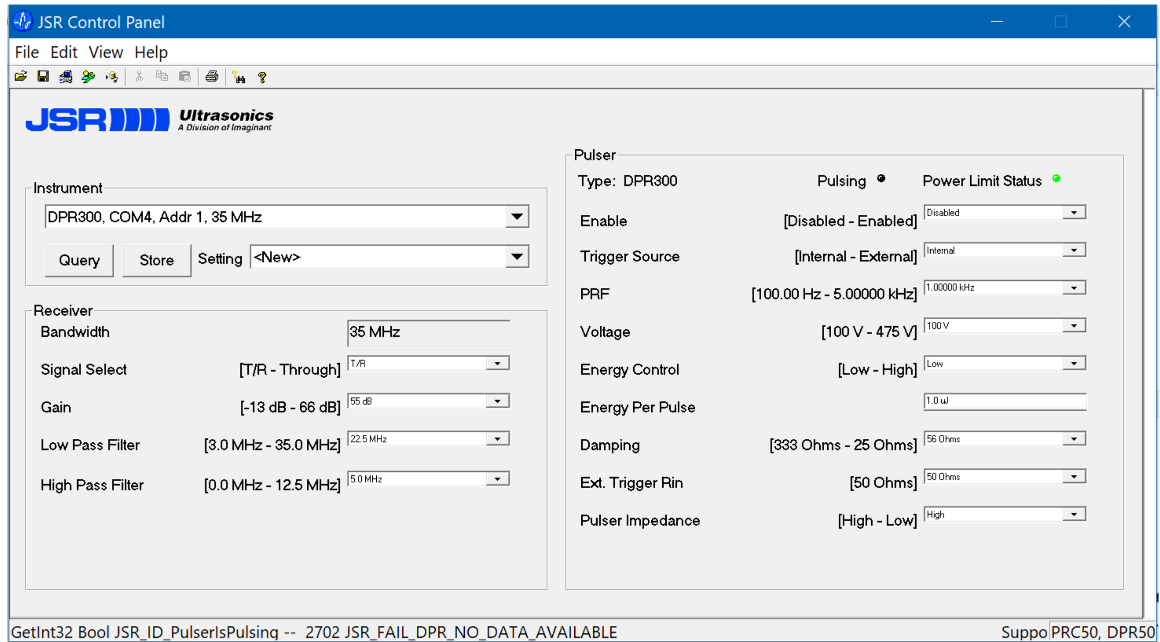


Figure 4.33: Parameters for JSR DPR300.

The results acquired using the DPR300 and oscilloscope were compared with the results acquired from the validation tests to serve the purpose of benchmarking. It should be noted that the minimum pulse voltage available for JSR DPR300 is 100V. Because the maximum voltage which the lab power source can achieve was 32.5V, the output was not comparable directly. Therefore, the results were normalized with (4.10) to provide a better comparison.

$$x_{normalized} = \frac{x_{original} - x_{min}}{x_{max} - x_{min}} \tag{4.10}$$

4.5.3 Voltage Level Experiment

The voltage level affects the results. To further investigate the issue, an experiment was conducted to evaluate the effect by adjusting the outputs from the lab source. Although it was not possible to boost the voltage beyond 32.5V for this prototype, it could provide some insight on the matter. The test setup was identical to Figure 4.30. The voltages used in this experiment ranged from 5V to 30V with a step size of 5V.

4.5.4 Smart Detection Experiment

From the voltage experiment, the relationship between the defect echo amplitude and the input voltage can be determined. Based on the parameters in algorithm that were implemented on the FPGA, the minimum voltage setting to allow the auto detection work for the defects in the specimens can be determined. This experiment was setup to examine the performance of the on-board processing. The test setup also resembles Figure 4.30.

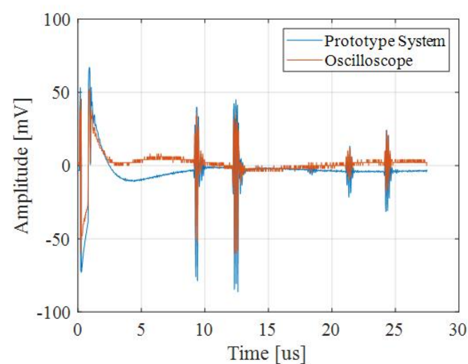
4.5.5 Other Functional Tests

Some miscellaneous tests were conducted to show other functions of the device. The experiment and tests so far have not covered the pulsing frequencies, therefore, a small experiment concerning this feature was conducted. The second functional test concerned envelope detection IC on the AFE. Comparisons of the test results from the envelope detection output were made between the non-defect and defect locations. After these two tests, a brief summary on the C code efficiency was given to show the capability of the system in a full data acquisition cycle.

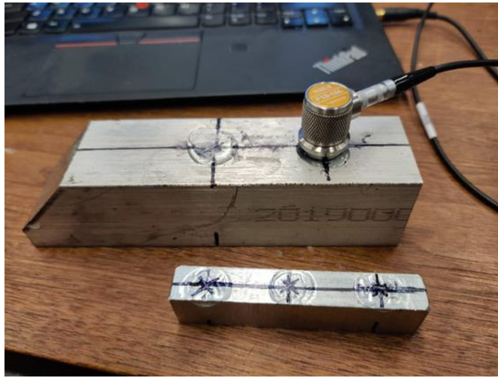
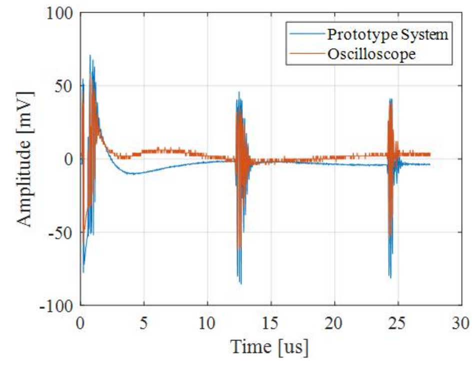
4.6 Experiment results

4.6.1 Data Validation Experiment

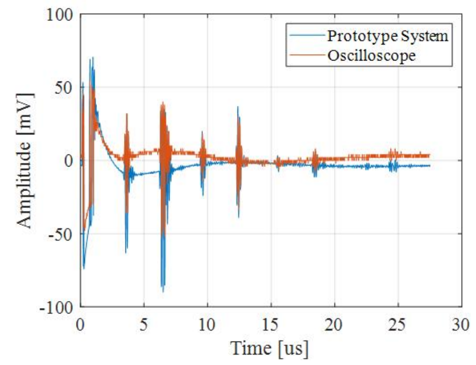
The results of the data validation experiment are shown in Figure 4.34.



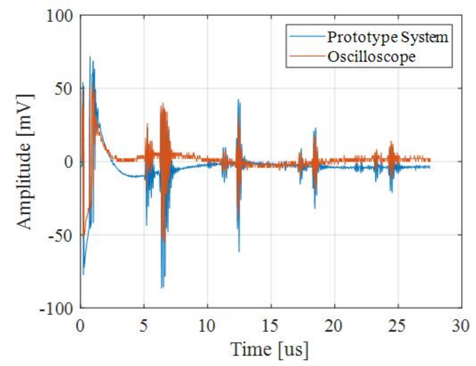
(a)

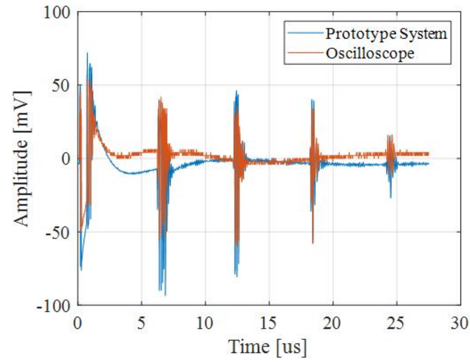
(b)



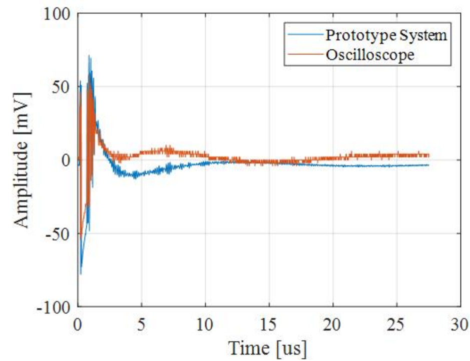
(c)



(d)



(e)



(f)

Figure 4.34: Validation test results: (a) to (e) corresponds to the results from test points A to E; (f) shows the probe response without contact.

From the test results shown in Figure 4.34, the measurement from the prototype system has a larger disturbance in the base trend than the oscilloscope data. This discrepancy may not only come from the devices, it can also be a consequence of cable connections. Referring to the connection shown in Figure 4.30(b). The signal does have to go through a longer route to reach FPGA than oscilloscope. Some phase differences in very low frequency components can be excused. This problem can also be fixed in future design with embedded high pass filters.

Moreover, the RF signals are considered as sparse vectors, so the useful information are signals with bigger amplitudes at the pulse locations. Comparing the pulse measurement, 10%~20% difference can be found in amplitudes. But the pulse magnitudes have a similar

overall trend in both devices. It seems to be a global problem and can be improved with a better calibration method. Nevertheless, the amplitudes demonstrate a similar trend in both configurations. In Figure 4.34(a), (c), and (d), the premature echo signals and the boundary reflections can be identified easily.

It can be concluded from the validation tests that although some discrepancies exist in the oscilloscope data and FPGA data, the key aspect in the data, timing, is identical. The amplitude variations in both devices are also similar. Therefore, the measurement data from the FPGA can be used as a basis to do the analyses.

4.6.2 Benchmark Experiment

Figure 4.35 shows the normalized comparison between the data acquired from DPR300 and the prototype system.

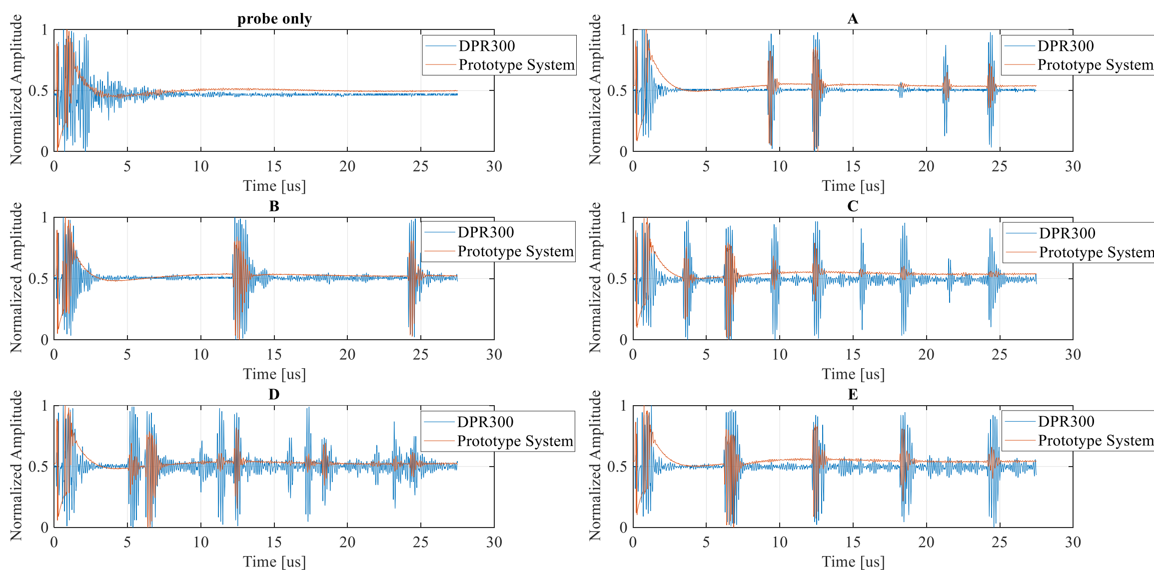


Figure 4.35: Normalized test data from DPR300 and the prototype system.

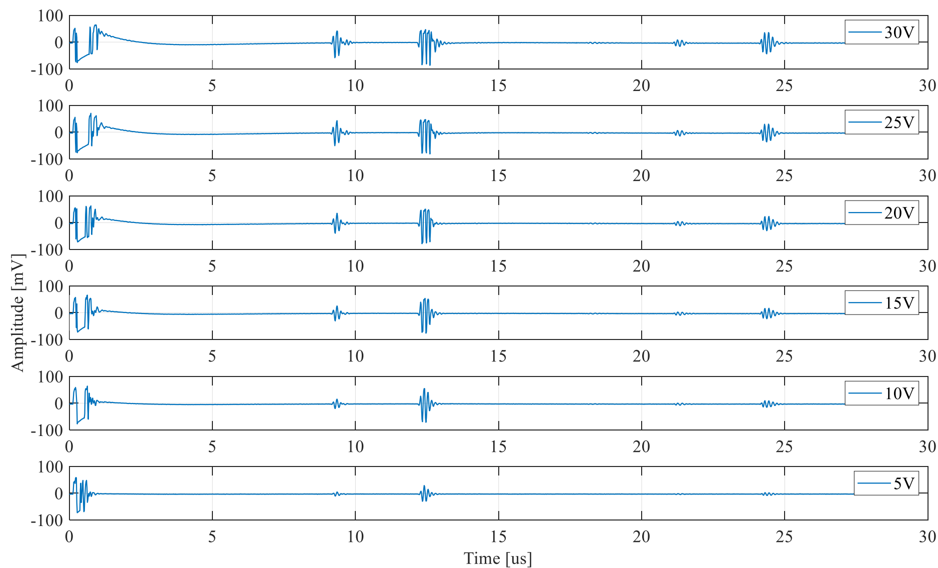
The original amplitude from the DPR300 measurement is within a range approximately ±4V. The results from DPR300 does not have a distortion in the base, because both the high-pass and low-pass filters are applied during the tests. It can be deduced from the test results that the HV voltage settings are critical for the clarity and defect detection capability. For

example, from data on D in Figure 4.35, some small disturbances can be identified by the prototype measurement, but they are much clearer in the DPR300 results. The pulses picked up by the prototype system align well with the signals received in the commercial system.

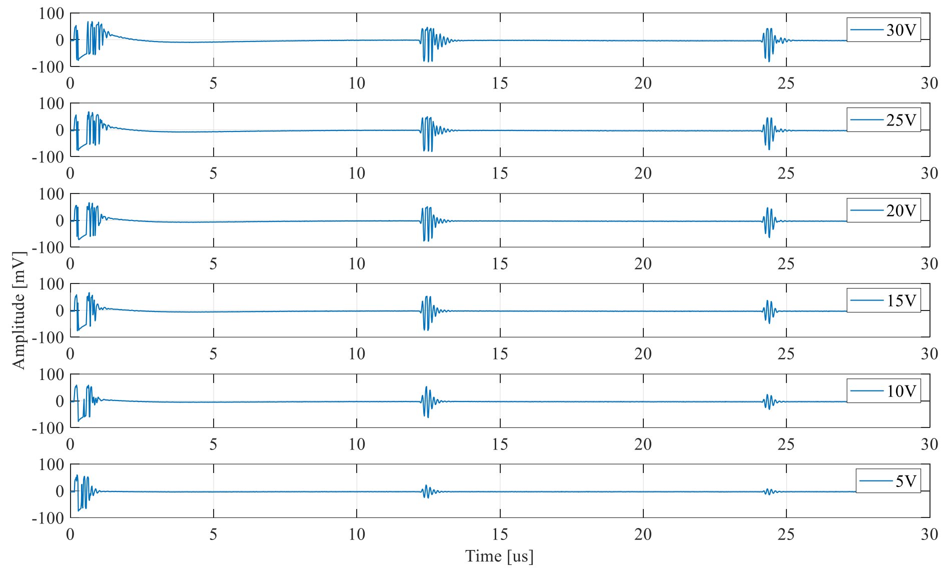
In conclusion, the prototype system can fulfill the needs for mm- to cm-level thickness detections or mm-level defect detections as demonstrated using the prepared specimens according to the results in Figure 4.34 (a), (c), (d) and Figure 4.35. It requires refinement especially in the signal quality in the analog end. An increase in the input HV voltages has the priority. The voltage level in this design (~30V) may not be enough for more demanding tasks like micron- or submicron-level detections.

4.6.3 Voltage Level Experiment

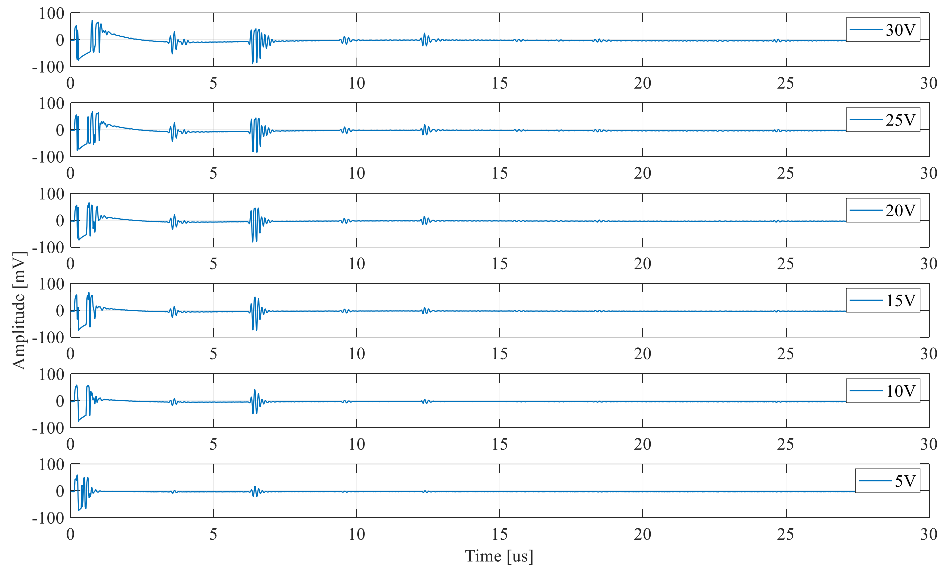
Figure 4.36 shows the RF signal acquired with different voltage settings in five picked locations.



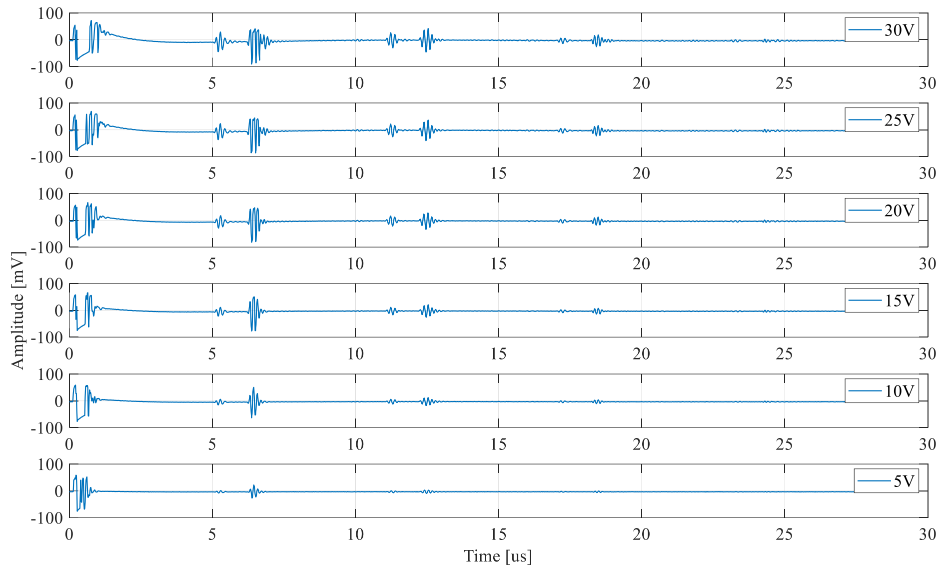
(a)



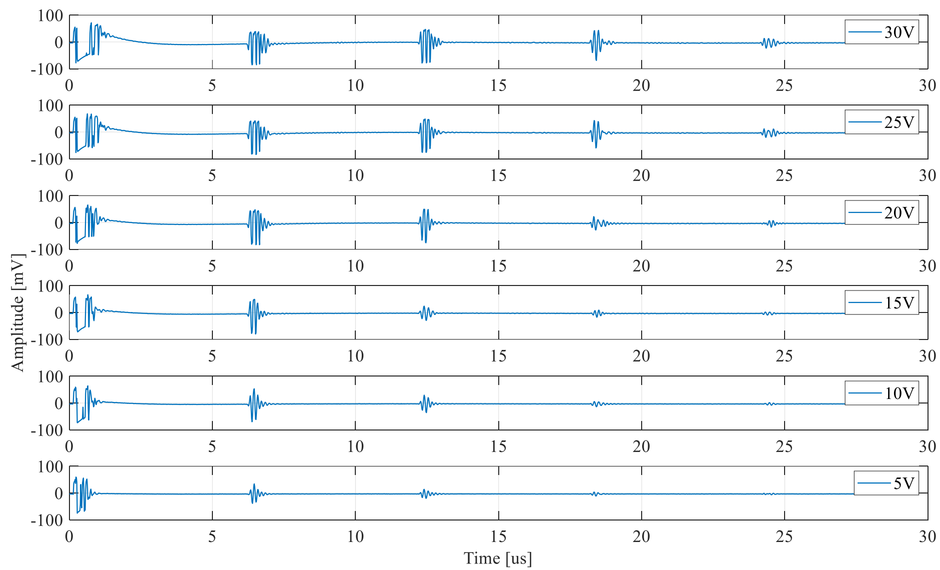
(b)



(c)



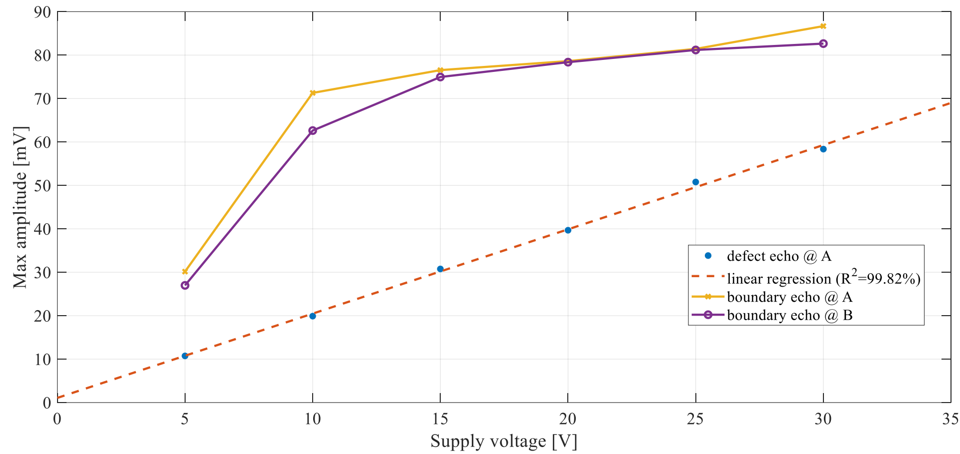
(d)



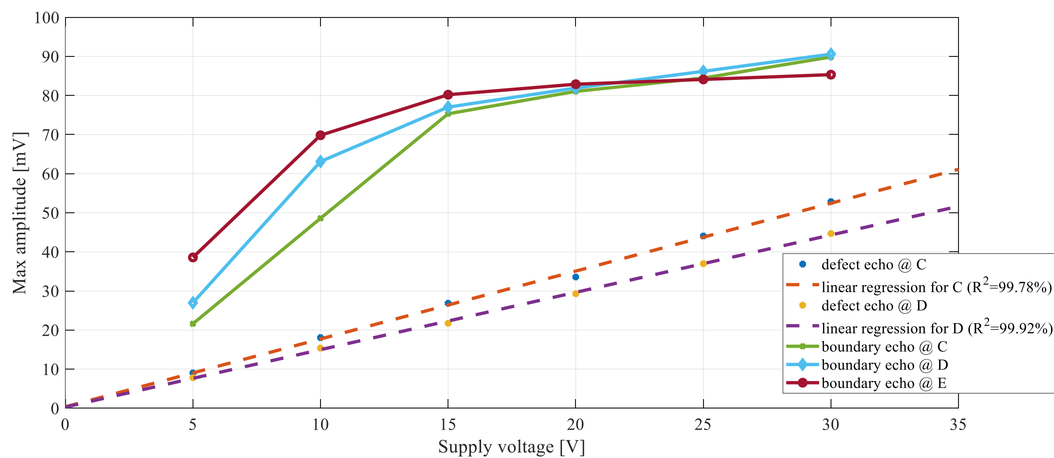
(e)

Figure 4.36: Voltage level experiment results: (a) to (e) are results on test points A to E, respectively.

From Figure 4.36, it is obvious that the reduction in voltage weakens the amplitudes in the echo pulses. It also reduces the base screw in the signal, as a “flatter” response can be observed in lower voltage settings. Collect the maximum absolute values for the first thickness echo and premature echo (if exists), the following relation between the collected values and driving voltages can be established (Figure 4.37).



(a)



(b)

Figure 4.37: Measurement voltages for defect and thickness boundary vs. supply voltage: measurements on (a) the steel specimen (A and B); (b) the aluminum specimen (C, D, and E).

In measurement on the steel specimen shown in Figure 4.37(a), there is an obvious turning point at 10~15V for the boundary echo amplitude. Although the change in maximum value stalls in its increment, the width of the pulse seems to be increasing as shown in Figure 4.36 for cases where >15V were used. As for the defect echo signal intensity, it keeps increasing linearly with the increase of the driving voltage. Similar observations can be made in Figure 4.37 (b) where the data are captured in aluminum measurement. The linear increment in the defect echo amplitudes supports the suggestions followed by the benchmark tests. The increase in the input voltage can help identify defects more easily and should be implemented as a priority. To find smaller defects, only high frequency is not enough, more power should be transmitted into the object to create sensible echo signals. However, for the thickness measurement, the evident pulses created by the boundary reflections can be easily identified even with a lower voltage setting. The voltage test results also suggest that the amplitude changes may have some potential to be used as a piece of information in the analysis. The depth difference of the artificial defect in this test not only generates different time delay in receiving the defect echo, it also results in a different reflecting amplitude. This observation can also be inferred from the commercial setup results in Figure 4.35, as different amplitude should indicate different level of detection. It can either be caused by the size, or the depth effect. The linearity coefficient may also be useful, but it requires further tests and analysis.

In conclusion, the prototype can be used as a development platform to study the effect of various settings in the system. It can be easily converted into a portable device which can conduct thickness or mm-level detection with low voltage power supply.

4.6.4 Smart Detection Experiment

If we convert the voltage responses for the defect echo shown in Figure 4.37 back to the raw values after the offset adjustment from the measurement, Figure 4.38 can be determined. Based on the simple detection algorithm discussed in Section 4.3.3.4, to be a valid count in the detection level, the data value should be larger than 28. In Figure 4.38, it can be concluded that to ensure all the artificial defects accumulate enough counts to be sensed, ~±22V should be applied in the test.

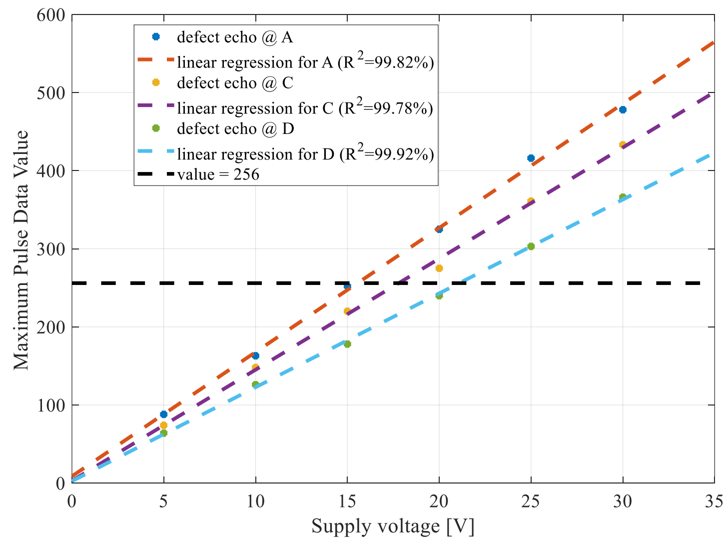
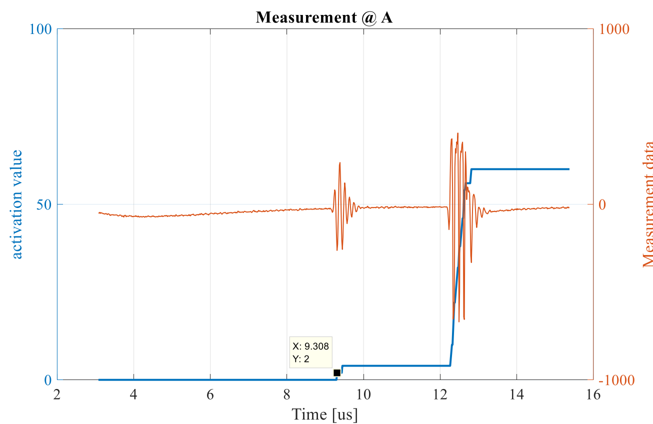
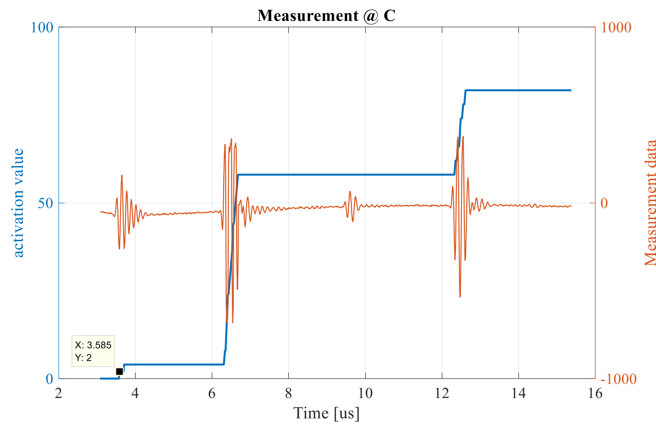


Figure 4.38: Linear relationship between supply voltage and max. value for the pulse data.

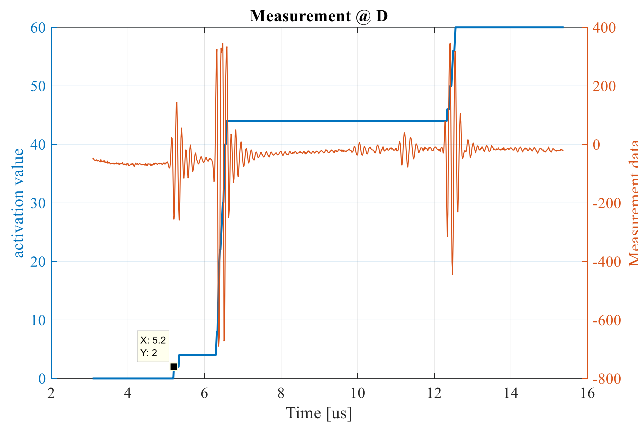
Given the fact that the trigger count for the detection was 3, ±25V were applied to guarantee the detection in tests. When a defect detection is triggered in the test, the data will be automatically saved to the micro-SD card. Take the saved data and process them with a replicate algorithm in MATLAB, the following results can be obtained (Figure 4.39). Note that the in the MATLAB simulation, each data point was expanded with one successive data point holding the same value to compensate for the doubled clock frequency in the smart detection block.



(a)



(b)



(c)

Figure 4.39: Simulation results from MATLAB for (a) test point A; (b) test point C; (c) test point D; blue lines are accumulated detection counts and orange curves are measurement data.

The data collected from the HEX display (decimal number in the parentheses), onscreen time, and MATLAB simulation are summarized in Table 4.1.

Table 4.1: Defect detection results

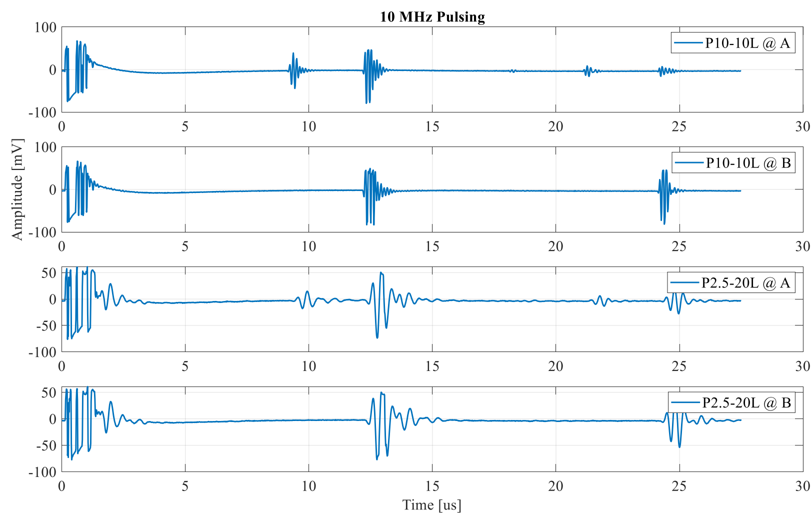
	Test on A	**Test on C**	**Test on D**
HEX display	267 (606)	F2 (242)	15C (348)
Time (us)	9.45	3.72	5.35
MATLAB time (us)	9.31	3.59	5.20

From Table 4.1, the detection time data in MATLAB are all slightly earlier than the reported time from the VGA display because of the delays in the data processing for absolute value calculations. Since the detection in smart detection block is based on the concurrent reading of the word count from the read control block, combined with the doubled clock frequency, the reported time would have some unpredictable but minor deviations. Overall, the smart detection block successfully reported the existence of all the mm-level artificial defects. The algorithm can be improved in multiple ways. Here are some examples:

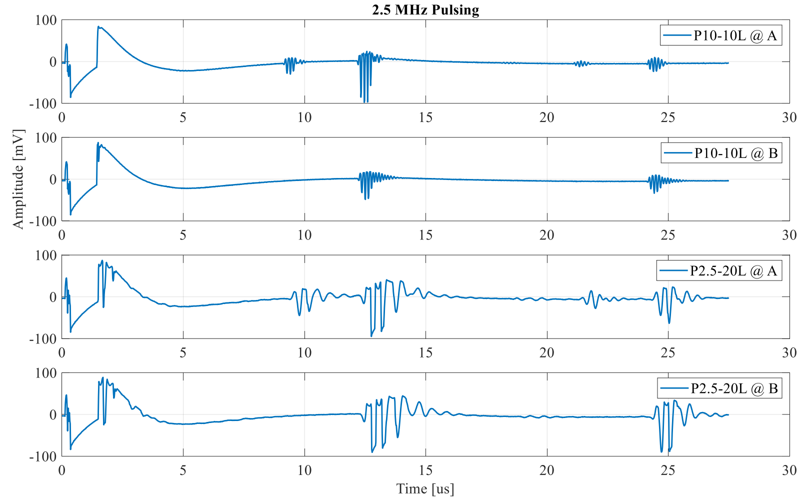
1. The minimal detection range can be optimized based on field measurement data
2. The minimal offset required to report a new detection can be adjusted
3. The data processing technique can be improved to use more complicated math

4.6.5 Other Functional Tests

The pulsing frequency tests were performed on the steel specimen at point A and B with ±25V input HV voltages. Two different probes were used. One was the 10 MHz probe P10-10L (SIUI), and the other was 2.5 MHz probe P2.5-20L (SIUI). Two pulsing conditions were tested (10 MHz and 2.5 MHz). The results are presented in Figure 4.40.



(a)



(b)

Figure 4.40: Test results under (a) 10 MHz pulsing; (b) 2.5 MHz pulsing.

Compare Figure 4.40(a) to Figure 4.40(b), the initial distortion is bigger in 2.5 MHz pulsing condition. In Figure 4.40(a), using P2.5-20L with 10 MHz pulse seems to be acceptable. But the waveform differences show that P10-10L still has the advantage of response time as some slight lag can be observed when using the 2.5 MHz probe. On the other hand, in Figure 4.40(b), P10-10L does not work well with the 2.5 MHz pulse, while the lag in P2.5-20L is still visible. Amplitude wise, using the P2.5-20L could acquire a larger response than using P10-10L. The larger element size of P2.5-20L (20 mm) than P10-10L (10 mm) may contribute to this result. From the results in Figure 4.40(a), it can be inferred that the probes worked as bandpass filters during the application. The vibrations excited inside the material are “filtered” by both probes and then the signal is sampled by the ADC. Because the sampling frequency by ADC is much higher (65 MHz) than the probe frequencies, the “frequency selection” performed by the probes can be observed. The ceiling frequency of the bandwidth of the input pulse sets the maximum working frequency of the probe, but the measurement accuracy and sensitivity are determined by the input energy, aperture of the probe, and the center frequency of the probes.

The AFE envelope test was done using both probes on the steel specimen at point B. The input HV voltages were set to ±32.5V. As demonstrated in Figure 4.41, after going through the on-board envelope detection, the signal can hardly provide useful information on the defect, although it may still be able to be used as a thickness measurement reference. Therefore, this on-board function should be substantially revised or excluded in the next design.

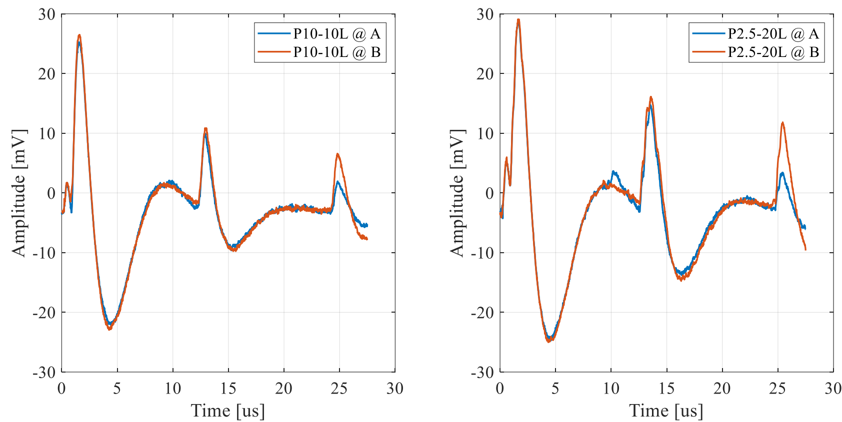


Figure 4.41: Envelope detected for measurements on the steel specimen with P10-10L and P2.5-20L.

When toggling on the switch (SW7), the timing function coded in C can provide real-time measurement on the time elapse during the NDT process. It was found that it took ~5300 us for a typical cycle (data transferring and VGA display) in C program to finish. ~7000 us was need if a data recording request was made during the cycle. The typical time for data transfer required 330 us, but the VGA display took 3000~5000 us to finish. Therefore, for each display update, there are about 5 to 6 data refresh operations. It may not be a critical issue because the VGA display is merely a reference. The data operation can be carried out without any VGA memory operations. For a typical 5300 us cycle, the screen refresh rate, if supported, can go up to ~180 FPS. But the VGA in the system is set to be 60 FPS. The bottleneck for the refresh rate in this case is the memory operation speed. The PRF in the design is 1000 kHz, which leaves an 1ms window for all the operations. Based on the elapsed time in the real setup, data from every pulse can be analyzed and saved if necessary.

4.6.6 Summary

The test results in Figure 4.35 make it very clear that the HV input voltages in the current design are not enough for more demanding applications. To further expand the application, higher voltage source should be developed. Other than the HV voltage rating, the design for power has another challenge from the power supply. The system is aimed to be portable. Therefore, it is not possible to carry around a big package like the lab power source. The next design should include both AC adapters for possible wall mount and an on-board rechargeable battery pack for portability.

There are some background noise frequencies in the measurement data. Some more specific filtering should be implemented onto the signal to provide a better signal quality. As described in Section 4.6.5, the on-board envelope detection chip is not working well. This chip is not essential in the design, and the function of this IC can be included into the FPGA programming because it is a chip used in digital signal processing. The on-board connections should be further secured, and proper shielding must be developed for portable applications to face possible environmental hazards.

The number of data points saved in the current settings is 2048, which lasts about 31.5 us with 65 MHz sampling rate in the design. In the future designs, higher sampling rate may be needed, and the system may work on larger structures. Then, a larger space to store more data is required. It would be better to make use of either the 64MB SDRAM on board or, even better, the 1GB DDR3 RAM on the HPS side for a larger storage space. The SRAM scratch pad can still be used as a buffer, but it may not be suitable as a permanent storage solution for real projects.

It is worth noting that the VGA drawing in this project is implemented through the calculations in the C program, i.e., it is a software-driven display. Hence, it is relatively slow since the VGA port is directly hooked to the FPGA side. If a GPU processor can be written on the FPGA fabric, the whole process can be more efficient. It can also reduce the unnecessary data transfer between the two fabrics so that it can make way for other data transfer demands. Currently, The VGA display is working at 640x480 in 8bits. The pixel

count limits the capability of data display. If the GPU system is made, because of the efficiency boost in data transfer, the display and color resolution can be increased. Then, more data can be displayed at the same time.

Chapter 5

Conclusions and Future Work

5.1 Ultrasonic Vibro-tactile Sensor

The hybrid approach, which starts with a simplified analytical model followed by an FEA refinement, proved successful in designing the vibro-tactile sensor. The vibration concentrator included into the design was effective, which increased the quality factor (Q_m) of the design from 1,244 to 3,896. In terms of vibration behavior, it reduced the difference between the series and parallel resonance frequencies from 1500 Hz to 90 Hz so that the electrical resonance frequencies can provide direct indication for their mechanical counterpart.

In the tactile sensing experiment, the frequencies of electrical resonances demonstrated similar robustness (CV: coefficient of variation < 0.05% in most measurements) to the established mechanical resonance frequencies. The frequency shifts in electrical resonances can be applied to the full sensing range available with the current samples (10 kPa to 140 kPa). The derived equivalent conductance of the load G_{load} was theoretically feasible to estimate the elastic modulus of the load and showed the potential to disregard the excessive modulus from the metallic sensor structure. In the experiment, the average data from G_{load} exhibited better linearity ($R^2 = 0.9998$) than electrical series resonance frequency shift Δf_1 ($R^2 = 0.9947$), electrical parallel resonance frequency shift Δf_2 ($R^2 = 0.9842$), and maximum phase angle frequency shift $\Delta f_{m\phi}$ ($R^2 = 0.9935$), in the valid sensing range (10 kPa and 70 kPa). However, the spikes in CV values made it hardly practical for trustworthy measurement. At the same time, the electrically determined equivalent circuit parameters suffered from the practical limitations from either driving voltage or inherent properties of the piezoelectric material in the vibration driver. Therefore, the frequency shifts from electrical resonances seem to be the best candidate for determining the elastic modulus, while the equivalent circuit parameters can be used only for references with the current setup.

As a future work, the underlying physics of the measurement should be further studied. The method of electro-mechanical analogy and the conventional vibration analysis should be combined to determine other parameters that are related to the material properties of the object and the vibration behavior of the sensor. Currently, although the equivalent electrical circuits can approximate the system electrical response with numerical fitting technique, the connections between these electrical components and the actual mechanical parameters are yet to be elucidated.

In summary, the vibro-tactile sensor can conduct non-destructive measurement on the elastic modulus (E) of soft materials in lab environment. However, the sensitivity of vibration behavior brings too many restrictions alongside its benefits. Further structural improvement is necessary for the vibro-tactile sensor to have better signal to noise ratio. The drawbacks in manipulation difficulties can be addressed with robotics. Vibro-tactile sensors are still promising probes to be used in non-destructive testing for soft materials.

5.2 FPGA-based Ultrasonic System

The developed FPGA-based ultrasonic system is easy to setup and field-programmable. The current system design included digital-to-analog (DA) and analog-to-digital (AD) conversions, high-voltage (HV) amplification, pulse multiplexer, delay-line design, software processing, and on-board hardware signal acquisition and processing. Although the currently developed system only supports one-channel detection, the necessary parts for the future phased-array modification have been implemented and tested. The implementation of the hardware-based algorithm demonstrated its capability of direct signal processing while data acquisition was performed.

In the design of the analog front end (AFE), it was found that the envelope detection IC was not worth it in the design. The HV input for AFE was not enough to comfortably detect defects less than mm-level. There was some low-frequency noise in the acquired signal, which indicates the necessity of including filters to the analog circuits. The design of the AFE board lacks the considerations for securing its position. Some mounting mechanism should be included in the future design. The arrangement of the I/O was also not optimal. It

should be considered more seriously when moving on to the phased-array AFE design, where the trace length can cause issues on the timing.

As for the FPGA, the functions required to make the system work have been implemented. However, the prototype requires further polishing to fully make use of the ability of an FPGA. Currently, the display was implemented with software. The VGA display had a low resolution (640x480x8) comparing to today's modern technology (4Kx32). This was partly attributed to the limitations of the FPGA itself, but there was still plenty of resources on the FPGA that was not utilized. Similar situation happened in the data transactions and storage. Most of the operations were done using the on-chip memory (SRAM), which is fast but expensive. The optimization can start with making use of the SDRAM and DDR3. Current algorithm applied on the ultrasonic signal was effective but rather primitive. To improve the performance and expand the application, more advanced algorithms, such as AI, should be developed and implemented. It can be done with the help of the high-level synthesis (HLS) provided by the development suite. Considering the limitations in the software provided by Intel, it may be wise to change the platform to Xilinx FPGAs. In order to live up to the claim of in-line NDT system, the FPGA-based system should be further developed to coordinate with robotics in the future.

Nevertheless, the prototype was working smoothly, and the primary concept of the data acquisition, processing, and communications were successfully carried out.

5.3 Contributions

5.3.1 Vibro-tactile Sensor

For vibro-tactile sensor, the design scheme for the ultrasonic concentrator was developed by adopting the electro-mechanical analogy, which could enhance the performance of the vibro-tactile sensor. A prototype was fabricated with the proposed methods and experiments were designed and conducted to test the performance. Based on the experimental results, electrical parameters were proposed as indicators for the elastic modulus of the object. Academically, four journal papers were produced from project:

1. Qian, Y.J., Han, S.W. and Kwon, H.J., 2016. Development of ultrasonic surface treatment device. In Applied Mechanics and Materials (Vol. 835, pp. 620-625). Trans Tech Publications Ltd.
2. SadeghiGoughari, M., Qian, Y., Jeon, S., Sadeghi, S. and Kwon, H.J., 2018. An experimental and numerical study on tactile neuroimaging: A novel minimally invasive technique for intraoperative brain imaging. The International Journal of Medical Robotics and Computer Assisted Surgery, 14(2), p.e1893.
3. Qian, Y., Han, S.W. and Kwon, H.J., 2019. Design of an Ultrasonic Concentrator for Vibro-Tactile Sensors Using Electro-Mechanical Analogy. International Journal of Precision Engineering and Manufacturing, 20(10), pp.1787-1800.
4. Qian, Y., Salehian, A., Han, S.W. and Kwon, H.J. 2020. Design and analysis of an ultrasonic tactile sensor using electro-mechanical analogy. Ultrasonics, Volume 105, 106129.

Among them, the first one is related to the electro-mechanical modelling of the ultrasonic vibration concentrator. The second one is concerned with the applications of the tactile sensing. The third and fourth ones describe the electro-mechanical design and analysis of the ultrasonic vibro-tactile sensor. The methodology and experiments in these publications are also covered in the thesis.

5.3.2 FPGA-based Research Platform

Fully functional ultrasonic pulse-echo sensing system prototype was developed. Hardware processing with parallelism was achieved with an FPGA-based DIY system. The effect of voltage level in ultrasonic testing was elucidated.

5.3.3 Engineering Designs

Other than the vibro-tactile sensor and FPGA-based system prototypes, technological support was provided to the local industry through both projects. During the development of the FPGA-based system, customized PCB and software were developed for a digital anglometer which has been commercialized. The projects concerned in this thesis were not only for

research purposes but also benefit a local industry partner so that they can develop technologies in mechatronics to make transitions towards next generation industry 4.0.

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Appendix A
Longitudinal Speed of Sound in Common Medium

The longitudinal speed of sound (c) in a material can be calculated with

$$c = \sqrt{\frac{E}{\rho}} \tag{A.1}$$

where E is the elastic properties and ρ is the density.

However, the sound speed in air requires the correction on temperature,

$$c = 331 + 0.6T \tag{A.2}$$

where T is the temperature in Celsius.

	Medium	**Speed of Sound [m/s]**
Sink Medium	Air (20 °C)	343
	Air (0 °C)	331
	Water (25 °C)	1493
	Sea Water (25 °C)	1533
High damping medium	Rubber	150
	Lead	1320
	Cork	518
Possible selections for structure design	Pyrex glass	5640
	Aluminum	5100
	Iron	5130
	Steel	6100
	Stainless steel	5790
	Wood (along the fiber)	1390 ~ 4670
	Brick	4176
	Titanium	6070
Typical electrode material	Gold	3240
	silver	3650
	Copper	3900

References: [151–154]

Appendix B
Derivation for (2.8)

Starting with Newton's Law:

$$F = ma \tag{B.1}$$

$$S\sigma = \rho V a \tag{B.2}$$

$$\frac{\partial (S\sigma)}{\partial x} dx = S\rho dx \frac{\partial^2 \xi}{\partial t^2} \tag{B.3}$$

$$\frac{\partial S}{\partial x} \sigma dx + S \frac{\partial \sigma}{\partial x} dx = S\rho dx \frac{\partial^2 \xi}{\partial t^2} \tag{B.4}$$

Inserting: $\sigma = E \cdot \frac{\partial \xi}{\partial x}$ into (B.4)

$$\frac{\partial S}{\partial x} E \frac{\partial \xi}{\partial x} dx + SE \frac{\partial^2 \xi}{\partial x^2} dx = S\rho dx \frac{\partial^2 \xi}{\partial t^2} \tag{B.5}$$

$$\frac{\partial^2 \xi}{\partial x^2} + \frac{1}{S} \frac{\partial S}{\partial x} \frac{\partial \xi}{\partial x} + -\frac{\rho}{E} \frac{\partial^2 \xi}{\partial t^2} = 0 \tag{B.6}$$

Recall $\frac{\rho}{E} = \frac{1}{c^2}$ and $k = \frac{\omega}{c}$. Note that for harmonic vibration

$$\xi(x,t) = \xi(x) e^{j\omega t} \Rightarrow \frac{\partial^2 \xi}{\partial t^2} = -\omega^2 \xi \tag{B.7}$$

$$\frac{\partial^2 \xi}{\partial x^2} + \frac{1}{S} \frac{\partial S}{\partial x} \frac{\partial \xi}{\partial x} + k^2 \xi = 0 \tag{B.8}$$

Additional comments:

Within the derivation, we can see that when the cross-sectional area is constant, we can derive the wave speed in uniform solid rod with the wave equation.

$$\frac{E}{\rho} \frac{\partial^2 \xi}{\partial x^2} = \frac{\partial^2 \xi}{\partial t^2} \Rightarrow c = \sqrt{\frac{E}{\rho}} \tag{B.9}$$

Appendix C

Derivation for (2.9)

Given

$$\frac{\partial^2 \xi}{\partial x^2} + \frac{1}{S}\frac{\partial S}{\partial x}\frac{\partial \xi}{\partial x} + k^2 \xi = 0 \tag{C.1}$$

Let $K^2 = k^2 - \frac{1}{\sqrt{S}}\frac{\partial^2 \sqrt{S}}{\partial x^2}$ and $y = \sqrt{S}\xi$,

$$\underbrace{\boxed{\frac{\partial^2 \left(\frac{1}{\sqrt{S}}y\right)}{\partial x^2}}}_{\mathbb{A}} + \underbrace{\boxed{\frac{1}{S}\frac{\partial S}{\partial x}\frac{\partial \left(\frac{1}{\sqrt{S}}y\right)}{\partial x}}}_{\mathbb{B}} + K^2\left(\frac{1}{\sqrt{S}}y\right) + \underbrace{\boxed{\frac{1}{\sqrt{S}}\frac{1}{\sqrt{S}}y\frac{\partial^2 \sqrt{S}}{\partial x^2}}}_{\mathbb{C}} = 0 \tag{C.2}$$

$$\begin{aligned} \mathbb{A}: \frac{\partial^2 \left(\frac{1}{\sqrt{S}}y\right)}{\partial x^2} &= \frac{\partial}{\partial x}\left(\frac{\partial y}{\partial x}\frac{1}{\sqrt{S}} + \frac{\partial \left(\frac{1}{\sqrt{S}}\right)}{\partial x}y\right) \\ &= \frac{\partial^2 y}{\partial x^2}\frac{1}{\sqrt{S}} + \underbrace{\boxed{\frac{\partial^2 \left(\frac{1}{\sqrt{S}}\right)}{\partial x^2}y}}_{\mathbb{D}} + \underbrace{\boxed{2\frac{\partial \left(\frac{1}{\sqrt{S}}\right)}{\partial x}\frac{\partial y}{\partial x}}}_{\mathbb{E}} \end{aligned} \tag{C.3}$$

$$\mathbb{D}: \frac{\partial^2 \left(\frac{1}{\sqrt{S}}\right)}{\partial x^2}y = \left[\frac{\partial}{\partial x}\left(-\frac{1}{S}\frac{\partial \sqrt{S}}{\partial x}\right)\right]y = -\frac{1}{S}\frac{\partial^2 \sqrt{S}}{\partial x^2}y + \frac{1}{S^2}\frac{\partial \sqrt{S}}{\partial x}\frac{\partial S}{\partial x}y \tag{C.4}$$

$$\mathbb{E}: 2\frac{\partial \left(\frac{1}{\sqrt{S}}\right)}{\partial x}\frac{\partial y}{\partial x} = -\frac{2}{S}\frac{\partial \sqrt{S}}{\partial x}\frac{\partial y}{\partial x} = -\frac{1}{S\sqrt{S}}\frac{\partial S}{\partial x}\frac{\partial y}{\partial x} \tag{C.5}$$

$$\mathbb{B}: \frac{1}{S}\frac{\partial S}{\partial x}\frac{\partial \left(\frac{1}{\sqrt{S}}y\right)}{\partial x} = \frac{1}{S}\frac{\partial S}{\partial x}\left(\frac{\partial y}{\partial x}\frac{1}{\sqrt{S}} + \frac{\partial \left(\frac{1}{\sqrt{S}}\right)}{\partial x}y\right) = \frac{1}{S\sqrt{S}}\frac{\partial S}{\partial x}\frac{\partial y}{\partial x} - \frac{1}{S^2}\frac{\partial \sqrt{S}}{\partial x}\frac{\partial S}{\partial x}y \tag{C.6}$$

$$\mathbb{C}: \frac{1}{\sqrt{S}}\frac{1}{\sqrt{S}}y\frac{\partial^2 \sqrt{S}}{\partial x^2} = \frac{1}{S}\frac{\partial^2 \sqrt{S}}{\partial x^2}y \tag{C.7}$$

Adding up (C.3) – (C.7) based on (C.2)

$$\frac{\partial^2 y}{\partial x^2}\frac{1}{\sqrt{S}} + K^2\frac{1}{\sqrt{S}}y = 0 \Rightarrow \frac{\partial^2 y}{\partial x^2} + K^2 y = 0 \tag{C.8}$$

Appendix D

Discussions on the inequality $K^2 > 0$ [121]

$$K^2 = k^2 - \frac{1}{\sqrt{S}}\frac{\partial^2\sqrt{S}}{\partial x^2} > 0 \Rightarrow k^2 > \frac{1}{\sqrt{S}}\frac{\partial^2\sqrt{S}}{\partial x^2} \tag{D.1}$$

Let $\gamma = \frac{1}{\sqrt{S}}\frac{\partial^2\sqrt{S}}{\partial x^2}$, another differential equation can be established

$$\frac{\partial^2\sqrt{S}}{\partial x^2} = \sqrt{S}\gamma \tag{D.2}$$

Solutions to this equation take different form based on the sign of γ

1. $\gamma < 0$

$$\sqrt{S} = C\, sin\sqrt{-\gamma}\, x + D\, cos\sqrt{-\gamma}\, x = R\, sin(\sqrt{-\gamma}x + \phi) \tag{D.3}$$

where $R = \sqrt{C^2 + D^2}$ and $\phi = \arctan\frac{D}{C}$. Therefore, the shape has a trigonometric profile.

2. $\gamma = 0$

$$\sqrt{S} = Cx + D \tag{D.4}$$

If $C = 0$, the shape has a cylindrical profile; otherwise, the shape has a conical profile.

3. $\gamma > 0$

$$\sqrt{S} = C \sinh\sqrt{\gamma}\, x + D \cosh\sqrt{\gamma}\, x \tag{D.5}$$

Note that

$$\begin{cases} \sinh x = \dfrac{e^x - e^{-x}}{2} \\ \cosh x = \dfrac{e^x + e^{-x}}{2} \end{cases} \tag{D.6}$$

If $C = 0$, the shape has a catenarian profile. If $C = \pm D$, the shape has a exponential profile.

For the first two cases, where $\gamma \leq 0$, the inequality $K^2 > 0$ will always be fulfilled. However, in the third case, where $\gamma > 0$, it depends. The condition for inequality to hold in

the third case is the requirement for the wave to propagate in the design. Take the exponential profile as an example, from (D.5), let $C = -D$

$$\sqrt{s} = Ce^{-\beta x} \tag{D.7}$$

Apply the boundary conditions $\begin{cases} x = 0 & S = S_1 \\ x = l & S = S_2 \end{cases}$,

$$\begin{cases} \sqrt{S_1} = C \\ \sqrt{S_2} = Ce^{\beta l} \end{cases} \Rightarrow \sqrt{\frac{S_2}{S_1}} = e^{-\beta l} \Rightarrow \beta = \frac{1}{l}\ln\sqrt{\frac{S_1}{S_2}} \tag{D.8}$$

Let $N = \frac{S_1}{S_2} = \frac{R_1}{R_2}$, then $\beta = \frac{1}{l}\ln N$.

$$\sqrt{S} = \sqrt{S_1}e^{-\beta x} \tag{D.9}$$

$$k^2 > \frac{1}{\sqrt{S}}\frac{\partial^2\sqrt{S}}{\partial x^2} = \frac{\beta^2\sqrt{S_1}e^{-\beta x}}{\sqrt{S_1}e^{-\beta x}} = \beta^2 \Rightarrow \frac{\omega}{\beta c} > 1 \Rightarrow f > \frac{\beta c}{2\pi} \tag{D.10}$$

(D.10) implies the dependency of the inequality on the frequency of the wave.

As for $K^2 > 0$,

$$\begin{aligned} & K^2 = k^2 - \beta^2 \\ & \Rightarrow \frac{1}{K} = \frac{1}{\sqrt{k^2 - \beta^2}} \\ & \Rightarrow \frac{\tilde{c}}{\omega} = \frac{c}{\omega\left[1 - \left(\frac{\beta c}{\omega}\right)^2\right]^{\frac{1}{2}}} \\ & \Rightarrow \tilde{c} = \frac{c}{\left[1 - \left(\frac{\beta c}{\omega}\right)^2\right]^{\frac{1}{2}}} \end{aligned} \tag{D.11}$$

From (D.11), it can be inferred that the speed of sound changes with the profile, and $\frac{\beta c}{\omega} < 1$ must be satisfied to allow the longitudinal waves propagate in the exponential profile rod.

Appendix E

Derivation for (2.16)

From the force equilibrium, we get

$$F = -S\sigma = -SE\epsilon = -SE\frac{\partial \xi}{\partial x} \tag{E.1}$$

Apply the boundary condition $\begin{cases} x = 0 & F = -F_1 & S = S_1 \\ x = l & F = -F_2 & S = S_2 \end{cases}$,

$$\begin{cases} F_1 = \dfrac{E}{2\sqrt{S_1}}\left(\dfrac{\partial S}{\partial x}\right)_{x=0} B - \sqrt{S_1}EKA \\ F_2 = \dfrac{E}{2\sqrt{S_2}}\left(\dfrac{\partial S}{\partial x}\right)_{x=l}(A\, sin\, K\, l + B\, cos\, K\, l) - \dfrac{K}{\sqrt{S_2}}(A\, cos\, K\, l - B\, sin\, K\, l) \end{cases} \tag{E.2}$$

Plug in the constants $\begin{cases} A = -\frac{\sqrt{S_2}\dot{\xi}_2 + \sqrt{S_1}\dot{\xi}_1\, cos\, Kl}{j\omega\, sin\, Kl} \\ B = \frac{\sqrt{S_1}\dot{\xi}_1}{j\omega} \end{cases}$

$$F_1 = \frac{E}{2j\omega}\left(\frac{\partial S}{\partial x}\right)_{x=0}\dot{\xi}_1 + \frac{S_1 EK}{j\omega}\frac{cos\, K\, l}{sin\, K\, l}\dot{\xi}_1 + \frac{\sqrt{S_1 S_2}EK}{j\omega\, sin\, K\, l}\dot{\xi}_2 \tag{E.3A}$$

$$F_2 = -\frac{E}{2\sqrt{S_2}}\left(\frac{\partial S}{\partial x}\right)_{x=l}\frac{\sqrt{S_2}\dot{\xi} + \sqrt{S_1}\dot{\xi}_1\, cos\, K\, l}{j\omega} + \frac{E}{2}\left(\frac{\partial S}{\partial x}\right)_{x=l}\sqrt{\frac{S_1}{S_2}}\frac{\dot{\xi}_1\, cos\, K\, l}{j\omega}$$

$$+\frac{\sqrt{S_2}EK}{j\omega \sin Kl}(\sqrt{S_2}\dot{\xi}\cos Kl + \sqrt{S_1}\dot{\xi}_1\cos^2 Kl) + \frac{\sqrt{S_1 S_2}EK\dot{\xi}_1}{j\omega}\sin Kl$$

$$= -\frac{E}{2j\omega}\left(\frac{\partial S}{\partial x}\right)_{x=l}\dot{\xi}_2 - \frac{E\, cos\, K\, l}{2j\omega}\sqrt{\frac{S_1}{S_2}}\left(\frac{\partial S}{\partial x}\right)_{x=l}\dot{\xi}_1 + \frac{E\, cos\, K\, l}{2j\omega}\sqrt{\frac{S_1}{S_2}}\left(\frac{\partial S}{\partial x}\right)_{x=l}\dot{\xi}_1 \tag{E.3B}$$

$$+\frac{S_2 EK}{j\omega}\frac{cos\, K\, l}{sin\, K\, l}\dot{\xi}_2 + \frac{\sqrt{S_1 S_2}EK(1 - sin^2 K l)}{j\omega\, sin\, K\, l}\dot{\xi}_1 + \frac{\sqrt{S_1 S_2}EK}{j\omega\, sin\, K\, l}\dot{\xi}_1$$

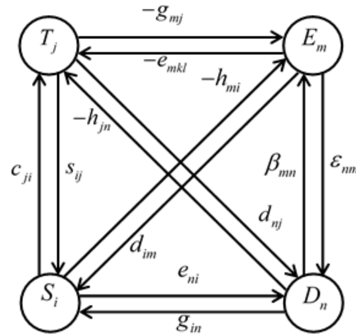
$$= -\frac{E}{2j\omega}\left(\frac{\partial S}{\partial x}\right)_{x=l}\dot{\xi}_2 + \frac{S_2 EK}{j\omega}\frac{cos\, K\, l}{sin\, K\, l}\dot{\xi}_2 + \frac{\sqrt{S_1 S_2}EK}{j\omega\, sin\, K\, l}\dot{\xi}_1$$

Knowing that $\begin{cases}\omega = kc \\ E = \rho c^2\end{cases}$, the final form can be easily found as

$$\begin{cases} F_1 = \dfrac{\rho c}{2jk}\left(\dfrac{\partial S}{\partial x}\right)_{x=0} \dot{\xi}_1 + \dfrac{\rho c K S_1}{jk} cot\, K\, l\ \dot{\xi}_1 + \dfrac{\rho c K\sqrt{S_1 S_2}}{jk\, sin\, K\, l} \dot{\xi}_2 \\ F_2 = -\dfrac{\rho c}{2jk}\left(\dfrac{\partial S}{\partial x}\right)_{x=l} \dot{\xi}_2 + \dfrac{\rho c K S_2}{jk} cot\, K\, l\ \dot{\xi}_2 + \dfrac{\rho c K\sqrt{S_1 S_2}}{jk\, sin\, K\, l} \dot{\xi}_1 \end{cases} \tag{E.4}$$

Appendix F

Relationships of the Parameters in Piezoelectric Materials [124]



Coefficient	Notation	Physical meaning	SI unit
Short-circuit compliance coefficient	s_{ij}^E	$(\partial S_i/\partial T_j)_E$	m2/N
Open-circuit compliance coefficient	s_{ij}^D	$(\partial S_i/\partial T_j)_D$	m2/N
Short-circuit stiffness coefficient	c_{ji}^E	$(\partial T_j/\partial S_i)_E$	N/m2
Open-circuit stiffness coefficient	c_{ji}^D	$(\partial T_j/\partial S_i)_D$	N/m2
Stress-free dielectric constant	ε_{nm}^T	$(\partial D_n/\partial E_m)_T$	F/m
Clamped dielectric constant	ε_{nm}^S	$(\partial D_n/\partial E_m)_S$	F/m
Stress-free impermittivity component*	β_{mn}^T	$(\partial E_m/\partial D_n)_T$	m/F
Clamped impermittivity component*	β_{mn}^S	$(\partial E_m/\partial D_n)_S$	m/F
Piezoelectric strain constant	d_{im} d_{nj}	$(\partial S_i/\partial E_m)_T$ $(\partial D_n/\partial T_j)_E$	m/V
Piezoelectric stress constant	e_{jm} e_{ni}	$-(\partial T_j/\partial E_m)_S$ $(\partial D_n/\partial S_i)_E$	N/(V·m)
Piezoelectric voltage constant	g_{in} g_{mj}	$(\partial S_i/\partial D_n)_T$ $-(\partial E_m/\partial T_j)_D$	V·m/N
Piezoelectric stiffness constant	h_{jn} h_{mi}	$-(\partial T_j/\partial D_n)_S$ $-(\partial E_m/\partial S_i)_D$	V/m

*impermittivity is the reciprocal of the permittivity

Appendix G

Derivation for (2.23)

Starting from Newton's Second Law,

$$F = ma \tag{G.1}$$

$$\frac{\partial(ST)}{\partial x}dx = S\rho dx\frac{\partial^2\xi}{\partial t^2} \tag{G.2}$$

$$\frac{\partial S}{\partial x}Tdx + S\frac{\partial T}{\partial x}dx = S\rho dx\frac{\partial^2\xi}{\partial t^2} \tag{G.3}$$

Since there is no change in the cross-sectional area, the term concerning the derivative of the shape function becomes zero. Recall (2.21)

$$T_3 = \frac{1}{s_{33}^D}S_3 - \frac{g_{33}}{s_{33}^D}D_3 \tag{2.21}$$

$$\frac{\partial T_3}{\partial x} = \rho\frac{\partial^2\xi}{\partial t^2} \tag{G.4}$$

$$\frac{\partial\left(\frac{1}{s_{33}^D}\frac{\partial\xi}{\partial x}\right)}{\partial x} - \frac{g_{33}}{s_{33}^D}\frac{\partial D_3}{\partial x} = \rho\frac{\partial^2\xi}{\partial t^2} \tag{G.5}$$

For the term $\frac{\partial D_3}{\partial x}$, since there is no free charge, Maxwell's equations require that $\nabla \cdot D = 0$ [123]. Then (G.5) becomes,

$$\frac{1}{s_{33}^D}\frac{\partial\left(\frac{\partial\xi}{\partial x}\right)}{\partial x} = \rho\frac{\partial^2\xi}{\partial t^2} \Rightarrow \frac{\partial^2\xi}{\partial t^2} - \frac{1}{\rho s_{33}^D}\frac{\partial^2\xi}{\partial x^2} = 0 \tag{G.6}$$

Appendix H

Derivation for (2.27)

The term to be transformed is $\frac{Sk(\dot{\xi}_1 \cos kl + \dot{\xi}_2)}{s_{33}^D j\omega \sin kl}$

Given equation for wave number

$$k = \frac{\omega}{c} \tag{H.1}$$

Knowing that

$$c = \sqrt{\frac{1}{\rho s_{33}^D}} \Rightarrow s_{33}^D = \frac{1}{\rho c^2} \tag{H.2}$$

and trigonometric conversion

$$\tan\frac{x}{2} = \frac{1 - \cos x}{\sin x} \tag{H.3}$$

Then

$$\frac{Sk(\dot{\xi}_1 \cos k\,l + \dot{\xi}_2)}{s_{33}^D j\omega \sin k\,l} = \frac{S\cancel{k}(\dot{\xi}_1 \cos k\,l + \dot{\xi}_2)}{\frac{1}{\rho c^{\cancel{2}}} j\cancel{k}\cancel{c} \sin k\,l}$$

$$= \frac{\rho c S(\dot{\xi}_1 \cos k\,l + \dot{\xi}_2)}{j \sin k\,l} \tag{H.4}$$

$$= \frac{\rho c S(\dot{\xi}_1 \cos k\,l + \dot{\xi}_2 + \dot{\xi}_1 - \dot{\xi}_1)}{j \sin k\,l}$$

$$= j\rho c S\dot{\xi}_1 \tan\frac{kl}{2} + \frac{\rho c S}{j \sin k\,l}(\dot{\xi}_1 + \dot{\xi}_2)$$

Appendix I

Parallel Plate Capacitor and Strain Rate

1. Parallel Plate Capacitor

If the length and width of the plates are much greater than their separation d, the electric field E near the center of the device will be uniform with the magnitude

$$E = \frac{\rho}{\varepsilon} \tag{I.1}$$

where $\rho = \frac{D}{A}$ is the charge density (A is the area) and ε is permittivity.

Voltage across the terminals can be expressed as

$$V = \int_0^d E\,dz = \int_0^d \frac{\rho d}{\varepsilon} = \frac{Qd}{\varepsilon A} \tag{I.2}$$

where Q is the charge. Since

$$C = \frac{Q}{V} \tag{I.3}$$

then

$$C = \frac{A}{d}\varepsilon = \frac{A}{d\beta} \tag{I.4}$$

Therefore, to be consistent with the notations in the original context,

$$C_0 = \frac{S}{l\beta_r} \tag{I.5}$$

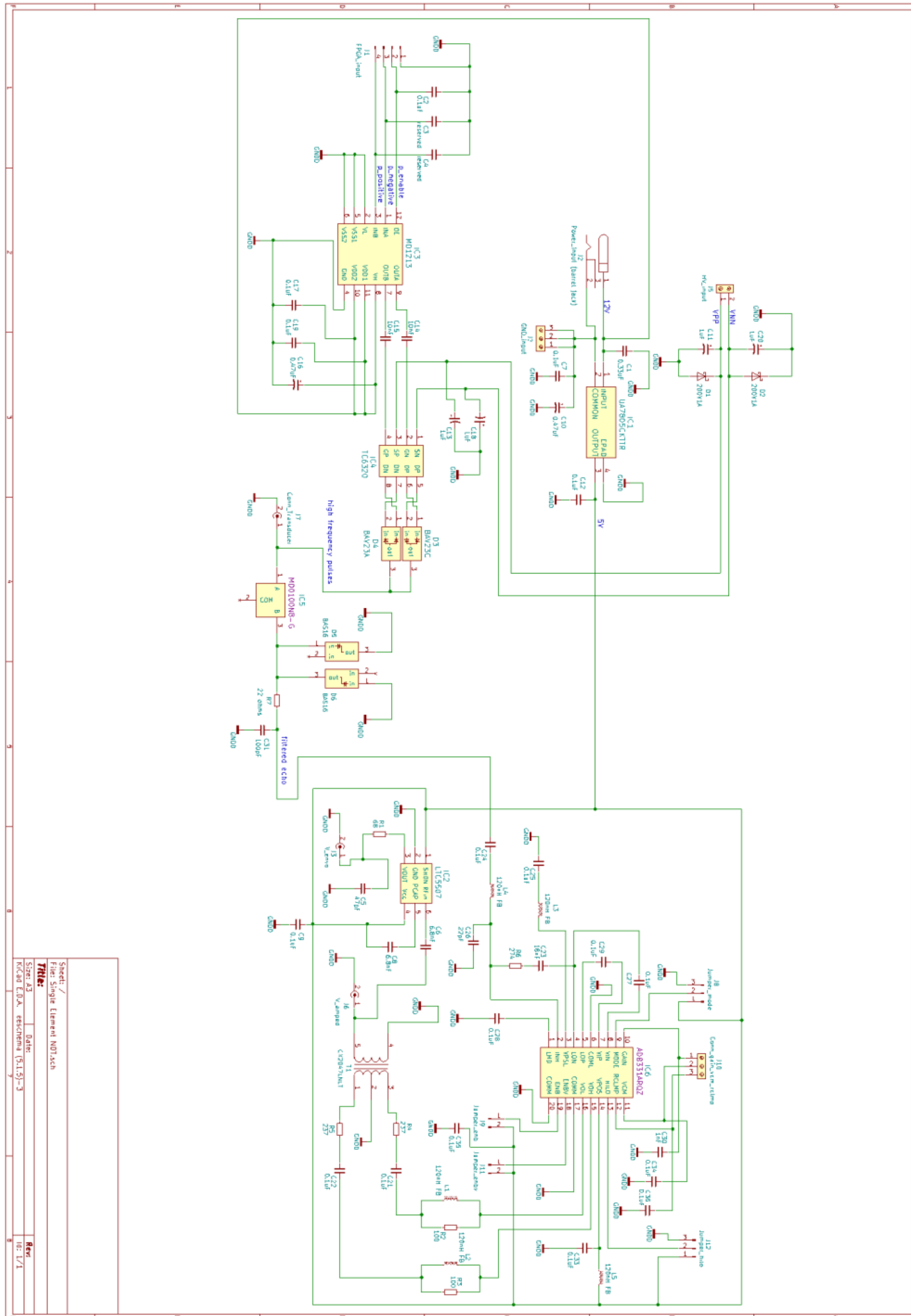
2. Strain Rate

The strain rate can be interpreted as the velocity at which both ends are moving away from each other, so given $\dot{S_3}$ as the strain rate in the longitudinal direction,

$$\dot{S_3} = \frac{d}{dt}\left(\frac{L(t) - L_0}{L_0}\right) = \frac{1}{L_0}\frac{dL(t)}{dt} = \frac{v(t)}{l_0} = \frac{\dot{\xi}\big|_{x=l} - \dot{\xi}\big|_{x=0}}{l_0} \tag{I.6}$$

Appendix J

Analog Front End (AFE) PCB Schematics



Appendix K

BOM list for AFE PCB

Parts	Footprint	quantity	Schematic	Website
Connectors				
Screw connectors	T2 5mm	1	J5	https://www.digikey.ca/product-detail/en/phoenix-contact/1729018/277-1236-ND/260604
Screw connectors	T3 5mm	2	J10	https://www.digikey.ca/product-detail/en/phoenix-contact/1729021/277-1237-ND/260605
BNC connectors	tht	3	J3,J6,J7	https://www.digikey.ca/product-detail/en/te-connectivity-amp-connectors/5-1634503-1/A97581-ND/1755969
pin header	3 pos/2.54 mm	2	J12	https://www.digikey.ca/product-detail/en/sullins-connector-solutions/PRPC003SAAN-RC/S1011EC-03-ND/2775251
Barrel jack	2.1mm-5.5mm	1	J2	https://www.digikey.ca/product-detail/en/mpd-memory-protection-devices/EJ503A/EJ503A-ND/5431753
pin header	2 pos/2.54mm	2	J1	https://www.digikey.ca/product-detail/en/sullins-connector-solutions/PRPC002SAAN-RC/S1011EC-02-ND/2775252
shunt jumper	2 pos/2.54mm	4	J9,J11	https://www.digikey.ca/product-detail/en/sullins-connector-solutions/QPC02SXGN-RC/S9337-ND/2618262
Capacitors				
0.1uF	0805 smt 50V	17	C2,C7,C9,C12,C17,C19,C21,C22,C24,C25,C27,C28,C29,C33,C34,C35,C36	https://www.digikey.ca/product-detail/en/samsung-electro-mechanics/CL21F104ZBCNNNC/1276-1007-1-ND/3889093
1uF	D6.3P2.5 tht 250V	4	C11,C13,C18,C20	https://www.digikey.ca/product-detail/en/nichicon/UVZ2E010MED/493-1411-ND/589152
10nF (10000pF)	0805 smt 200V	2	C14,C15	https://www.digikey.ca/product-detail/en/samsung-electro-mechanics/CL21B103KDCNNNC/1276-1170-1-ND/3889256
0.47uF	D5P2 tht 50V	2	C10,C16	https://www.digikey.ca/product-detail/en/elna-america/RFS-50VR47ME3-5/604-1131-ND/2171182
0.33uF	0805 smt 50V	1	C1	https://www.digikey.ca/product-detail/en/samsung-electro-mechanics/CL21B334KBFNNNE/1276-1123-1-ND/3889209
6.8nF (6800pF)	0805 smt 50V	2	C6,C8	https://www.digikey.ca/product-detail/en/murata-electronics/GRM2195C1H682JA01D/490-1638-1-ND/587496
47pF	0805 smt 50V	1	C5	https://www.digikey.ca/product-detail/en/yageo/CC0805JRNPO9BN470/311-1107-1-ND/303017
18nF	0805 smt 50V	1	C23	https://www.digikey.ca/product-detail/en/murata-electronics-north-america/GRM21B5C1H183JA01L/490-3321-1-ND/702862
22pF	0805 smt 50V	1	C26	https://www.digikey.ca/product-detail/en/samsung-electro-mechanics/CL21C220JB61PNC/1276-2605-1-ND/3890691
1nF	0805 smt 50V	1	C30	https://www.digikey.ca/product-detail/en/kemet/C0805C102K5RECAUTO/399-17883-1-ND/8640550
100pF	0805 smt 50V	1	C31	https://www.digikey.ca/product-detail/en/yageo/CC0805JRNPO9BN101/311-1111-1-ND/303021
10uF	D5P2.5 tht 50V	1	C32	https://www.digikey.ca/product-detail/en/panasonic-electronic-components/ECA-1HM100I/P10425CT-ND/8603345
reserved			C3,C4	
Inductors				
120nH FB	0603 smt 300mA	5	L1,L2,L3,L4,L5	https://www.digikey.ca/product-detail/en/taiyo-yuden/HK1608R12J-T/587-1558-1-ND/1008173
Resistors				
274 Ohms	1206 0.25W	1	R6	https://www.digikey.ca/product-detail/en/yageo/RC1206FR-07274RL/311-274FRCT-ND/731683
237 Ohms	0603 0.25W	2	R4,R5	https://www.digikey.ca/product-detail/en/vishay-dale/CRCW0603237RFKEAHP/541-237SCT-ND/5326829
100 Ohms	0603 0.25W	2	R2,R3	https://www.digikey.ca/product-detail/en/te-connectivity-passive-product/CRGP0603F100R/A130404CT-ND/8578236
68 Ohms	0603 0.25W	1	R1	https://www.digikey.ca/product-detail/en/vishay-dale/CRCW060368R0FKEAHP/541-68.0SCT-ND/5326867
22 Ohms	2512 smt 1W	1	R7	https://www.digikey.ca/product-detail/en/stackpole-electronics-inc/RMCF2512JT22R0/RMCF2512JT22R0CT-ND/6053408
Diode				
BAS16	SOT-23 3	2	D5,D6	https://www.digikey.ca/product-detail/en/on-semiconductor/BAS16/BAS16FSCT-ND/458926
BAV23A	SOT-23 3	1	D4	https://www.digikey.ca/product-detail/en/diodes-incorporated/BAV23A-7-F/BAV23A-FDICT-ND/750010
BAV23C	SOT-23 3	1	D3	https://www.digikey.ca/product-detail/en/diodes-incorporated/BAV23C-7-F/BAV23C-FDICT-ND/717832
SMD1200PL-TP	SOD-123F	2	D1,D2	https://www.digikey.ca/product-detail/en/micro-commercial-co/SMD1200PL-TP/SMD1200PL-TPMSCT-ND/2698529
ICs				
UA7805	TO-263-3_TabPin4	1	IC1	https://www.digikey.ca/product-detail/en/texas-instruments/UA7805CKTTR/296-20796-1-ND/1204660
LTC5507	SOT-23-6	1	IC2	https://www.digikey.ca/product-detail/en/linear-technology-analog-devices/LTC5507ES6-TRMPBF/LTC5507ES6-TRMPBFCT-ND/891042
MD1213	12QFN 4*4	1	IC3	https://www.digikey.ca/product-detail/en/microchip-technology/MD1213K6-G/MD1213K6-GCT-ND/5169523
TC6320	8SOIC 3.9	1	IC4	https://www.digikey.ca/product-detail/en/microchip-technology/TC6320TG-G/TC6320TG-GCT-ND/5169535
MD0100	to-243AA(SOT-89 3)	1	IC5	https://www.digikey.ca/product-detail/en/microchip-technology/MD0100N8-G/MD0100N8-GCT-ND/7065597
AD8331	QF20	1	IC6	https://www.digikey.ca/product-detail/en/analog-devices-inc/AD8331ARQZ/AD8331ARQZ-ND/751157
Transformer	CX2047LNLT	1	T1	https://www.digikey.ca/product-detail/en/pulse-electronics-network/CX2047LNLT/553-2291-1-ND/5014425
Transformer	CX2041NLT	1	T1	https://www.digikey.ca/product-detail/en/pulse-electronics-network/CX2041NLT/553-2290-1-ND/5014424