Development of Control Circuits for Silicon MOS Quantum Dot Qubit Network

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Future quantum processors intend to operate on millions of qubits and Silicon Metal Oxide Semiconductor (MOS) Quantum Dot qubits are a good fit for such a large-scale system due to their compactness in size and large coherence time. To control the operations of the qubits in such a large-scale system, efficient and careful design of the control circuits is very challenging. Here, in this thesis a control circuit is designed for silicon MOS quantum dot qubits operating on a node/ network architecture. Rather than using a 2D array of quantum dots, a node/ network architecture provides enough space for the wiring of integrated control circuits. The control circuit designed here is expected to work on millikelvin (mK) temperature and number of control lines from the mK temperature to 1-4 K temperature, where the digital control systems are operated, is reduced significantly compared to the number of qubits. The reduction in number of control lines from mK temperature is one of the basic requirements while scaling up. All these control circuits operate on the quantum dots based on the assumption that, all the dots are at same potential throughout the network. In practice due to fabrication variations and connection differences the potential of quantum dots varies from qubit to qubit. To solve this problem and pre-tune all the quantum dots to same potential prior to the operation of control circuit, a device level error correcting scheme is introduced and verified by simulation in this thesis.

Acknowledgements

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Last but not the least, I am thankful to my family and friends for their love and support.

Dedication

This thesis is dedicated to my parents Dr. Nurul Absar and Tahmina Absar.

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Chapter 1

Introduction

1.1 Introduction

Quantum processors have the potential to build such a sophisticated system that can provide tremendous speedup and memory enhancement to specific problems such as prime number factorization [1], complex molecules simulation [2], database search [3], financial modelling and forecasting [4] etc. Developments and new discoveries in fields such as machine learning and artificial intelligence are expected to accelerate tremendously with the help of quantum computers. Physicists, material scientists and engineers are working together in different aspects of this field to develop large-scale quantum processors with various kinds of approaches based on different materials and phenomena.

Quantum computers use quantum bits (qubits) which are two level quantum systems with unique properties including superposition and entanglement. Such properties enable exponential speedup in operation compared to classical computation in specific tasks. Different physical systems have been explored as qubits including superconducting circuits [5], ion trap systems [6], spin in quantum dots [7], topological nanowires [8], nuclear magnetic resonance (NMR) [9], defects in solids [10], photonic systems [11] and many more. Each type of systems has its own pros and cons. In this work, a control circuit is developed for a large-scale silicon MOS quantum dot qubit network.

One of the major concerns in implementing a large-scale quantum processor is the error prone nature of quantum systems. The information stored in a quantum system can be altered by system's interaction with environment known as decoherence. In this process, the quantum system loses its quantum nature. Thermal radiation, cross talk between

qubits, changing electric or magnetic field can cause decoherence. Hence, developing an error correcting scheme is one of the primary requirements of a fault-tolerant quantum processor. The most popular approach in correcting errors in the quantum processor is to encode quantum information into a larger space. Such process requires the number of physical qubits to be several orders of magnitude higher than the number of logical qubits. As a result, in a large-scale quantum system, the exponential speedup over the classical computer requires operation of millions of physical qubits. Connecting and controlling such a large number of qubits is extremely challenging. Silicon-based quantum dot qubits have several advantages for scaling up to the large number of qubits needed for universal quantum computing. Firstly, due to small footprint (10-100 nm) of quantum dots, it can be closely packed in the processor [12]. Secondly, realization of the quantum dot qubits in isotopically enriched silicon (^{28}Si) improves the coherence time compared to other quantum dot technologies and in [13] the reported dephrasing time is $T_2^* = 120$ µs and $T_2 = 28$ ms. The long coherence time make the qubits less error prone. Last but not the least, the widespread use of silicon technology in classical computing assures the precision in fabrication and low manufacturing cost compared to others.

Quantum processors require high fidelity qubits working with a control circuit interface which maintains a smooth communication between the qubits and the electronics required to control the qubits. The qubits operate at very low temperature around millikelvin (mK) range because any thermal disturbance destroys information stored in quantum systems. The electronics controlling those qubits in today's systems mainly sit at room temperature. Connecting these qubits with room temperature electronics requires step by step cooling which creates significant complexity in connection. Current implementations require at least one control line for each qubit. One of the recent milestones in the field of quantum computing is the quantum supremacy achieved with 53 qubits, which needs 200 wideband coaxial-cables, 45 bulky microwave circulators, and racks of room temperature electronics to operate [14], projecting up to millions of qubits it will be simply unmanageable to operate in this way. In addition, these control signals will also bring extra noise and heat to the circuit which will create errors in the computation. One way to reduce the complex circuits is to push the control circuits as close as to the qubits, for which the control circuits need to work at cryogenic temperatures close to the temperature of the qubits.

In this thesis, a control circuit is developed for silicon MOS quantum dot qubit network. The control circuit is designed to operate at millikelvin temperature close to the qubits. All the operations on the qubits using these control circuits are performed based on the assumption that all the quantum dots are at the same potential. In practice due to fabrication variations and connection differences the potential of quantum dots varies throughout the network. To solve this problem and pre-tune all the quantum dots to

the same potential prior to the operation of control circuit, a device level error correcting concept is introduced and verified by simulation in this thesis.

1.2 Background of Silicon Quantum Dots

Quantum dots (QDs) are nanoscale semiconductor crystals which have the capability to transport electrons. The quantum dot qubits are being developed based on the charge or spin properties of single electrons.

The basic mechanism in Silicon MOS Quantum Dot is to use a MOS gate to electrostatically confine electrons in a quantum dot [15]. A single electron can be trapped in a quantum dot by repelling electric fields imposed from all sides. For a certain quantum dot system, a charge stability diagram is usually constructed which gives the information about the number of electron occupancy in the dot with changing gate voltage.

Figure 1.1 shows a simple silicon MOS quantum dot device structure. The device consists of a layer of SiO_2 on top of a layer of Si-substrate, is controlled by two gates namely plunger gate (PG) and screening gate (SG). By applying voltage on PG, quantum dot is formed in the Si region underneath PG. SG prevents the accumulation of electron below the portion of the PG which overlaps SG. In a quantum processor while working with a lot of quantum dots, there will be other gates such as tunneling gates. Tunneling gates are usually placed between neighbouring quantum dots to tunnel electron from one quantum dot to others. Detail device structure for the network/node approach will be discussed in Chapter 3.

The quantum processor consists of a 2D array of quantum dots coupled together. Each quantum dot is occupied by a single electron. When a large static magnetic field is applied, the Zeeman effect lifts the spin degeneracy and form a two-level qubit system. For biasing these qubits constant voltage level between 0.5-3 V is supplied to the gate of the quantum dots.

The qubits can be initialized to either spin up $|\uparrow\rangle$ or spin down $|\downarrow\rangle$ state in a quantum dot. At first, the quantum dot is coupled to an electron reservoir. Then, the dot is tuned by changing the gate voltages in such a way that, the chemical potential of the reservoir lies between spin up $|\uparrow\rangle$ and spin down $|\downarrow\rangle$ states. Both spin states are separated in energy by the Zeeman splitting. When an electron is loaded to the dot from the reservoir depending on the thermal energy of the reservoir in comparison to Zeeman splitting, spin up $|\uparrow\rangle$ or spin down $|\downarrow\rangle$ states are initialized. In a quantum processor, where operations are performed by a large array of quantum dots it is not feasible to couple each quantum

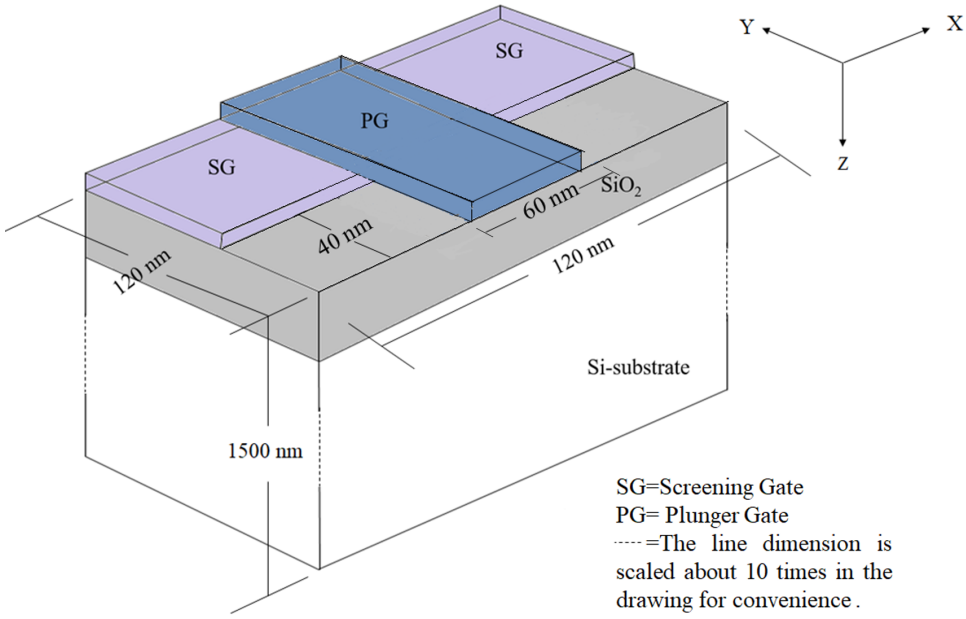


Figure 1.1: Silicon MOS quantum dot device.

dot to a separate reservoir for initialization due to area and noise constrains. As a result, only few quantum dots are coupled to the reservoir for initialization and using sequential tunneling mechanism between the dots those initialized electrons can be moved to other dots in the network.

The fundamental operations of the processor require single qubit and two qubit rotations. Single qubit rotations can be performed in several ways [16] [17]. One of the ways is to use electron spin resonance (ESR). ESR is performed by applying an on-resonance microwave field perpendicular to the static magnetic field. Another alternative way is to use Electron spin dipole resonance (EDSR). EDSR requires electric microwave pulses applied to the metal gates defining the quantum dots.

Two qubit operation can be implemented by exchange interaction using tunnel coupling and detuning energy between neighbouring dots. As tunnel coupling and detuning can be realized by switching electrical gate voltages thus two qubit operations can be realized by controlling the gate voltages. The gate voltages required for these operations are in the millivolt range.

1.3 Thesis Overview

This thesis is organized into four main chapters followed by a conclusion. Chapter 1 introduces the background of quantum processors with basic working principle of Silicon Quantum Dot processors. Chapter 2 provides an overview of the recent related works in developing control circuits for quantum processors. Chapter 3 provides details about the network for which the control circuit is developed. The chapter discusses about the working principle of the network and based on operation requirements the development of the control circuit architecture. In Chapter 4 transistor level design and sizing of the control circuit to meet the required specification of the system is discussed and its performance is analyzed. Chapter 5 proposed a method to pre-tune the qubits so that the reported circuits can work as expected. Finally, Chapter 6 concludes the main results of this work and discuss about future directions.

Chapter 2

Literature Review

In the past two decades the performance of quantum processors was mainly limited by the low fidelity of the qubits. With technological developments there had been a sufficient improvement in the fidelity to allow the application of error correcting protocols [18]. This is the first step towards the ultimate goal of fault-tolerant quantum computers at a large scale. Meanwhile, the technology also starts to be limited by the electronics in addition to the qubits. Developing high fidelity qubits as well as high performance and well-designed approach for the electronics interface both are equally critical for large scale quantum computing.

Due to the nature of the quantum systems fan in and fan out of the qubits is not permitted. Hence, each individual qubit requires separate access of control electronics [19]. As each qubit needs to be addressed individually in quantum processor, it requires a single connection to the outside world where the electronics are placed. In this chapter some recent work in the field of developing electronics interface for quantum computers are discussed.

2.1 Develpement of Cryo-electronics Systems

There have been rapid development in the field of cryo-electronics for quantum processors. Hornibrook *et al.* [20] addressed several problems in scaling up quantum processors. The authors designed a prime line/address line architecture for solid state quantum dot qubits by taking the advantage of the universal behaviour of quantum gates which means any operation can be realized by applying a bunch of repeated single and two qubit unitaries.

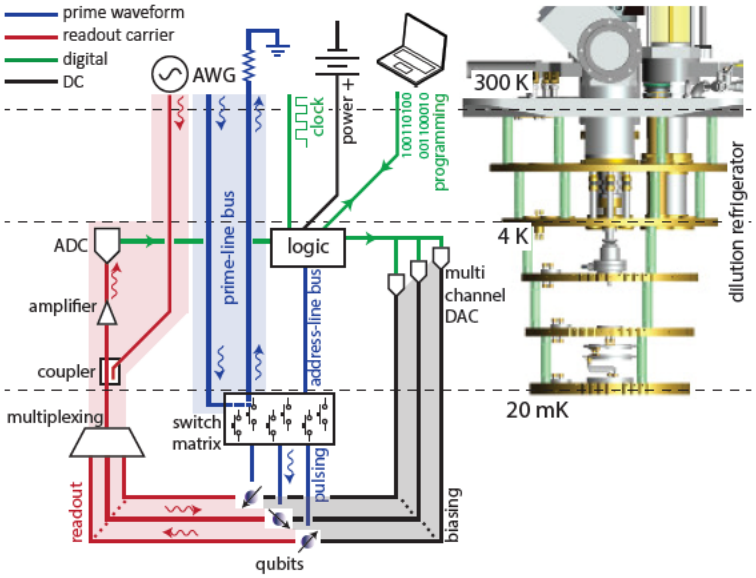


Figure 2.1: The control micro-architecture designed in [20] for large scale quantum processors. The switching circuit is placed at mK temperature with the qubits, which is controlled by digital logic at 4 K. Other electronics and CPU are placed at room temperature.

Hence, depending on the quantum algorithm used each cycle input signals will be applied to some particular qubits. Their approach separates the address line information from the input signals called "prime waveforms". The authors use the address line information to control a switch matrix which conveys the "prime waveforms" to the qubits based on the digital address provided on the address line. The switching circuit is placed as close to the qubits as possible to avoid any delays. The switch used in this work is a High Electron Mobility Transistor (HEMT) switch. Figure 2.1 shows the arrangement of the circuits for this approach. The switching matrix is placed at mK temperature near the qubits which gets the addressing information from a digital logic system which is placed at 4 k temperature. Some readout circuits are also placed at that temperature and all the electronics signal generators are at room temperature. This approach reduces the I/O interface by using a switching matrix and using digital logic system at cryogenic temperature rather than room temperature.

Continuing the idea of placing some switching circuit with the qubits and digital logic at around 1-4 K temperature Patra *et al.* proposed a generalized cryogenic control system template that might be a scalable solution for the future quantum computers [21]. The

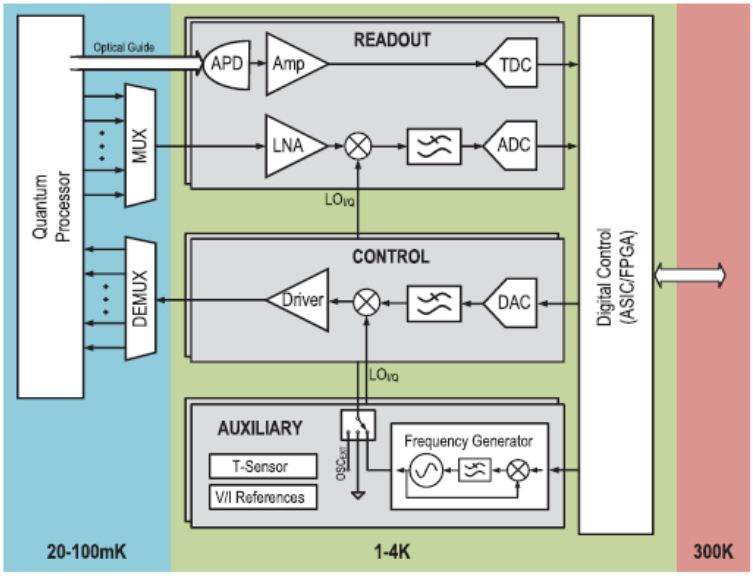
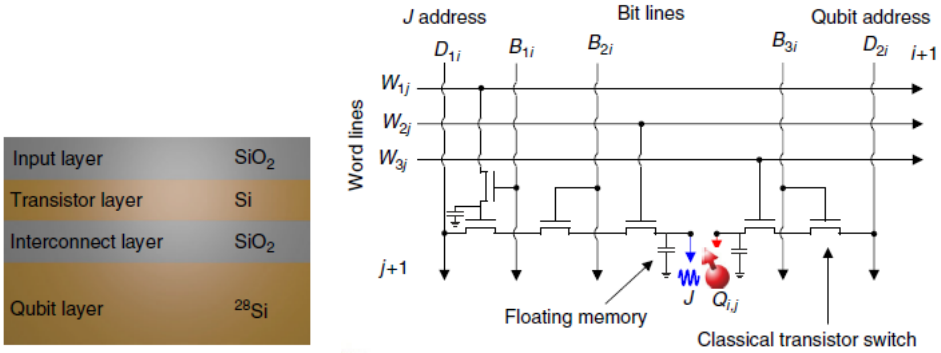


Figure 2.2: The generalized control and readout system architecture at cryogenic temperature proposed in [21]. Here, some multiplexing/demultiplexing circuits are placed with the qubits at mK temperature to reduce the number of I/O pins. The main electronics controllers with the digital logic systems like FPGA are placed at 1-4 K.

cryogenic control circuit proposed is designed in a standard CMOS technology as only CMOS technology can work at such low temperatures around 30 mK [22] [23]. Figure 2.2 shows the proposed cryogenic control and readout circuit. Here, the main components of the controller is designed to operate at 4 K temperature and some multiplexing and demultiplexing circuits are placed at mK. Ideally all the controllers should be on mK temperature with the qubits but not enough cooling power is available at that low temperature to extract heat from the full controller system. That's why only some multiplexing/demultiplexing is done to reduce the number of interconnects from mK to 4 k temperature.

After the proposal by Patra *et al.* different researches using different qubit technology used the same approach for their cryogenic control circuits. Focus has been given towards reducing the number of I/O lines from the mK to 4 K temperature. Veldhorst *et al.* proposed an architecture where the number of I/O lines increases as square root of the number of qubits for a spin based quantum computer [24]. They used a silicon-on-insulator (SOI) wafer where the bottom layer contains the qubits and the top layer contains the transistors to control the qubits. Different layers of the design in shown in Figure 2.3a.



(a) (b)

Figure 2.3: (a)The different layers of the silicon-on-insulator (SOI) wafer reported in [24]. The bottom layer is isotopically enriched silicon-28 layer to form the qubits and top layer is the transistors to control the qubits. Both the layers are connected through interconnects in the SiO_2 layer, (b) Control circuit for a single qubit with Q gate to tune the qubit to its resonance frequency for operation and J gate for exchange interaction between qubits. Depending on the Bit lines and Word lines, data line will get connected to particular Q/J gate or a set of Q/J gates.

Each qubit is connected to a data line and another data line is connected to a gate between two adjacent qubits for exchange interaction. The data lines are controlled by bit line (B) and word line (W) to provide individual or row by row or global addressability to the qubits. Figure 2.3b shows the electrical circuitry connected to each quantum dot qubits. There are total six transistors connected to each qubit for selecting the appropriate qubits for particular operation.

Some other works [25] [26] employed crossbar like architecture to address individual qubits and supply appropriate control signals according to their operating principal. These approaches were able to achieve reduced number of control lines from mK temperature to 4 K compared to the number of qubits. In [25] for a 2D square array of N qubits the total number of control lines were reduced to $4\sqrt{(2N)}+1$.

Some off-the-shelf CMOS circuits like multiplexers, which is one of the important components used in the control circuit of any type of quantum processor to reduce the I/O connections, have been tested successfully at mK temperature [27]. The reported work got a switching success rate of 100% at temperatures $\leq$ 80 mK.

The ultimate goal is to make a single chip with the qubits and integrated control circuits

operating at the same temperature. Researcher are working in the field of qubit technology to create "hot qubits" that can operate at temperatures up to 1.5 k [28]. Now, the goal is to design integrated cryo-electronics to operate at around 1.5 k temperature.

In this work, an integrated control circuit for silicon MOS quantum dot qubit network is designed. The main focus was to reduced the number of I/O lines as much as possible to reduce circuit complexity.

2.2 Conclusion

With decades of research the developments in quantum computing have improved the coherence time of the qubits and fidelity of the logic gates to a point where we can envision that in near future a scalable system with millions of qubits is possible to implement. In this situation, we need to start thinking about the new challenges that will emerge with a large-scale system and on top of that list comes the quantum to classical electronics interface. The way processors are tested today with a lot of wiring and step by step cooling process from cryogenic temperature to room temperature might not work with millions of qubits. In this thesis, the focus is to develop a scalable control circuit for the silicon MOS quantum dot qubit network which will be able to provide the network with the necessary control signals required for its operation.

Chapter 3

System Analysis and Choice of Architecture

3.1 Introduction

A large-scale quantum processor is introduced for semiconductor quantum dot spin qubits by Buonacorsi *et al.* [29]. The processor is built on a node/network approach. One node consists of seven quantum dots including one data qubit, two ancilla qubits, dots for electron shuttling operation and readout operations. Figure 3.1 shows the gate level layout of a single node.

One of the major challenges in building quantum processors is to develop an error correcting protocol. Unlike classical computing, quantum information is very sensitive to noise or decoherence. Initially no cloning theorem [30] and collapse of wavefunction due to measurement [31] in qubits made classical error correcting schemes inappropriate for quantum information. A breakthrough happened when Shor demonstrated an error correcting scheme in quantum systems [32] for the first time. Subsequently a lot of different quantum error correcting schemes and protocols have been developed which reduces the quantum error rate. The choice of error correcting protocol influences the architecture and gate operations of the system.

Currently Surface codes [33], which are an instance of topological quantum error correcting codes are one of the leading candidates for large scale quantum error correction. Surface codes operate on two-dimensional qubit arrays and it can achieve error threshold rate close to 1% [34]. While scaling up this kind of error tolerance behaviour is very important. The node architecture proposed in [29] is based on surface code operation. Rather

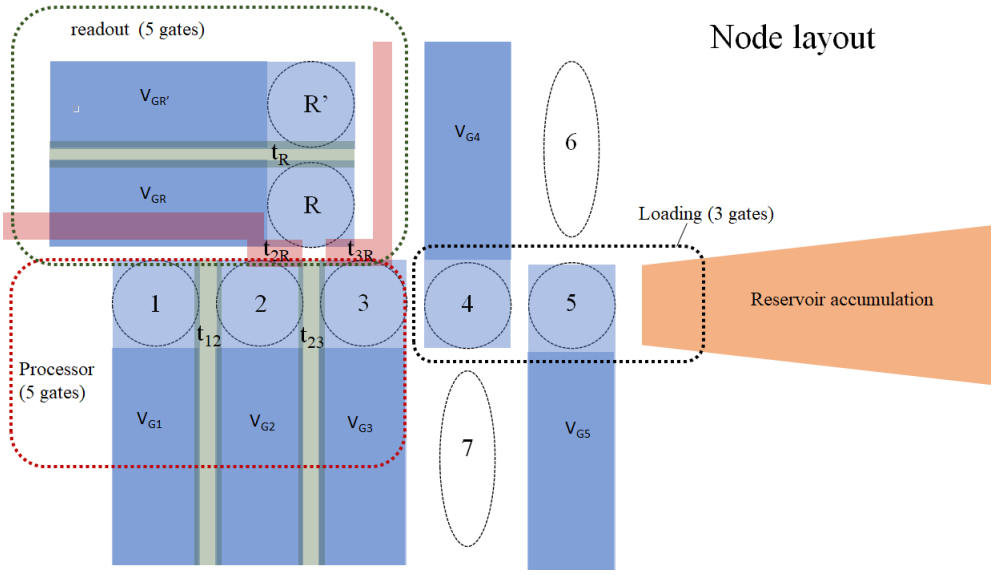


Figure 3.1: Node layout in Silicon MOS quantum dot processor. The processor consists of five gates. Gates labelled as V_{G1}, V_{G2}, V_{G3} are single "via" gate electrodes (blue color), used to form quantum dots and gates labelled as t_{12} and t_{23} are inter-dot tunneling gates (green color) between dot 1, dot 2 and dot 2, dot 3 respectively. For loading electrons from the reservoir gates (blue color) are needed to create "shuttle" dots. These gates are labelled as V_{G4} and V_{G5}. R and R' specify the double quantum dot for readout operation and t_R is the inter-dot tunneling gate between the double quantum dot. t_{2R} and t_{3R} are the gate electrodes (red color) to control exchange between the readout qubit, R, and ancilla qubits 2 and 3.

than using 2D quantum dot arrays like many existing design [35] [36] [37] [38] the system is made of 2M×2N node arrays as shown in Figure 3.2. This kind of approach provides space between qubits to improve qubit isolation and make integration more practical.

3.2 Operation Inside the Network

The first step in the network approach is to distribute entanglement between different nodes. In this purpose a four qubit GHZ state is created within four neighbouring nodes by first loading singlets and sharing them between nodes followed by some local gate operations and ancilla measurements. Afterwards, X or Z stabilizer operation is realized by local gate operations between data qubit and ancilla qubit followed by measuring ancilla

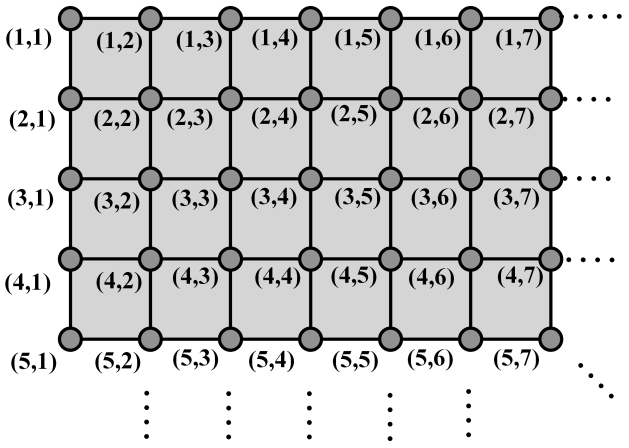


Figure 3.2: Node arrays in a Silicon MOS quantum dot qubit network. Inside each node there are K number of gates(V_{G1}, V_{G2},. . . ,V_{Gk}).

qubit. Figure 3.3 shows the sequence of stabilizer operation in four neighbouring nodes. Most of the gate operations and rotations are performed by sending input pulses with operation specific pulse width and amplitude. Some single-qubit rotations are performed by Electron Spin Resonance (ESR) using a global microwave field.

A stabilizer cycle consists of four steps as shown in Figure 3.4. Here, for both Z stabilizer and X stabilizer each cycle is split into two cycles as plaquettes in four adjacent nodes cannot be stabilized at the same time. The nodes Which will be activated at a certain time depends on both the stabilizer cycle and local gate operation. For example, to create GHZ state Y (π) rotation is performed in node 1 and node 3 as shown in the 3^{rd} step of Figure 3.3. So, for that operation only gates at node 1 and node 3 need to be connected to the input signal and if Z1 stabilizer cycle is considered then Figure 3.5 shows the activated nodes in this situation. After the stabilizer operation, the results are given to a classical data processing node which observes and determines if any node requires a corrective pulse for correcting an error that occurred in the code.

For local operations, individual addressability of each node is required to create holes (disconnect input signal from the node) in the surface code for operations and send correcting pulses depending on the output from the classical data processor. All these operations are performed considering all quantum dots are at the same potential. If due to difference in connection or fabrication variations all quantum dots are not at the same potential (which is the case in practice), a way is suggested in Chapter 5 to pre-tune all the dots to the same potential. In the next two sections (Section 3.3, Section 3.4) the circuitry to provide required control signals for global and local operations is discussed.

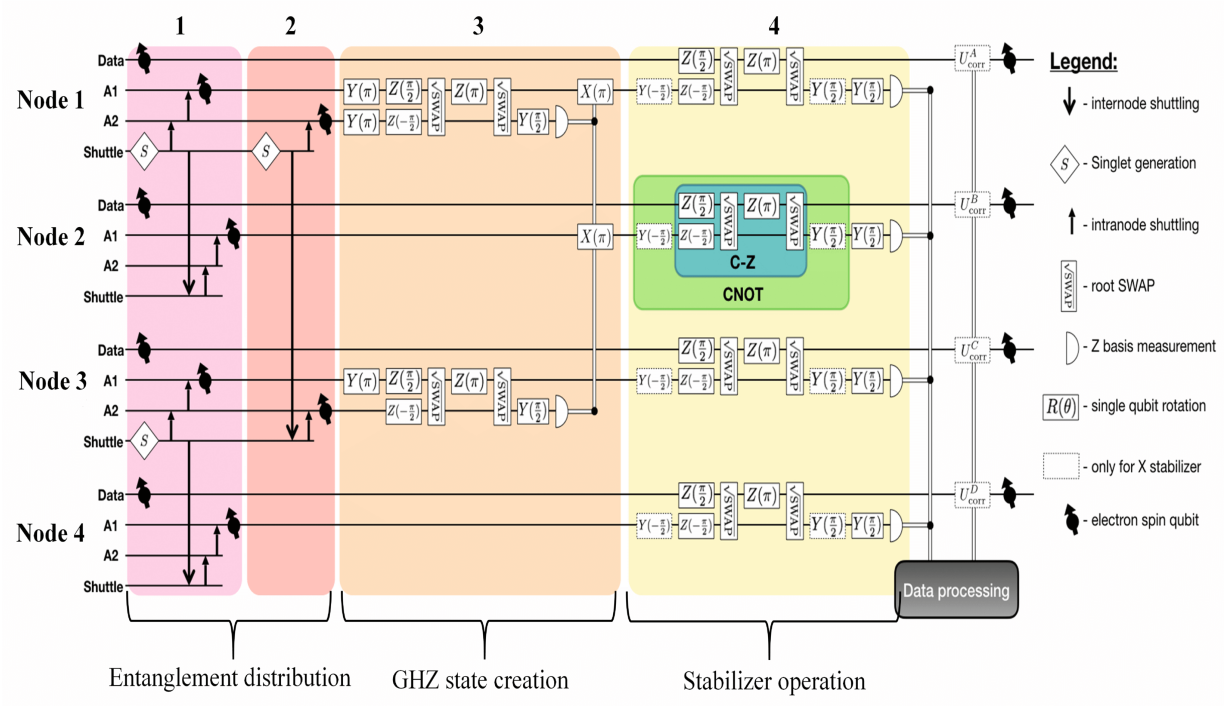


Figure 3.3: Operations in four neighbouring nodes. Here, A1 and A2 indicate ancilla qubit 1 and 2 respectively. In step 1 and 2 entanglement is distributed between different nodes by loading and sharing singlets between them. At the end of step 3 by some local gate operations and ancilla measurements four qubit GHZ state is formed. Step 4 represents stabilizer operation by performing conditional quantum gate (control-NOT or control-Z) operations followed by ancilla measurements [29].

3.3 Global Control Signals for the Network

The global control operations include turning on and turning off input pulses on different sets of nodes depending on stabilizer cycle and gate operations. To control that, a circuitry is needed which will turn on and turn off signals on different nodes based on operational requirements. The circuit complexity can be reduced by taking advantage of symmetries in the circuit. A unit cell is formed by taking four neighbouring nodes and for global operation similar nodes of the unit cells are connected or disconnected together. So, same corners of the unit cells can be tied together and connected to four different digital control signal lines, which will turn on or turn off the set of nodes with the help of a switching circuitry. Only four control lines are needed for this kind of global operations.

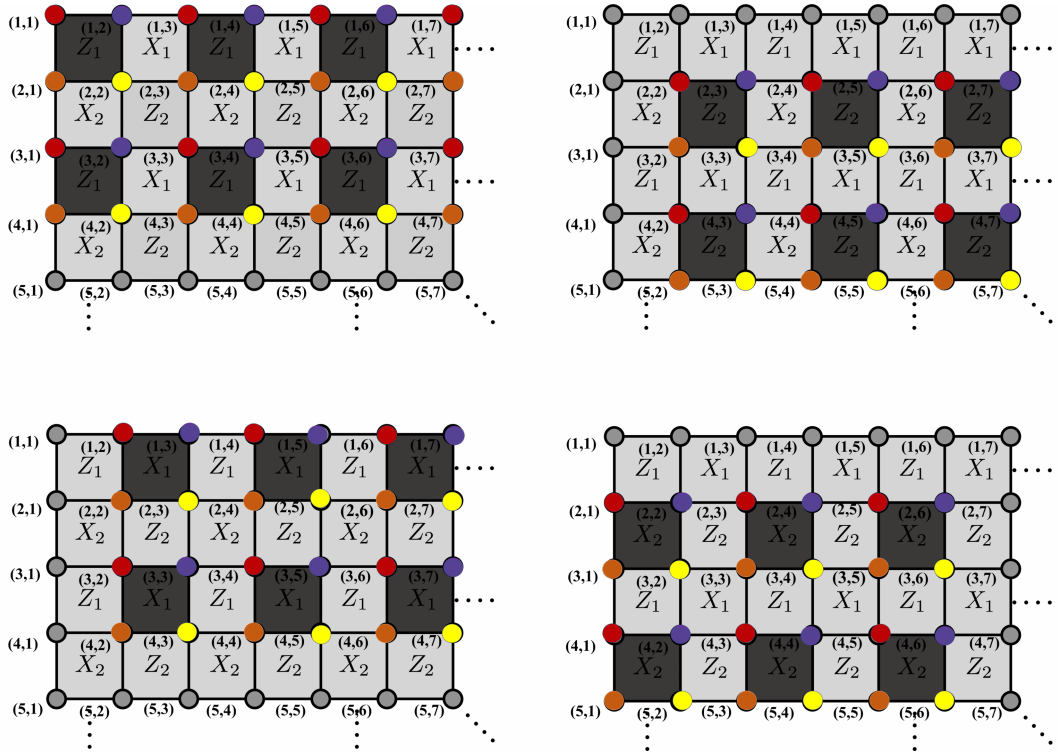


Figure 3.4: A full stabilizer cycle in four steps. For both Z stabilizer and X stabilizer each cycle is split into two cycles as plaquettes in four adjacent nodes cannot be stabilized at the same time. Four different colors show which operations occur at which node.

To minimize the amount of noise near the qubits, these circuits are planned to be placed in the mK temperature with the quantum dots. For controlling the global operations, shift registers can be used in the mK temperature which will provide control signal to the switching circuitry connected to the nodes. These shift registers will eventually be controlled by some digital logic system like FPGA at cryogenic temperature. For Y (π) rotation in Z1 stabilizer cycle the mechanism is showed in Figure 3.6.

3.4 Local Control Signals for the Network

Local operations like creating holes or sending correction pulses to a particular node, require individual addressability of each node rather than addressing a set of nodes together like the global operations. Control signal from a demultiplexer tree provides individual

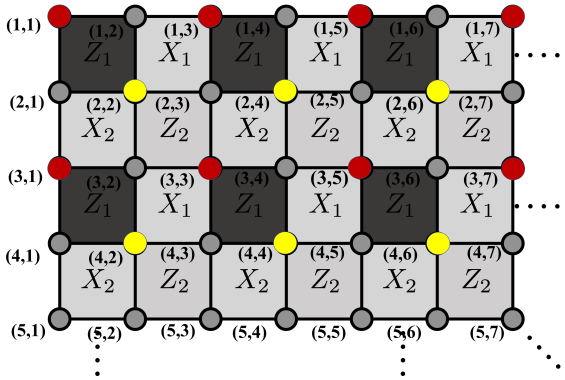


Figure 3.5: Node 1 and node 3 are activated during Y (π) rotation. Also depending of stabilizer cycle different set of unit cell will be activated. Here, stabilizer is at Z1 cycle.

addressability to nodes with the help of a switch connected to each node. Control signal from the demultiplexer will turn off or turn on the switch connected to the node. Multiple demultiplexer trees are needed to have multiple surface code holes at the same time, as one demultiplexer tree can address one node at a time. Again, to send correcting pulses to a certain node, first all the nodes are turned off using proper circuitry and then using demultiplexer tree a certain node will be turned on. Figure 3.7 shows the global and local control circuitry of $(i, j)^{th}$ node of the unit cell.

Here, total 3 switching circuits (SW_1, SW_2, SW_3) are included with each node. For normal operation all three switches will be closed and the signal will flow from V_{G_K} to the physical gate in the node through a clamper circuit. The clamper circuit provides the gates with the required dc voltage on top of input signal to create the quantum dots. In case of hole creation, SW_2 of Figure 3.7 is open thus the input signal doesn't reach the physical gate of the qubits. SW_2 gets the control signal from demultiplexer tree. The way these demultiplexers are designed (which will be covered in Chapter 4) by default all the outputs are logic 1 and when a particular node is addressed by selection pins, that particular output provides a logic 0 signal. Multiple demultiplexer trees are connected in parallel to create multiple holes at the same time. The output of these demultiplexers are connected to a nand gate before connecting to SW_2. So, in default cycle when both the demultiplexer provides logic 1 signals, the output of the nand gate will be low (according to nand gate truth table). Here, an active low switch is used so that by default the low output from the nand gate will keep SW_2 closed and signal will flow normally. In case of hole creation, if either of the demultiplexer tree is addressing a particular node, it will output a logic 0 signal on the output which is connected to that node. If one of the inputs of the nand gate is low, its output will be high which will eventually disconnect the switch

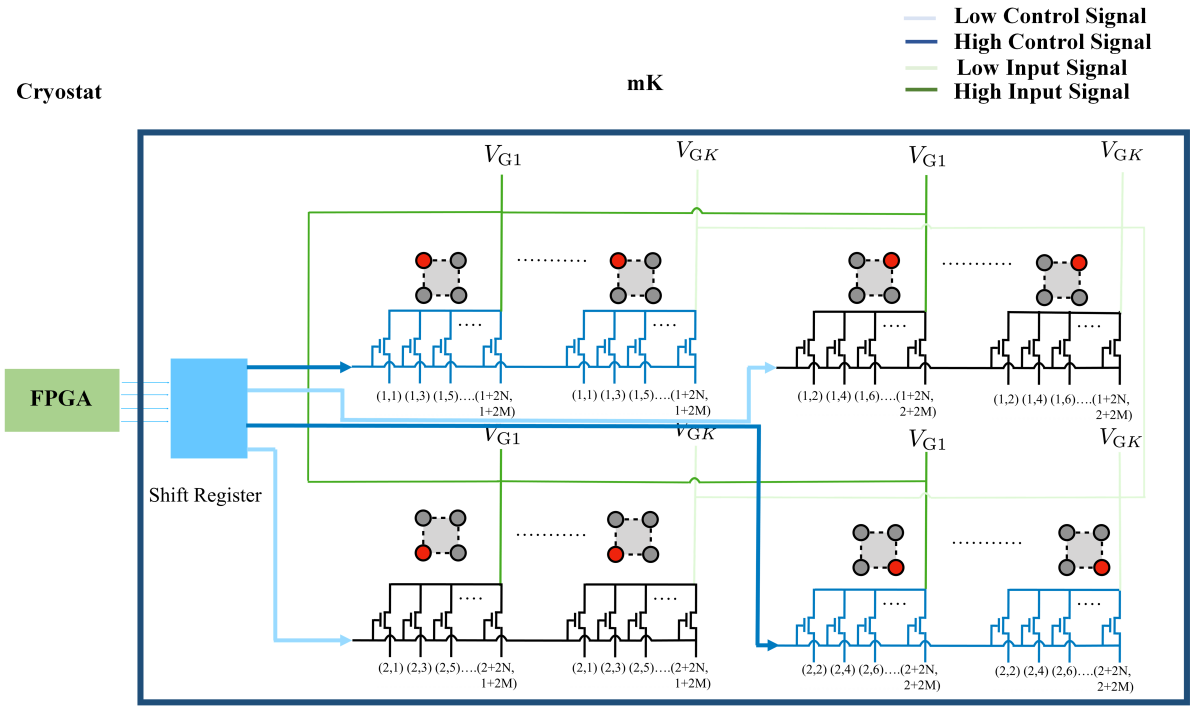


Figure 3.6: During Y (π) rotation in Z1 stabilizer cycle node 1 and node 3 need high control signal to close the switch (active high switch) so that inputs can get connected to the gates inside these nodes. At mK temperatures, shift registers provide these global control signals to the nodes and FPGA/ Digital logic controls these shift registers from cryogenic temperature.

and turn off the node input. Table 3.1 summarizes the logic behind hole creating circuitry. For simplicity only two demultiplexer tree is considered here.

When sending correction pulses to a particular node, at first all the nodes are turned off by disconnecting SW_3 of all nodes using a universal control signal. Then, the node where the correcting pulse is required, is turned on by using the demultiplexer tree. As discussed before by default demultiplexer tree supply logical high signal and a node is address by logical low signal. An inverter is added after the demultiplexer output to switch the default. Then output of the inverter is fed to one of the inputs of a two input nor gate and the other input is a universal control signal, which is shared between all the nor gates connected to individual nodes. So, in normal operation output of the demultiplexer tree is logic 1, which will be inverted to logic 0 by the inverter and then fed to a two input

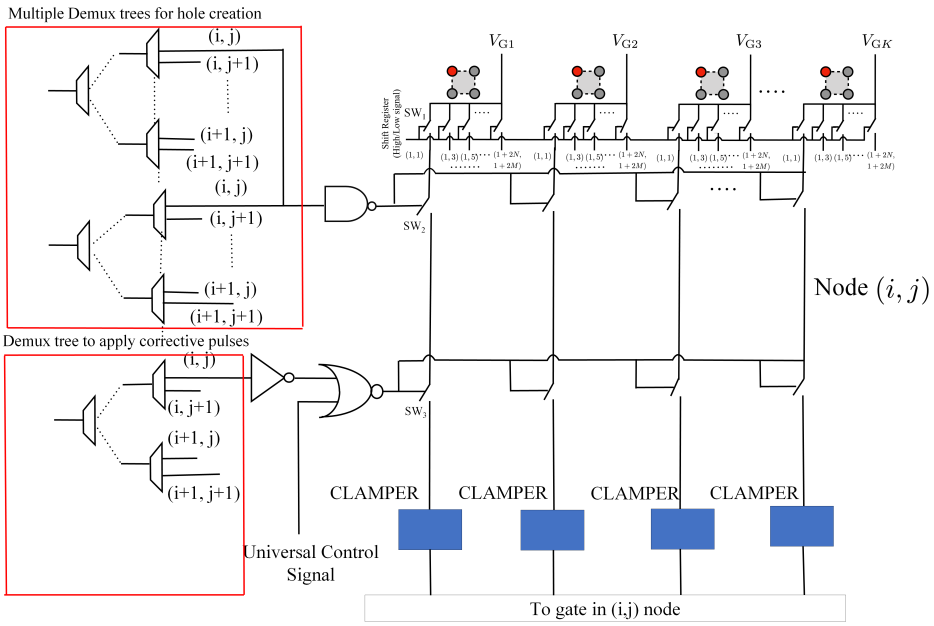
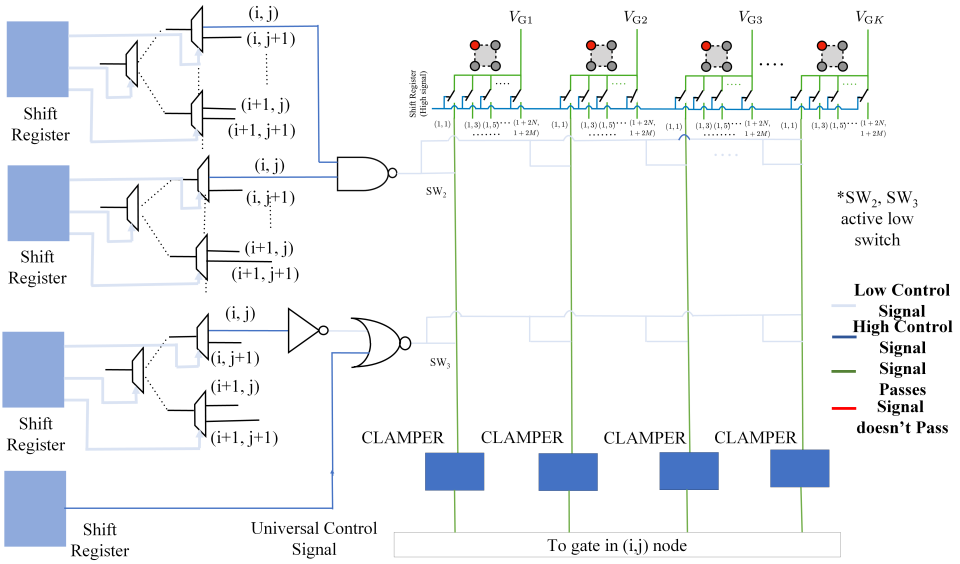


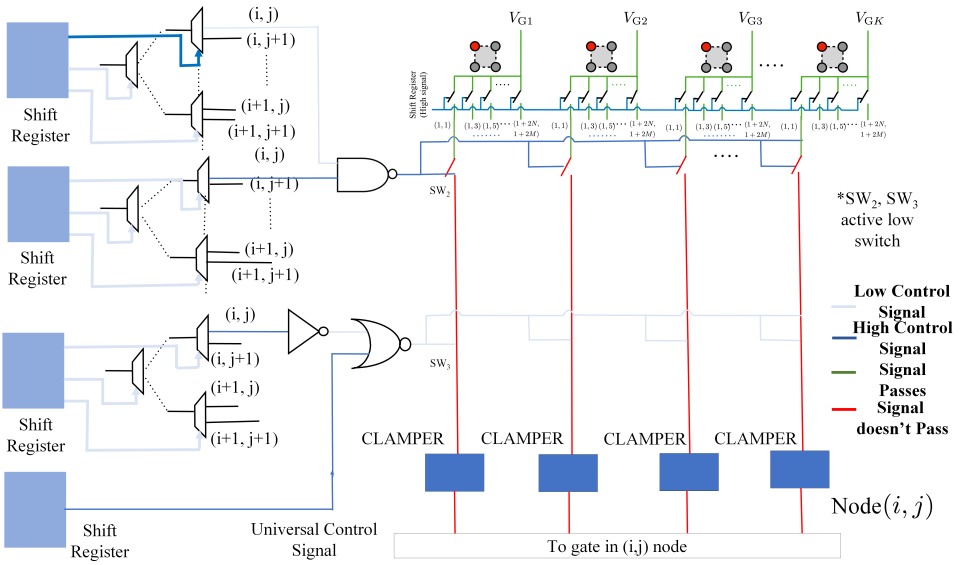
Figure 3.7: Global and local control circuitry for $(i, j)^{th}$ node of the unit cell. SW_1 controls the global operations and gets the control signal directly from the shift register. SW_2 and SW_3 control local operations of creating holes and sending correcting pulses respectively. SW_2 and SW_3 both are connected to demultiplexing trees, which will turn on or turn off depending on the control signal from the tree. Here, V_{G1}, V_{G2},...,V_{Gk} are different input voltages applied to each gate of a node. The clamper circuit provides necessary dc voltage required to define quantum dots.

nor gate. The other input of the nor gate is the universal control signal, which is by default logic 1. Hence, output of the nor gate will be logic 0 which will keep the active low switch closed and signal flow won't be interrupted. Before sending the correction pulse by making the universal control signal logic 0, SW_3 is disconnected. Then, the node which needs correction is addressed by the demultiplexer tree, which eventually closes SW_3 for that node and appropriate correction pulse is supplied to the node. The logic required to implement this operation is showed in Table 3.2

The control signals required by the demultiplexer tree and other gates are provided by shift registers. All these circuitries are designed to operate at mK temperature. The shift registers are programmed by a digital logic system at cryogenic temperature. Figure 3.8 and Figure 3.9 illustrates all different operations in the nodes controlled by the designed circuitry.

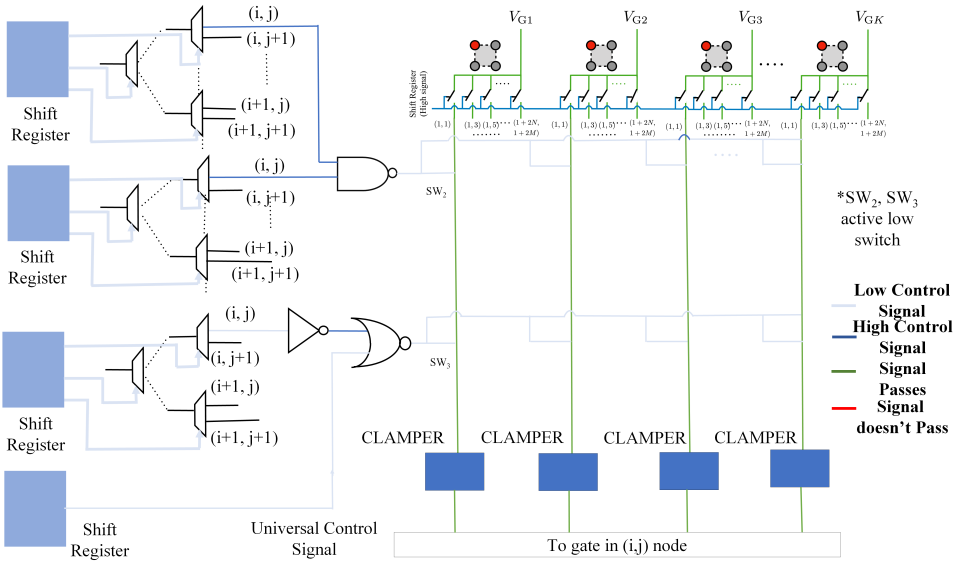


(a)

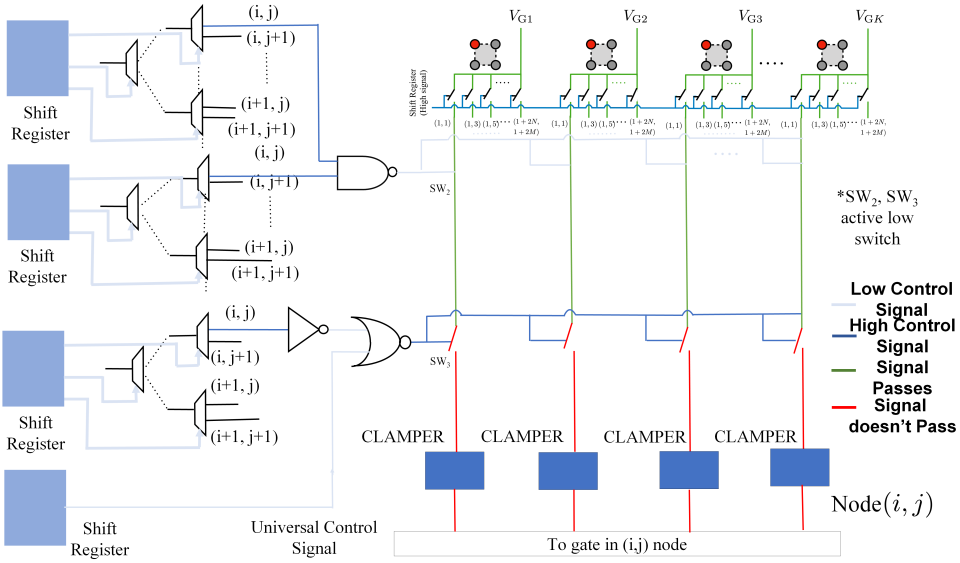


(b)

Figure 3.8: (a) Normal mode of operation where both demultiplexer trees are providing 1 V output which are the inputs to a nand gate. The output of the nand gate is 0 V Which activates SW_2 and thus signal flows to the node. (b)Hole creation at node (i,j). Demultiplexer tree is providing 0 V output to (i,j) node, which after passing through nand gate eventually supplies 1 V to SW_2 and disconnects it.



(a)



(b)

Figure 3.9: (a) Sending correction pulses to node (i,j). Demultiplexer tree is providing 0 V output to the node (i,j) , which after passing through inverter and nand gate eventually supplies 0 V to SW_3 and sends the corrective pulse to the node. (b) Signals to other nodes while sending correction pulse to node (i,j).Demultiplexer tree is providing 1 V output to the other nodes, which after passing through inverter and nand gate eventually supplies 1 V to SW_3 and disconnects it. Here, for both (a) and (b) universal control signal = 0 V.

Demultiplexer 1 output	Demultiplexer 2 output	Nand output	SW_2 state	Mode of Operation
1	1	0	Close	Normal operation
0	1	1	Open	Hole creation
1	0	1	Open	Hole creation
0	0	1	Open	Hole creation

Table 3.1: Different modes of operation for the circuitry used to create holes in each node.

Demultiplexer output	Universal Signal	Nor output	SW_3 state state	Mode of Operation
0	0	0	Close	Correction pulse supplied to specific node
0	1	0	Close	Normal operation
1	0	1	Open	All node voltage turned off
1	1	0	Close	Normal operation

Table 3.2: Different modes of operation of the circuitry controlling correcting pulses.

3.4.1 Control line calculation

Present implementation of the quantum processors requires at least 2 coax cables per qubit [39]. This current approach does not scale up due to increasing number of cables with qubits. Here, in this section a generalized equation is derived to calculate the number of control lines with increasing number of nodes for Silicon MOS quantum dot qubit network. It is shown that, the number of control lines from mK to cryogenic temperature is reduced significantly compared to the number of nodes. Let,
N = Number of nodes,
K= Binary demultiplexer level/ number of control line from demultiplexers,
S= Number of simultaneous holes created,
M = Bits of shift register (M$\geq$4),
C= Control lines from shift register to FPGA (at cryogenic temperature),
X= Number of shift registers.
Step 1 : Calculate K : For one hole creation,

$$K_1 = \frac{logN}{log2} \tag{3.1}$$

BEGIN

input number of nodes (N) in the processor
input number of simultaneous holes (S) created in surface code
input bits of shift register (M) used in the system
input number of control lines per shift register *(C)*
binary demultiplexer level, $K = \frac{logN}{log2}$ *(S+1)*
number of shift registers, $X = \frac{K}{M}$
number of control lines required by *X+1* shift registers = *C*(X+1)*

END

Figure 3.10: Steps to determine the number of control lines for the operation of silicon MOS quantum dot qubit network proposed in [29].

For simultaneous hole creation,

$$S \cdot K_1 = \frac{S \cdot logN}{log2} \tag{3.2}$$

For sending correction pulse,

$$K_2 = \frac{logN}{log2} \tag{3.3}$$

So, from Equation 3.2 and 3.3,

$$K = S \cdot K_1 + K_2 = \frac{logN}{log2}(S+1) \tag{3.4}$$

Here, binary demultiplexer level = number of control lines required by the demultiplexer.
Step 2 : Calculate X :

$$X = \frac{K}{M} \tag{3.5}$$

Step 3 : Calculate Local Control Lines :

$$C \cdot X \tag{3.6}$$

Step 4 : Calculate Total Local and Global Control Lines :

$$C \cdot X + C = C \cdot (X+1) \tag{3.7}$$

For example, using above mention calulations, when N= 10000; S=2; M=8; C=4 Total control lines from cryogenic temperature to mK $\approx$ 24.

Figure. 3.10 shows the sequence of operations to determine the number of control lines for silicon MOS quantum dot qubit network proposed in [29].

This kind of circuit arrangement reduces the number of control lines require from cryogenic to mK temperature, which is an important consideration while designing these circuits to reduce the circuit complexity and power consumption associated with cooling and extra noise injection into mK temperature.

Chapter 4

Circuit Design and Performance Analysis in TSMC 65nm

In this chapter the design and performance of circuits needed for the node network are analyzed in Cadence Virtuoso using TSMC 65nm technology. The main components of the designed network include, switch, binary demultiplexer tree and clamper circuit/ bias tee.

4.1 Circuit Design

4.1.1 Switch

In any node total 3 switching circuits are required: One for controlling the global control signals depending on stabilizer cycle and gate operation, one for controlling local hole creation and the last one for sending correcting pulses. For controlling the global operation an active high switch is used for operation simplicity, so that a logical high control signal will turn on a certain set of nodes. On the other hand, the way hole creation and sending of correction pulse to a particular node is designed, an active low switch will reduce circuit complexity.

Here, a pass gate switch is used for the switching operation. In the pass gate, one n-channel MOSFET (NMOS) and one p-channel MOSFET (PMOS) transistors are connected back-to-back in parallel with each other. An inverter is used between the gate of the NMOS

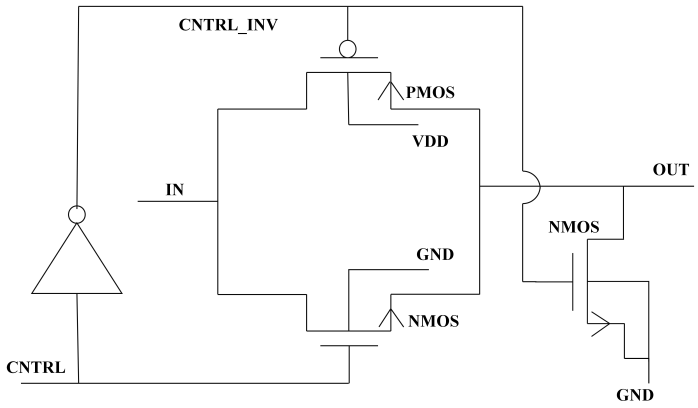


Figure 4.1: Pass gate switch (Active high). When, CNTRL = 1 V, NMOS and PMOS both are biased into conduction and the switch is closed. When, CNTRL = 0 V, NMOS and PMOS both are at cut-off region and the switch is open.

and PMOS to provide two complementary control voltages to the gate of the transistors. In case of active high switch, the control signal is directly connected to the gate of NMOS and the inversion of the control signal is connected to the gate of PMOS. When the control signal is high, both devices are biased into conduction and the switch is closed. On the other hand, when the control signal is low both NMOS and PMOS transistors are at cut-off and the switch is open. The output of the switch goes to a high impedance state when the switch is open. To convert it to logic 0 from the high impedance state output is passed through a NMOS transistor.

In case of active low switch, the control signal is directly connected to the gate of PMOS and the inversion of the control signal is connected to the gate of NMOS. So, When the control signal is low, the switch is closed as both devices are in conduction and when the control signal is high, switch is open as both transistors are at cut-off region. Figure 4.1 shows the active high pass gate switch circuitry and Table 4.1 shows the truth table for active high and active low pass gate switch. Transistor level circuit sizing and performance will be analyzed in Section 4.2 and Section 4.3 respectively.

Input to the network is GHz range pulse with amplitude between of 100-200 mVs and the control signal which is the output of demultiplexer tree after passing through some other gates is either 0 V or 1 V. The area of a single switch designed is around 14 um $\times$ 15 um.

CNTRL (V)	IN (V)	OUT (Active high) (V)	OUT (Active low) (V)
1	X	IN	0
0	X	0	IN

Table 4.1: Truth table for the switching circuit. (Both active low and active high)

4.1.2 Binary Demultiplexer Tree

For the binary demultiplexer tree, in order to use only universal gates and to keep the number of gates as low as possible with easier addressability first three levels have three slightly different design of binary demultiplexer circuits and afterwards these three levels can be considered as a unit cell for further scaling. In the first level of the demultiplexer tree, its necessary to have an enable pin to turn on the tree. Afterwards in the following levels an enable pin is not required. Figure 4.2 shows three different demultiplexer circuits designed. In Section 4.2 transistor level sizing of the demultiplexer tree will be discussed. The performance of the circuit will be observed in Section 4.3.

The 3 level unit cell of the demultiplexer tree is showed in Figure 4.3 and its truth table is mentioned in Table 4.2. So, here using binary demultiplexer circuits, a 1-to-8 demultiplexer is designed which provides 1V at all the output channels if not enabled. When the demultiplexer tree is enabled and a particular channel is selected by Sel1, Sel2 and Sel3 it outputs 0V at that channel.Delay between the output channel selected and output connected is around 130 ps. The area of the designed demultiplexer circuit is around 24 um $\times$ 66 um.

4.1.3 Clamper Circuit/ Bias tee

A circuitry is needed to supply dc voltage on top of the input pulses to the gates in each node to define quantum dots. Here, a clamper circuit is designed for that purpose. The clamper circuit changes the dc level of the input signal without changing the shape of the signal. A capacitor and a diode is used for this purpose as shown in Figure 4.4. The required dc bias is fed through a diode and input signal is fed through the capacitor. The capacitor is charged to its peak input value when the diode is in forward bias and the circuit passes the input to output when the diode is in reverse bias. Circuit performance will be discussed in the Section 4.3.The area of the designed circuit is around 50 um $\times$ 50 um.

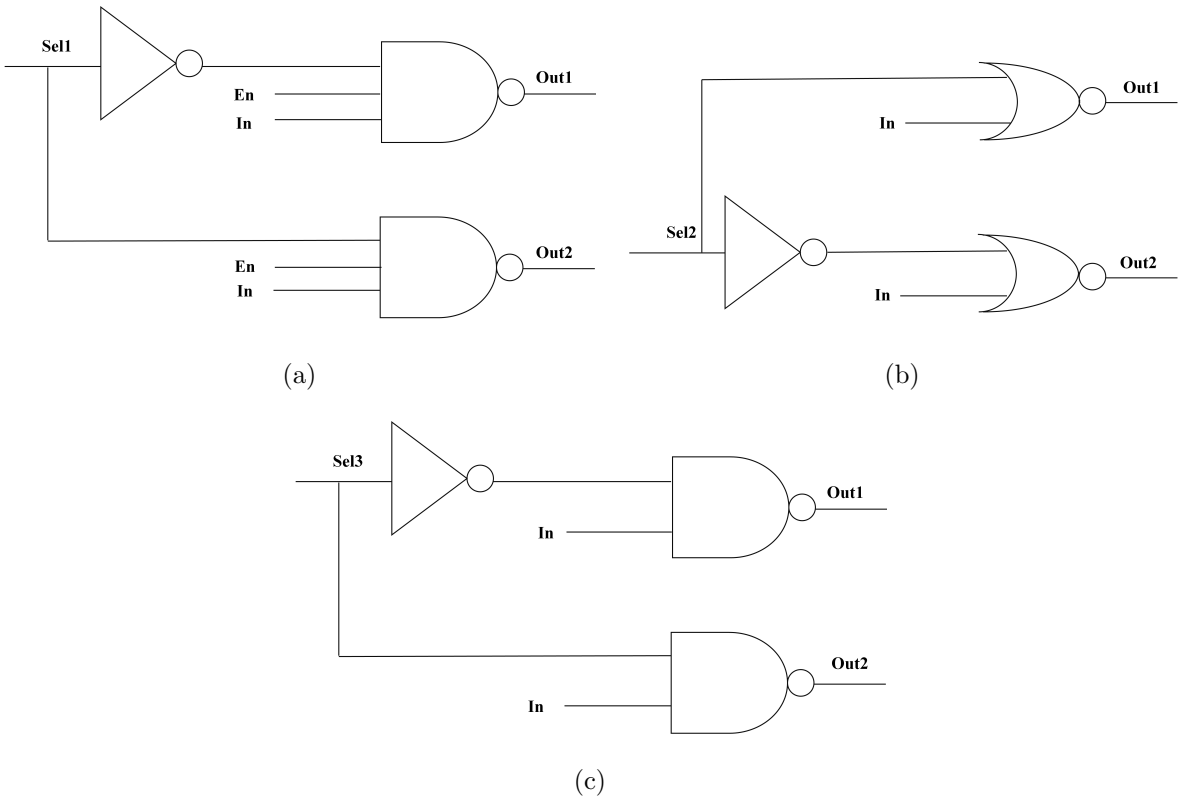


Figure 4.2: (a) Binary demultiplexer circuit with 3-input nand gates and inverter for 1^{st} level of the demultiplexer tree. If En is high then depending on Sel1, In will be connected to either Out1 or Out2. (b) Binary Demultiplexer circuit with 2-input nor gates and inverter for 2^{nd} level of the demultiplexer tree. Depending on Sel2, In will be connected to either Out1 or Out2 (c) Binary Demultiplexer circuit with 2-input nand gates and inverter for 3^{rd} level of the demultiplexer tree. Depending on Sel3, In will be connected to either Out1 or Out2.

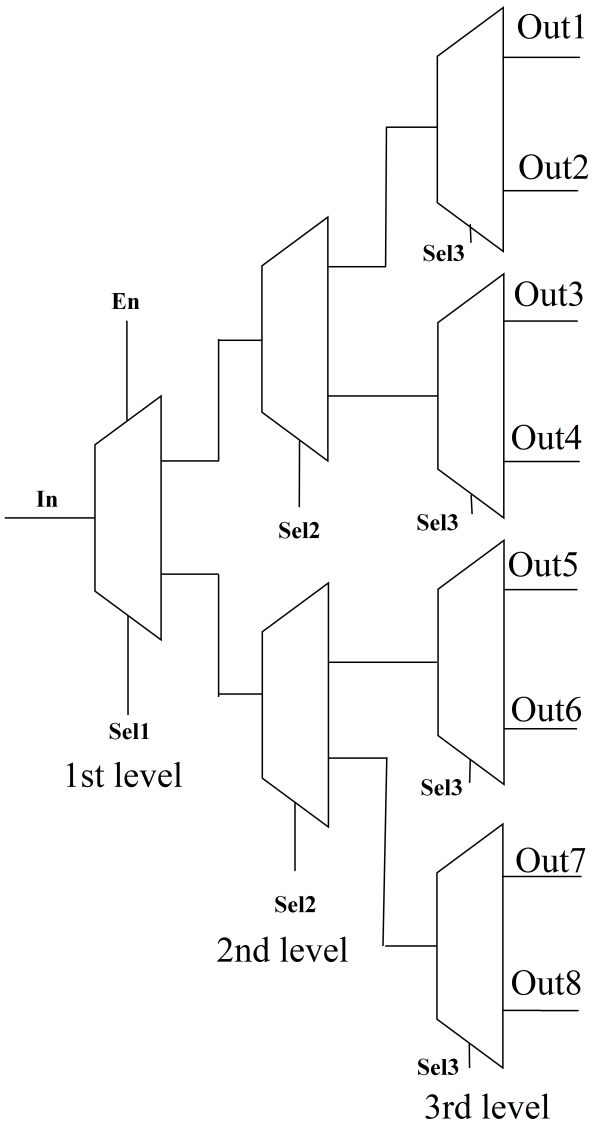


Figure 4.3: 3 level binary demultiplexer tree. If En=1, by providing proper control signal to Sel1, Sel2 and Sel3 one of the eight outputs is selected at a certain time. (Power pins are not shown for simplicity of the diagram.)

In (V)	EN (V)	Sel1 (V)	Sel2 (V)	Sel3 (V)	Out1 (V)	Out2 (V)	Out3 (V)	Out4 (V)	Out5 (V)	Out6 (V)	Out7 (V)	Out8 (V)
1	0	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
1	1	0	0	1	1	0	1	1	1	1	1	1
1	1	0	1	0	1	1	0	1	1	1	1	1
1	1	0	1	1	1	1	1	0	1	1	1	1
1	1	1	0	0	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	0

Table 4.2: Truth table of 3 level binary demultiplexer circuit.

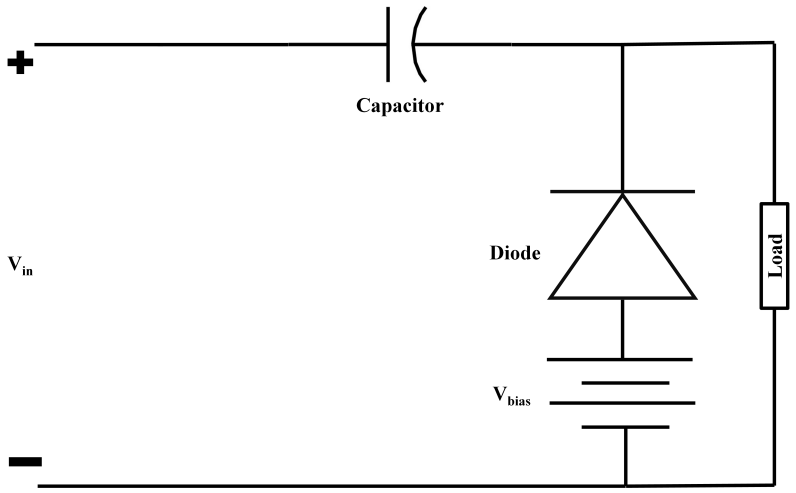


Figure 4.4: Clamper circuit with dc bias. The input is fed to one end of the capacitor and the other end is connected to a dc bias through a diode. When the diode is in forward bias the capacitor is charged to the peak value of input and when the diode is in reverse bias the clamper circuit passes the input signal to output.

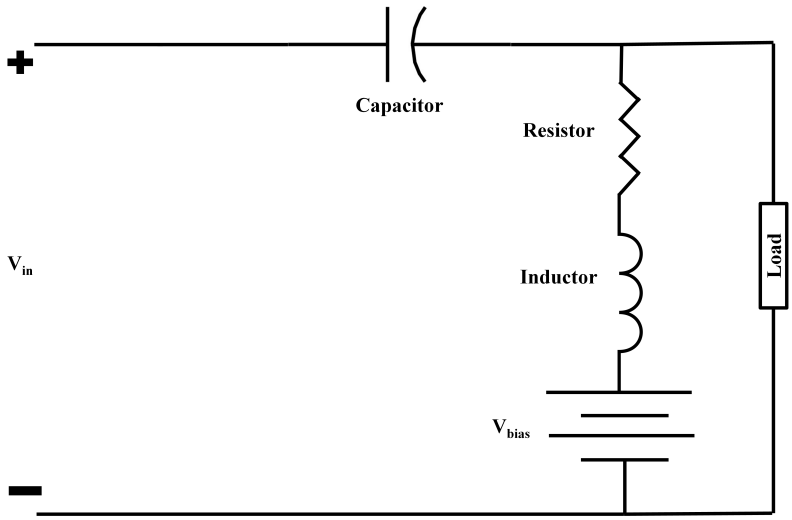


Figure 4.5: Bias tee circuit. The input is connected to one end of the capacitor and the dc bias is fed through an inductor.

One of the major concerns with the clamper circuit is that, it might not work at low temperatures around mK range as the diode is most likely to freeze out at that temperature. Diode works fine till 77 K but below that temperature it shows strange behaviours. Some specially made silicon diodes have shown to be working around 1.4 K. Although the diode chosen here is a highly doped diode (details in sub-section 4.3.3), which has lower tendency to freeze out, but its still not yet been tested (design submitted for fabrication, details in Appendix A).

If the clamper circuit doesn't work another similar circuit called bias tee is also design for the same purpose. The bias tee circuit consists of a capacitor, resistor and inductor. The input is supplied through the capacitor and the dc voltage is fed through an inductor. Figure 4.5 shows the circuit for a bias tee. The issue with bias tee is that, it requires some settling time depending on the value of the resistor and the capacitor. The area of the designed bias tee is around 180 um $\times$ 120 um.

4.2 Circuit Sizing

4.2.1 Switch

Here, circuit sizing needs to be done very carefully as the amplitude of the input signal is in millivolts and frequency is in GHz. Any distortion in pulse shape due to increase in RC delay is not acceptable. Loss in amplitude might be calibrated but still it should be as low as possible.

For all the transistors, length is 65 nm as the technology used to design and observe the performance of the circuits is TSMC 65 nm technology. Now, to calculate the width of the transistors first it is important to know the value of load. All the circuitry discussed here will be directly connected to the gate of the quantum dots. The gate capacitance of the quantum dots is very small in the range of 10's of aF. Considering the capacitance of the interconnects and clamper circuit the load to the switching network is approximate as 1 pF.

In the switch design, the pass gate NMOS and PMOS transistor widths are chosen to be 20 um after running simulations for 1 pF load with three cascaded switches as there are three switches between the input and the gates of the quantum dots in the node network. Widths lower than 20 um distorts the input signal due to RC delay and widths greater than 20 um improves the performance but considering the increase in size performance improvement is low. So, after considering the specifications a trade off between size and performance is made and 20 um is the chosen to be the width of the pass gate transistors. Here, for NMOS and PMOS both transistor sizes are chosen to be 20 um as in pass gate PMOS and NMOS aid each other rather than competing with each other (in other cases like in inverter usually width of PMOS is twice the width of NMOS as mobility of electron is higher than holes). The size of NMOS which is converting the high impedance state to logic zero can be small. The inverter to provide complimentary control signals to the pass gate is not a critical component of the circuit and can be smaller in size. Figure 4.6 shows input and output signals for different sizes of pass gate. The transistor level sizing for the switching circuit is shown in Figure 4.7.

4.2.2 Binary Demultiplexer Tree

The sizing of the demultiplexer tree will depend on the output load on the tree. The load to the binary demultiplexer tree is the pass gate switch. To determine how much capacitive load is provided by the pass gate switch the following approach is used:

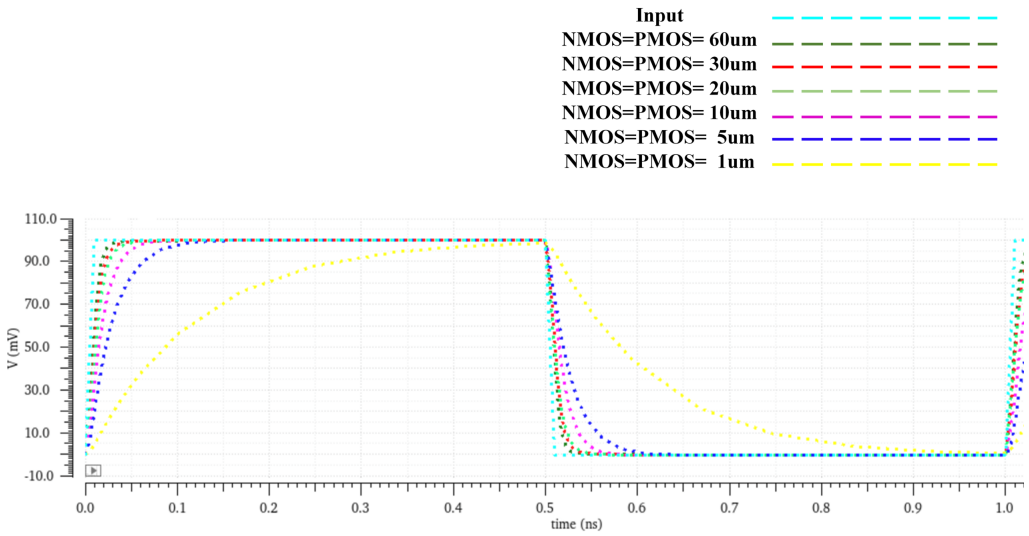


Figure 4.6: Input and output waves of 3 cascaded switches with different pass gate transistor sizing. With increasing size, the delay is reduced. After 20 um the improvement in performance is less compared to the size of the transistors.

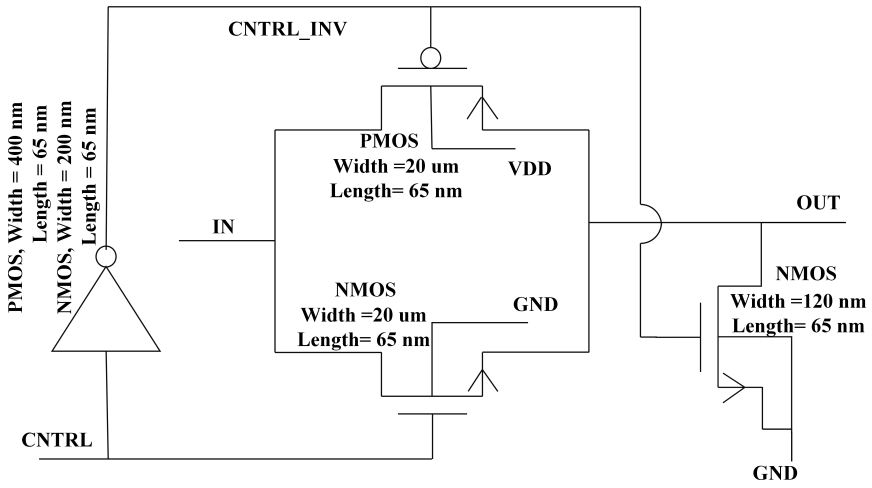


Figure 4.7: Pass gate switch with transistor sizes for the active high configuration. For active low configuration the sizes are same, only the inverter connection is opposite.

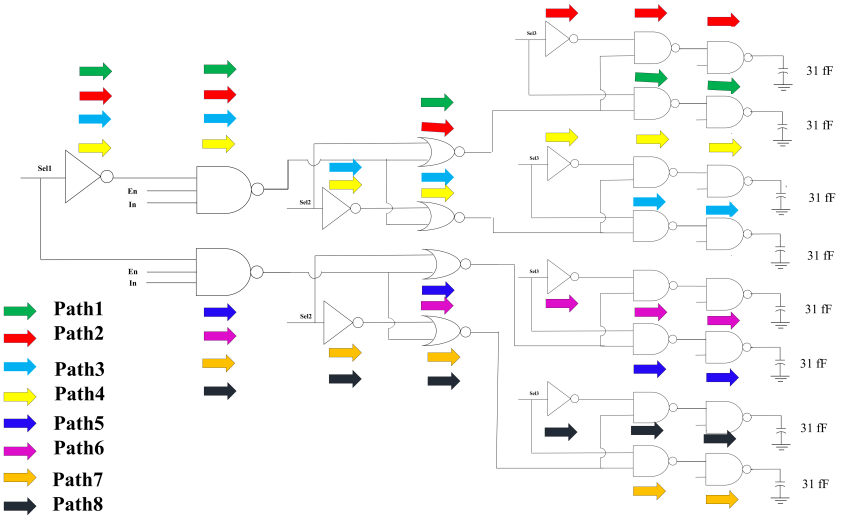


Figure 4.8: Gate level design of demultiplexer tree unit cell with different signal flow paths indicated. Each path has a load of 31 fF. At a certain time only one of these eight paths will be activated using Sel1, Sel2 and Sel3.

(i) An inverter is used to drive the pass gate switch.

(ii) The delay of the inverter is calculated.

(iii) Again, the same inverter is used to drive a capacitive load and by trial and error method for the delay calculated in (ii) the value of the capacitive load is determined.

Load calculated by this process = 21 fF and considering wire capacitance as 10 fF. So, total capacitive load = 21 fF + 10 fF = 31 fF.

Now, for 31 fF load using logical effort the transistor level sizing of binary demultiplexer tree is determined. Sizing calculations are done for three level binary demultiplexer tree as connected as shown in Figure 4.3. There are two different demultiplexer trees- one for hole creation and one for sending correction pulses. First considering the tree for hole creation shown in Figure 4.8. Figure 4.8 shows all the different paths signal can flow.

To determine the gate size, for a given output load input capacitance needs to be calculated. Input capacitance can be calculated using the following formula :

$$C_{in} = \frac{g \cdot C_{out}}{f} \tag{4.1}$$

Where, C_{in} = Input Capacitance;
C_{out} = Output Capacitance;
g = Logical effort of the gate;
f = Best stage effort = $\sqrt[n]{F}$
n = Total number of stages;
F= Total path effort = GBH;
G= Path logical effort;
B= Branch effort;
H= Electrical effort;

Path 1 Sizing :

$$G = 1 \times \frac{5}{3} \times \frac{5}{3} \times \frac{4}{3} \times \frac{4}{3} = \frac{400}{81}; \tag{4.2}$$

$$B = 1; \tag{4.3}$$

$$H = \frac{C_{load}}{C_{in}}; \tag{4.4}$$

$$C_{load} = 31fF; C_{in} = C_G; \tag{4.5}$$

$$C_G = W \cdot L \cdot \frac{\epsilon_{ox}}{t_{ox}} = W \cdot C_g = (W_n + W_p) \cdot C_g \tag{4.6}$$

$$=(W_n + W_p) \cdot \text{ 2fF (worse case)} \approx 2 \text{ fF}$$

So, from Equation 4.4 and Equation 4.5,

$$\text{H= } \frac{31fF}{2fF} = 15.5$$

$$\text{Now, F= GBH= } \frac{6200}{81}$$

Here, Total stage n= 5; So,

$$\text{f} = \sqrt[5]{\frac{6200}{81}} = 2.38$$

Working backward from output load using Equation 4.2,
5^{th} stage NAND gate (2- input) : $W_p + W_n = \frac{4 \times 31}{3 \times 2.38} \approx 17.37$

$\frac{W_p}{W_n} = \frac{2}{2}$; $W_p \approx 8.69$, $W_n \approx 8.69$;

4^{th} stage NAND gate (2- input) : $W_p + W_n = \frac{4 \times 17.37}{3 \times 2.38} \approx 9.73$

$\frac{W_p}{W_n} = \frac{2}{2}$; $W_p \approx 4.87$, $W_n \approx 4.87$;

3^{rd} stage NOR gate (2- input) : $W_p + W_n = \frac{5 \times 9.73}{3 \times 2.38} \approx 6.8$

$\frac{W_p}{W_n} = \frac{4}{1}$; $W_p \approx 5.44$, $W_n \approx 1.36$;

2^{nd} stage NAND gate (3- input) : $W_p + W_n = \frac{5 \times 6.8}{3 \times 2.38} \approx 4.76$

$\frac{W_p}{W_n} = \frac{2}{3}$; $W_p \approx 1.9$, $W_n \approx 2.86$;

1^{st} stage INVERTER : $W_p + W_n = \frac{1 \times 4.76}{2.38} \approx 2$

$\frac{W_p}{W_n} = \frac{2}{1}$; $W_p \approx 1.33$, $W_n \approx 0.67$;

Path 2 Sizing : From path 1 calculations, F = $\frac{6200}{81}$; f= 2.38

$$f_{nand} = \frac{f}{g} = \frac{2.38}{\frac{4}{3}} = 1.785$$

Now, for path 2,

$$\begin{gathered} \text{F}= f_{inv} \times f_{nand_1} \times f_{nand_2} \\ \text{or, } \frac{6200}{81} = f_{inv} \times 1.785 \times 1.785 \\ \text{or, } f_{inv} = 24.023 \end{gathered}$$

So, 1^{st} stage INVERTER in path 2 : $W_p + W_n = \frac{1 \times 9.73}{24.023} \approx 0.41$

$\frac{W_p}{W_n} = \frac{2}{1}$; $W_p \approx 0.27$, $W_n \approx 0.14$;

Using the same process for other paths the transistor sizes are calculated and for scaling simplicity close values of transistor sizes are approximately considered same. Table 4.3 shows all the sizes for the demultiplexer tree used for hole creation.

Circuit	1^{st} level demultiplexer		2^{nd} level demultiplexer		3^{rd}level demultiplexer		Other gates	
	NMOS um	PMOS um	NMOS um	PMOS um	NMOS um	PMOS um	NMOS um	PMOS um
Inverter	0.67	1.33	0.14	0.27	0.14	0.27	X	X
3- input NAND	2.86	1.9	X	X	X	X	X	X
2- input NOR	X	X	1.36	5.44	X	X	X	X
2-input NAND	X	X	X	X	4.87	4.87	8.69	8.69

Table 4.3: Transistor sizing for the demultiplexer tree used for hole creation.

Circuit	1^{st} level demultiplexer		2^{nd} level demultiplexer		3^{rd}level demultiplexer		Other gates	
	NMOS um	PMOS um	NMOS um	PMOS um	NMOS um	PMOS um	NMOS um	PMOS um
Inverter	0.67	1.33	0.18	0.36	0.18	0.36	7.5	3.8
3-input NAND	2.6	1.7	X	X	X	X	X	X
2-input NOR	X	X	1.1	4.4	X	X	4.8	19.3
2-input NAND	X	X	X	X	3.5	3.5	X	X

Table 4.4: Transistor sizing for the demultiplexer tree used for sending correction pulses.

Now, for sending correction pulses the demultiplexer tree includes an inverter and nor gate before the 31 fF load. The sizing calculations will be similar as before. Table 4.4 shows all the sizes for the demultiplexer tree used for sending correction pulses.

4.3 Performance Analysis

4.3.1 Switch

The input to the pass gate switch is in millivolts range around ± 100 mVs to ±200 mVs and the control signal will be either 0 V or 1 V depending on the type of operation in the node. The inputs can be a train of pulses with period as low as 1 ns or single pulses with pulse width as large as 100 ns. The amplitude of the input signal is always in mV range. For the operations on the quantum dots the signal levels needs to be precise and stable. For example, if a pulse with a pulse width of 100 ns and amplitude of 100 mV is applied

to the input, after passing through the switches the 100 mV level needs to be stable for the 100 ns time, any decaying in the signal level with time is not accepted. A little loss in amplitude can be accepted if its linear with increasing voltage as it can be calibrated. Figure 4.9 shows the outputs of the designed switch for different types of input signals for active high configuration. For ± 100 mV input, the output from the switch is also ± 100 mV and when the control signal is 0 V output goes to 0 V as observed in Figure 4.9a, 4.9b. For longer pulse width there is no decaying in the amplitude of the designed switch as shown in Figure 4.9d. For active low configuration all the results are similar, only the difference is in the control signal, when the control signal is 0 V input passes through the circuit and when the control signal is 1 V output goes to 0 V.

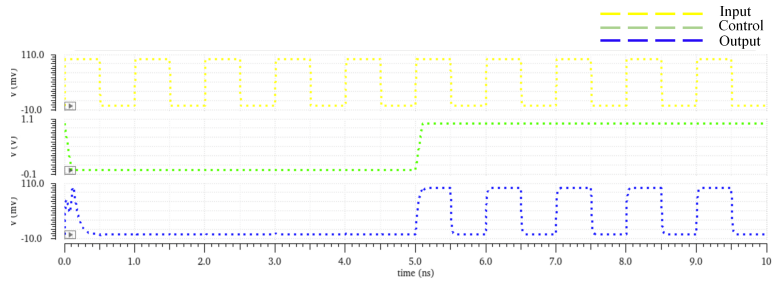
Another important thing to observe is the delay caused by the switching circuitry between input and output. Delay between two waveforms is usually calculated by, taking difference between the time each wave takes to reach half of its amplitude. Here, for 100 mV input delay is calculated by taking the time difference between input and output to reach 50 mV. The calculated delay for rising edge is 2.591 ps and for falling edge 2.377 ps for a pulse of 1 ns period. Figure 4.10 shows the maximum delay between input and output to reach the higher and lower level of amplitude. For the rising edge there is a delay of around 60 ps between the input and output to reach 100 mV amplitude and for the falling edge there is a delay of around 50 ps between the input and output to reach 0 V amplitude.

However, in the node network there are total three switches connected between input and output. So, it is very important to observe how the input is changing after passing through three switches as the input voltage amplitude is very small and it can be very fast. Figure 4.11 shows the difference between output after one switch and output after three switches. In the output after three switches the delay (calculated at half of the amplitude) in the rising edge and falling edge both is increased by 7 ps from the output after one switch.

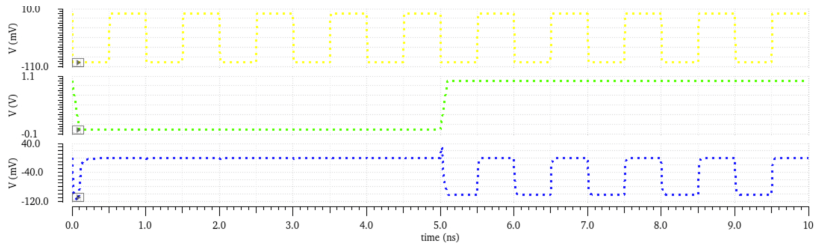
As these switches will operate in mK temperature, another important thing to consider is power consumption. Power consumed by the designed switch is shown in Figure 4.11. The power consumed due to conduction losses of the MOSFETs is as high as around 9 nW and due to switching losses is around 40 uW.

4.3.2 Demultiplexer Tree

The demultiplexer tree provides a control signal to the pass gate switch depending on the operation of the network. Table. 4.2 shows the truth table of the demultiplexer circuit. By



(a)



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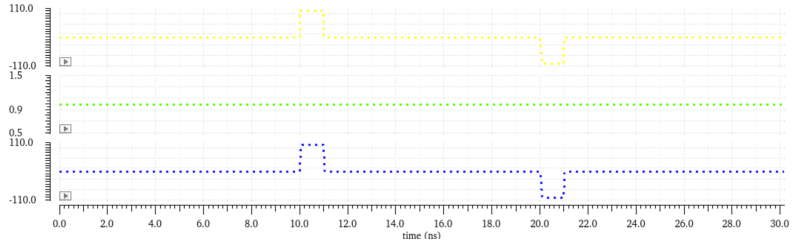

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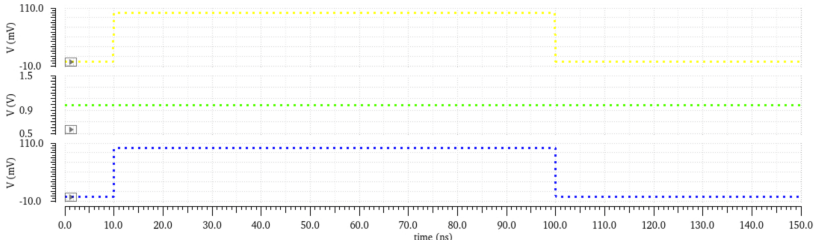
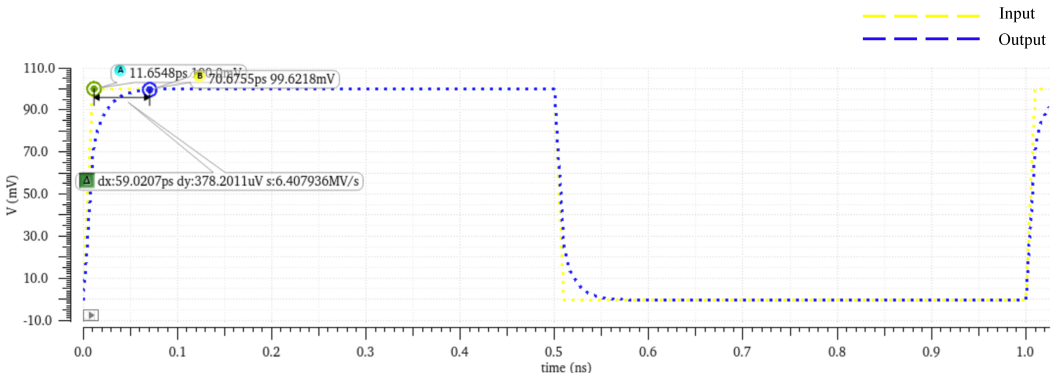
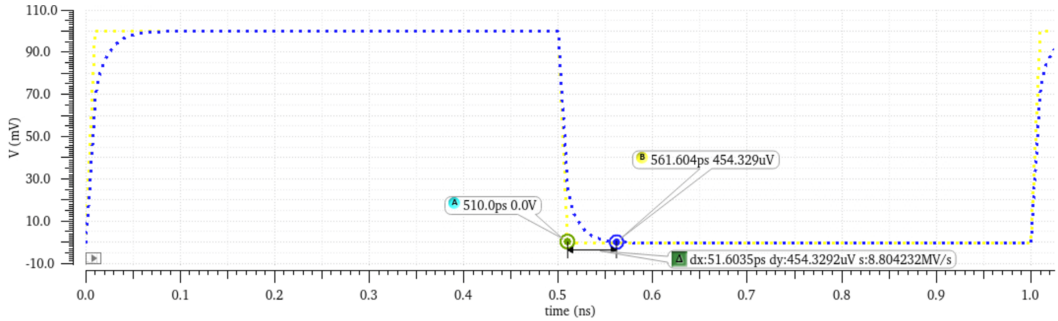


(d)

Figure 4.9: Output for (a) 100 mV pulse with 1 ns period for 0V and 1V control signals,(b) -100 mV pulse with 1 ns period for 0V and 1V control signals,(c) Two 100 mV and -100 mV amplitude pulse separated by 9 ns with 1V control signal, (d) Output for a pulse of 90 ns pulse width and 100 mV amplitude with 1V control signal. (Active high configuration)



(a)



(b)

Figure 4.10: Delay between input and output of a switch on (a) rising edge is around 60 ps to reach 100 mV amplitude , (b) falling edge is around 50 ps to reach 0 V amplitude.

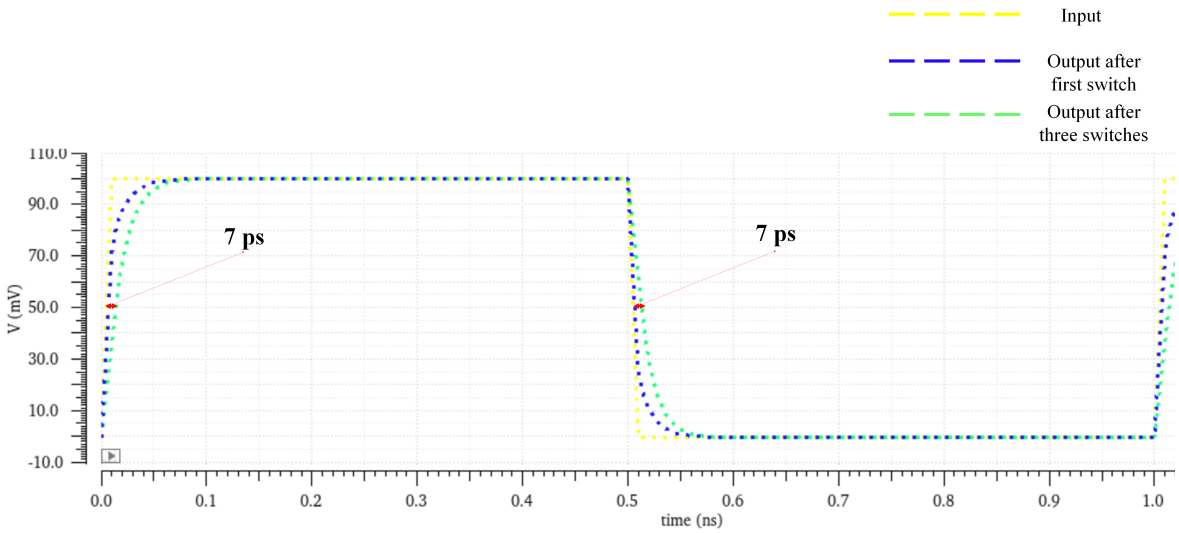


Figure 4.11: Delay between input, output after one switch and output after three switches cascaded.

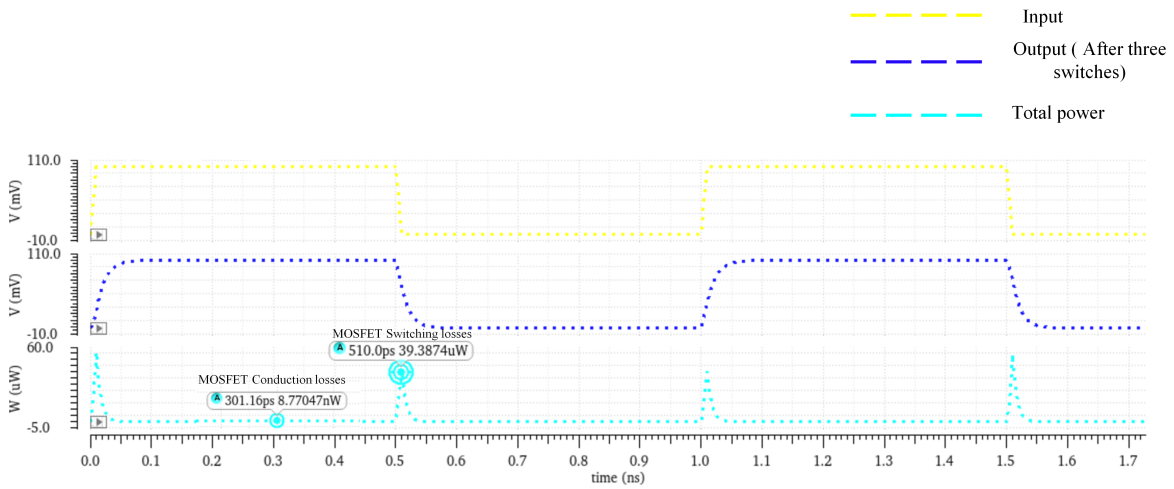


Figure 4.12: Power consumption of the designed switch. The power consumed due to conduction losses of the MOSFETs is around 9 nW and due to switching losses is around 40 uW.

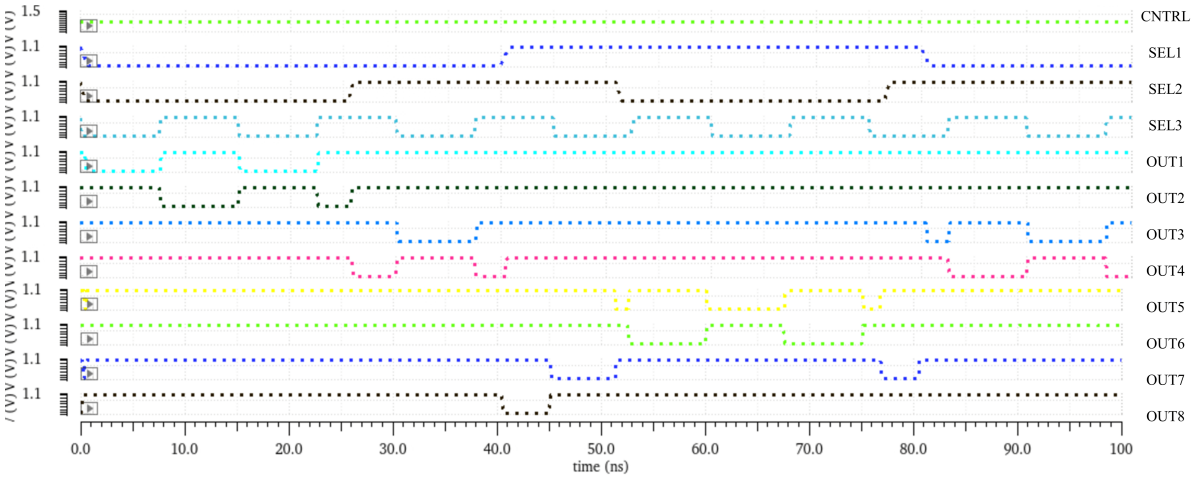


Figure 4.13: Addressing different demultiplexer channel by changing selection signals SEL1, SEL2 and SEL3. At a time only one channel can be addressed. (Here, En =1 for the considered time)

selecting proper values for the selection signals (Sel1, Sel2, Sel3) different outputs of the demultiplexer tree can be addressed for a particular time. Figure 4.13 shows how different output channels are addressed for different time period by selecting the channel.

There might be some glitches in the outputs as the rise time and fall time of the selection signals doesn't change abruptly rather it takes a little bit time. Glitches are not wanted in a circuit as they cause power dissipation and sometimes it may assign wrong values to the output. The good news is that there are many ways to remove glitches from the circuits. Carefully re-timing the selection signals can assure that, the rise time and fall time doesn't contribute to any glitches. Hazard filtering and balanced path delay techniques can also help in removing glitches. The switching activity should be as low as possible to avoid transitions so that both the glitches and unnecessary power dissipation is reduced.

4.3.3 Clamper Circuit/ Bias tee

Clamper circuit have a capacitor and a diode as shown in Figure 4.4. The capacitor of the clamper circuit creates a voltage divider with the output capacitance. The capacitance of the clamper circuit is chosen to be 1 pF and the output load is also approximately 1 pF. So, the clamper circuit will reduce the amplitude of the input signal by almost half due to the voltage divider formed.

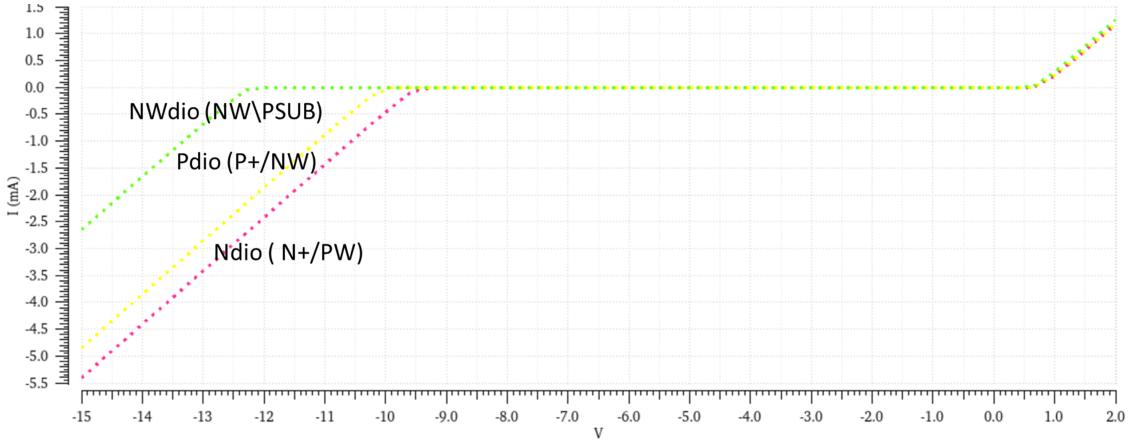


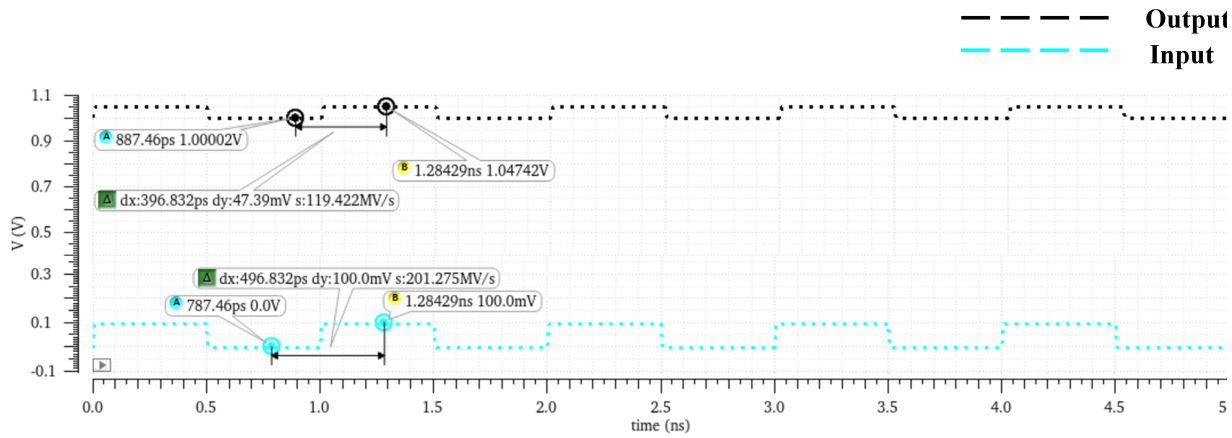
Figure 4.14: I-V characteristics of NW-diode, P-diode and N-diode.Greater the breakdown voltage, lower the doping density.

Here, the diode used is p-diode. As the circuit will be operating at very low temperature (in mK range), the diode has a chance of suffering from freeze out. If the diode is lightly doped there is a higher chance of freeze out. Highly doped diodes have an impurity band which overlaps with the conduction or valence band rather than having a single donor level. This kind of overlap between two bands results in free carriers even at zero Kelvin.

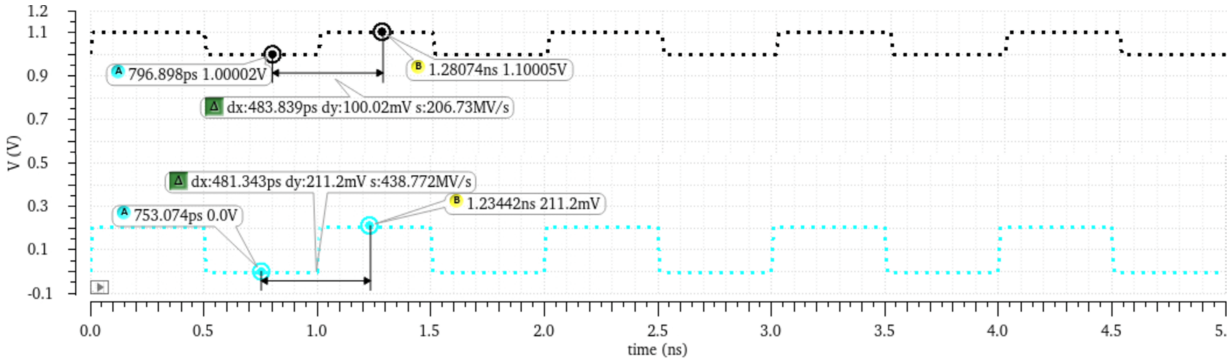
The breakdown voltage of the diode is inversely proportional to the square of the doping density. So, roughly greater the breakdown voltage lowers the doing density. Figure 4.14 shows the I-V characteristics of different diode from TSMC 65 nm technology. The p+/nW diode and n+/pw diode have lower breakdown voltage than nw/psub diode and hence more suitable for low temperature applications.

Figure 4.15 shows the input and output from the clamper circuit designed with 1 pF capacitor and p-diode for a load of 1 pF. From the figure it can be observed that input calibration is required to get 100 mV output due to the divider form between the clamp capacitor and output load. Here, for 211.2 mV input, the output is 100 mV. The dc voltage supplied 1 V and so the output is shifted to 1 V.

For bias tee, the capacitor value used is also 1 pF which creates a voltage divider with the load capacitance. As the load capacitance is 1 pF, the output voltage amplitude is almost half of its amplitude. By calibrating the input, required output voltage can be obtained. The issue with bias tee is that depending on the value of R and C it takes some time to settle to the dc voltage. Once it settles to the value then there is no decaying in the amplitude.



(a)



(b)

Figure 4.15: (a) Output for 100 mV input to clamper circuit is roughly around 50 mV due to the voltage divider formed between the load and clamper circuit capacitance, (b) 211.2 mV input gives 100 mV output (dc voltage = 1 V).

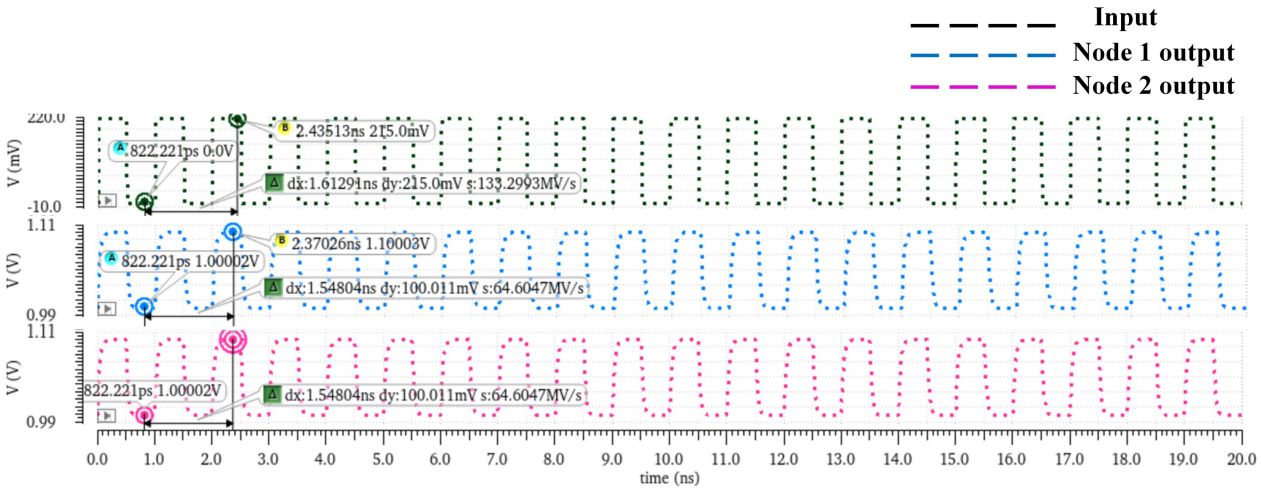


Figure 4.16: Normal operation in two nodes for 215 mV, 1 ns pulse train. Output is around 100 mV at 1 V dc level.

4.3.4 Simulation Results of Full Network Circuitry

The network is simulated for two nodes. Each node has one gate for simplicity of simulation. Two demultiplexer tree is added for hole creation and one demultiplexer tree is for sending correction pulses. There are total three switches connected between input to output. The first switch, which is an active high switch, is controlled by a digital signal (0 V/ 1 V) replicating the shift register output for global control. Second switch, which is an active low switch, is connected to both demultiplexing tree for hole creation through a nand gate. Finally, third switch, which is also an active low switch, is connected to the demultiplexer tree for sending correction pulses. A clamp circuit is added after the switches to provide the dc level to the dots.

Figure 4.16 shows normal operation in two nodes. The input is a 215 mV, 1 ns pulse train. It can be observed that, the input signal is directly passing to the output with the added dc voltage level from clamp circuit as all the switches are closed in normal operation.

Figure 4.17 shows holes created in both the nodes at different time period which means, using demultiplexer tree node 1 is addressed from 0 to 3.5 ns and node 2 is addressed from 7 to 10.5 ns. Figure 4.18 indicates the simultaneous hole creation in both nodes which means, both the demultiplexer tree for hole creation is addressing two different nodes at the same time.

In case of sending correction pulses first all the inputs to the nodes are turned off and

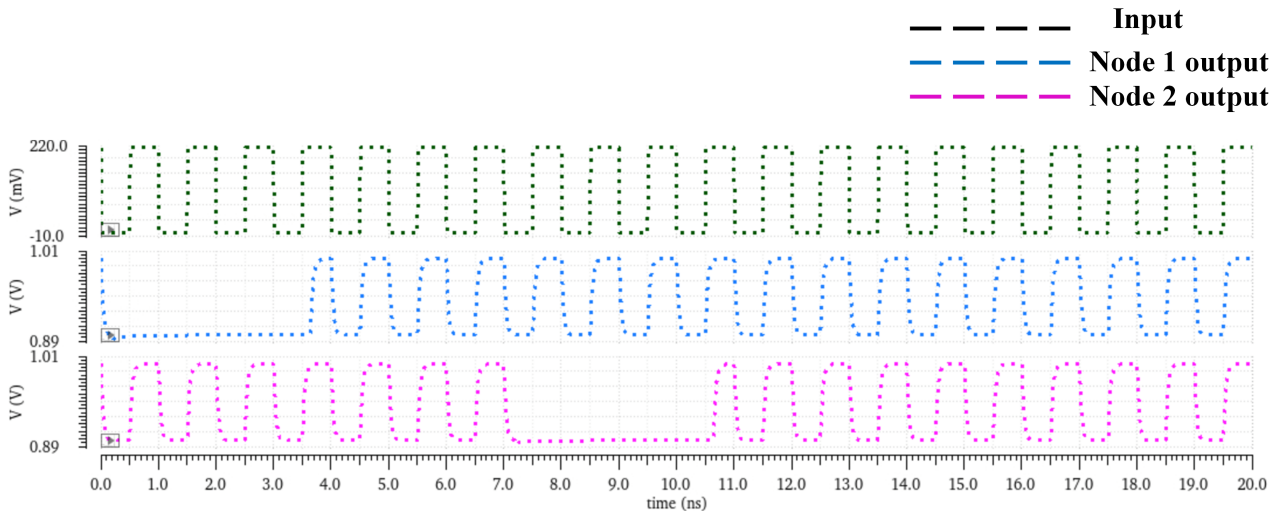


Figure 4.17: Hole is created in node 1 from 0 s to 3.5 ns and in node 2 from 7 ns to 10.5 ns.

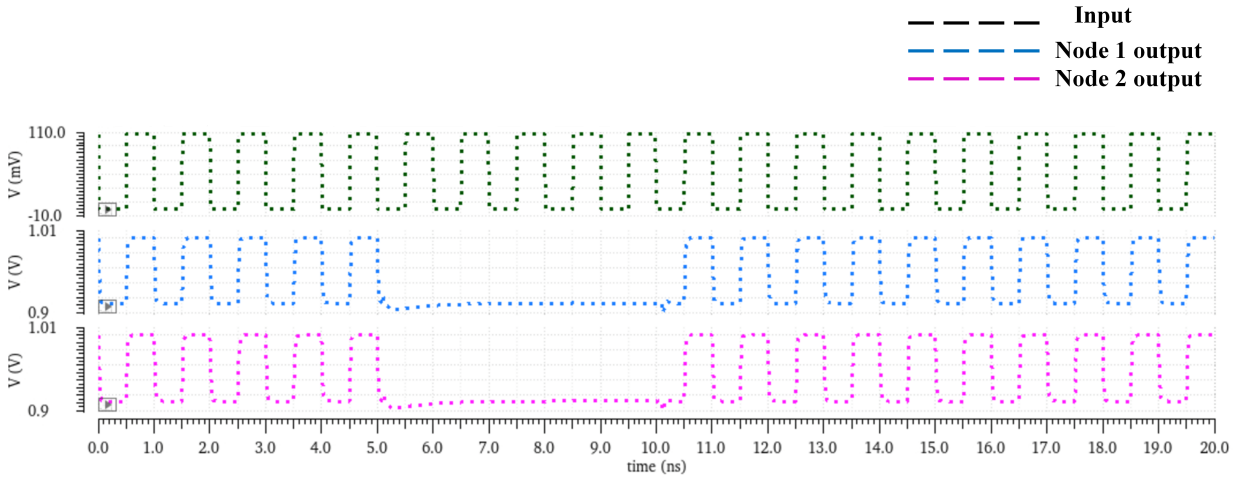


Figure 4.18: Hole is created simultaneously in node 1 and node 2 from 5 ns to 10 ns.

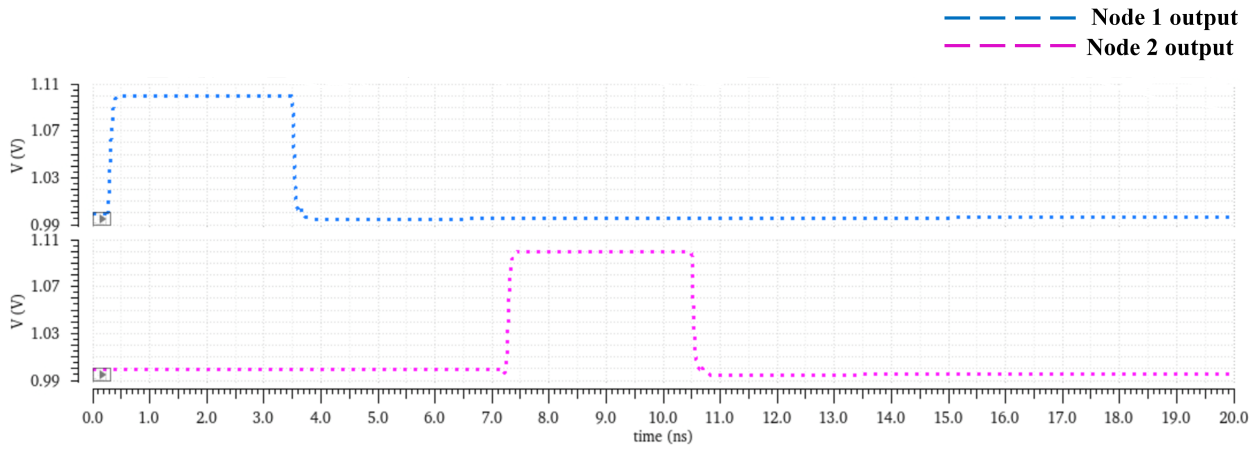


Figure 4.19: Corrective pulses send to node 1 from 0 s to 3.5 ns and node2 from 7 ns to 10.5 ns.

then a correction pulse is sent to the desire node as shown in Figure 4.19. Here, it can be observed that when corrected pulses are sent to a certain node at that time other node voltage is fixed at the dc level and no input passes to the output.

Chapter 5

Pre-tuning Quantum Dots in the Network

Silicon metal-oxide-semiconductor (MOS) qubits are one of the most promising platforms for a future quantum information processor. In such a network, all the quantum dots operating at the same time are controlled by the same external voltage. Such a global operation is only possible, if all the quantum dots in the system are at the same potential (Chapter 4 's operations are based on this assumption). But due to fabrication variations, dot position and system configuration the potential of individual dots varies in the network. To solve this issue and pre-tune all the dots to be at the same potential, an idea of adding floating gates to the silicon MOS quantum dot devices is introduced here. By setting voltages on floating gate it is possible to tune individual dots so that, the global control can work. While dealing with thousands of qubits this kind of idea can give much better scalability.

Figure 5.1 shows the structure of the Silicon MOS quantum dots. The device is composed of four layers. First a layer of Si-substrate, followed by a layer of SiO_2. Then, the first metal layer is introduced which is known as the screening gate. A screening gate layer prevents accumulation of electrons under the section of the plunger metal gate which overlaps screening gate. The second metal layer is the plunger gate layer. The potential on the plunger gate controls the electron occupancy of quantum dot.

The floating gate is considered in the same layer as the screening gate. The orientation of such an arrangement is shown in Figure 5.2. Observations are made by changing the geometry and position (d) of the floating gate.

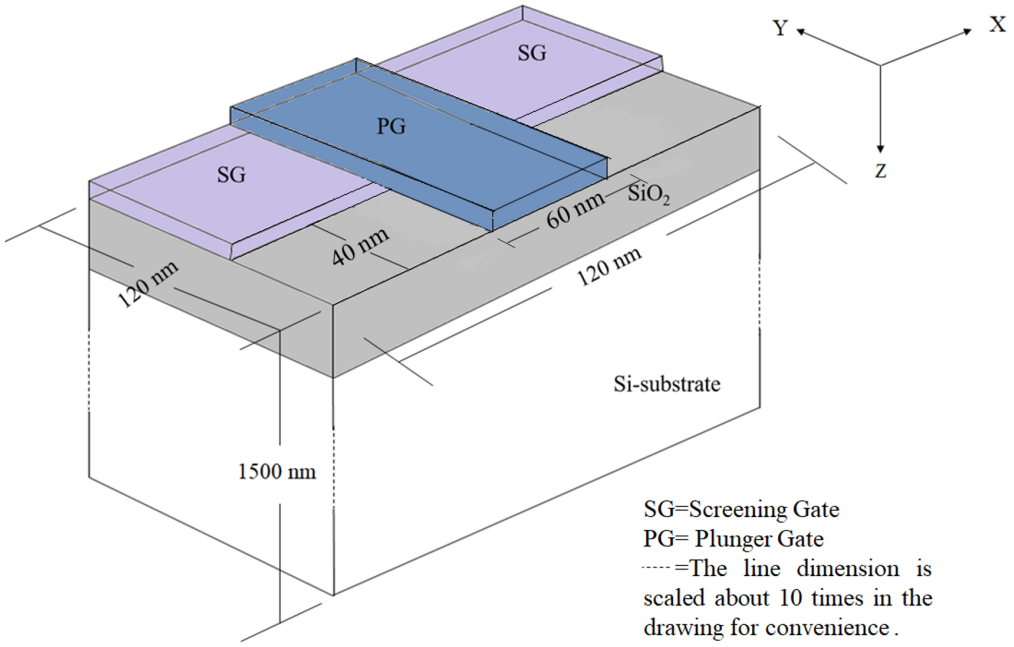


Figure 5.1: Silicon MOS quantum dot device. Quantum dot is formed under the section of PG, where it doesn't overlap the SG.

5.1 Floating Gate for Pre-tuning Quantum Dots

To observe the effectiveness of adding a floating gate to pre-tune quantum dots, a structure like the one showed in Figure 5.2 is simulated in a software named nextnano. A single quantum dot is formed for observation purpose. Figure 5.3 shows the density of electron (10^{18}e/cm) in the single dot formed on the interface of Si-substrate and SiO_2.

The physical phenomenon can be understood from the vertical energy band diagram. Figure 5.4 shows the vertical energy band diagram. Band banding occurs between the interface of Si-substrate and SiO_2. Quantum dot is formed around 17 nm into the SiO_2 for the dimensions considered.

To understand the effectiveness of the floating gate the way results are computed is summarize below:

(i) Firstly, without any floating gate simulations are conducted to find the potential on the plunger gate (V_p) which accumulates a single electron in the quantum dot. Here, the total charge density is integrated over the surface to determine the number of electrons

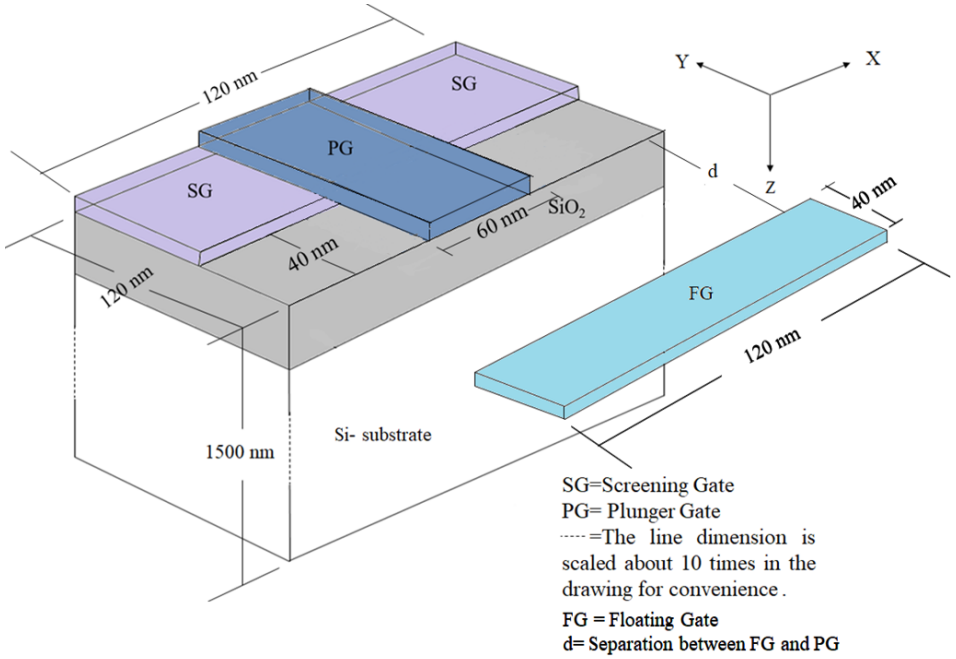


Figure 5.2: Silicon MOS quantum dot device with floating Gate. FG is in the same layer as SG.

accumulating.

(ii) Then, some deviations (δV_p) are added to the plunger gate voltage, V_p, which changes the electron accumulation in the dot.

(iii) Now, the floating gate is added to the simulation. The voltage on the floating gate (V_f) which can compensate for the deviations, that is, which can again accumulate single electron in the quantum dot is determined.

Here, Figure 5.5 shows for different voltage deviation on plunger gate how much voltage is needed on the floating gate to get back to the single electron accumulation on the quantum dot. The separation between the floating gate and the plunger gate (d) is varied. When, d is maintained at 20 nm single electron accumulation in the quantum dot is obtained at 0.655 V plunger gate voltage and when d is 30 nm, single electron accumulation in the quantum dot is obtained at 0.617 V plunger gate voltage. For d= 40 nm, single electron accumulation occurs at 0.592 V plunger gate voltage.

From Figure 5.5, it can be observed that as the voltage deviation is increasing on plunger gate (V_p), more voltage is required on the floating gate (V_f) to compensate for the

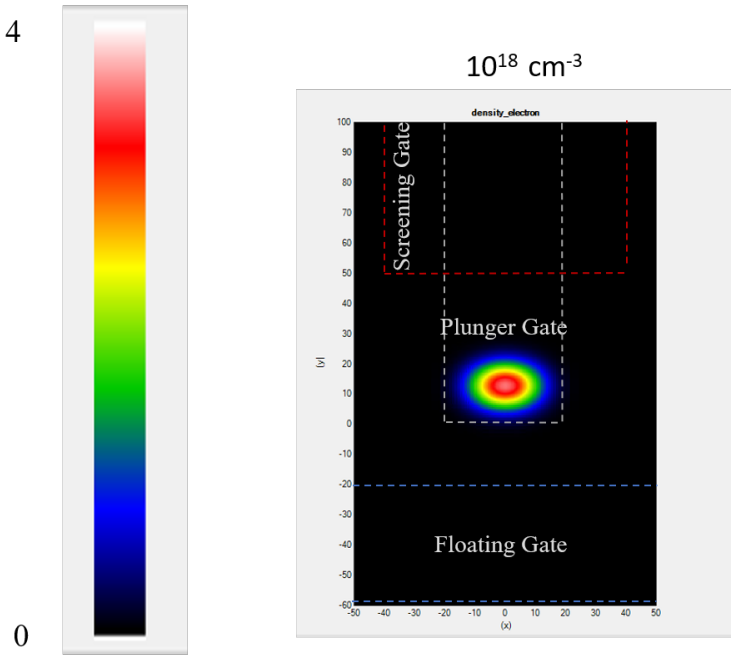


Figure 5.3: Density of electron (10^{18}e/cm) in the quantum dot. (x= length of the device; y = Total scale considered summing the width of the device, separation between floating gate and plunger gate, and floating gate width)

deviation and the floating gate shows a linear response with changing voltage deviation.

By observing Figure 5.5 it can also be noted that the effectiveness of the floating gate depends on the distance of floating gate from the plunger gate. It can be summarized that, with every 10 nm decrease in distance between floating gate and plunger gate about 10% less voltage is required on the floating gate for same deviations. On the other hand, for 10 nm increase in the separation, about 10% more voltage is required on the floating gate at the same deviation. So, closer the floating gate to the plunger gate the more control it has over the dot position. Table 5.1, Table 5.2, Table 5.3 and Figure 5.6 clearly illustrate this dependency.

Now, if the size of the floating gate is reduced the effectiveness of the gate is reduced. For example, if the length of the gate is made $\frac{1}{3}$ of the previously considered gate (120 nm) we can observe from Table 5.4 that the floating gate voltage required to regain the single electron accumulation in the dot is more than 1.5 times the previous voltage.

As the floating gate is now made $\frac{1}{3}$ of the previous one it can be moved left and right

Distance,d (nm)	δV_p (V)	V_f (V)	$\frac{V_f}{\delta V_p}$
10	0.05	-0.055	1.1
20	0.05	-0.065	1.3
30	0.05	-0.075	1.5
40	0.05	0.083	1.66
50	0.05	0.093	1.86
10	-0.05	0.051	1.02
20	-0.05	0.064	1.28
30	-0.05	0.07	1.4
40	-0.05	0.079	1.58
50	-0.05	0.088	1.76

Table 5.1: Floating gate voltage (V_f) with changing position of the gate (d) for $\pm$ 0.05 V voltage deviation on plunger gate (δV_p).

Distance,d (nm)	δV_p (V)	V_f (V)	$\frac{V_f}{\delta V_p}$
10	0.1	-0.109	1.09
20	0.1	-0.125	1.25
30	0.1	-0.145	1.6
40	0.1	0.166	1.66
50	0.1	0.185	1.85
10	-0.1	0.101	1.01
20	-0.1	0.123	1.23
30	-0.1	0.138	1.38
40	-0.1	0.153	1.53
50	-0.1	0.17	1.7

Table 5.2: Floating gate voltage (V_f) with changing position of the gate (d) for $\pm$ 0.1 V voltage deviation on plunger gate (δV_p).

Distance,d (nm)	δV_p (V)	V_f (V)	$\frac{V_f}{\delta V_p}$
10	0.15	-0.165	1.1
20	0.15	-0.2	1.33
30	0.15	-0.227	1.51
40	0.15	0.256	1.71
50	0.15	0.284	1.89
10	-0.15	0.148	0.987
20	-0.15	0.178	1.187
30	-0.15	0.199	1.327
40	-0.15	0.22	1.467
50	-0.15	0.24	1.6

Table 5.3: Floating gate voltage (V_f) with changing position of the gate (d) for $\pm$ 0.15 V voltage deviation on plunger gate (δV_p).

δV_p (V)	V_f (V) Floating gate length (L_f) =120 nm	V_f (V) Floating gate length (L_f) =40 nm	$\frac{V_f}{\delta V_p}$ (L_f =120 nm)	$\frac{V_f}{\delta V_p}$ (L_f =40 nm)	Increment
0.05	-0.075	-0.125	1.5	2.48	1.65
0.1	-0.16	-0.225	1.6	2.55	1.59
0.15	-0.227	-0.382	1.51	2.547	1.69
-0.05	0.07	0.12	1.4	2.4	1.71
-0.1	0.138	0.23	1.38	2.3	1.67
-0.15	0.199	0.298	1.33	1.99	1.5

Table 5.4: Effect of reducing the size of floating gate by $\frac{1}{3}$.

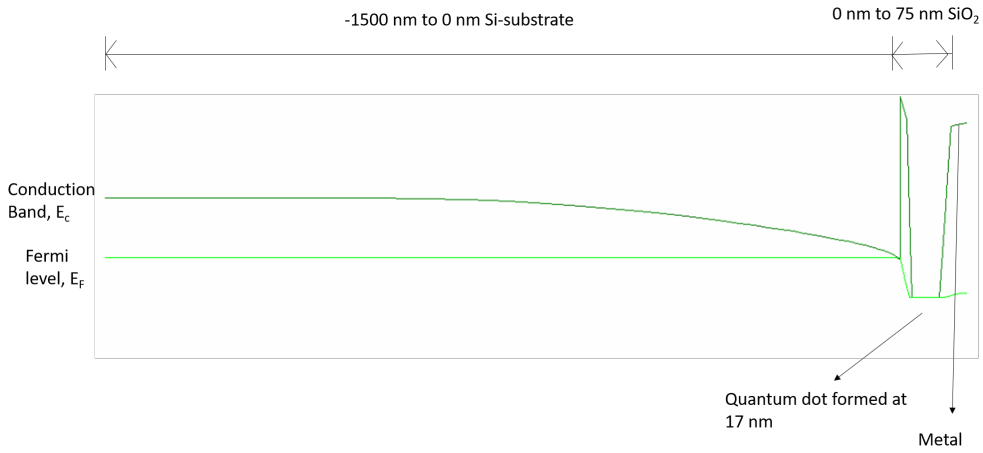


Figure 5.4: Energy band diagram of silicon MOS quantum dot (Along z axis at x = 0 nm and y = 0 nm). At the interface of Si-substrate and SiO_2 band banding occurs. Quantum dot formed at 17 nm into the SiO_2.

δV_p (V)	V_f (V) Left Position	V_f (V) Right Position	$\frac{V_f}{\delta V_p}$ Left Position	$\frac{V_f}{\delta V_p}$ Right Position
0.05	-0.163	-0.16	3.26	3.2
0.1	-0.33	-0.33	3.3	3.3
0.15	-0.51	-0.51	3.4	3.4

Table 5.5: Effect of Changing the lateral position of the floating gate.

directions also as shown in Figure 5.7.

Results are investigated by changing the position to left and right. In both cases, almost 1.5 times more voltage than the middle position is required to get back to the single electron point as shown in Table 5.5. The middle position seems the ideal one in these three cases.

5.2 Observing Charging Energy of Quantum Dots

While analyzing a quantum dot, some characteristics are important to observe and any significant change in these characteristics after adding the floating gate might cause serious issues in operation of the system. One of the such characteristic is charging energy. It is

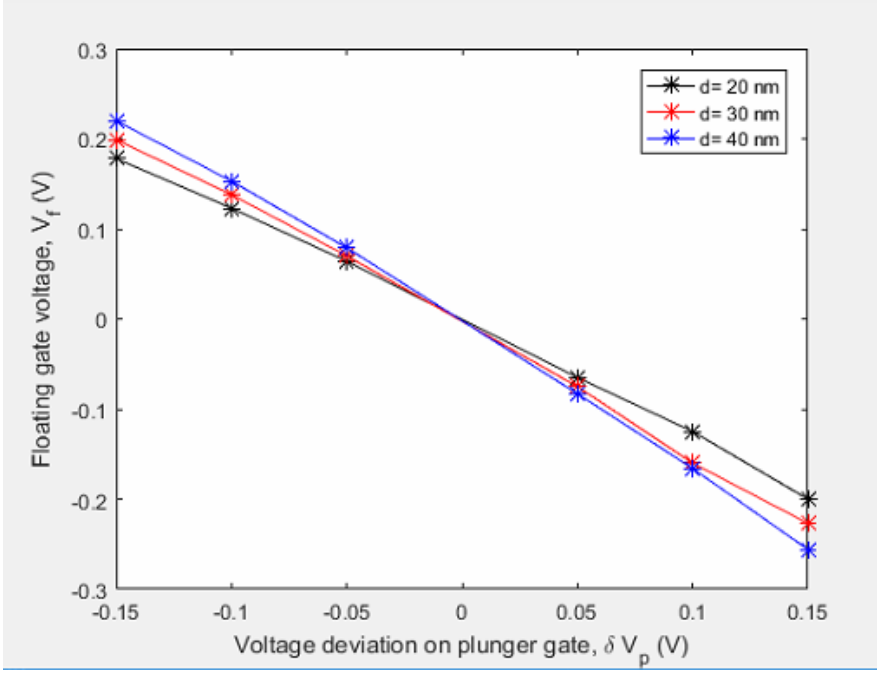


Figure 5.5: Floating gate voltage (V_f) with changing voltage deviation on plunger gate voltage (δV_p) for d=20 nm, 30 nm, and 40 nm. As the voltage deviation is increasing on V_p, more voltage is required on V_f to compensate for the deviation and if the distance (d) between floating gate (FG) and plunger gate (PG) is increased more voltage is required on FG for same voltage deviation on PG.

the energy required to add or remove a single electron from the dot. The charging energy (E_c) is calculated using the formula,

$$E_c = \frac{e^2}{2C} \tag{5.1}$$

Where, e= Charge of electron= 1.61×10^{-19} C;

C = Capacitance of the dot = $8\epsilon_r\epsilon_o$R ;

Here, ϵ_r= 11.68

ϵ_o= 8.85×10^{-12} F/m

R = Radius of the dot, which is the only parameter that is variable. So, observations are made to understand if this radius is different before and after using the floating gate to compensate for the deviations in the plunger gate.

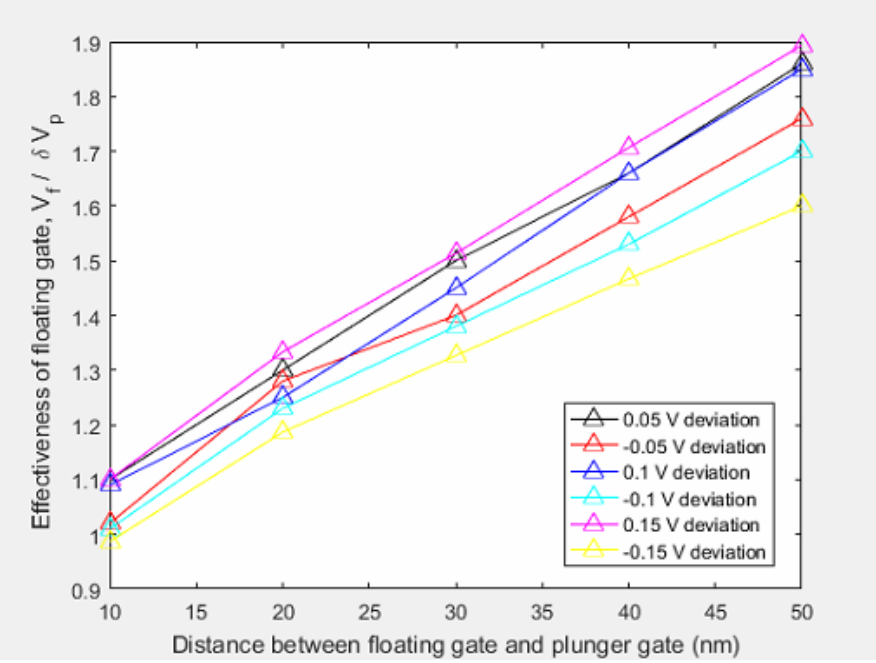


Figure 5.6: Floating gate voltage (V_f) with changing position of the gate (d) for ± 0.05 V, ± 0.1 V and ± 0.15 V voltage deviation on plunger gate (δV_p). Effectiveness of V_f reduces with increasing d.

Here, the dot is not perfectly circular, it's elliptical in shape. So, it has a major axis value (a) and minor axis value (b). The goal is to determine the major and minor axis values before and after the floating gate is added.

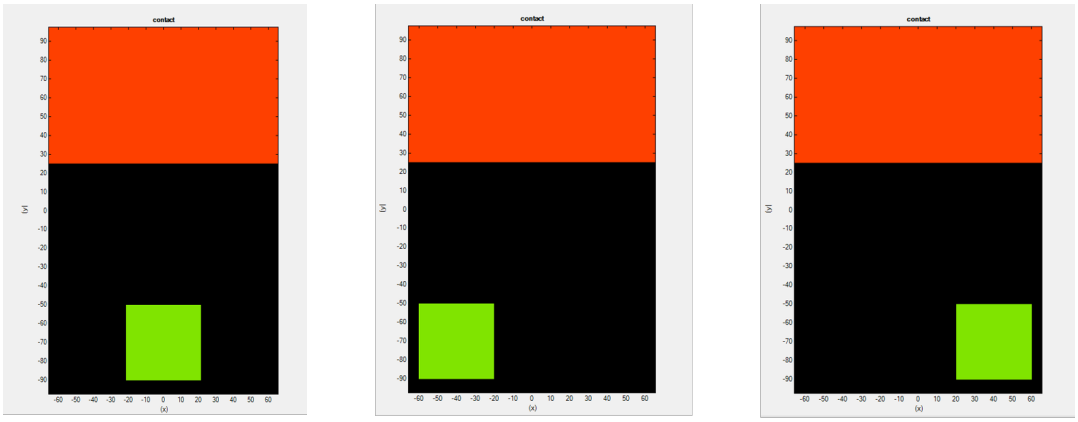
Calculating major axis (a) of the quantum dot :

By solving the schrodinger equation we have the 2D electron wavefunction. Major axis, a, of the dot is along the length (x axis) of the device shown in Figure 5.2. The step by step process of determining a is given below -

(i) First 2D electron wavefunction along the length (x axis) and depth (z axis) of the device at the maximum probability of the function along the width (y axis or minor axis) is extracted. Figure 5.8 (a) shows the extracted 2D wavefunction.

(ii)Then a slice of the 2D wavefunction is cut along x axis at the maximum probability of the function along z axis, which is showed in Figure 5.8 (b).

(iii) Now, to determine the major axis of the dot the standard deviation(σ) of the 1D slice is calculated. From Figure 5.8 (b) it can be observed that, 3 σ limit is set to reach



(a) (b) (c)

Figure 5.7: Screening gate (red) and floating gate (green) (a) in the middle position (at 0 offset), (b) in the left position (40 nm offset in the left direction), (c) in the right position (40 nm offset in the right direction).Here, d = 30 nm.

the tail of the wavefunction.

Another important property to note is the dot position. Observations are made to determine if the dot position is changed after adding the floating gate. In case of the major axis, it can be determined by noting the peak of the 1D slice along x axis. The peak is always at 0 nm. So, in the x direction there is no change in the dot position.

Table 5.6 and Table 5.7 shows the change in major axis of the dot with added deviations and floating gate voltage. It can be observed that if the positive deviation on plunger gate is increased the major axis length is increased and if the negative deviation on plunger gate is increased the major axis length is decreased. We can conclude from Table 5.6 that, at 20 nm separation between the plunger and floating gate, addition of floating gate voltage regains the initial value of the major axis (before any deviation was added) with maximum $\pm$ 5% variation for the considered cases of deviations. When the separation between the plunger and floating gate is 30 nm the variation is increased to $\pm$ 7% (Table 5.7).

Calculating minor axis (b) of the quantum dot :

Minor axis, b, of the dot is along the width (y axis) of the device. The step by step process of determining b is given below -

(i) First the 2D electron wavefunction along the width (y axis) and depth (z axis) of the device at the maximum probability of the function along the length (x axis or major axis) is extracted. Figure 5.9 (a) shows the extracted 2D wavefunction.

Deviation V	Major axis, a (without floating gate) nm	Major axis, b (with floating gate) nm
-0.15	23.20	36.97
-0.1	25.67	36.21
-0.05	30.56	35.42
0	**34.84**	**34.84**
0.05	39.57	34.17
0.1	44.96	33.64
0.15	51.8	33.20

Table 5.6: Change in major axis of the dot with deviation and floating gate voltage. (floating gate at 20 nm distance from the plunger gate)

Deviation V	Major axis, a (without floating gate) nm	Major axis, b (with floating gate) nm
-0.15	23.69	38.05
-0.1	24.77	37.0
-0.05	30.53	36.26
0	**35.53**	**35.53**
0.05	40.95	34.82
0.1	47.11	34.18
0.15	57.07	33.66

Table 5.7: Change in major axis of the dot with deviation and floating gate voltage. (floating gate at 30 nm distance from the plunger gate)

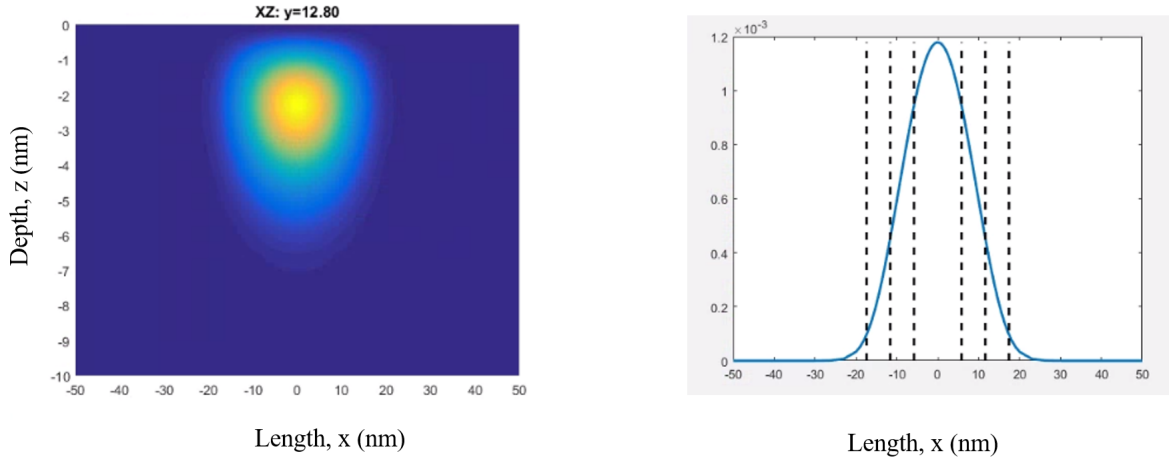


Figure 5.8: (a) 2D wavefuction Along x and z axis at y = maximum probability, (b) 1D cut along x at y, z = maximum probability.

(ii)Then a slice of the 2D wavefunction along y axis at the maximum probability of the function along z axis is cut, which is showed in Figure 5.9 (b).

(iii) Now, to determine the minor axis of the dot the standard deviation(σ) of the 1D slice is calculated. 3 σ limit is considered to get to the tail of the curve.

To determine the shift of dot position along minor axis we observe the peak of the 1D slice along y axis. Along the minor axis the dot position is changed as the floating gate is added. This change is expected due to the orientation of the floating gate.

Table 5.8 and Table 5.9 shows the change in the length and position of the dot minor axis with added deviations and floating gate voltage. It can be observed that if the positive deviation on plunger gate is increased the minor axis length is increased and if the negative deviation on plunger gate is increased the minor axis length is decreased. We can conclude from Table 5.8 and Table 5.9 that, at 20 nm and 30 nm separation between plunger gate and floating gate, addition of floating gate voltage helps to get back to the initial length of the minor axis (without any deviation) with maximum 10 % variation for the considered cases of negative deviation and - 5% variation for positive deviations.

In case of the dot position along y axis, when the deviation is added the dot position is almost same as before but when floating gate is used to compensate the deviation the dot position is changed. When floating gate is compensating for the positive deviation, i.e when negative voltage is added to the floating gate the quantum dot is pushed towards

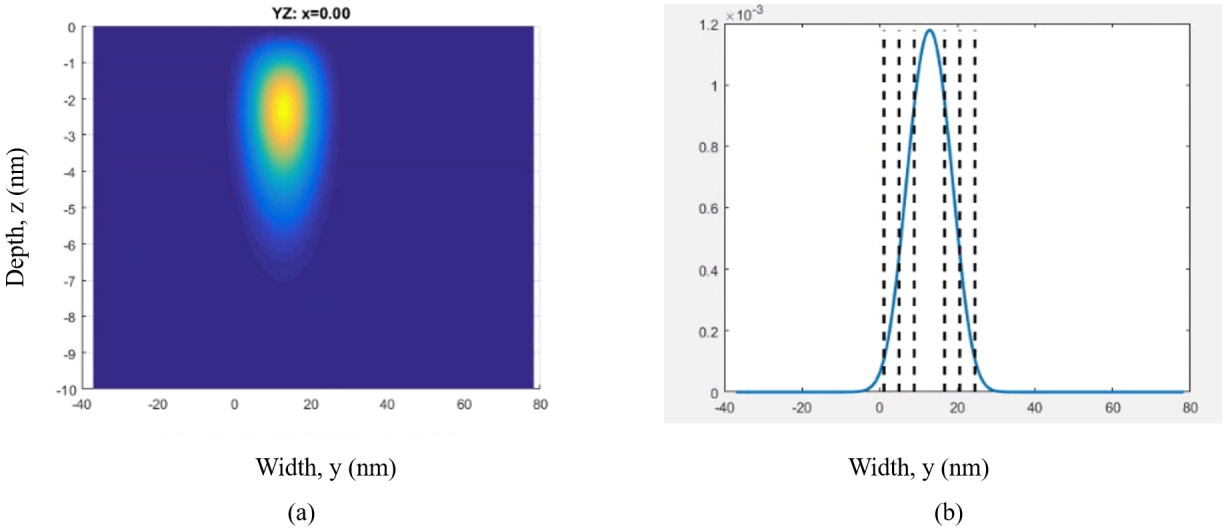


Figure 5.9: (a) 2D wavefuction Along y and z axis at x = maximum probability, (b) 1D cut along y at x, z = maximum probability.

the screening gate from the initial position by 10% for the considered deviations. When floating gate is compensating for the negative deviation, i.e when positive voltage is added to the floating gate the quantum dot is shifted towards the floating gate from the initial position by 5% for the considered deviations .

Once the values of major axis and minor axis are calculated, we can observe the change in charging energy using Equation 5.1. Equation 5.1 is defined for a circle so it consists of a radius term. As the quantum dot formed is of elliptical shape, we have the major axis and minor axis values. So, Equation 5.1 might not give us the exact charging energy but we can have the idea about how charging energy is affected due to the addition of floating gate. As the radius is inversely proportional to the charging energy, an increase in the shape of dot will decrease the energy and decrease in the dot shape will increase the charging energy. If we calculate the radius of the dot as the average value of major axis and minor axis to determine the charging energy we get the results as shown in Table 5.10.

So, From Table 5.10 we observe that adding of floating gate almost regain the initial charging energy with a variation below ±10%.

Deviation V	Minor axis, a nm	Peak nm	Minor axis, b nm	Peak nm
	without floating gate		with floating gate	
-0.15	18.40	13.08	25.43	10.20
-0.1	19.51	12.80	24.65	11.29
-0.05	21.69	12.80	23.98	12.01
0	**23.43**	**12.80**	**23.43**	**12.80**
0.05	24.88	12.80	22.91	13.66
0.1	26.30	12.80	22.46	14.27
0.15	28.52	13.08	22.08	14.59

Table 5.8: Change in minor axis of the dot with deviation and floating gate. (floating gate at 20 nm distance from the plunger gate)

Deviation V	Minor axis, a nm	Peak nm	Minor axis, b nm	Peak nm
	without floating gate		with floating gate	
-0.15	19.16	11.29	27.26	7.81
-0.1	19.60	11.29	26.13	9.09
-0.05	22.54	11.06	25.31	10.20
0	**24.63**	**11.06**	**24.63**	**11.06**
0.05	26.42	11.06	24.00	12.01
0.1	28.33	11.29	23.46	12.53
0.15	32.20	11.52	22.99	13.36

Table 5.9: Change in minor axis of the dot with deviation and floating gate. (floating gate at 30 nm distance from the plunger gate)

Deviation V	Charging Energy (without floating gate) meV	Charging Energy (with floating gate) meV
-0.15	9.03	5.93
-0.1	8.72	6.13
-0.05	7.29	6.28
0	**6.40**	**6.40**
0.05	5.74	6.58
0.1	5.13	6.71
0.15	4.34	6.83

Table 5.10: Change in charging energy with deviation and floating gate voltage. (floating gate at 20 nm distance from the plunger gate)

5.3 Observing Energy Band Symmetry

It is also important to observe if the introduction of floating gate is changing the band symmetry. So, first observations are made to see if the electrons are at the same energy level before the deviation and after the floating gate voltage is provided. Results show that, in all cases the electron is going to the lowest energy level in conduction band.

To understand if the symmetry is affected, the difference between the ground state and first excitation state is calculated. Table 5.11 shows how the difference between the ground state and first excitation state (Δe_g) is affected before and after the floating gate voltage is applied.

Figure 5.10 gives a clear idea that, the addition of floating gate doesn't affect the difference between the ground state and first excitation state (Δe_g) that much. Δe_g is almost $\approx$ 2 meV with a deviation below $\pm$10%.

5.4 Summary

The results are summarized below,

(i) Floating gate voltage can effectively compensate the deviations in the plunger gate voltage.

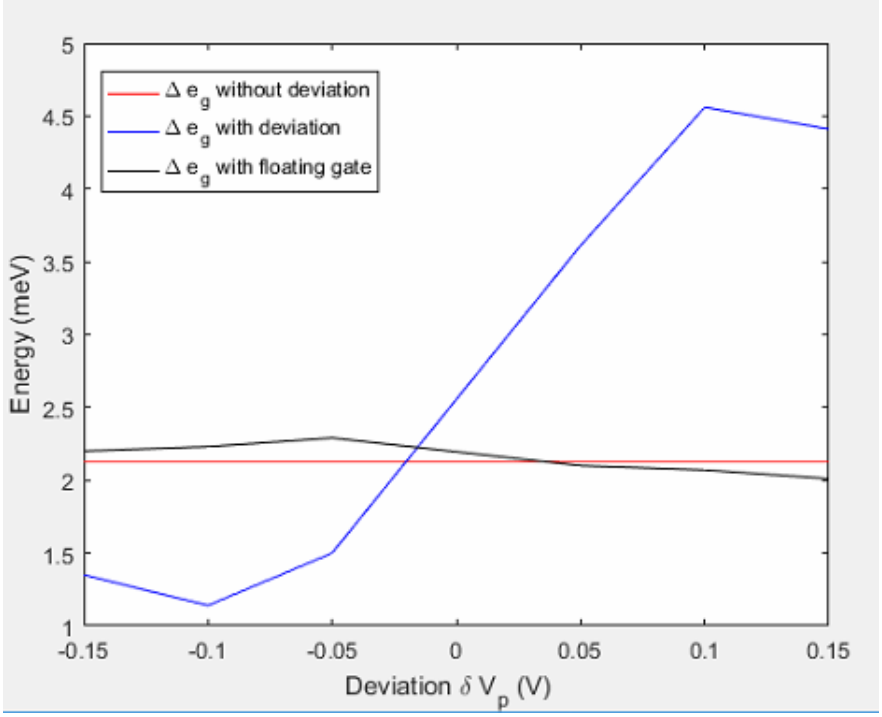


Figure 5.10: Δe_g changes by a lot due to added deviation and when the floating gate is added to regain the single electron region it regains the band symmetry as Δe_g is almost same as before any deviation was added with variations below $\pm 10\%$.

(ii) The distance between the floating gate and the plunger gate affects the performance of floating gate. Closer the floating gate better the control it has over the plunger gate deviation. With every 10 nm increase or decrease in distance between floating gate and plunger gate about 10% more or less voltage is required on the floating gate for same deviations respectively.

(iii) The size of floating gate also affects its performance. If the gate is made smaller in compared to the screening gate and device size, almost 1.5 times more voltage is required to get back to the single electron point.

(iv) When the size is reduced, the lateral position also plays an important role. If the gate is placed at the middle position rather than left or right, it shows better performance (1.5 times better performance).

(v) The charging energy is almost constant before the deviation is added and after the deviation is corrected by the floating gate with a variation below $\pm 10\%$.

Δe_g (Without deviation) meV	Deviation V	Δe_g (With deviation) meV	Δe_g (With floating gate) meV
2.13	0.05	1.35	2.20
2.13	0.1	1.14	2.23
2.13	0.15	1.5	2.29
2.13	-0.05	3.61	2.10
2.13	-0.1	4.56	2.07
2.13	-0.15	4.41	2.01

Table 5.11: Observing the change in Δe_g due to floating gate.

(vi) The electron is at the same energy level before the deviation and after the correction by floating gate.

Chapter 6

Conclusion and Future Work

The main focus of this thesis is to develop a scalable control circuit for silicon MOS quantum dot qubit network proposed in [29]. The control circuit is developed on the assumption that all the quantum dots are at the same potential, but this is not the case in practice. To solve this issue a device level floating gate concept is introduced to pre-tune all the quantum dots to the same potential.

In Chapter 3 the operation of the silicon MOS quantum dot qubit network is explained and the architecture of the designed control circuit is discussed. The circuit is designed to work at mK temperature. The main components of the circuit consist of a switching circuit, binary demultiplexer trees and clamper circuit/ bias tee. The control signals supplied to these circuits are designed to be supplied by shift resistors. These shift resistors are connected to the digital logic system at cryogenic temperature.

The control circuit architecture reported in chapter 3 is designed in TSMC 65 nm technology and design details are included in chapter 4. The transistor level design, sizing, and the performance of all these circuits are analyzed in this chapter. A chip layout is prepared to test the control circuit. The chip design is attached in Appendix A. The future target is to test this chip and analyzing its performance at mK temperature.

Chapter 4 introduces the idea of adding a floating gate to the silicon MOS quantum dot devices to pre-tune all the quantum dots in the network to same potential, so that all the global operations can work. By simulating the structure in nextnano software first the position and geometry of floating gate is finalized. It is observed that, the effectiveness of the floating gate increases as the distance between the floating gate and plunger gate of the device is reduced. With every 10 nm decrease in distance between floating gate and plunger gate about 10% less voltage is required on the floating gate to regain its initial

potential for same deviations added to the device. Again, if the floating gate size is made smaller than the device size the effectiveness of the gate is reduced. For example, if the gate is made one third of the screening gate and device size, almost 1.5 times more voltage is required to get back to the single electron point. After the geometry and distance between floating gate and plunger gate is fixed, its important to observe if addition of this floating gate to the device is affecting quantum dot properties. It is observed that, the charging energy is almost constant before the deviation is added and after the deviation is corrected by the floating gate with a variation below $\pm 10\%$. Moreover, the energy band symmetry is also restored after the correction by floating gate. The future target is to fabricate a silicon MOS quantum dot device with a floating gate and verify this concept practically.

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computing. In *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, pages 456–458. IEEE, 2019.

APPENDICES

Appendix A

Appendix

The chip submitted for fabrication has 3 parallel branches and some individual circuit for testing. First branch consists of a circuitry needed to control one node, one gate architecture. It has two demultiplexer trees, three cascaded switching circuits, clamper circuit and other gates like nor gate and inverters for expected operation explained in chapter 3, section 3.4. Figure A.1 shows the layout of branch 1.

The next branch has the same circuitry except the clamper circuit. This branch is made with a bias tee, so that if the clamper circuit doesn't work as expected we can test the functionality using bias tee. Figure A.2 shows the layout of branch 2.

The third branch is designed for a higher load. Sometimes due to chip packaging the load might be higher than expected. So, this branch is designed for 10 pf load while the other two branches are designed for 1 pf. Figure A.3 shows the layout of branch 3.

Some individual circuits like the switching circuit, bias tee and clamper circuits are designed to test individually to observe their performance at millikelvin temperature. Figure A.4 shows the layout of the individual circuits.

The post layout simulation of branch 1 is shown in Figure A.5 and A.6. Figure A.5 (a) shows the default cycle, where for a 100 mV, 1 GHz pulse the output is around 88 mV. The output DC level is at 1.3 V for an input biasing of 2 V. The drop in DC level is due to the 0.7 V drop across the diode in the clamper circuit. The delay between input and output is around 60 ps for 1 ns period of input pulse as shown in Figure A.5 (b) . The maximum power consumption by the branch is around 170 uW as shown in Figure A.5 (c). Figure A.6 (a) and (b) show the hole creation and sending correction pulse phenomenon for certain period.

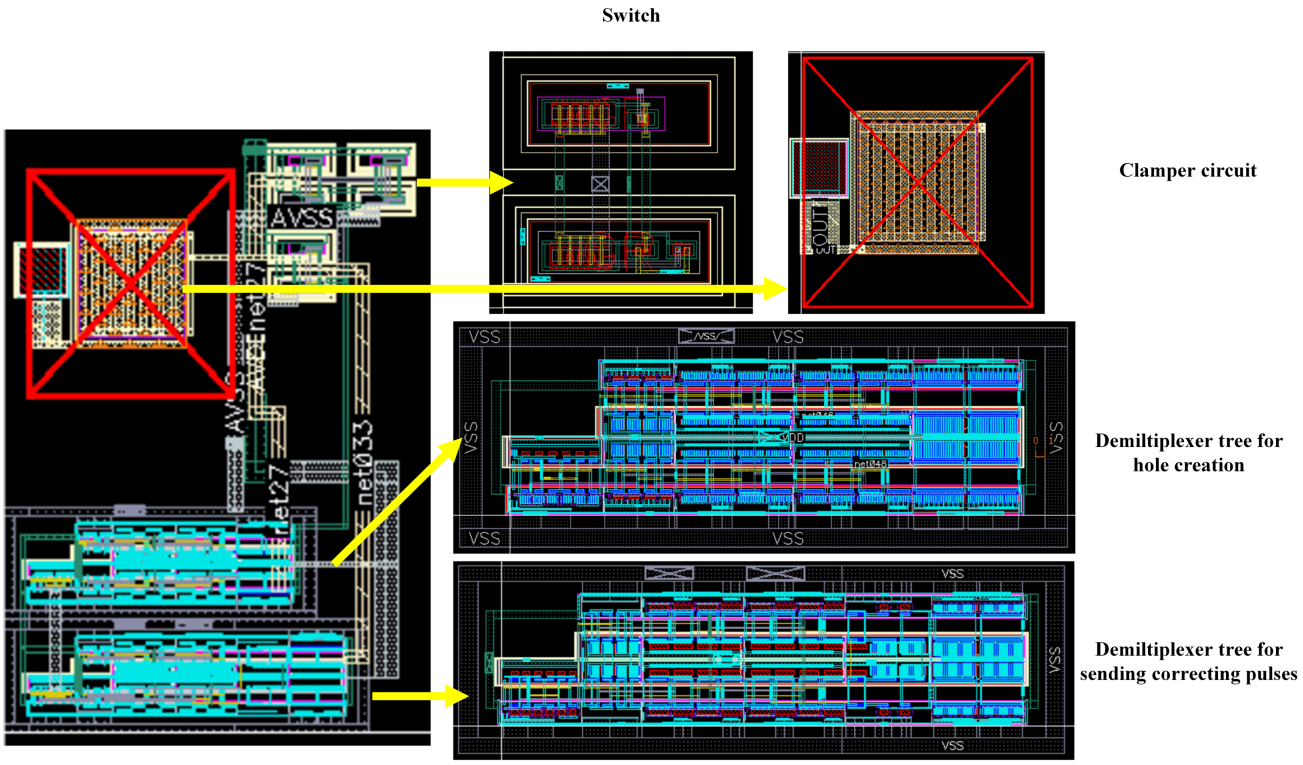


Figure A.1: Layout of branch 1 with two demultiplexer tree, three switches, clamper circuit and other gates like nor gate and inverter to support the operations.

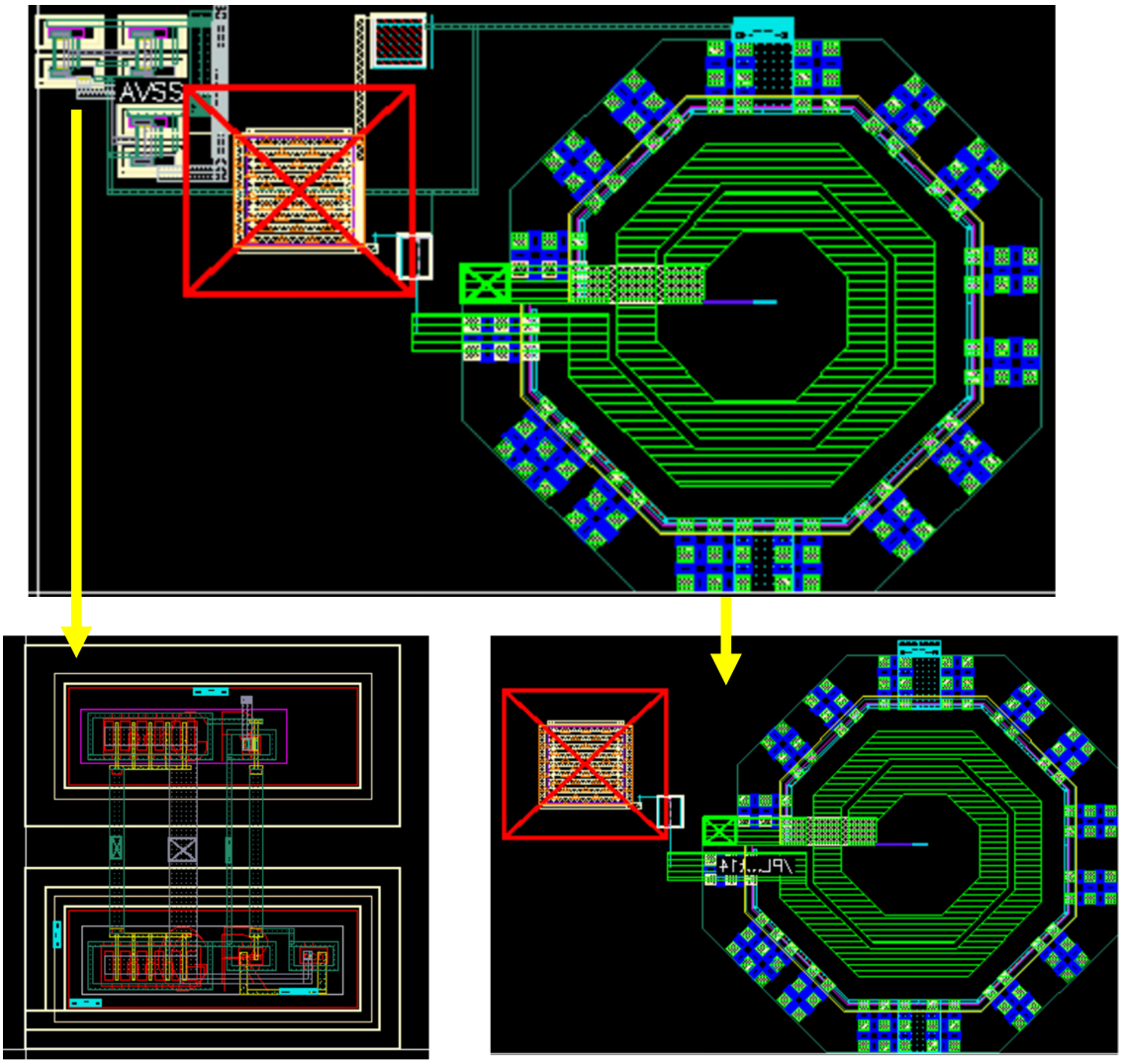


Figure A.2: Layout of branch 2 with three switches, clamper circuit and other gates like nor gate and inverter to support the operations. This branch shares the demultiplexing tree with branch one.

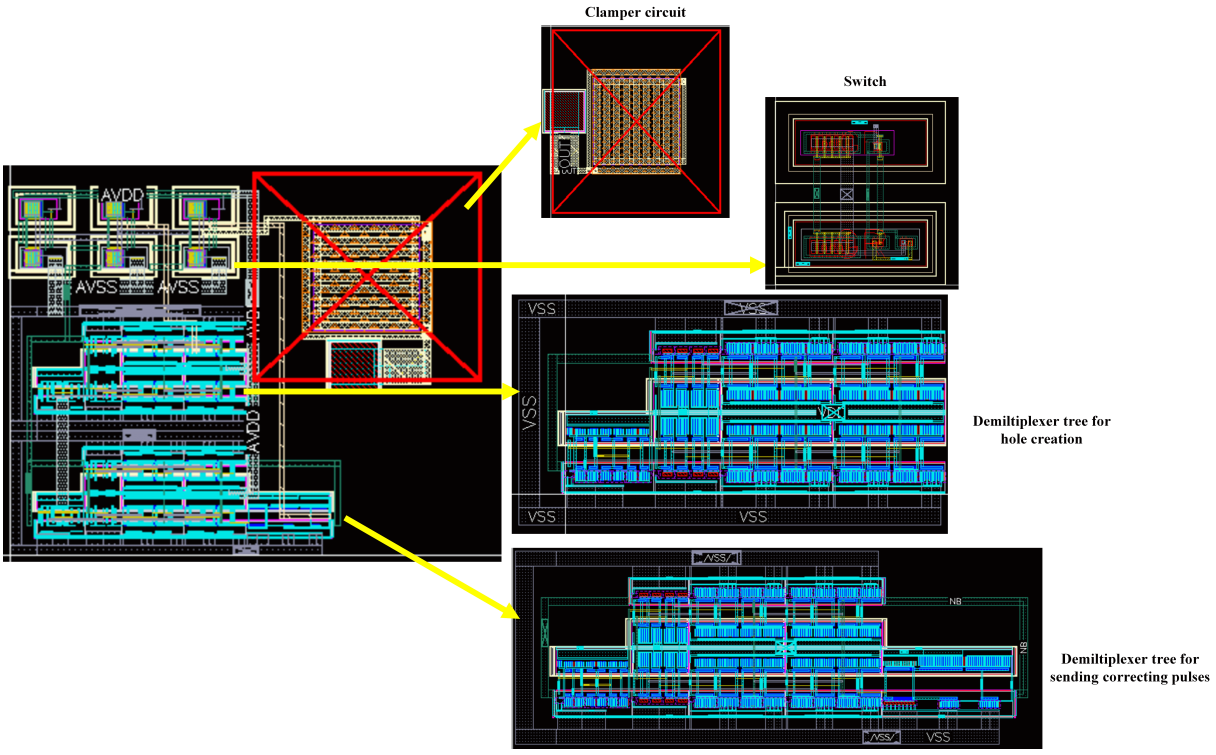


Figure A.3: Layout of branch 3 with two demultiplexer tree, three switches, clamper circuit and other gates like nor gate and inverter to support the operations.

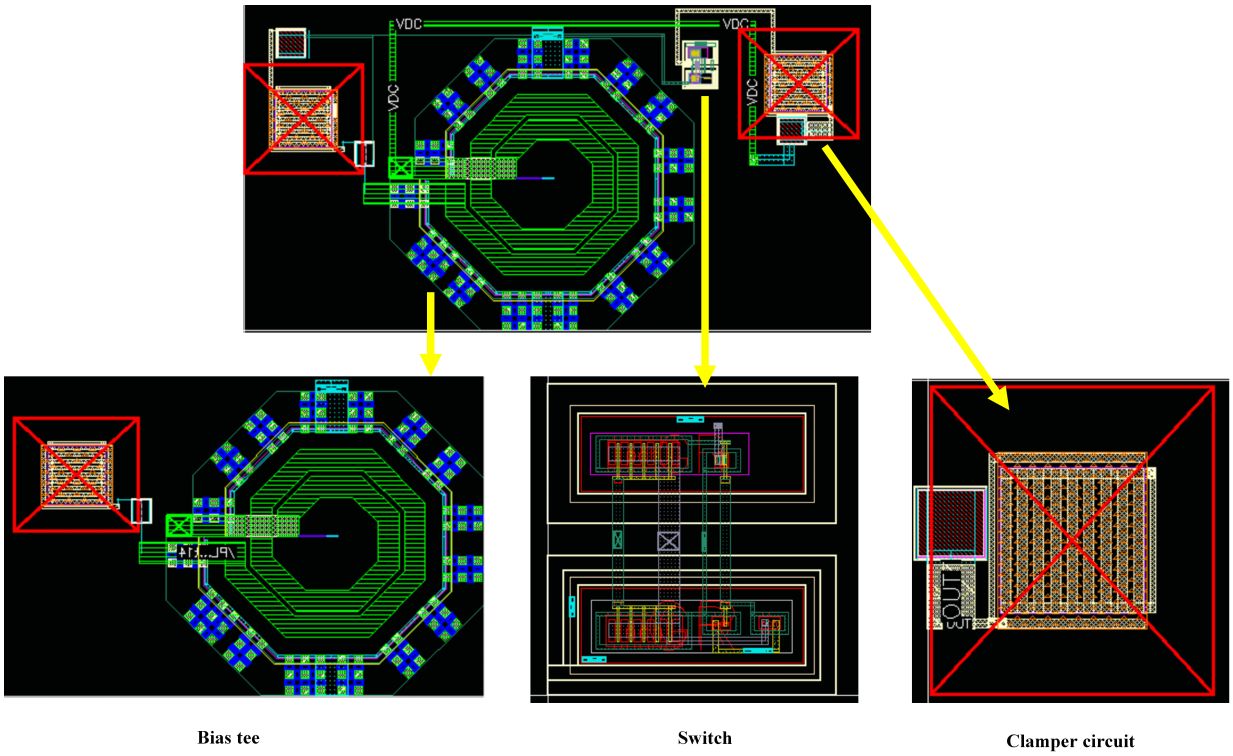
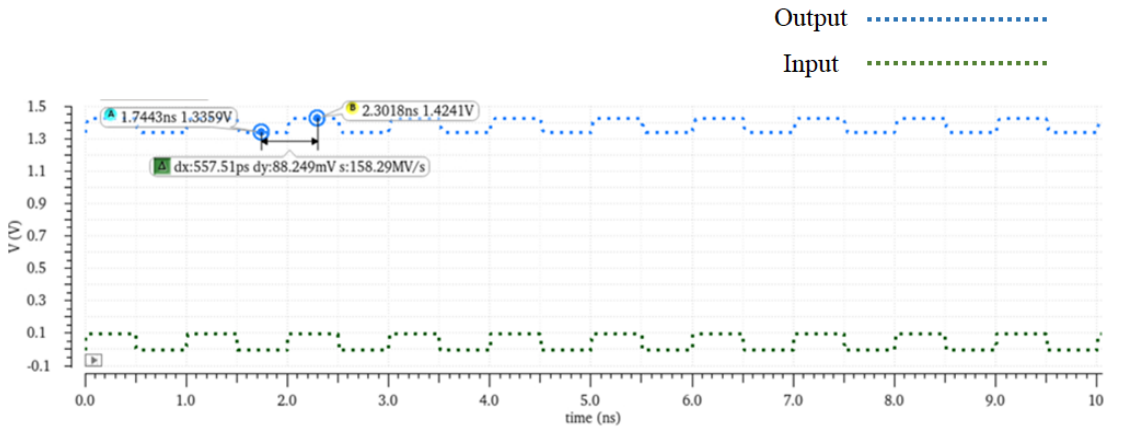
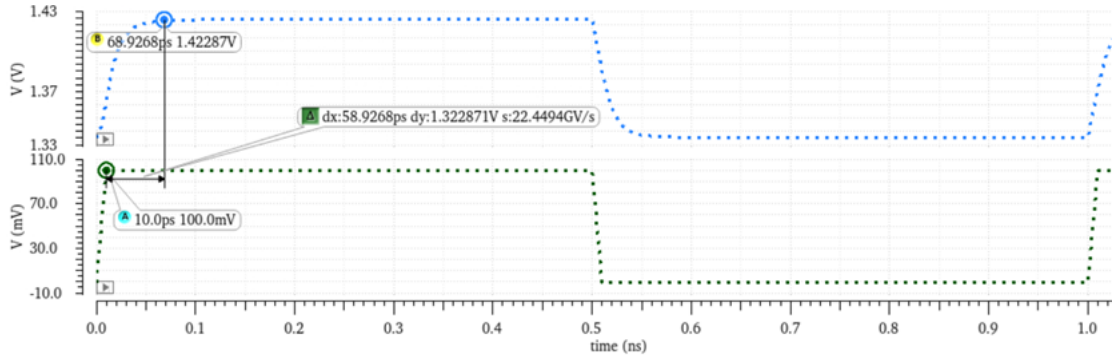


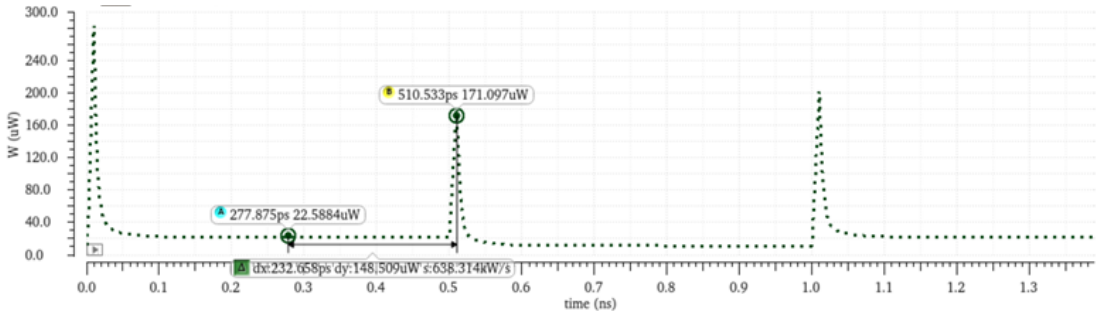
Figure A.4: Layout for testing some individual circuits like bias tee, switch and clamper circuit.



(a)

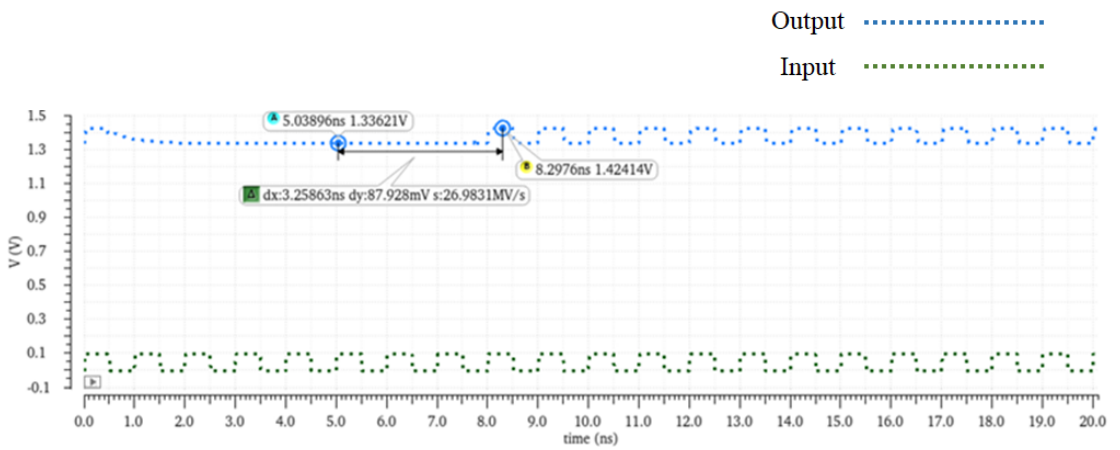


(b)

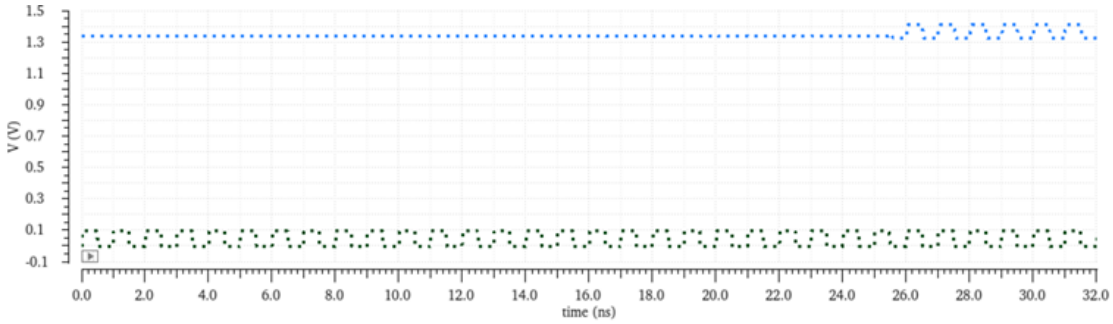


(c)

Figure A.5: (a) Input and output for 100 mV pulse with 1 ns period in default cycle for branch 1, (b) Delay between input and output signals, (c) Total power consumed by branch 1.



(a)



(b)

Figure A.6: (a) Hole created for 8 ns, (b) Correction pulse sent for 6 ns. (branch 1)