Theoretical Investigation of Contact Effects on the Performance of 2D-Material Nanotransistors

by

Demin Yin

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Examining Committee Membership

The following served on the Examining Committee for this thesis. The decision of the Examining Committee is by majority vote.

External Examiner: Hyunhyub Ko

Professor, School of Energy and Chemical Engineering, Ulsan

National Institute of Science and Technology (UNIST)

Supervisor: Youngki Yoon

Associate Professor, Dept. of Electrical and Computer Engineering,

University of Waterloo

Internal Member: Dayan Ban

Professor, Dept. of Electrical and Computer Engineering, University

of Waterloo

Internal Member: Guoxing Miao

Associate Professor, Dept. of Electrical and Computer Engineering,

Institute for Quantum Computing, University of Waterloo

Internal-external Member: Vivek Maheshwari

Associate Professor, Dept. of Chemistry, University of Waterloo

AUTHOR'S DECLARATION

This thesis consists of material all of which I authored or co-authored: see Statement of Contributions included in the thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Statement of Contributions

The following publications and preprints, of which I am the primary author, have been adapted into material for Chapters 3, 4, and 5 respectively of this thesis:

- D. Yin, A. AlMutairi, and Y. Yoon, "Assessment of High-Frequency Performance Limit of Black Phosphorus Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2984–2991, 2017, doi: 10.1109/TED.2017.2699969.
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Professor Sunkook Kim's group (Sooho Choo), Professor Woong Choi, and Professor Hyuk-Jun Kwon carried out the lab experiments, collected and analyzed the experimental data, and assisted with the writing of Section 4.3.5 and 4.3.6.

Abstract

Two-dimensional (2D) materials have attracted significant attention for electronic device applications since the first graphene transistor was demonstrated in 2004. Various 2D materials not only exhibit excellent carrier mobility and suitable bandgap, but also provide great opportunities for flexible and transparent device applications. However, the fabrication of high-performance 2D transistors is limited by various factors, such as unintentional doping, defects, and poor contact properties. In this study, some of the promising 2D materials, such as black phosphorus (BP) and molybdenum disulfide (MoS₂), and their electronic devices are studied. In particular, the contact effects on the performance of 2D material nanoscale transistors are explored by means of theory. Simulation methods for ohmic and Schottky contact in 2D-material field-effect transistors (FETs) are discussed in detail. Simulation settings in non-equilibrium Green's function (NEGF) and boundary conditions in Poisson's equation are specified. A quantum transport simulator is built to explore the performance of those devices with different types of contacts.

First, the effects of contact resistance (R_c) on the high-frequency performance limit of BP FETs are studied using self-consistent quantum simulations. A detailed comparison between intrinsic and extrinsic cut-off frequency (f_T) and unity power gain frequency (f_{max}) is made. Unlike zero-bandgap graphene devices, semiconducting BP FETs exhibit clear saturation behaviors, which is critical for high f_{max} . It is shown that near THz frequency range of f_T and f_{max} are highly promising for high-frequency applications, which is possible with an aggressive channel length scaling ($L_{ch} \approx 10$ nm) along with state-of-the-art fabrication techniques for low R_c . Our benchmarking against the experimental data indicates that there still exists large room for optimization of R_c .

Based on the recent temperature studies of 2D-material FETs, two different trends can be observed. We propose a model based on the effective mass approximation to explain the low-temperature current-voltage measurements of multilayer MoS₂ thin-film-transistors (TFTs). Our model suggests that the different temperature responses with Schottky and ohmic contacts result from various aspects of contacts, such as Schottky barrier height and barrier thickness. We also investigated the distinct device-to-device low-temperature responses in multilayer MoS₂ TFTs. Our comprehensive study provides a systematic scheme for the analysis of the contact properties in 2D material-based FETs.

Recently two-dimensional transition metal dichalcogenides (TMDs) lateral heterojunction field-effect transistors (FETs) have been demonstrated experimentally, in which metallic TMDs were used

for the source/drain. We systematically investigate the contact property and device performance of monolayer 1T/1T'-2H MoS₂, MoSe₂, and MoTe₂ FETs. Schottky barrier (SB) heights are extracted from density functional theory calculations, and non-equilibrium Green's function (NEGF) transport simulations have been performed to study device characteristics. Our simulation results reveal that **ON** and **OFF**-state characteristics of these devices are limited due to the inherent Schottky barrier. We optimize the performance of TMD lateral heterojunction SBFETs by using two different approaches: improving the electrostatic control by scaling equivalent oxide thickness and gate underlap and by moderately doping the gate underlap region. Our comprehensive study reveals that 1T'-2H MoTe₂ SBFET shows the highest **ON** current (\sim 1 mA/ μ m) among the three with a reasonably small subthreshold swing (80 mV/dec) if properly scaled, while 1T-2H MoS₂ SBFET exhibits the highest I_{on}/I_{off} (\sim 10⁷) when Ohmic contact is established with moderate doping in the gate underlap region. This study not only provides physical insight into the electronic devices based on novel TMD heterostructures but also suggests engineering practice for device performance optimization in experiments.

We also investigate the geometric effect of contact in 2D heterojunctions. The electron transport through the interface has been simulated with the top-contact and side-contact 1T-2H MoS₂. We studied the five potential stacking modes in top-contact MoS₂ junctions. The accurate maximally localized wannier functions and Schottky barrier height in top and side contact junctions have been extracted for conductance calculation. The conductance comparison shows side contact is better than top contact in the 1T-2H MoS₂ heterojunction. The oscillations of conductance are observed with different 1T2H overlap lengths with a top contact. Also, it is compared with the strong conductance oscillation in the semiconducting mono-bi-monolayer black phosphorus (BP) heterojunctions. The current flow pattern of the 1T-2H MoS₂ junction shows that the majority of current transitions from 1T layer to 2H layer happen at the edge. We further modify the weak van der Waals interactions at the edge, suggesting a potential engineering method to achieve a better contact property in metal-semiconductor top-contact junctions. This study may help us better understand metal-semiconductor junctions in 2D materials.

Lastly, future works are suggested. The device simulations of top contact and side contact MoS₂ FETs are the next work to compare their device performance. There are huge numbers of novel systems in van der Waals 2D material heterojunctions. We can achieve tunneling FETs by engineering the band alignment between 2D materials with different bandgaps. In addition, with the developed simulator, vertical tunneling junctions can be investigated in layered 2D material systems.

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ABBREVIATIONS

2D Two-dimensional

TMD Transition metal dichalcogenides

BP Black phosphorus

FET Field-effect transistor

SBFET Schottky barrier field-effect transistor

CVD Chemical vapor deposition

RF Radio frequency

DOS Density of States

PDOS Projected density of states

SBH Schottky barrier height SBW

Schottky barrier width

MOS Metal-oxide-semiconductor

DFT Density functional theory

Local density approximation LDA

GGA Generalized gradient approximation

PBE Perdew-Burke-Ernzerhof

PAW Projector-augmented wave

EM Effective mass

TΒ Tight-binding

MLWF Maximally localized Wannier functions

LCAO Linear combination of atomic orbitals

NEGF Non-equilibrium Green's function

EOT Equivalent oxide thickness

SS Subthreshold slope

Chapter 1

Introduction

1.1 2D Materials

The experimental demonstration of single-layer graphene by Novoselov *et al.* in 2004 [1], has explored a new area of two-dimensional (2D) materials and their device applications. Since then, many other 2D materials, such as hexagonal-boron nitride (h-BN), transition metal dichalcogenides (TMDs), black phosphorus (BP), and complex oxides, have been grown or achieved by micromechanical exfoliation. In their bulk forms (i.e., with many layers), in-plane atoms are firmly packed by strong covalent bonds through valence electrons, while adjacent layers are held together by relatively weak van der Waals force. The atomic-scale thickness and the pristine interfaces lead to many interesting physics and novel applications in electronic devices.

The field-effect transistor (FET) is a building block of modern semiconductor electronics. 2D materials have drawn significant attention for the active channel material in FETs. Notably, the International Technology Roadmap for Semiconductors (ITRS) 2011 considered graphene as a candidate for future electronics [2]. In the following sections, the emerging 2D materials will be briefly reviewed.

1.1.1 Semi-metallic Graphene and Metallic 1T/1T' TMDs

Graphene is the monolayer form of bulk graphite, with carbon atoms arranged in a 2D honeycomb lattice, as shown in Figure 1.1. The first demonstrated graphene was achieved from graphite using sticky tape [1]. Although the quality of graphene obtained by mechanical exfoliation is good, which is confirmed by the observation of the room-temperature quantum Hall effect [3]. It suffers from the low yield and the small size of the samples. Graphene with a larger surface area can be achieved by chemical methods, with the reduction of graphene oxide. Nowadays, high-quality, large-scale graphene can be obtained by the chemical vapor deposition (CVD) method [4], [5].



Figure 1.1 Atomistic structure of monolayer graphene [6].

Graphene shows extremely high mobility up to $40,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and high thermal conductivity [7], [8]. These suggest the great potential of graphene as a novel material for next-generation electronic devices. However, graphene suffers from zero bandgaps, which leads to small $I_{\text{on}}/I_{\text{off}}$, limiting its application. However, as a large ON-OFF ratio is not required for radio frequency (RF) applications, the ultra-high mobility and atomic thickness make graphene suitable for RF applications. High cut-off frequency (f_{T}) up to a few hundred gigahertz can be achieved due to high mobility [9], [10], but the highest reported unity power gain frequency (f_{max}) is around 50 GHz due to a zero bandgap [11].

The semi-metallic property of graphene comes from its unique band structure. At K point, the conduction band bottom meets the valance band top, forming cone-shaped band structures. To investigate the semi-metallic graphene, we will start from its atomistic structure. The schematic unit cell of graphene is shown in Fig 1.2. There are two atoms (named A and B atoms, respectively) in one unit cell with around 1.42 Å bond length (a_{C-C}). The honeycomb lattice can be characterized by defining the primitive unit vectors of \mathbf{a}_1 and \mathbf{a}_2 as

$$\mathbf{a}_1 = \left(\frac{3}{2}a_{C-C}, \frac{\sqrt{3}}{2}a_{C-C}\right), \mathbf{a}_2 = \left(\frac{3}{2}a_{C-C}, -\frac{\sqrt{3}}{2}a_{C-C}\right)$$

And the vectors describing the separation between type A atoms to its nearest neighbor type B atoms are \mathbf{R}_1 , \mathbf{R}_2 , and \mathbf{R}_3 as,

$$\mathbf{R}_1 = (a_{C-C}, 0), \mathbf{R}_2 = \left(-\frac{1}{2}a_{C-C}, \frac{\sqrt{3}}{2}a_{C-C}\right), \mathbf{R}_3 = \left(-\frac{1}{2}a_{C-C}, -\frac{\sqrt{3}}{2}a_{C-C}\right)$$

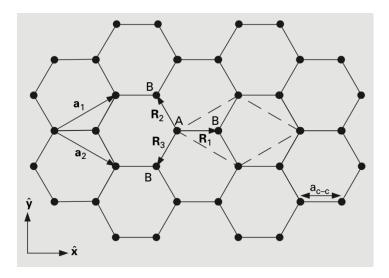


Figure 1.2 The honeycomb lattice of graphene and its primitive unit cell [12].

For the nearest tight-binding approximation, the hopping parameter is $t_0 = -3$ eV, which only happens between two neighboring carbon atoms. Then, the Hamiltonian matrix of graphene can be written as

$$H = \begin{bmatrix} 0 & t_0 \\ t_0 & 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ t_0 & 0 \end{bmatrix} e^{i\mathbf{a_1}\cdot\mathbf{k}} + \begin{bmatrix} 0 & 0 \\ t_0 & 0 \end{bmatrix} e^{i\mathbf{a_2}\cdot\mathbf{k}} + \left\{ \begin{bmatrix} 0 & 0 \\ t_0 & 0 \end{bmatrix} e^{i\mathbf{a_1}\cdot\mathbf{k}} + \begin{bmatrix} 0 & 0 \\ t_0 & 0 \end{bmatrix} e^{i\mathbf{a_2}\cdot\mathbf{k}} \right\}^{\dagger}$$

In this way, we can plot the band structure of graphene, as shown in Fig. 1.3. The band structure of graphene near the K points can be regarded as a linear dispersion. It leads to massless particles, which is of great interest in condensed matter physics. The six **K**-points where conduction and valence bands meet are also called Dirac points. The linear energy dispersion near **K**-points also leads to ultra-high Fermi velocity. For 2D materials with parabolic band shape, the density of states (DOS) is approximately constant. For graphene with a linear *E-k* relation, it exhibits a linear DOS near the **K** points. The reason why graphene is considered a semi-metal is that the DOS vanishes to zero even though there is no bandgap, in contrast to regular metals with large DOS at the Fermi level.

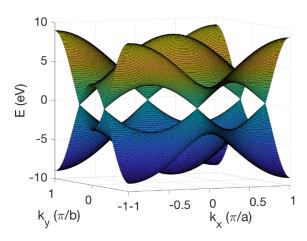


Figure 1.3 Band structure of graphene in normalized reciprocal lattice. The two surfaces denote the conduction band bottom and valence band top of graphene.

There are several ways to open the band gap of graphene for digital applications; for example, tailoring graphene into graphene nanoribbons, or applying a strong vertical electric field across multilayer graphene, and applying strains in graphene. However, they all suffer from significant mobility degradation once the bandgap is introduced.

TMDs have attracted extensive attention due to their broad potential applications [13], [14]. TMDs exhibit various crystal structures with unique properties[15]–[19]. Based on the atomic structure and symmetry, TMDs can be classified into two categories: H-phases and T- (or T'-) phases. The top view and side view of the 2H, 1T, and 1T' phase of MoSe₂ is shown in Figure 1.4. The H-phase TMDs are semiconducting in general and have been widely studied, especially in electronics applications. The T-phase TMDs generally show metallic properties, which show great potential in energy-related applications and electrochemical reactions. Figure 1.5 shows the density of state (DOS) of graphene and 1T MoS₂. Both graphene and 1T MoS₂ are zero bandgap materials. However, graphene demonstrates zero DOS at the Fermi level E_f, whereas 1T MoS₂ has non-zero DOS at E_f. In this way, graphene is considered a semi-metallic material, and 1T TMDs are considered as a metallic material. The T-phase TMDs can be synthesized directly in certain growth conditions, or they can be transferred from H-phase TMDs by phase-engineering.

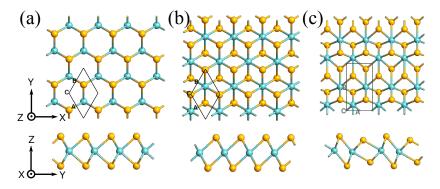


Figure 1.4.Top (top) and side view (bottom) of the atomistic structure of (a) 2H, (b) 1T, and (c) 1T' monolayer MoSe₂. MoS₂ and MoTe₂ have similar atomistic structures with different cell sizes. The primitive cells of 2H, 1T and 1T' structures are shown in the top view.

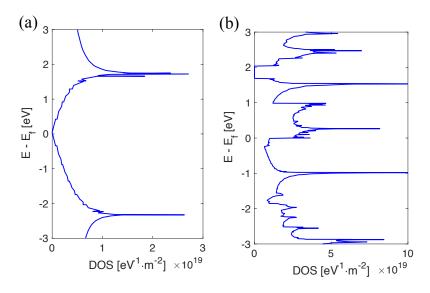


Figure 1.5 Density of States (DOS) of (a) semi-metallic graphene (b) metallic 1T MoS₂.

1.1.2 Semiconducting BP and TMDs

For digital applications, in general, the bandgap is critical. Therefore, semiconducting 2D material with a finite bandgap along with high mobility would be highly desired. Group-VIB transition metal dichalcogenides (TMDs) MX_2 (M = Mo, W; X = S, Se, Te) have attracted significant attention due to their extraordinary electronic and optical properties. Monolayer TMDs exhibit a direct bandgap in the visible frequency range and excellent mobility (around 200 cm² V⁻¹ s⁻¹ [20]) at room temperature, making them promising candidates for electronic and optoelectronic devices.

The synthesis of the monolayer to few-layer TMDs has been following graphene practice, as bulk TMD materials have a similar layered structure as graphite. Mechanical/chemical exfoliation and chemical vapor deposition (CVD) growth are the two primary TMDs' synthesis methods. In general, the exfoliation

method is favorable for less-defect, high-quality MX_2 films, while the CVD method is favorable for the growth of large-area (up to wafer-scale) MX_2 films. For instance, large single-crystal MoS₂ domain (>100 μ m) and large-area films can be grown on SiO₂ substrates using solid-phase sulfurization of MoO₃, MoCl₅, or Mo thin films [21]–[23]. The quality of CVD synthesized MoS₂ is comparable to those of the exfoliated MoS₂ films within one domain [23]. However, large-area MoS₂ films synthesized by CVD suffer from a large number of grain boundaries, which can significantly degrade the electrical properties [21]–[23]. Hence, the device properties of MoS₂ electronics can benefit by reducing grain boundaries in the CVD-grown thin films.

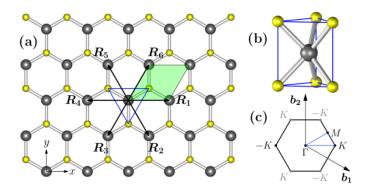


Figure 1.6 (a) Top view of monolayer MX_2 . (b) Schematic of unit cell structure in trigonal prismatic coordination. (c) The 2D first Brillouin zone of MX_2 [24].

The structure of 2H-phase MX_2 monolayers is similar to that of graphene from the top view. Each unit cell consists of one M atom sandwiched by two X atoms, forming a trigonal prismatic structure, as shown in Figure 1.6(a) and (b) in the ball and sticks model. The large grey ball is for M, and the small yellow ball for X. R_1 through R_6 shows the nearest neighbors. The shape of the 2D unit cell is shown in the shadowed green diamond region with a lattice constant a. The three-dimensional schematic of the trigonal prismatic unit cell is shown in Figure 1.6(b). As we can see here, each X atom is shared by its neighbors. MX_2 also demonstrates a hexagonal first Brillouin zone with a near honeycomb atomic structure as shown in Figure 1.6(c). The b_1 and b_2 are the reciprocal basis vectors. Two inequivalent valleys K and K are shown.

Black phosphorus (BP) is a stable allotrope of the phosphorus element in a layered form. Few layers BP has attracted lots of attention due to its moderate band gap as well as intriguing electrical properties. The layers of BP are also weakly bonded through van der Waals force. The in-plane phosphorus atoms are strongly bonded like the carbon atoms in graphite. However, unlike graphene, the in-plane phosphorus atoms are arranged in a puckered honeycomb lattice. This opens the bandgap, which is critical for digital device applications. Few-layer BP can be achieved by mechanical exfoliation. Recent theoretical studies have predicted that monolayer BP can exhibit extremely high hole mobility (10,000 cm² V⁻¹s⁻¹) [25]. The

experiment has demonstrated over 1,000 cm² V⁻¹s⁻¹ high field-effect mobility [26]. Theoretical studies have predicted the bandgap can be tuned by changing the number of layers. The bandgap decreases gradually from 2.0 eV in its monolayer form to 0.3 eV in bulk [27], [28]. The wide tuning range of BP makes it favorable for optical device applications.

At this moment, the main focus of the experiment is given to the synthesis of bulk BP rather than thin film at a wafer-scale [29]. Few layer BP are obtained through mechanical or chemical exfoliation from bulk BP. Although bulk crystals of BP are proven stable for more than several months, few-layer BP is found to be unstable in the presence of moisture and oxygen in the air [30]. However, few-layer BP can be stable for at least a few weeks after being encapsulated by Al₂O₃ over-layers under an ambient environment [31]. Similarly, poly(methyl methacrylate) (PMMA) coating [32], graphene, and hBN encapsulation [33] have also proven to be effective. Overall, few-layer BP does not have serious issues in stability if effective passivation methods are used, although few-layer BP is not as stable as graphene or TMDs.

The atomic structure of a few-layer BP is achieved by relaxing bulk BP [25]. The structure changes slightly from the bulk to the monolayer form. The top view and side view of the atomic structure of monolayer BP and bilayer BP are shown in Figure 1.7 (a), (c), and (d), respectively. Unlike graphene, the shape of the unit cell of BP is rectangular, as shown in Figure 1.7, which is partly due to the fact that the phosphorus atoms are not located on the same surface. The Brillouin zone of monolayer BP is rectangular, as shown in Figure 1.7(b). From monolayer to the bilayer, the value of *a* decreases abruptly by 0.06 Å, while it changes gently from bilayer to bulk BP. The value of *b* increases gently as the number of layers increases. The interlayer spacing is almost constant, with around 3.20 Å regardless of the thickness of BP.

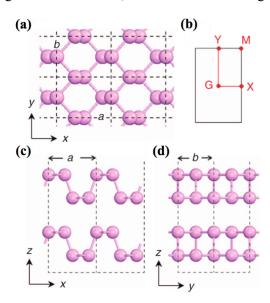


Figure 1.7(a) Top view of the atomic structure of monolayer BP. (b) Brillouin zone of monolayer BP. (c) (d) Side views of the atomic structure of bilayer BP [25].

Table 1.1 Structural information for few-layer BP [25].

N_L	1	2	3	4	5	Bulk
a <i>(Å)</i>	4.58	4.52	4.51	4.50	4.49	4.47
b <i>(Å)</i>	3.32	3.33	3.33	3.34	3.34	3.34

Unlike TMDs, monolayer and bilayer BP exhibit strong anisotropic electron and hole effective mass. The hole effective mass of BP along the zigzag direction is more than six times larger than that along the armchair direction. The extracted electron and hole effective mass of monolayer and bilayer BP along armchair (*x*-) direction and zigzag (*y*-) direction are shown in Table 1.2. The strong anisotropic properties of 2D materials can be applied to novel electronic, thermoelectric, and optoelectronic device applications.

Table 1.2 Effective mass of monolayer and bilayer BP extracted from tight-binding band structure. Subscripts "e" and "h" denote "electron" and "hole", and subscripts "x" and "y" denote for armchair and zigzag directions.

	m _{ex} /m ₀	m _{ey} /m ₀	m _{hx} /m ₀	m _{hy} /m ₀
Monolayer	0.17	0.87	0.19	1.17
Bilayer	0.18	1.13	0.20	0.78

1.1.3 Insulating h-BN

Boron nitride (BN) is a conventional material with superior thermal and chemical stability. BN exists in various forms, which are similar to structured carbon lattices. The hexagonal form (h-BN) corresponds to the graphite lattice structure, and the cubic (sphalerite structure) form corresponds to the diamond lattice structure. Even in layered h-BN bulk, due to the highly polar B-N bonds, various stacking modes exist [34], [35]. Unlike conductive graphite, h-BN exhibits unique electronic properties with a wide bandgap, low dielectric constant, high thermal conductivity, and chemical inertness.

Monolayer h-BN has a structure similar to graphene, with alternating boron and nitrogen atoms arranged in the honeycomb lattice structure. In-plane B-N atoms are bonded by sp² covalent bonds similar to graphene, while the interlayers are held together by weak van der Waals force. In spite of a large number of studies and its seemingly simple crystal structure, the very basic band gap remains controversial due to the inconsistent values reported experimentally and theoretically. Early experiments suggested h-BN as a direct band gap material with around 6.0 eV band gap [35], [36], while *ab-initio* calculations claimed that h-BN is an indirect bandgap crystal [34], [37]. The inconsistencies between experiments and simulations can be ascribed to the impurity and defects of h-BN samples. The early obtained h-BN crystalline samples

may actually be a mixture of different stackings. Recent simulations on h-BN with various polytypes showed that, with different stacking modes, h-BN exhibits different band structures [34], [38]. The band gap can be indirect, quasi-direct, or direct, and the values vary from 3.27 eV to 5.98 eV. A recent experiment also supports the indirect band gap of 5.96 eV by using high-purity crystals [39]. The phonon-assisted two-photon absorption suggests an exciton binding energy about 130 meV, and supports the indirection band gap in h-BN, showing a good matching to the simulation results.

The h-BN thin films can be obtained through a top-down or bottom-up approach [40]. The top-down approach is by mechanical or chemical exfoliation from bulk h-BN, and this method is simple. High-quality flakes can be obtained, although the limited size hiders the applications in large-area devices. On the other hand, the bottom-up approach is by CVD growth. Wafer-size high-quality thin film can be obtained, while it needs unconventional boron-containing precursors. Nevertheless, growth control of high-quality few-layer h-BN is still challenging.

Various forms of BN have been used for lubricant and abrasive material for a long time, and the unique electronic properties of BN have now been utilized and attract lots of attention. The h-BN is considered a promising candidate for optoelectronic and high-power electronic devices. Due to the wide band gap, hBN based devices can operate in the deep-ultraviolet range. Few layer h-BN films can play an important role in novel 2D electronics. The high electrical resistivity, low dielectric constant, and structural and mechanical similarity to graphite make h-BN a good candidate for dielectric layer and insulating substrates for many 2D material devices. Various groups have demonstrated with experiments that the device performance of graphene FETs can be significantly boosted by replacing conventional SiO₂ support and dielectric layer with h-BN thin films. Wang et al. showed that, by encapsulating graphene with h-BN, the remarkably low contact resistance is achieved by edge contact, and ultra-high mobility up to 140,000 cm² V⁻¹s⁻¹ has been observed [41]. Similarly, the device performance of single-layer WS₂ FET has been improved by employing h-BN thin films as a substrate and the capping layer, with up to 214 cm² V⁻¹s⁻¹ high field-effect mobility at room temperature and ON/OFF ratio as high as 10⁷ [42]. By integrating h-BN with other 2D materials, heterostructures can be achieved to realize novel devices. The rich physics in the graphene/h-BN van der Waals vertical heterostructure may lead to novel electronic and optoelectronic devices [43]-[45]. Based on a WS₂/h-BN/graphene/SiO₂ van der Waals heterostructure, Qiu et al. demonstrated non-volatile memory devices [46]. In this device, WS₂ is used as a FET channel, h-BN serves as a tunnel barrier, and graphene acts as an electron confining layer. It should be noticed that research of h-BN for electronic applications is still in its very early stage, and rapid progress is expected in the near future.

1.2 Effect of Contact Resistance

The electronic properties of semiconductors play a primary role in determining the device performance, yet metal-semiconductor junction is comparably important. As the size of the device shrinks to the nanoscale, the effect of contact resistance becomes more dominant. Generally, a high electrical resistance is due to the large Schottky barrier at the metal-semiconductor interface. This hinders the injection/ejection of charge carriers to/from the channel and consequently degrades the overall device performance. Here we will focus on the effect of contact resistance on two different electronic devices: digital and analog applications.

In digital applications, transistors switch between ON and OFF states. Ideally, low I_{off} and high I_{on}/I_{off} are desired for low standby power consumption, and high I_{on} is desired for fast switching speed. However, large contact resistance will significantly limit I_{on} . As the intrinsic delay, which determines device speed, can be approximately evaluated by $\tau = CV_{DD}/I_{on}$, where V_{DD} is the power supply voltage and C is the gate capacitance of the transistor, the device gets slower with large contact resistance (R_c) . Assuming the clock frequency $f \sim 1/\tau$, large R_c will also result in larger dynamic power consumption as $P_D \sim fCV_{DD}^2$. For analog applications, the parasitic resistance significantly reduces the cutoff frequency (f_T) and the unity power gain frequency (f_{max}) , as $f_T = \frac{g_m}{2\pi\{C_{gg,t}[1+g_d(R_S+R_D)]+C_{gd,t}g_m(R_S+R_D)\}}$, where g_m is the transconductance, and $C_{gg,t}$ is the total gate capacitance. Details of the effect of contact resistance on radiofrequency applications will be discussed in a later chapter.

The quantum limit of the contact resistance is predicted by $R_c \sim h/(2e^2M)$, where h is Planck's constant, e is the element electron charge, and M is the number of electron modes whose wavelength fits the conductor. This means that the minimum contact resistance exits even in ballistic transport, and only certain electron modes that fit can be injected into the channel, while the rest will be reflected [47], [48]. Considering $M \sim k_F W$, where W is the width of the channel and k_F is the Fermi wave vector, as k_F increases, the density of electrons in 2D channel $n_{2D} = k_F^2/2\pi$ increases, and more modes M fit the channel. Thus, the minimum contact resistance can be calculated as $R_c W \sim \frac{h}{2e^2k_F} \sim \frac{0.026}{\sqrt{n_{2D}}} k\Omega$ µm. Normally the electron density of semiconductor is in the unit of 10^{13} cm⁻², which gives a minimum $R_c W \sim 30 \Omega$ µm. This is far less than that of usual experimental results, indicating there is plenty of room for improvement.

1.3 Towards Ohmic Contact 2D FETs

1.3.1 Challenges to Achieve Practical Ohmic Contacts

The metal-semiconductor junction can play a critical role in determining the device's performance. In general, the quality of contact is evaluated by contact resistance. For conventional 3D materials like Si and

Ge, low contact resistance can be achieved by using highly transparent tunneling contacts through heavy doping of the semiconductor in the contact region. However, there are several major issues for metal contact with 2D material. Unlike the conventional metal-semiconductor junctions, the thickness of 2D material is thinner than the depletion and transfer lengths. Due to the ultrathin thickness, the commonly adopted heavy doping in the contact region is not applicable; it would also modify the structure and property of 2D material. The interface between the 2D semiconductor and 3D metal normally leads to large contact resistance, which drastically restrains the drain current. In addition, the advantage of free dangling bonds of the 2D material surface becomes a disadvantage when it comes to forming a strong bond with the metal.

The presence of a significant Schottky barrier has been a major issue for many cases [49]–[51]. It is straightforward to choose contact metal with large (for p-type semiconductors) or small (for n-type semiconductors) work functions to achieve a small Schottky barrier, which has also been proven to be effective. Nonetheless, it is not a perfect approach due to the following reasons: (i) It is challenging to find a metal with a proper work function that exhibits high conductivity, high chemical, thermal and electrical stability. (ii) TMDs and BP exhibit thickness-dependent band gap, and BP also shows a strong anisotropic band structure, thus contact resistance cannot be easily predicted. (iii) The 2D semiconductor-metal interface could also be impacted by Fermi level pinning, proven by both experiment and theory [51]–[53].

Many recent experimental works have demonstrated progress in improving contact properties. The approaches include the use of small work function metals, graphene, or doped TMDs as electrodes, thermal annealing, ionic-liquid doping of contact regions, phase-engineering, selective etching, and thin tunnel barriers. Unfortunately, some methods suffer from poor air, thermal or long-term stability. The effective methods towards practical thermal and long-term stable ohmic contacts can be generally classified into two types: reducing the Schottky barrier height (SBH) and thinning the Schottky barrier width (SBW).

1.3.2 Reducing Schottky Barrier

Various methods have been realized to achieve ohmic contact by reducing SBH, which can be generally categorized as selective metal contact, graphene contact, and thin layer tunneling contact. Das *et al.* demonstrate that the metal-to-MoS₂ interface is strongly impacted by Fermi level pinning close to the conduction band, and low work function metals like Sc can significantly reduce contact resistance [54]. Based on the standard electron affinity of MoS₂ and the work function of the corresponding metal, the band diagram should be the same as Figure 1.8(a). Thus, electron current is expected by Sc and Ti contacts, and hole current is expected by Ni and Pt contacts with MoS₂ FETs, as shown in Figure 1.8(b). However, experimental results tell a different story. The transfer characteristics of back-gated MoS₂ FETs with Sc, Ti, Ni, and Pt metal contacts with threshold voltage shift are shown in Figure 1.8(c). All these FETs exhibit n-type characteristics, which indicate the Fermi levels of Sc, Ti, Ni, and Pt metals are lined up closed to the

conduction band of MoS_2 , as shown in the insert figure in Figure 1.8(c). We notice a clear on-state current degradation as higher work function metal is used. The extracted Schottky barrier heights are shown in Figure 1.8(d). The extracted $d\Phi_{SB}/d\Phi_{M}$ is around 0.1, indicates a strong pinning effect at the metal- MoS_2 interface. It also explains why most metal contact MoS_2 transistors exhibit n-type characteristics.

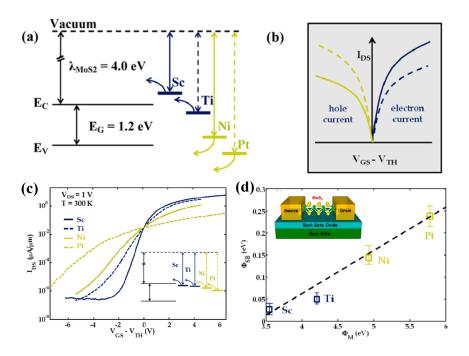


Figure 1.8 (a) Expected line-up of various metal Fermi levels with the conduction band (E_C) and valence band (E_V) of MoS₂-metal contact. (b) Expected transfer characteristics based on (a). (c) Transfer characteristics of back-gated MoS₂ thin-film transistor with various contacts. The inset demonstrates the actual line-up of metal Fermi level with E_C and E_V of MoS₂. (d) Extracted Schottky barrier height for Sc, Ti, Ni, and Pt. The inset shows the device structure of the back gated MoS₂ transistor [54].

To overcome the limitation of metal contacts, graphene contacts have been introduced and proven to be effective [55]–[58]. Graphene is mechanically strong, flexible, and thermally stable, especially desirable for flexible electronics applications. More importantly, the Fermi level of graphene can be effectively tuned by gate control or chemical doping to minimize the SBH at the graphene/semiconductor interface [53], [59]. Yu *et al.* demonstrated that large-scale electronic systems based on graphene/ MoS₂ heterostructures could be grown by a CVD method, and high-performance transistors can be achieved with reliable ohmic contact where graphene is used as electrodes, and circuit interconnects. The comparison between graphene/MoS₂ heterojunction contact and traditional metal/MoS₂ junctions demonstrates over ten times larger current with graphene/MoS₂ heterojunction contact FETs. The extracted Schottky barrier height Φ_B as a function of gate bias V_{bg} for both devices is shown in Figure 1.9(c). The Φ_B of graphene/MoS₂ FETs decreases significantly from 110 to 0 meV with V_{bg} increased from 0 to 35 V. On the other hand, the Φ_B of metal/MoS₂ FETs

shows a weak dependence on the change of V_{bg} , varying from 50 to 40 meV with V_{bg} increasing from 0 to 80 V. For an ideal metal-semiconductor contact, Φ_B is determined by the metal work function (W_m) and the semiconductor's electron affinity (χ_s), with $\Phi_B = W_m - \chi_s$. In metal/MoS₂ FETs, the change in Φ_B is limited by the modulation of midgap interface states. However, W_m can be modulated as shown in Figure 1.9(d). Here, when V_{bg} is larger than 35 V, the Schottky barrier height becomes zero, and an ohmic contact is achieved. The work function of graphene is modulated by the electric field, which is consistent with previous works [53]. This study shows that graphene outperforms Ti to make contact with MoS₂, which can be achieved using electronic doping or chemical doping.

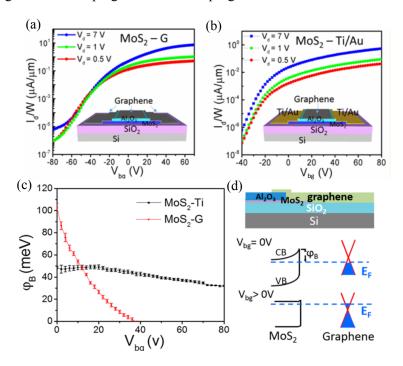


Figure 1.9 (a) Transfer characteristics of (a) back gated MoS_2 /graphene (MoS_2 -G) and (b) MoS_2 -Ti FETs at various V_D at room temperature. The insets are the device schematics, respectively. (c) Extracted barrier height as a function of back-gate bias for MoS_2 -G and MoS_2 -Ti FETs. (d) Upper panel: Experimental setup. Lower panel: schematic band diagram of MoS_2 -G FETs at $V_{bg} = 0$ and $V_{bg} > 0$ with corresponding E_F [57].

Chuang *et al.* report a new strategy to fabricate low contact resistance with TMD transistors using van der Waals assembly of substitutionally doped TMDs for source/drain [60]. The WSe₂ transistors with 2D/2D contacts have been demonstrated with a low contact resistance of ~0.3 k Ω μ m, high on/off ratios up to 10⁹, and high drive currents are exceeding 320 μ A μ m⁻¹. High field-effect mobility (μ FE) up to 200 cm² V⁻¹ s⁻¹ is achieved at room temperature, and up to 2000 cm² V⁻¹ s⁻¹ high μ FE can be achieved at cryogenic temperature. The 2D/2D contact is formed by the vertical junction between highly doped WSe₂ (Nb_{0.005}W_{0.995}Se₂) and intrinsic WSe₂. This method can also be applied to other TMDs, like MoS₂. In conventional metal/MoS₂ contacts, the hole injection has been obstructed by a large Schottky barrier.

However, the band offset in degenerately p-doped MoS_2 ($Nb_{0.005}Mo_{0.995}S_2$)/ intrinsic MoS_2 vertical junction can be tuned by the gate voltage, resulting in near barrier-free contact with low contact resistance. Furthermore, 2D/2D hetero contact is also investigated. Degenerately p-doped WSe_2 ($Nb_{0.005}Mo_{0.995}S_2$)/intrinsic $MoSe_2$ contact also shows a low ohmic contact resistance.

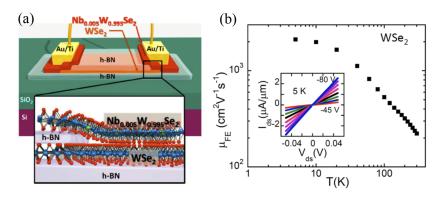


Figure 1.10 (a) Design and characteristics of WSe₂ FETs with 2D/2D source and drain contacts. The inset shows side view of degenerately p-doped WSe₂ (Nb_{0.005}W_{0.995}Se₂)/ intrinsic WSe₂ vertical hetero junction. (b) Two terminal field effect hole mobility of 2D/2D contact WSe₂ device at various temperatures [60].

It is much more challenging to achieve thin SBW by degenerately doping for 2D materials since ionized impurity doping would substantially damage the structural integrity of the atomically thin channel. Ionic liquid doping and gas doping have been developed to achieve ohmic contact with WSe₂ and MoS₂ FETs. Fang *et al.* demonstrated high-performance p-type field-effect transistors based on monolayer WSe₂ as an active channel with chemically doped source/drain (S/D) contacts combined with high- κ gate dielectrics [61]. The high hole field-effect mobility of ~250 cm² V⁻¹ s⁻¹ with an almost ideal subthreshold swing of ~60 mV/dec, and large I_{ON}/I_{OFF} up to 10⁶ at room temperature has been achieved. Low contact resistance is achieved for hole injection by using large work function Pd contacts by patterning NO₂ chemisorption on WSe₂. Although Pd was found to be the best contact for p-type WSe₂ FETs, a small Schottky barrier still exists at the Pd-WSe₂ interface. Heavily p-doped WSe₂ is achieved by surface NO₂ doping to reduce the barrier width at the metal-WSe₂ interface, inspired by a similar approach in carbon nanotubes and graphene where NO₂ molecules also serve as p-type surface dopant [62], [63]. As we can see in Figure 1.11(b), a drastic enhancement of ~1000 times larger I_{ON} is observed after surface doping of S/D by NO₂, without affecting the I_{OFF} level.

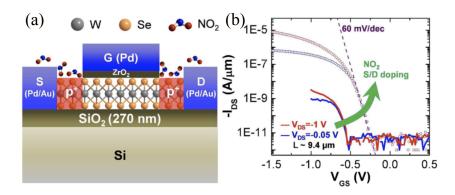


Figure 1.11 (a) Schematic of a top-gated WSe₂ monolayer FETs with chemically doped S/D contacts by NO₂ exposure. The top gate also serves as a protective layer for the active channel from NO₂ doping. (b) Transfer characteristics of WSe₂ FET with L \sim 9.4 μ m before and after NO₂ doping of the S/D contacts [61].

Hsun-Jen *et al.* reported the fabrication of both n-type and p-type WSe₂ FETs with h-BN passivated channels and ionic-liquid (IL)-gated graphene contacts [55]. High $I_{\rm ON}/I_{\rm OFF}$ up to 10^7 and large electron and hole mobility ~200 cm² V⁻¹ s⁻¹ are achieved at 170 K. As we can see from Figure 1.12(b), the on-state current at $V_{bg} = 70$ V increases by order of magnitude to 3 μ A/ μ m, while the hole current measured at $V_{bg} = -70$ V decreases by more than three orders of magnitude. Although a small Schottky barrier still exists at the graphene-WSe₂ interface, the contact resistance is significantly reduced by the combined effect of SBH reduction and SBW narrowing due to the IL gating.

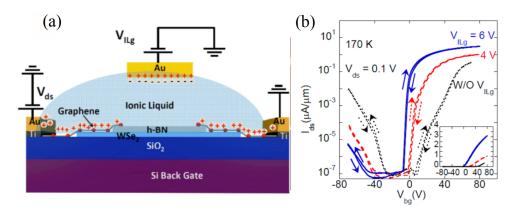


Figure 1.12 (a) Schematic illustration of the structure and working principle of a WSe₂ FET with ionic-liquid gated graphene contacts. (b) Transfer and output characteristics of a 6 nm thick WSe₂ FET device with graphene contacts and a 4.8 μ m long channel passivated by h-BN, at $V_{ds} = 0.1$ V and T = 170 K, V_{ILg} varying from 0 to 6 V. The inset shows the same date with linear scale [55].

Ferromagnetic contact by inserting a thin tunneling layer, like MgO or TiO₂, between TMDs and metal, not only reduces the contact resistance but also provides possibilities for novel spin-based electronics [64], [65]. Ohmic contact can also be achieved by using atomically thin h-BN as a tunneling layer [66]. Other

methods like thermal annealing [67] and selective etching[68], [69] also provide new ideas to lower SBH. Jingli *et al.* reported high-performance MoS₂ FETs with low contact resistance, achieved by using atomically thin hexagonal boron nitride as a tunneling layer between MoS₂ and Ni/Au metal contacts at the source and drain side [66]. Figure 1.13(a) shows the scanning electron microscope (SEM) image, optical image, and schematic side view of the fabricated device. The Schottky barrier heights are extracted from the thermionic emission regime, as shown in Figure 1.13(b) and (c). The metal contact shows the highest Schottky barrier height, around 158 meV. With one or two-layer h-BN insertion, the barrier height is reduced to 31 meV.

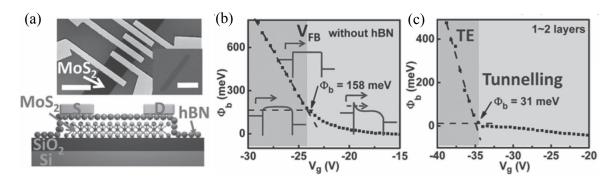


Figure 1.13 (a) SEM image (upper inset), optical image (upper), and side view schematic of MoS₂ FETs with h-BN as tunneling layer at S/D. Extracted barrier height at various Vg for MoS₂ FETs (b) without h-BN and (c) with 1 or 2 layers h-BN as tunneling layer at S/D [66].

1.3.3 Use Metallic 2D Material as Leads

Besides all these attempts to reduce the Schottky barrier by degenerate doping and engineering metal leads, the phase transition between TMD materials provides an exciting way to reduce contact resistance using metallic 2D material.

Cho *et al.* [70] reported MoTe₂ ohmic hetero-phase homojunction by using laser-induced phase patterning. The junction between the semiconducting 2H phase and the metallic 1T' phase is stable up to 300°C. Compared to 2H contact MoTe₂ devices, 1T' contact MoTe₂ device demonstrates 50 times larger field-effect carrier mobility around 50 cm² V⁻¹s⁻¹, while retaining a high on/off ratio of 10⁶. Figure 1.14(d) shows the significant reduction in the Schottky barrier height. The extracted barrier height for 1T'/2H MoTe₂ device is only 0.01 eV compared to 0.2 eV of 2H contact. The phase transition between 1T' and 2H avoids device performance degradation caused by the impurity-involved transfer process. It suggests the great potential of using metallic 2D material as a buffer contact layer for next-generation devices.

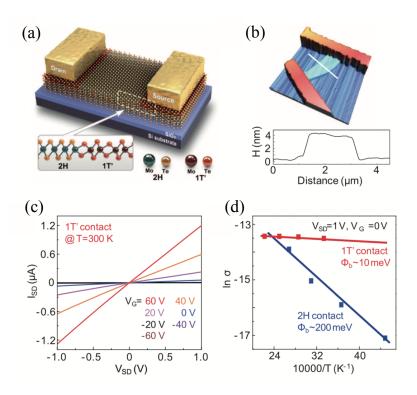


Figure 1.14 (a) Schematic diagram of a MoTe₂ device with 1T'/2H in-plane heterojunction. (b) AFM image of a fabricated device with 2H MoTe₂ in the channel and metal leads on 1T' MoTe₂. (c) I_{SD}-V_{SD} characteristics of 1T'/2H MoTe₂ device with gate voltage ranging from -60 V to 60 V. (d) Extracted barrier and Arrhenius plot of the conductance comparison between 1T' contact and 2H contact MoTe₂ device [70].

Sung et al. [17] reported on the polymorphic integration of distinct metallic 1T' and semiconducting 2H MoTe₂ crystals within the same atomic planes by heteroepitaxy. Two types of devices are fabricated, as showing in Figure 1.15. One type is 2H-only MoTe₂ FETs with metal leads on 2H MoTe₂. Another type of device is 1T'-2H heterojunction MoTe₂ FETs with 2H MoTe₂ as channel and in-plane 1T' MoTe₂ as metal leads. The coplanar contact is atomically coherent, and the extracted lowest barrier height is ~25 meV, which is significantly reduced compared to the 2H-only device with 0.15 eV barrier height. The small on-state barrier height gives small contact resistance and much larger What's more, the 1T'-2H WTe2 FETs are also fabricated following a similar process. This work demonstrates the generality of the synthetic integration approach for other TMDC polymorph films with large areas.

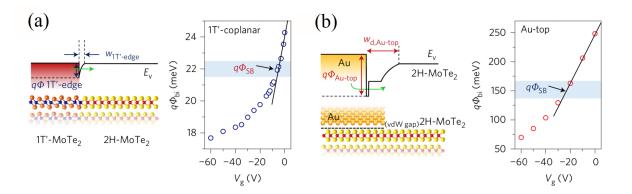


Figure 1.15 Comparison of the 1T'-side contact and Au-top contact MoTe₂ FETs. Schematic energy band at the metal-semiconductor interface and effective Schottky barrier height for (a) polymorphic 1T'-side contact and (b) Au-top contact for MoTe₂ FETs with 2H channel [17].

Zhang *et al.* [16] reported the direct synthesis of large-area metal-semiconductor (1T'-2H) heterostructure of MoTe₂ by chemical vapor deposition (CVD) technique. The phase transition from 2H to 1T' is controlled by reaction temperature and time. Device performance of FETs based on direct-grown 1T'-2H MoTe₂ with 1T' MoTe₂ serving as electrode contact is compared with devices using Ti as electrodes on 2H MoTe₂. The schematic device structure is shown in Figure 1.16(a). The transfer length method (TLM) is used to extract the contact resistance between the Ti/Au and 2H MoTe₂ interfaces as well as the metallic 1T' MoTe₂ interface, as shown in Figure 1.16(b). The measured contact resistance is 3.26 k Ω µm for 1T' MoTe₂ and 326.5 M Ω µm for 2H MoTe₂. The differential contact resistance between 2H-metal and 1T'-metal is in order of 10⁶. The 1T'-2H-1T' in-plane hetero-junction-based transistor is shown in Figure 1.16(c). From the comparison of normalized current between 1T'-2H transistor and 2H only transistor in Figure 1.16(d), we can see a great improvement in the current. It suggests contact resistance is reduced. This one-step CVD method to synthesize large-area, seamless-bonding 2D lateral metal-semiconductor junction can improve the performance of 2D electronic and optoelectronic devices.

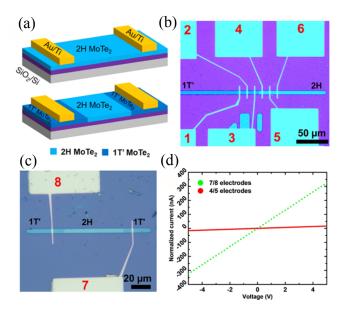


Figure 1.16 (a) Schematic MoTe₂ device structures. On the top, 2H only device with metal electrodes; on the bottom, 1T'-2H device with metal electrodes on 1T' MoTe₂. (b) Optical image of a MoTe₂ ribbon contacted by metal. Electrodes 1-3 are in contact with the 1T' phase, whereas electrodes 4-6 are in contact with the 2H phase. (c) Optical image of a 1T'-2H-1T' MoTe₂ ribbon, where metal electrodes 7 and 8 are in contact with the 1T' phase. (h) Normalized I_{DS}-V_{DS} curves acquired by electrodes 4 and 5, and 7 and 8 [16].

Ma *et al.* [18] also investigated the structural and electrical properties of in situ-grown lateral 1T'-2H MoTe2 homojunction in detail, which is grown by flux-controlled phase engineering. Here, the channel material 2H phase MoTe₂ was first grown on the substrate and patterned into individual channels. Then 1T' MoTe₂ was grown around the 2H channels and further patterned. In the last, the metal was deposited on 1T' MoTe₂ to avoid the Schottky contact between metal and 2H MoTe₂. The schematic device structures are shown in Figure 1.17(a) and (b). The contact resistance of 1T' electrodes extracted from transfer length method measurements is $470 \pm 30 \,\Omega$ µm. The back gate voltage-dependent Arrhenius plots in Figure 1.17(c) and (d) are measured to extract barrier height. The barrier of the 1T'-2H junction is around 30 ± 10 meV at zeros back gate voltage, which is much smaller than the barrier height between 2H MoTe₂ and Ti electrodes. The significant improvement in device performance compared to the metal-2H contacts suggest the great potential of in-plane heterojunctions in large-scale 2D integrated circuits.

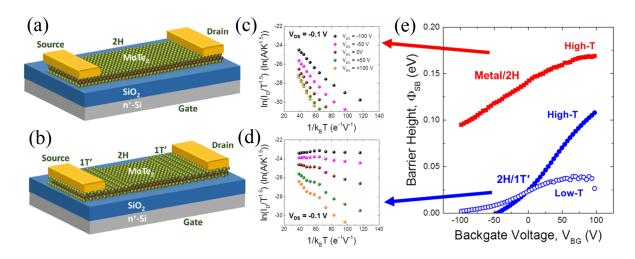


Figure 1.17 Schematic diagram of (a) 2H only and (b) 1T'-2H heterojunction MoTe₂ FETs device structures. Backgate voltage-dependent Arrhenius plots with V_{BG} ranging from -100 to 100 V for (c) 2H only and (d) 1T'-2H MoTe₂ FETs at $V_{DS} = -0.1$ V. (e) Effective Schottky barrier height of the 2H only device in the high-temperature regime (red squares) and 1T'-2H device in the high- (close blue circles) and low- (open blue circles) temperature regimes as a function of V_{BG} [18].

Similar works have been achieved by Ma *et al.* [19]. The large-scale monolayer 2H-WSe₂ is grown by CVD, and the semiconducting-to-metallic phase transition in WSe₂ is achieved via controlled *n*-BuLi treatment. In addition, two types of transistors using 2H WSe₂ as a channel are fabricated. The schematic device structure and I_{DS}-V_G characteristics are shown in Figure 1.18(a) and (b). The device performance is substantially improved with metallic 1T' phase WSe₂ serving as source/drain electrodes compared to the devices using metal like Pd/Ti and Au/Ti as electrodes, showing high on/off current ratios of 10⁷, high mobilities up to 66 cm² V⁻¹s⁻¹, and better SS down to 0.658 V/dec. These results further suggest that phase engineering can be a generic strategy to improve device performance for many kinds of 2D TMDC materials.

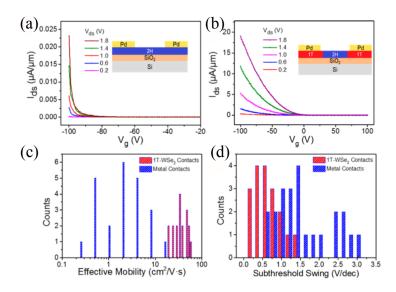


Figure 1.18 (a) I_{DS}-V_G curves for 2H only back-gated monolayer WSe₂ FET with metal contacts. Inset: Schematic device structure of 2H only WSe₂ FET. (b) I_{DS}-V_G curves for 1T-2H back-gated WSe₂ FET with metal contacts on 1T WSe₂. Inset: Schematic device structure of 1T-2H WSe₂ FET [19].

Kappera *et al.* [15] demonstrated 1T-2H MoS₂ transistors by inducing metallic 1T MoS₂ on 2H MoS₂ nanosheets. The measured contact resistance is around 200-300 Ω μm at zero gate bias, which is significantly smaller than devices directly depositing metal on MoS₂ (0.7 kΩ μm - 10 kΩ μm). FETs with 1T MoS₂ as electrodes are tested in air exhibit mobility of around 85 cm² V⁻¹s⁻¹, SS value below 100 mV/dec, high on/off ration above 10⁷, and large on-state current approaching 100 μA μm⁻¹. The electrostatic force microscopy phase image of the 1T-2H-1T MoS₂ nanosheet is shown in Figure 1.19(a). The extracted contact resistance and schematic device structure of the two types of devices are shown in Figure 1.19(b) and (c). This work suggests that phase engineering of electrodes is an effective strategy for further improving the performance of 2D MoSe₂ devices.

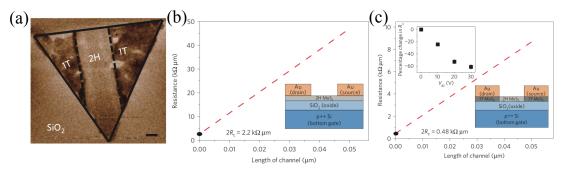


Figure 1.19 (a) Electrostatic force microscopy phase image of a monolayered MoS₂ nanosheet showing the locally patterned 2H (bright color) and 1T (dark color) phases. The scale bar is 1 μ m. Resistance versus 2H channel lengths for Au deposited directly on (b) the 2H phase and on (c) the 1T phase [15].

Even with all this exciting progress in using metallic TMD as electrodes, the reported fabricated transistors are still limited in MoS₂, WSe₂, and MoTe₂. Some underlying physics is still unclear to us. What is the mechanism of barrier lowing by using metallic TMD? How is the lattice mismatch and defects at the interface affect the device performance? Can this process extend to all 2D materials? And most importantly, can we further improve device performance by device engineering? In this work, attempts are made using quantum mechanism-based simulation to investigate the contact effect on 2D material nanotransistors' performance.

Chapter 2

Simulation Methods

2.1 Material Properties

As the conventional silicon metal-oxide-semiconductor field-effect transistor (MOSFET) technology is approaching its limits, the development of simulation tools for novel materials and nanoscale devices is becoming more and more critical. To support the long and expensive experimental processes in exploring new materials and devices, the computer-aided design stands out for its cost and time efficiency. For the device simulation, we need to start with the materials. Understanding the properties of new materials is the first step. In this section, we will briefly introduce how we extract the necessary information for device simulation from the first principle studies of novel materials.

2.1.1 DFT Calculations

Density functional theory (DFT) is the most successful and widely adopted method to study the electronic properties of novel materials. The DFT theory is derived from the many-body Schrodinger equation. For a system containing N particles, it is described by

$$\left[\sum_{i} -\frac{\hbar^2}{2m_i} \nabla_i^2 + V(r_1, \cdots r_N)\right] \Psi(r_1, \cdots r_N) = E \Psi(r_1, \cdots r_N)$$
 (2.1)

However, this equation is almost impossible to solve directly for any system containing many atoms. For example, if a system containing 10 electrons and no nuclei, with 100 grid points along each spatial direction. We need to solve a matrix with a size of $100^{3\cdot 10} = 10^{60}$. The first step to make this problem feasible is the Boron-Oppenheimer approximation, which separates the wavefunctions for the nuclei and the electrons. We can further consider the valance electrons. The nuclei along with the core electrons can be considered as a closed shell and treated classically. Still, the problem is too large to solve. An important concept is introduced, which is the electron density at any position r_1 is defined as:

$$n(r_1) = N \int r_2 \cdots \int r_N \Psi^*(r, r_2, \cdots r_N) \Psi(r, r_2, \cdots r_N)$$
(2.2)

It reduces the dimension of the problem from 3N to 3. Most approaches in solid-state physics are based on the single-electron eigenvalue equations, where each electron interacts only with the mean-field of all the others. The Schrodinger equation can be written in the following form

$$\widehat{H}\Psi(r_1,\cdots r_N) = (\widehat{T} + \widehat{V} + \widehat{U})$$
(2.3)

$$\left[\sum_{i}^{N} -\frac{1}{2}\nabla_{i}^{2} + \sum_{i}^{N} V(r_{i}) + \sum_{i < j}^{N} U(r_{i}, r_{j})\right] \Psi(r_{1}, \dots r_{N}) = E\Psi(r_{1}, \dots r_{N})$$

where the three terms in Hamiltonian are kinetic energy (\hat{T}) , external potential (\hat{V}) , and electron-electron interactions (\hat{U}) [71], [72]. There are two fundamental theorems in DFT by Hohenberg-Kohn:

- The ground-state energy is a unique functional of electron density.
- The electron density that minimizes the energy of the overall functional is the true ground-state electron density.

For non-degenerate ground-states, the wavefunction uniquely depends on the potential \hat{V} , and there exists exactly one \hat{V} that produces the prescribed charge density. The ground-state wavefunction and energy are unique functionals of the density. The general energy functional can be expressed as

$$E_V[n(r)] = F[n(r)] + \langle \Psi[n(r)] | \hat{V} | \Psi[n(r)] \rangle$$
(2.4)

where the variable F is called universal functional as it doesn't depend on the specific system and is defined as

$$F[n(r)] = \langle \Psi[n(r)] | \hat{T} + \widehat{U} | \Psi[n(r)] \rangle \tag{2.5}$$

The ground state energy $E_{0,V}$ can be written as

$$E_{0,V} = E_V[n_0(r)] (2.6)$$

With the knowledge above, we can rewrite the many-electron Schrodinger equation through a set of single-electron equations

$$(\widehat{T} + \widehat{V_{Ne}} + \widehat{V_H} + \widehat{V_{XC}})\Psi_i = E_i \Psi_i$$
(2.7)

where \widehat{T} is the kinetic energy term, $\widehat{V_{Ne}}$ is the potential interaction term of the electron and the atomic nuclei, $\widehat{V_H}$ is the Hartree potential describing the repulsive interactions of the single electron to the total electron density of the system. These three terms are known terms. The $\widehat{V_{XC}}$ is the unknown term, which is the functional derivative of the exchange-correlation functional E_{XC} .

$$\hat{T} = -\frac{1}{2}\nabla_i^2 \tag{2.8}$$

$$\widehat{V_{Ne}} = -\frac{Z_A}{r_{iA}} \tag{2.9}$$

$$\widehat{V_H} = \int \frac{n(r_j)}{r_{ij}} dr_j \tag{2.10}$$

$$\widehat{V_{XC}} = \frac{\delta E_{XC}}{\delta n} \tag{2.11}$$

One can find the solution following a self-consistency scheme:

- 1. Define a trailing electron density n(r)
- 2. Solve Kohn-Sham equations with n(r) and obtain a single electron wave function Ψ_i .
- 3. Calculate the electron density $n_{new}(r)$ based on the single-electron wave functions using Eqn. (2.2).
- 4. Check if $n_{new}(r) = n(r)$. If yes, calculate the ground-state energy E_0 . If not, adjust n(r) using a weighted average of $n_{new}(r)$ and n(r) and go back to step 1 until the difference is below the tolerance.

There are several methods to approximate E_{XC} . Here we'll just briefly introduce the two simplest ones as the local density approximation (LDA) method and generalized gradient approximation (GGA) method. The LDA assumes the system has a uniform electron gas with density n(r), the electrons are moving in the background of positive charge distribution, and the total ensemble is charge neutral. While the LDA method has been successfully applied to many quantum chemistry problems, it suffers from underestimating the band gap of most semiconductors when dealing with solid-state physics problems. The accuracy can be improved by taking into account the gradient of the electron density beside the local density itself. It is known as the GGA method. The most commonly used GGA functional these days are the Perdew-Wang (PW91) functional and Perdew-Burke-Ernzerhof (PBE) functional.

There are several packages available for DFT simulation: VASP, Quantum Espresso, Abinit, and Siesta. In this study, all the DFT simulations are performed using Quantum Espresso. Quantum Espresso is an integrated open-source package for electronic-structure calculations and materials modeling in nanoscales based on DFT, plane waves, and pseudopotentials. There are device simulation packages based on DFT-NEGF, such as Quantum ATK. However, in most cases, DFT is too complicated for device simulations. DFT-NEGF is limited by the size of atomic numbers limited to a few hundred atoms. For practical device simulations in sub-micrometer scales, we need a more practical method to describe material properties, for example, by using effective mass approximations, tight-binding (TB) approximations, and maximally localized Wannier functions (MLWF).

2.1.2 Effective Mass Approximation

The effective mass approximation was extensively used to describe electronic motion in the presence of slowly varying perturbations. Under effective mass approximation, the motion of the electrons is described

by the one-electron Hamiltonian, assuming that the many-body interactions among electrons are negligible. In solid-state physics, band structures around the conduction band bottom can be described as

$$E(k) = E_0 + \frac{\hbar^2 k^2}{2m^*} \tag{2.12}$$

where E(k) is the energy of an electron at wavevector k, E_0 is usually the conduction band bottom or valence band top. By analogy with three-dimensional ellipsoidal energy bands, the E(k) of 2D materials can be approximated by

$$E(k) = E_0 + \frac{\hbar^2}{2m_x^*} (k_x - k_{0,x})^2 + \frac{\hbar^2}{2m_y^*} (k_y - k_{0,y})^2$$
 (2.13)

where m_x^* and m_y^* are the inertial effective masses along x and y axes around $k_{0,x}$ and $k_{0,y}$. We can further define the density of states effective mass (m_{dos}) and conductivity effective mass (m_c) by

$$m_{dos} = \left(m_x m_y\right)^{1/2} \tag{2.14}$$

$$m_c = 2\left(\frac{1}{m_x} + \frac{1}{m_y}\right)^{-1} \tag{2.15}$$

Here we use monolayer MoS_2 as an example to show how to extract effective mass from DFT band structures. Most TMDs materials exhibit isotropic electron-effective mass. The band structure from DFT calculations of MoS_2 is shown in Figure 2.1(a). Here the mid-bandgap (E_i) is not at 0 eV since this is the direct output from the DFT simulation. The usual band structure can be easily achieved by shifting E_i to 0 eV. To extract the effective mass for electrons, we first plot the surface of the conduction band in the k-space in Figure 2.1(b). There are two conduction band valleys in the first Brillouin zone, which is indicated by the hexagon (white line). Since we are only interested in the bands near the conduction band bottom, an enlarged surface plot around the K point is shown in Figure 2.1(c). By applying parabolic fitting, we extracted the effective mass along the x and y direction and compared the bands with DFT bands in Figure 2.1(d) and (e). The polar plot of the electron effective mass of MoS_2 is shown in Figure 2.1(f). The electron effective mass of MoS_2 is near isotropic and is around $0.57m_0$. Similar processes can be adapted to extract hole effective mass is also near isotropic and is around $0.61m_0$.

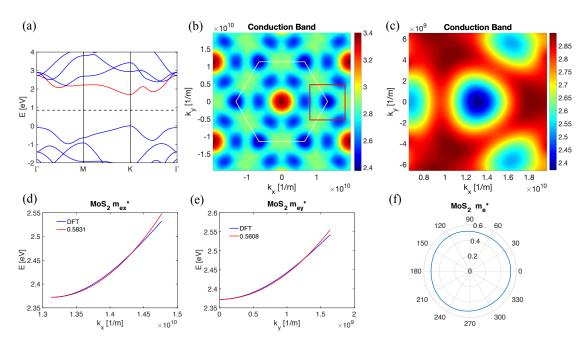


Figure 2.1 (a) MoS_2 band structure along with high symmetry points from DFT, red line denotes the conduction band (b) Surface plot of MoS_2 conduction band in k-space, the white line indicates the first Brillouin zone, the red line indicates the fitting range around K point which is the conduction band bottom. (c) Surface plot of MoS_2 conduction band around K point. The DFT bands compared with the parabolic fitting of E(k) around K points along (d) K-direction and (e) K-direction. (f) Extracted electron effective mass polar plot.

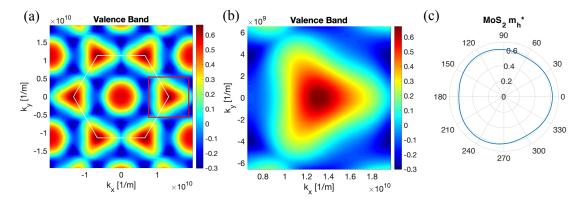


Figure 2.2 (a) Surface plot of MoS_2 valence band in k-space. (b) Surface plot of valence band around K point. (c) Extracted hole effective mass polar plot.

2.1.3 Tight-binding Approximation

A tight-binding method is an approach to the calculation of electronic band structure using an approximate set of wave functions based upon the superposition of wave functions. It is closely related to the linear combination of atomic orbitals (LCAO) method, which is also a semi-empirical method. The name "tight binding" itself suggests that, in this model, electrons are considered tightly bounded to atoms. This method

can describe complex band structures with much better accuracy than the effective mass method, while at the same time, it can be applied to much larger systems than DFT up to a few thousand atoms. In this chapter, we will use monolayer TMD and monolayer to few-layer BP as examples to briefly demonstrate how the TB method solves band structures.

For monolayer TMD, here we adopt a three-band tight-binding approximation [24]. It is assumed that only three d orbitals $(d_{z^2}, d_{xy}, d_{x^2-y^2})$ of M (Mo, W) atom are considered and p orbitals of X (S, Se, Te) atom are neglected, since the Bloch states of monolayer MX_2 near the band edges mostly consist of these three orbitals. We will start with the nearest-neighbor tight-binding (NN TB) model. The on-site Hamiltonian matrix for the unit cell as shown in Fig. 1.6(a) can be written as

$$H_0 = \begin{bmatrix} \epsilon_1 & 0 & 0 \\ 0 & \epsilon_2 & 0 \\ 0 & 0 & \epsilon_2 \end{bmatrix}$$

The integrations with neighbor unit cells as denoted by R_1 to R_6 can be written as

$$H_1 = \begin{bmatrix} t_0 & t_1 & t_2 \\ -t_1 & t_{11} & t_{12} \\ t_2 & -t_{12} & t_{22} \end{bmatrix}$$

$$H_{2} = \begin{bmatrix} t_{0} & \frac{1}{2}t_{1} - \frac{\sqrt{3}}{2}t_{2} & -\frac{\sqrt{3}}{2}t_{1} - \frac{1}{2}t_{2} \\ -\frac{1}{2}t_{1} - \frac{\sqrt{3}}{2}t_{2} & \frac{1}{4}t_{11} + \frac{3}{4}t_{22} & \frac{\sqrt{3}}{4}(t_{22} - t_{11}) - t_{12} \\ \frac{\sqrt{3}}{2}t_{1} - \frac{1}{2}t_{2} & \frac{\sqrt{3}}{4}(t_{22} - t_{11}) + t_{12} & \frac{3}{4}t_{11} + \frac{1}{4}t_{22} \end{bmatrix}$$

$$H_{6} = \begin{bmatrix} t_{0} & \frac{1}{2}t_{1} + \frac{\sqrt{3}}{2}t_{2} & \frac{\sqrt{3}}{2}t_{1} - \frac{1}{2}t_{2} \\ -\frac{1}{2}t_{1} + \frac{\sqrt{3}}{2}t_{2} & \frac{1}{4}t_{11} + \frac{3}{4}t_{22} & -\frac{\sqrt{3}}{4}(t_{22} - t_{11}) - t_{12} \\ -\frac{\sqrt{3}}{2}t_{1} - \frac{1}{2}t_{2} & -\frac{\sqrt{3}}{4}(t_{22} - t_{11}) + t_{12} & \frac{3}{4}t_{11} + \frac{1}{4}t_{22} \end{bmatrix}$$

$$H_{3} = H_{6}^{T}$$

$$H_{4} = H_{1}^{T}$$

$$H_{5} = H_{2}^{T}$$

In this way, the Hamiltonian matrix of NN TB MX₂ can be written as

$$H = H_0 + H_1 e^{i\vec{k}\cdot \overrightarrow{R_1}} + H_2 e^{i\vec{k}\cdot \overrightarrow{R_2}} + H_3 e^{i\vec{k}\cdot \overrightarrow{R_3}} + H_4 e^{i\vec{k}\cdot \overrightarrow{R_4}} + H_5 e^{i\vec{k}\cdot \overrightarrow{R_5}} + H_6 e^{i\vec{k}\cdot \overrightarrow{R_6}}$$

The fitted parameters of the three-band NN TB model of monolayer MX_2 using generalized gradient approximations (GGA) are shown in Table 2.1. a and Z_{X-X} are the relaxed lattice constant and X-X distance in the z-direction, respectively. The energy parameters ϵ_1 to t_{22} are given in the unit of eV. Here we use MoS₂ and MoSe₂ as two examples to show the band structures plotted by using the TB parameters (blue) and the first principle results (red) in Figure 2.3(a) and (b), respectively.

Table 2.1 Fitted parameters of the three-band NN TB models for monolayer MX₂ [24].

	a(Å)	$z_{X-X}(\mathring{A})$	ϵ_1	ϵ_2	t_0	t_1	t_2	t ₁₁	t ₁₂	t ₂₂
					GGA					
MoS_2	3.190	3.130	1.046	2.104	-0.184	0.401	0.507	0.218	0.338	0.057
WS_2	3.191	3.144	1.130	2.275	-0.206	0.567	0.536	0.286	0.384	-0.061
$MoSe_2$	3.326	3.345	0.919	2.065	-0.188	0.317	0.456	0.211	0.290	0.130
WSe_2	3.325	3.363	0.943	2.179	-0.207	0.457	0.486	0.263	0.329	0.034
$MoTe_2$	3.557	3.620	0.605	1.972	-0.169	0.228	0.390	0.207	0.239	0.252
WTe_2	3.560	3.632	0.606	2.102	-0.175	0.342	0.410	0.233	0.270	0.190

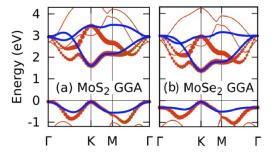


Figure 2.3 The NN TB band structures (blue line) of MX₂ monolayer compared with the first principle results (red lines) for (a) MoS₂ and (b) MoSe₂ [24].

The tight-binding parameters of BP are extracted from *GW* approximation [73] and listed in Table 2.2. The interactions between each atom in one unit cell are shown in Figure 2.4. Due to the rectangular unit cell, the Hamiltonian matrix of the interaction between unit cell to its neighbor cells can be written as follows:

$$\alpha = \begin{bmatrix} 0 & t_1 & t_4 & t_5 \\ t_1 & 0 & t_2 & t_4 \\ t_4 & t_2 & 0 & t_1 \\ t_5 & t_4 & t_1 & 0 \end{bmatrix}$$

$$\beta = \begin{bmatrix} 0 & 0 & 0 & 0 \\ t_3 & 0 & 0 & 0 \\ t_4 & t_5 & 0 & 0 \\ t_2 & t_4 & t_3 & 0 \end{bmatrix}$$

For bilayer BP, interlayer interactions need to be added to the Hamiltonian matrix. The interlayer interactions can be described as bottom to the top layer (B2T) and top to bottom layer (T2B). The relevant matrices are given as:

In this way, the interactions between unit cell to its neighbor cells can be written as:

$$\begin{split} \alpha_{bi} &= \begin{bmatrix} \alpha & \alpha_{T2B} \\ \alpha_{B2T} & \alpha^T \end{bmatrix} \\ \beta_{bi} &= \begin{bmatrix} \beta & \beta_{T2B} \\ \beta_{B2T} & \beta^T \end{bmatrix} \\ \gamma_{bi} &= \begin{bmatrix} \gamma & \gamma_{T2B} \\ \gamma_{B2T} & \gamma^T \end{bmatrix} \\ \delta_{1bi} &= \begin{bmatrix} \delta_1 & \delta_{1T2B} \\ \delta_{1B2T} & \delta_1^T \end{bmatrix} \\ \delta_{2bi} &= \begin{bmatrix} \delta_2 & \delta_{2T2B} \\ \delta_{2B2T} & \delta_2^T \end{bmatrix} \\ H_{bi} &= \alpha_{bi} + \beta_{bi} e^{i\vec{k}\cdot(a,0)} + \gamma_{bi} e^{i\vec{k}\cdot(0,b)} + \delta_{1bi} e^{i\vec{k}\cdot(a,b)} + \delta_{2bi} e^{i\vec{k}\cdot(a,-b)} \\ + \beta_{bi}^T e^{i\vec{k}\cdot(-a,0)} + \gamma_{bi}^T e^{i\vec{k}\cdot(0,-b)} + \delta_{1bi}^T e^{i\vec{k}\cdot(-a,-b)} + \delta_{2bi}^T e^{i\vec{k}\cdot(-a,b)} \end{split}$$

Table 2.2 Intralayer (*t*) and interlayer (*h*) hopping parameters of tight-binding parameters for monolayer and bilayer BP [73].

Number of layers	1	2	3	4	5
Intralayer (t) [eV]	-1.220	3.665	-0.205	-0.105	-0.055
Interlayer (h) [eV]	0.295	0.273	-0.151	-0.091	_

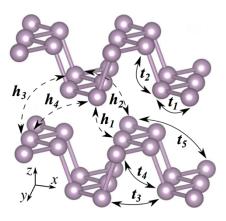


Figure 2.4 Intralayer and interlayer interactions in bilayer BP [73].

The comparison between DFT bands and tight-binding bands of monolayer and bilayer BP is shown in Figure 2.5. The conduction band bottom and valence band top are both located in Γ points. Even though the E(k) from the TB method is away from DFT bands along most high symmetry points, it captures the

bands around Γ points pretty well. This is already enough for large-scale device simulations with very good accuracy.

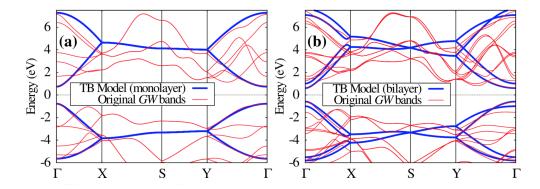


Figure 2.5 Band structure using tight-binding (blue line) in comparison with the original *GW* band structure (red line) for (a) monolayer BP and (b) bilayer BP [73].

2.1.4 MLWF Approximation

Most of the DFT codes are using plane-waves to expand the single-particle Kohn-Sham wavefunctions. However, this is not suitable for transport simulations. The localized basis functions are desired for high-accuracy quantum transport simulations. Wannier introduced a localized, real-space representation of Bloch states. Later, Marzari and Vanderbilt developed a formally and computationally attractive method for the construction of such Wannier functions (WFs) with maximal localization criteria. It is implemented in the Wannier90 code [74]. The Bloch Hamiltonian is transformed to the MLWF basis. The MLWF can fit band structure very well, yet still practical for device scale simulations. With the help of Wannier90, we can study complex heterojunction structures, which is difficult in the TB method. In this section, we will use bilayer AB stacking 1T2H MoS₂ as an example to demonstrate how MLWF makes hetero-junction device simulation possible.

The top view and side view of the atomic structure of the 1T2H bilayer is shown in Figure 2.6(a). The primitive cell is highlighted by a black rhombus panel. This is the cell used for band structure calculation for most material studies. And the corresponding band structure is shown in Figure 2.6(b). As the existence of Van Der Waals interaction between 1T and 2H layer, the band structure of 1T2H bilayer is different from 1T bands overlie on 2H bands. The 1T2H MoS₂ is a metallic material with zero bandgaps. However, the primitive cell is not suitable for NEGF simulation. We constructed a rectangular supercell which is denoted by the grey panel, with twice the number of atoms compared to the primitive cell. From the orbital contribution analysis, we found the bands near the Fermi level is mainly contributed by the five d orbitals $(d_{z^2}, d_{xz}, d_{yz}, d_{xy}, d_{x^2-y^2})$ from Mo atom, and three p orbital (p_x, p_y, p_z) from S atom. As there are 4 Mo atoms and 8 S atoms in one supercell, the extracted MLWF is 44 by 44 matrix. The band structure from

extracted MLWF is compared with the DFT bands in Figure 2.6(c). We can see that the fitting is very good for a large energy range.

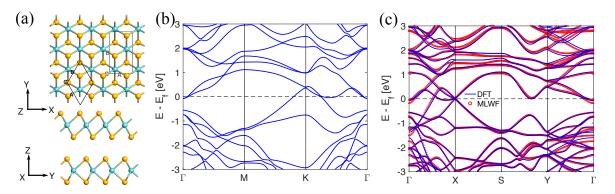


Figure 2.6 (a) Top view and side view of 1T2H bilayer (b) Band structure along high symmetry points from DFT of MoS₂ primitive cell (c) Band structure of MoS₂ rectangular supercell comparison between DFT and MLWF.

2.2 Schottky Barrier

2.2.1 Metal-Semiconductor Junction

For modeling of Schottky contact device, we will start from the ideal case of the conventional 3D semiconductor-metal junction. The band diagrams of metal and n-type semiconductor are shown in Figure 2.7, where ϕ_{Bn} is the barrier height, and E_{Fm} is the fermi level of metal, Ψ_{bi} is the build-in potential of the semiconductor. The barrier height is determined by the work function of metal (ϕ_m) and electron affinity of semiconductor (χ) , and we have $q\phi_{Bn} = q(\phi_m - \chi)$ [75]. Here the interface states and image-force barrier lowering will not be considered. We will focus on the current transport process.

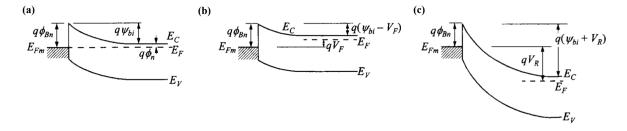


Figure 2.7 Energy band diagrams of metal and n-type semiconductors under different biasing conditions (a) Thermal equilibrium (b) Forwards bias (c) Reverse bias [75].

For forward bias conditions, five basic transport processes are normally considered, as shown in Figure 2.8. These five processes are (1) electrons emission over barrier, (2) electron tunneling through barrier, (3) recombination in the space-charge region, (4) diffusion of electrons, (5) diffusion of holes. Here processes (1) and (2) will be mainly discussed. For thermionic emission, the following assumptions are made to derive

the current: 1) barrier height $q\phi_{Bn}$ is much larger than kT, 2) thermal equilibrium is established, 3) the existence of net current flow doesn't affect equilibrium. Thus we can decompose the total current into two current fluxes, one from semiconductor to metal and the other from semiconductor to metal.

$$J_n = J_{S \to M} - J_{M \to S} \tag{2.16}$$

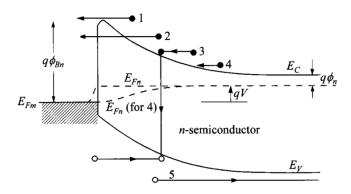


Figure 2.8 Five basic transport processes for forward bias metal and n-type semiconductor contacts [75].

Since only thermionic emission is considered here, the current flow only depends on barrier height, and the barrier shape is immaterial. The current density from semiconductor to metal is determined by the electrons with sufficient energy to overcome the barrier, which is $E_{Fn} + q\phi_{Bn}$.

$$J_{S \to M} = \int_{E_{Fn} + q\phi_{Bn}}^{\infty} q \nu_x dn \tag{2.17}$$

Where v_x is the carrier velocity along the transport direction. The electron density is given according to

$$dn = N(E)F(E)dE \approx \frac{4\pi (2m^*)^{\frac{3}{2}}}{h^3} \sqrt{E - E_C} \exp\left(-\frac{E - E_C + q\phi_n}{kT}\right) dE$$
 (2.18)

Where N(E) is the density of states and F(E) is the distribution function, m^* is the effective mass of electron at conduction band. If we assume for electrons, all the energy in the conduction band is kinetic energy. We will have $\sqrt{E - E_C} = v\sqrt{m^*/2}$. Then Equation 2.18 can be written as

$$dn \approx 2\left(\frac{m^*}{h}\right)^3 \exp\left(-\frac{q\phi_n}{kT}\right) \exp\left(-\frac{m^*v^2}{2kT}\right) (4\pi v^2 dv)$$
 (2.19)

This describes the number of electrons per unit volume with velocities between v and v + dv in all directions. Since the desired transport direction is along +x direction, with the transformation $4\pi v^2 dv = dv_x dv_y dv_z$. We can have

$$J_{S \to M} = 2q \left(\frac{m^*}{h}\right)^3 \exp\left(-\frac{q\phi_n}{kT}\right) \int_{v_{0x}}^{\infty} v_x \exp\left(-\frac{m^* v_x^2}{2kT}\right) dv_x$$

$$\int_{-\infty}^{\infty} \exp\left(-\frac{m^* v_y^2}{2kT}\right) dv_y \int_{-\infty}^{\infty} \exp\left(-\frac{m^* v_z^2}{2kT}\right) dv_z$$

$$= \left(\frac{4\pi q m^* k^2}{h^3}\right) T^2 \exp\left(-\frac{q\phi_n}{kT}\right) \exp\left(-\frac{m^* v_{0x}^2}{2kT}\right)$$
(2.20)

The velocity v_{0x} is the minimum velocity to surmount the barrier, which is given by $\frac{1}{2}m^*v_{0x}^2 = q(\psi_{bi} - V)$. We can further get

$$J_{S \to M} = \left(\frac{4\pi q m^* k^2}{h^3}\right) T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \exp\left(\frac{qV}{2kT}\right) = A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \exp\left(\frac{qV}{2kT}\right)$$
(2.21)

where the prefactor $A^* = \frac{4\pi q m^* k^2}{h^3}$ is the effective Richardson constant for thermionic emission, neglecting the effects of optical-phonon scattering and quantum effect. For free electrons $(m^* = m_0)$ the Richardson constant is 120 A/cm²-K². For electrons injected from metal to semiconductor remain constant as barrier height is not affected by bias. At thermal equilibrium (V = 0) we have $J_{S \to M} = J_{M \to S}$.

$$J_{M\to S} = A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \tag{2.22}$$

In the way, we get

$$J_n = A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \left[\exp\left(\frac{qV}{2kT}\right) - 1\right] = J_{TE} \left[\exp\left(\frac{qV}{2kT}\right) - 1\right]$$
(2.23)

where
$$J_{TE} = A^*T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right)$$
.

The thermionic current is strongly affected by temperature. When the temperature is low, the tunneling current will become the dominant part. Similarly, when the semiconductor is highly doped, the barrier becomes thinner, and the tunneling current becomes more significant. As we increase the doping concentration, the degenerate semiconductor will form an ohmic contact with metal where the tunneling current is the dominant transport process. We can roughly categorize the components into three types as shown in Figure 2.9: (1) thermionic emission (TE) over the barrier as we discussed above, (2) field emission (FE) near the Fermi level, which is a pure tunneling process and (3) thermionic-field emission (TFE) at an energy between TE and FE, which is tunneling of thermally excited carriers through thinner barrier than FE. The relative contributions of these components depend on both temperature and doping level. The further analytical expression is complex and not intuitive. Rigorous numerical simulations based on quantum mechanisms are needed as we will discuss in the following chapters.

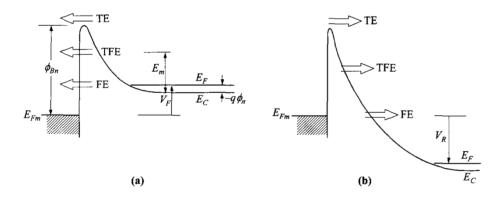


Figure 2.9 Energy band diagrams of tunneling currents in Schottky metal and n-type semiconductor under (a) forward bias (b) reverse bias. E_m is where the TFE peak locates [75].

2.2.2 Extracting SB Height from DFT Simulation

Extracting Schottky barrier height is one key step towards practical device simulations. Here we'll use 1T-2H heterojunction MoS₂ as an example to demonstrate how barrier height is extracted from DFT simulations. The top view and side view of in-plane 1T-2H MoS₂ heterojunction, top contact 1T-2H junction with AB stacking, and top contact 1T-2H with AA stacking heterojunctions are shown in Figure 2.10. As DFT simulations are using plan wave functions, in the x-direction, heterojunctions are constructed with enough length for 1T and 2H MoS₂. Enough space is used in the z-direction to screen the interactions. Van der Waals interactions are considered with vdW-DF2 Van der Waals density functional. A 7×11×1 kspace sampling is used for self-consistent simulations. A denser k mesh of $15 \times 21 \times 1$ is used for non-selfconsistent simulations. The kinetic energy cutoff for wavefunctions is set to 50 Ry, and the kinetic energy cutoff for charge density and potential is set to 400 Ry. The difference between AB and AA stacking in bilayer 1T2H MoS₂ as shown in Figure 2.10(b) and (c) is, for AA stacking, all the Mo atoms in bottom 2H MoS₂ are under the Mo atoms in the top 1T layer, similarly for S atoms; for AB stacking, all the Mo atoms in the bottom 2H layer are under the S atoms in top 1T layer, S atoms in the bottom 2H layer are under Mo atoms in top 1T layer. AB stacking are slightly more stable than AA 1T2H stacking MoS₂. The projected density of states (PDOS) of 2H MoS₂ in the right part of the heterojunction is extracted. Then we can read the E_c and E_v from the PDOS plot and read the difference to the common Fermi level, which is the Schottky barrier height. The bandgap read from PDOS fits the bandgap calculated from free-standing 2H MoS₂. As we can see in the right part of Figure 2.10, 1T-2H side contact MoS₂ heterojunction is *n*-type with Φ_{Bn} = 0.70 eV, 1T-2H top contact MoS₂ heterojunctions with AB stacking and AA stacking are p-type with Φ_{Bp} = 0.72 eV and 0.74 eV respectively. We also notice in the bandgap region of PDOS, the top contact is clean with close to zero value. However, in the side contact heterojunction, some non-zero value exists. This is because the coupling formed in the side contact heterojunction is much stronger than the Van der Waals

interactions in top contact. The stronger interactions make $2H \text{ MoS}_2$ semi-metallic when it's close to $1T \text{ MoS}_2$. This can be observed in the space distributed PDOS plot of side contact heterojunction in Figure 2.11. The white lines in the 2H part denote the conduction band bottom and valence band top. The red color indicates high DOS, and blue indicates low DOS. For $2H \text{ MoS}_2$ away from the interface, it is semiconducting with a clear bandgap. However, for $2H \text{ MoS}_2$ in the middle and right end (as this is still periodic along x-axis), we notice red peaks in the bandgap energy range, which makes semiconducting $2H \text{ MoS}_2$ "semi-metallic."

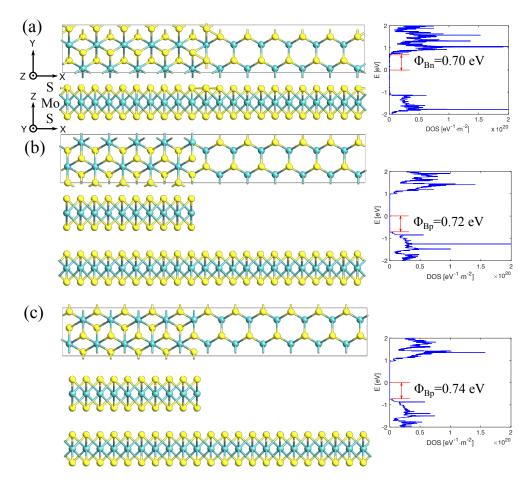


Figure 2.10 Top view and side view of MoS₂ heterojunctions with (a) 1T-2H side contact (b) 1T-2H top contact with AB stacking (c) 1T-2H top contact with AA stacking. The projected density of states (PDOS) plots from 2H MoS₂ are on the right column.

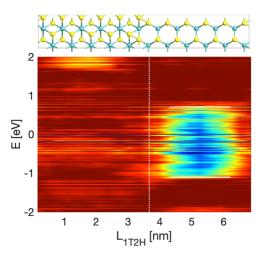


Figure 2.11 Space distributed PDOS for side contact 1T-2H MoS₂ heterojunction.

The different extracted barrier height indicates the geometry of junction has strong effects. In DFT simulation, the metallic 1T MoS₂ is strained to match the lattice constant of 2H MoS₂. In real experiments, things can be much more complex. There might exist defects at the interface, the interface between 1T and 2H might be nonuniform, the interface atoms might suffer from hanging dangling bonds. All these nonideal effects might result in the shifting of Schottky barrier height. In this study, we will only focus on the ideal case.

2.3 Quantum Transport Simulations

The wave-like behavior of electrons becomes substantially significant in nanoscale devices. As a result, the semiclassical transport equation, like Boltzmann Transport Equation (BTE), may not be valid anymore. A full quantum mechanical transport non-equilibrium Green's function (NEGF) approach is needed. With the help of DFT simulation, we can extract the H matrix describing the material properties and extract Schottky barrier height at the metal-semiconductor interface. In this section, the atomic quantum transport simulation method will be briefly introduced [76]. We will start from the 1D atomic chain and expand to more generalized forms in Green's functions.

2.3.1 Phase Coherent Quantum Transport in 1D Atomic Chain

The Hamiltonian of a spatially uniform one-dimensional grid point with spacing a and with a constant potential is

$$-t\Psi_{q-1} + (E - \epsilon)\Psi_q - t\Psi_{q+1} = 0$$
 (2.24)

Where E is the energy, and Ψ_q is the wave function at grid point q. Using the Bloch theorem, the solution of Equation 2.24 is

$$E = \epsilon + 2t \cos(ka)$$

$$\Psi_q = e^{ikqa}$$
(2.25)

A general nearest neighbor uniform tight-binding Hamiltonian can be given as

$$-t_{q,q-1}\Psi_{q-1} + (E - \epsilon_q)\Psi_q - t_{q,q+1}\Psi_{q+1} = 0$$
(2.26)

where ϵ_q is the onsite potential at gird q and $t_{q,q+1}$ is the hopping parameter from grid q to q+1. We have $t_{q,q+1} = t_{q+1,q}^{\dagger}$ as the Hamiltonian is Hermitian. In effective mass approximation, we have

$$t = t_{q,q+1} = t_{q,q+1} = -\frac{\hbar^2}{2m^*a^2}$$

$$\epsilon_q = V_q + \frac{\hbar^2}{m^*a^2} = V_q - 2t$$
(2.27)

Where m^* is the effective mass and V_q is the electrostatic potential at grid q.

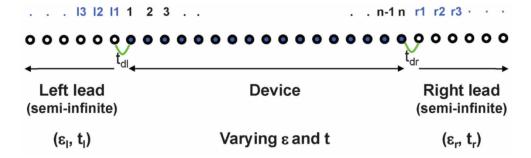


Figure 2.12 A schematic of the setting of Schottky contact FET. The Source and Drain are semi-infinite metal leads, with a notation of (1, 1, 2, ...) and (r1 r2 ...). The Device region is with the notation of (1, 2, 3 ...) [76].

A typical SBFET can be divided into three parts: semi-infinite source metal lead, semi-infinite drain metal lead, and semiconducting device region, as shown in Figure 2.7. The effective mass of electron in the semiconductor is m^* and the effective mass of electron in metal is m_t^* . The potential of the source (drain) lead ϵ_l (ϵ_r) and the hopping parameter t_l (t_r) is assumed to be constant. Then the Hamiltonian of the device and leads can be expressed as

$$-t_{l}\Psi_{l3} + (E - \epsilon_{l})\Psi_{l2} - t_{l}\Psi_{l1} = 0$$

$$-t_{l}\Psi_{l2} + (E - \epsilon_{l})\Psi_{l1} - t_{l,d}\Psi_{1} = 0$$

$$-t_{d,l}\Psi_{l1} + (E - \epsilon_{1})\Psi_{1} - t_{1,2}\Psi_{2} = 0$$
(2.28)

$$-t_{2,1}\Psi_1 + (E - \epsilon_2)\Psi_2 - t_{2,3}\Psi_3 = 0 (2.30)$$

•

$$-t_{n,n-1}\Psi_{n-1} + (E - \epsilon_n)\Psi_n - t_{d,r}\Psi_{r1} = 0$$
 (2.31)

$$-t_{r,d}\Psi_n + (E - \epsilon_r)\Psi_{r1} - t_r\Psi_{r2} = 0$$

$$-t_r\Psi_{r1} + (E - \epsilon_r)\Psi_{r2} - t_r\Psi_{r3} = 0$$
(2.32)

•

Follow the routing, we want to fold the influence of semi-infinite metal leads into Σ_S and Σ_D . The wave function in source and drain leads due to waves incident from left is

$$\Psi_{ln} = (e^{+ik_lx_{ln}} + s_{ll}e^{-ik_lx_{ln}}) \text{ in region L}$$
(2.33)

$$\Psi_{rn} = s_{rl} e^{+ik_r x_{rn}} \text{ in region R}$$
 (2.34)

Where x_{ln} and x_{rn} correspond to integer times grid spacing (a), s_{ll} and s_{rl} are the reflection and transmission amplitudes. The normalization constant has been neglected, and the corresponding eigenvalues are

$$E - \epsilon_l = 2t_1 cos(k_l a) = t_1 \left(e^{ik_l a} + e^{-ik_l a} \right)$$
(2.35)

Similarly, for right lead, with indexes r. Substituting (2.38) and (2.40) in (2.33) we have

$$s_{ll} = t_l^{-1} (-t_l + t_{l,d} \Psi_1)$$
 (2.36)

Substituting (2.36) and (2.33) in (2.28) we have

$$(E - \epsilon_1 - t_{d,l}e^{ik_la}t_l^{-1}t_{l,d})\Psi_1 - t_{1,2}\Psi_2 = -2it_{d,l}\sin(k_la)$$
(2.37)

Equation (2.37) is a modification of equation (2.29). As we can see here, the influence of the entire semi-infinite left lead has been included in grid point 1. Similarly, substituting (2.34) and $E - \epsilon_r = 2t_r cos(k_r a)$ into (2.32), we have

$$s_{lr} = \frac{t_{r,d}}{t_r} \Psi_n \tag{2.38}$$

Once we substitute (2.34) and (2.38) into (2.31) we can fold the influence of the entire semi-infinite right lead into grid point n.

$$-t_{n,n-1}\Psi_{n-1} + \left(E - \epsilon_n - \frac{t_{r,d}}{t_r}e^{ik_r a}\right)\Psi_n = 0$$
 (2.39)

To get the wave function in the device due to waves incident from left lead, we can solve the following *n*-dimensional matrix:

$$A\Psi_D^{(L)} = i_L \tag{2.40}$$

Where the size of A is n by n, $\Psi_D^{(L)}$ and i_L is n by 1. i_L is the source function at (k, E) due to the left lead. Similarly, for waves incident from right lead, we have

$$A\Psi_D^{(R)} = i_R \tag{2.41}$$

Where i_R is the source function due to the right lead.

Matrix A is

$$A = EI - H_D - \Sigma_S - \Sigma_D \tag{2.42}$$

And the only nonzero elements in Σ_S and Σ_D are

$$\Sigma_{S}(1,1) = \frac{t_{d,l}t_{l,d}}{t_{l}}e^{ik_{l}a}$$
(2.43)

$$\Sigma_D(n,n) = \frac{t_{d,r}t_{r,d}}{t_r}e^{ik_r a}$$
(2.44)

The physical meaning of Σ_S and Σ_D is that the on-site potential at grid point 1 is shifted from ϵ_1 to ϵ_1 + $Re(\Sigma_S)$, at grid point n the on-site potential is shifted from ϵ_n to $\epsilon_n + Re(\Sigma_D)$. The scattering rate of electrons from grid point 1 of the device to the left lead is $-2Im(\Sigma_S)$, and from grid point n of the device to right lead is $-2Im(\Sigma_D)$ in the weak coupling limit. The only nonzero element of A, i_L , and i_R are

$$A(1,1) = E - \epsilon_1 - \Sigma_S(1,1) \text{ and } A(n,n) = E - \epsilon_n - \Sigma_D(n,n)$$
 (2.45)

$$A(i,i) = E - \epsilon_i \tag{2.46}$$

$$A(i, i+1) = -t_{i,i+1} \text{ and } A(i+1, i) = -t_{i,i+1}^{\dagger}$$
 (2.47)

$$i_L(1) = -2it_{d,l}\sin(k_l a)$$
 (2.48)

$$i_R(n) = -2it_{d,r}\sin(k_r a) \tag{2.49}$$

2.3.2 Self-Energy

2.3.2.1 Schottky Contact

For a nominal SBFET with effective mass approximation, we assume a uniformly distributed semiconductor with effective mass m^* and space grid a, we have

$$t_{i,i+1} = t_{i+1,i} = t = -\frac{\hbar^2}{2m^*a^2} \text{ and } \epsilon_i = -2t$$
 (2.50)

The source and drain metal lead are with the same effective mass m_t^* and same space grid a, we have

$$t_r = t_l = t_m = -\frac{\hbar^2}{2m_t^* a^2} \tag{2.51}$$

For source lead, to avoid using the bottom of the conduction band, we shift the energy down by E_{offset} , which is normally set to 1 eV or $2t_m$. According to Equation 2.40, we have

$$E - E_{offset} - 2t_m = 2t_m cos(k_l a)$$
(2.52)

For source lead we have

$$k_l a = cos^{-1} \left(1 - \frac{E - E_{offset}}{t_m}\right)$$
 (2.53)

Similarly, for drain side we have

$$k_r a = cos^{-1} \left(1 - \frac{E - E_{offset} + V_d}{t_m}\right)$$
 (2.54)

The simplest approximation for coupling between the source and device [77], and drain and device would be

$$t_{d,l} = t_{l,d} = t_{d,r} = t_{r,d} = t_m = -\frac{\hbar^2}{2m_t * a^2}$$
 (2.55)

Under this assumption, we have $\Sigma_S(1,1) = t_m e^{ik_l a}$, and $\Sigma_D(n,n) = t_m e^{ik_r a}$. Relative studies have shown that the value of m_t^* has a small effect on final results [78].

For a nominal SBFET with a tight-binding approximation, it becomes more complex. We will start from the basic form of monolayer black phosphorus along the armchair direction. As we have discussed in Chapter 2.3.1, we can eliminate the influence of two semi-infinite leads into Σ_S and Σ_D . And the only nonzero elements are $\Sigma_S(1,1)$ and $\Sigma_D(n,n)$, where n is the number of girds in the device region. For SBFET, there are no transitional areas in the device region. The semiconducting device region is directly connected to semi-infinite metal leads. We will start from the device region. The atomistic structure of each grid of monolayer BP is shown in Figure 2.14. We will use the tight-binding parameters provided in Chapter 2.1.3. The basis function for monolayer BP is one orbital for each atom. Then the size of Hamiltonian is 4 by 4 matrix. Then we will look at the Hamiltonian for metal leads. We lack the exact format of Hamiltonian of metal leads without knowing its atomics structure and its basis functions. But we will show under a certain assumption we can get Σ_S and Σ_D without knowing the exact Hamiltonian of metal leads.

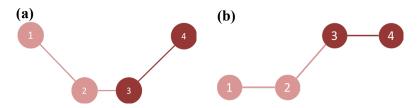


Figure 2.13 Atomistic structure of monolayer BP grid in device region in (a) top-down view, (b) side view.

Let's assume there are w atoms in one metal grid point and one orbital for each atom. Then the size of Hamiltonian would be w by w. Let's assume for the source side, the last atom of metal is connected to the first atom of BP with some coupling parameter p. We have shown that the only nonzero element in Σ_S locates in [I,I] as $\Sigma_S(1,1) = \beta^{\dagger}G_S(l1,l1)\beta$, where β is the coupling matrix of neighbor grids from BP to metal. The size of β is A by A the only coupling is between the last atom in metal and the first in BP, we have the only nonzero element locates in (w,I) in β and (I,w) in β^{\dagger} as follows,

$$\beta = \begin{bmatrix} 1 & 2 & 3 & 4 \\ 2 & & & \\ 3 & & & \\ \vdots & & & \\ y & & p \end{bmatrix}, \qquad \beta^{\dagger} = \begin{bmatrix} 1 & 2 & 3 & \cdots & \cdots & w \\ 2 & & & & \\ p & & & & \\ \end{bmatrix}$$
(2.56)

The size of $G_D(l1, l1)$ is w by w. We would have

$$\Sigma_S(1,1) = \beta^{\dagger} G_S(l1,l1) \beta$$

$$\begin{bmatrix}
1 & 2 & 3 & \cdots & \cdots & w \\
1 & 2 & 3 & \cdots & \cdots & w \\
2 & 3 & 4 & \vdots & \ddots & \vdots & 3 & 1 \\
3 & 4 & \vdots & \ddots & \vdots & 3 & 1 \\
y & \vdots & \ddots & \vdots & 3 & 1 \\
g_{Sw1} & \cdots & g_{Sww}\end{bmatrix} \begin{bmatrix}
g_{S11} & \cdots & g_{S1w} \\
\vdots & \ddots & \vdots & \vdots \\
g_{Sw1} & \cdots & g_{Sww}\end{bmatrix} \begin{bmatrix}
\vdots & \vdots & \ddots & \vdots \\
\vdots & \vdots & \ddots & \vdots \\
\vdots & \vdots & \ddots & \vdots \\
y & \vdots & \vdots & \ddots & \vdots \\
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y & \vdots & \vdots & \vdots & \ddots & \vdots \\
y & \vdots &$$

In this way, we prove the only nonzero element in $\Sigma_S(1,1)$ locates in [1,1]. Similarly, for the drain side, we assume the last atom in BP is connected to the first atom in metal. As the only nonzero element in Σ_D locates in [n,n] as $\Sigma_D(n,n) = \beta G_D(r1,r1)\beta^{\dagger}$, we have

$$\Sigma_{D}(n,n) = \beta G_{D}(r1,r1)\beta^{\dagger}$$

$$= \frac{1}{2} \begin{bmatrix} 1 & 2 & 3 & \cdots & \cdots & w \\ 1 & 2 & 3 & \cdots & \cdots & w \\ 2 & 3 & 4 & \vdots & \ddots & \vdots \\ q_{Dw1} & \cdots & q_{Dww} \end{bmatrix} \begin{bmatrix} 1 & 2 & 3 & 4 \\ 2 & 3 & \vdots \\ \vdots & \ddots & \vdots \\ y_{Dw1} & \cdots & q_{Dww} \end{bmatrix} \begin{bmatrix} 1 & 2 & 3 & 4 \\ \vdots & \ddots & \vdots \\ w & \vdots & \ddots & \vdots \\ q_{QD11}q \end{bmatrix}$$

$$(2.58)$$

We have converted the unknown matrix β , $G_D(l1, l1)$ and $G_S(r1, r1)$ into two unknown parameters $pg_{Sww}p$ and $qg_{D11}q$. In this way, we get Σ_S and Σ_D . The value of $pg_{Sww}p$ and $qg_{D11}q$ reflect the contact quality between metal and semiconductor. For example, if we use the rectangular supercell shown in Figure 2.14 as the building block for a monolayer BP SBFET. Then at the leftmost side of the channel, atom 1 is connected to source metal; at the rightmost side, atom 4 is connected to drain metal. The continuous carrier injection from metal to BP channel is modeled by self-energy matrix

$$\Sigma_{S} = -i \begin{bmatrix} t_{0} \\ \\ \\ \end{bmatrix}, \Sigma_{D} = -i \begin{bmatrix} \\ \\ \\ \\ t_{0} \end{bmatrix}$$
 (2.59)

Where there's the only nonzero element at the left top corner for Σ_S and right bottom corner for Σ_D . The t_0 value determines the contact quality, and a commonly adopted value is around 2 eV [79].

Besides the self-energy matrix, additional modifications should be addressed in the settings of Poisson equations. We need to change the boundary condition for source-semiconductor and drain-semiconductor interface to fixed boundary conditions. For the source side, the potential should be fixed to Φ_{Bn} and for the drain side, the potential should be fixed to Φ_{Bn} . This will be discussed in later chapters.

2.3.2.2 Ohmic Contact

For Ohmic contact devices, we assume semi-infinite leads at source and drain with heavily doping. The device can also be divided into three parts. However, for Ohmic contact devices, the simulated device region consists of two transition regions near the source and drain and the channel region in the middle. The transition regions play an important role, and it should be sufficiently long that the potential can smoothly

drop and match with μ_S and μ_D . The semi-infinite source and drain can be eliminated by a certain process as follows.

We first consider a device with just drain and device region. The interactions from device to drain can be described by the matrix τ (size n × rn), then the interactions from drain to device is τ^{\dagger} (size rn × n). We have

$$G_{tot} = \begin{bmatrix} G & G_{dD} \\ G_{Dd} & G_D \end{bmatrix} = \begin{bmatrix} (E+i0^+)I - H & -\tau \\ -\tau^+ & (E+i0^+)I_D - H_D \end{bmatrix}^{-1}$$
(2.60)

Where H_D is the Hamiltonian of the semi-infinite drain in size rn × rn, I_D is an identity matrix same size as H_D , 0^+ is infinitesimal number gives rise to a finite broadening. In this way, we can write G in the form as follows:

$$G = [(E + i0^{+})I - H - \Sigma_{D}]^{-1} = [(E + i0^{+})I - H - \tau G_{D}\tau^{+}]^{-1}$$
(2.61)

where $\Sigma_D = \tau G_D \tau^{\dagger}$. If we assume interaction only exits between two neighbor grids, the hopping matrix t_{dr} (size determined by the basic function of each grid) between grid n in the device region and r1 in the semi-infinite right lead region can be described by β . Then the only nonzero element in τ locates at [n, 1]. The nonzero element in τ^{\dagger} locates in [1, n] as follows

$$\tau = \begin{pmatrix} 0 & \cdots & 0 \\ \vdots & \ddots & \vdots \\ \beta & \cdots & 0 \end{pmatrix}, \tau^{\dagger} = \begin{pmatrix} 0 & \cdots & \beta^{\dagger} \\ \vdots & \ddots & \vdots \\ 0 & \cdots & 0 \end{pmatrix}$$
 (2.12)

In this way, the only nonzero element in Σ_D locates in [n, n] as $\Sigma_D(n,n) = \beta G_D(r1,r1)\beta^{\dagger}$. Now we need to solve the surface Green's function g_{s_s} which is $G_D(r1,r1)$. We can use Equation 2.16 to assume that

$$g_s^{new} \approx g = [(E + i0^+)I - a - U_N - \beta g_s^{old} \beta^{\dagger}]^{-1}$$
 (2.63)

Where a is self-energy of the grid in the device region, U_N is the potential at grid n in the device region obtained from Poisson's Equations. Usually, Equation 2.68 start with an initial guess of $g_s^{old} = [(E+i0^+)I - a - U_N]^{-1}$. Once $|g_s^{new} - g_s^{old}| < 10^{-10}$, we can assume this is the converged result for surface Green's function. In this way, we can get Σ_D for NEGF simulation.

The same method can be applied to source side semi-infinite lead. The Green's function can be written as

$$G = [(E + i0^{+})I - H - \Sigma_{S}]^{-1} = [(E + i0^{+})I - H - \tau^{\dagger}G_{S}\tau]^{-1}$$
(2.64)

where $\Sigma_S = \tau^{\dagger} G_S \tau$, G_S is the Green's function for semi-infinite source lead, the hopping matrix from device to source is τ^{\dagger} (size n × ln), and the hopping matrix from source to the device is τ (size ln × n). With the assumption that interaction only happens between neighbor grids which are β , we have $\Sigma_S(1,1) = \beta^{\dagger} G_S(l1,l1)\beta$, the rest are zero. Similarly, the surface Green's function at the source side can be achieved by

$$g_s^{new} \approx g = [(E + i0^+)I - a - U_1 - \beta^{\dagger} g_s^{old} \beta]^{-1}$$
 (2.65)

Where a is self-energy, U_l is the potential at grid 1 in the device region. The initial guess is usually $g_s^{old} = [(E + i0^+)I - a - U_1]^{-1}$. Once $|g_s^{new} - g_s^{old}| < 10^{-10}$, we can get a converged Σ_s for NEGF simulation.

2.3.3 Electron and Current Densities in Terms of Green's Function

The Green's function corresponding to Schrodinger's equation for the device and leads is

$$[E - H + i\eta]G = I \tag{2.66}$$

where η is an infinitesimally small positive number that pushes the poles of G to the lower half-plane in complex energy, and H is the Hamiltonian. This equation is usually written in another form as

$$[EI - H_D + \Sigma_{lead}]G = I \tag{2.67}$$

The wave functions in device region due to waves incident from source and drain can be written as

$$\Psi_{Device}^{S} = Gi_{S} \tag{2.68}$$

$$\Psi_{Device}^{D} = Gi_{D} \tag{2.69}$$

Only two columns G(:, 1) and G(:, n) are necessary for device simulation as i_S and i_D are nonzero only at grid points 1 and n. With the wavefunctions, we can get the electron density in real space as

$$n(x) = \int \left[\left| \Psi_{Device}^{S}(x) \right|^{2} f_{S}(E) + \left| \Psi_{Device}^{D}(x) \right|^{2} f_{D}(E) \right] dk \tag{2.70}$$

The detailed derivations will be omitted. For device simulations, the electron density at grid point q can be expressed as

$$n_q = 2 \int \frac{dE}{2\pi} G(E) \Sigma_{lead}^{in}(E) G^{\dagger}(E) \Big|_{q,q}$$
 (2.71)

where Σ_{lead}^{in} is a sparse matrix with only nonzero elements at

$$\Sigma_{lead\ 1.1}^{in}(E) = \Sigma_{S}^{in}(E) \tag{2.72}$$

$$\Sigma_{lead\ n.n}^{in}(E) = \Sigma_D^{in}(E) \tag{2.73}$$

Where the in-scattering self-energy matrix due to source and drain can be written as

$$\Sigma_S^{in}(E) = -2Im[\Sigma_S(E)]f_S(E) \tag{2.74}$$

$$\Sigma_D^{in}(E) = -2Im[\Sigma_D(E)]f_D(E) \tag{2.75}$$

Where f_S and f_D are the Fermi distribution in source and drain, Σ_S and Σ_D are the self-energy matrix discussed before, which depends on whether the device is Ohmic contact or Schottky contact, and whether effective mass approximation or TB approximation has been assumed.

The current density between two grid points q and q + 1 per unit energy can also be derived from the device wavefunction as

$$J_{q \to q+1}(E) = \frac{e\hbar}{2mai} 2 \left[\left(\Psi_q^{S^{\dagger}} \Psi_{q+1}^S - \Psi_{q+1}^{S^{\dagger}} \Psi_q^S \right) f_S(E) + \left(\Psi_q^{D^{\dagger}} \Psi_{q+1}^D - \Psi_{q+1}^{D^{\dagger}} \Psi_q^D \right) f_D(E) \right]$$
(2.76)

Again, the detailed derivations are omitted. The current density can be expressed as

$$J_{q \to q+1} = \frac{e\hbar}{2mai} 2 \int \frac{dE}{2\pi} \left[G(E) \Sigma_{lead}^{in}(E) G^{\dagger}(E) \Big|_{q,q+1} - G(E) \Sigma_{lead}^{in}(E) G^{\dagger}(E) \Big|_{q+1,q} \right]$$
(2.77)

2.3.4 Overview of Non-equilibrium Green's Function (NEGF) Methods

In previous chapters, quantum transport simulations are discussed under the assumption of the 1D atomic chain. This is the foundation of NEGF simulations and can be expanded to 2D or 3D simulation by replacing H matrix accordingly. In this chapter, we will briefly summarize the NEGF in a generalized form of formalism under non-equilibrium bias. From the retarded Green's function at given energy [80], we have

$$G(E) = [EI - H - \Sigma_S - \Sigma_D]^{-1}$$
 (2.78)

where I stands for identity matrix. The Fermi distribution of source and drain are:

$$f_S(E) = \frac{1}{\exp\left(\frac{E - \mu_S}{k_B T}\right) + 1}$$
 (2.79)

$$f_D(E) = \frac{1}{\exp\left(\frac{E - \mu_D}{k_B T}\right) + 1}$$
(2.80)

The total spectral function [A] can be described by:

$$[A] = i[G - G^{+}] = [A_{1}] + [A_{2}]$$
(2.81)

where $A_1 = G\Gamma_1G^+$ and $A_2 = G\Gamma_2G^+$. The Γ_1 and Γ_2 can be described as $\Gamma_1 = i[\Sigma_S - \Sigma_S^+]$ and $\Gamma_2 = i[\Sigma_D - \Sigma_D^+]$. It describes the broadening matrices to the source and drain. The correlation function can be expressed as

$$[G^n] = [A_1]f_S + [A_2]f_D (2.82)$$

The density matrix can be written in the form of

$$[\rho] = \frac{1}{2\pi} \int G^n(E) dE \tag{2.83}$$

This gives the information we need to start the loop for Poisson's equations, which in turn gives us a new potential for NEGF input. The details will be explained later. Once we got the self-consistent result, the current per spin can be expressed as

$$\widetilde{I_{S/D}} = Trace \left[\Gamma_{1/2} A\right] f_{S/D} - Trace \left[\Gamma_{1/2} G^n\right]$$
(2.84)

The current at the terminal can be written as

$$I_{S/D} = -\frac{q}{h} \int \widetilde{I_{S/D}} \, dE \tag{2.85}$$

Where q and h are the free electron charge and the Planck's constant, respectively.

2.4 Electrostatics

2.4.1 Self-consistent Simulation

Within the NEGF formalism discussed above, we usually describe the device by three parts: source, drain, and channel. The source and drain parts are regarded as two infinite reservoirs and coupled to channel described by self-energy matrices, Σ_S and Σ_D . The Fermi levels of source and drain, μ_S and μ_D are controlled by the applied voltage. The channel region is represented by Hamiltonian H. Incoherent carrier transport due to scattering can be described by self-energy Σ_{Scat} . To discretize above operators, the effective-mass (EM) or tight-binding (TB) approximation can be adopted. Mode space representation is usually adopted instead of three-dimensional real space simulation to reduce the computational cost by minimizing the size of the operator matrices. With the above information, the transmission coefficient at a given energy (T(E)), electron density (ρ), and current (I) can be computed self-consistently with Poisson's equation. The general procedures consist following steps [81]:

- (1). The finite Difference Method (FDM) is chosen to discretize all operators for a given device.
- (2). An initial guess of self-consistent potential $U_{SC}(\vec{r})$ is given to start the self-consistent loop.
- (3). With initial $U_{SC}(\vec{r})$, the device Hamiltonian H can be written according to the approximation we adopted (EM or TB). The Σ_S and Σ_D can also be computed.
- (4). The density matrix is calculated through the retarded Green's function.
- (5). The charge density (ρ) of the device can be obtained by a density matrix, which will be passed to Poisson equations to solve the new self-consistent potential $U_{SC}(\vec{r})$.
- (6). Step (3) to (5) are iterated until the results reach our criteria.
- (7). The current can be calculated from the converged self-consistent potential and density matrix.

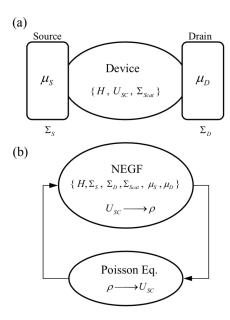


Figure 2.14 (a) Schematic structure of device coupled to the source and drain contacts. (b) Self-consistent simulation scheme between NEGF and Poisson [82].

2.4.2 Overview of Electrostatics Calculation

In this section, we will briefly review the steps to get the numerical solutions for Poisson's Equation. The FDM method is used for solving general double-gate MOSFET structure. Figure 2.16(a) shows the device structure with schematic uniformly spaced grids. The naming of girds is showing in Figure 2.16(b).

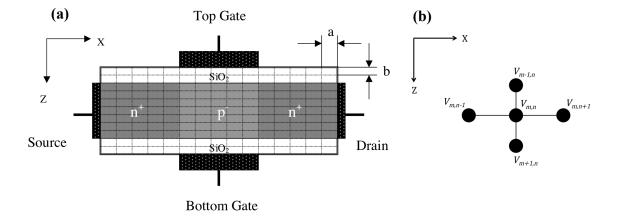


Figure 2.15 (a) A schematic of double-gate MOSFET structure in the 2D simulation domain. Uniformly spaced grids are used in both X and Z directions with spatial constants a and b, respectively [81]. (b) Computational molecule for the 5-pointed star.

First, we assume the semiconductor has the same dielectric constant as the insulating layer. The numeric solution to the Poisson equation can be obtained by Gauss's law

$$\nabla \cdot \boldsymbol{D}(\boldsymbol{r}) = \rho(\boldsymbol{r}) \tag{2.86}$$

Where D, r, and ρ stand for electric flux density, position vector, and charge density, respectively. Since we assume a uniform distributed dielectric material, according to constitutive relation, we have $D(r) = \varepsilon_0 \varepsilon_r E(r)$, where ε_0 is the permittivity of vacuum, ε_r is the dielectric constant of semiconductor and insulating layer and E(r) is the electric field function. And we know $E(r) = -\nabla \cdot V(r)$, where V(r) is the space potential function, the former equation can be written as

$$\nabla^2 \mathbf{V}(\mathbf{r}) = -\frac{\rho(\mathbf{r})}{\varepsilon_0 \varepsilon_r} \tag{2.87}$$

As we have shown in Figure 2.2, \boldsymbol{a} and \boldsymbol{b} are the mesh spacings along \boldsymbol{X} and \boldsymbol{Z} directions, respectively. And $V_{m,n}$ is the potential at gird [m, n]. The solution domain consists of N_X nodes along \boldsymbol{X} direction and N_Z nodes along \boldsymbol{Z} direction. A 2D numerical solution to the Poisson equation should be in the size of $N_X \times N_Z$. In this way, the same number of equations are needed. We rewrite Equation (2.87), and at grid [m, n] we have

$$\frac{\partial^2 V_{m,n}}{\partial x^2} + \frac{\partial^2 V_{m,n}}{\partial z^2} = -\frac{\rho_{m,n}}{\varepsilon_0 \varepsilon_r}$$
 (2.88)

where $\rho_{m,n}$ is the charge density at node [m, n]. Equation (2.88) can be rewritten using FDM as

$$\frac{V_{m,n+1} - 2V_{m,n} + V_{m,n-1}}{a^2} + \frac{V_{m+1,n} - 2V_{m,n} + V_{m-1,n}}{b^2} = -\frac{q(p-n+N_D-N_A)_{m,n}}{\varepsilon_0 \varepsilon_r}$$
(2.89)

Where p is the hole concentration and n is the electron concentration, N_D and N_A are donor and acceptor concentrations, q is the elementary charge. Ans it can be simplified as

$$\frac{a}{b}V_{m-1,n} + \frac{b}{a}V_{m,n-1} - 2(\frac{a}{b} + \frac{b}{a})V_{m,n} + \frac{b}{a}V_{m,n+1} + \frac{a}{b}V_{m+1,n}$$

$$= \frac{ab}{\varepsilon_0\varepsilon_r}q(p-n+N_D-N_A)_{m,n}$$
(2.90)

According to the doping of semiconductors, n or p can be neglected in fully depleted ultra-thin body MOSFET.

Next, we will consider more realistic situations. As shown in Figure 2.16(a), the dielectric constant of semiconductor and oxide layer most times are different. The discontinuity of ε_r should be considered. If node [m,n] is within the oxide regions or the semiconductor regions, we have $\varepsilon_r = \varepsilon_{ox}$ or $\varepsilon_r = \varepsilon_{SC}$. In case that the node is positioned at the SC/Oxide interface, Equation (2.90) is rewritten as

$$\frac{a}{b}\varepsilon_{Top}V_{m-1,n} + \frac{b}{a}\left(\frac{\varepsilon_{Top} + \varepsilon_{Bot}}{2}\right)V_{m,n-1} - 2\left(\frac{a}{b} + \frac{b}{a}\right)\left(\frac{\varepsilon_{Top} + \varepsilon_{Bot}}{2}\right)V_{m,n} + \frac{b}{a}\left(\frac{\varepsilon_{Top} + \varepsilon_{Bot}}{2}\right)V_{m,n+1} + \frac{a}{b}\varepsilon_{Bot}V_{m+1,n} = \frac{ab}{\varepsilon_0}q(p-n+N_D-N_A)_{m,n}$$
(2.91)

where ε_{Top} and ε_{Bot} are dielectric constants for the materials above and below the interface.

Next, we will consider the boundary conditions for the nodes. At the gate contact, the gate potential is fixed as $V = V_G$, so Dirichlet boundary conditions should be specified. The numerical equation to be satisfied at the interface between oxide and top/bottom gate is $V_{m,n} = V_G$, where V_G is determined by the gate bias and the work function of the metal.

However, in ballistic simulations, we impose floating boundary conditions for the rest boundaries to solve the Poisson equation. This boundary condition is by assuming $n \cdot \nabla V = 0$ at the end of the simulation region of source and drain, where n is the surface unit normal vector. It looks contrary to the scattering-dominated simulations where we assume fixed boundary conditions at the source and drain based on equilibrium statistics to obtain charge neutrality. Here in the ballistic case, at high V_{DS} , the source injected carriers are partially exhausted due to the drain injected carriers are suppressed. In this way, it's better to impose a zero-field boundary condition instead of fixing the potential. In order to obtain macroscopic charge neutrality, the potential will float to the correct value according to μ_S and μ_D provided in NEGF. The boundary conditions are as follows:

 $V_{m,n} - V_{m\pm 1,n} = 0$ for the top and bottom edges excepted the gate covered region,

 $V_{m,n} - V_{m,n+1} = 0$ for the left and right edge,

 $2V_{m,n} - (V_{m+1,n} + V_{m,n\pm 1}) = 0$ for the two corner nodes along the top edge,

 $2V_{m,n} - (V_{m-1,n} + V_{m,n\pm 1}) = 0$ for the two corner nodes along the bottom edge.

To this point, we have $N_X \times N_Z$ equations to solve V_{mn} . A certain algorithm can be applied to speed up the simulation. The self-consistent result of all grids can be solved in each iteration. However, only the potential of the semiconductor region is needed for NEGF simulation. For example, a monolayer MOSFET structure has [H] in size of $MN_X \times MN_Z$, where M is the number of the basis for each grid. The potential we solved from Poisson's equations for semiconductor layer is in size of $N_X \times 1$. We will assume in each individual grid has a constant potential, and it becomes in size $MN_X \times 1$. We put it in diagonal of a matrix which is U_{SC} . And we can get $H = H_0 + U_{SC}$ which feeds back to NEGF sections and start a new loop till we get converged results.

2.4.3 Electrostatics Calculation for Hetero-structure

For a hetero-junction device, some additional assumptions are made. A schematic device structure of double gate top contact 1T-2H MoS₂ heterojunction is shown in Figure 2.16. Here we use a denser grid with a = 2dx and c = 2dz. To mimic the situation where metallic 1T MoS₂ is used as leads instead of conventional metal, a fixed boundary condition is assumed at the left end of source 1T MoS₂ and right end of drain 1T MoS₂. Spacing oxide is assumed below extended 1T leads. In the channel region, 2H MoS₂ is sandwiched by the top and bottom gate oxide. At all these heterojunction interfaces, the effects of different permittivity materials need to be addressed carefully.

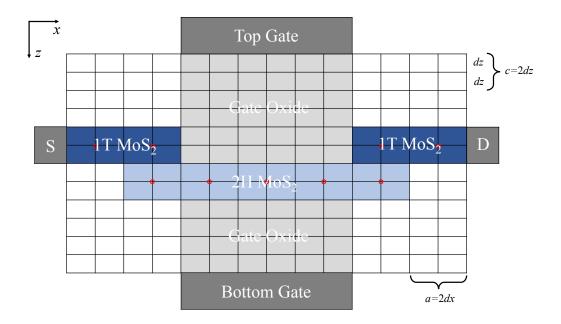


Figure 2.16 A schematic of double-gate MOSFET structure for top contact 1T-2H heterojunctions. Uniformly spaced grids are used in both x and z directions with spatial constants dx and dz, respectively. The red dots indicate grids in NEGF simulations.

A more generalized five-point star with different permittivity materials is shown in Figure 2.17. We have

$$\nabla \cdot [\epsilon(\mathbf{r})\nabla V(\mathbf{r})] = \nabla \cdot \left\{ \epsilon(\mathbf{r}) \left[\frac{\partial V(\mathbf{r})}{\partial x} + \frac{\partial V(\mathbf{r})}{\partial z} \right] \right\} = -\frac{\rho(\mathbf{r})}{\epsilon_0}$$
 (2.92)

Which can be expanded to

$$\frac{1}{2a} \left[\frac{\epsilon_{2} (V_{m,n+1} - V_{m,n})}{a} - \frac{\epsilon_{1} (V_{m,n} - V_{m,n-1})}{a} \right] + \frac{1}{2a} \left[\frac{\epsilon_{4} (V_{m,n+1} - V_{m,n})}{a} - \frac{\epsilon_{3} (V_{m,n} - V_{m,n-1})}{a} \right] + \frac{1}{2c} \left[\frac{\epsilon_{3} (V_{m+1,n} - V_{m,n})}{c} - \frac{\epsilon_{1} (V_{m,n} - V_{m-1,n})}{c} \right] + \frac{1}{2c} \left[\frac{\epsilon_{4} (V_{m+1,n} - V_{m,n})}{c} - \frac{\epsilon_{2} (V_{m,n} - V_{m-1,n})}{c} \right] = -\frac{\rho(r)}{\epsilon_{0}}$$
(2.93)

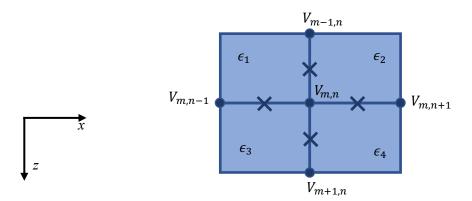


Figure 2.17 Finite-difference mesh for the generalized Poisson equation. Each blue square represents a region of constant dielectric permittivity. The rectangular mesh has a width of a and height of c.

Besides the adjusted Poisson equations, another thing that needs to be considered carefully is the permittivity of metallic 2D material 1T MoS₂. In conventional MOSFET, we assume the potential of metal is constant, which means infinite large permittivity. However, for the 2D metal in nanometer scale, things need to be considered carefully. This will be discussed in later chapters.

Chapter 3

Assessment of High-Frequency Performance Limit of Black Phosphorus Field-Effect Transistors

3.1 Motivation

2D materials are very intriguing for next-generation electronic devices due to their unique physical properties such as compelling electrical characteristics, large immunity to aggressive scaling, excellent optical and mechanical properties. For more than a decade, graphene has been explored extensively, and it turned out that graphene is promising for radio-frequency (RF) applications [83] rather than switching devices, mainly due to its ultra-high carrier mobility (\sim 10,000 cm²V⁻¹s⁻¹) [84] and high saturation velocity ($> 3\times10^7$ cm s⁻¹) [85] yet inherently large leakage current. Graphene field-effect transistors (FETs) exhibit as comparably high cutoff frequency (f_T) as state-of-the-art InAs high-electron-mobility transistors(HEMTs) and GaAs metamorphic HEMTs [83], [86], [87], although III-V semiconductors (\sim 1 THz) [88] still outperform graphene FETs. The f_T of graphene FET (GFET) can reach a few hundred GHz when channel length scales down below 100 nm [10]. However, the unity power gain frequency (f_{max}) of GFETs is significantly limited due to its poor saturation behavior of drain current. The highest reported f_{max} is \sim 50 GHz, which is far less than f_T [11]. Moreover, its large output conductance (g_d) also significantly limits the intrinsic voltage gain of GFETs. To overcome such limitations, a large bandgap, as well as high carrier mobility, would be required. And black phosphorus (BP) can be an outstanding contender for high-frequency applications among many 2D materials.

Black phosphorus is a layered material with high hole mobility (10,000 cm²V⁻¹s⁻¹) and a thickness-dependent direct bandgap ranging from 0.3 eV (bulk) to 2 eV (monolayer) [25], [89]. Even at its early stage, BP FETs have demonstrated high field-effect mobility (~1,000 cm²V⁻¹s⁻¹) and a high on-off current ratio (>10⁵) [26], [90], which are critically important not only for high-performance logic circuits but also for high-frequency applications. Recently, gigahertz frequencies ($f_T = 17.5 \text{ GHz}$; $f_{max} = 14.5 \text{ GHz}$) have been reported with BP FETs on a bendable substrate [91], [92]. However, the performance of BP FETs is currently limited by various factors. For example, the source/drain contact resistance ($R_{S/D}$) of BP FETs is relatively high (~5 k Ω · μ m) [92] compared to that of GFETs, for which $R_{S/D} = 0.1 \text{ k}\Omega$ · μ m was reported [93], [94]. Gate resistance (R_G) can be another limiting factor for f_{max} , and parasitic resistance (C_P) can also significantly affect the extrinsic performance of the device negatively [95]. As the high-frequency performance limit of BP FETs has remained unexplored yet, it would be worth investigating BP FETs based on rigorous models, and numerical simulations before more extensive experimental efforts will be made.

In this study, we investigate the high-frequency performance limit of BP FETs using self-consistent quantum transport simulations and the small-signal circuit model. We thoroughly explore the effects of various device parameters on f_T and f_{max} by varying equivalent oxide thickness (EOT), channel length (L_{ch}), device width (W), R_G , $R_{S/D}$ and C_P . Our simulation results reveal that BP FETs can exhibit as good f_T as GFETs. Furthermore, f_{max} of BP FETs is not limited, unlike that of GFETs, enabling near THz frequencies for both f_T and f_{max} with proper engineering. Our benchmark against experimental data indicates that there exists huge room for optimization to boost the high-frequency performance of BP FETs, particularly with channel length scaling.

3.2 Approach

3.2.1 Device Structure

Figure 3.1 (a) shows a schematic device structure of a simulated BP FET. Monolayer BP is used for the channel as it can provide better performance than multilayer BP in the conventional FET structure[96]. A single-gate device structure is considered following the recent experimental demonstrations, and Al_2O_3 (κ = 9) is used for the gate oxide [92], [97]. For a nominal device, we set the following device parameters: 15-nm channel length and 3-nm-thick gate dielectric (equivalent oxide thickness of EOT = 1.3 nm). Source and drain extensions are p-doped, where Ohmic contact is achieved with a doping concentration of 1.3×10^{13} cm⁻². We assume that metal electrodes are deposited, as shown in Fig. 3.1(a). Device parameters such as channel length, contact resistance, and parasitic capacitances will be varied to explore their impacts on the device performance.

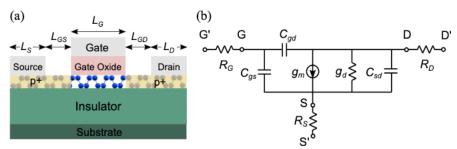


Figure 3.1 (a) Device structure of simulated black phosphorus (BP) field-effect transistor (FET). Monolayer BP is used for the channel, and the source/drain is p-doped, forming an Ohmic contact. Single-gate geometry is used. (b) Small-signal equivalent circuit of the BP FET. g_m and g_d are the transconductances and the output conductance; R_G , R_S , and R_D are the gate resistance, the source, and the drain contact resistance, respectively; C_{gs} , C_{gd} , and C_{sd} are the small-signal gate-to-source, the gate-to-drain, and the source-to-drain capacitance, respectively [98].

3.2.2 Numerical Simulations

Transport properties of BP FETs are simulated based on the non-equilibrium Green's function (NEGF) formalism within a tight-binding (TB) approximation, self-consistently with the Poisson's equation[80]. To accurately describe electronic states of monolayer black phosphorus, five TB parameters ($t_1 = -1.220 \text{ eV}$, $t_2 = 3.665 \text{ eV}$, $t_3 = -0.205 \text{ eV}$, $t_4 = -0.105 \text{ eV}$, $t_5 = -0.055 \text{ eV}$) are used in the Hamiltonian matrix [73]. Considering the anisotropic nature of the band structure of black phosphorus, we took the armchair orientation for the transport direction due to its light hole effective mass ($m_{hx} = 0.19m_{\theta}$) for the p-type conduction. Ballistic transport is assumed considering relatively short channel length with NEGF simulations, and the effect of scattering is treated separately based on the Landauer-Lundstrom-Datta model [99] in section 3.3.6. The large dimension of the device width is treated by a mode space approach with a periodic boundary condition. Charge density and current are calculated by using the numerical summation of the transverse momentum. Therefore, device characteristics such as current and transconductance are given per unit width, with which different widths of devices (*e.g.*, 1 µm or 10 µm) are considered. The open boundary condition is treated by contact self-energies [100]. Power supply voltage of $V_{DD} = 0.5 \text{ V}$ is used, and the room temperature is assumed.

3.2.3 Equivalent Small-Signal Circuit Model

Quasi-static treatment is used to assess high-frequency performance following standard procedures [101]. The steady-state channel charge (Q_{ch}) and drain current (I_D) are computed by performing self-consistent DC simulations. The intrinsic gate capacitance (C_{gg}) and transconductance (g_m) are extracted from the I_{D} – V_G characteristics as

$$C_{gg} = \frac{\partial Q_{ch}}{\partial V_G}\Big|_{V_D}, \quad g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D}.$$
 (3.2)

Similarly, intrinsic gate-to-drain capacitance (C_{gd}) and the output conductance (g_d) can be extracted from the I_D – V_D characteristics as

$$C_{gd} = -\frac{\partial Q_{ch}}{\partial V_D}\Big|_{V_C}, \quad g_d = \frac{\partial I_D}{\partial V_D}\Big|_{V_C}.$$
 (3.3)

Then, we can obtain gate-to-source capacitance as

$$C_{gs} = C_{gg} - C_{gd}. (3.4)$$

In this study, the main interest lies in cutoff frequency (unity current gain frequency) f_T and unity power gain frequency f_{max} of BP FETs. The intrinsic f_T can be calculated as

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{3.5}$$

and intrinsic f_{max} is given by

$$f_{max} = \frac{f_T}{2\sqrt{g_d R_G + 2\pi f_T C_{gd} R_G}},$$
 (3.6)

where R_G is the gate resistance and it can be determined by

$$R_G = \alpha R_{SHG} \frac{W}{L} \times \frac{1}{N}. \tag{3.7}$$

 R_{SHG} is the gate sheet resistance of metal gate being related to the gate metal's resistivity (ρ_G) and thickness (Λ_G) as $R_{SHG} = \frac{\rho_G}{\Lambda_G}$. α is 1/3 when the gate terminal is brought out from one side, and 1/12 when connected to both sides. W and L are the width and the length of gate metal per finger, respectively. N is the number of fingers. We assumed that the gate metal is connected from one end $(\alpha = 1/3)$ and a single finger structure is used (N = 1) for the nominal device.

In practical devices, f_T and f_{max} can be significantly limited by other device parameters such as source/drain contact resistance and parasitic capacitances. The extrinsic f_T is calculated as

$$f_T = \frac{g_m}{2\pi \{C_{gg,t}[1 + g_d(R_S + R_D)] + C_{gd,t}g_m(R_S + R_D)\}}$$
(3.8)

and the extrinsic f_{max} is given as

$$f_{max} = \frac{g_m}{4\pi\sqrt{\Psi_1 + \Psi_2 + \Psi_3}} \tag{3.9}$$

where Ψ_1 , Ψ_2 and Ψ_3 are

$$\Psi_1 = R_G \left[(R_S + R_D) (C_{gg,t} g_d + C_{gd,t} g_m)^2 + C_{gg,t} (C_{gg,t} g_d + C_{gd,t} g_m) \right]$$
(3.10)

$$\Psi_2 = R_D \left[R_S (C_{gg,t} g_d + C_{gd,t} g_m)^2 + C_{gd,t} (C_{dg,t} g_d + C_{dd,t} g_m) \right]$$
(3.11)

$$\Psi_{3} = R_{S} \left[g_{m} (C_{gg,t} - C_{gd,t}) (C_{gd,t} - C_{dd,t}) + g_{d} (C_{gg,t} - C_{gd,t}) (C_{gg,t} - C_{dg,t}) \right]$$
(3.12)

and the capacitance with subscript t is the total capacitance considering various parasitic components:

$$C_{gg,t} = C_{gg} + C_{gd,p} + C_{gs,p} (3.13)$$

$$C_{gd,t} = C_{gd} + C_{gd,p} (3.14)$$

$$C_{dg,t} = C_{dg} + C_{dg,p} \tag{3.15}$$

$$C_{dd,t} = C_{dd} + C_{dg,p} + C_{ds,p} (3.16)$$

The intrinsic capacitances of C_{dg} and C_{dd} are determined by

$$C_{dg} = -\frac{\partial Q_D}{\partial V_{GS}}, C_{dd} = \frac{\partial Q_D}{\partial V_{DS}}, \tag{3.17}$$

where we treat C_{dg} and C_{dd} being zero as the variation of charge inside the drain is negligible. Based on a planar MOSFET structure, we estimate C_p induced by the contacts as:

$$C_{gs,p} = (\epsilon_S + \epsilon_0)W \times \frac{K\left(\sqrt{1 - k_{gs}^2}\right)}{K(k_{gs})}, k_{gs} = \sqrt{\frac{L_{GS}}{L_{GS} + L_G}}$$
(3.18)

$$C_{gd,p} = C_{dg,p} = (\epsilon_S + \epsilon_0)W \times \frac{K\left(\sqrt{1 - k_{gd}^2}\right)}{K(k_{gd})}, k_{gd} = \sqrt{\frac{L_{GD}}{L_{GD} + L_G}}$$
(3.19)

$$C_{ds,p} = (\epsilon_S + \epsilon_0)W \times \frac{K\left(\sqrt{1 - k_{ds}^2}\right)}{K(k_{ds})}, k_{ds} = \sqrt{\frac{(2L_S + L_{DS})L_{DS}}{(L_S + L_{DS})^2}}$$
(3.20)

where ϵ_S and ϵ_0 are dielectric constant of semiconductor and air, respectively, L_G is the gate length, and K(k) is the complete elliptic integral of the first kind, defined as

$$K(k) = \int_0^1 \frac{dw}{(1 - w^2)^{1/2} (1 - k^2 w^2)^{1/2}}$$
(3.21)

The inductance of contact is ignored in the small-signal circuit as its impact is negligible compared to those of contact resistance and parasitic capacitance [101]–[104].

3.3 Results

3.3.1 Transfer and Output Characteristics of BP FETs

First, we have plotted the intrinsic transfer and output characteristics of the nominal device based on the self-consistent NEGF quantum transport simulations. Figure 3.2(a) shows the I_D – V_G characteristics of the BP FET at V_D = -0.5 and -0.7 V in linear scale (left axis) and logarithmic scale (right axis). It exhibits large on current ($I_{on} > 1.5$ mA/ μ m), large transconductance ($g_m \sim 6.4$ mS/ μ m), large on/off current ratio (I_{on}/I_{off} reaches 4.8×10^7 and 1.8×10^{10} at V_{DD} = -0.5 V and -0.7 V, respectively), and excellent switching characteristics with a small subthreshold swing (SS = 64.8 mV/dec). One of the main advantages of monolayer BP over graphene is the presence of a large bandgap, which enables a clear saturation behavior in I_D – V_D characteristics, as shown in Fig. 3.2(b). Output conductance of g_d = 147 μ S/ μ m and 62 μ S/ μ m are achieved at V_G = -1 V and -0.8 V, respectively, even with a short channel length (15 nm).

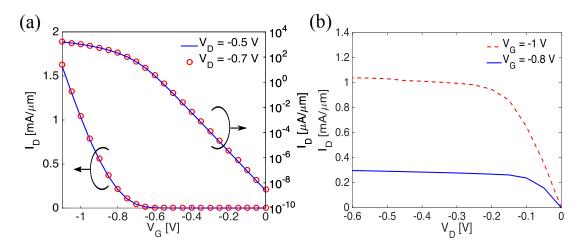


Figure 3.2 (a) I_D – V_G characteristics of a nominal BP FET at V_D = -0.5 and -0.7 V. (b) I_D – V_D characteristics of the same device at V_G = -0.8 and -1 V [98].

3.3.2 Effect of EOT

In general, the efficiency of gate control is critical for the device performance of field-effect transistors [96]. Higher gate efficiency can be realized in various manners: by using double-gate geometry, high- κ dielectric, or thinner gate oxide. For switching devices, smaller EOT is generally preferred for steep subthreshold slope, large I_{on}/I_{off} and large g_m . However, it could be different for high-frequency applications, and therefore, we investigate the effect of EOT on the intrinsic f_T by varying it from 0.5 to 25 nm. Since the intrinsic f_T is a function of transconductance and gate capacitance, g_m and C_{gg} are plotted in Fig. 3.3(a) and 3.3(b), respectively, where both increase as EOT is scaled down. Figure 3.3(c) shows the intrinsic f_T as a function of EOT, and the peak value of 5.7 THz is achieved at EOT = 5 nm. Therefore, in the subsequent discussion, we will use EOT = 5 nm to evaluate the high-frequency performance of BP FETs. It should be noted that the peak value of intrinsic f_T is not achieved with the thinnest EOT considered in our simulations, which is due to the fact that the increase of C_{gg} prevails over that of g_m as EOT scales down less than 5 nm.

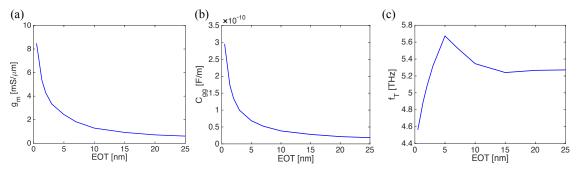


Figure 3.3 (a) g_m , (b) small-signal intrinsic gate capacitance C_{gg} , and (c) intrinsic cutoff frequency f_T as a function of EOT varying from 0.5 to 25 nm. The g_m and C_{gg} are extracted at $I_{on} = 1$ mA/ μ m from the simulation results [98].

3.3.3 Effect of Channel Length Scaling

We investigate the effect of channel length scaling on the intrinsic high-frequency performance of BP FETs by varying the channel length from 5 to 150 nm. Figures 3.4(a) and 3.4(b) show the g_m and C_{gg} as a function of L_{ch} , respectively, for a fixed EOT of 5 nm. While our ballistic transport simulation results show that g_m is nearly constant for the channel longer than 30 nm, it decreases as the channel length scales down less than 30 nm due to the short-channel effects. The intrinsic gate capacitance is extracted from our numerical simulation results at $V_G = -1.3$ V, and the C_{gg} exhibits nearly linear dependence to the channel length. Then, we have plotted the intrinsic f_T vs. $1/L_{ch}$, which shows nice linearity for long-channel devices. But it starts to deviate from $1/L_{ch}$ dependence for $L_{ch} < 30$ nm due to the degradation of g_m . A similar trend was also observed in graphene FETs [105]. To show the linearity of f_T to $1/L_{ch}$ for the long-channel devices, we have plotted a guideline (dashed line) in Fig. 3.4(c) with $f_T = 100$ GHz· μ m/ L_{ch} , which is, surprisingly, very similar to that of graphene FETs reported earlier [106]. Although semiconducting black phosphorus has relatively lower mobility than graphene, BP FETs can exhibit a comparable cutoff frequency as graphene FETs due to relatively smaller C_{gg} .

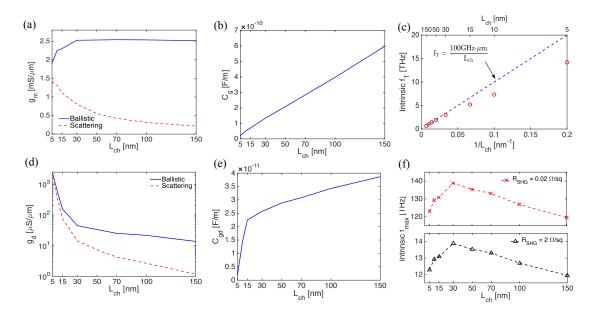


Figure 3.4 Intrinsic f_T and unity power gain frequency f_{max} calculated for various L_{ch} with a fixed EOT of 5 nm at the on state ($V_G = -1.3 \text{ V}$; $V_D = -0.5 \text{ V}$). Channel length dependence of (a) g_m , (b) C_{gg} , (c) intrinsic f_T , (d) g_d , (e) C_{gd} , and (f) intrinsic f_{max} for gate sheet resistance of $R_{SHG} = 2 \Omega/\text{sq}$ with a fixed device width of $W = 1 \mu m$. The dashed line in (c) shows the linear fitting for long-channel devices with $f_T = 100 \text{ GHz} \cdot \mu m/L_{ch}$ [98].

One of the most significant drawbacks of graphene FETs for high-frequency applications is the limited unity power gain frequency. It has been observed from many experiments that f_{max} is significantly lower than f_T in graphene FETs [83], [86]. This is attributed to the fact that graphene is semi-metal and hence the

current cannot be saturated with increasing the drain voltage. On the other hand, semiconducting BP-based FETs can offer significantly smaller g_d along with large f_T , which makes BP FETs attractive for high-frequency applications. Figure 3.4(d) shows the output conductance as a function of L_{ch} , which is extracted from the numerical simulations at $V_D = -0.5$ V. We notice that g_d increases slowly as L_{ch} decreases from 150 nm to 30 nm, where the gate controls the electrostatic potential in the channel region well, and the g_d can be as low as 13 μ S/ μ m at 150-nm channel, which is smaller than that of graphene FETs by two orders of magnitude [102]. However, as the channel length further scales down below 30 nm, g_d increases significantly due to the short-channel effect, but the g_d of BP FETs still remain one order smaller than that of graphene FETs [102].

The gate-to-drain capacitance for various channel length is shown in Fig. 3.4(e), which is also extracted from the numerical simulation results at $V_D = -0.5$ V. As the channel length scales down from 150 nm to 15 nm, C_{gd} is also linearly decreased, which can be explained by the strong correlation of the channel charge to the length of the device, considering that C_{gd} is proportional to ΔQ_{ch} for a given V_D variation as shown in Eq. (3.2). Notably, the channel length dependence of C_{gd} becomes even more significant (i.e., C_{gd} vs. L_{ch} shows a steeper slope) at $L_{ch} < 15$ nm, where the ΔQ_{ch} for a given V_D variation becomes more susceptible to the change of channel length due to the short-channel effect.

The intrinsic unity power gain frequency is plotted in Figure 3.4(f) using the intrinsic f_T , g_d , and C_{gd} evaluated above for a gate resistance. In general, R_G depends on the geometry of the device and the actual fabrication process of the gate electrode (*e.g.*, the number and the width of gate fingers, and the materials of the gate). Here we use a single-finger metal gate reached out from one side, and the width of the transistor is assumed to be W = 1 µm. Unlike the cutoff frequency, f_{max} is significantly affected by the device width, and the detailed investigation on its effect will be reserved for a later discussion. As can be seen from Eq. (3.6), distributed gate resistance is linearly proportional to W and R_{SHG} . A few decades ago, R_G was the most limiting factor for the polysilicon gate. Nowadays, however, the use of metal gates has enabled a considerable reduction of R_{SHG} . The intrinsic f_{max} is investigated in Figure 3.4(f) using $R_{SHG} = 2$ Ω/\Box [107], [108]. The peak value is observed to be 14 THz at ~30 nm channel length, where two competing terms exist as shown in Eq. (5): f_{max} is mainly dictated by $2\pi f_T C_{gd}$ for long-channel devices, whereas g_d becomes predominant for short-channel devices.

3.3.4 Effect of Contact Resistance

So far, we have investigated the intrinsic performance without considering contact resistances and parasitic capacitances. Now we will extend our discussion to the extrinsic f_T and f_{max} . First, we focus on the effect of contact resistance, and the impact of parasitic capacitance will be discussed separately in the following section. $R_{S/D}$ has been known as one of the limiting factors of device performance in 2D material electronics

[104]. By carefully choosing the source and drain metal and optimizing fabrication processes, low $R_{S/D}$ (0.1–0.78 k Ω · μ m) has been realized for graphene and MoS₂ devices [109], [110]. In the case of BP FETs, 5 k Ω · μ m could be a typical value extracted from recent experiments [92], [111], [112]. First, we have taken this value along with W=1 μ m and $R_{SHG}=2$ Ω/\Box to investigate the extrinsic f_T and f_{max} . Figure 3.5 shows that both f_T and f_{max} can be ~500 GHz at $L_{ch}=10$ nm and reduces as the channel length increases, resulting in a half-peak value when $L_{ch}=150$ nm. If the contact resistance is reduced significantly to 0.58 k Ω · μ m, which is the lowest value reported for BP FETs [113], the extrinsic f_T and f_{max} can be tremendously improved. By reducing the contact resistance from 5 k Ω · μ m to 0.58 k Ω · μ m, the peak values of f_T and f_{max} can be enhanced by 7 times, leading to ~3.5 THz, if the parasitic capacitance is ignored.

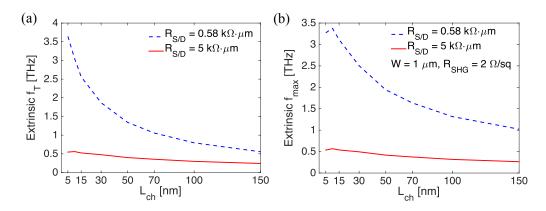


Figure 3.5 Effect of contact resistance $R_{S/D}$ on extrinsic f_T and f_{max} ignoring parasitic capacitance. (a) Extrinsic f_T and (b) f_{max} for $R_{S/D} = 0.58$ and 5 k Ω · μ m with W = 1 μ m and $R_{SHG} = 2$ Ω/sq [98].

3.3.5 Effect of Parasitic Capacitance

In practice, parasitic capacitance is one of the most important factors to consider when evaluating f_T and f_{max} as C_p is very sensitive to device size and geometry. Based on the planar device structure shown in Figure 3.1(a), we calculate the parasitic capacitance using Eqs. (3.12)–(3.15), where metal line width $(L_{S/D})$, the spacing between the gate and the source/drain metal $(L_{GS/GD})$, and the gate length $(L_G = L_{ch})$ determine the parasitic capacitance. We used three different values of 14 nm, 200 nm and 1 μ m for $L_{GS/GD}$ with $L_{S/D} = 200$ nm, and we have $C_{gs,p} = C_{gd,p} = C_{dg,p}$ according to the conditions considered in this study. In Figure 3.6(a)-(d), the parasitic capacitances are evaluated at various channel lengths for three different $L_{GS/GD}$ and compared to their intrinsic values (dashed lines in Figure 3.6(a)-(c)). As the metal lines are getting closer (with smaller $L_{GS/GD}$), parasitic capacitances increase significantly at all channel lengths.

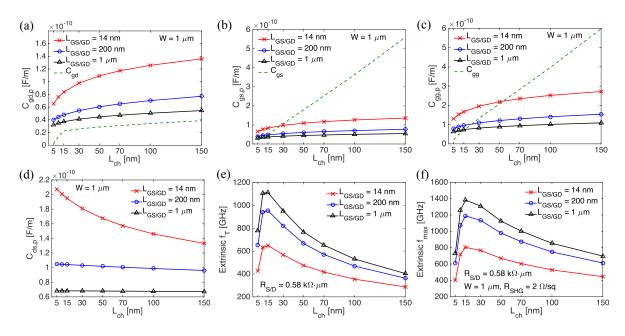


Figure 3.6 Parasitic capacitances and their effects on extrinsic f_T and f_{max} with various L_{ch} . (a) parasitic small-signal gate-to-drain capacitance $C_{gd,p}$, (b) gate-to-source capacitance $C_{gs,p}$, (c) gate capacitance $C_{gg,p}$, and (d) drain-to-source capacitance $C_{ds,p}$ as a function of L_{ch} for three different source/drain to gate metal distances $L_{GS/GD}$ of 14 nm, 200 nm and 1 μ m, with a fixed $W = 1 \mu$ m. In (a)-(c), dashed lines represent the intrinsic values for comparison. (e) Extrinsic f_T and (f) f_{max} as a function of L_{ch} with $R_{S/D} = 0.58 \text{ k}\Omega \cdot \mu$ m, $R_{SHG} = 2 \Omega/\text{sq}$ and $W = 1 \mu$ m [98].

When a transistor is operated in the saturation region, the intrinsic C_{gd} is negligible, but its parasitic capacitance is not. For example, with $L_{GS/GD} = 14$ nm, $C_{gd,p}$ is greater than C_{gd} by 3-4 times for the channel length from 15 to 150 nm as shown in Figure 3.6(a). Therefore, $C_{gd,p}$ plays an important role for the extrinsic f_T and f_{max} . On the other hand, $C_{gs,p}$ and $C_{gg,p}$ could be less critical since the intrinsic C_{gs} and C_{gg} are large in the saturation region, and impact of $C_{gs,p}$ and $C_{gg,p}$ would be relatively insignificant, especially for long channel devices, as shown in Figure 3.6(b) and 6(c). However, our results reveal that $C_{gs,p}$ and $C_{gg,p}$ become comparable to or even larger than intrinsic capacitances for the short-channel devices. Moreover, as $L_{GS/GD}$ decreases, the contribution by the parasitic components becomes more dominant in the total gate capacitance $C_{gg,t}$ for a given channel length, as can be seen in Figure 3.6(c). Figure 3.6(d) shows $C_{ds,p}$ for different $L_{GS/GD}$ as a function of channel length, which exhibits that $C_{ds,p}$ increases as the channel length scales down, unlike other parasitic capacitances discussed above, due to the strong interaction between source and drain metal lines.

Considering all parasitic capacitances and intrinsic ones along with contact resistance, we have plotted the extrinsic f_T and f_{max} in Figure 3.6(e) and 3.6(f). When comparing these with the dashed lines in Figure 3.5(a) and 3.5(b), we can clearly see the following distinctions. First, the values are significantly reduced. Second, the extrinsic f_T and f_{max} exhibit large degradation at extremely scaled channel lengths. The peak

values are found at ~15 nm channel: the maximum f_T varies from 600 GHz to 1.1 THz; the maximum f_{max} from 800 GHz to 1.4 THz under different parasitic capacitances.

3.3.6 Effect of Scattering

So far, we have ignored the effect of scattering. Although we focus on relatively short channel lengths for the maximum f_T and f_{max} in this study, in order to minimize the gap between our assessment and the actual measurements, we take the effect of scattering into account using $I_{proj} = \frac{\lambda_{max}}{L_{ch} + \lambda_{max}} I_{bal}$, where λ_{max} is the peak mean free path of BP, I_{bal} is the ballistic current determined by the NEGF simulations, and I_{proj} is the projected current considering scattering [99]. To determine λ_{max} , we have taken the measurement data (I_D – V_G plot) from Ref. [92] and followed the approach outlined in Ref. [114]. Figures 3.7(a) and 3.7(b) show the field-effect mobility and mean free path of black phosphorus. The extracted peak mobility is 245 cm²V⁻¹s⁻¹, which is in good agreement with Ref. [92] and the corresponding mean free path turns out to be 14 nm. The consequent g_m and g_d after considering the scattering effects are shown in Figs. 4(a) and (d) with dashed lines, respectively where apparent degradation can be observed particularly for the long-channel devices. We assume that scattering has negligible impacts on intrinsic capacitance for the size of devices considered in this study[102], [115], and parasitic capacitance is determined solely by the device structure, not by scattering.

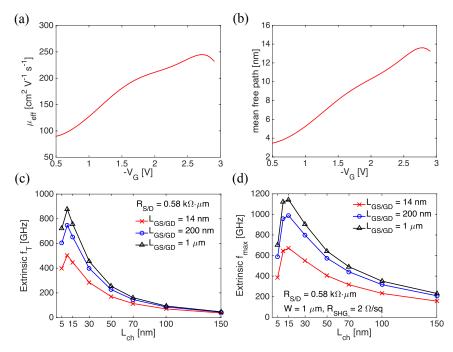


Figure 3.7 (a) Field-effect mobility and (b) mean free path extracted from experiment (Ref. [92]). (c) Extrinsic f_T and (d) f_{max} are calculated considering the scattering effect along with contact resistances and parasitic capacitances [98].

The corresponding extrinsic f_T and f_{max} are plotted in Figure 3.7(c) and 3.7(d) with $R_{S/D} = 0.58 \text{ k}\Omega \cdot \mu\text{m}$, moderate gate sheet resistance ($R_{SHG} = 2 \Omega/\Box$) and $W = 1 \mu\text{m}$ for three different parasitic capacitances. The peak values can be found at L_{ch} of 10–15 nm. Although scattering affects the extrinsic f_T and f_{max} of long-channel devices significantly (f_T and f_{max} become only 50 GHz and 200 GHz, respectively, at $L_{ch} = 150 \text{ nm}$), their impacts can be minimal for the short channel region where the peak frequencies are achieved. Even with scattering, the maximum f_T ranges from 500 to 900 GHz; the peak f_{max} from 650 GHz to 1.15 THz for different parasitic capacitances.

3.3.7 Effect of Device Width

In theory, f_T is not a function of device width since the units of both g_m in the numerator and capacitances in the denominator in Eq. (7) are given per unit width, and the width information is canceled out. However, things will be different for f_{max} because the distributed gate resistance is proportional to the device width. We have studied the effect of W on the extrinsic f_{max} in Figure 3.8 by considering W = 1 and 10 µm under $R_{S/D} = 0.58 \text{ k}\Omega \cdot \text{µm}$, $R_{SHG} = 2 \Omega/\square$, and $L_{GS/GD} = 200 \text{ nm}$. In general, smaller device width is preferable for high f_{max} , and the peak f_{max} of W = 1 µm is 5 times larger than that of W = 10 µm with $\alpha = 1/3$ (solid lines). Alternatively, f_{max} can be improved with a smaller gate resistance by using the gate terminal brought out from both sides, where α becomes 1/12. The blue dashed line in Figure 3.8 indicates that a huge improvement can be achieved with $\alpha = 1/12$ if the width of the device is large. For example, the peak f_{max} can be enhanced by 100% if α is changed from 1/3 to 1/12 for W = 10 µm. However, the gain of $\alpha = 1/12$ can be quite small (less than 10%) if high f_{max} is already achieved with a small width (W = 1 µm).

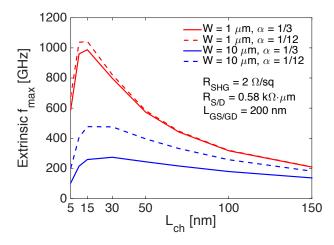


Figure 3.8 The effects of device width and α on extrinsic f_{max} at various L_{ch} with $R_{S/D} = 0.58 \text{ k}\Omega \cdot \mu \text{m}$ and $R_{SHG} = 2 \Omega/\text{sq}$, considering scattering and moderate parasitic capacitance ($L_{GS/GD} = 200 \text{ nm}$) [98].

3.3.8 Performance Limit Projection and Benchmark

Finally, the high-frequency performance limit is projected in Figure 3.9 based on optimal device parameters to achieve the maximum f_T and f_{max} . By using $R_{SHG} = 0.02 \ \Omega/\Box$ [95], [101] with $\alpha = 1/12$, $W = 1 \ \mu m$, $L_{GS/GD} = 1 \ \mu m$ and $R_{S/D} = 0.58 \ k\Omega \cdot \mu m$, the peak f_T of 900 GHz and the peak f_{max} of 1.2 THz are projected at $L_{ch} = 10 \ nm$. In order to benchmark against experimental data [91], [92], we have extrapolated the simulation results up to 1- μ m channel length. The measurement data show f_T of 17.5 GHz and f_{max} around 14.5 GHz at 250 nm [92], which are still quite smaller than the values projected in Figure 3.9. This indicates that there exists large room to improve in fabrication through optimization and engineering various parameters discussed in this study. According to our results shown in Figure 3.9, the realization of a short-channel BP FET is strongly suggested as both f_T and f_{max} exhibit significant improvement if L_{ch} becomes shorter than 100 nm. Aggressive scaling of channel length beyond THz f_{max} can be achievable with a BP FET, making it very attractive for future high-frequency applications.

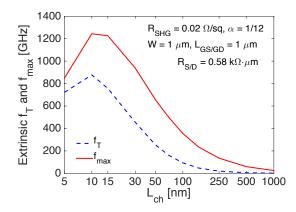


Figure 3.9 Performance limit projection of extrinsic f_T and f_{max} at $R_{S/D} = 0.58$ k Ω ·µm, $R_{SHG} = 0.02$ Ω /sq, $\alpha = 1/12$ and W = 1 µm, considering scattering and small parasitic capacitance ($L_{GS/GD} = 1$ µm) [98].

3.4 Discussion

Since BP has a highly anisotropic band structure, it would be useful to discuss the effect of different orientations. The main significance of heavier effective mass with zigzag orientation in the transport direction is twofold: (i) Ballistic current is reduced due to the small carrier velocity and the less number of transverse modes [116], [117]. (ii) Scattering mean free path becomes shorter due to the heavier effective mass, resulting in lower mobility, as supported by the recent experiment [118]. Consequently, it is expected that f_T and f_{max} will be limited in zigzag transport direction as compared with armchair orientation. On the other hand, in theory, contact resistance will remain unaffected by different orientations since thermionic emission current in a two-dimensional system depends on density-of-states effective mass [119]. Recent experimental studies also exhibited that the measured current, transconductance, and field-effect mobility

are significantly limited in zigzag orientation [113], [118], which indicates that the impacts of effective mass on the ballistic current, mobility, and scattering mean free path are not altered by the minimal influence of different orientations on the contact resistance.

In this study, we used the quasi-static approach considering the equivalent capacitive and resistive elements but neglecting the inductive elements, as is widely used in similar studies [102]–[106], [120], [121]. To validate our approach, we evaluated the LC characteristic frequency $[f_{LC} = 1/(2\pi\sqrt{L_kC_{gg}})]$ for the simulated BP FETs, using the kinetic inductance $[L_k = (m^*/pq^2)(L_{ch}/W); p$ and q are hole density per unit area and elementary charge] and C_{gg} extracted from the simulated data, leading to $f_{LC} \sim 9$ THz for 15 nm channel device. This is significantly higher than the peak frequencies of ~ 1 THz evaluated in this study (Figure 3.9), thus validating the quasi-static approximation. Nonetheless, further work will be needed to examine the exact role of kinetic inductance and non-quasi-static effects through time-dependent transport simulations, which is beyond the scope of this study.

3.5 Conclusion

By using atomistic quantum transport device simulations and equivalent small-signal circuit model, high-frequency behaviors of BP FETs are studied. We have investigated intrinsic and extrinsic f_T and f_{max} considering source/drain contact resistance, parasitic capacitance, distributed gate resistance, and device width, and have discussed the impact of each device parameter on the high-frequency performance one by one. Our simulation results and assessment not only reveal the great potential of BP FETs for high-frequency applications, but also shed light on the proper direction to optimizations. The main points of this study can be summarized as follows:

- 1) BP FETs exhibit clear saturation behaviors with increasing drain voltage, unlike graphene FETs, resulting in >10 THz frequencies for both intrinsic f_T and f_{max} . While intrinsic f_T increases monotonically with channel length scaling, f_{max} starts to degrade at $L_{ch} < 30$ nm.
- 2) Although extrinsic f_T and f_{max} are significantly affected by contact resistance and parasitic capacitance, they can remain near THz frequency range ($f_T = 900 \text{ GHz}$; $f_{max} = 1.2 \text{ THz}$) through proper engineering, particularly with an aggressive channel length scaling ($L_{ch} \approx 10 \text{ nm}$).
- 3) In spite of the significantly lower mobility of semiconducting BP compared to that of semi-metallic graphene, f_T of BP FETs can be comparable to that of graphene FETs. Moreover, f_{max} of BP FET is unconstrained due to large output resistance. Although the measurement data shows relatively lower values ($f_T = 17.5 \text{ GHz}$; $f_{max} = 14.5 \text{ GHz}$ at $L_{ch} = 250 \text{ nm}$)[92] simply because BP FETs are still in their infancy yet, our assessment and benchmark indicate that there exists large room for optimization, suggesting further advancement of high-frequency performance of the state-of-the-art BP FETs for future analog and RF applications.

Chapter 4

Temperature-Dependent Transport Characteristics of Ohmic and Schottky Contact MoSe₂ FETs

4.1 Introduction

Transition metal dichalcogenides (TMDs) are layered materials, which can be isolated as ultrathin layers by exfoliation from bulk crystals or can be achieved by direct syntheses. TMDs have attracted intensive attention due to their suitable bandgap for electronic devices [13], [122]-[125]. The direct bandgap in the visible frequency range and good mobility at room temperature make TMDs promising for flexible electronics and optoelectronics. However, the fabrication of high-performance TMDs transistors is challenging, limited partly by metal-semiconductor contact properties. The presence of a significant Schottky barrier has been a major issue [49]–[51]. In traditional silicon-based electronics, ohmic contact with low resistance can be achieved by selective ion implantations in source/drain regions to reduce the barrier width between semiconductor and metal. However, effective doping by ion implantation is less practical for ultrathin monolayer and few-layer TMDs. Many recent experimental works have demonstrated various progress toward improved contact properties. The method includes the use of low work function metals, graphene, or doped TMDCs as electrodes, thermal annealing, ionic-liquid doping of contact regions, phase-engineering, selective etching, and the introduction of thin tunnel barriers. However, some methods suffer from poor air, thermal or long-term stability. The effective methods of practical thermal and longterm stable ohmic contacts can be generally classified as two types: reducing the Schottky barrier height (SBH) and thinning the Schottky barrier width (SBW).

In this work, we provide a simple physical model of temperature-dependent transport behavior for TMD FETs. We discuss the effect of lowering SBH and thinning SBW to achieve an ohmic contact. Our experimental collaborator fabricates thin-film MoS₂ FETs to verify our models further. The device-to-device variations are also discussed along with other non-ideal factors. Our simple model reveals the underlying physics in the temperature-dependent transport behaviors. It may provide guidelines to fabricate high-performance ohmic contact devices in experiments.

4.2 Computational Method

In this work, monolayer MoSe₂ is used in our simulation. However, this model can be applied to other TMDs and general 2D materials. Non-equilibrium Green's function (NEGF) formalism with an effective mass approximation is used for transport simulation along with Poisson's equation for self-consistent

solutions. Since n-type Schottky contact is assumed in our model, only electron (n-type) current is calculated. The value of $0.49 \, m_0$ is used for electron effective mass along transport and transverse directions since MoSe₂ has anisotropic effective mass near conduction band minimum [24], [126]. The nominal device structure is shown in the inset of Figure 4.1(a). The details of parameters are as follows: Monolayer MoSe₂ ($E_g = 1.43 \, \text{eV}$, $\varepsilon_r = 6.9$) for the channel material with 15 nm gate-controlled channel length (L_G) and 15 nm underlap length (L_U) at both source and drain sides, single-gate device structure with 3.4 nm-thick SiO₂ ($\varepsilon_r = 3.9$) gate dielectric. The 15 nm L_U is to mimic the Schottky barrier at the metal-semiconductor interface. The total channel length (L_{ch}) is the sum of L_U and L_G . Ballistic transport is assumed in our NEGF simulation, and the scattering effect will be considered separately. These simulation settings can be altered for other materials or device structures to explore the underlying physics without changing our conclusion for temperature-dependent transport behavior. The Schottky barrier height for electrons (Φ_{Bn}) is assumed to be 0.3 eV for Schottky contact devices [127]. Flat band condition at $V_G = 0 \, \text{V}$ is assumed here. We use 300 K and 77 K as two typical temperatures for room temperature and low temperature for our simulations.

4.3 Results and Discussion

4.3.1 Temperature-Dependent Transport in the Ballistic Regime

Due to the existence of barriers in the Schottky contact FETs, the current level is limited, and the current also degrades more at a lower temperature. Self-consistently calculated ballistic I_D - V_G characteristics for monolayer Schottky contact MoSe₂ FET is shown in Figure 4.1(a). We notice that the room-temperature devices' threshold voltage ($V_{\rm TH}$) is lower than the low-temperature device. Six times larger $I_{\rm on}$ ($V_{\rm G}$ = 1.2 V) can be explained by the Fermi distribution of electrons. Figure 4.1(b) shows the potential of the device along the transport direction at $V_G = 1.0 \text{ V}$. As we can see that E_C (conduction band) at 300 K and 77 K are almost identical. However, the difference in current can be reflected in the linear-scale energy-resolved current spectrum (I_E) in Figure 4.1(c). We can see that the peak of I_E at 300 K locates around 0.1 eV, while the peak of I_E at 77 K locates slightly below μ_s . According to the Landauer equation, the factor making such a difference in current is the Fermi distribution. A similar shape between the Fermi distribution and logarithm-scale energy-resolved current spectrum can be observed in Figure 4.1(d), which verifies our explanation. Below μ_s , I_E of 300 K and 77 K are overlapped. Above μ_s , I_E of 77 K drops exponentially in the same trend as the Fermi distribution. Due to the near-zero I_E above μ_s at 77 K, its I_{on} is much smaller than that of 300 K. To turn on the FET, larger V_G is needed at lower temperatures, and this results in a larger threshold voltage $V_{\rm TH}$. In general, due to the barrier at the Schottky contact, the significant difference in the shape of the tail of the Fermi distribution determines the overall current level.

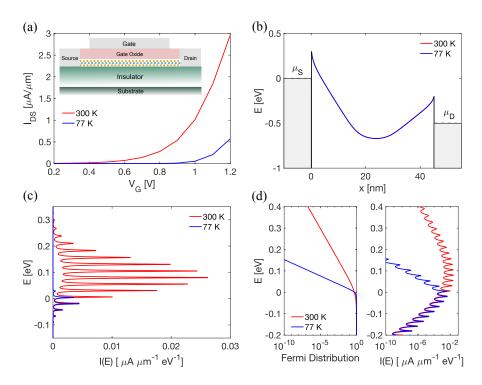


Figure 4.1 Nominal Schottky contact MoSe₂ FETs with $\Phi_{Bn} = 0.3 \text{ eV}$: (a) I_D - V_G characteristics. A schematic illustration of device is shown in the inserted panel. (b) Conduction band bottom (E_C) diagram. (c) Linear scale energy-resolved current spectrum (I_E). (d) Left panel: Fermi distribution. Right panel: logarithmic scale I_E . The solid red line is for 300 K, and the blue line is for 77 K.

Our first model is to lower the Schottky barrier height (SBH) by reducing Φ_{Bn} to 0 eV to achieve an ohmic contact device. Other parameters are the same as the nominal device. We name this kind of contact as the type I contact. Flat band condition at $V_G = 0$ V is assumed here. The I_D - V_G characteristic is shown in Figure 4.2(a). The current level is significantly increased. The V_{TH} of 300 K is also slightly smaller than that of the 77 K device. The on-state current at 77 K is still smaller than 300 K, but the difference is much less than that of the Schottky contact situation. At the off-states, potential along transport direction is almost identical at 300 K and 77 K, whereas, at on-state, due to the large carrier injection, 300 K devices exhibit slightly higher barriers at the source side, as shown in Figure 4.2(b). It can also be reflected in the energy-resolved current spectrum in Figure 4.2(c). We notice that the peak of I_E at 77 K is around 0 eV, which corresponds to μ_s . However, at 300 K, the peak of I_E locates around 0.04 eV, which is close to the top of the barrier (0.02 eV). The tail of the Fermi distribution is less important here compared to the Schottky contact situation since the majority of I_E locates around μ_s . The insignificant barrier at 300 K reduces the difference in the current level between 300 K and 77 K.

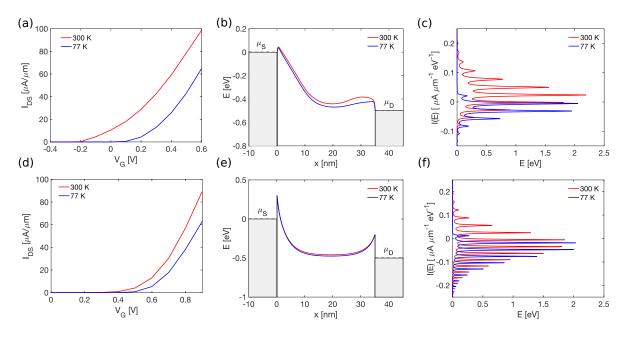


Figure 4.2 Ohmic contact MoSe₂ FETs by lowering SBH (Type I): (a) I_D - V_G characteristics. (b) E_C diagram. (c) Linear scale I_E . Ohmic contact MoSe₂ FETs by thinning SBW (Type II): (d) I_D - V_G characteristics. (e) E_C diagram. (f) Linear scale I_E . The solid red line is for 300 K, and the blue line is for 77 K.

The second ohmic contact model is to use thin Schottky barrier width (SBW) by reducing $L_{\rm U}$. We name this kind of contact as type II contacts. The "effective barrier height" is lowered due to the thin barrier width. Zero underlap regions at source and drain sides are assumed in our model to explore the limit of device performance. Other parameters are the same as the nominal device, with $\Phi_{\rm Bn}=0.3~{\rm eV}$ and $L_{\rm G}=45~{\rm nm}$ to make $L_{\rm ch}$ same. The $I_{\rm D}$ - $V_{\rm G}$ characteristic is shown in Figure 4.2(d). Significantly a hundred times larger $I_{\rm on}$ is achieved as compared to that of Schottky contact FETs. The device potential along transport direction at the on-state ($V_{\rm G}=0.8~{\rm V}$) is shown in Figure 4.2(e). The $E_{\rm c}$ of 300K is slightly higher due to a slightly large current injection. At both temperatures, it exhibits a near-transparent thin barrier at the source side. The temperature-dependent Fermi distribution can explain the difference in on-state current, as in Figure 4.2(f). Above μ_s , $I_{\rm E}$ drops to zero quickly at 77 K, as the Fermi distribution drops exponentially in Figure 4.1(d). At the same time, $I_{\rm E}$ at 300 K exhibits a nearly symmetric waveform around μ_s . The small mismatch in $I_{\rm E}$ corresponds to the same amount of difference in channel potential in Figure 4.2(e). The barrier height of type II contact SBFET is 0.3 eV, same as the SBFET demonstrated in Figure 4.1. However, due to the thin Schottky barrier at the metal-semiconductor interface, the majority of electron transport happens around μ_s . It suggests the "effective barrier height" of type II contact SBFET is around 0 eV.

4.3.2 Mean Free Path (λ_{max}) and Mobility (μ) of MoSe₂

To this point, we reveal the distinct temperature-dependent behavior for short-channel FETs in the ballistic region. The difference becomes even more notable when considering scattering effects. We take the effect of scattering using $I_{proj} = \frac{\lambda_{max}}{L_{ch} + \lambda_{max}} I_{bal}$, where λ_{max} is the peak mean free path of MoSe₂, I_{bal} is the ballistic current determined by the NEGF simulations, and I_{proj} is the projected current considering scattering [99]. To determine temperature-dependent λ_{max} , we have taken the measurement data (σ - V_G , Conductivity-Gate voltage plot) from Ref. [60] to extract I_D - V_G plot, and follow the approach outlined in Ref. [114]. Here we limit our temperature range from 50 K to 300 K. The extracted λ_{max} is shown in Figure 4.3(a), and the dashed line indicates the fitted λ_{max} -T plot. It matches our expectation that the lower temperature, the longer mean free path, since both ionized impurity scattering and phonon scattering can be suppressed at lower temperatures. The mean free path at 77 K and 300 K can be read from the dashed line being 21 nm and 8.5 nm. We further compare our extracted mobility to the experimental results shown in Figure 4.3(b), which shows a good match. The μ_{max} increases rapidly as temperature decreases.

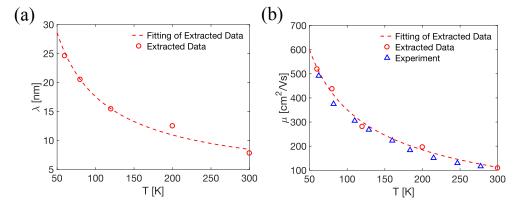


Figure 4.3 (a) Mean free path at various temperatures. The red circle stands for extracted data from Ref, and the red dashed line stands for the fitting. (b) Mobility at various temperatures. Blue triangles represent experimental results from Ref. [60]. The Red dashed line represents the fitting of extracted mobility.

4.3.3 Temperature-Dependent Transport in the Diffusive Regime

For the nominal Schottky contact and ohmic contact devices, $L_{\rm ch} = L_{\rm G} + 2L_{\rm U}$, which is 45 nm. The $I_{\rm D}$ - $V_{\rm G}$ characteristics of Schottky, type I, and II ohmic contact FETs are shown in Figure 4.4 (a), (b), and (c), respectively. Compared to the ballistic results, $V_{\rm TH}$ doesn't change, but the current is smaller. This can be understood as scattering coefficient $\frac{\lambda_{max}}{L_{ch} + \lambda_{max}}$ is always smaller than 1. For a FET with a given $L_{\rm ch}$, the scattering coefficient is notably affected by λ_{max} , as longer λ_{max} leads to a larger scattering coefficient. In this way, the current is less degraded at a lower temperature. For the Schottky contact FETs, $I_{\rm on}$ at 300 K is less than one-sixth of its ballistic value, and $I_{\rm on}$ at 77 K is around one-third of its ballistic value. Still, $I_{\rm on}$ at

300 K demonstrates about two times larger current than its value at 77 K. Same magnitude of current degradation happens for type I and type II ohmic contact FETs. However, because $I_{\rm on}$ at low temperature is near to $I_{\rm on}$ at room temperature, current at lower temperature soon exceeds its value at room temperature after considering the scattering effect, as $V_{\rm G}$ increases. We stop at $V_{\rm G} = 0.6$ V for type I ohmic contact FETs where $I_{77\rm K}$ is around 1.4 times of $I_{300\rm K}$, and $V_{\rm G} = 1.0$ V for type II ohmic contact FETs where $I_{77\rm K}$ is about 1.7 times of $I_{300\rm K}$. A higher current ratio may be achieved in experiments at high gate voltage. The temperature-dependent transport behavior matches with experiment results in Ref. [60].

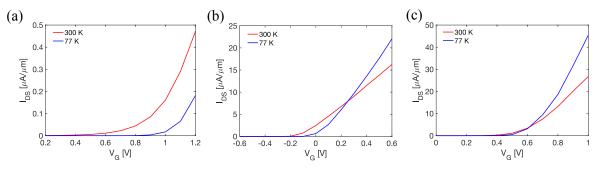


Figure 4.4 I_D - V_G characteristics of MoSe₂ FETs considering scattering of (a) nominal Schottky contact; (b) ohmic contact by lowering SBH (Type I); (c) ohmic contact by thinning SBW (Type II). The red line is for 300 K, and the blue line is for 77 K.

Next, we studied the temperature-dependent on-state current for both ohmic and Schottky FETs as shown in Figure 4.5. Here the $I_{\rm on}$ is taken at $V_{\rm G}=1.1~{\rm V}$ for the Schottky contact FETs ($\Phi_{\rm Bn}=0.3~{\rm eV}$), $V_{\rm G}=0.5~{\rm V}$ for type I ohmic contact FETs ($\Phi_{Bn} = 0$ eV) and $V_G = 0.9$ V for type II ohmic contact FETs ($\Phi_{Bn} = 0.3$ eV). As the temperature increase, I_{on} of type I and II ohmic contact FETs increases, while I_{on} of Schottky contact FETs decreases. As we have explained earlier, this depends on the energy range where the majority of transport happens. The two competing effects of Fermi distribution and scattering effect work as follows: the greater Schottky barrier is, the worse current degradation at a lower temperature because of the logarithmic decrease of Fermi distribution above μ_s ; the lower temperature, the larger scattering coefficient, due to longer mean free path. In other words, for the Fermi distribution, the further I_E peak above μ_s , the larger difference in current at various temperatures. However, if the I_E peak is near or below μ_s , the Fermi distribution is 1 for all temperatures. For the scattering, the lower temperature, the longer mean free math, and higher mobility; thus, current is larger. For the Schottky contact devices, even with higher mobility at low temperature, current still degrades at a lower temperature, since Fermi distribution is the dominant factor as most transport happens above μ_s . For type I and II ohmic contact devices, the scattering effect is the dominant factor due to near zero "effective barrier height". Current degradation due to the Fermi distribution is less important because the majority of transport happens around μ_s .

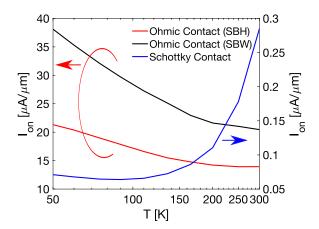


Figure 4.5 I_{on} -Temperature characteristics of MoSe₂ FETs. I_{on} is taken at $V_G = 1.1$ V, 0.5 V, and 0.9 V for nominal MoSe₂ FETs with Schottky contact, type I and II ohmic contacts.

We further explore the effect of channel length, and it turns out that it does not change our conclusion. The on-state current ratio of $I_{50\text{K}}/I_{300\text{K}}$ is used to indicate the temperature-dependence as shown in Figure 4.6. I_{on} is taken at $V_{\text{G}} = 1.1 \text{ V}$, 0.5 V, and 0.9 V for MoSe₂ FETs with Schottky contact, type I and II ohmic contacts, respectively. The current is estimated using $I_{proj} = \frac{\lambda_{max}}{L_{ch} + \lambda_{max}} I_{bal}$. The ballistic current of longer L_{ch} FETs should be the same as the nominal device since ballistic NEGF simulation is assumed. 45 nm to 1 μ m L_{ch} are examined here. For the Schottky contact devices at all channel lengths, we have $I_{50\text{K}}/I_{300\text{K}} < 1$. As L_{ch} increases, $I_{50\text{K}}/I_{300\text{K}}$ slightly increases and saturates around 1/3. The $I_{50\text{K}}/I_{300\text{K}}$ is larger than one for both ohmic contact FETs, and it also increases gradually as L_{ch} increases. Overall, the distinct temperature-dependent on-state current ratio doesn't change with L_{ch} .

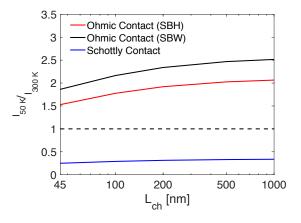


Figure 4.6 On state temperature-dependence current (indicates by $I_{50 \text{ K}}/I_{300 \text{ K}}$) at various $L_{\text{ch.}}$ I_{on} is taken at $V_{\text{G}} = 1.1 \text{ V}$, 0.5 V, and 0.9 V for MoSe₂ FETs with Schottky contact, type I and II ohmic contacts, respectively.

4.3.4 Device-to-Device Variation

In the following sections, we will discuss device-to-device variations with the support of experimental data. In the simulation, 15 nm $L_{\rm U}$ and 0.3 eV $\Phi_{\rm Bn}$ are chosen to mimic MoSe₂ Schottky contact, while the value can be altered based on the quality of contact. Longer $L_{\rm U}$ means more "Schottky", which means smaller current, similar to the effect of barrier height. Also, as $L_{\rm U}$ and $\Phi_{\rm Bn}$ increase, the low-temperature current suffers more from current degradation, which means the on-state current ratio of $I_{\rm Low\ T}/I_{\rm High\ T}$ will be smaller. Our analysis matches well with experiments [49], [60]. For type I ohmic contact, we reduce $\Phi_{\rm Bn}$ to zero to explore the ideal case (negative barrier height would be similar). It is straightforward that increasing $\Phi_{\rm Bn}$ makes it less "Ohmic". Thus the on-state current ratio of $I_{\rm Low\ T}/I_{\rm High\ T}$ will be decreased until it becomes smaller than one. It matches well with various experiments of ohmic contact FETs by lowering barrier height [54], [56], [58], [60], [128], [129]. For type II ohmic contact, we make thin SBW by reducing $L_{\rm U}$ to zero. The ohmic contact can still be achieved with moderately long $L_{\rm U}$. The thinner SBW, the more transparent the barrier to electrons, which also reflects the quality of the contact. As $L_{\rm U}$ increases, the on-state current ratio of $I_{\rm Low\ T}/I_{\rm High\ T}$ will be decreased until it becomes smaller than one like the Schottky contact situations. It matches with experiment results of ohmic contact by thinning SBW [55], [130]. In experiments, lowering SBH and thinning SBW may happen at the same time.

4.3.5 Device Fabrication and Characterization

Our model can be further applied to other TMDs or, more generally, other 2D materials. The electron mass, the bandgap can be changed to other materials without changing our conclusion. MoS_2 FETs are fabricated to support our model. Mechanically exfoliated multilayer MoS_2 flakes were transferred onto the high-k aluminum oxide (Al_2O_3) dielectric layer with a thickness of 50 nm, which was deposited on the p-type doped silicon wafer. Then, source/drain (S/D) electrodes were patterned through the E-beam evaporation of Ti/Au (20/100 nm), photolithography, and etching techniques. The MoS_2 TFTs were thermally annealed at 300 °C for 30 minutes for enhancing contact properties between the active channel and S/D electrodes. More details of fabricating conditions were reported earlier [131], [132]. X-ray diffraction (XRD) pattern was measured by using Bruker D8 Discover diffractometer with Cu-K α radiation. Raman spectra were obtained through high-resolution Renishaw Raman microscope with an excitation wavelength (λ_{ex}) of 514 nm. The X-ray photoelectron spectroscopy (XPS) experiments were performed by using Thermo:Electron X-ray photoelectron spectrometer. The current–voltage characteristic curves at RT were investigated using a Keithley-4200 Semiconductor Characterization System with a probe station under atmospheric environments. During the low-temperature measurement of transport properties, the temperature was controlled using a variable temperature cryogenic probe system (LakeShore, TTPX). Significant variations

in contact resistance between Ti/Au and MoS_2 were observed among samples and across a sample [133]–[135].

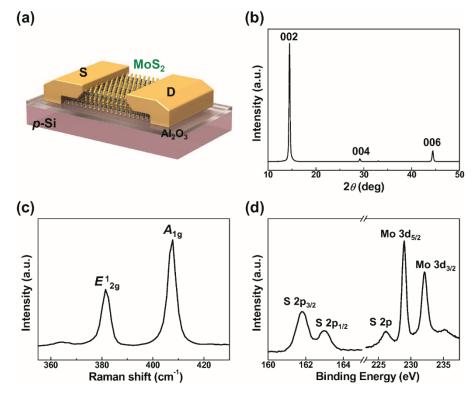


Figure 4.7 (a) 3D schematic illustration of a back-gated multilayer MoS₂ TFT with a 50-nm-thick ALD Al₂O₃ gate insulator. (b) A representative XRD pattern of natural MoS₂. (c) A representative Raman spectroscopy measurement on natural MoS₂. (d) A representative XPS measurement on natural MoS₂ [136].

The three-dimensional schematic structure of back-gated MoS₂ TFT is shown in Figure 4.7(a), which employs multilayer MoS₂ as the active channel, Ti/Au layers as S/D electrodes, and a 50-nm-thick atomic-layer-deposited (ALD) Al₂O₃ as the gate dielectric. The thickness of multilayer MoS₂, mechanically exfoliated from bulk MoS₂ crystals, is in the range of 50 ± 30 nm. We characterized the crystallinity of all the natural MoS₂ used for exfoliation by XRD. The representative XRD pattern depicted in Figure 4.7(b) shows the family of (00*l*) reflections only, revealing its single-crystal nature. We also characterized exfoliated MoS₂ flakes by Raman spectroscopy with λ_{ex} of 532 nm. All tested MoS₂ flakes exhibit two signature Raman-active modes: E_{2g}^1 (at 381.4 cm⁻¹) and A_{1g} (at 407 cm⁻¹) as shown in Figure 4.7(c). The distance between the two modes (25.6 cm⁻¹) is consistent with that of bulk crystals [137], indicating the multilayer structure of the exfoliated MoS₂ crystals. We further characterized exfoliated MoS₂ flakes by XPS. Figure 4.7(d) shows the existence of Mo⁴⁺ (3d^{3/2} and 3d^{5/2}) and S²⁻ (2p_{1/2} and 2p_{3/2}). Within the given conditions, overall XPS results indicate negligible differences among the natural MoS₂ samples.

4.3.6 Temperature-Dependent Transport in Experiment

Here, we investigate the contact properties of back-gated MoS₂ TFTs based on natural MoS₂ crystals by means of low-temperature measurement on current-voltage characteristics. Significant variations in contact resistance between Ti/Au and MoS₂ were observed among samples and across a sample. We classify the fabricated devices into two groups: one group of MoS_2 TFTs shows large I_{on} consistently for a wide range of temperature variation, which indicates ohmic contact; another group of MoS₂ TFTs exhibit relatively lower I_{on} along with a significant temperature dependence, which implies the existence of a significant Schottky barrier (Φ_B). Figure 4.8(a) and (b) show the output characteristics ($I_{ds}-V_{ds}$) of two multilayer MoS₂ TFTs (Device A and Device B) measured at 85K, and 300 K, where dissimilar device characteristics are observed corresponds to Schottky contact and Ohmic contact device respectively. It needs to be mentioned that the distinct output characteristics in Figure 4. 8 are consistently observed in our other MoS₂ TFTs. This can be related to the intrinsic variation of natural MoS₂ as all the MoS₂ TFTs are fabricated with the same materials (MoS₂ flakes exfoliated from the same natural crystal, identical Al₂O₃ gate dielectric, and Ti/Au electrodes) under the same processes. We further measured the on-state current at $V_{\rm GS}=3$ V for device A and B from 85 K to 320 K, as shown in Figure 4.9. Device A exhibits a smaller current and strong temperature-dependent behavior, as we have discussed for the Schottky contact situation in our model. Device B exhibits a larger current, which is constant in a wide range of temperatures.

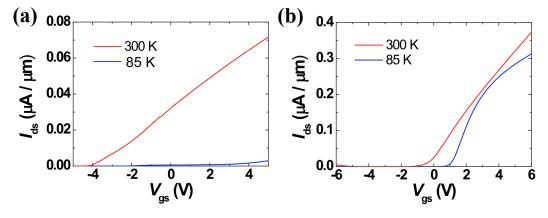


Figure 4.8 Measured I_{DS}-V_G characteristics at 300 K and 85 K of (a) Device A (b) Device B.

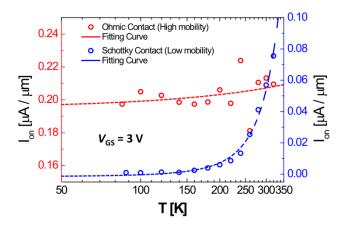


Figure 4.9 Measured *I*_{on}–T characteristics of Device A (blue line) and B (red line).

In our model, we analyze n-type contact by calculating electron current. Similarly, p-type contact can be analyzed by estimating the hole current near the valance band. The effect of equivalent oxide thickness (EOT) is not performed through simulation. While thinner EOT gives better gate control, FETs will benefit from the thinner barrier at the semiconductor-metal interface. Subthreshold region device performance is not discussed in this study since it's straightforward that smaller subthreshold swing can be obtained with lower temperatures due to less thermionic current.

4.4 Conclusion

In this work, we provide a simple model about the contact properties in 2D-material FETs and validate our model by low-temperature current-voltage measurements of multilayer MoS₂ TFTs. For the Schottky contact devices, current degrades more at a lower temperature. To achieve ohmic contact, "effective barrier height" should be lowered by reducing SBH or thinning SBW. Both methods improve the current level significantly. Moreover, at a lower temperature, the current may exceed its value at room temperature due to less scattering, verified by many experimental works. Our simple model suggests the different temperature responses between the Schottky and ohmic contact are determined by the energy range where the majority of transport happens. We also investigate the distinct device-to-device low-temperature responses in multilayer MoS₂ TFTs. The inconsistent contacts could be caused by the intrinsic variation of the electronic properties of natural MoS₂ flakes. We show that the ohmic contact devices can be distinguished from those with Schottky barriers if low-temperature behaviors are characterized. Our model reveals the origin of temperature dependency. Our comprehensive theoretical and experimental study provides a systematic scheme to investigate the contact properties in 2D-material FETs, which will significantly advance the fundamental knowledge and understanding of the metal-semiconductor interface to promote the realization of high-performance 2D-material TFTs.

Chapter 5 Performance Optimization of Monolayer 1T/1T'-2H MoX₂ Lateral Heterojunction Transistors

5.1 Motivation

Two-dimensional (2D) materials can be promising components of next-generation 'more than Moore' transistors. Among many 2D materials available today, monolayer transition metal dichalcogenides (TMDs) attract significant attention due to their chemical stabilities, suitable bandgaps, excellent carrier mobilities, and compatibility with bipolar doping [66], [55], [13]. Consequently, field-effect transistors (FETs) based on atomically thin TMD semiconductor channels have been widely studied over a decade. In general, the overall performance of 2D-material devices is significantly affected by contact resistance [54], [138]. In conventional silicon-based FETs, degenerate semiconductors are used to form Ohmic contacts. However, for 2D materials, achieving degenerate semiconductors is challenging due to their ultra-thin nature, and therefore, most fabricated 2D-material transistors have Schottky contacts based on metalsemiconductor junctions. The Schottky barrier strongly depends on source and drain metals used, and many studies have tried to use proper work-function metals such that Fermi levels (E_t) can exist close to the conduction or the valence band of TMD materials to achieve better contact properties [54], [61], [138], [139]. However, it can be challenging to find proper metals having a desirable work function that can provide low contact resistance for given 2D materials. In addition, conventional doping processes such as ion implantation can substantially damage the structural integrity of 2D materials, which may lead to significant alternation of their band structures.

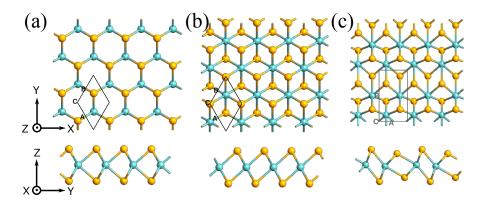


Figure 5.1. Top (top) and side view (bottom) of the atomistic structure of (a) 2H, (b) 1T, and (c) 1T' monolayer MoSe₂. MoS₂ and MoTe₂ have similar atomistic structures with different cell sizes. The primitive cells of 2H, 1T and 1T' structures are shown in the top view.

Recently, low contact resistance using metallic TMDs for the source and the drain of 2D-material FETs has been demonstrated [15], [140]–[142], [70], [16]–[18]. Figure 1 shows the atomistic configurations of

2H, 1T, and 1T' phases of monolayer MoSe₂ as an example. Different TMDs may have different stable phases, and 2H phase is most stable for many TMDs such as MoS₂ and MoSe₂. It was shown that 2H phase can be transformed into 1T or 1T' phase, and some 1T/1T' phases are stable at room temperature [70], [143]–[147]. Recently, 1T/1T'-2H TMD in-plane heterojunctions have been achieved experimentally [15], [140]–[142], [70], [16]–[18]. Subsequently, theoretical studies on the 1T/1T'-2H junction properties have also been reported [148]–[150]; however, most of them mainly discussed the material properties rather than the performance of devices based on such heterostructures. In addition, many previous works used ATK package for an integrated simulation of density functional theory (DFT) and non-equilibrium Green's function (NEGF), which makes it difficult to investigate and optimize material and device parameters independently. Moreover, when a combined DFT-NEGF approach is directly used, the size of a simulated device is restricted due to the computational limit in the DFT calculation. If NEGF device simulation could be performed separately from DFT material calculations, it would be more useful as device-level optimization could be done thoroughly. We do notice that there exists enough room to improve the performance of in-plane heterojunction TMD FETs reported earlier both experimentally and theoretically. For this kind of nanoscale devices based on novel material systems, direct experimental investigations could often be extremely challenging and expensive, and therefore, quantum transport simulation may provide a powerful tool for device engineering and useful insight into novel TMD-based in-plane heterostructure devices. We also note that there exists a previous study on the device performance of 1T-2H MoS₂ FET [149], in which, however, the exact Schottky barrier (SB) height was not rigorously evaluated based on the DFT calculation, unlike other previous studies [67], [148], [151].

In this study, we simulate 1T/1T'-2H MoX₂ (X = S, Se, Te) SBFETs. DFT calculations are used to achieve the SB height at the 1T/1T'-2H junction and the effective mass of the 2H channel. Then, we perform NEGF device simulations using the extracted parameters from the DFT calculations. First, we compare device performance of 1T/1T'-2H lateral heterojunction SBFETs based on MoS₂, MoSe₂ and MoTe₂. Then, we optimize the performance of those three devices using two different strategies: (i) by scaling equivalent oxide thickness (EOT) and gate underlap and (ii) by moderately doping the gate underlap region. Our simulation results reveal that the performance of MoX₂ heterojunction SBFETs can be optimized for either high-performance or low-power device applications if proper engineering design strategies are applied.

5.2 Simulation Method

5.2.1 DFT Calculation

The geometric optimizations of MoS₂, MoSe₂ and MoTe₂ are performed with the projector augmented wave (PAW) pseudopotential within generalized gradient approximation (GGA) exchange-correlation functional

and cut-off energy of 50 Ry using Quantum Espresso [152]. A Γ -centered grid of 21 \times 21 \times 1 k-points is used for variable cell optimization. A vacuum layer of 20 Å is used to avoid interactions. Unit cells are relaxed until the total force becomes less than 0.001 Ry/a.u. and the stress is less than 10^{-7} Ry/ a_0^3 (a_0 being Bohr radius) in all directions. The lattice constants of primitive cells for 2H MoS₂, MoSe₂ and MoTe₂ are 3.19, 3.33 and 3.55 Å, respectively. The thicknesses of monolayer MoS₂, MoSe₂ and MoTe₂ are 6.15, 6.47 and 6.98 Å, respectively [153]. The band structures of 2H and 1T/1T' monolayer MoX₂ are shown in Fig. 5.2. For all 2H phases, the conduction band bottom and the valence band top locate at the K point, forming a direct bandgap. For all three cases, 1T/1T' are metallic as their bands cross the Fermi level. 2H and 1T MoX₂ have hexagonal lattice structures [Fig. 5.1(a) and 5.1(b)], and 1T' MoX₂ has a rectangular lattice [Fig. 5.1(c)]. The bandgap (E_g) of 2H MoS₂, MoSe₂ and MoTe₂ are 1.71, 1.43 and 1.10 eV, respectively (Table I). The calculated values are close to the reported value from experiments: 1.85-2.0 eV for monolayer 2H MoS₂ [123], [154], 1.53-1.56 eV for monolayer MoSe₂ [155], [156], and around 1.10 eV for monolayer MoTe₂ [157], [158]. Effective masses for electrons and holes of 2H MoX₂ (Table 5.1) are extracted around the K point, which is used in the subsequent NEGF device simulations. We have chosen the zigzag direction being the transport direction (x) and the armchair direction as the transverse direction (y) because the inplane heterojunctions between 1T/1T' and 2H MoX₂ can only form along the zigzag direction.

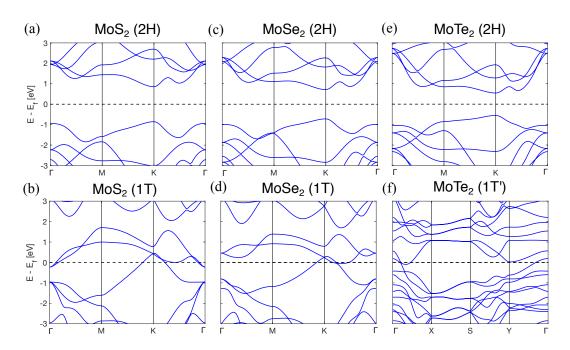


Figure 5.2 Band structure of monolayer (a) 2H MoS₂, (b) 1T MoS₂, (c) 2H MoSe₂, (d) 1T MoSe₂, (e) 2H MoTe₂, and (f) 1T' MoTe₂ along high symmetry points. Dashed lines indicate the location of the Fermi level.

Table 5.1 Bandgap (E_g), effective mass for electrons (m_e) and holes (m_h) along zigzag (x) and armchair (y) directions for 2H MoS₂, MoSe₂ and MoTe₂.

2H	E_g (eV)	$m_e^x (m_0)$	$m_e^y(m_0)$	$m_h^x(m_0)$	$m_h^y(m_0)$
MoS_2	1.71	0.58	0.56	0.73	0.67
$MoSe_2$	1.43	0.65	0.62	0.81	0.73
MoTe ₂	1.10	0.70	0.65	0.84	0.78

As suggested by experiments [15], [140]–[142], [70], [16]–[18], 1T/1T'-2H TMD heterostructures can reduce SB height to improve the overall device performance. It was reported that accurate values of SB height cannot be achieved from the difference of the metal work function and the electron affinity of semiconducting TMDs [159]. In addition, such a method cannot take into account the interaction between 1T/1T' and 2H TMDs. Therefore, we extract the SB height directly from 1T/1T'-2H heterojunctions using DFT calculation [160]. We construct 1T-2H heterostructure for MoS₂ and MoSe₂ and 1T'-2H heterostructure for MoTe₂ as shown in Fig. 5.3. 1T-2H MoSe₂, 1T-2H MoSe₂ and 1T'-2H MoTe₂ heterostructures were fabricated experimentally [15], [70], [140], [141], [161]. The supercell is periodic in x-, y- and z- directions. A vacuum layer in the z-direction is set to be 20 Å to avoid interactions. In constructing heterojunctions, lattice mismatch is inevitable although the difference in lattice constants for 1T and 2H MoX₂ could be minimal [148]. To form seamless in-plane heterojunction and minimize lattice mismatch, we maintain the cell size of semiconducting 2H MoX₂ and deform the metallic 1T/1T' MoX₂ to match its 2H counterpart, following the method used in previous works [151], [160], to evaluate SB height. We have confirmed that it has only minor impacts on the band structure of metallic MoX₂ as they still have gapless metallic properties with almost same density of states (DOS). It should be noted that there is no universal method for optimizing 1T/1T'-2H heterojunctions, which requires extensive research. It is beyond the scope of this study and suggested for a future work. The projected DOS (PDOS) is plotted for 2H MoS₂, MoSe₂ and MoTe₂ in the right panels of Fig. 5.3(a), (b) and (c), respectively, following the method specified in Ref. 35. The regions with zero DOS match the bandgap of the 2H MoX₂. The SB height of the heterojunction is achieved by subtracting the Fermi level from the conduction band edge [160]. The SB heights (Φ_{Bn}) of 1T-2H MoS₂ and MoSe₂ and 1T'-2H MoTe₂ heterojunctions are 0.70, 0.51 and 0.44 eV, respectively. Our results agree well with the reported values calculated using the DFT-NEGF method [148], [150].

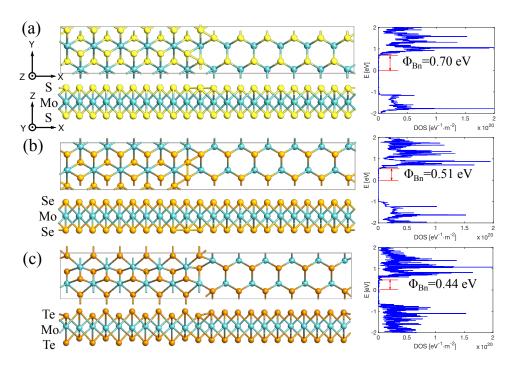


Figure 5.3 Atomistic structure of (a) 1T-2H MoS₂, (b) 1T-2H MoSe₂, and (c) 1T'-2H MoTe₂ heterojunctions (top: top view, bottom: side view) (left panels) and the projected density of states (PDOS) of their corresponding 2H MoX₂ (right panels).

5.2.2 NEGF Simulation

Figure 5.4(a) shows a schematic device structure of the simulated MoX₂ heterojunction SBFET. Intrinsic monolayer 2H MoX₂ is used for the channel. Seamless in-plane heterojunction is formed by using 1T (MoS₂ and MoSe₂) or 1T' (MoTe₂) MoX₂ for the source and the drain. A double-gate device geometry is used for a good electrostatic control. For a nominal device, we set the following device parameters: 3.1 nm-thick SiO₂ ($\kappa = 3.9$) is used for the top and the bottom gate oxide; the equivalent oxide thickness (EOT) is 3.1 nm with a 15-nm gate length (L_G) and 10-nm gate underlap (L_U). Device parameters such as gate underlap length, EOT and doping concentration in the gate underlap region will be varied to engineer the performance of the devices. The dielectric constants of 6.4, 7.4 and 8.9 are used for monolayer 2H MoS₂, MoSe₂, MoTe₂, respectively [162].

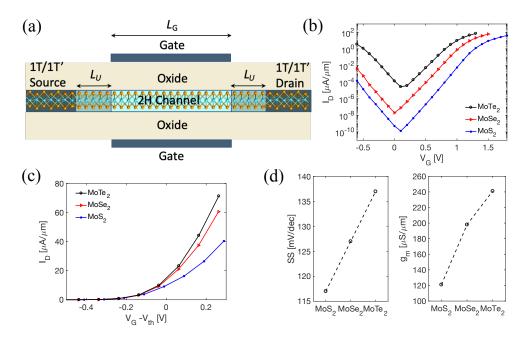


Figure 5.4 (a) Simulated device structure with a double-gate geometry. 2H MoX₂ is used for a channel and 1T/1T' phase is used for the source and the drain. (b) Log-scale I_D vs. V_G and (b) linear-scale I_D vs. $(V_G - V_{th})$ plot for Schottky barrier FETs based on 1T/1T'-2H heterojunction MoS₂, MoSe₂ and MoTe₂. (d) Subthreshold swing (SS) and transconductance (g_m) for the same devices.

Transport properties of MoX₂ heterojunction SBFETs are simulated using the non-equilibrium Green's function (NEGF) formalism within an effective-mass approximation, self-consistently with Poisson's equation. Electron current (I_n) and hole current (I_p) are calculated separately, and the total current is achieved by $I = I_n + I_p$. Due to the relatively short channel length considered in this study, ballistic transport is assumed. Anisotropic effective mass is used as shown in Table I. The effective mass of 1T/1T' MoX₂ is assumed to be free electron mass (m_0), and its variation has only a negligible effect on the simulation results [78], [163]. The coupling parameters are $t_0 = \frac{\hbar^2}{2m^*a^2}$ and $t_m = \frac{\hbar^2}{2m_0a^2}$ in channel and metallic source/drain regions, respectively, where m^* is the effective mass of the channel and a = 1 Å. A coupling parameter of $t_c = \frac{t_0 + t_m}{2}$ is used at the interface between metallic source/drain and semiconducting channel, where the SB height extracted from the DFT calculation is adopted. While both 1T/1T' and 2H MoX₂ are included for the NEGF calculation, the simulation domain for Poisson's equation is limited to the 2H channel region (including gate oxide) assuming flat bands for the 1T/1T' source and drain, as a previous DFT-NEGF study revealed that band bending of the source/drain in a 1T/1T'-2H heterostructure FET is negligible [151]. For electron current, virtual conduction band minimum is taken at 1 eV below the source/drain Fermi level; similarly, for hole current, virtual valence band maximum is chosen at 1 eV above the source/drain Fermi

level [78], [163]. The open boundary condition from semi-infinite source/drain extension is treated by self-energies $\Sigma_{S/D}$. Power supply voltage of $V_{DD} = 0.5$ V is used, and the room temperature is assumed.

5.3 Performance Comparison of Nominal MoX₂ Heterojunction SBFETs

First, we compare the performance of nominal devices. Figure 5.4(b) shows the I_D – V_G characteristics of SBFETs based on monolayer MoS₂, MoSe₂ and MoTe₂ lateral heterostructures. At a given gate voltage, MoTe₂ SBFET exhibits the largest current and MoS₂ SBFET shows the smallest, which is attributed to the inherent difference of electronic structure such as bandgap, effective mass and SB height. As it can be seen in Fig. 5.4(b), all three devices demonstrate ambipolar behaviors. Minimum current (I_{min}) is achieved when electron current (I_n) and hole current (I_p) are the same. MoTe₂ SBFET exhibits the largest I_{min} , which is due to the smallest bandgap of 2H MoTe₂ among the three. Similarly, MoS₂ SBFET shows the smallest I_{min} due to its largest E_g . To compare ON-state characteristics, we have plotted I_D vs. (V_G – V_{th}) by considering threshold voltage (V_{th}) shift in Fig. 5.4(c). Subthreshold swing (SS) and transconductance (g_m) of the three devices are compared in Fig. 5.4(d). Due to the largest SB height, MoS₂ SBFET exhibits the smallest SS and g_m . At the same time, due to the largest bandgap, MoS₂ SBFETs also show the largest ON/OFF current ratio (I_{on}/I_{off}) [see Fig. 5.4(b)]. It should be noted that the overall device performance of all three MoS₂ heterojunction SBFETs is far from optimization. Therefore, it is suggested to engineer various device parameters in order to achieve better device performance. For device performance optimization, we will use the MoS₂ heterojunction SBFET for our example in the subsequent discussion.

5.4 Engineering MoX₂ Heterojunction SBFETs by Scaling EOT and Gate Underlap

5.4.1 EOT Scaling

Efficient gate control is, in general, critical for the overall device performance of FETs. Small EOT is preferred for steep subthreshold slope, large I_{on}/I_{off} and large g_m . Better gate efficiency can be achieved by using double-gate geometry, high-κ dielectric, or thin gate oxide. In this work, we achieve small EOT by substituting SiO₂ with high-κ dielectric while keeping the physical thickness the same. Figure 5.5(a) shows I_D vs. (V_G – V_{th}) with various EOTs from 0.5 to 3.1 nm. A noticeable increase of I_{on} can be achieved with smaller EOTs at the same gate overdrive voltage after V_{th} shift due to the better electrostatic control with larger g_m . Figure 5.5(b) shows the log-scale I_D – V_G plot. It is observed that the subthreshold swing of both n-type and p-type branches becomes smaller as EOT decreases. The voltage for the minimum current (V_{min}) slightly increases (i.e., shifted to the right) with smaller EOT. This is due to the fact that SB height for holes (Φ_{Bp}) is greater than that for electrons (Φ_{Bn}) for the MoS₂ heterostructure. In this case, I_p is more susceptible to the change in EOT compared to I_n . In other words, by decreasing EOT, the increase of I_p is

greater than that of I_n , which leads to the right shift of V_{min} . For the n-type MoS₂ heterojunction SBFET, by varying EOT from 3.1 to 0.5 nm, SS can be reduced to 80 mV/dec from 117 mV/dec [Fig. 5.5(c)] and g_m increases by more than 5 times [Fig. 5.5(d)] by using ZrO₂ ($\kappa = 25$) for gate oxide instead of SiO₂.

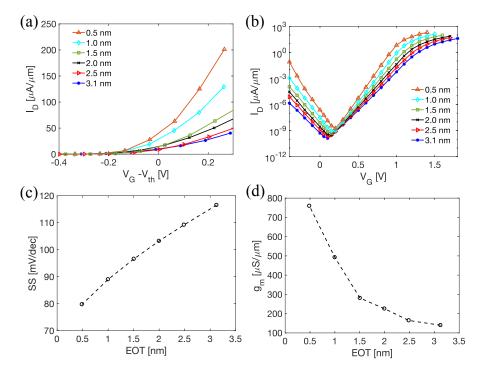


Figure 5.5 MoS₂ heterojunction SBFETs for EOTs from 0.5 to 3.1 nm (with the gate underlap length of 10 nm). (a) I_D vs. $(V_G - V_{th})$, (b) log-scale I_D vs. V_G . (c) SS and (d) g_m as a function of EOT.

5.4.2 Gate Underlap Scaling

Next, we investigate the effect of gate underlap scaling on the performance of MoS₂ heterojunction SBFETs by varying L_U from 0 to 10 nm. Figures 5.6(a) shows I_D – V_G characteristics for various lengths of gate underlap with an EOT of 0.5 nm. In general, a shorter gate underlap results in smaller V_{th} and larger I_{on} . By scaling L_U from 10 nm to 0 nm, SS reduces to 74 mV/dec from 80 mV/dec and g_m increases to 1370 μ S/ μ m from 760 μ S/ μ m [Fig. 5.6(b)]. This improvement stems from barrier thickness thinning at the source-channel interface. This can be even more prominent when EOT is large. Figure 5.6(c) shows the conduction band profile near the source-channel interface for L_U of 10 nm (dotted line) and 0 nm (solid line). For SBFETs, the current is, in general, affected largely by the Schottky barrier. When L_U is short, the gate control becomes more efficient, particularly near the source-channel interface. Consequently, the Schottky barrier becomes thinner, which leads to smaller SS and larger g_m .

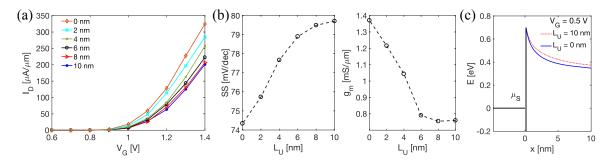


Figure 5.6 MoS₂ heterojunction SBFETs for various gate underlap lengths (L_U) from 0 to 10 nm (with EOT = 0.5 nm). (a) I_D – V_G characteristics, (b) SS and g_m as a function of L_U . (c) Conduction band profile near the source-channel interface for L_U = 0 nm (blue solid line) and 10 nm (red dotted line) (with EOT = 3.1 nm) at V_G = 0.5 V.

5.4.3 Performance Comparison of Scaled MoX₂ Heterojunction SBFETs

Using the scaled EOT and gate underlap discussed above, we compare the device performance of MoX₂ heterojunction SBFETs. I_D vs. ($V_G - V_{th}$) and log-scale $I_D - V_G$ characteristics are shown in Fig. 5.7(a) and 7(b), respectively. MoTe₂ SBFET demonstrates the highest I_{on} and the largest g_m , and MoS₂ SBFET shows the largest I_{on}/I_{off} , as observed for the nominal devices, due to the same reason discussed earlier. However, the overall device performance for all three devices was significantly improved, which can be seen by plotting I_{on} vs. I_{on}/I_{off} in Fig. 5.7(c), where dashed lines are for the nominal devices and the solid lines are for scaled devices. The curves are shifted from the bottom left to the top right corner (see an arrow), which indicates that both I_{on} and I_{on}/I_{off} are considerably improved. MoS₂ SBFET demonstrates the largest I_{on}/I_{off} while that of MoTe₂ SBFET is quite limited due to large I_{off} . The I_{on} of MoTe₂ SBFET can be most enhanced among the three devices by means of EOT and gate underlap scaling. MoSe₂ SBFET shows intermediate characteristics. Figure 5.7(d) shows the improvement of SS and g_m with EOT and gate underlap scaling. Compare to the nominal MoX₂ heterojunction SBFETs, SS is significantly reduced to 70-80 mV/dec from 120-140 mV/dec. g_m also benefits significantly from better gate control, and it can be improved by ~10 times compared to that of the nominal device.

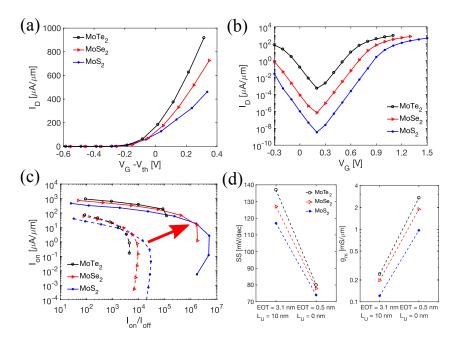


Figure 5.7 Performance comparison of MoS₂, MoSe₂ and MoTe₂ heterojunction SBFETs with no gate underlap and EOT = 0.5 nm. (a) I_D vs. (V_G-V_{th}) , (b) log-scale I_D-V_G , and (c) I_{on} vs. I_{on}/I_{off} . Dashed lines are for the nominal devices $(L_U = 10 \text{ nm}, \text{EOT} = 3.1 \text{ nm})$, and solid lines are for the scaled ones $(L_U = 0 \text{ nm}, \text{EOT} = 0.5 \text{ nm})$. (d) SS and g_m of the nominal and the scaled devices.

5.5 Engineering MoX₂ Heterojunction SBFETs by Doping Gate Underlap Region

So far, we have used EOT and gate underlap scaling to achieve the performance improvement of MoX_2 heterojunction SBFETs. However, in practice, scaling EOT and gate underlap requires advanced fabrication processes, which could be challenging. In this section, we try to enhance device performance in an alternative manner by using doping in the gate underlap region. Degenerate semiconductors are used for conventional silicon FETs to form Ohmic contacts, which requires high doping concentration, and it is practically channeling for 2D materials. Here we use moderate doping in the gate underlap region to achieve better device performance. The nominal MoS_2 SBFET was used below for the sake of discussion. Device parameters are the same as the ones used for the nominal device, except that moderate doping is used for the gate underlap region. Doping concentration (N_D) is varied from 0 to 5×10^{12} cm⁻² for n-type doping, which is achieved by varying the doping concentration directly in Poisson's equation. Gate metal work function is unchanged throughout the process.

5.5.1 Effect of Gate Underlap Doping on N-type Conduction

Figure 5.8(a) shows log-scale I_D – V_G characteristics with various N_D in the gate underlap regions. For n-type conduction (i.e., the right side of the I_D – V_G curve for the electron transport), SS decreases significantly to 62 mV/dec with 5.00×10^{12} cm⁻² from 117 mV/dec for the nominal device [Fig. 5.8(b)]. This superior

improvement in SS is due to the fact that the gate underlap doping makes SBFETs behave like 'Ohmic-contact' FETs. Figure 5.8(c) shows the potential profile with various N_D in a subthreshold region ($V_G = 0.5$ V). We can see that the potentials in the gated region (10 nm < x < 25 nm) are well controlled for all N_D values. For the nominal SBFET ($N_D = 0 \text{ cm}^{-2}$, blue line), the electrons tunnel through a relatively thick Schottky barrier at the source-channel interface. However, with increasing doping concentration, SB thickness becomes thinner due to the band bending. Consequently, the current with higher doping concentration can be significantly larger than that of the nominal device [see Fig. 5.8(a)]. As N_D increases, the SB becomes more transparent and Ohmic-like contacts are created. In addition, due to the barrier lowering in the gate underlap region, the conduction band profile in the channel region looks like that of a conventional metal-oxide-semiconductor (MOS) FET [see E_c at 5 nm < x < 30 nm in Fig. 5.8(c) for $N_D = 5.00 \times 10^{12} \text{ cm}^{-2}$]. Due to the Ohmic-like contacts and MOSFET-like band profile, the operation mechanism with gate underlap doping becomes analogous to that of conventional MOSFETs, and the SS with $N_D = 5.00 \times 10^{12} \text{ cm}^{-2}$ can be 62 mV/dec, which is close to the theoretical limit for the conventional MOSFET.

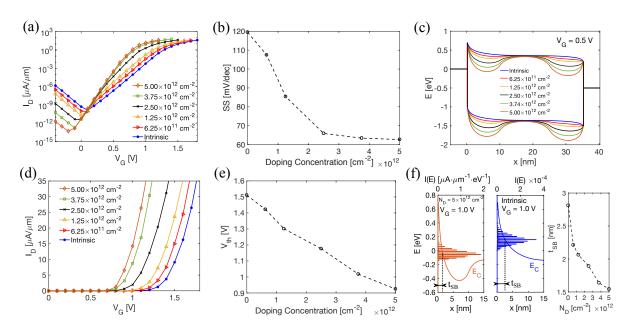


Figure 5.8 Effect of doping gate underlap regions. (a) Log-scale I_D – V_G and (b) SS with various doping concentrations (N_D). (c) Conduction band (E_c) and valence band (E_v) profile at V_G = 0.5 V. (d) Linear-scale I_D – V_G and (e) V_{th} for different N_D . (f) E_c profile near the source-channel interface (bottom x-axis) with energy-resolved current spectrum, I(E) (top x-axis) at V_G = 1.0 V for N_D = 5.00×10¹² cm⁻² (left panel) and the intrinsic case (mid panel). The right panel shows the thickness of SB (t_{SB}), which is obtained at the energy level giving the peak I(E).

Figure 5.8(d) shows linear-scale I_D – V_G characteristics for the same doping concentration used above in the gate underlap region. With increasing N_D , threshold voltage decreases, which can be seen in Fig. 5.8(e), where V_{th} as a function of N_D is plotted. This trend can be explained by comparing the potential profile and

SB thickness (t_{SB}) with two different N_D values in Fig. 5.8(f). At $V_G = 1.0$ V, the nominal device is in the subthreshold region, whereas the device with $N_D = 5.00 \times 10^{12}$ cm⁻² is in the ON state [see Fig. 5.8(d)]. For the nominal device, SB thickness is 2.8 nm at $V_G = 1$ V [the mid-panel in Fig. 5.8(f)], which is reduced significantly to 1.5 nm if $N_D = 5.00 \times 10^{12}$ cm⁻² is used [the left panel in Fig. 5.8(f)]. In addition, the peak of I(E) [shown with the top axes of the left and the mid panels in Fig. 5.8(f)] is also lowered, which increases the number of electrons injected from the source. Hence, if higher N_D is used in the gate underlap region, devices are turned ON at lower gate voltages, resulting in a negative V_{th} shift. The right panel of Fig. 5.8(f) shows t_{SB} (which is measured at the energy level showing a peak of the energy-resolved current spectrum) as a function of N_D at $V_G = 1.0$ V. This gives us an intuitive illustration of how doping in the gate underlap region can improve ON-state characteristics through barrier thinning and V_{th} shift.

5.5.2 Effect of Gate Underlap Doping on P-type Conduction

While SS of the n-type conduction improves significantly with N_D , that of p-type conduction [the left side of the I_D – V_G curve for the hole transport in Fig. 5.8(a)] is nearly unchanged with the doping concentration. This is due to the fact that p-type conduction is still based on tunneling through the SB at the channel-drain junction, unlike the n-type conduction that becomes MOSFET-like transport when gate underlap doping is used. In addition, it can be seen from Fig. 5.8(a) that I_{min} becomes smaller with higher doping. Figure 5.9(a) is I_{min} vs. N_D plot, where I_{min} of the device with $N_D = 5.00 \times 10^{12}$ cm⁻² is smaller by three orders of magnitude as compared to that of the nominal device. For the p-type conduction, the SB at the channel-drain interface becomes thicker with increasing N_D [the left panel of Fig. 5.9(b)]. Consequently, the peak location of I(E) is pushed away from the chemical potential of the drain and the magnitude of I(E) decreases exponentially as the doping increases [the right panel of Fig. 5.9(b)], making the total hole current smaller. In addition, as N_D increases, the subthreshold slope in the n-type conduction becomes steeper, which results in a smaller electron current in the deep subthreshold region (e.g., $V_G < 0.1$ V). Therefore, the minimum current exponentially decreases with increasing N_D since the total current is determined by $I_n + I_p$ where both I_n and I_p become smaller with doping at the relevant gate voltages of operation. This reduced I_{min} is preferred for low-power device applications as I_{on}/I_{off} can increase significantly.

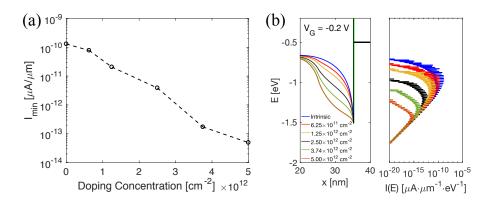


Figure 5.9 Effect of gate underlap doping on the minimum current and p-type transport. (a) I_{min} vs. N_D . (b) E_v profile near the channel-drain interface (left panel) and energy-resolved current spectrum (right panel) for various doping concentrations.

5.5.3 Performance Comparison of MoX₂ Heterojunction SBFETs with Doping in the Gate Underlap Regions

We compare the device performance of MoX_2 heterojunction SBFETs with doping in gate underlap regions. We have used $L_U = 10$ nm and $N_D = 3.75 \times 10^{12}$ cm⁻² for all three devices based on MoS₂, MoSe₂ and MoTe₂. Figure 5.10(a) and 10(b) are I_D vs. $(V_G - V_{th})$ and log-scale $I_D - V_G$ characteristics, respectively. While overall trends are similar to those of nominal devices, significant performance improvement is observed. Figure 5.10(c) compares I_{on} vs. I_{on}/I_{off} of the devices with gate underlap doping (solid lines) against those of nominal devices (dashed lines). The curves are shifted to the right, indicating that significant improvement is achieved for I_{on}/I_{off} by three orders of magnitude with doping in the gate underlap region. The quantitative comparisons of SS and g_m are given in Fig. 5.10(d). With gate underlap doping, all three devices show a nearly ideal SS of 63-68 mV/dec, unlike the nominal devices. However, the improvement in g_m is quite limited. Least improvement was observed with MoS₂, while g_m of MoSe₂ and MoTe₂ SBFETs could be increased by 41% and 32%, which is, however, relatively insignificant compared to performance improvement through EOT and gate underlap scaling [see the right panel of Fig. 5.7(d)]. As discussed earlier, doping in the gate underlap region transforms an SBFET into a MOSFET-like device, where the top of the channel potential barrier is manipulated by the gate voltage, in the OFF states. However, when high V_G is applied and the channel potential barrier becomes low, the transport is still affected mainly by the SB, which doesn't show a noticeable difference with varying N_D . Therefore, the improvement in g_m in Fig. 5.10(d) is limited, and the curves in Fig. 5.10(c) are shifted only to the right without showing significant improvement in I_{on} .

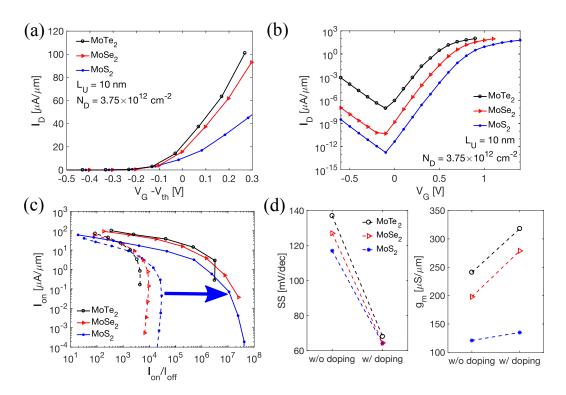


Figure 5.10 Performance comparison of MoS₂, MoSe₂ and MoTe₂ heterojunction SBFETs with doped gated underlap region ($N_D = 3.75 \times 10^{12} \text{ cm}^{-2}$). (a) I_D vs. ($V_G - V_{th}$) and (b) log-scale $I_D - V_G$. (c) I_{on} vs. I_{on}/I_{off} where dashed lines are for nominal devices and the solid lines are with gate underlap doping. (d) SS and g_m comparison between the nominal devices and the ones with gate underlap doping.

5.6 Design Strategies

In sections 5.4 and 5.5, we have investigated two different approaches to optimize device performance. By using scaled EOT and gate underlap (EOT = 0.5 nm, L_U = 0 nm), both ON and OFF-state characteristics could be improved adequately. On the other hand, if moderate doping is used in the gate underlap region within our nominal device structure (EOT = 3.1 nm, L_U = 10 nm), we could achieve nearly ideal SS (down to 62 mV/dec) but an only negligible gain for the ON-state characteristics. Figure 5.11 summarizes the observations from our simulations, where MoS₂ heterojunction SBFETs are used again for the sake of discussion. A red arrow indicates that both I_{on} and I_{on}/I_{off} are improved with EOT and gate underlap scaling. For example, for I_{on}/I_{off} = 10^3 , I_{on} is increased by 23 times. This kind of device engineering would be favorable for high-performance device applications. On the other hand, a blue arrow indicates that gate underlap doping can be used for low-power device applications as it can significantly enhance I_{on}/I_{off} . For instance, by using N_D = 3.75×10^{12} cm⁻², maximum-achievable I_{on}/I_{off} could be more than 10^7 , which is larger than that of the nominal device by three orders of magnitude.

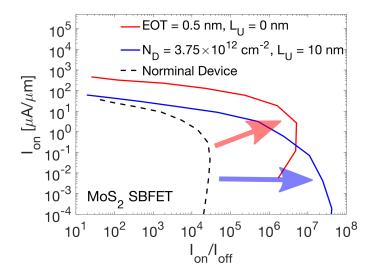


Figure 5.11 I_{on} vs. I_{on}/I_{off} comparison for MoS₂ SBFETs. The nominal device is shown with a dashed line; the device with EOT and gate underlap scaling with a red solid line; the device with gate underlap doping with a blue solid line.

5.7 Discussion and Conclusion

In this study, we have not considered Fermi level pinning, which might be caused by an imperfection in reality. In that case, SB height at the 1T/1T'-2H MoX₂ junction could be affected and differ from the values calculated by DFT. Nonetheless, the engineering methods, analyses and qualitative conclusions of this study would still remain the same.

It should be pointed out that device performance could not be improved further by applying both optimization methods simultaneously. For example, if gate underlap doping (with $N_D = 5.00 \times 10^{12}$ cm⁻²) is used along with EOT and gate underlap scaling (EOT = 0.5 nm; $L_U = 5$ nm), device performance is similar to that of the scaled SBFET discussed in Section B. This is because the effect of gate underlap doping becomes minimal due to the strong electrostatic control by the gate through thin EOT and short gate underlap. This suggests to avoid excessive scaling when designing a MOSFET-like device through gate underlap doping.

In summary, we discussed the performance of in-plane heterojunction SBFETs based on 1T/1T'-2H MoS₂, MoSe₂, MoTe₂. We extracted SB height and effective mass from DFT calculations, and NEGF simulations are performed for the transport behaviors. Their inherent device performance can be limited mainly by Schottky contacts, and engineering of device parameters was suggested to achieve better performance using two possible approaches: (i) EOT and gate underlap scaling, and (ii) moderate doping in the gate underlap region. If better gate control is achieved by means of EOT andww gate underlap scaling, ON-states characteristics such as I_{on} and g_m can be largely enhanced along with noticeable improvement in the OFF-state performance, making the device more suitable for high-performance applications.

Alternatively, if moderate doping is used in the gate underlap region, steep switching and superior I_{on}/I_{off} can be achieved. Although only minimal gain can be expected for the ON-state characteristics, gate underlap doping could be suggested for the fabrication of low-power electronic devices.

Chapter 6 Electron Transport through 1T-2H MoS₂ Interface: Top Contact vs. Side Contact

6.1 Introduction

Two-dimensional (2D) material attracts significant attention for the next-generation transistor. The advantages of 2D materials reside in their naturally passivated surfaces, the great electrostatic control due to atomistic thickness, and high carrier mobility. Transition metal dichalcogenides (TMDs) are one of the promising 2D materials. Among the many TMDs, MoS₂ is the most significantly studied [13], [132], [135]. One of the main challenges towards high-performance transistors is the contact problem. It is reported that the contact resistance can be as low as 200 Ω μm by using metalized 1T MoS₂ electrodes [15]. Similar works are reported in 1T'–2H MoTe₂ heterojunction transistors [16]–[18], [70] and 1T–2H WSe₂ heterojunction transistors [19]. These works reduce contact resistance and the Schottky barrier by introducing in-plane metallic-semiconducting heterojunction. It is well known that the side contact is more favorable for low contact resistance, and related works have been investigated extensively, especially the contact between conventional metal to 2D material [164]–[167].

In this work, 1T–2H MoS₂ heterojunctions with different geometries are examined by atomistic simulations. We extract accurate maximally localized wannier functions (MLWF) from DFT simulations. The Schottky barrier height is extracted from DFT simulations of top contact and side contact junctions. We calculated the conductance from NEGF formalism at zero bias. The simulation results suggest side contact is more favorable for conducting current. The oscillations of conductance are carefully studied and compared to the conductance oscillation in semiconducting mono-bi-monolayer black phosphorus (BP) heterojunctions. The current flow patterns are presented, showing the edge state is critical in determining conductance and current flow patterns. Extended studies of modifying weak van der Waals interactions at the edge are performed, suggesting a potential method for better contact property in metal-semiconductor top-contact junctions.

6.2 Simulation Method

6.2.1 General DFT Simulation Settings

The atomic structures of 2H, 1T, and AB1 stacking 1T2H MoS₂ are shown in Figure 6.1. The geometric optimizations of all structures are performed with the projector-augmented wave (PAW) pseudopotential and cut-off energy of 50 Ry, using Quantum Espresso [168]. A Γ -centered grid of 21 × 21 × 1 k-points is used for variable cell optimization for 2H and 1T MoS₂ primitive cell. A vacuum layer of 20 Å is used to avoid interactions in the z-direction. Primitive cells are relaxed until the total force becomes less than 0.001

Ry/a.u. and the stress is less than 10^{-7} Ry/ a_0^3 (a_0 being Bohr radius) in all directions. The 2H and 1T MoS₂ primitive cells are both hexagonal lattices, with a 3.19 and 3.20 Å lattice constant. To minimize the lattice mismatch in 1T2H bilayer system, the 1T and 1T2H MoS₂ primitive cells are relaxed by a fixed cell optimization with the lattice constant of 3.19 Å. The strain in 1T MoS₂ is defined as $\Delta = \frac{a_{2H} - a_{1T}}{a_{2H}} = 0.31$ %. Because the lattice mismatch is small, the bands of strained 1T MoS₂ (blue solid line) are quite similar to free-standing 1T MoS₂ (red dotted line).

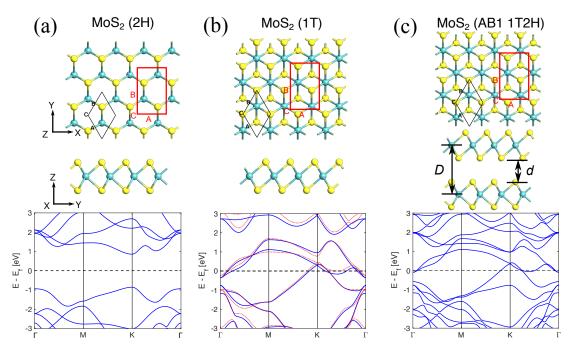


Figure 6.1Top view and side view of optimized atomic positions of (a) 2H MoS₂ (b) 1T MoS₂ (c) AB1 stacking 1T2H MoS₂ with the 2H lattice constant and their corresponding band structures. The red dotted lines in 1T MoS₂ bands stand for free-standing 1T, and the blue lines are for strained 1T with the 2H lattice constant. The primitive cells are shown in the black panel. The red panels denote the supercells used for quantum transport simulation.

For 1T2H MoS₂, due to van der Waals interaction between 2H and 1T layer, the band structure is not the overlay of 2H and 1T MoS₂ bands. Van der Waals density functionals (vdW-DF2) is used for electron density, along with a semi-empirical pairwise interatomic dispersion interaction of DFT-D method, to address the vdW interactions appropriately.

6.2.2 Stacking Modes in Bilayer 1T2H MoS₂

The potential stacking modes are studied and shown in Figure 6.2. The five different types are named according to the names of bilayer TMDs [169] and classified as three types: (1) All the Mo(S) atoms of the bottom 2H layer are placed under the Mo(S) atoms of the top 1T layer (S atoms of 2H under lower S atoms of 1T layer for AA1; under upper S atoms of 1T layer for AA2); (2) All the Mo(S) atoms of the bottom 2H

layer are placed under the S(Mo) atoms of the top 1T layer (S atoms of 2H under lower S atoms of 1T layer for AB1; under upper S atoms of 1T layer for AA2); (3) Staggered stacking from AB stacking mode. These polytypisms can be transformed from one to another by sliding in *y*-directions or by rotating around the *z*-axis. The total energy is calculated for all five structures, and the energy differences are listed in Table 1. Here we set the AB1 stacking 1T2H MoS₂ as a reference because it has the lowest energy. The AB2 stacking has the second-lowest total energy, with only a 1.633 meV difference per primitive cell. The AB1 and AB2 stacking modes have almost the same Mo-Mo distance (*D*) and interlayer distance (*d*). The AA2 stacking has the third-lowest total energy and the almost same interlayer distance. The lower stability may come from stronger Pauli repulsions between the Mo atoms on the same site. The less stable AC1 and AA1 stackings have a noticeable larger interlayer distance, suggesting a stronger repulsive force between the 1T and 2H layers.

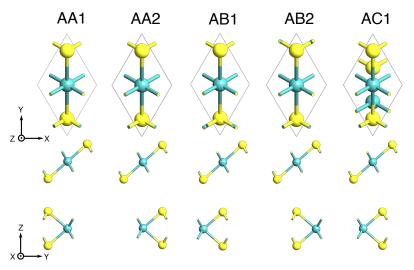


Figure 6.2 Top view and side view of optimized atomic structure of 1T2H MoS₂ in different stacking mode: (a) AA1 (b) AA2 (c) AB1 (d) AB2 (e) AC1

The band structures of these five-stacking modes 1T2H MoS₂ are quite similar. Here we analyze the bands contributed from the bottom 2H MoS₂. The conduction band bottom (E_C), valence band top (E_V), and bandgaps (E_g) are summarized in Table 1. Due to van der Waals interaction, the bottom 2H MoS₂ also contributes slightly to the bands near E_f . At the same time, bandgaps are all slightly larger than the free-standing 2H MoS₂ with 1.711 eV as predicted by DFT. Besides the contribution from interlayer van der Waals interaction, the atomic positions are also slightly changed due to structural optimization. Some works refer to the difference between the E_C and E_f as the "vertical Schottky barrier," in contrast to the usual Schottky barrier in SBFETs. This vertical Schottky barrier is included in the band alignment in the MLWF matrix. For all the 2H, 1T, and 1T2H MoS₂ supercells, MLWF matrix are extracted by wannier90, where the d orbitals (d_{z^2} , d_{xz} , d_{yz} , d_{xy} , $d_{x^2-y^2}$) are considered for the Mo atoms, and the p orbital (p_x , p_y , p_z) are

considered for the S atoms. For all the 2H, 1T and 1T2H MoS₂ supercells, MLWF matrix are extracted by wannier90 [74], where the d orbitals (d_{z^2} , d_{xz} , d_{yz} , d_{xy} , $d_{x^2-y^2}$) are considered for the Mo atoms, and the p orbital (p_x , p_y , p_z) are considered for the S atoms. Which gives a 22 by 22 Hamiltonian matrix for 1T and 2H MoS₂, and a 44 by 44 Hamiltonian matrix for 1T2H MoS₂.

Table 6.1 Comparison between the fixed cell relaxed vdW-DF2 bilayer 1T2H MoS₂. The bandgaps contributed from the bottom 2H layers are also summarized here.

MoS_2	AA1	AA2	AB1	AB2	AC1
$E - E_{min}$ (meV)	91.974	14.286	0	1.633	22.858
$D\left(\right.$ Å)	6.795	6.334	6.335	6.334	6.422
d (Å)	3.531	3.076	3.075	3.075	3.160
E_C of 2H (eV)	1.017	0.9711	0.987	1.015	0.986
E_V of 2H (eV)	-0.719	-0.768	-0.755	-0.717	-0.752
E_g of 2H (eV)	1.736	1.739	1.742	1.732	1.738

6.2.3 Schottky Barrier Height

The side contact and the top contact heterojunctions are constructed and shown in Figure 6.3 to extract the Schottky barrier between metallic 1T and semiconducting 2H MoS₂. Here we mainly compare the side contact and the top contact with AB1 stacking, as AB1 1T2H MoS₂ is the most stable structure. The top contacted heterojunction with AA2 stacking is also shown here as this represents the most stable structure in AA stacking mode. The projected density of states (PDOS) is plotted in the right panels of Fig. 6.3(a), (b), and (c), following the method specified in Ref. [160]. The regions with zero DOS match the bandgap of the free-standing 2H MoS₂. The SB height of the heterojunction is achieved by subtracting the Fermi level from the conduction/valence band edge. The SB heights (Φ_B) of side contact, top contact with AB1 stacking, and top contact with AA2 stacking heterojunctions are 0.70 (n-type), 0.72 and 0.74 eV (p-type), respectively [160]. The regions with zero DOS match the bandgap of the 2H MoS₂. The SB height of the heterojunction is achieved by subtracting the Fermi level from the conduction/valence band edge. The SB heights (Φ_B) of side contact, top contact with AB1 stacking, and top contact with AA2 stacking heterojunctions are 0.70 (n-type), 0.72 and 0.74 eV (p-type), respectively.

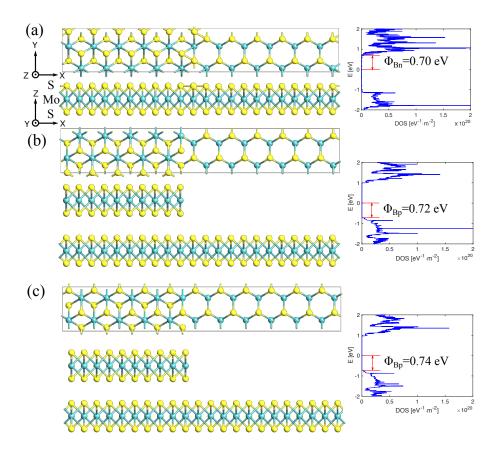


Figure 6.3 Top view and side view of the atomic positions along the transport direction of 1T-2H MoS₂ heterojunctions (a) Side contact (b) Top contact with AB1 stacking (c) Top contact with AA2, and their corresponding extracted barrier height.

6.3 Results and Discussion

6.3.1 1T-2H MoS₂ Side Contact

The atomic structure of side contact 1T-2H MoS₂ heterojunction is shown in Figure 6.4(a). The electron transport properties are studied by non-equilibrium Green's function (NEGF) formalism within an MLWF approximation at equilibrium state. The 1T and 2H MoS₂ lengths are set as 3.2 nm. The 1T MoS₂ is highlighted with a light blue background. Figure 6.4(b) shows the schematic device Hamiltonian matrix with 1T MoS₂ in the top left corner and 2H MoS₂ in the right bottom corner. The H matrix is extracted from free-standing 1T and 2H MoS₂ supercells. The bands are aligned to match the Schottky barrier extracted in Fig. 6.3(b). The only unknown part for device simulation is the coupling matrix at the interface. It has been reported that the coupling matrix at the interface has negligible effects on device transport properties in lateral heterojunctions [149], [170]. It has been reported the choosing of coupling matrix at interface has small effect to device transport properties in lateral heterojunctions [149], [170]. Here we test the effect of coupling matrix with three different settings: by using the coupling between neighbor cells from 1T, from

2H, and the average of the two. Here we compare the conductance of the junction from the NEGF formalism $G(E) = \frac{2q^2}{h}T(E)$, where $T(E) = trace(\Gamma_s G^r \Gamma_D G^{r+})$ is the transmission calculated from recursive Green's function. $G^r = [(E+i0^+)I - H - \Sigma_S - \Sigma_D]^{-1}$ is the retarded Green's function, $\Gamma_{S/D} = i(\Sigma_{S/D} - \Sigma_{S/D}^+)$ is the broadening function, and $\Sigma_{S/D}$ is the self-energy matrix at semi-infinite source and drain, which is calculated by recursive surface green's function. Here the transport behaviors are investigated assuming $k_y = 0$ for two reasons: 1) The conduction band bottom and valence band top of 2H MoS₂ locate at K point, which is captured by assuming $k_y = 0$; 2) For fast convergence. Comparisons of $k_y = 0$ and $k_y = 201$ from 0 to π/b are carefully tested, showing a very small difference. And $k_y = 0$ is assumed for all following works. From Fig. 6.4(c), we can see the difference in conductance with three settings. However, the overall shape is quite similar. Here we use the average of coupling from 1T and 2H as the interface coupling matrix.

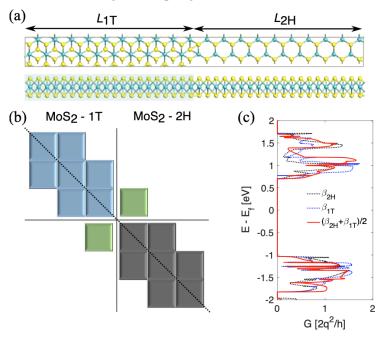


Figure 6.4 (a) Schematic of the atomic structure of side contact 1T-2H MoS₂ heterojunction (b) Schematic of device Hamiltonian matrix with 1T MoS₂ in up left corner and 2H MoS₂ in the bottom right corner. The coupling at the interface is denoted by green blocks. (c) Conductance comparison with different coupling at the interface.

6.3.2 1T-2H MoS₂ Top Contact

The top contact 1T-2H MoS₂ heterojunction, as shown in Figure 6.5(a), is formed through van der Waals interactions. The schematic device Hamiltonian is demonstrated in Fig. 6.5(b). The Hamiltonian matrix for 1T, 2H, and 1T2H MoS₂ are extracted from free-standing supercells, respectively. The coupling matrix at two interfaces is extracted from the bilayer 1T2H MoS₂ system, as shown in Fig. 6.5(c). For the 1T-1T2H interface, the interlayer interactions can be extracted from two neighboring 1T2H MoS₂ cells, with the

bottom 2H layer in the left is replaced with vacancy. This 22 by 44 matrix highlighted by green blocks represents the van der Waals interactions between metallic 1T in the left and metallic 1T2H MoS₂ in the middle. Similarly, for the 1T2H-2H interface, the 44 by 22 matrix represented by yellow blocks is extracted from neighboring 1T2H MoS₂ cells with 1T layer in the right replaced by the vacancy.

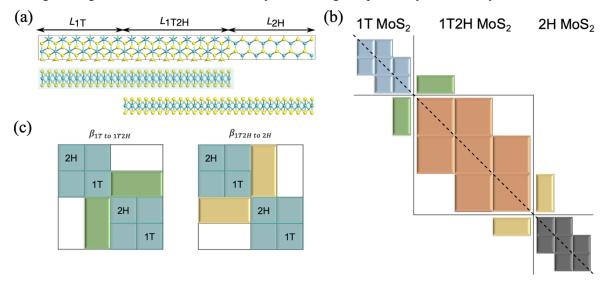


Figure 6.5 (a) Schematic of the atomic structure of top contact AB1 stacking 1T-2H heterojunction (b) Schematic of device Hamiltonian matrix with 1T, 1T2H, and 2H MoS₂ blocks, the coupling at two interfaces are denoted by green and yellow blocks (c) Schematic of the extracted coupling matrix at the interface.

The conductance of the top contact 1T-2H MoS₂ heterojunction is closely related to the 1T2H MoS₂ length. Space projected conductance plot with L_{1T2H} ranging from 0 nm to 9.6 nm and $L_{1T} = L_{2H} = 3.2$ nm is shown in Figure 6.6(a). The bandgap from the conductance plot fits the E_g calculated from DFT. The energy ranges around E_C and E_V are critical in determining the current of transistors. The zoomed-in plots around E_C and E_V are shown in Fig. 6.6(b). We notice when L_{1T2H} is smaller than 1 nm, the conductance is small in all energy range. This suggests electron/hole transport is inhibited because of too short overlap length. When L_{1T2H} is larger than 1nm, the overall shape of G is similar. However, a close look at the conductance near E_C and E_V suggests it oscillates with 1T2H length. For shorter L_{1T2H} , the conductance peaks are more localized compared to longer L_{1T2H} . The conductance plots with different L_{1T2H} at specific energies are shown in Fig. 6.6(c). For example, at the energy 0.1 eV above E_C and 0.1 eV below E_V , conductance oscillates between large and small values in a period around 1–2 nm. This may come from quantum confinement in the bilayer section.

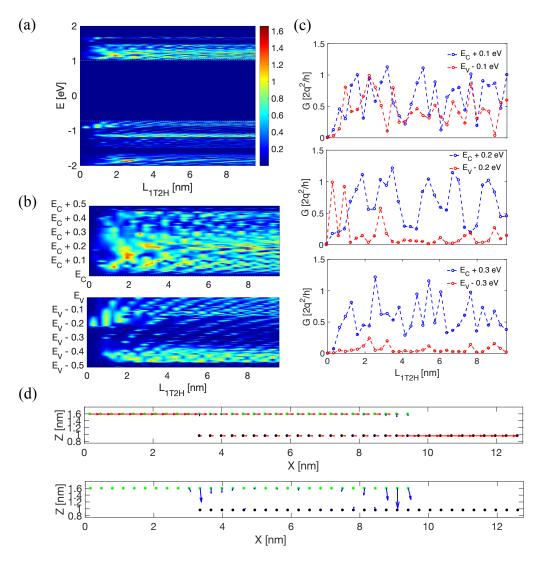


Figure 6.6 (a) Space projected conductance plot of top contact AB1 stacking 1T-2H MoS₂ with L_{1T2H} from 0 to 9.6 nm (b) Zoomed in space projected conductance plot around E_C and E_V (c) Comparison of conductance at different energies (d) Current flow pattern with $L_{1T} = L_{2H} = 3.2$ nm, $L_{1T2H} = 6.4$ nm. Green dots represent one 1T MoS₂ cell, and black dots represent one 2H MoS₂ cell along the transport direction. The bottom figure used a larger ratio to show the interlayer current flow pattern more clearly.

Similar conductance oscillation has been reported in stacking graphene nanoribbons [171]. However, the top contacted AB1 stacking 1T-2H MoS₂ system shows weaker oscillations compared to the graphene nanoribbons (GNRs) system. It may because the orbitals in MoS₂ are much more complex than GNRs. At the same time, heterojunction formed by metallic 1T and semiconducting 2H MoS₂ is expected to demonstrate different behavior compared to junctions formed by two semi-metallic graphene flakes. One of the interesting questions is, in the region of bilayer 1T2H part, will electron prefer metallic 1T rather than semiconducting 2H MoS₂? Here we simulated the current flow pattern to investigate this question. The

rectangular supercell for 1T and 2H MoS₂ is considered as gird points for the current flow. The current from pth cell to qth cell in an energy range between E_1 and E_2 , which is nonzero only when these two cells are nearest neighbors, is calculated by

$$I_{p\to q} = \frac{2q}{h} \int_{E_1}^{E_2} dE \, Im \big[G_{p,q}^n(E) H_{q,p} - H_{p,q} G_{q,p}^n(E) \big]$$

Where $G_{p,q}^n(E)$ is the (p,q) submatrix in $G^n(E)$, and $H_{q,p}$ is the (p,q) submatrix in the device Hamiltonian matrix. In Figure 6.6(d), monolayer 1T and 2H MoS₂ are both 3.2 nm, and bilayer 1T2H MoS₂ is 6.4 nm. The 1T MoS₂ supercells are represented by green dots, and 2H MoS₂ supercells are represented by black dots. The upper plot demonstrates interlayer interactions (blue arrows) and intralayer interactions (red arrows) with a common scale bar within the energy range of $|E| \le 2$ eV. Because of the weak van der Waals interactions, interlayer current flow is much smaller than intralayer current flow. Current flow is gradually transferred from the top 1T layer to the bottom 2H layer. A zoomed-in plot showing only the interlayer current flow with a smaller scale bar is shown at the bottom. It indicates the majority of current transfer happens around two interfaces at 1T edge and 2H edge. And the 1T MoS₂ edge is the dominant one. In the middle region, current oscillates between the top 1T layer and bottom 2H layer. The results suggest the importance of edge states in this kind of top-contact metallic-semiconducting heterojunctions.

6.3.3 Mono-bi-monolayer BP Heterojunction

To fully understand the effect of staggered stacking in top contact, mono-bi-monolayer black phosphorus (BP) heterojunction is constructed as shown in Figure 6.7(a). Here we adopt a tight-binding (TB) approximation for the device Hamiltonian matrix [73]. The monolayer BP has a bandgap of 1.52 eV, and bilayer BP has a bandgap of 1.12 eV. The bands are aligned where E_i of monolayer and bilayer BP locate at 0 eV. The space projected conductance plot is shown in Figure 6.7(b). In the energy range of $|E| \le$ 0.56 eV, conductance is zero as this is determined by the bandgap of middle bilayer BP. In the energy range of $0.56 \le |E| \le 0.76$ eV, conductance is small as we are assuming semi-infinite monolayer BP source and drain, and this is still within the E_g of monolayer BP. The conductance oscillation is more significant in mono-bi-monolayer BP heterojunction than in the top contacted 1T-2H MoS₂ heterojunction. The junction is turned on and off in a period of bilayer region length. A detailed comparison of conductance at various energies is plotted in Figure 6.7(c). At the energy 0.1 eV above E_C and 0.1 eV below E_V , conductance is small. And the junction is turned on and off in a period L_{bi} around 2 nm for electrons. For holes, the conductance is slightly shifted to the left. This is due to the quantum well formed by monolayer and bilayer BP bands along the transport direction. For example, the EC forms a well with 0.2 eV depth in energy. The difference between conductance for electrons and holes is expected to be related to the significant difference between the effective mass of electrons and holes in monolayer and bilayer BP. At the energy 0.3 eV above E_C and 0.3 eV below E_V , this is out of the quantum well formed by E_C , and more like a ballistic transport situation. The conductance becomes larger, and the junction is turned on and off in a period L_{bi} around 4 nm for electrons and 2 nm for holes. It is also expected to be related to the effective mass difference in electron and hole. Another noticeable difference is the conductance is close to zero when $L_{bi} < 2$ nm.

It suggests mono-bi-monolayer BP heterojunction can be considered "broken" if bilayer length is not long enough. The current flow pattern is also investigated. An example of $L_{mono} = 2.3$ nm and $L_{bi} = 9$ nm is shown in Figure 6.7(d) in the energy range of $|E| \le 2$ eV. The oscillation of current flow between top and bottom layer is more significant compared to top contact 1T-2H MoS₂ heterojunction. The edge state is not substantial, and the current flow is uniformly and periodically distributed along the bilayer region. The interlayer current flow is stronger than the 1T-2H top contact junction, suggesting stronger van der Waals interactions in mono-bi-monolayer BP junction.

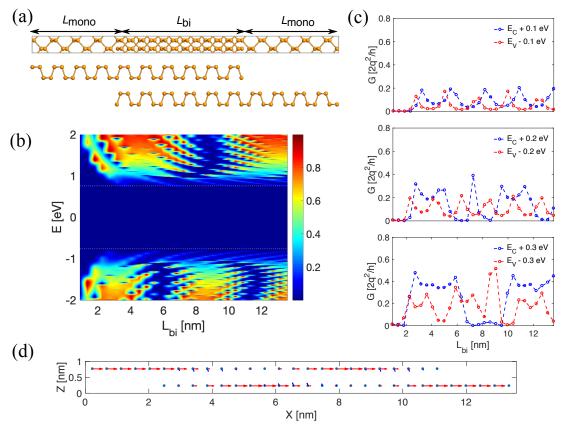


Figure 6.7 (a) Schematic of atomic structure of mono-bi-mono BP junction (b) Space projected conductance plot with L_{bi} from 1 to 13 nm (c) Comparison of conductance at different energies (d) Current flow pattern with $L_{mono} = 2.3$ nm and $L_{bi} = 9$ nm.

6.3.4 Comparison between Top Contact and Side Contact

We come back to the question of how is the $1T-2H MoS_2$ top contact compared to the $1T-2H MoS_2$ side contact. We constructed an artificial structure shown in Figure 6.8(a). Here top contact and side contact is

compared within one device. In the left region, another 1T MoS₂ is connected to the bottom 2H MoS₂ layer using the same coupling as in the side contact 1T-2H junction. It is assumed no interaction between top 1T MoS₂ and bottom 1T MoS₂ to mimic independent current injection. And same MLWF is used for the top and bottom 1T MoS₂. A recursive surface green's function is used to calculate Σ_S assuming same semiinfinite 1T MoS₂ source for top and bottom layers. The bands are aligned the same to the top contact situation, where we assume a $\Phi_{Bp} = 0.72$ eV at the 1T2H and 2H interface. At the 1T/1T and 1T2H interface, a $\Phi_{Bp} = 0.76$ eV is read from Table 6.1 for the artificial 1T-2H side contact. The current flow pattern is shown in Figure 6.8(b) with $L_{1T/1T} = L_{1T2H} = L_{2H} = 0.32$ nm. We can see the current is larger in the bottom layer at the left end, suggesting side contact is more favorable for current. In the 1T2H MoS₂ part, the current gradually transferred from the top 1T layer to the bottom 2H layer, similar to the top contact situation. Again, the majority of current transferring happens at the edges. The current flow pattern stays almost the same with changing junction length. A comparison of conductance between top contact, side contact, and this artificial structure is shown in Figure 6.8(c). As the energies around E_C and E_V are critical in determining current, the zoomed-in plots are given on the right side. In the energies close to E_C and E_V , the artificial contact demonstrates the largest conductance. But not simply the sum of the conductance of top contact and side contact.

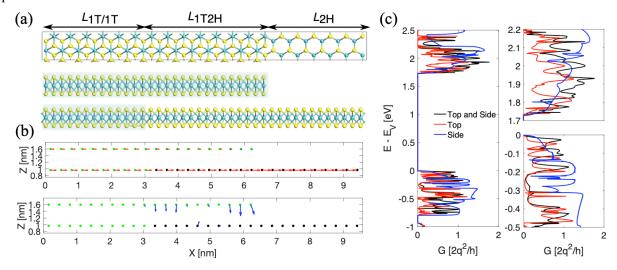


Figure 6.8 (a) Atomic structure of constructed MoS_2 junction having both top contact and side contact (b) Current flow pattern with zoomed-in for interlayer current flow (c) Comparison of conductance with zoomed-in for energies around E_C and E_V .

6.3.5 Engineering Edge States in Top-Contact 1T-2H MoS₂ Junction

From our previous results, we find edge state is extremely important in determining conductance and current flow pattern. In the experiment, edge states can be more complex due to various defects or contaminations. For example, vacancies, dislocations, grain boundaries, and so on. These defects will affect

the van der Waals interactions between two layers. Here we will not discuss how defects change interlayer interactions. We consider the extreme cases of no coupling and strong covalent coupling. Three situations will be discussed, shown in Figure 6.9(a). And the current flow pattern is compared in Fig. 6.8(b) using a common scale bar. The conductance is then compared in Fig. 6.9(c). In the first set: the interlayer interaction is replaced by a zero matrix. It represents no van der Waals interactions at 1T edge. We find the cells near the edge are still important from the zoomed-in plot for interlayer current flow pattern. As there's no van der Waals interaction between the rightmost cell in the top 1T layer to bottom layer, the only coupling is the vertical tunneling from the top 1T cell to the bottom 2H at the same site in the 1T2H section. From the conductance comparison, we find the difference compares to the original top contact is very small. This result is under the assumption that only the interlayer van der Waals interaction at 1T edge is affected. It supports this van der Waals interaction itself is a weak coupling. The second situation assumes the coupling at the interface is the same as the intralayer covalent coupling between neighbor cells in 2H MoS₂. The current flow pattern is significantly changed compared to the original situation. With this strong coupling at the interface, the electron will prefer the top 1T layer and transfer to the bottom 2H layer at the very end edge. And the interlayer current is as strong as the intralayer current. Under this assumption, no more oscillations in conductance as electrons always prefer the top metallic 1T layer. From the conductance plot in Fig. 6.8(c), we can see the this is better than the original top contact. The third situation assumes the coupling at the interface is the same as the intralayer covalent coupling between neighbor cells in 1T MoS₂. It is expected this coupling is even stronger than in semiconducting 2H MoS₂. We have a similar current flow pattern and even larger conductance, as shown in Fig. 6.9(b) and (c). In practice, the conductance can be smaller than set 2 and set 3. These two sets suggest the upper limits of top contact to be similar as side contact. However, it proposes the edge engineering for future work.

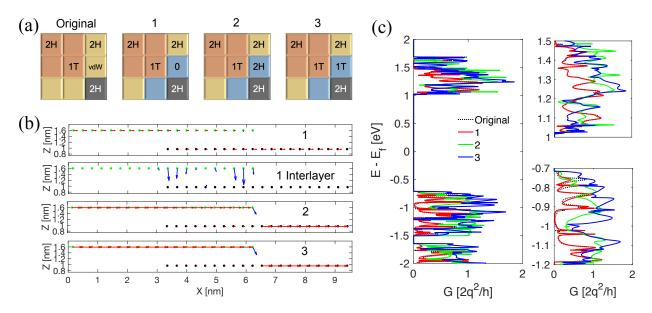


Figure 6.9 (a) Schematic of the device Hamiltonian matrix at the 1T2H-2H interface with modified van der Waals interactions (b) Current flow pattern with $L_{1T} = L_{2H} = L_{1T2H} = 3.2$ nm in the energy range $|E| \le 2 \, eV$. The second subplot shows the interlayer current flow for device 1 with a smaller scale (c) Comparison of conductance, with zoomed-in energies around E_C and E_V .

6.4 Disucussion and Conclusion

In this study, we showed the importance of edge states for transport properties. The defects and contaminations would change the van der Waals interactions, which leads to different conductance and current flow pattern. It is expected that the extracted Schottky barriers from DFT will also change if there are defects and contaminations in heterojunction. A more detailed study in DFT is in the plan for the next work. Nonetheless, the analyses and qualitative conclusion of this study would still remain the same with different extracted barrier heights.

Because of the defect-less heterojunction considered in this work, the difference in conductance between top contact and side contact is still in the same order. In experiments, defects and contaminations may lead to deformed stacking 1T2H MoS₂ with weaker van der Waals interactions between two layers. It may further weaken the coupling at the edges. And a much smaller conductance is expected for top contact heterojunctions. Our analysis above fits the observations of smaller contact resistance for side contact in experiments. Not only because the covalent bonding in side contact is stronger than van der Waals bonding in top contact, but also the side contact is less affected by defects and contaminations. On the other hand, our simulations point out in the ideal case, the device performance of top contact will not be significantly worse than side contact.

In summary, we investigate the geometric effect of top contact and side contact in 1T-2H MoS₂ heterojunctions. The different stacking modes in top contact are studied by DFT simulations, and AB

stacking is the most stable mode. The Schottky barriers are extracted from DFT simulations for top contact and side contact. We perform NEGF simulations for transport properties at zeros bias. The oscillations of conductance in top contact heterojunction are investigated in detail, comparing with oscillations of conductance in staggered graphene flakes and staggered BP heterojunctions. Compared to semiconductingsemiconducting mono-bi-monolayer BP heterojunction, metallic-semiconducting 1T-2H MoS₂ heterojunction is different in two parts: 1) The transfer of current flow from the top layer to bottom layer is dominated by narrow regions near the edges, and it is not uniformly distributed through the bilayer region; 2) The oscillation of current flow between the top and bottom layer is weak. We compare the conductance and current flow pattern between top contact and side contact 1T-2H MoS₂ heterojunctions, showing side contact is better than top contact. As the edge states are important in top contact 1T-2H junctions, we discuss the potential effects of defects and contaminations by assuming different interlayer interactions at the edge. We find with strong interlayer coupling at the edge, the conductance will be enhanced, and the current flow pattern will change significantly to an edge-dominated point current flow between the top and bottom layers. Our results support that side contact is better in 2D material devices in experiments and propose engineering edge states may improve device performance of top contact metallic-semiconducting heterojunctions.

Chapter 7 Conclusion and Future Work

7.1 Conclusion

The aim of this dissertation is to investigate the effects of contact resistance on device performance in nanoscale transistors. A multiscale simulation approach has been used for device simulation, which is introduced in Chapter 2. A generalized workflow from material to the device has been introduced. For material properties, we first apply the first principle simulations for structural optimization and bandstructure plot. Then we extract effective mass, tight-binding parameters, or maximally localized Wannier functions from DFT results based on our needs. These are used for device simulations. We also introduce how to extract the Schottky barrier height by DFT simulations from the constructed junctions. For device simulations, we introduce the NEGF method for quantum transport simulations and the finite difference method to solve Poisson's equations. The main works can be summarized into four parts.

7.1.1 Effect of Contact in BP RF Transistors

In Chapter 3, we investigate the effect of contact resistance in transistors for RF applications. We project the frequency limit of BP FETs based on rigorous atomistic quantum transport simulations and the small-signal circuit model. Our self-consistent non-equilibrium Green's function (NEGF) simulation results show that semiconducting BP FETs exhibit clear saturation behaviors with the drain voltage, unlike zero-bandgap graphene devices, leading to >10 THz frequencies for both intrinsic cutoff frequency (f_T) and unity power gain frequency (f_{max}). To develop a keen insight into practical devices, we discuss the optimization of f_T and f_{max} by varying various device parameters such as channel length (L_{ch}), oxide thickness, device-width, gate resistance, contact resistance, and parasitic capacitance. Although extrinsic f_T and f_{max} can be significantly affected by the contact resistance and parasitic capacitance, they can remain near THz frequency range (f_T = 900 GHz; f_{max} = 1.2 THz) through proper engineering, particularly with an aggressive channel length scaling ($L_{ch} \approx 10$ nm). Our benchmark against the experimental data indicates that there still exists large room for optimization in fabrication, suggesting further advancement of high-frequency performance of state-of-the-art BP FETs for future analog and radio-frequency applications.

7.1.2 Temperature-Dependent Transport in 2D Ohmic and Schottky Contact Transistors

In Chapter 4, we investigate the two distinct temperature-dependent transport behaviors of 2D Ohmic and Schottky contact transistors. It is observed that the fabricated MoS₂ TFTs can be classified into two groups based on low-temperature behaviors: one with a large Schottky barrier showing thermally activated transport and the other with an Ohmic contact exhibiting consistently high mobility at various temperatures. We propose a simple model based on monolayer MoS₂ FETs to explain this temperature-dependent

behavior. Especially for the ohmic contact device, we discuss two situations with reduced SBH and thinned SBW. Our simulation results suggest that the different temperature responses mainly come from two parts: the temperature-dependent Fermi distribution of carriers at leads and the temperature-dependent mean free path of MoS₂ material. We suggest that the ohmic contact devices can be distinguished from the devices with Schottky barriers based on low-temperature measurements. The comprehensive theoretical and experimental studies provide a systematic scheme to investigate the contact properties in 2D material-based FETs, which may help us understand metal-semiconductor interface and promote the realization of high-performance 2D-material transistors.

7.1.3 In-plane Heterojunction Transistors Using Metallic 2D Material as Contacts

Recently two-dimensional transition metal dichalcogenides (TMDs) lateral heterojunction field-effect transistors (FETs) have been demonstrated experimentally, in which metallic TMDs were used for the source/drain. In Chapter 5, we systematically investigate the contact property and device performance of monolayer 1T/1T'-2H MoS₂, MoSe₂, and MoTe₂ FETs. Schottky barrier (SB) heights are extracted from density functional theory calculations, and non-equilibrium Green's function (NEGF) transport simulations have been performed to study device characteristics. Our simulation results reveal that on and off-state characteristics of these devices are limited due to the inherent Schottky barrier. Here we optimize the performance of TMD lateral heterojunction SBFETs by using two different approaches. First, we have improved the electrostatic control by scaling equivalent oxide thickness and gate underlap, which boosts both on and off-state characteristics, making the device suitable for high-performance applications. On the other hand, moderate doping has been used in the gate underlap region, which can only improve on/off current ratio with negligible impacts on on-state characteristics, and hence, this engineering approach is more preferred for low-power applications. Our comprehensive study reveals that 1T'-2H MoTe₂ SBFET shows the highest on current (~1 mA/μm) among the three with a reasonably small subthreshold swing (80 mV/dec) if properly scaled, while 1T-2H MoS₂ SBFET exhibits the highest I_{on}/I_{off} (~10⁷) when Ohmic contact is established with moderate doping in the gate underlap region. This study not only provides physical insight into the electronic devices based on novel TMD heterostructures but also suggests engineering practice for device performance optimization in experiments.

7.1.4 Electron Transport through Top Contact and Side Contact 2D Heterojunctions

In Chapter 6, 1T–2H MoS₂ heterojunctions with different geometries are studied by DFT and NEGF simulations. We extract accurate maximally localized Wannier functions (MLWF) from DFT results. The Schottky barrier height is extracted from DFT simulations of top contact and side contact junctions. We calculate the conductance from NEGF formalism at zero bias. The simulation results suggest side contact

is more favorable for conducting current. The oscillations of conductance are carefully studied and compared to the conductance oscillation in mono-bi-monolayer black phosphorus (BP) heterojunctions. The current flow patterns are presented, showing the edge state is critical in determining conductance and current flow patterns. Extended studies of modifying weak van der Waals interactions at the edge are performed, suggesting a potential method for better contact property in metal-semiconductor top-contact junctions.

7.2 Future Works

7.2.1 Device Performance Comparison between Top Contact and Side Contact

In Chapter 6, the conductance and current flow pattern of 1T-2H heterojunction is investigated at an equilibrium state. A detailed device simulation is in the plan. A new simulator based on Julia language has been developed, with the capability to handle heterojunction in both NEGF and electrostatic simulations. Converging of NEGF simulations may become more difficult than homogeneous 2D material transistors. Simulation regions will be divided into several parts according to the number of heterojunctions in the transistor. We need to pay attention to the interface coupling matrix as it is closely related to the convergence of NEGF simulation. For electrostatic simulations, we may need to fill the vacant space with gate oxide or spacer in heterojunctions, as shown in Figure 2.16. It will introduce more interfaces in electrostatic grids. And the finite difference equations will be more complex. Another interesting topic is the permittivity of 2D metal. Even though with zero bandgaps, 1T/1T' TMDs demonstrate metallic properties, the DOS of 2D metals are expected smaller than conventional metal. At the same time, nanoscale metals may not be treated as conventional metals. The comparison of device simulation between top and side contact in 1T-2H TMD heterojunctions is needed. It may help us understand the geometric effect of contact more thoroughly.

7.2.2 Extended Works on 2D Metal-Semiconductor Heterojunctions

At the end of Chapter 6, we discussed defects and contaminations in 2D material, especially at edge states, which may change the conductance and current flow pattern significantly. At the same time, defects and contaminations may also change the extracted Schottky barrier height. In the reported 1T/1T'-2H TMDs, extracted Schottky contact can be less than 0.1 eV. However, in most DFT simulations, the values reported are much larger than 0.1 eV. How defects, contaminations, and doping affect the Schottky barrier is an interesting and important topic.

Besides the 1T/1T'-2H heterojunctions in TMD material, there are many other 2D material systems with the metallic-semiconducting interface. For example, van der Waals junctions formed by semi-metallic

graphene and semiconducting BP, homogeneous junction formed by metallic multilayer arsenene and monolayer semiconducting arsenene [170], [172], [173]. Investigating these novel systems may help us better understand the contact problem in 2D materials and may shed light on novel electronics devices based on tunneling. The ultimate goal could be to achieve circuit-level electronics based on all 2D materials.

7.2.3 Vertical Tunneling in Contact and Stacked 2D Materials

Since the birth of graphene, people have tried to open the bandgap of graphene and make it suitable for digital applications. One of the well-known methods is by layered structure, either hexagonal boron nitride or MoS₂ is sandwiched between graphene sheets [174]. There are also reported works using hBN as a buffer layer between metal and MoS₂ to reduce barrier height. All these works utilized the vertical tunneling current in layered 2D materials. In normal 2D material, electrons are confined in the plane and considered as quantum confinement states in the vertical directions. The tunneling of carriers in the vertical directions in 2D materials is an interesting topic. It may propose a generalized method to reduce contact resistance using a tunneling barrier instead of a Schottky barrier.

At the same time, the developed simulator for heterojunctions can also be used for the simulation of van der Waals heterojunctions. We can carefully engineer the band alignments by selecting semiconductors with desired bandgap and work functions. It can be used for vertical tunneling FETs. The grain boundaries in CVD-grown 2D material are an inevitable problem. How the grain boundaries affect the overall device performance is still unclear. We can investigate such a problem by constructing junctions within the same material, like mono-bi-monolayer BP junctions. Device performance can be compared with normal monolayer or bilayer BP FETs. With the newly developed simulator, a lot of interesting works would be possible.

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Appendix

Related Publications

- 1. D. Yin, and Y. Yoon, "Electron transport through 1T/1T'-2H MX₂ interface: Top contact and side contact", (submitted, revised, and under review).
- 2. R. K. A. Bennett, D. Yin, and Y. Yoon, "Assessing the Role of a Semiconductor's Anisotropic Permittivity in Hafnium Disulfide Monolayer Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 67, no. 6, pp. 2607–2613, Jun. 2020, doi: 10.1109/TED.2020.2985023.
- 3. W. Choi, D. Yin*, S. Choo, S. Jeong, H. Kwon, Y. Yoon, and S. Kim. "Low-temperature behaviors of multilayer MoS₂ transistors with ohmic and Schottky contacts," *Appl. Phys. Lett.*, vol. 115, no. 3, p. 033501, Jul. 2019, doi: 10.1063/1.5099380. (*co-first author)
- Y. Zhao, D. Yin, and Y. Yoon, "Intrinsic Performance of Germanane Schottky Barrier Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4188–4195, Oct. 2018, doi: 10.1109/TED.2018.2844741.
- 5. A. AlMutairi, D. Yin, and Y. Yoon, "PtSe₂ Field-Effect Transistors: New Opportunities for Electronic Devices," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 151–154, Jan. 2018, doi: 10.1109/LED.2017.2773599.
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