Oscillator-Based Electrochemical Capacitance Imager with Frequency-Division-Multiplexed Readout

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Electrochemical biosensors, built using complimentary-metal-oxide semiconductor (CMOS) technology, have shown promise for various applications in health-care diagnostics, disease detection, and life science research. Unlike traditional bench-top instrumentation, CMOS-based platforms offer large-scale integration of sensor pixel arrays and readout electronics on the same chip, yielding improved spatial resolution, throughput, and signal-to-noise ratio (SNR) compared to non-integrated systems.

In this thesis, we present the design and electronic characterization of a CMOS oscillator-based electrochemical capacitance imager for biosensing. The imager features both time-division multiplexed (TDM) and frequency-division-multiplexed (FDM) readout, and is suitable for overcoming Debye-length-screening effects in integrated electrochemical biosensors. The implementation of FDM readout enables improved frame rate or improved signal-to-noise ratio (SNR) when compared to an imager that employs standard TDM readout. Each pixel in the array contains a 5-MHz–180-MHz capacitance-to-frequency converter (CFC) to detect changes in the interfacial capacitance at an in-pixel working electrode, ranging in area from 2×2-μm^2 to 200×200-μm^2.

We report experimental results from electronic characterization of a 420-pixel, 3.0×2.5 mm^2 capacitance imager, fabricated in a 1.8-V, 0.18-μm mixed-signal CMOS process. To the best of our knowledge, our work is the first demonstration of a CFC-based CMOS capacitance imager for biosensing with both TDM and FDM readout.

Acknowledgements

I would like to thank my supervisor, Dr. Peter M. Levine, for his supervision and support. His professionalism and tireless commitment to helping me succeed is something I am grateful for. In addition, I would like to thank Dr. David Nairn and Dr. Lan Wei for serving on my thesis review committee.

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Chapter 1

Background and Motivation

Electrochemical biosensors, built using standard complementary metal–oxide–semiconductor (CMOS) technology, allow for high-throughput, parallelized, fully-electronic imaging of biological analytes. Unlike traditional bench-top instrumentation, CMOS-based platforms offer large-scale integration of the sensor arrays and readout electronics on the same chip. These platforms have been rapidly adopted for certain applications in health-care diagnostics, disease detection, and life science research [1, 2]. This thesis describes the design and experimental characterization of a novel CMOS oscillator-based capacitance imager for biosensing.

1.1 Capacitive Biosensors

Capacitive biosensors are a type of impedimetric biosensor. Impedimetric biosensors operate by measuring the electrical impedance of cells, proteins, DNA, and other biological

analytes in contact with an electrode which is immersed in a conductive solution (electrolyte). Capacitive biosensors are typically "affinity-based", meaning that a biological recognition probe, such as an antibody or a receptor protein, immobilized on the surface of an electrode, is used to selectively bind to the target analyte. The binding process between the capture probe and the target results in a change in the interfacial capacitance, which can be measured in a variety of ways.

The transduction process due to probe-analyte interaction typically takes place on an electrode within an electrolyte bath. In a capacitive biosensor, the change in the dielectric properties of the electrode-electrolyte interface is monitored as a voltage or current signal. Specifically, a particular attribute of the measured electrical signal, such as amplitude, frequency spectrum, pulse width, or time-delay, is monitored. For example, a capacitance-to-frequency converter maps the change in capacitance to a change in the frequency of a voltage or current signal.

Parallel electrochemical measurement of analytes in an array format is analogous to an image sensor in a digital camera. In an image sensor, a change in light intensity is mapped to an electrical signal by a pixel circuit, as shown in Figure 1.1. An array of such pixels is used to construct a digital image. Analogously, a capacitive biosensor must sense the change in the interfacial capacitance and generate a proportional electrical signal. The measured response from each pixel in the array can then be used to build a capacitance imager.

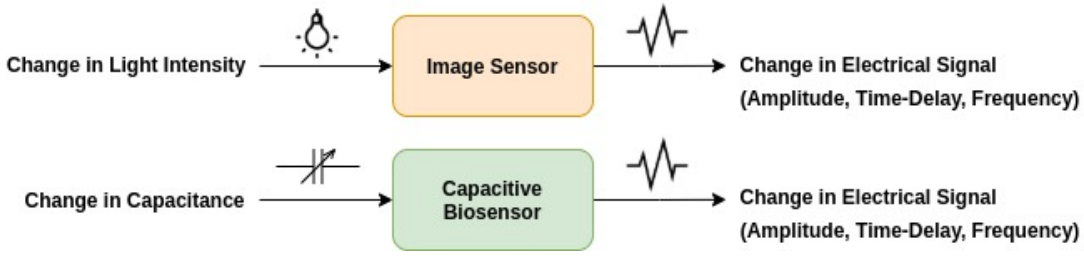


Figure 1.1: Working principle of an image sensor and a capacitive biosensor.

1.1.1 Leveraging CMOS Technology

Advances in semiconductor chip technology over the several decades have made CMOS technology an attractive platform for biosensor design [3] [4]. CMOS biosensors allow for large-scale integration of the electrodes and the required readout electronics, combining both sensing and processing on a single silicon chip. This high level of integration allows for miniaturization, higher throughput, and massively-parallelized sensing. Further, CMOS-based platforms offer relatively high signal-to-noise ratio (SNR) due to reduced parasitics along the signal path. These advantages address the shortcomings of more traditional bench-top instrumentation, such as impedance analyzers, used in biosensing applications.

1.1.2 Applications of Capacitive Biosensing

The application of biosensors has been proven useful in disease detection, health-care diagnostics, and life science research. More specifically, capacitance biosensors have been used in applications such as:

1. *In vitro* detection of cancer cells [5].

2. Cell viability studies [6].

3. Detection of viruses and microorganisms [7].

4. Detection of proteins, DNA, and other small molecules [2].

The general sensing mechanism for affinity-based capacitive biosensors is the same for many applications. The following examples illustrate this.

Detection of DNA Hybridization

Detection of specific deoxyribonucleic acid (DNA) sequences in biological samples, such as saliva and blood, can be used to identify certain infectious or inherited diseases [8]. The assay development process involves immobilizing DNA oligonucleotide probes onto the surface of an electrode, which serve as sequence-specific recognition elements. When a sample containing the target molecule (i.e., single-stranded DNA having a complementary sequence), comes in contact with the immobilized probe, binding of the probe and the target molecule occurs. Water and solute molecules near the electrode-electrolyte interface are displaced as a result. This displacement causes a change in the interfacial capacitance, which can be sensed in various ways by the electronic circuits connected to the electrode. These sensor interface circuits are generally composed of an analog front-end (AFE) gain stage, followed by an analog-to-digital converter (ADC) for digitization. The detection principle is shown in Figure 1.2

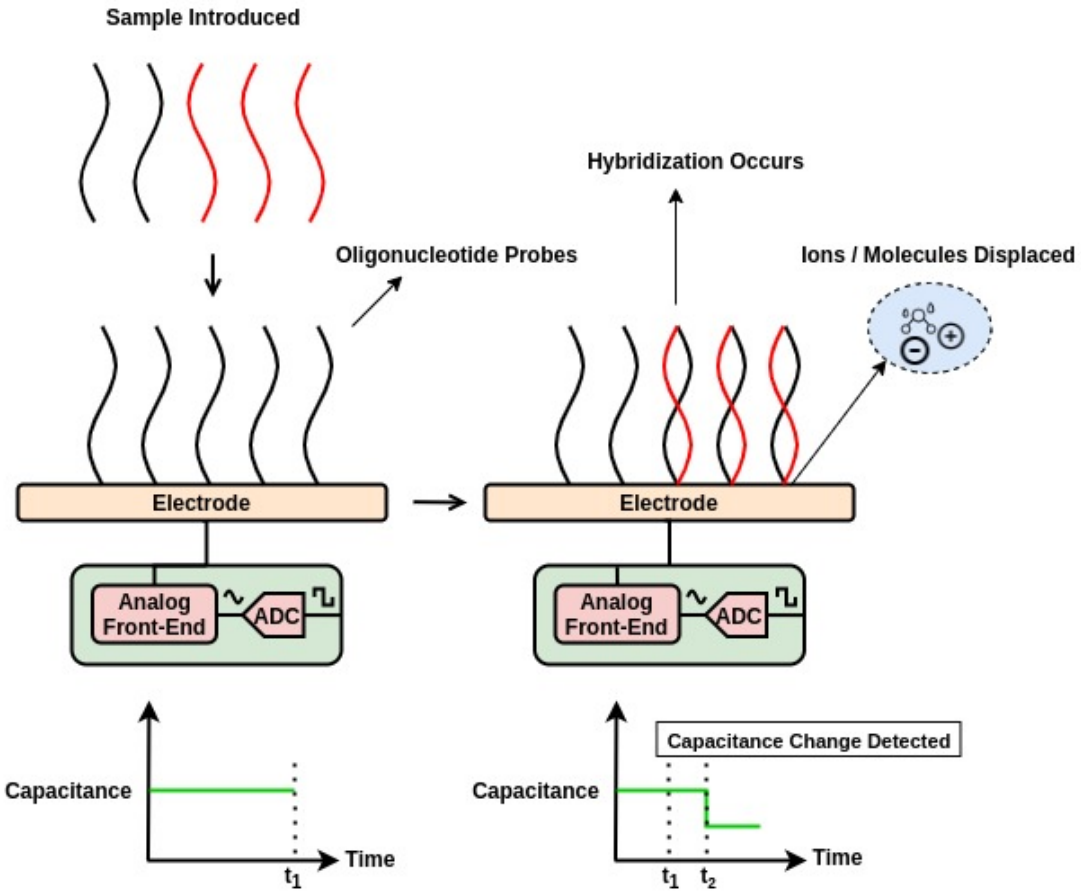


Figure 1.2: Capacitive sensing of DNA hybridization.

Detection of Neurodegenerative Disorders

Early onset of neurodegenerative disorders, such as Alzheimer's, can be identified through the presence of biomarkers in a sample [9] [10]. The typical detection procedure involves analyzing brain-based biosamples (cerebrospinal fluid) for specific biomarkers such as amyloid beta peptide and tau protein [11]. Procuring such biosamples involves a spinal tap, which is invasive and uncomfortable. Alternatively, blood-based capacitive biosensing is

an attractive and practical solution. Blood contains the same biomarkers of interest, but in lower concentrations [11]. Probes specific to the biomarker of interest are immobilized onto the electrode surface. Upon introduction of the sample, probe-analyte interaction induces a change in capacitance, which is measured by the sensor.

1.2 Sensor Interface Model

The process of interfacing biological signals with sensor electronics begins with the study of the electrode-electrolyte interface. An equivalent circuit model of this interface must be developed before designing the supporting electronics.

1.2.1 Randles Circuit

The simple RC circuit shown in Figure 1.3, known as a Randles circuit, is a generic electrical model used to represent the electrode-electrolyte interface. The electrode on which the analyte is sensed is referred to as the "working" electrode (WE). A CMOS-based biosensor typically includes one or more WEs integrated on the chip surface. A "reference" electrode (RE), connected externally, is used to set the potential of the electrolyte through a negative feedback amplifier, as shown in Figure 1.3. A third "counter" electrode (CE), connected to the output of the feedback amplifier, ensures that the potential difference V_{ref} between the WE and RE is maintained for a wide range of sensor currents I_{sense}. This three-electrode system, with the feedback amplifier, behaves as a voltage regulator, and is referred to as a "potentiostat". Further, to prevent damage to the analyte, the potential difference between the WE and the RE is kept small (1 mV to 10 mV). The transduction process

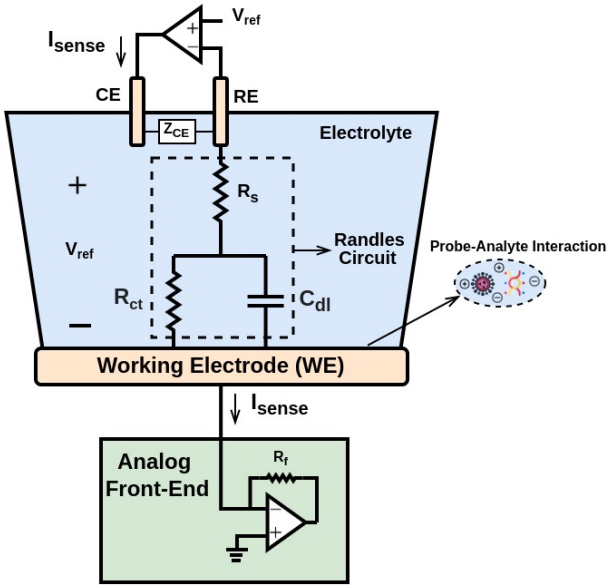


Figure 1.3: Randles circuit model of the electrode-electrolyte interface with potentiostat.

due to probe-analyte interaction occurs at the WE, and the resulting signal is measured by an AFE circuit.

The passive components defined in Figure 1.3 represent various electrical properties of the interface. Resistor R_{ct} models the charge-transfer resistance, and is associated with leakage current flowing between the WE and the electrolyte. Resistor R_s represents the electrolyte resistance. In a bounded area between the WE and the RE, R_s is given by:

$$R_s = \frac{l}{\kappa A}\,, \tag{1.1}$$

where l is the length of the conducting channel, A is the area of the conducting channel, and κ is the conductivity of the electrolyte. R_s is relatively low in concentrated electrolytes.

The interface also exhibits a capacitive profile. This is due to the fact that when a charged

electrode is immersed in an electrolyte, it attracts counter charges. The layer of solvent molecules between the separated charges serves as a dielectric, and the resulting structure is referred to as the "electrical double layer" (EDL). The charge separation within the EDL is modelled by capacitor C_{dl} as shown in Figure 1.3, and is referred to as the "double-layer capacitance". Capacitance C_{dl} has a major influence on impedance measurements, and can be modelled as the series combination of Helmholtz layer capacitance C_H and Stern layer capacitance C_{stern}. Capacitance C_H behaves like a linear parallel-plate capacitor, whereas C_{stern} is non-linear and varies with dc electrode voltage V_{DC}, absolute temperature T, and Debye length λ_d. The reciprocal of C_{dl} can therefore be expressed as:

$$\frac{1}{C_{dl}} = \frac{1}{C_H} + \frac{1}{C_{stern}} = \frac{d}{A \times \epsilon} + \frac{\lambda_d}{\epsilon} \operatorname{sech}\left(\frac{qV_{DC}}{2k_BT}\right), \tag{1.2}$$

where d is the Helmholtz distance (i.e., the distance between the electrode and the first layer of counter charges), q is the elementary charge, k_B is Boltzmann's constant, and ϵ is the permittivity of the electrolyte.

1.2.2 Debye Length

The concentration of counter charges in the EDL is high, and gradually tapers off into the bulk of the electrolyte, where charges are uniformly distributed. The Debye length λ_d is a measure of how far this electric field extends into the electrolyte, and serves as a measure of the thickness of the EDL. Further, λ_d scales inversely with the square root of the electrolyte concentration, and, for a monovalent electrolyte such as NaCl, λ_d is given by:

$$\lambda_d = \sqrt{\frac{\epsilon k_B T}{q^2 N_a 2c}}, \tag{1.3}$$

where N_a is Avogadro's number, and c is the concentration of the electrolyte in mol/m^3. Figure 1.4 shows the variation of λ_d with c for NaCl in water ($\epsilon_r = 78$) at 298 K. For a concentration of 1 mM, the Debye length $\lambda_d = 9.63$ nm. However, if the concentration of NaCl is increased to 100 mM, the Debye length becomes $\lambda_d = 0.96$ nm.

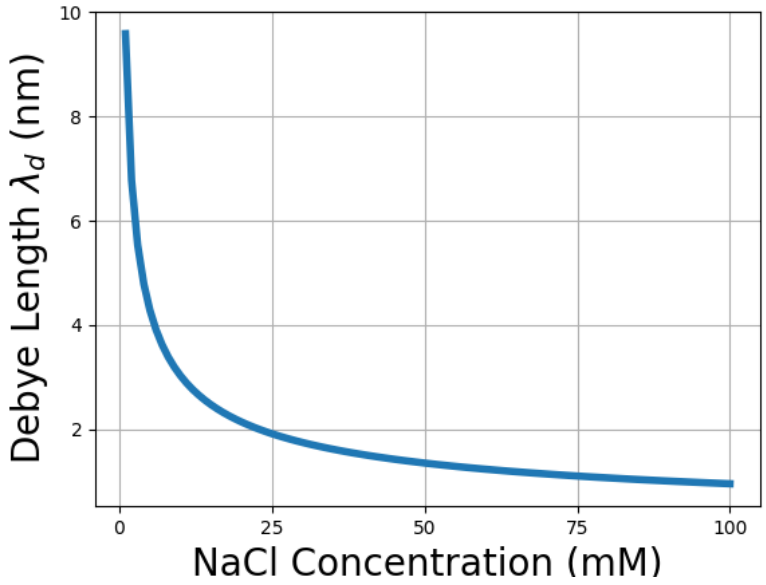


Figure 1.4: Debye length vs NaCl concentration.

1.2.3 Probing within the Debye Length

Electrochemical impedance spectroscopy (EIS) is considered the "gold standard" measurement technique for characterizing the interfacial impedance $Z(j\omega)$, modelled by the

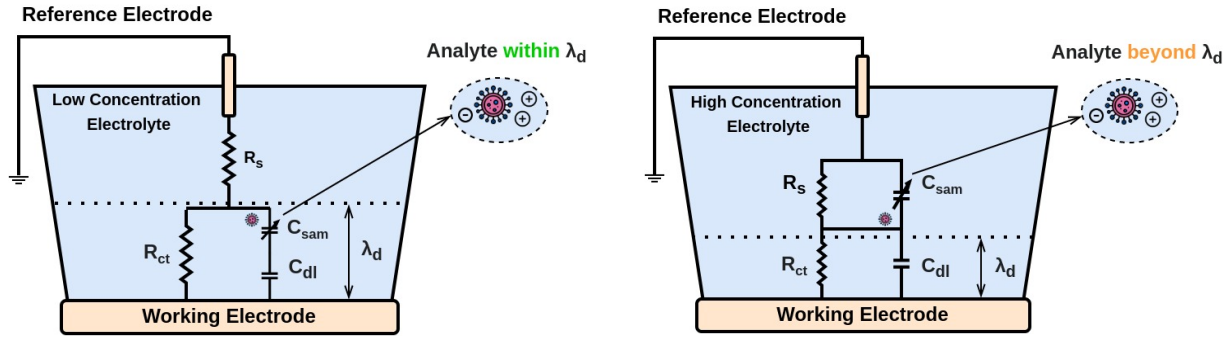


Figure 1.5: Model of the interfacial impedance $Z(j\omega)$ when the analyte is (a) within λ_d, and (b) beyond λ_d.

Randles circuit in Figure 1.3, over a wide frequency range. Measurements are typically made by applying a small sinusoidal ac voltage $V_{app}(t) = V_o sin(\omega t + \phi)$, where V_o is the voltage amplitude and ϕ is the phase, to the RE, and sensing the resulting current $I_{sense}(t)$ that flows through the WE. Current $I_{sense}(t)$ is given by $I_{sense}(t) = I_o sin(\omega t + \theta)$, where I_o is the current amplitude and θ is the phase. The impedance $Z(j\omega)$ is therefore given by:

$$Z(j\omega) = \frac{|V_o|e^{j\phi}}{|I_o|e^{j\theta}}, \tag{1.4}$$

where $|V_o|e^{j\phi}$ is the input voltage phasor and $|I_o|e^{j\theta}$ is output current phasor. Precise measurement of the magnitude and phase of $I_{sense}(t)$ is required, and this is typically accomplished with a lock-in amplifier (a type of homodyne receiver) connected to the WE.

The circuit model presented in Figure 1.3 is purely derived from the physics of the electrode-electrolyte interface, and the discussion thus far does not account for the analyte. The location where probe-analyte interaction occurs, with respect to the EDL, determines the

required operating frequency of the sensor, influencing the design choices for the AFE.

Changes in the interfacial capacitance due to probe-analyte interaction occurring within the EDL can be sensed with relatively low-frequency signals. To understand why, consider the interface model shown in Figure 1.5(a). The capacitance to be sensed C_{sam} can be modelled in series with C_{dl}, since the interaction between probe and analyte occurs within λ_d. Since C_{dl} is typically an order of magnitude larger than C_{sam}, the series combination is dominated by C_{sam}. The equivalent impedance at the interface is therefore expressed as:

$$Z(j\omega) \approx \frac{R_{ct}}{1 + j\omega R_{ct} C_{sam}} + R_s \approx \frac{(R_{ct} + R_s)\left(1 + j\omega C_{sam}(\frac{R_{ct}R_s}{R_{ct}+Rs})\right)}{1 + j\omega R_{ct} C_{sam}}, \tag{1.5}$$

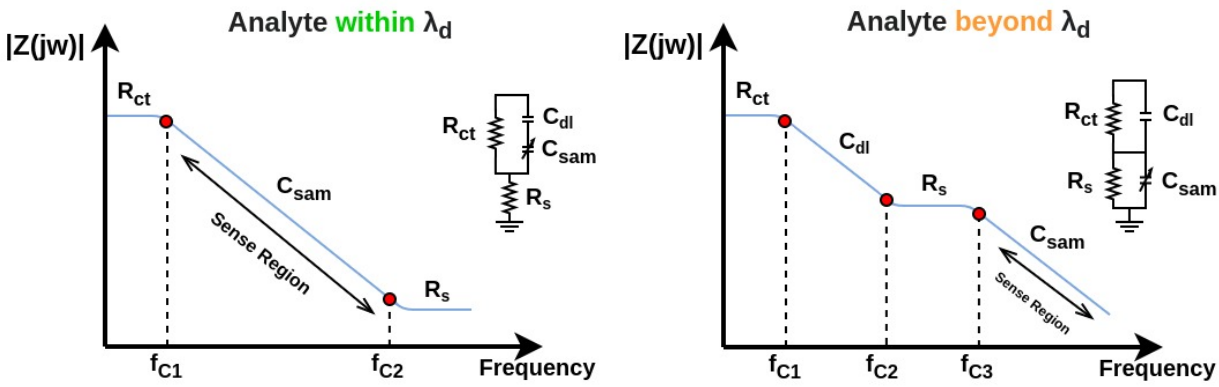
where ω is the angular frequency in rad/s, and $\omega = 2\pi f$, where f is the frequency in Hertz.

Figure 1.6(a) shows the magnitude of the impedance as a function of frequency for interactions occurring within the EDL. The impedance magnitude $|Z(j\omega)| = R_{ct} + R_s \approx R_{ct}$, when operating the sensor with frequencies below pole frequency f_{c1}, where f_{c1} is given by:

$$f_{c1} \approx \frac{1}{2\pi R_{ct} C_{sam}}. \tag{1.6}$$

It is clear that the sensor must be operated at frequencies above f_{c1} to sense changes in C_{sam}. When R_{ct} is large, there is negligible dc current flow through the EDL (i.e., the Faradaic current is small), and so f_{c1} is located at a relatively low frequency. This allows for capacitive sensing at relatively low operating frequencies. For typical biosensing applications, probe-analyte interactions occurring within the EDL are sensed with operating frequencies in the 10 kHz to 10 MHz range. A second cutoff frequency f_{c2} sets the frequency at which $|Z(j\omega)|$ approaches R_s, as expected from 1.5:

$$f_{c2} \approx \frac{1}{2\pi R_s C_{sam}}. \tag{1.7}$$



(a) (b)

Figure 1.6: Interfacial impedance magnitude (a) within λ_d, and (b) beyond λ_d.

1.2.4 Probing Beyond the Debye Length

To maximize the extent of probe-analyte interaction, it is beneficial to perform biosensing directly in the physiological fluid of the sample. However, at physiological salt concentration levels (i.e. in the 120 mM–150 mM range), λ_d becomes relatively small due to ionic packing at the interface. Analytes present well beyond the Debye length are effectively "screened" by C_{dl}, meaning that C_{sam} is no longer modelled in series with C_{dl}. Consequently, the effective interfacial capacitance is dominated by C_{dl} at lower frequencies.

At the limit, when the analyte approaches the bulk of the solution, C_{sam} can be modelled in parallel with R_s as shown in Figure 1.5(b). The equivalent impedance at the interface when probe-analyte interaction occurs in the bulk of the electrolyte is therefore given by

$$Z(j\omega) = \frac{R_{ct}}{1 + j\omega R_{ct} C_{dl}} + \frac{R_s}{1 + j\omega R_s C_{sam}} = \frac{(R_{ct} + R_s)\left(1 + j\omega(\frac{R_{ct}R_s}{R_{ct}+R_s})(C_{dl} + C_{sam})\right)}{(1 + j\omega R_{ct} C_{dl})(1 + j\omega R_s C_{sam})}. \tag{1.8}$$

$|Z(j\omega)|$ is shown in Figure 1.6(b). To sense changes in C_{sam}, an operating frequency above the pole f_{c3} is required, where f_{c3} is given by

$$f_{c3} \approx \frac{1}{2\pi R_s C_{sam}}. \tag{1.9}$$

In physiological fluids with relatively high conductivity, λ_d is typically in the 0.5nm–1nm range. Sensing changes in C_{sam} therefore requires operating the sensor at relatively high frequencies. Reducing the concentration of the electrolytic bath in which sensing takes place is not a practical solution, since the properties of the analyte could be altered, affecting the extent of binding.

1.3 Measuring Interfacial Capacitance

While EIS can be used to measure changes in the interfacial capacitance C_{sen} at the WE, precise measurements of the magnitude and phase of $I_{sense}(t)$ flowing through the WE are required. This results in added design complexity for the AFE. Two alternative techniques for measuring C_{sen} are now presented.

1.3.1 Charge-Based Capacitance Measurement

The charge-based capacitance measurement (CBCM) technique was originally proposed as a method to characterize interconnect capacitance on a CMOS chip [12]. The technique has since gained popularity in the biosensor community due to its implementation simplicity [2, 4]. The working principle is shown in Figure 1.7. Capacitance C_{sen} at the WE is charged and discharged via devices M_p and M_n, controlled by non-overlapping clock signals ϕ_1 and ϕ_2. The instantaneous current $i(t)$ through C_{sen} is given by $i(t) = C_{sen}\frac{dv(t)}{dt}$, where $v(t)$ is the instantaneous voltage across C_{sen}. The average current I_{avg} over one period T_s of the clock signal can therefore be expressed as:

$$\begin{aligned} I_{avg} &= \frac{1}{T_s}\int_0^{T_s} C_{sen}\frac{dv(t)}{dt}\,dt \\ &= \frac{1}{T_s}\int_0^{V_{app}} C_{sen}\,dv \\ &= \frac{C_{sen}\times V_{app}}{T_s}. \end{aligned} \tag{1.10}$$

Current I_{avg} is typically measured by an integrator, and C_{sen} is therefore obtained for a pre-defined voltage V_{app} and sample period T_s.

1.3.2 Capacitance-to-Frequency Conversion

Capacitance-to-frequency conversion is another popular technique used for sensing C_{sen} [5, 3]. A capacitance-to-frequency converter (CFC) maps C_{sen} to the frequency of a voltage or current, and is typically realized by a RO, allowing for a compact sensor architecture. A

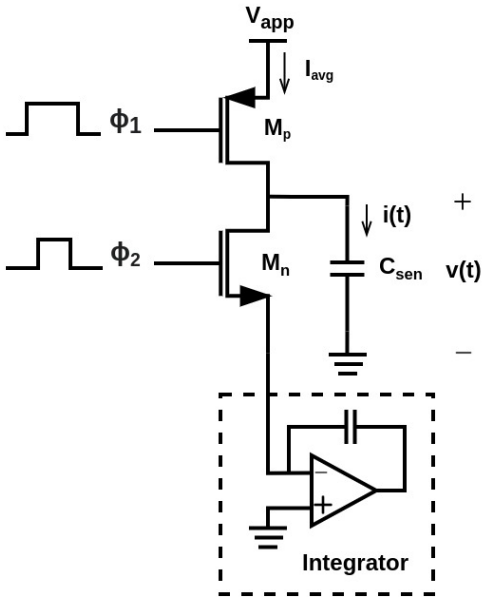


Figure 1.7: Charge-based capacitance measurement technique.

change in C_{sen} results in a proportional change in the operating frequency f_{op} of the CFC, where f_{op} can be expressed as:

$$f_{op} = -S \times C_{sen} + f_0\,, \tag{1.11}$$

where f_0 is the operating frequency when C_{sen} is not present, and S is the frequency sensitivity of the CFC to a change in C_{sen}. CFC-based architectures are attractive since the output signal from each pixel can be treated as a digital "clock", which results in reduced design complexity. An on-chip counter can serve as an ADC to measure changes in f_{op}.

1.4 CMOS Biosensor Array

An array-based CMOS electrochemical biosensor consists of pixel circuits arranged in rows and columns on a chip similar to the architecture of a CMOS visible-light imager, as shown in Figure 1.8. This architecture allows for parallelized sensing and high spatial resolution when the pixel pitch is small (i.e., center-to-center spacing between pixels is small). Each pixel in a typical array consists of a WE connected to a sensitive AFE gain stage. A fully-integrated platform also includes additional amplification stages and on-chip ADCs to digitize the measured signals. Row-wise enable signals (R0, R1, R2) allow for pixels in a row to be activated simultaneously.

Depending on the architecture, pixel output signals are typically digitized in one of two ways:

1. All pixels in the array share a single ADC.
2. Each column of pixels shares an ADC. Figure 1.8 shows this architecture, often referred to as a "column parallel" architecture, for a 3×3 biosensor array.

The digitized data from the on-chip ADCs can be sent to an external microcontroller or computer for further processing.

1.4.1 Readout Techniques

Since the ADCs are typically shared by a column of pixels, the measured signals must be multiplexed for digitization and subsequent readout. Techniques such as time-division

multiplexing (TDM) or frequency-division multiplexing (FDM) can be used. It is first beneficial to consider a few performance parameters which will allow for a fair comparison between the various multiplexing techniques available.

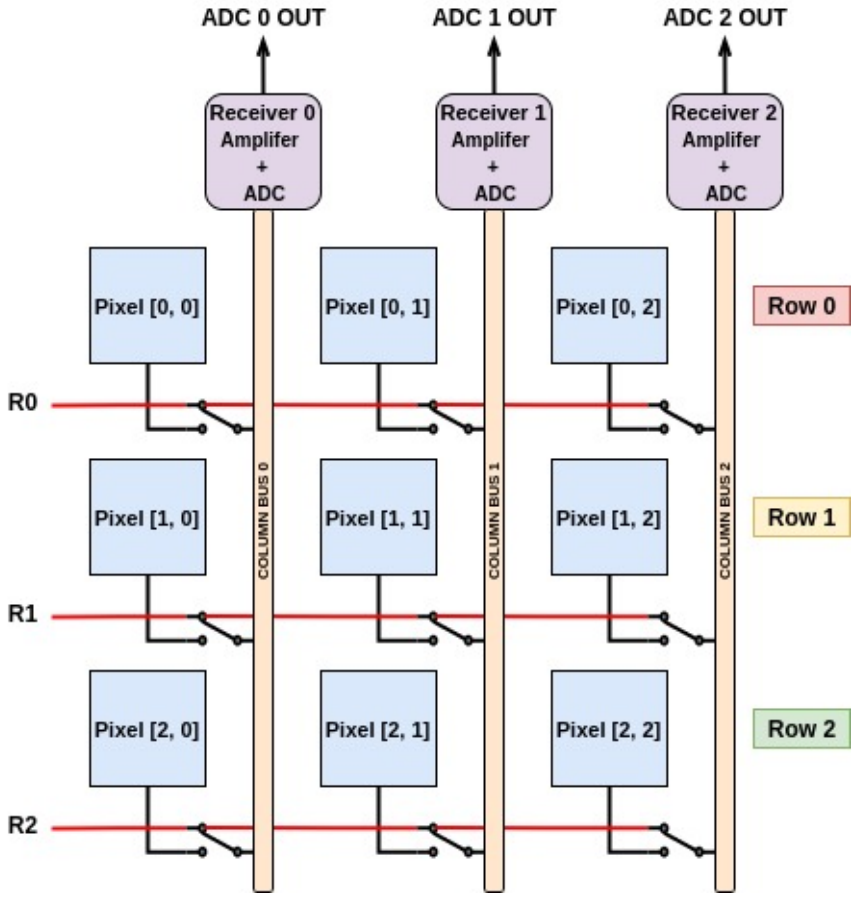


Figure 1.8: A 3 × 3 biosensor array.

- **Integration Time**: The integration time t_{int} is the time period during which the pixel is actively measuring signal changes at the electrode-electrolyte interface. It is also referred to as the "exposure time" or "acquisition time".

- **Frame Readout Time**: The frame readout time t_{frame} is the total time taken to digitize and read out the entire array of pixels.
- **Frame Rate**: The frame rate FR is given by $FR = (t_{frame})^{-1}$ and is expressed as frames per second (fps).
- **Signal-to-Noise Ratio**: The SNR is defined as the ratio of the signal power to the noise power (variance) for a measurement. Averaging the measured signal by taking multiple samples improves the SNR by decreasing the variance of the uncertainty. More precisely, assuming the noise follows a Gaussian distribution, averaging N samples of the signal decreases the noise power by a factor of N. However, this requires longer integration times. The SNR is therefore proportional to t_{int}.

Time-Division Multiplexing

Array-based biosensors typically employ TDM readout due to its implementation simplicity. Consider the example of a 3×3 array shown in Figure 1.8. Each row of pixels is allocated a fixed integration time $t_{int,TDM}$ to drive the corresponding column bus, as shown in Figure 1.9(a). The signal on each column bus is then digitized, and the data is stored in a temporary buffer. Assuming that the temporary buffers are read out in time t_{read}, the frame readout time $t_{frame,TDM}$ is given by:

$$t_{frame,TDM} = 3 \times t_{int,TDM} + t_{read}. \tag{1.12}$$

The frame rate FR_{TDM} is therefore given by $FR_{TDM} = (t_{frame,TDM})^{-1}$. Further, the SNR for each measurement is proportional to $t_{int,TDM}$ (i.e., $SNR_{TDM} \propto t_{int,TDM}$).

Frequency-Division Multiplexing

FDM readout can be used as an alternative to TDM, allowing for improved FR, or improved SNR at a fixed FR due to longer t_{int}. In row-wise FDM, each row operates in a unique frequency band as shown in Figure 1.9(b). The column bus can therefore be driven simultaneously by all active pixels in a column. The resulting signal is a superposition of signals from multiple pixels, and contains frequency content in each of the unique frequency bands. For a 3×3 array, with row integration time $t_{int,FDM}$, and buffer readout time t_{read}, the frame readout time $t_{frame,FDM}$ is given by:

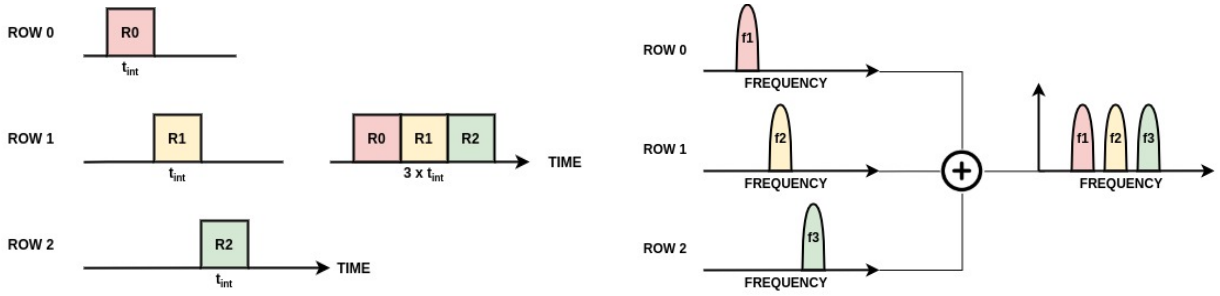
$$t_{frame,FDM} = t_{int,FDM} + t_{read}. \tag{1.13}$$

Assuming a fixed $FR = (t_{frame,TDM})^{-1} = (t_{frame,FDM})^{-1}$, it is clear that employing FDM allows for $t_{int,FDM} = 3 \times t_{int,TDM}$ (i.e., each measurement can be averaged for a longer period of time). The SNR is therefore improved since $SNR_{FDM} \propto 3 \times t_{int,TDM}$. However, employing this technique requires that each row operate in a unique frequency band, which results in increased implementation complexity compared to TDM.

1.5 Challenges and Objectives

Although CMOS-based biosensors are a promising solution for imaging and detection of biological analytes, the high level of integration results in increased design complexity. A few common challenges in designing CMOS-based biosensors are now discussed.

Sensing in High-Concentration Electrolytes



(a) (b)

Figure 1.9: (a) Time-division multiplexing (b) Frequency-division multiplexing.

Sensing changes in the interfacial capacitance at physiological salt concentrations is a well known obstacle. The increased ionic strength of an electrolyte used to simulate a physiological environment results in reduced λ_d, and so C_{sam} is screened by C_{dl}. One way to circumvent this problem is to reduce the concentration of the electrolyte. However, this may not be practical since the properties of the analyte are potentially altered. The more promising solution is to operate the biosensor at higher frequencies, thereby overcoming the screening effect.

Increasing Spatial Resolution

The spatial resolution is a measure of the smallest analyte that can be resolved by a biosensor. Advances in CMOS technology can be leveraged to design compact electrodes and pixel circuits. Integrating these pixels into high-density arrays increases the spatial resolution.

Increasing Frame Rate

With large, dense arrays, the readout time is a major concern for real-time applications. A frame of data must be read out before processing next measurement. Various multiplexing

schemes can be used to improve the frame rate.

Improving Detection Limit

A capacitive biosensor must be designed to sense small changes in C_{sen}. The limit of detection (LOD), is a measure of the smallest change in C_{sen} that can be reliably sensed by the AFE. Improving LOD involves improving the SNR of the AFE circuit.

1.6 Summary of Previous Work

Several research groups are actively working on addressing the challenges outlined in Section 1.5. Research efforts to probe beyond the EDL in concentrated solutions and improve signal readout from dense pixel arrays are discussed below.

Bacteria Detection with CFC-based Biosensor: Couniot et al. [3]

The authors describe an oscillator-based CMOS biosensor designed for capacitive detection of bacterial cells. The active area of the chip consists of a single five-stage ring oscillator to implement CFC-based measurements. The authors report operating frequencies in the 8 kHz–290 MHz range. The output of the oscillator is followed by a ten-stage frequency divider with a division factor of 1024. This enables readout by standard scopes and microcontrollers.

Detection of DNA Hybridization in Concentrated Solutions: Lee et al. [13]

The authors target probing beyond the Debye length in concentration solutions. The design employs an ion-sensitive field-effect transistor (ISFET) as a floating-gate metal-oxide-semiconductor (MOS) capacitor at the output of a ring oscillator. The threshold

voltage V_{th} of the ISFET connected to the oscillator is modulated upon analyte detection, which in turn modulates the oscillator frequency. The authors report operating frequencies up to 100 MHz.

Biosensor Array for Cell Viability Studies: Senevirathna et al. [5]

The authors describe the design of a CFC-based biosensor array for cell viability studies. The chip features a 4×4 array of interdigitated electrodes, with each pair connected to a three-stage ring oscillator. The measured signal from each array is digitized with a counter and driven off-chip through an I^2C interface.

Biosensor Array with Code-Division Multiplexed Readout: Hu et al. [7]:

The authors describe the design of a 512×256 sensor array for impedance spectroscopy, pH measurements, and optical imaging. The chip features code-division multiplexed (CDM) readout which enables extended integration times at a given frame rate.

1.7 Proposed Work

We propose to design a CMOS capacitance imager for electrochemical biosensing that addresses two key challenges:

- **Sensing beyond the electrical double layer**.
- **Employing frequency-division multiplexed readout** which allows for improved FR at a fixed SNR, or improved SNR at a fixed FR, compared to TDM readout.

The fundamental building block of our proposed design is a CFC, realized by a five-stage, inverter-based RO. Each pixel converts changes in C_{sen} at the WE, to a proportional shift in the operating frequency of the RO. We design the RO to operate over a wide range of frequencies (5 MHz–180 MHz), allowing it to probe analytes within and beyond the EDL, with relatively high sensitivity.

Our imager architecture features both TDM and FDM readout. Sensors that employ FDM readout typically require some form of up-conversion of the measured signal (i.e., the baseband signal) to a unique carrier frequency band. Given that the signal of interest in the proposed design is the operating frequency of the RO, up-conversion is not required. As far as we are aware, our proposed design is the first to implement FDM readout using CFC-based pixels.

Table 1.1 compares the measured performance of previously-reported CMOS capacitance biosensors to our proposed design.

1.7.1 Thesis Organization

This thesis is organized as follows:

- **Chapter 2** details the design of our CMOS capacitance imager and includes simulation results.
- **Chapter 3** describes the system level design for our capacitance imager.
- **Chapter 4** details the experimental characterization of the electronic performance of our fabricated imager.
- **Chapter 5** is a summary of our proposed design, and provides potential directions of improvement for future work.

	[3]	[7]	[5]	[2]	**Target**
Sensing Method	CFC	CBCM	CFC	CBCM	CFC
Technology	0.25 μm	0.18 μm	0.35 μm	90 nm	0.18 μm
Supply	2.5 V	3.3 V	3.3 V	1.2 V	1.8 V
Frequency Range	8 kHz–291 MHz	100 MHz	58 MHz–61 MHz	1 MHz–70 MHz	5 MHz–180 MHz
Readout Mode	TDM	TDM & CDM	TDM	TDM	TDM & FDM
Number of Pixels	2	131,072	16	65,536	<1000
Min Electrode Area (μm^2)	100 × 100	-	30 × 30	90 nm radius	2 × 2
Max Electrode Area (μm^2)	200 × 200	-	30 × 30	90 nm radius	200 × 200
Digitization	Off-chip	Off-chip	On-chip	On-chip	Off-chip

Table 1.1: Performance specifications comparison.

Chapter 2

Circuit Design

This chapter details the performance specifications and design of our capacitance imager. The design of each sub-block is presented along with simulation results.

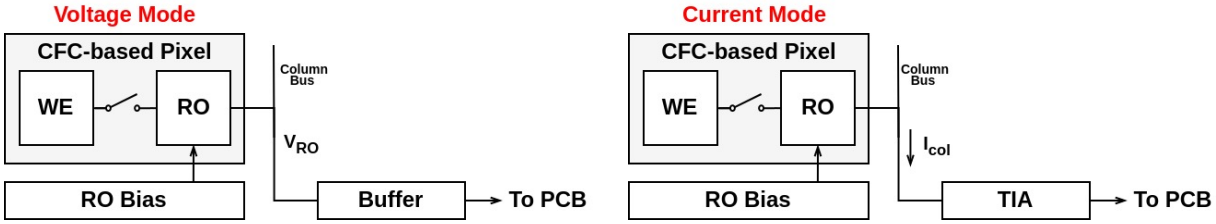


Figure 2.1: Core circuit blocks when operating in (a) voltage mode, and (b) current mode.

As shown in Figure 2.1, each pixel consists of a WE connected to a RO, serving as CFC. A temperature-compensated bias network allows for row-wise frequency tuning. Each pixel can be operated in voltage or current mode. In voltage mode, the rail-to-rail output

voltage of the enabled RO directly drives the corresponding column bus. The signal is subsequently driven off chip for digitization by a voltage buffer, as shown in Figure 2.1(a). In current mode, the RO output voltage toggles a gated current source within the pixel. This allows multiple pixels operating in unique frequency bands to simultaneously drive the corresponding column bus, facilitating FDM readout of a column of pixels. The current mode signal on the column bus is subsequently driven off the chip by a high-speed transimpedance amplifier (TIA), as shown in Figure 2.1(b). Digital control signals required for pixel activation, multiplexer channel selection, and RO bias tuning are generated using three on-chip shift registers.

2.1 Pixel Design

2.1.1 Target Specifications

As a starting point for the design process, we first determine the target specifications for the pixel.

Tuning Range

For increased sensitivity to probe-analyte interaction occurring beyond the EDL, the AFE is required to operate at higher frequencies (typically $\geq$ 50 MHz), as discussed in Chapter 1. Since very few research groups have shown array-based biosensor platforms operating at frequencies above 100 MHz [2] [3], in this work, we target a RO frequency range of 5 MHz–180 MHz as this will allow for sensitive probing both within, and beyond the EDL.

Our design must therefore allow for both coarse-grained and fine-grained tuning of the RO through a bias network.

Temperature Stability

The operating frequency of the RO is temperature dependent. Enabling multiple pixels increases the net power consumption, thereby raising the temperature of the chip. It is therefore necessary to ensure that variations in the operating frequency, due to chip temperature fluctuations, do not mask the signal generated during detection of the analyte. A temperature-compensated bias network is required to maintain a relatively stable RO operating frequency over a typical range of operating temperatures from 10°C–70°C.

Detection Range

The target capacitance detection range is set by the specific application for which the biosensor is designed (DNA hybridization, whole-cell measurements, antigen-antibody binding, etc.). As a primer for the design process, we assume an approximate C_{sen} change of 150 fF, as this is typical for capacitive biosensing applications.

2.1.2 Ring Oscillator Design

Proposed Topology

The fundamental building block of each pixel is a RO. A five-stage, inverter-based topology allows for a compact design. The RO is biased using a current-starved architecture, as

shown in Figure 2.2. Transistors M2 and M5 limit the bias drain current I_D at each stage, allowing for frequency tuning. The voltages V_P and V_N used to set I_D are generated by a current mirror external to the pixel. The first stage of each RO is modified to operate as a NAND gate, allowing for active-high enable of pixels in a row. Probe-analyte interaction takes place on a functionalized WE, which is connected to the output of the second stage through a transmission gate.

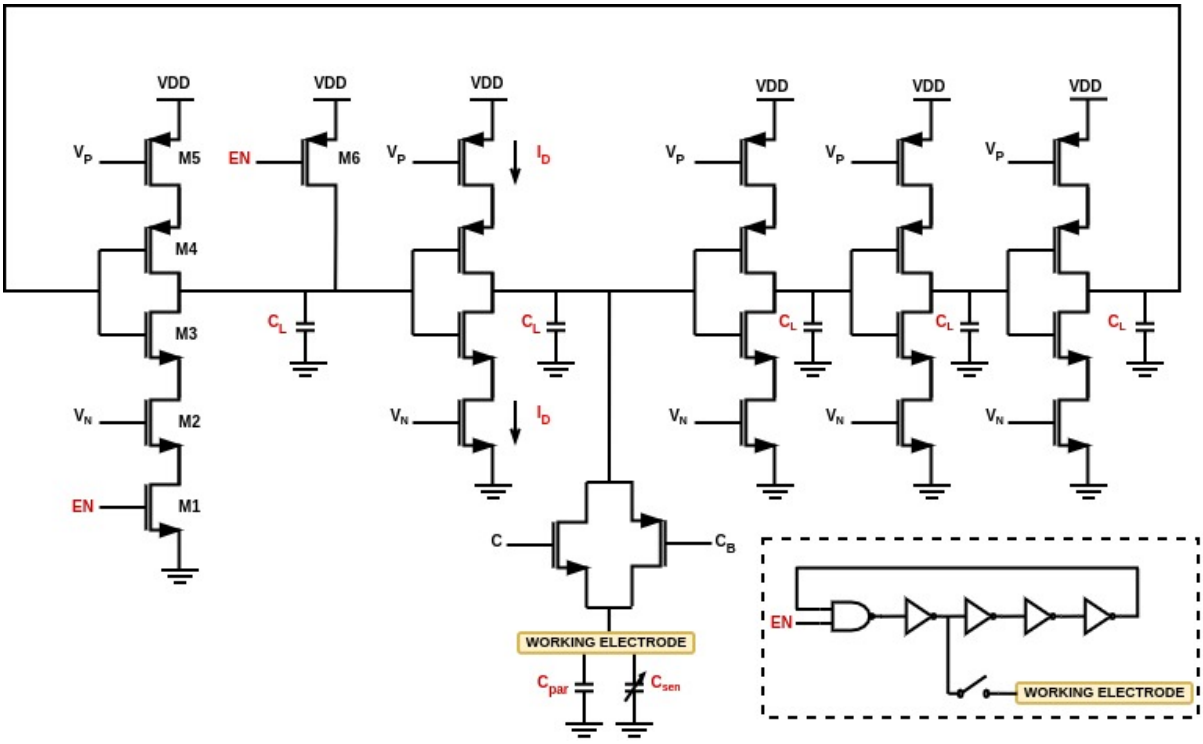


Figure 2.2: Ring oscillator architecture.

The operating frequency f_{op} of an n-stage RO is given by [14]:

$$f_{op} = \frac{1}{n \times (t_{pHL} + t_{pLH})}, \tag{2.1}$$

where n is an odd integer and $n \geq 3$, and t_{pHL} and t_{pLH} represent the high-to-low and low-to-high propagation delays, respectively.

Delays t_{pHL} and t_{pLH} are directly proportional to the total capacitance C_L seen at the output of each stage. For a supply voltage V_{DD}, and inverter switching threshold V_m, t_{pLH} and t_{pHL} of stage-n are given by:

$$t_{pLH} = \frac{C_L \times V_m}{I_D}, \tag{2.2}$$

$$t_{pHL} = \frac{C_L \times (V_{DD} - V_m)}{I_D}. \tag{2.3}$$

Equation 2.1 can therefore be modified to show the relationship between f_{op} and I_D for a five-stage RO:

$$f_{op} = \frac{I_D}{5 \times C_L \times V_{DD}}. \tag{2.4}$$

The total capacitance seen at the output of the second stage includes, the load capacitance C_L, parasitic capacitance C_{par} due to interconnect and the transmission gate used to connect the RO to the WE, and the interfacial capacitance to be sensed C_{sen}. A change in C_{sen} results in a change in the delay of the second stage, which in turn modulates f_{op}. It is therefore necessary to ensure that the device and interconnect parasitics are relatively small for increased sensitivity to changes in C_{sen}.

Equation 2.4 can be further manipulated to show the relationship between f_{op} and C_{sen} as

$$f_{op} = \frac{I_D}{(C_{L'} + C_{sen}) \times V_{DD}}, \tag{2.5}$$

where $C_{L'} = 5C_L + C_{par}$. To begin the design process, we consider the capacitance contributions of a single inverter stage. The equivalent digital model shown in Figure 2.3 assumes that at any given time, one of the two devices, M_p and M_n, is in the triode region, while the other device is in cutoff. The capacitance C_L seen at the output of each RO stage is therefore given by

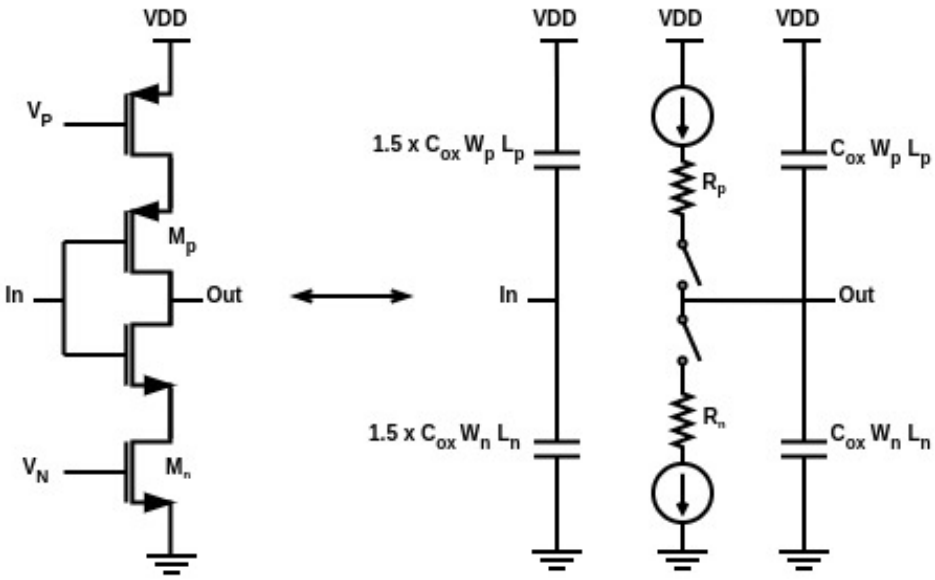


Figure 2.3: Digital model of ring oscillator stage.

$$C_L = \frac{5}{2} \times C_{ox}(W_p L_p + W_n L_n), \tag{2.6}$$

where C_{ox} is the gate oxide capacitance per unit area, L_p and L_n are the lengths of M_p and M_n, respectively, and W_p and W_n are the widths of M_p and M_n, respectively. For the TSMC 0.18-μm process used, C_{ox} is calculated to be approximately 8.5 fF/μm^2 for gate oxide thickness $t_{ox} = 4$ nm. For increased sensitivity to changes in C_{sen}, it is beneficial

to keep C_L relatively small. For a bias current $I_D = 200$ μA, a supply voltage $V_{DD} = 1.8$ V, and maximum required f_{op} of 180 MHz, $C_L \approx 115$ fF from 2.4. For minimum length devices ($L_p = L_n = 0.18$ μm), $W_p = 2W_n$ to ensure $t_{pHL} \approx t_{pLH}$ ($R_p \approx R_n$), and $C_L = 115$ fF, 2.6 can be solved to yield $W_n = 10$ μm. Device dimensions for the first stage of the RO are provided in Table 2.1.

Device	**Aspect Ratio** $\frac{W}{L}$ $(\frac{\mu m}{\mu m})$
M1	$\frac{1}{0.18}$
M2, M3	$\frac{10}{0.18}$
M4, M5	$\frac{20}{0.18}$
M6	$\frac{2}{0.18}$

Table 2.1: Ring oscillator transistor sizing.

Sensitivity and Transfer Characteristic

The relationship between f_{op} and C_{sen} is clearly nonlinear, as seen in 2.5. However, for small changes in C_{sen}, the response can be linearized. The first-order Taylor expansion f'_{op} for 2.5 is given by

$$f'_{op} = -\frac{(I_D/V_{DD})}{(C_{L'})^2} \times C_{sen} + \frac{(I_D/V_{DD})}{C_{L'}}. \tag{2.7}$$

The transfer characteristic can therefore be expressed as

$$f_{op} = -S \times C_{sen} + f_0, \tag{2.8}$$

where $f_0 \approx \frac{(I_D/V_{DD})}{C_{L'}}$ is the operating frequency of the RO when $C_{sen} = 0$, and $S = \frac{f_0}{C_{L'}}$ is the sensitivity. Sensitivity S can be improved by operating at higher f_0 and by reducing C_{par} at the electrode interface.

Tuning Range

A temperature-compensated bias network, located at the edge of each row, is used to tune the RO over the required 5 MHz to 180 MHz operating range. The architecture of the bias network is shown in Figure 2.4. A temperature-stabilized voltage V_{ref}, from an off-chip source, is applied to the non-inverting terminal of an operational transconductance amplifier (OTA). Reference current I_{ref} is generated by imparting V_{ref} across digitally selected poly-silicon resistors R1 to R8, forming a voltage-controlled current source. Current I_{ref} is mirrored to transistors M_p and M_n to generate I_D used to bias the current-starved inverters of the RO. For the selected RO device dimensions, and after accounting for parasitics at the electrode interface, I_D in the range of 10 μA–300 μA is necessary to achieve the required frequency range.

The bias network allows for three levels of RO frequency tuning. The first level of control is a form of coarse-grained tuning accomplished by varying V_{ref}. Once V_{ref} is set, a second level of control is made possible by varying I_{ref} through the resistors R1 to R8. This allows for multiple pixels in a column to operate in unique frequency bands when the bias setting is fixed by V_{ref}. A third level of fine-grained tuning is accomplished by adjusting the current mirror ratio in the bias network. The effective width of the PMOS device M_5 can be varied by adding or removing unit-width diode-connected PMOS devices (M6 to M12) to the network.

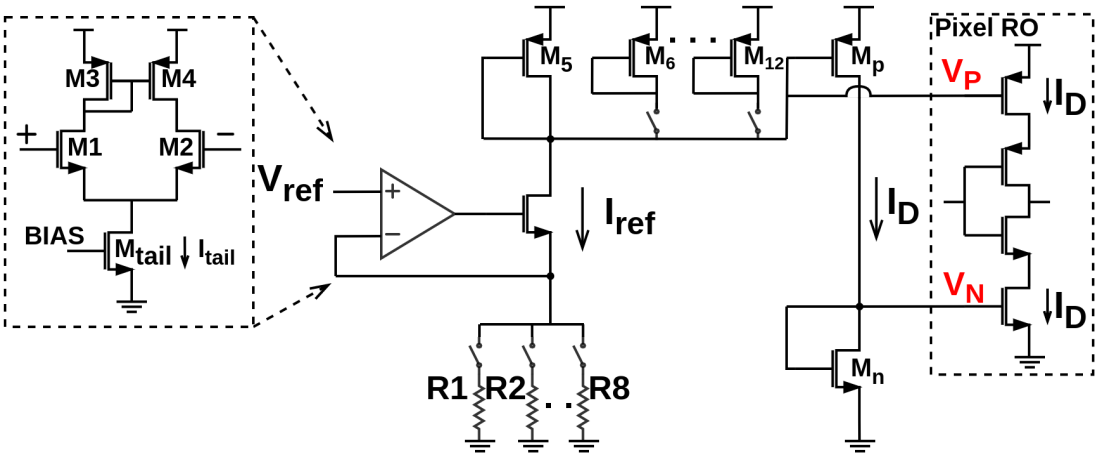


Figure 2.4: Temperature-compensated bias network.

Temperature Stability

Frequency f_{op} can be kept relatively stable over a 10°C–70°C range by compensating for the temperature dependence of I_D. For devices in saturation, I_D is given by

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2. \tag{2.9}$$

From 2.9 it can be seen that a decrease in the carrier mobility μ, due to an increase in temperature, decreases I_D. However, a decrease in the threshold voltage V_{th}, due to an increase in temperature, increases I_D.

Current I_D is measured to be proportional-to-absolute-temperature (PTAT) over the required operating range of temperatures, as shown in Figure 2.5. To enhance the stability of I_D over this range, the complementary temperature dependence of poly-silicon resistors R1 to R8 is used. The simulated temperature coefficient (TC) of I_D, when using poly-silicon

resistors, is approximately 36 nA/°C, which translates to a f_{op} TC of 36 kHz/°C. Without the resistor-based compensation, the simulated f_{op} TC is 1.15 MHz/°C.

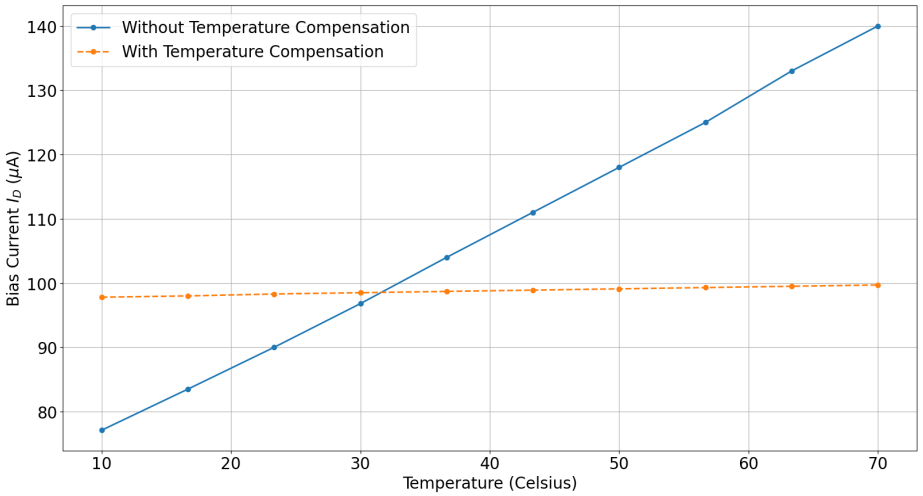


Figure 2.5: Temperature dependence of I_D with and without temperature compensation.

Power Consumption

The average current I_{avg} drawn by the RO is the bias current I_D. The average power consumed P_{avg} per pixel is therefore given by:

$$P_{avg} = V_{DD} \times I_{avg} = V_{DD} \times I_D. \tag{2.10}$$

For I_D in the range 10 uA–400 uA, and $V_{DD} = 1.8$ V, P_{avg} varies from 18 μW to 760 μW per active pixel.

2.1.3 Current Source Design

A current source within each pixel allows for current–mode operation of the RO, and facilitates FDM readout of a column of pixels. Figure 2.6 shows the complete pixel circuit, including the gated current source formed by transistors M5, M6, and M7. When control

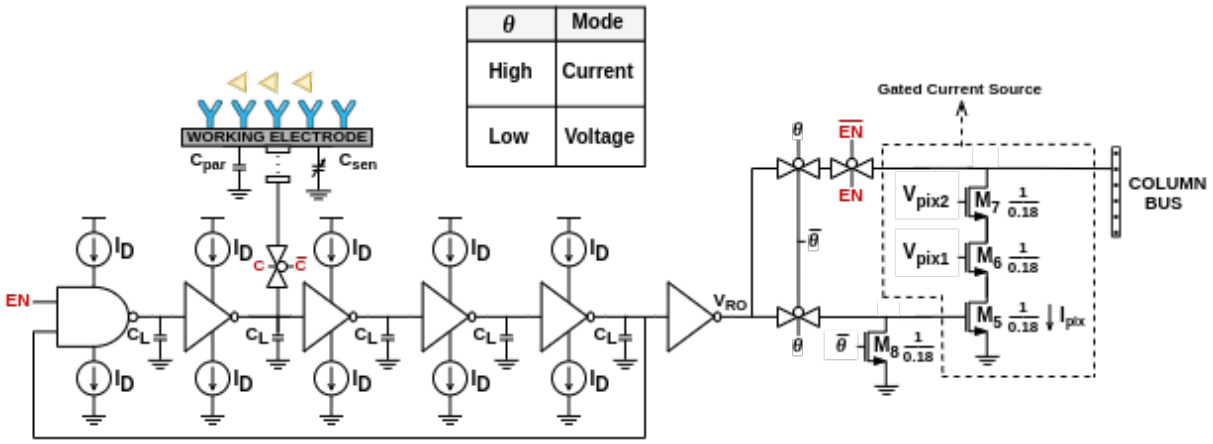


Figure 2.6: Complete pixel circuit with RO and gated current source.

signal θ is enabled, the signal V_{RO} drives transistor M5 between triode and cutoff regions through a transmission gate. Transistors M6 and M7 form a cascode current source, biased from a mirror network external to the pixel. The cascode structure offers higher output resistance r_o compared to a single NMOS current source, where r_o is given by:

$$r_o \approx g_{m7} \times r_{o6} r_{o7}, \tag{2.11}$$

where g_{m7} is the small-signal transconductance of M7, and r_{o6}, r_{o7} are the output resistances of transistors M6 and M7, respectively. We choose device dimensions accordingly to achieve a pixel current I_{pix} in the range of 10 μA–50 μA, and $r_o \approx 5$ MΩ per pixel.

2.1.4 Pixel Simulation Results

Tuning Range

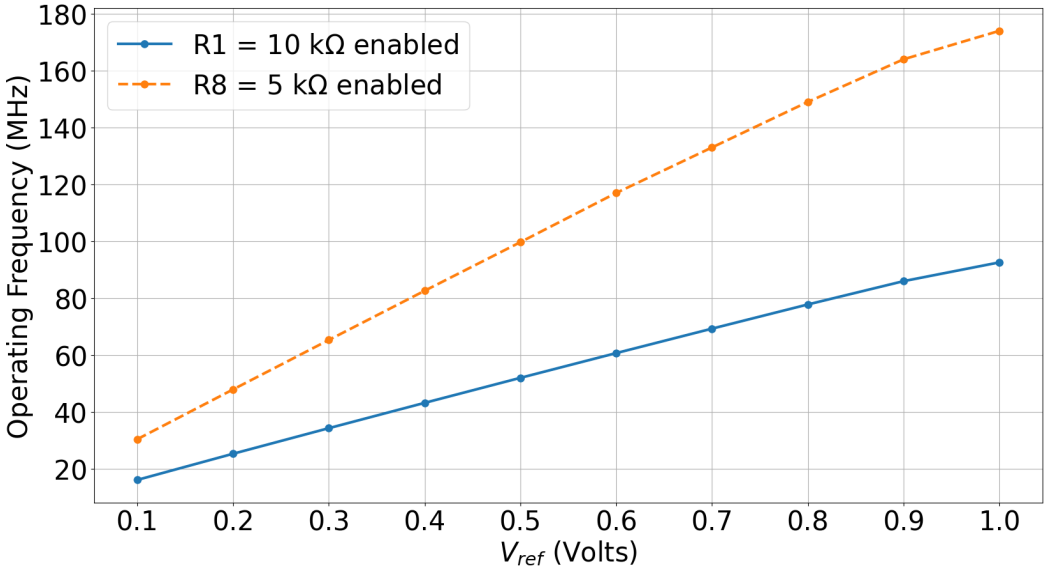
Figure 2.7(a) shows the ability to tune the operating frequency of the RO by varying the voltage V_{ref} between 0.1 V and 1 V. Once the bias voltage is fixed ($V_{ref} = 1$ V), a second level of tuning is accomplished by varying I_D through resistors R1 to R8, as shown in Figure 2.7(b).

Sensitivity and Detection Range

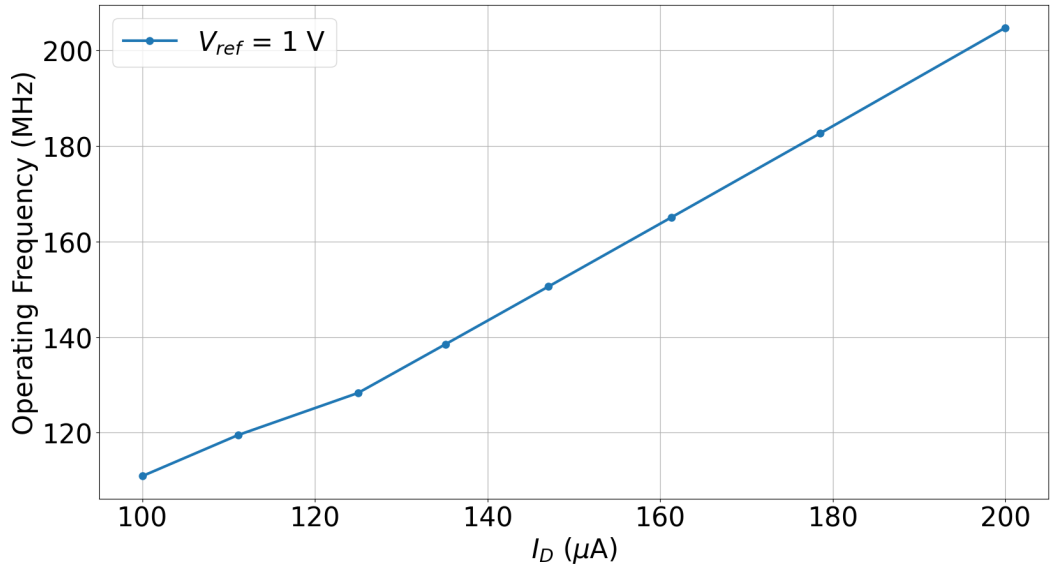
We ran simulations with a single active pixel to verify the theoretical transfer characteristic developed in Section 2.1.2. To estimate the highest achievable sensitivity for the device dimensions chosen, C_{par} is assumed to be negligible. Figure 2.8(a) shows the simulated transfer characteristic for a single pixel when C_{sen} is varied over a 1 pF range. Although the transfer characteristic is nonlinear as predicted by 2.5, the response can be linearized for small changes in C_{sen}. Figure 2.8(b) shows the response over a 170–fF range for $f_0 =$ 40 MHz, 80 MHz, and 160 MHz. The sensitivity $S \approx f_0/C'_L$ approximately doubles for each doubling in f_0, which is expected from 2.7. The inclusion of C_{par} at the electrode interface decreases S.

Frequency Uncertainty

Random fluctuations in the phase, and therefore, the frequency, limits the ability of the RO to detect real-time changes in C_{sen}. The uncertainty in the measured f_{op} can be attributed

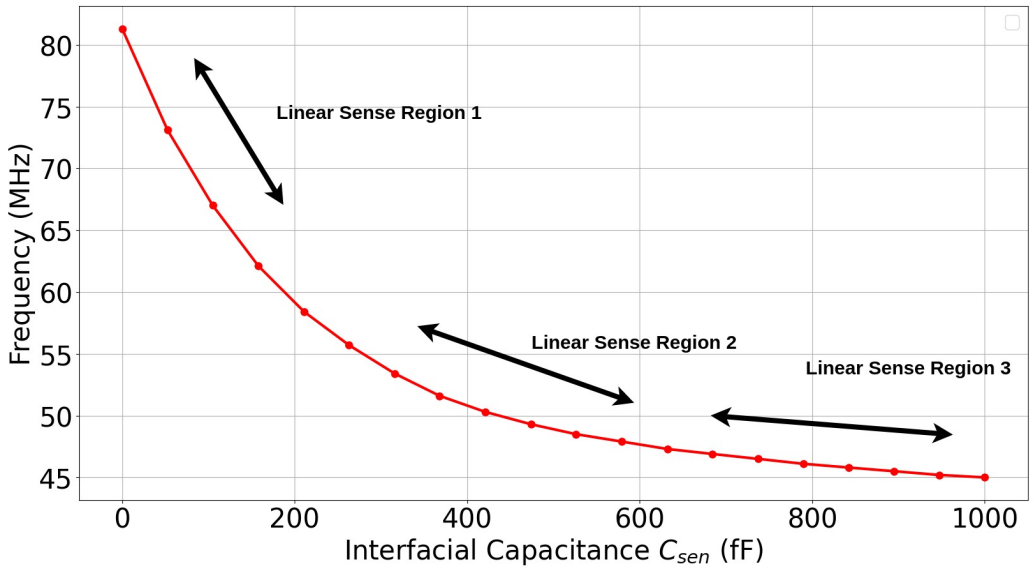


(a)

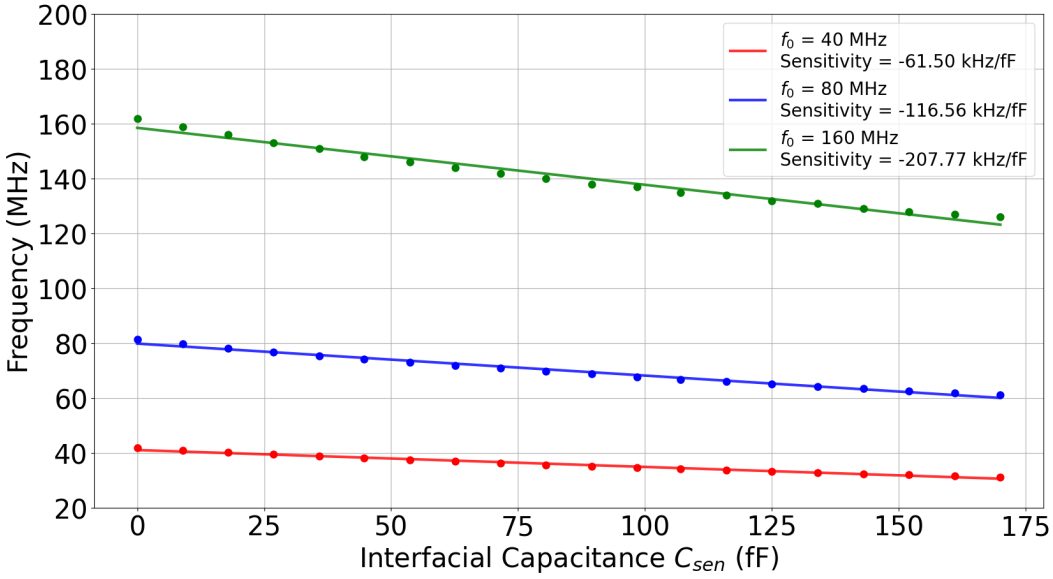


(b)

Figure 2.7: Tuning ring oscillator by varying (a) V_{ref} and (b) I_D for $V_{ref} = 1$ V.



(a)



(b)

Figure 2.8: Transfer characteristic simulations (a) over 1 pF range and (b) for different f_0.

to the phase noise of the RO. While the design was not optimized for a specific phase noise specification, we ran simulations to investigate its impact on the LOD.

Figure 2.9 shows the single-sideband phase noise $L(f)$ over a 1 kHz–200 MHz frequency offset for f_{op} = 70 MHz, 117 MHz, and 172 MHz. Flicker noise dominates over a 100 MHz frequency offset, with a steady -30 dB/decade roll-off. The RMS frequency deviation Δf_{rms} is obtained by integrating $L(f)$ over the frequency range of interest, and is given as

$$\Delta f_{rms} = \sqrt{2 \int_{f_1}^{f_2} f^2 \times L(f)\, df}, \tag{2.12}$$

where f_1 and f_2 are the lower and upper limits of integration, respectively. We assume f_1= 1 kHz and f_2 = 1 MHz to capture the phase noise contribution close to f_{op}. Simulation results yield Δf_{rms} = 28 kHz for f_{op} = 70 MHz, 52 kHz for f_{op} = 117 MHz, and 89 kHz for f_{op} = 172 MHz.

2.1.5 Summary of Pixel Specifications

A summary of the pixel simulation results is provided in Table 2.2.

2.2 Transimpedance Amplifier Design

The current source within each enabled pixel in Figure 2.6 drives the corresponding column bus when the pixel is operated in current mode. A high bandwidth TIA is required to drive the column bus signal off the chip. In this section, we discuss the design process for the TIA.

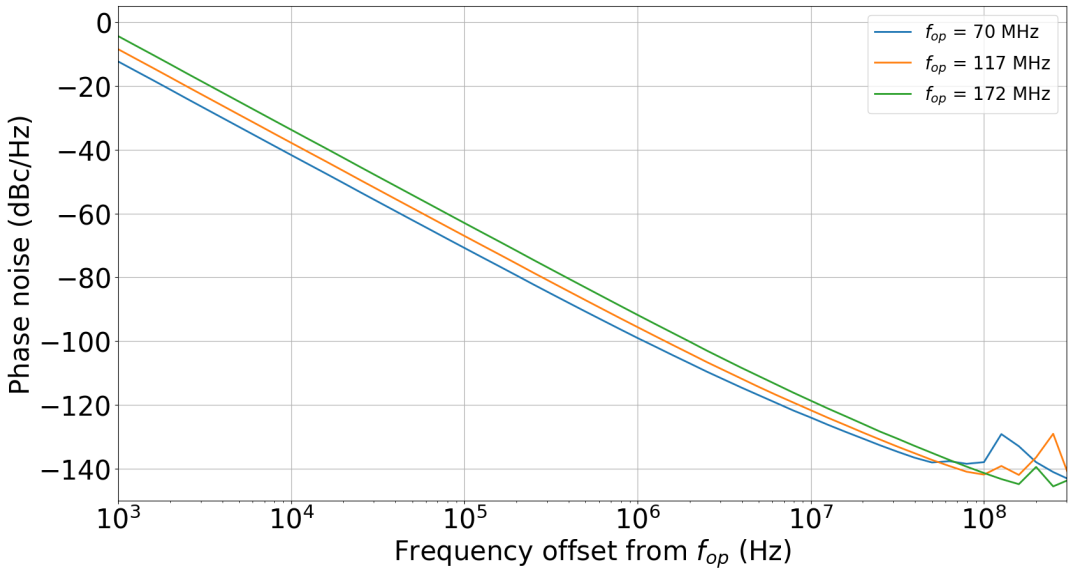


Figure 2.9: Phase noise $L(f)$ for various f_{op}.

2.2.1 Target Specifications

The RO is designed to operate at frequencies up to 180 MHz. To provide some margin, the TIA is therefore designed to meet a target -3–dB bandwidth of 200 MHz. Further, the TIA must drive the off-chip capacitive load presented by a standard oscilloscope used for signal readout. We estimate this capacitive load to be in the 20–pF to 25–pF range, which includes contributions from interconnect parasitics.

Given that there is design flexibility with the pixel current amplitude, the gain of the TIA is set to ensure a minimum voltage signal level of 5 mV peak-to-peak at the input of the oscilloscope, while also achieving the 200 MHz bandwidth. For minimum $I_{pix} = 10$ μA, the minimum required gain is therefore set to 500 Ω (53.9 dBΩ). The target specifications for the TIA are presented in Table 2.3.

Parameter	Target	Simulated
Frequency Range	5 MHz to 180 MHz	1.8 MHz to 218 MHz
Pixel Current	10 μA to 50 μA	8 μA to 63 μA
RMS Frequency Deviation	-	28 kHz @ 70 MHz 52 kHz @ 117 MHz 89 kHz @ 172 MHz
Temperature Coefficient	-	36 kHz/°C
Detection Range (C_{sen})	150 fF	1 pF
Max Sensitivity (kHz/fF)*	-	-61.5 @ 40 MHz -116.56 @ 80 MHz -207.77 @ 160 MHz
Power Consumption	-	10 μW to 760 μW

Table 2.2: Summary of pixel simulated performance.

*Results were obtained while varying C_{sen} over a 150 fF range and assuming C_{par} is negligible.

2.2.2 Proposed Topology

We implement a resistive feedback TIA as shown in Figure 2.10. The gain of this topology is given by

$$\frac{V_{out}}{I_{in}} = \frac{-A_o R_F}{1 + A_o}, \tag{2.13}$$

where R_F is the feedback resistance and A_o represents the open-loop gain of the voltage amplifier, realized by a differential pair with active PMOS load. A differential input topology is favoured over a single-ended topology since the column bus voltage can be varied

Parameter	Target
Gain	$\geq 500\ \Omega$
Bandwidth	200 MHz
Phase Margin	$\geq 45^{\circ}$
Input-Referred Current Noise	$\leq 10\ \mu\mathrm{A}_{rms}$

Table 2.3: TIA target specifications.

by setting the voltage V_{CM} at the non-inverting input terminal of the differential pair. For $A_o \gg 1$, the gain $\frac{V_{out}}{I_{in}} \approx -R_F$.

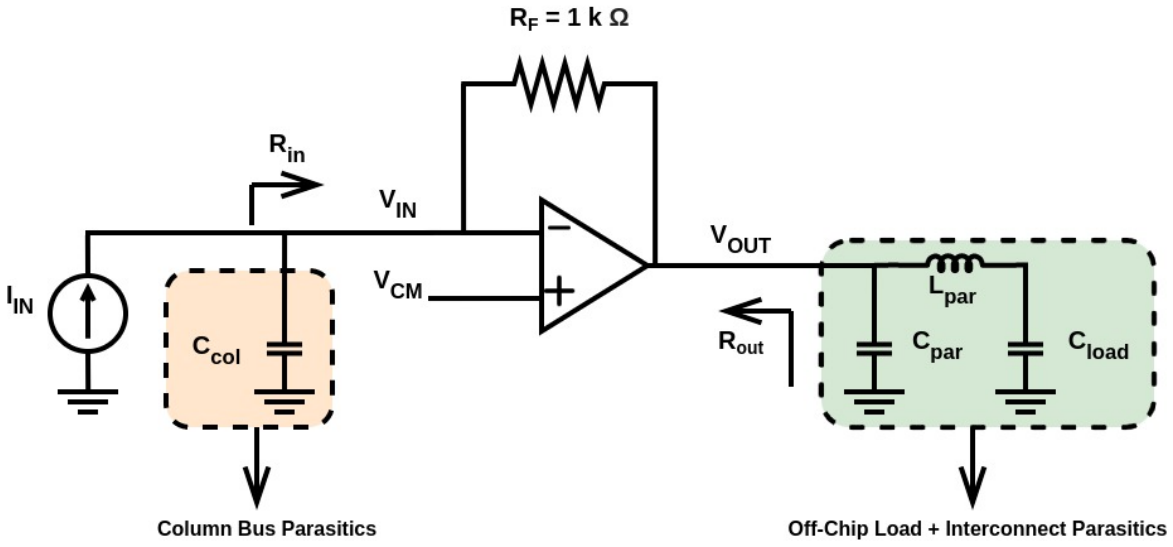
A diode-connected NMOS transistor is used to bias the tail current source formed by transistor M_{tail}, for all eight TIAs on the chip. The mirror ratio is set to five to facilitate large bias currents on the order of 5 mA per TIA. The current into the bias network I_{TIA} is varied using an off-chip potentiometer.

2.2.3 Bandwidth

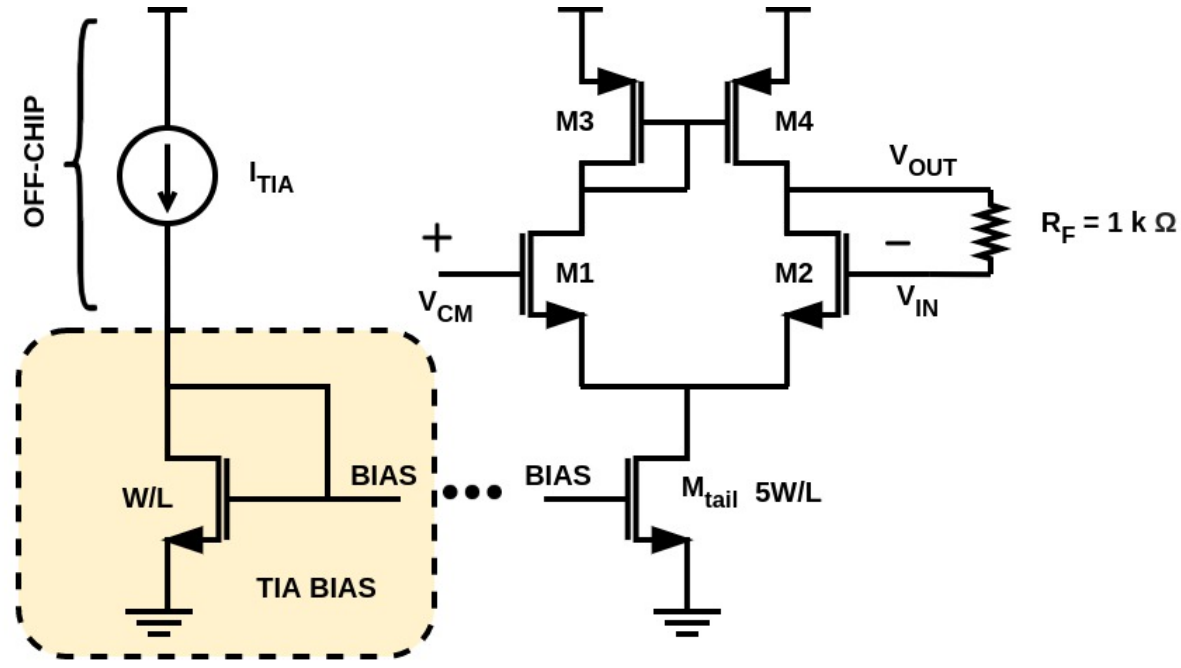
At the TIA input, the bandwidth is limited by the array column capacitance C_{col} and the TIA input resistance R_{in}. The pole frequency formed at the input $f_{p1,TIA}$ is given by

$$f_{p1,TIA} = \frac{1}{2\pi C_{col} R_{in}}. \tag{2.14}$$

Capacitance C_{col} includes the output capacitance of all pixels on the column bus and interconnect parasitics. We estimate C_{col} to be ≈ 1 pF from post-layout parasitic extraction. The input resistance R_{in} for this topology is given by



(a)



(b)

Figure 2.10: TIA (a) architecture and (b) transistor-level implementation.

$$R_{in} = \frac{R_F}{1 + A_o}. \tag{2.15}$$

For the amplifier in Figure 2.10(a), the open-loop dc gain A_o is given by

$$A_o = g_{m_{1,2}} \times r_{o2}||r_{o4}, \tag{2.16}$$

where $g_{m_{1,2}}$ is the small-signal transconductance of transistor M1 and M2, and r_{o2}, r_{o4} are the output resistances of transistors M2 and M4, respectively.

At the output of the TIA, the bandwidth is limited by the load capacitance C_{load} and output resistance R_{out}. The pole frequency $f_{p2,TIA}$ at the output is given by

$$f_{p2,TIA} = \frac{1}{2\pi C_{load} R_{out}}, \tag{2.17}$$

where R_{out} represents the output resistance of the TIA, and is given by

$$R_{out} = \frac{r_{o2}||r_{o4}}{1 + A_o} = \frac{r_{o2}||r_{o4}}{1 + g_{m_{1,2}}(r_{o2}||r_{o4})}. \tag{2.18}$$

Using the expression for R_{in} and R_{out}, $f_{p1,TIA}$ and $f_{p2,TIA}$ can also be expressed as

$$f_{p1,TIA} = \frac{1 + g_{m_{1,2}}(r_{o2}||r_{o4})}{2\pi C_{col} R_F} \tag{2.19}$$

$$f_{p2,TIA} = \frac{1 + g_{m_{1,2}}(r_{o2}||r_{o4})}{2\pi C_{load}(r_{o2}||r_{o4})} \approx \frac{g_{m_{1,2}}}{2\pi C_{load}}. \tag{2.20}$$

A large dc tail current $I_{tail} \geq 5$ mA is used to obtain $g_{m_{1,2}} = 24.6$ mS for the input pair. The output pole $f_{p2,TIA}$ dominates the frequency response since $C_{load} \gg C_{col}$. For $C_{load} =$ 20 pF, $f_{p2,TIA} \approx 200$ MHz. For fixed $R_F = 1$ kΩ, and $A_o \approx 16$ V/V, the midband gain is approximately 940 Ω. Transistor dimensions for the TIA are summarized in Table 2.4

Device	**Aspect Ratio** $\frac{W}{L}$ $(\frac{\mu m}{\mu m})$	$\frac{I_D}{W}$ $(\frac{mA}{\mu m})$
M_{tail}	$\frac{100}{0.5}$	0.05
M1, M2	$\frac{100}{0.5}$	0.025
M3, M4	$\frac{200}{0.5}$	0.0125

Table 2.4: Transistor sizing for TIA.

2.2.4 Noise

We analyzed the input-referred noise current of the TIA to compare the minimum pixel current to the noise floor. The noise contributions from the feedback resistor R_F and the differential pair amplifier were accounted for.

The input-referred noise current power spectral density (PSD) $\overline{I^2_{n,TIA}(f)}$ is given by:

$$\overline{I^2_{n,TIA}(f)} = \overline{I^2_{n,res}(f)} + \overline{I^2_{n,diff}(f)}, \tag{2.21}$$

where $\overline{I^2_{n,res}(f)}$ and $\overline{I^2_{n,diff}(f)}$ are the input-referred noise contributions from R_F and the differential pair, respectively.

The individual contributions can be further expanded as:

$$\overline{I^2_{n,TIA}(f)} = \left(\frac{4k_BT}{R_F}\right) + \left(\overline{I^2_{n,G}(f)} + \overline{I^2_{n,D}(f)}\right), \tag{2.22}$$

where $\overline{I^2_{n,G}(f)}$ and $\overline{I^2_{n,D}(f)}$ are the gate current induced shot noise and channel thermal noise of the input pair, respectively. The noise from the feedback resistor $R_F = 1$ kΩ dominates the contributions from the devices, yielding an input-referred rms noise current of $I^{rms}_{n,TIA} = 68.44\ nA_{rms}$. An SNR ≥ 41 dB is achieved at the input of the TIA due to design flexibility with the pixel current amplitude (10 uA to 50 uA).

2.2.5 TIA Simulation Results

Gain

Figure 2.12 shows the frequency response of the TIA with feedback resistor $R_F = 1$ kΩ. The TIA is biased with a tail current of 5 mA. An LC network, as shown in Figure 2.10, is used to model the interconnect parasitic capacitance C_{par} (1 pF) and bondwire inductance L_{par} (5 nH). Capacitance C_{load} is set to 20 pF. The simulated gain is 59.2 dBΩ (912 Ω). A -3 dB bandwidth of 198 MHz is achieved.

Noise

Figure 2.12 shows the input-referred current noise PSD for the TIA. For a single-pole system, the equivalent noise bandwidth is given by $f_{n,-3dB} = \frac{\pi}{2} \times f_{p2,TIA} = 315$ MHz. Integrating over $f_{n,-3dB}$, while setting the lower limit of integration to 100 Hz, the input-referred rms noise current $I^{rms}_{n,TIA} \approx 79.2\ nA_{rms}$ which is comparable to theoretical calculations.

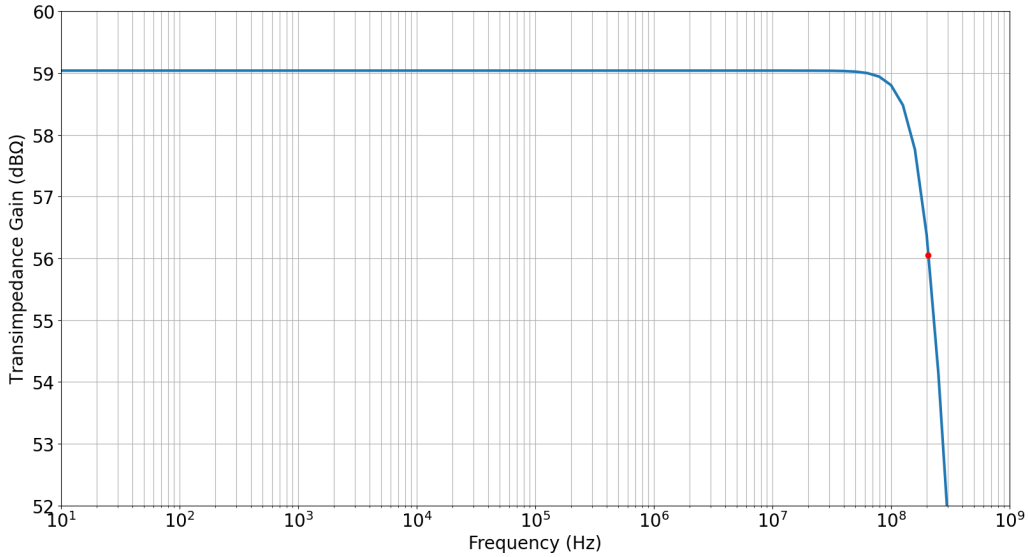


Figure 2.11: Gain of TIA versus frequency.

Stability

The stability of the TIA is assessed to ensure a phase margin $\geq 45°$. Figure 2.13 shows the loop gain magnitude and phase response. The phase margin is measured to be approximately 78°.

2.2.6 Summary of TIA Specifications

A summary of the TIA performance specifications is provided in Table 2.5.

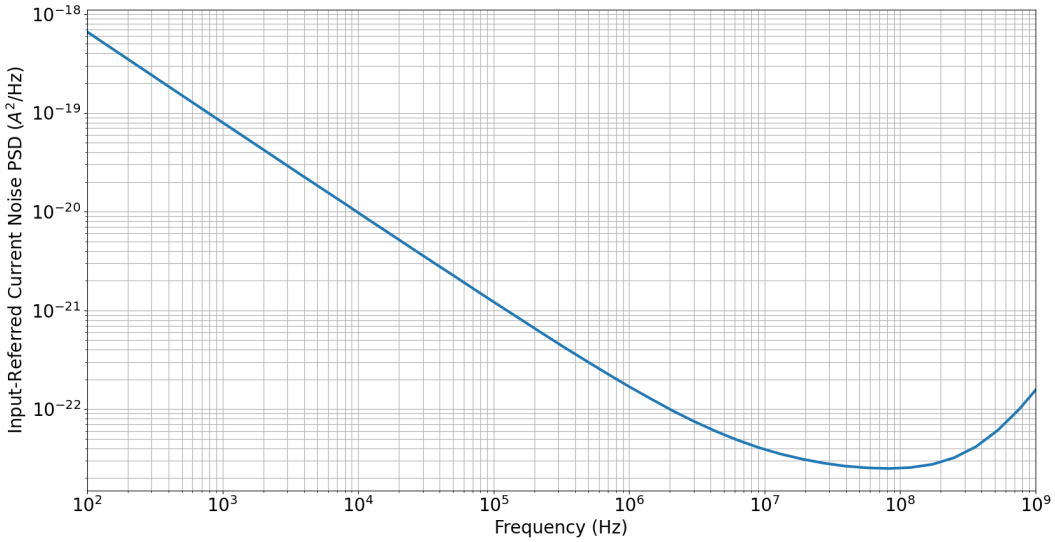


Figure 2.12: TIA input-referred current noise PSD from 100 Hz to 1 GHz.

2.3 Voltage Buffer Design

When a pixel is operated in voltage mode, the output of the RO is connected directly to the corresponding column bus through a transmission gate, as shown in Figure 2.6. A buffer is required to drive the rail-to-rail voltage signal off the chip.

2.3.1 Proposed Topology

The voltage buffer topology we employ is commonly used for driving high-speed digital signals off-chip. The architecture is shown in Figure 2.14. The buffer consists of four inverter stages. The aspect ratio of the devices in each stage is progressively increased by

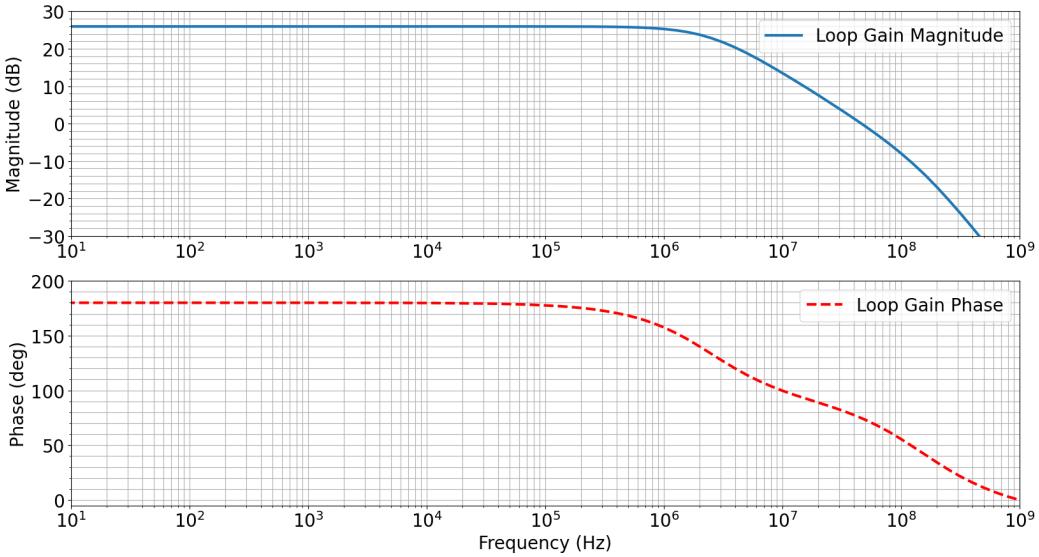


Figure 2.13: TIA loop gain magnitude and phase.

a factor of ten, which results in a simulated rise/fall time of ≈ 0.8 ns with $C_L = 20$ pF. Transistor sizing for each stage of the buffer is provided in Table 2.6.

2.3.2 Simulation Results

Simulation results for the voltage buffer operating at 200 MHz are shown in Figure 2.15. The load network shown in Figure 2.10(a) simulates the contributions of interconnect parasitics and the input impedance of a standard oscilloscope.

Parameter	Target	Simulated
Gain	$\geq 500\ \Omega$	$912\ \Omega$
Power Consumption	-	9 mW @ 5 mA tail current
Bandwidth	180 MHz	198 MHz
Phase Margin	$\geq 40^{\circ}$	78°
Input-Referred Current Noise	$\leq 10\ \mu A_{rms}$	$79.2\ nA_{rms}$

Table 2.5: TIA performance specifications

Device	Aspect Ratio (N | P) $\frac{W}{L}$ $(\frac{\mu m}{\mu m})$
Stage 1	$\frac{0.22}{0.18} \mid \frac{0.44}{0.18}$
Stage 2	$\frac{1}{0.18} \mid \frac{2}{0.18}$
Stage 3	$\frac{10}{0.18} \mid \frac{20}{0.18}$
Stage 4	$\frac{100}{0.18} \mid \frac{200}{0.18}$

Table 2.6: Transistor sizing for voltage buffer.

2.4 Digital Shift Registers

The chip has two 128-bit shift registers and one 64-bit shift register to set various control signals on the chip. The list of control signals include:

- Electrode switch control
- 64:8 Multiplexer control
- Pixel bias setting control

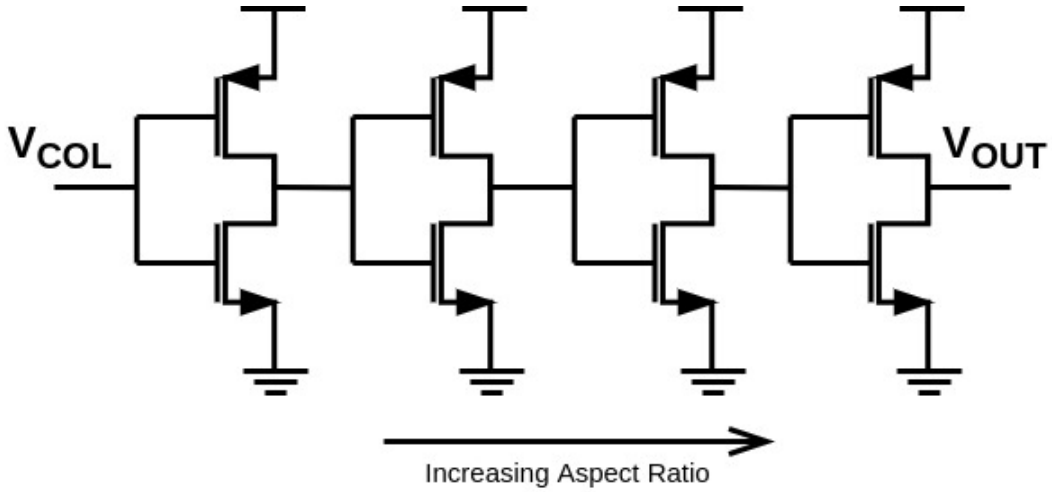


Figure 2.14: Voltage-mode buffer architecture.

- Pixel enable control
- Output mode selection control

The shift registers are implemented with D-flip-flops cascaded together, as shown in Figure 2.16. Each stage also includes four series inverters at the output to prevent hold time violations.

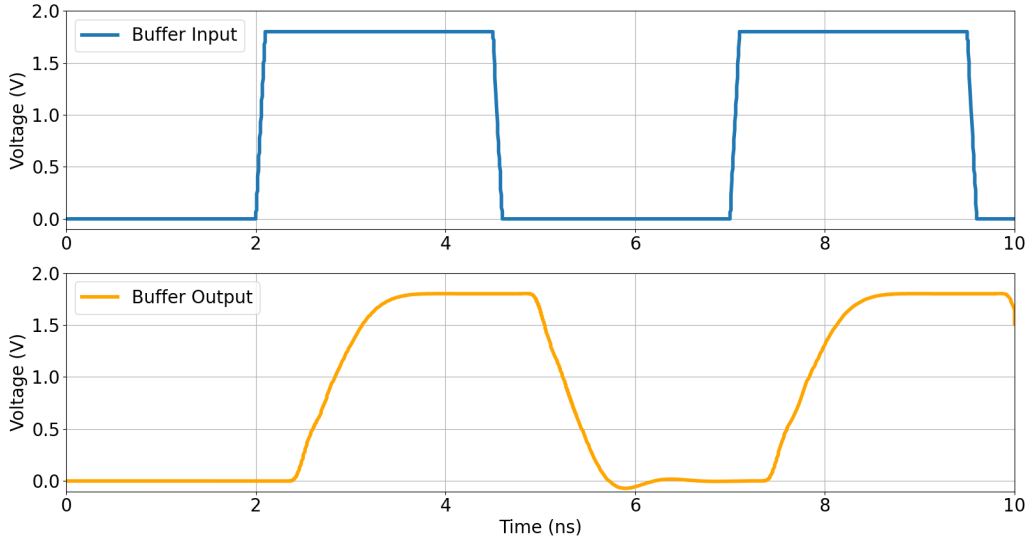


Figure 2.15: Transient simulation of voltage buffer at 200 MHz.

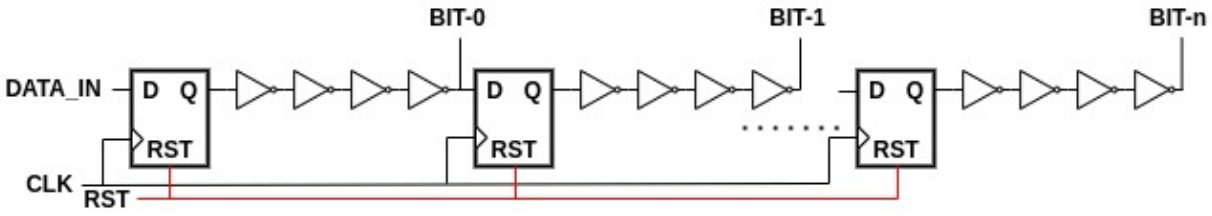


Figure 2.16: Shift register.

Chapter 3

Chip Architecture and System Design

In this chapter, we provide a system-level description of the chip architecture. The chapter begins with a detailed description of the chip floorplan. Different modes of operating the imager are also discussed. Finally, strategies for electrode fabrication are presented.

3.1 Chip Architecture

The architecture of the proposed capacitance imager is similar to that of a visible-light imager. A pixel forms the fundamental building block of a larger array. Integrating these pixels into large arrays allows for parallelized sensing.

3.1.1 Chip Floorplan

The floorplan of the proposed chip can be divided into five distinct sub-blocks, as shown in Figure 3.1.

- Pixel Arrays
- Pixel Bias
- Analog Multiplexers
- Column Readout Circuits
- Digital Control

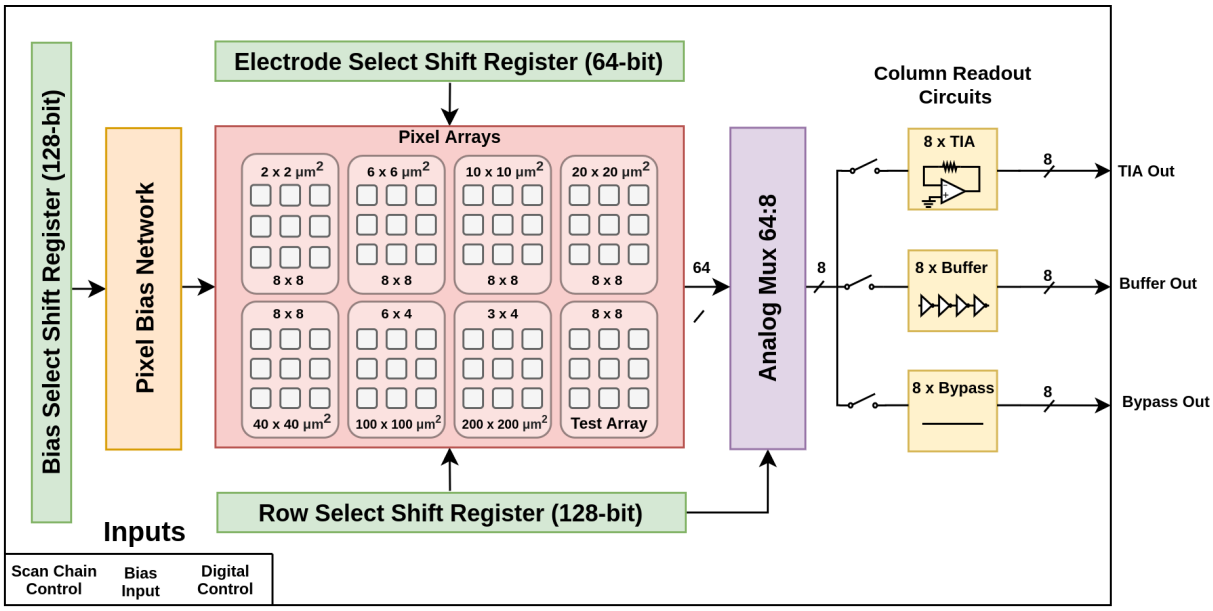


Figure 3.1: Electrochemical capacitance imager architecture.

Pixel Arrays

The active area of the chip consists of the electrodes and the underlying pixel circuits. As mentioned in Section 1.3.1, C_{dl} is influenced by the electrode dimensions. To test the response of different capacitance profiles, the chip is designed with eight unique arrays. Each array consists of identical pixel circuits. However, the electrodes connected to the pixel differ in area from array to array. A test array is also included, in which the electrode connected to each pixel is replaced by a configurable impedance network.

Table 3.1 shows the size and electrode dimensions of each array. The active area consists of a total of 420 pixels, 356 of which are usable for biosensing, while the remaining 64 are used for electronic testing.

Array	Electrode Dimensions (μm^2)	Rows × Columns	Number of Pixels
0	2 × 2	8 × 8	64
1	6 × 6	8 × 8	64
2	10 × 10	8 × 8	64
3	20 × 20	8 × 8	64
4	40 × 40	8 × 8	64
5	100 × 100	6 × 4	24
6	200 × 200	3 × 4	12
7 (Test Array)	-	8 × 8	64
	Total	**57 rows, 56 columns**	**420**

Table 3.1: Properties of eight on-chip electrode arrays.

Pixels are arranged in rows and columns as shown in Figure 3.2. The architecture allows for row-wise enabling and biasing of pixels. A total of 57 rows exist, and the control signals

required to enable/disable each row are generated by a 128-bit shift register. Further, only a single array can be operated at any given time. The output of a single column of pixels is connected to the corresponding column bus.

Pixel Bias

The operating frequency of the pixel RO is set by the temperature-compensated bias network described in Chapter 2. The imager is designed with eight identical pixel bias networks, capable of being tuned independently with digital control signals from a 128-bit shift register. The voltages V_p and V_n, generated by each bias network, are used to vary the current through each inverter stage of the RO. The single reference voltage V_{ref}, provided externally, is shared by all eight bias networks.

A row of pixels in an array shares V_p and V_n generated by a single bias network. Eight unique bias networks are required since there are a maximum of eight rows in an array of pixels. This allows for each row to operate in a unique frequency band.

Analog Multiplexers

The column bus of each array in the active area is connected to a single input of a 64:8 analog multiplexer, implemented with eight 8:1 multiplexers. The architecture is shown in Figure 3.3, and it employs transmission gates to select eight of the 56 available column bus signals (Table 3.1) to be driven off chip by readout amplifiers.

Since only one array is operational at any given time, the eight output signals from the 64:8 analog multiplexer represent the column bus signals of the operational array. Depending

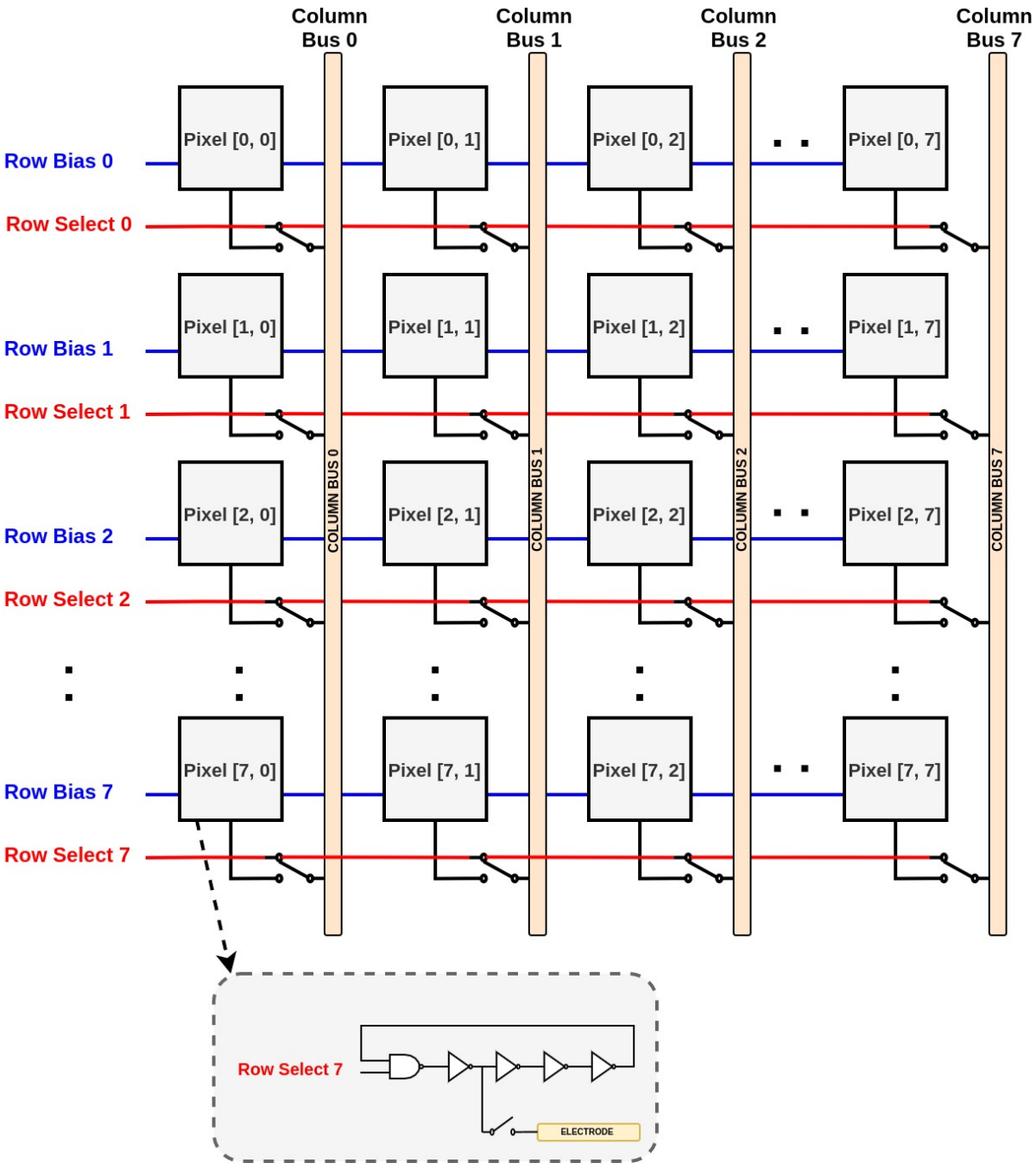


Figure 3.2: An 8×8 pixel array.

on the mode of operation, the output signals are driven directly off chip or are further switched between the on-chip TIA and voltage buffer, as shown in Figure 3.1.

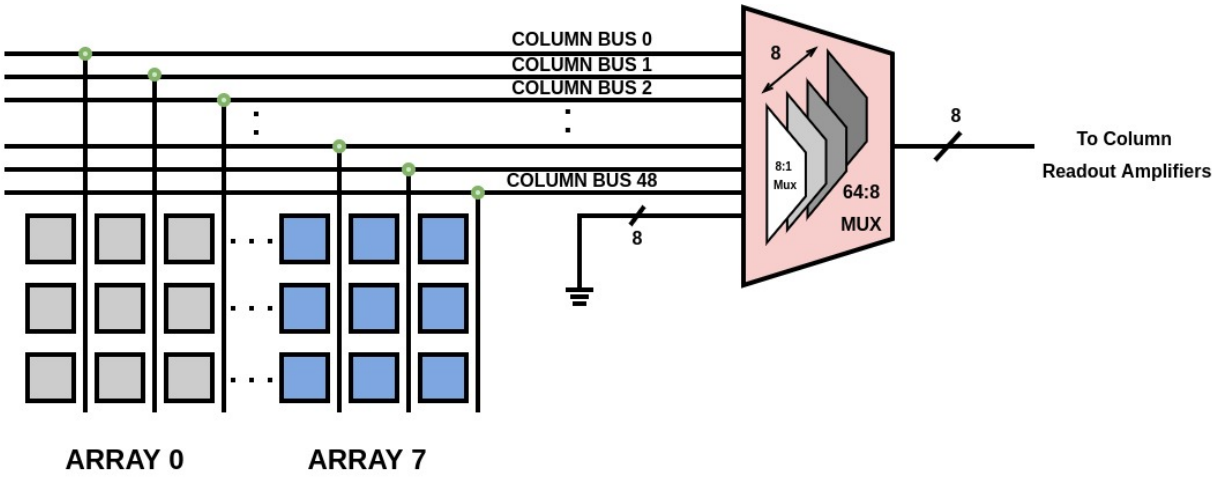


Figure 3.3: 64:8 Analog multiplexer.

Column Readout Circuits

The output signals from the 64:8 analog multiplexer are driven off chip by one of three types of column readout circuits:

- **TIA**: When operating in current mode, the high-speed TIAs convert the column bus current to a voltage, which then is driven off chip for digitization.
- **Voltage Buffer:** When operating in voltage mode, the voltage signal on the column bus (one active pixel) is driven off chip by a voltage buffer.
- **Bypass:** The column bus output can be directly driven off chip through bypass switches (i.e., the TIAs and voltage buffers can be bypassed).

Digital Control

Three shift registers are used to set the various digital control signals required to operate the imager. Each shift register converts a serial input bit pattern into a parallel output. The chip is designed with two 128-bit shift registers and one 64-bit shift register. The 64-bit shift register is used exclusively to connect/disconnect the WEs to the underlying pixels. The output of each shift register is routed to an output pad on the chip which is used for debugging purposes.

3.1.2 Power Domains

The chip is powered by two 1.8–V power rails: analog VDD (AVDD) and digital VDD (DVDD). The power rails are referenced to analog ground (AVSS) and digital ground (DVSS), respectively. AVDD powers the pixels, the pixel bias network, and the column readout circuits. DVDD is used to power the shift registers and other control circuits. The substrate (body) terminals of all NMOS transistors on the chip are connected to AVSS. Sensitive analog blocks are placed within guard rings to prevent interference caused by switching activity on the digital rail.

3.1.3 Electrodes

The electrodes serve as the interface between the analyte and pixel circuit. The 0.18-μm CMOS process used has six aluminum interconnect layers. The electrodes are formed using the top metal layer (metal-6) of the CMOS process.

The electrochemical properties of the electrode must be considered before carrying out on-chip biosensing. Since aluminum is electrochemically active, post-processing of the electrodes formed on the metal-6 layer is required. In this work, the electrode fabrication process is not carried out, however, two options for fabrication are presented in Figure 3.4.

The first option involves deposition of a noble metal on top of metal-6. Gold is typically used for its biocompatibility and good conductivity. Alternatively, the top metal layer can be wet etched, exposing the tungsten vias below. The vias can either directly interact with the analyte, or can be coated with a biocompatible layer.

3.1.4 Protection Circuits

The input and output (I/O) pads on the chip are protected from overvoltages, transient voltages, and reverse polarity connections. Specifically, AVDD and DVDD are protected with series-connected diodes to protect on-chip circuits from damage due to electrostatic discharge (ESD) events.

3.1.5 On-Chip Impedance Network

To test the sensitivity of the RO to changes in the interfacial capacitance, an on-chip impedance network is used as shown in Figure 3.5. A dedicated portion of the test array is connected directly to a configurable passive network, instead of electrodes. The pixels that are not connected to an impedance network serve as reference pixels, and are used in the calibration process of the sensor. The impedance network provides interfacial capacitance in the 10-fF–170-fF range in 10 fF increments, and 0.2-kΩ–10-kΩ shunt resistors which are

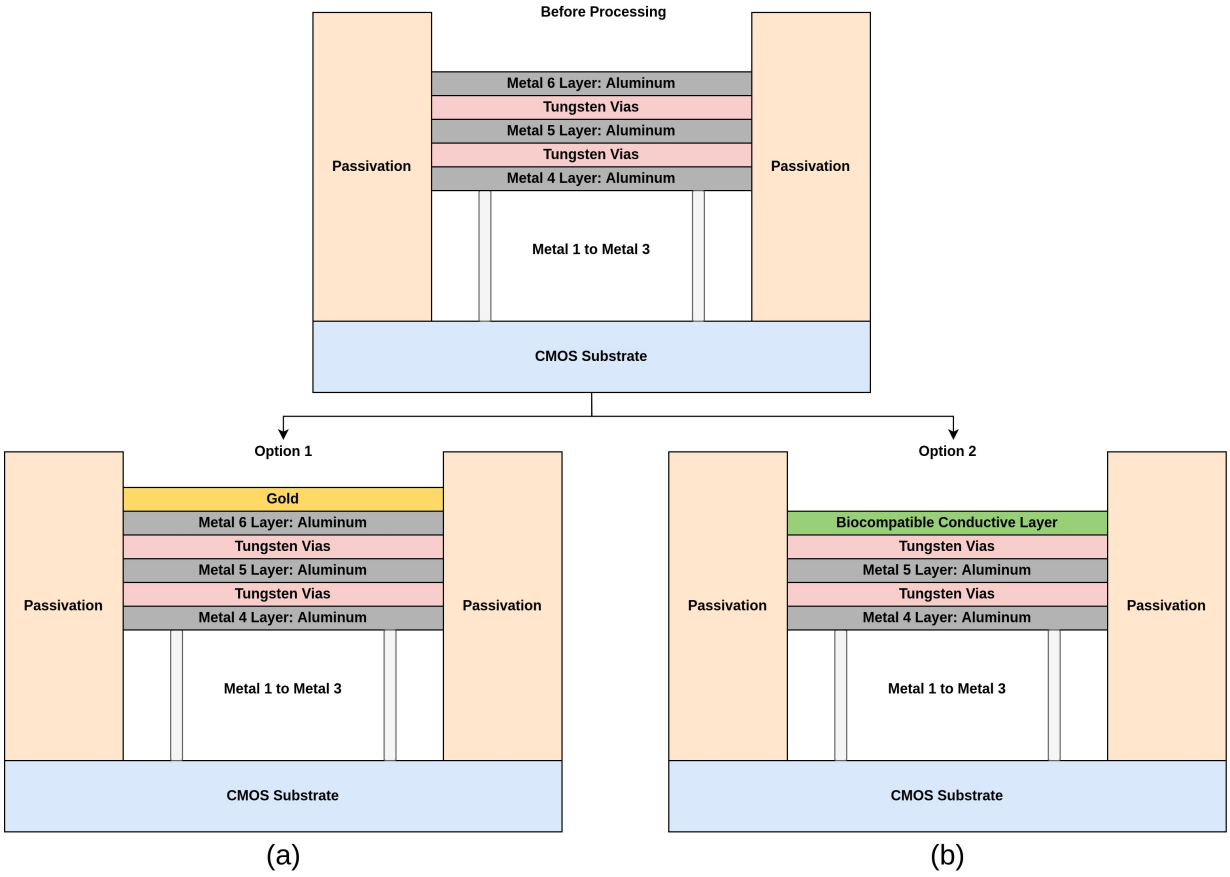


Figure 3.4: Electrode fabrication options with (a) gold layer and (b) biocompatible conductive layer.

enabled through digitally-controlled transmission gates. These networks allow for modelling of the electrode-electrolyte interface for processes occurring within and beyond the EDL. This enables purely electronic characterization of the performance of the sensor.

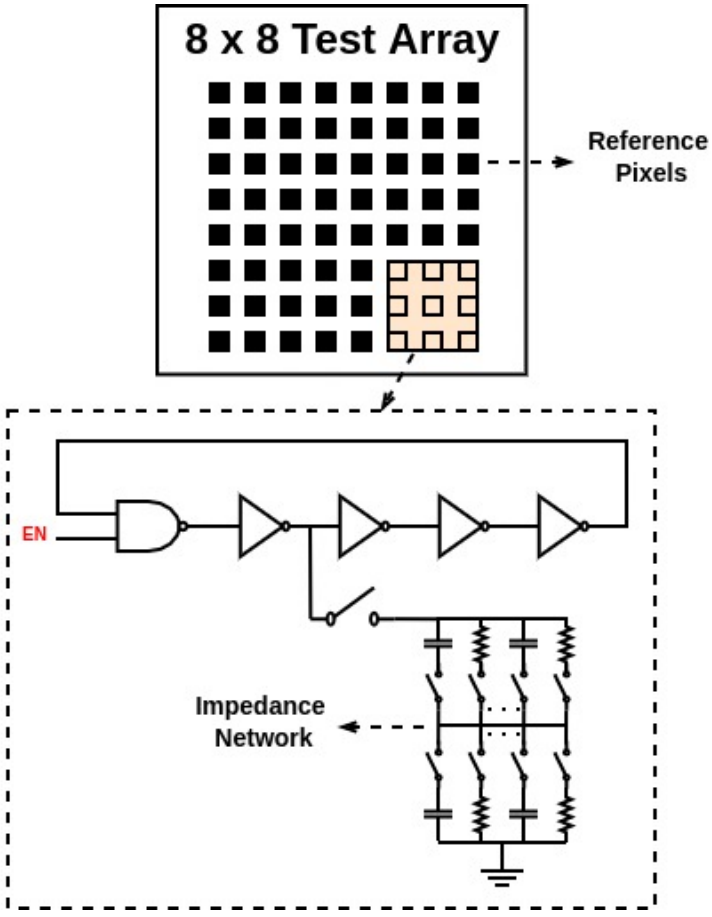


Figure 3.5: Test impedance network.

The die photograph of the electrochemical capacitance imager is shown in Figure 3.5. The chip has been fabricated in a TSMC 1.8–V, six-metal, 0.18–μm CMOS process and has dimensions of 3.0 mm $\times$ 2.5 mm. Further, the chip contains 84 I/O pads and is packaged in a ceramic pin grid array (CPGA) package.

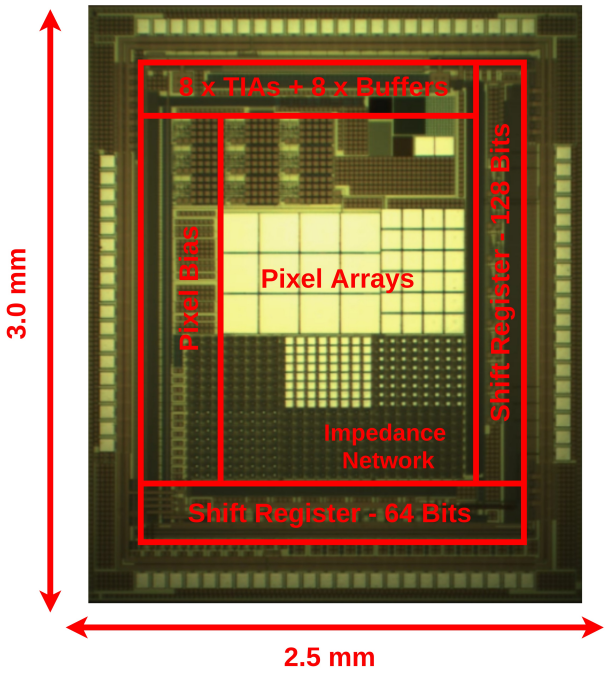


Figure 3.6: Die photograph of the electrochemical capacitance imager.

3.2 Modes of Operation

Each pixel in the array can be operated in either voltage mode or current mode. When operating in voltage mode, only TDM readout is possible, since only a single pixel can drive the column bus at any given time. Current-mode operation supports both TDM and FDM readout.

Chapter 4

Experimental Results

In this chapter, we report on the experimental characterization of the electronic performance of the fabricated capacitance imager prototype.

4.1 Electronic Characterization Setup

The system diagram in Figure 4.1 shows the supporting electronics and measurement apparatus required to operate the imager. The output signals from the on-chip TIA and voltage buffers are digitized by an oscilloscope. Since the signal of interest is a change in the operating frequency of the enabled pixels, the frequency-domain representation of the output signal is acquired by applying a fast-Fourier transform (FFT) to the time-domain signal. The change in the individual frequency components of the resulting signal are mapped to corresponding changes in C_{sen}.

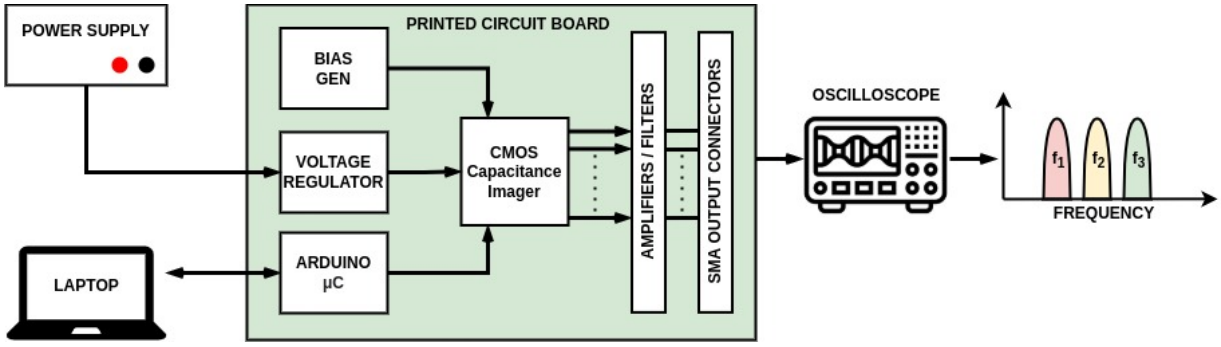


Figure 4.1: System diagram for electronic characterization.

4.1.1 Printed-Circuit Board Design

We designed a custom four-layer printed-circuit board (PCB) to characterize the performance of the CMOS imager, as shown in Figure 4.2. Voltage references and other bias circuits required to operate the chip are integrated onto the PCB. Further, the output signals from the on-chip column readout amplifiers can be amplified or filtered on the PCB by off-the-shelf components before digitization by an oscilloscope. Digital signals required to operate the on-chip shift registers (i.e., clock, reset, and data signals) are generated externally by an Arduino microcontroller board that connects directly to the PCB.

4.1.2 Software

The software used to control the Arduino is written in the C++ programming language. The I/O block on the Arduino generates the required signals to control the digital circuits on the capacitance imager. Python scripts are used to control measurement instrumentation to automate the acquisition process.

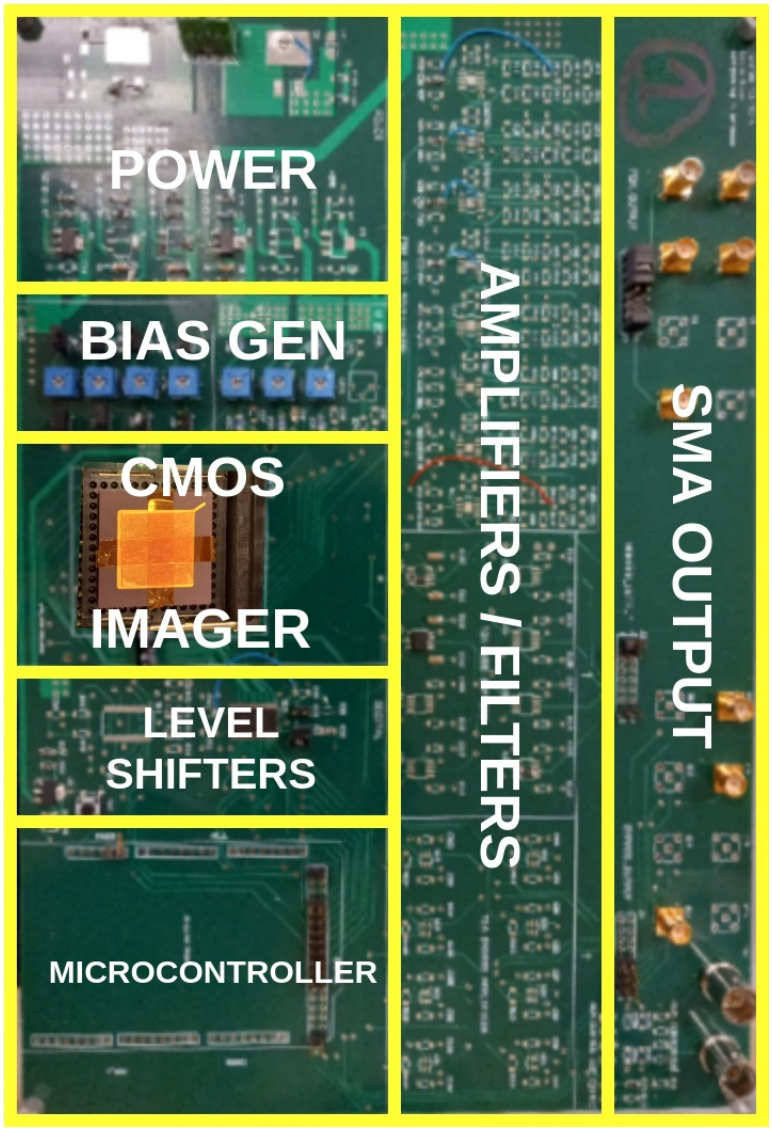


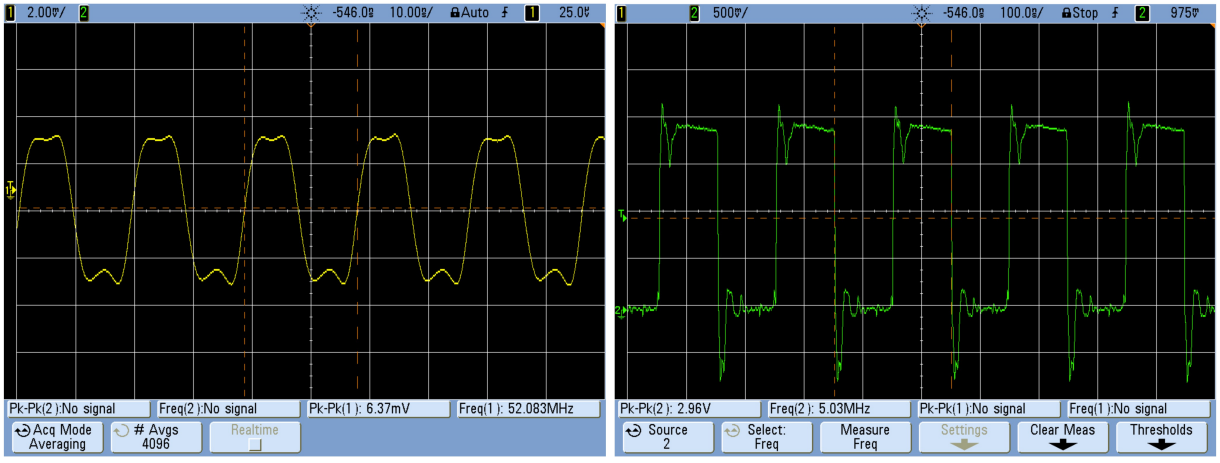
Figure 4.2: PCB used for electronic characterization of the capacitance imager.

4.2 Electronic Characterization Results

4.2.1 Pixel Performance

Voltage-Mode and Current-Mode Operation

Time-domain waveforms of a single reference pixel RO in the test-array, operating in voltage mode and current mode are shown in Figure 4.3. In voltage mode, the operating frequency is set to 5 MHz to show RO functionality in the lower frequency range, while in current mode, the operating frequency is set to 52 MHz. Ringing due to the package parasitics (bond-wire inductance) is seen in the voltage-mode screen capture and can be attenuated with appropriately adding series resistance to the output signal traces.



(a) (b)

Figure 4.3: Time-domain response of a single pixel operating in (a) voltage mode and (b) current mode.

Tuning Range

A select portion of the RO tuning range is presented in Figure 4.4. By setting V_{ref} from the off-chip source to 0.4 V or 0.64 V, and then enabling bias resistors R1-to-R8 one at a time, the bias current I_D of the RO is varied. A frequency range between 50 MHz and 140 MHz is achieved as measured at the output of the TIA when operating in current mode. The RO tuning curves are comparable to simulated results.

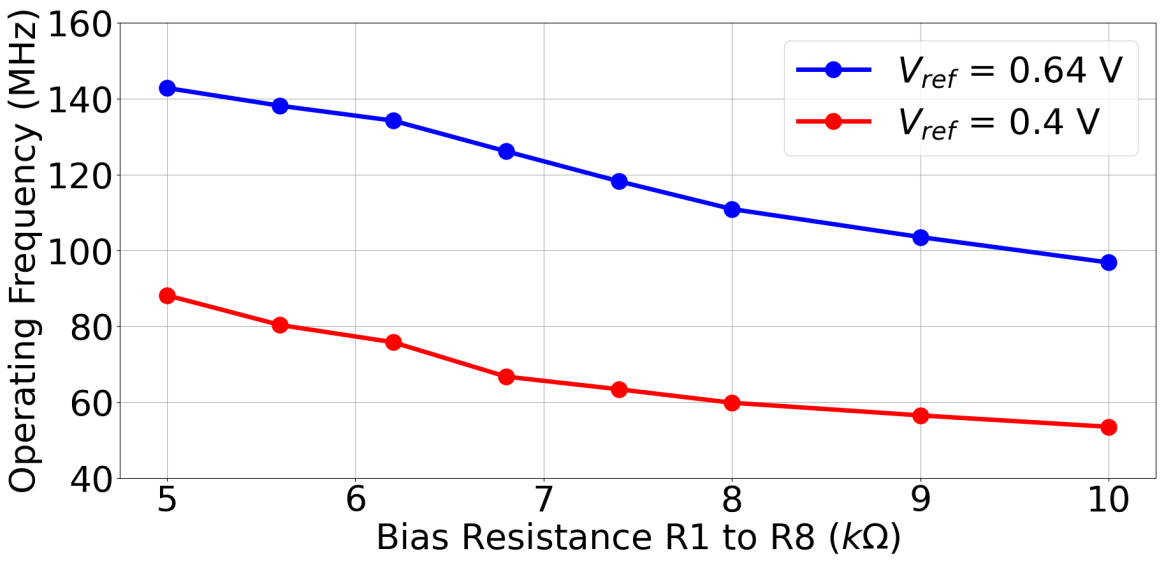


Figure 4.4: Ring oscillator tuning range.

Frequency Uncertainty

The SNR for our CFC-based sensor can be defined as

$$SNR = 20 \log_{10} \left(\frac{|\Delta f|}{\sigma_f} \right), \tag{4.1}$$

where $\Delta f = f_{op} - f_0$ (i.e., the change in the mean operating frequency from the unloaded operating frequency f_0, due to a change in C_{sen}, and σ_f is the standard deviation of f_{op}. Random frequency deviation of the RO output frequency due to noise, therefore, degrades the SNR of the sensor. To investigate the effect of frequency deviation on the performance, we measure the mean and σ_f of f_{op} from 1000 repeated measurements of the unloaded RO period, at f_{op} of 40 MHz, 80 MHz, and 160 MHz are measured. From the histograms shown in Figure 4.8, σ_f is measured to be 0.676 MHz, 1.662 MHz, and 3.871 MHz, at these frequencies respectively. The increase in σ_f with f_{op} was observed in simulation, however, the measured deviation is significantly higher. We aim to investigate this discrepancy in further detail in the future.

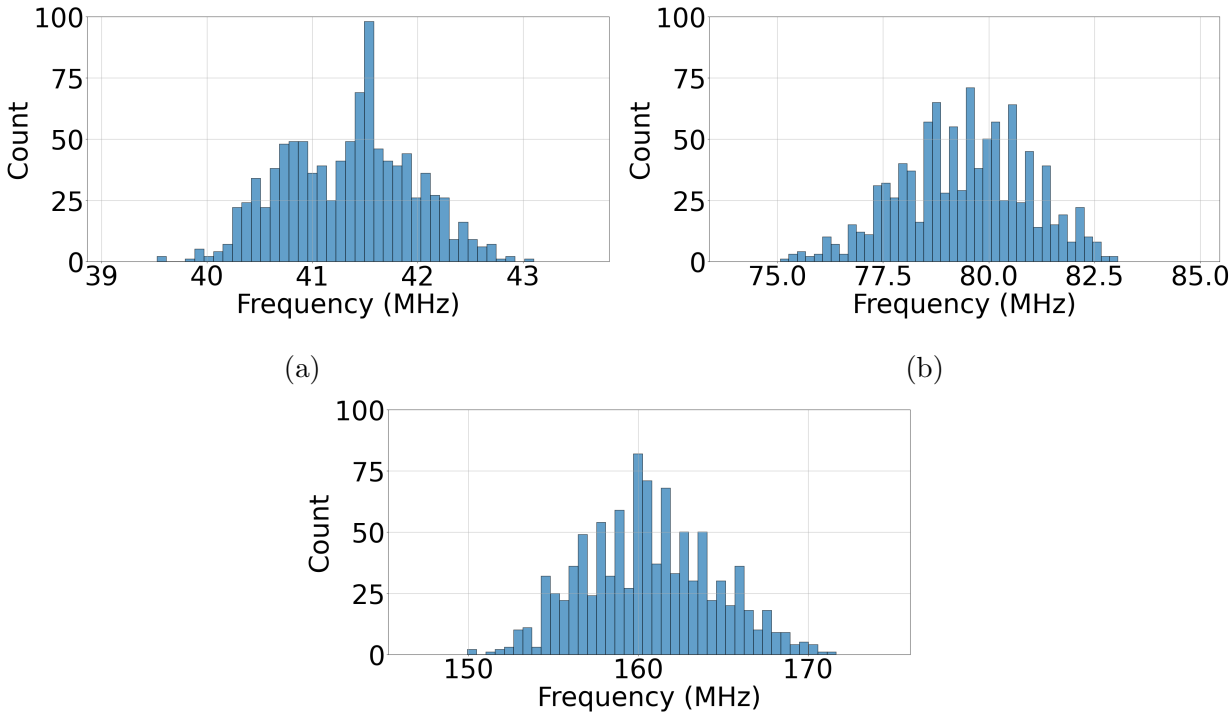


Figure 4.5: Frequency deviation of f_{op} at (a) 40 MHz (b) 80 MHz (c) 160 MHz.

4.2.2 Transfer Characteristics and Sensitivity

The transfer characteristic shows the change in f_{op} when C_{sen} is varied over a wide range. The sensitivity of test-array pixels is measured by employing the on-chip test network used to model changes in C_{sen} over a 10fF–170fF range. Capacitance $C_{L'}$ at the output of the second stage of a test pixel is estimated to be approximately 3 pF due to the presence of large interconnect parasitics between the pixel and test network.

Single Pixel Readout

The transfer characteristic of a single pixel operating in current mode is shown in Figure 4.6. The mean f_{op} is plotted for f_0 of approximately 40 MHz, 80 MHz, and 160 MHz. The sensitivity to changes in C_{sen} doubles with each doubling of f_0 as expected from the linear approximation of the transfer characteristic presented in Chapter 2. The measured sensitivity is approximately 4.5 times smaller than the simulated sensitivity at the same frequencies (as shown on page 39). We attribute this to the large interconnect parasitics between the pixel and the test network.

The SNR for each f_{op} over the capacitance range is displayed in Figure 4.7. Due to the increased sensitivity at higher frequencies, the SNR is expected to increase, however, the observed increase in frequency uncertainty σ_f limits the improvement. The limit of detection (LOD) defined as the smallest change in C_{sen} observed at an SNR = 0 dB is measured to be 57 fF at $f_0 = 40$ MHz, 70 fF at $f_0 = 80$ MHz, and 74 fF at $f_0 = 160$ MHz.

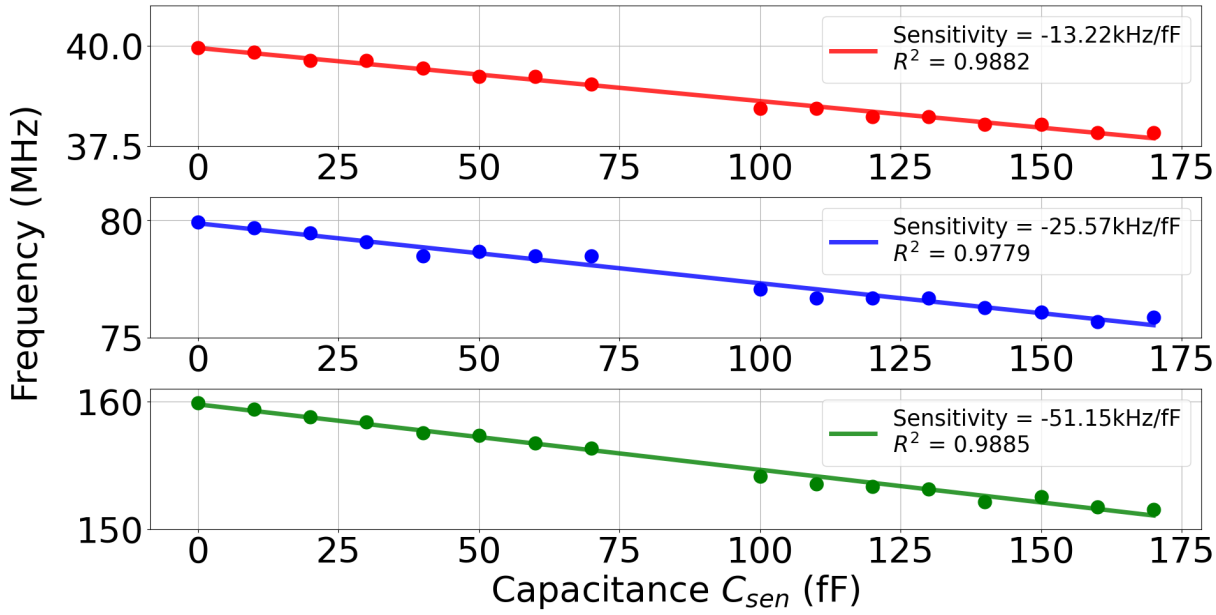


Figure 4.6: Transfer characteristic of a single pixel.

FDM Readout

To demonstrate FDM readout, one test-array pixel is operated at f_0 = 126 MHz, and a second pixel, in the same column, at f_0 = 117 MHz, while simultaneously varying the capacitance connected to each pixel. Figure 4.8(a) shows the ac-coupled time-domain waveform of the column bus signal measured at the output of the TIA, over a 2 μs period. The FFT in Figure 4.8(b) shows the frequency spectrum measured at the TIA output, where the RO frequency shift due to each capacitance change is clearly evident. Further, as shown in Figure 4.8(c), the sensitivity to changes in C_{sen} for both pixels is approximately the same, which is expected due to similar operating frequencies. Furthermore, for a fixed *FR*, FDM readout allows for longer signal averaging times compared to TDM readout, providing an SNR advantage.

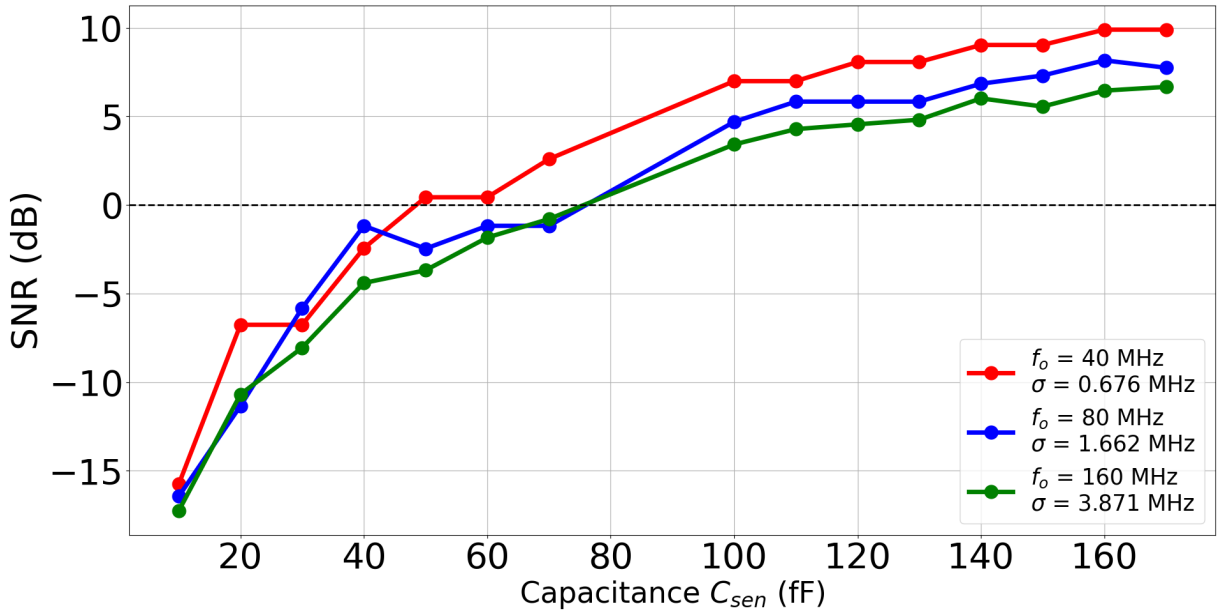


Figure 4.7: SNR of a single pixel for different f_0.

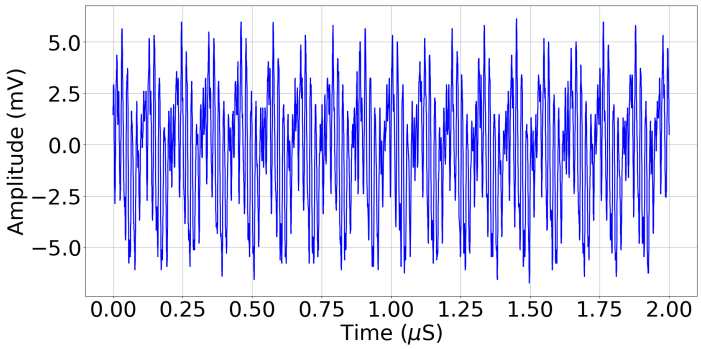
4.2.3 Performance Summary

Table 4.1 compares the measured results to simulation. The LOD of the sensor is relatively high due to low sensitivity to changes in C_{sen}. This is attributed to large parasitics between the test pixels and the test impedance network. Further, in the above calculations, the output frequency is averaged over 1000 repeated measurements. Increasing the number of samples, and therefore, the sampling time, will lower the LOD.

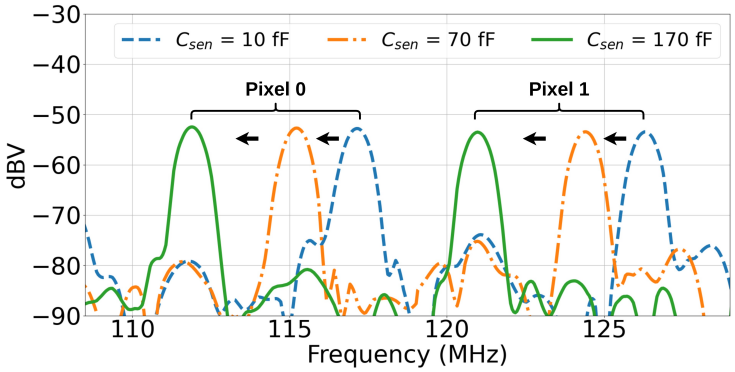
Table 4.2 compares the performance of our imager to several previously-reported CMOS electrochemical capacitance sensors. As shown in the table, our imager is the only one that provides both TDM and FDM readout. Our LOD is relatively high because we average only 1000 periods of the output signal, plus the large C_{par} in our test-array interface reduces f_{op} sensitivity.

Parameter	Simulated	Measured
Pixel Tuning Range	5 MHz–180 MHz	5 MHz–172 MHz
Readout Method	TDM & FDM	TDM & FDM
Power Consumption	-	90 mW (one active column)
Sensitivity (kHz/fF)*	-61.5 @ 40 MHz -116.56 @ 80 MHz -207.77 @ 160 MHz	-13.22 @ 40 MHz -25.57 @ 80 MHz -51.15 @ 160 MHz
Limit of Detection	-	57 fF @ 40 MHz 70 fF @ 80 MHz 74 fF @ 160 MHz

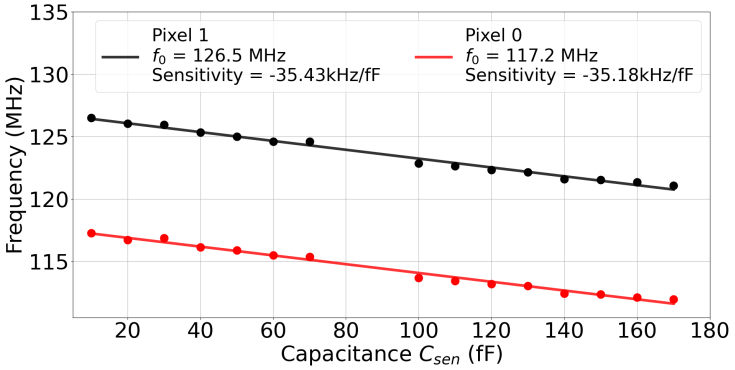
Table 4.1: Simulated and measured characterization results for the capacitance imager.



(a)



(b)



(c)

Figure 4.8: FDM operation with two active pixels. (a) Time-domain waveform, (b) output spectra, and (c) transfer characteristic for both pixels.

	[3]	[7]	[5]	[2]	**This Work**
Sensing Method	CFC	CBCM	CFC	CBCM	CFC
Technology	0.25 μm	0.18 μm	0.35 μm	90 nm	0.18 μm
Supply	2.5 V	3.3 V	3.3 V	1.2 V	1.8 V
Frequency Range	8 kHz–291 MHz	100 MHz	58 MHz–61 MHz	1 MHz–70 MHz	5 MHz–180 MHz
Readout Mode	TDM	TDM & CDM	TDM	TDM	TDM & FDM
Number of Pixels	2	131,072	16	65,536	420
Min Electrode Area (μm^2)	100 × 100	-	30 × 30	90 nm radius	2 × 2
Max Electrode Area (μm^2)	200 × 200	-	30 × 30	90 nm radius	200 × 200
Digitization	Off-chip	Off-chip	On-chip	On-chip	Off-chip
Die Area (mm^2)	-	3.9 × 6.4	3.0 × 3.0	3.2 × 2.1	3.0 × 2.5
Limit of Detection (averaging time)*	5 fF	0.7 aF (1 ms)	14.4 aF (1 s)	0.5-1 aF	57 fF (25 μs @ 40 MHz) 70 fF (12.5 μs @ 80 MHz) 74 fF (6.25 μs @ 160 MHz)
Power Consumption (mW)	29	-	-	15	90 (one active column)

Table 4.2: Performance comparison to previous work.

Chapter 5

Conclusion and Future Work

This thesis presented the design and electronic characterization results of a novel high-frequency CFC-based electrochemical capacitance imager, fabricated in a 0.18-μm CMOS process. The chip is capable of capacitive imaging beyond the EDL by operating at frequencies up to 180 MHz. Further, the design features FDM readout, which allows for either improved FR, or improved SNR at a given FR compared to standard TDM readout. We also aim to perform electrochemical characterization of the imager in the future. To the best of our knowledge, our work is the first to demonstrate CFC-based sensing with FDM readout.

5.1 Future Work

The list below highlights potential areas of improvement for future generations of the capacitance imager:

- The current version of the imager supports up to eight active pixels in a column. Scaling up the number of pixels in an array requires that the readout circuits operate over a wider bandwidth. It is therefore worth investigating alternative multiplexing techniques, such as code-division multiplexing (CDM).

- Our reported LOD is relatively high due to large parasitics between the test–array pixels and test–impedance networks. It would be beneficial therefore to implement an in-pixel test network to improve the sensitivity to changes in C_{sen} for better electronic characterization.

- Digitizing the output signal on-chip would be beneficial for a fully-integrated system.

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APPENDICES

Appendix A

Bonding Diagram and I/O Pin Descriptions

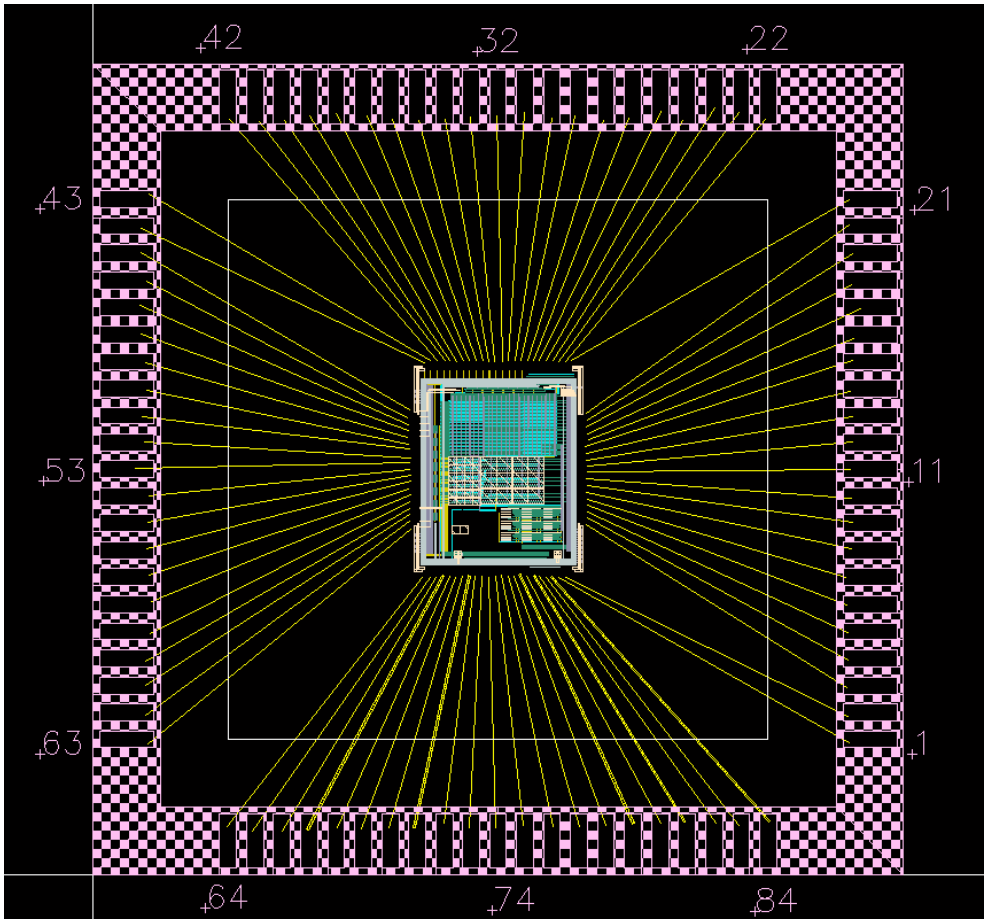

Figure A.1: Bonding diagram

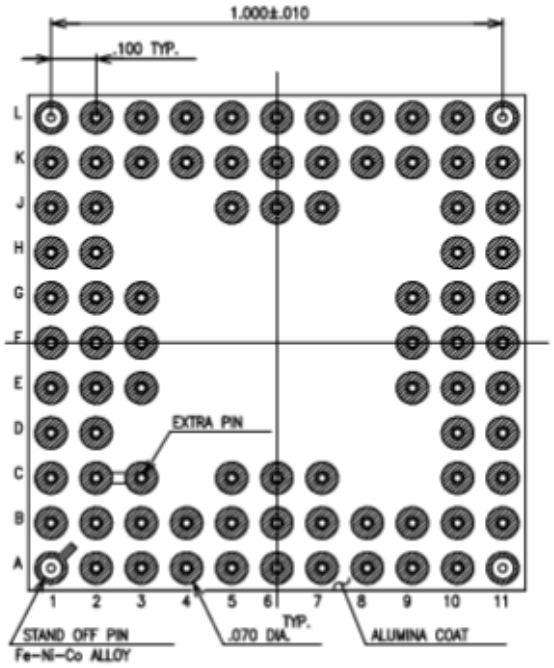

Figure A.2: CPGA-85 PCB footprint

The CPGA package shown in Figure A.2 displays the PCB footprint from the bottom up.

PIN	SIGNAL	I/O/PWR/GND	DESCRIPTION
1	dvss	GND	Digital Ground
2	dvss	GND	Digital Ground
3	dvss	GND	Digital Ground
4	dvss	GND	Digital Ground
5	dvss	GND	Digital Ground
6	dvss	GND	Digital Ground
7	dvss	GND	Digital Ground
8	dvss	GND	Digital Ground
9	dvss	GND	Digital Ground
10	dvss	GND	Digital Ground
11	dvdd	PWR	Digital Power 1.8 V
12	dvdd	PWR	Digital Power 1.8 V
13	dvdd	PWR	Digital Power 1.8 V
14	dvdd	PWR	Digital Power 1.8 V
15	dvdd	PWR	Digital Power 1.8 V
16	dvdd	PWR	Digital Power 1.8 V
17	dvdd	PWR	Digital Power 1.8 V
18	dvdd	PWR	Digital Power 1.8 V
19	dvdd	PWR	Digital Power 1.8 V
20	dvdd	PWR	Digital Power 1.8 V
21	buffer_out<7>	O	Voltage Buffer Output
22	buffer_out<6>	O	Voltage Buffer Output
23	buffer_out<5>	O	Voltage Buffer Output
24	buffer_out<4>	O	Voltage Buffer Output
25	buffer_out<3>	O	Voltage Buffer Output
26	buffer_out<2>	O	Voltage Buffer Output
27	buffer_out<1>	O	Voltage Buffer Output
28	buffer_out<0>	O	Voltage Buffer Output
29	tia_bypass<7>	O	Array Column Output (Bypass TIA/Buffer)
30	tia_bypass<6>	O	Array Column Output (Bypass TIA/Buffer)
31	tia_bypass<5>	O	Array Column Output (Bypass TIA/Buffer)
32	tia_bypass<4>	O	Array Column Output (Bypass TIA/Buffer)
33	tia_bypass<3>	O	Array Column Output (Bypass TIA/Buffer)
34	tia_bypass<2>	O	Array Column Output (Bypass TIA/Buffer)
35	tia_bypass<1>	O	Array Column Output (Bypass TIA/Buffer)
36	tia_bypass<0>	O	Array Column Output (Bypass TIA/Buffer)
37	tia<7>	O	TIA Output
38	tia<6>	O	TIA Output
39	tia<5>	O	TIA Output
40	tia<4>	O	TIA Output
41	tia<3>	O	TIA Output
42	tia<2>	O	TIA Output
43	tia<1>	O	TIA Output
44	tia<0>	O	TIA Output
45	tia_current_ctrl_test	I	Test TIA Tail Bias Current
46	tia_vcm_test	I	Test TIA Common Mode Voltage
47	tia_in_test	I	Test TIA Input

48	ota_v_neg	I	Test OTA Inverting Input
49	ota_v_pos	I	Test OTA Non-Inverting Input
50	avdd	PWR	Analog Power 1.8 V
51	avdd	PWR	Analog Power 1.8 V
52	avdd	PWR	Analog Power 1.8 V
53	avdd	PWR	Analog Power 1.8 V
54	avdd	PWR	Analog Power 1.8 V
55	avss	GND	Analog Ground
56	avss	GND	Analog Ground
57	avss	GND	Analog Ground
58	avss	GND	Analog Ground
59	avss	GND	Analog Ground
60	starve_ctrl_nmos	O	NMOS Gate Voltage for RO Bias Network
61	starve_ctrl_pmos	O	PMOS Gate Voltage for RO Bias Network
62	tia_out_test	O	Test TIA Output Voltage
63	ota_out_test	O	Test OTA Output Voltage
64	sc_bias_clk	I	Bias Scan Chain 128-bit Clock
65	sc_bias_rstn	I	Bias Scan Chain 128-bit Reset
66	sc_bias_data_in	I	Bias Scan Chain 128-bit Data
67	sc_arrays_clk	I	Array Control Scan Chain 128-bit Clock
68	sc_arrays_rstn	I	Array Control Scan Chain 128-bit Reset
69	sc_arrays_data_in	I	Array Control Scan Chain 128-bit Data
70	sc_eswitch_clk	I	Electrode Switch Scan Chain 64-bit Clock
71	sc_eswitch_rstn	I	Electrode Switch Scan Chain 64-bit Reset

72	sc_eswitch_data_in	I	Electrode Switch Scan Chain 64-bit Data
73	sc_bias_dout	O	Bias Scan Chain 128-bit Output
74	sc_arrays_dout	O	Array Control Scan Chain 128-bit Output
75	sc_eswitch_dout	O	Electrode Switch Scan Chain 64-bit Output
76	bangap_vref	I	Temperature Stabilized Input Voltage for RO Bias Network (0.3-0.9 V)
77	bias_amp_current_ctrl	I	RO Bias Network OTA Tail Current (0.8-1 V)
78	tia_current_ctrl	I	TIA Tail Current (1.2-1.8V)
79	pixel_current_ctrl_1	I	Pixel Current Control Voltage 1 (0.9-1.3V)
80	pixel_current_ctrl_2	I	Pixel Current Control Voltage 2
81	tia_vcm	I	TIA Common Mode Voltage (0.5-1.2 V)
82	OUTPUT_DEMUX_CTRL	I	Output Demultiplexer Control Voltage
83	OUTPUT_MUX_CTRL<0>	I	Output Multiplexer Control Voltage
84	OUTPUT_MUX_CTRL<1>	I	Output Multiplexer Control Voltage

Glossary

ADC Analog-to-Digital Converter 4, 15, 16

AFE Analog Front-End 4, 7, 11, 13, 16, 21, 27

CBCM Charge Based Capacitance Measurement 14

CDM Code-Division Multiplexing 22

CFC Capacitance-to-Frequency Converter 14, 15, 21, 23, 26, 69, 77

CMOS Complementary metal–oxide–semiconductor 1, 3, 6, 14, 16, 19–23, 60, 66, 73, 77

DNA Deoxyribonucleic acid 4

EDL Electrical Double Layer 8, 10, 11, 21, 23, 27, 62, 77

EIS Electrochemical Impedance Spectroscopy 9

FDM Frequency-Division Multiplexing 17, 19, 23, 27, 36, 64, 72, 77

ISFET Ion-sensitive field-effect transistor 21, 22

LOD Limit of Detection 21, 71, 73, 78

MOS Metal-Oxide-Semiconductor 21

PCB Printed Circuit Board 66

RO Ring Oscillator 14, 23, 26–33, 35–37, 40, 41, 49, 57, 61, 68–70, 72

SNR Signal-to-Noise Ratio 3, 18, 19, 21, 22, 47, 69–71, 77

TDM Time-Division Multiplexing 17–19, 22, 23, 64, 72, 77

TIA Transimpedance Amplifier 27, 40–43, 45–48, 59, 65, 69, 72