17 - 21 GHz Low-Noise Amplifier with Embedded Interference Rejection

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The ever-growing demand for high performance wireless connectivity has led to the development of fifth-generation (5G) wireless communication standards as well as satellite communication (Satcom). Both 5G wireless communications and Satcom use higher carrier frequencies than traditional standards such as 4G and WiFi. While the higher carrier frequencies allow for larger bandwidths and faster data rates, they come with the cost of high free-space path loss. This high loss necessitates the use of active phased array antennas, which can require hundreds of integrated circuits (ICs) designed in Complimentary Metal-Oxide Semiconductor (CMOS) processes. Furthermore, in a future world with ubiquitous 5G wireless base stations and Satcom users, it is conceivable that Satcom receivers can be jammed by high-power Satcom transmitters and 5G signals. Therefore, Satcom phased arrays must be designed for resilience against these sources of interference while supporting high data rates.

One of the key components in a Satcom receiver is the low-noise amplifier (LNA). It is responsible for amplifying the weak, noisy signal received from the satellite into a signal with sufficiently high signal-to-noise ratio for demodulation. One possible solution for making the phased array resilient to sources of interference is to embed filtering in the LNA.

This thesis presents two LNA designs that employ embedded filtering for resiliency to interference from 5G wireless signals and Satcom transmitters. First, the circuit-level specifications of a 17.7 - 21.2 GHz (K-band) LNA for satellite communication phased array beamformers are derived from the system requirements. Next, the LNA designs are presented. The first LNA is designed to have out-of-band filtering at 24-30 GHz, which corresponds to the bands containing both 5G and Satcom transmitter interferers. The second LNA is designed to have out-of-band filtering at 27-30 GHz, which addresses a different scenario where the Satcom transmitter is the sole source of interference. Both LNAs are implemented in the Global Foundries 130nm 8XP Silicon-Germanium Bipolar CMOS (SiGe BiCMOS) process. A novel transformer feedback notch is introduced that enhances the filtering capabilities of the amplifier. The full electromagnetic simulation of the first LNA shows a peak gain of 28.8 dB, a minimum noise figure of 1.85 dB, and and input 1 dB compression point (IP_{1dB}) greater than -17 dBm between 24 and 30 GHz. The second LNA shows a peak gain of 27.9 dB, a minimum noise figure of 1.78 dB, and an IP_{1dB} greater than -15 dBm between 27 and 30 GHz. Both LNAs meet specifications sufficient for a Satcom receiver at the same time as having resiliency to out-of-band interference sources.

Acknowledgements

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I would also like to thank my parents for their unwavering support, without which I would never have been able to focus on my education as much as I have. Finally, I would like to thank all the colleagues at the University of Waterloo in CIARS and in EmRG for their valuable advice and discussions.

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Chapter 1

Introduction

1.1 Motivation

The evolution of wireless communications infrastructure is a seemingly never-ending phenomenon in modern society. In 2009, the 4G Long Term Evolution (LTE) mobile communications standard was released. While 4G LTE technology has continued to develop since then, there has also been considerable development in the technologies for 5G millimeter-wave communications and satellite communications [14][3].

1.1.1 Satellite and 5G Communications

Satellite communications (Satcom) allow for widespread internet connectivity across the world in both urban and rural areas. Companies such as SpaceX, Amazon, OneWeb, and Viasat are all major contenders in the field and are deploying networks to enable this technology [15]. Satellite communications involve three main components: 1) a constellation of satellites orbiting the planet, 2) a gateway network on the ground that serves data from fiber connections over the air to satellites, and 3) user terminals on the ground that receive and transmit user data. This architecture is illustrated in Figure 1.1. The Satcom downlink is when the satellite transmits data to the user and the user receives. The uplink is when the user transmits to the receiving satellite. Satcom systems often use frequency-division duplexing (FDD), meaning both the uplink and downlink are operational at the same time, but use separate carrier frequency bands [3].

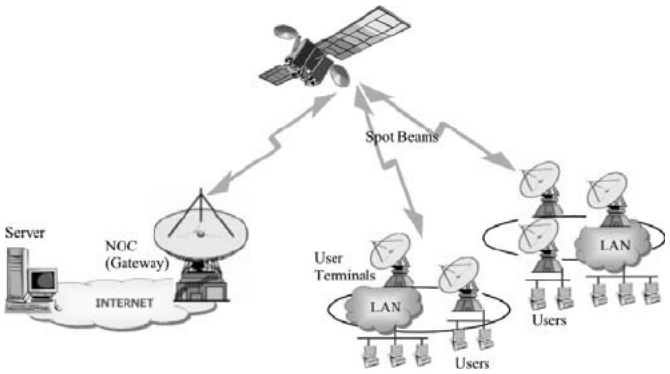


Figure 1.1: Satellite communications architecture [1].

In addition to satellite communications, future wireless communications will include 5G millimeter-wave (mm-wave) infrastructure. 5G mm-wave communications will involve a large number of base-stations in urban environments with small cell sizes on the order of 100 meters [14]. These "micro-cells" allow for gigabit data speeds to users, despite the high free-space path loss at millimeter wave frequencies.

The frequencies used for Satcom and 5G in the lower mm-wave frequencies are shown in Figure 1.2. Ku-band satcom uses the 10.7 - 12.75 GHz for the downlink, and 14 - 14.5 GHz for uplink [16]. K/Ka-band satcom uses 17.7 - 21.2 GHz for the downlink and 27.5 - 31 GHz for the uplink [4][17]. One of the 5G bands is 24.25 - 29.5 GHz, which overlaps with the Satcom Ka uplink band and is close to the K-band Satcom dowlink frequencies [14].

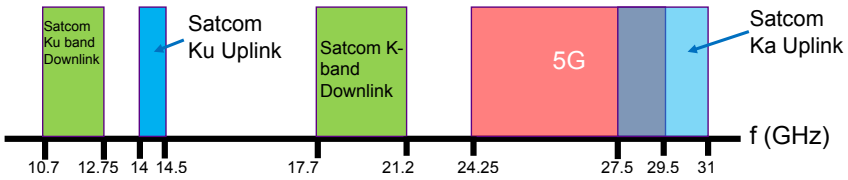


Figure 1.2: Low-millimeter wave frequency bands for Satcom and 5G communications (axis not to scale)

1.1.2 Phased Array Antennas

The Satcom bands shown in Figure 1.2 have relatively high atmospheric attenuation, which is a problem due to the long distance that Satcom signals travel between the satellite and

user terminal. Figure 1.3 shows the atmospheric attenuation vs. frequency and how it increases with frequency. Furthermore, high frequency signals inherently experience higher free-space path loss (FSPL) due to their smaller wavelength, which is shown in (1.1), where r is the distance, f is the frequency, and c is the speed of light. Therefore, conventional single-antenna designs used in relatively lower frequency wireless communications such as in 4G LTE are not suitable for Satcom systems.

$$FSPL = \left(\frac{4\pi r f}{c}\right)^2 \tag{1.1}$$

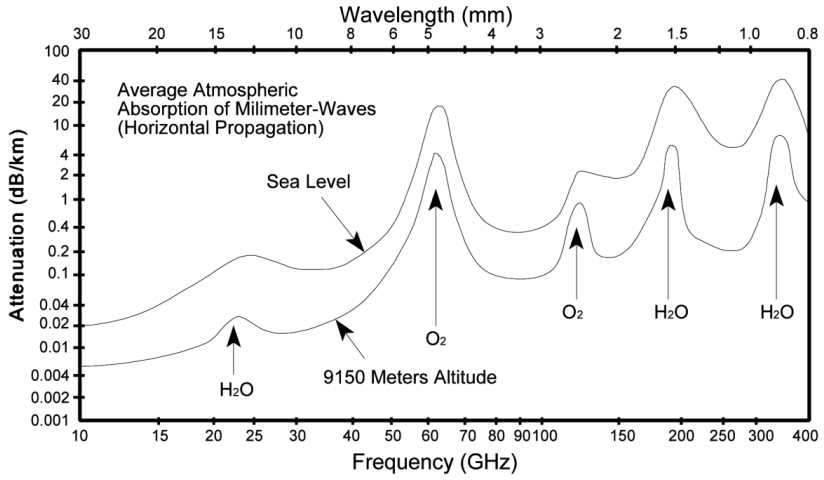
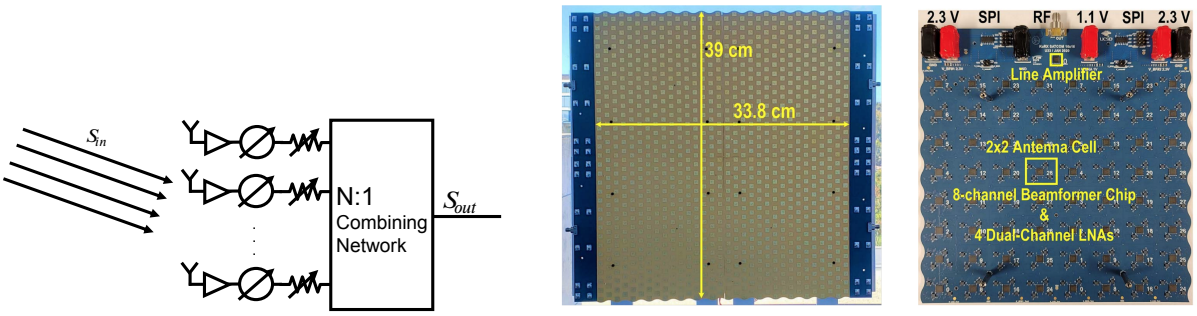


Figure 1.3: Atmospheric attenuation vs. frequency [2].

To overcome the high free space path loss, Satcom systems employ phased array antennas. A phased array antenna is any collection of antennas where each antenna transmits or receives the same signal but at different phases. Each antenna of a phased array requires its own transmitter or receiver chain that includes gain control and phase shifting components. Figure 1.4 shows an example of a receive phased array employing an RF beamforming architecture, with Figure 1.4a showing the conceptual block diagram and Figure 1.4b showing an example array implementation. The block diagram shows how the array consists of a collection of elements, each connected to a receiver that has a gain stage, a phase shifter, and a variable attenuator. All of these paths are combined into an output signal, which is then connected to a demodulator (not shown). As shown in Figure 1.4b, an example implementation of this architecture is to use PCB-based patch antennas as

the antenna elements, and beamformer integrated circuits (ICs) that contain the receiver chains. The phase shifter allows a different delay to be added to each path, which allows the direction of reception to be steered, known as "beam-steering."



(a) (b)

Figure 1.4: A phased array receiver. (a). Conceptual block diagram. (b) An example phased array receiver [3].

Phased arrays overcome high free space path loss and atmospheric attenuation by way of power combining. In the receiver, when the signals from all the paths are combined, the signal adds constructively while the noise power, since it is uncorrelated between each path, stays the same at the output. Therefore, phased arrays see a N-fold factor increase in signal-to-noise (SNR) ratio compared to conventional antennas. The tradeoff is that as more elements are added to the array, the array becomes more directive. Conceptually, higher directivity means it is able to receive more radiation power, but the area in the far-field from which it receives that power becomes narrower (i.e. the beam becomes narrower) [18]. In order for the array to transmit or receive signals from multiple directions, it needs a phase shifter for each antenna element, which is often part of the beamformer ICs such as in Figure 1.4.

The high directivity of phased arrays make them suitable for millimeter wave communications. Since, as shown in Figure 1.4, phased arrays receiver require electronics for each array element, the design of the electronics and beamformers of phased arrays is an interesting problem. The design of these electronics is the topic of this thesis.

1.2 Problem Statement

With the improvements in silicon CMOS and SiGe technologies for radio-frequency (RF) and millimeter wave applications over the last two decades, it is becoming increasingly attractive to implement phased array beamformers using integrated circuits (ICs) manufactured with these processes. The high integration level, high yield, and low cost of silicon technologies allows for the mass production of low-cost phased array antennas for satellite communications (Satcom). Therefore, it is of utmost importance to explore the design of high-performance, low-cost silicon-based receiver beamformer ICs for satellite communication phased arrays.

In the future, it is expected that 5G millimeter wave base stations will serve high speed, high bandwidth data to users in urban areas. At the same time, satellite communications will also provide service to users worldwide, in both rural and urban areas. It is possible that strong 5G wireless signals can pose as a source of interference for Satcom receivers, which must receive a weak signal from a far-away satellite. Furthermore, in a realistic Satcom user terminal, a transmitter and a receiver are placed side by side and operate at the same time, leaving the possibility for the transmitter to also jam the receiver. Thus, a high-performance Satcom beamformer receiver must include resilience to these sources of interference.

The purpose of this work is to design a low-noise amplifier (LNA) for a Satcom user terminal beamformer receiver operating at 17.7 - 21.2 GHz. The LNA should include built-in filtering of out-of-band signals. The LNA will be designed in the GlobalFoundries 130nm (SiGe) Bipolar CMOS (BiCMOS) 8XP process. This process is a suitable technology for RF and millimeter wave ICs due to its high oscillation frequency (f_{max}) of 320 GHz and low minimum noise figure [19]. The work includes novelty in that, to the author's best knowledge, there is no prior work on Satcom LNAs designed specifically to reject 5G signals. In addition, a novel circuit topology is introduced in the LNA to improve its out-of-band rejection. In brief, the purpose of this work is to demonstrate the feasibility of using silicon processes for the design of interference rejecting LNAs that can be used for Satcom receivers.

1.3 Thesis Organization

This thesis is organized as follows. Firstly, Chapter 2 presents a review of existing design techniques for LNAs, including filtering techniques. Chapter 3 focuses on the system

analysis for Satcom phased arrays and LNAs. This chapter derives the specifications for an LNA that is suitable for a Satcom receive phased array. It also includes and analysis of the power level of 5G interference sources and transmitter self-interference signals on the Satcom receiver. This analysis is used to derive specifications for the interference resiliency of the LNA. Next, Chapter 4 focuses on the design of two LNAs with out-of-band interference rejection. The first design includes rejection of both 5G wireless and Satcom self-interference sources. The second design only includes resiliency to self-interference. The design procedure of the amplifier and the simulation results are presented. Chapter 5 shows some measurement results of Design 1, but the results are inconclusive due to a circuit layout issue. Finally, chapter 6 provides concluding remarks and proposes some future work that can be done based on the work in this thesis.

Chapter 2

Background and Literature Review

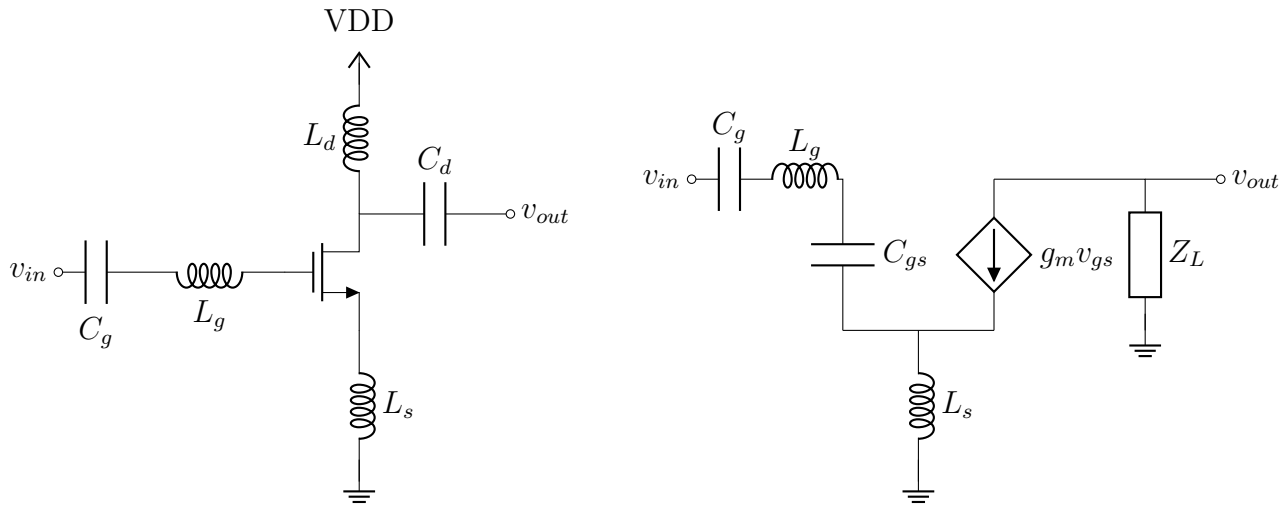
This chapter presents a review of LNA design techniques in CMOS and SiGe processes. Common LNA topologies such as the common-source and cascode amplifier are reviewed. Next, existing filtering techniques for phased arrays and embedded LNA filters are reviewed.

2.1 LNA Design Without Filtering

Before reviewing filtering techniques, it is prudent to review typical LNA performance that can be achieved without filtering. The performance achieved by such LNAs, including out-of-band gain and linearity, can be used to estimate the amount of modification required to meet the filtering specifications derived in Section 3.2.8.

2.1.1 Common-source LNA

The simplest LNA topology is a common-source amplifier with inductive degeneration and a series inductor at the gate of the input transistor. Figure 2.1a shows the schematic of this topology. The small signal equivalent is of the amplifier is also shown in 2.1b.



(a) Common source LNA.

(b) Small signal equivalent.

Figure 2.1: Common source LNA and its small signal equivalent circuit.

In the design of the common-source LNA, the transistor can be sized such that the real part of the optimal source impedance Z_{s-opt} is equal to the source impedance, 50 Ω [20, p. 443]. The input impedance of the LNA can be shown to be given by (2.1). The degeneration inductor, L_s, can be selected such that the real part of Z_{in} equals 50 Ω, while the gate inductor L_g can be selected to resonate with the capacitance C_{gs} at the intended center frequency of the LNA.

$$Z_{in} = \frac{1}{sC_{gs}} + sL_g + sL_s + g_m\frac{L_s}{C_{gs}}. \tag{2.1}$$

Assuming ideal inductors, the voltage gain of the common source stage at the center frequency, when both the input and output impedances are at resonance, is given by (2.2), where R_p is the equivalent parallel resistance of the load and R_s is the signal source impedance [21, p. 204] For ideal inductors and capacitors, $R_p = r_0$, where r_0 is the output resistance of the transistor due to channel-length modulation.

$$A_v = |\frac{v_{sig}}{v_{in}}| = \frac{1}{2}\frac{\omega_T}{\omega_0}\frac{R_p}{R_s}. \tag{2.2}$$

The single-transistor common-source LNA is the lowest noise topology for an LNA,

because the only noise sources are one transistor and the parasitic resistances of the passive components. The noise figure of the common-source topology is given by 2.3, where R_{source} represents the impedance of the source driving the LNA (typically 50 Ω), ω_0 is the center frequency of the matching network, and ω_T is the unity gain frequency of the transistor [21, p. 204].

$$F_{CS} = 1 + g_m R_{source} \gamma \left(\frac{\omega_0}{\omega_T} \right)^2 . \tag{2.3}$$

The common-source topology has been successfully used to implement a K-band LNA in [22], where three such common-source stages were cascaded in a 45-nm silicon-on-insulator (SOI) process. The design achieved 23 dB of gain, a minimum of 1.6 dB noise figure in-band, and an IP_{1dB} greater than -15 dBm from 24 - 30 GHz.

While [22] shows that the out-of-band linearity requirement derived in Section 3.2.8 can be satisfied with only common-source stages, a number of problems remain with the simple common-source design. For one, the out-of-band small-signal rejection is not sufficient to meet the specification. In [22], the amplifier only has 8 dB less gain at 24 GHz than at the center frequency. The low rejection indicates that an interference-rejecting LNA should use additional techniques in order to achieve both the linearity and small-signal rejection specifications.

Another problem with the common-source stage is that it can exhibit instability due to its inductive load and the feedback capacitance C_{gd}. Figure 2.2 shows the small signal equivalent of a common-source LNA including C_{gd}. Assuming L_s is small and Z_L is inductive ($Z_L = sL_L$), the input impedance can be approximated as (2.4) [20, p. 406]. This equation shows that the input impedance of the CS LNA for small L_s is negative, which can lead to oscillations. Making L_s sufficiently large adds a real term to the input impedance, which stabilizes the effect of $C_g d$.

$$Z_{in} \approx \frac{-1}{\omega^2 g_m C_{gd} L_L}. \tag{2.4}$$

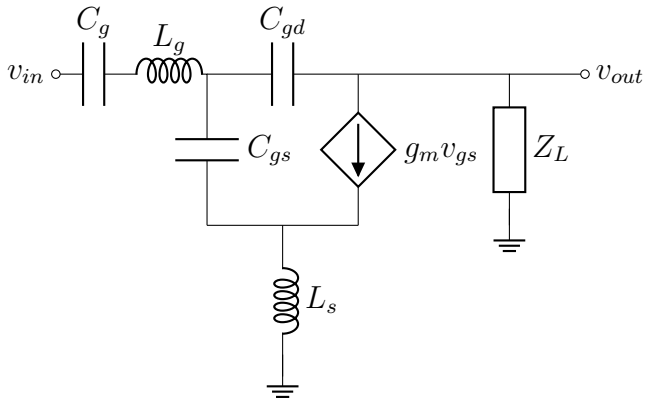


Figure 2.2: Small signal equivalent of a common-source LNA with C_{gd}.

2.1.2 Cascode LNA

Figure 2.3 shows the schematic of a cascode LNA. Similarly to the common source LNA, it uses a series inductor L_g and a degeneration inductor L_s to accomplish simultaneous noise and conjugate matching at the input. The amplifier consists of a common-source transistor M_1, and a common-gate, cascode transistor M_2. The parasitic capacitances at the drain of M_1 are represented by an equivalent capacitance C_X, where C_X is approximately given by $C_{gd1} + C_{db1} + C_{sb1} + C_{gs2}$.

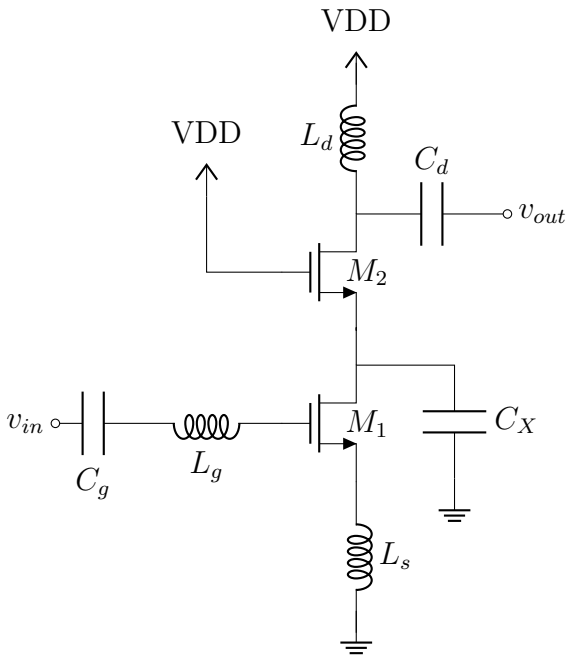


Figure 2.3: Cascode LNA schematic.

The noise figure of the cascode LNA is given by 2.5 [21]. Compared to 2.3, it is clear that the cascode transistor adds a second term to the noise figure. However, the advantage in using the cascode LNA is that it mitigates the effect of C_{gd1}, preventing a negative input resistance from arising due to the load of M_1.

$$F_{cas} = 1 + g_m R_{source}\gamma \left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{\gamma}{g_{m2}R_{source}} \left(\frac{2L_g\omega_0}{g_{m2}}\right)^2 \left(\frac{1 + sr_{o1}C_X}{1 + s\frac{C_X}{g_{m2}}}\right)^2. \tag{2.5}$$

2.2 A Review of Out-of-Band Filtering Techniques

There are a number of filtering techniques that can be used for phased array receivers. Broadly speaking, these techniques can be classified as either passive or active. The passive techniques include off-chip filtering, single LC notches, multiple distributed LC notches, and transformer-based notches. The active techniques include using frequency-dependent feedback networks and negative resistance generators. This section will review

these techniques and the results that have been achieved with them in CMOS and BiCMOS technologies.

2.2.1 Passive Filtering Techniques

Off-Chip Filtering

One method of achieving out-of-band in a Satcom LNA is to implement the filtering on the printed circuit board (PCB) that contains the beamformer chips. In [4], the authors implemented a 1024-element K-band receive phased array for Satcom applications. The out-of-band filtering was achieved through the antenna matching network and a notch filter, both of which are implemented on the PCB. The block diagram of the antennas, LNAs, and one beamformer in the array is shown in Figure 2.4. The antenna and matching network were both implemented on the PCB. The LNAs were implemented on separate ICs, and were followed by a PCB-level LC notch filter. Finally, the 8 receive channels went into the beamformer inputs.

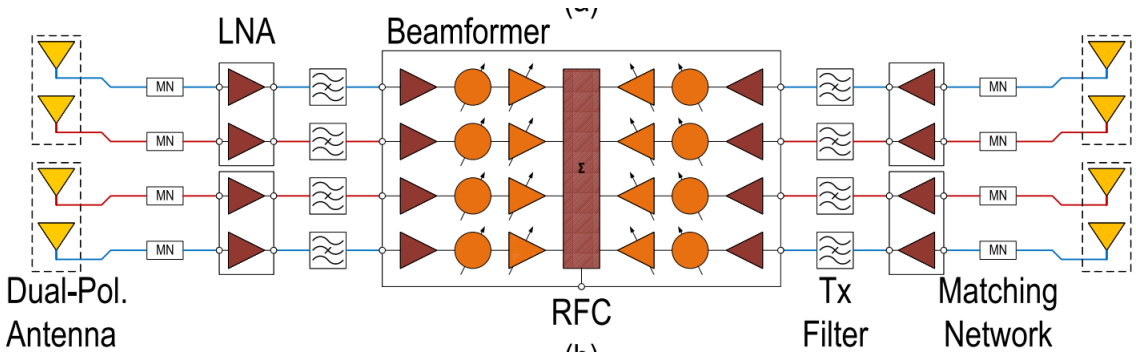


Figure 2.4: Block diagram of the beamformer and its connections from [4].

The filtering techniques used in [4] are highly effective at attenuating the transmit self-interference at 27-30 GHz. The antenna response and matching network attenuate the blocker power of -20 dBm to -60 dBm, preventing the LNA from saturating. The filtering after the LNA gives an effective LNA gain of 7 dB at 27 GHz, leading to an out-of-band input power of -53 dBm at the input of the beamformer. Both the input powers are far from the out-of-band IP_{1dB} points of the LNA and beamformer (-20 and -30 dBm respectively).

While the technique of filtering on the PCB adds sufficient resiliency to out-of-band blockers, it has some disadvantages. Firstly, the matching network on the PCB adds a loss

of about 1.2 dB, which directly impacts the noise figure of each receiver chain. Furthermore, this architecture requires a discrete LNA and a discrete beamformer in order to implement the on-PCB notch filter. Having separate ICs for the LNA increases component cost and complexity compared to a solution where the LNA and beamformer are integrated onto one die.

Single LC Notch

One simple technique for embedding filtering in an LNA on-chip is to add a single notch filter consisting of an inductor and a capacitor. For example, in [5], a shunt LC notch is placed at the drain of the common-source device of a cascode amplifier, as shown in Figure 2.5. The frequency of the notch is given by

$$\omega = \frac{1}{\sqrt{L_2(C_1 + C_2)}}. \tag{2.6}$$

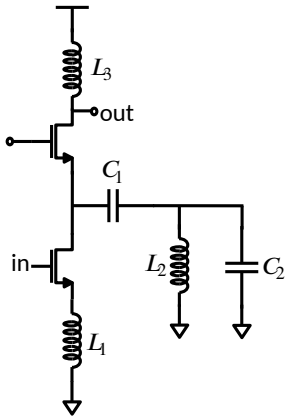


Figure 2.5: Shunt LC notch used in [5]

The shunt LC notch shown in Figure 2.5 is suitable for narrow-band rejection of a blocker. In [5], it is used in a 5-GHz wireless local area network (WLAN) receiver as an image-rejection filter. As another example, it is used in [23] but in a differential topology, where the filter serves to reject the 1.77 GHz image of a 1.55 GHz signal.

[6] presents another topology that achieves a single notch in the frequency response. The topology is shown in Figure 2.6. The degeneration inductor of the cascode LNA stage

is replaced with a transformer, where the secondary coil forms a resonator between L_2 and C_{var}. Using a varactor as the resonator capacitor allows the notch frequency to be tuned. In [6], the notch was used as an image-reject filter for a 5-GHz receiver, and the tunability meant that the center frequency of the signal could be changed and the notch re-tuned to the new image frequency.

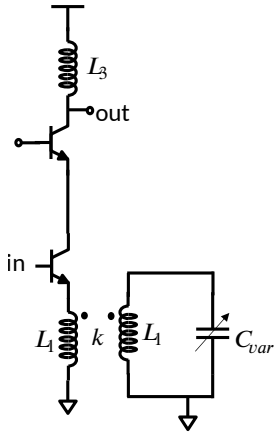


Figure 2.6: Degeneration Transformer LC notch used in [6]

A single notch can also be placed at the input of the LNA, as done in [7]. The conceptual schematic of the filtering LNA is shown in Figure 2.7. The parallel resonance of L_1 and C_2 forms a high impedance in the stop-band, which attenuates signals at the blocker frequency and results in low small-signal gain in the stop-band. The work in [7] achieved over 30 dB of small-signal rejection at 30 GHz, where the LNA was designed to amplify signals at 20 GHz. In addition, it showed tolerance to a blocker power of -13 dBm at 30 GHz without compromising in-band linearity.

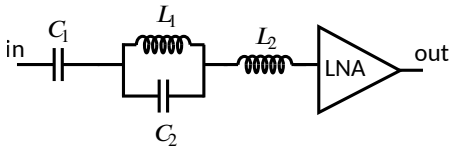


Figure 2.7: Parallel LC notch used at the input of an amplifier, as in [7].

Single LC notches are a simple way of rejecting a blocker at a single frequency, which is why they were used for image rejection in [5], [6], and [23]. However, they are inherently narrow-band because the LC resonator only presents a short or open at one frequency. In

addition, like with all passive notches, the amount of filtering rejection is limited by the low quality factor of on-chip spiral inductors, which is generally between 10 and 30 for modern CMOS processes with thick metal layers [20]. Also, the extra inductor increases the circuit area.

A 3-coil Inter-Stage Transformer Notch

The transformer-based notch presented in [6] can be used in other locations within an LNA besides the first-stage degeneration. In [8], the authors used a 3-coil inter-stage transformer to implement a notch filter in the inter-stage matching network of a 2-stage LNA designed in a 65-nm CMOS process. The LNA was designed to amplify Satcom signals from 10.7 - 12.7 GHz (Ku-band) and to attenuate the corresponding transmit band at 14 - 14.5 GHz. The LNA consists of two amplifier stages. The inter-stage matching of the LNA from is implemented using a 3-coil transformer. The schematic of the transformer is shown in Figure 2.8a. An approximate equivalent circuit of the 3-coil network is shown in Figure 2.8b, for which the component values are given by equations (2.7) - (2.10). The equivalent components L_{14} and C_3' form a series-parallel notch that blocks the first stage current from developing a voltage across the inter-stage transformer formed by L_{12} and L_2, causing a zero in the transfer function. The frequency of this notch is given by (2.11).

(a) (b)

Figure 2.8: The 3-coil transformer from [8]. (a) Transformer schematic. (b) Equivalent circuit.

$$L_{14} = k_{13}^2 L_1. \tag{2.7}$$

$$C_3' = \frac{L_3}{k_{13}^2 L_1} C_3. \tag{2.8}$$

$$L'_{12} = (1 - k_{13}^2)L_1. \tag{2.9}$$

$$k''_{12} = \frac{k_{12}}{1 - k_{13}^2}. \tag{2.10}$$

$$\omega_{notch} = \frac{1}{\sqrt{L_{14}C'_3}} = \frac{1}{\sqrt{L_3C_3}}. \tag{2.11}$$

Since the 3-coil transformer-based notch is another type of single LC filtering technique, it suffers from the same aforementioned disadvantages. However, this technique has the advantage of being more compact with proper layout of the tertiary coil.

Distributed Notch Filtering

The single LC passive techniques described in the previous sections are narrow-band. One way to widen the bandwidth of the filtering is to simply add more notches in the circuit.

In [9], a 20 GHz Satcom LNA with out-of-band filtering at 27.5-31 GHz is designed. The schematic of the amplifier is shown in Figure 2.9. The filtering is achieved using 4 notches that are distributed throughout the 2-stage amplifier. The amplifier was implemented in a 0.25μm SiGe BiCMOS process, and consumes 92 mW from a 2.5 V supply. The amplifier achieved over 30 dB of small signal rejection with respect to its peak gain in the stop-band of 27.5 - 31 GHz. Due to the distributed nature of the notches, the rejection is wideband, as the resonant frequency of each notch is tuned to a slightly different frequency within the stop-band.

The authors in [9] also compared the filtering LNA to a reference design without filtering. The addition of the filtering reduced the in-band gain by a 2-3 dB and increased the noise figure by 0.2 dB. This degradation in noise figure is mainly due to the additional loss caused by the two notches in the first stage. Furthermore, due to the presence of two notches within the first stage, one before the input transistor Q_1 and another before the cascode transistor Q_2, the $\text{IP}_{1\text{dB}}$ of the filtering LNA is 20 dB higher than the non-filtering one. The out-of-band $\text{IP}_{1\text{dB}}$ in the LNA without filtering is already -10 dBm, exceeding the specification derived in Section 3.2.8, which can be attributed to the large devices chosen and their high power consumption.

Overall, the distributed notches as implemented in [9] illustrate the trade-off between

high rejection and noise figure, as well the trade-off between power consumption and linearity.

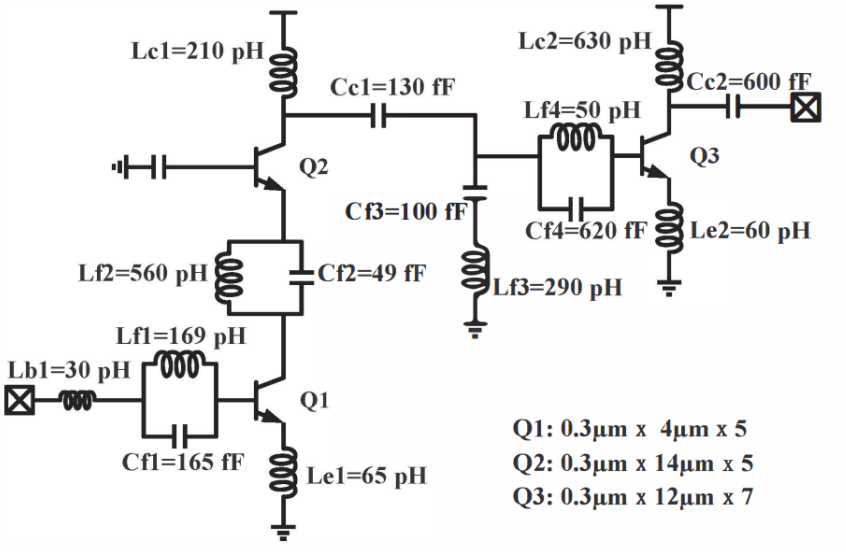


Figure 2.9: Schematic of the filtering LNA designed in [9].

Another example of distributed notch filtering is in [10], where a wideband 24-43 GHz LNA for 5G applications is designed with rejection at 10-15 GHz. The schematic of the LNA is shown in Figure 2.10. The LNA implements its out-of-band filtering with three shunt-series LC notches formed by the resonances of L_1 with C_2, L_2 with C_4, and L_3 with C_6. These resonances allow for greater than 60 dB of out-of-band small-signal rejection, and an out-of-band IIP_3 20 dB greater than the in-band $IIP3_3$.

The LNA in [10] also illustrates a trade-off between out-of-band filtering and power consumption. The amplifier has 3 stages and 17-20 dB of gain, at a power consumption of 20.5 mW. However, a similar wideband LNA in the same CMOS process has been implemented with only 2 stages and 17 mW of power consumption, with approximately 1 dB lower noise figure [24]. The additional power consumption and higher noise figure in [10] can be attributed to the losses of the filtering elements.

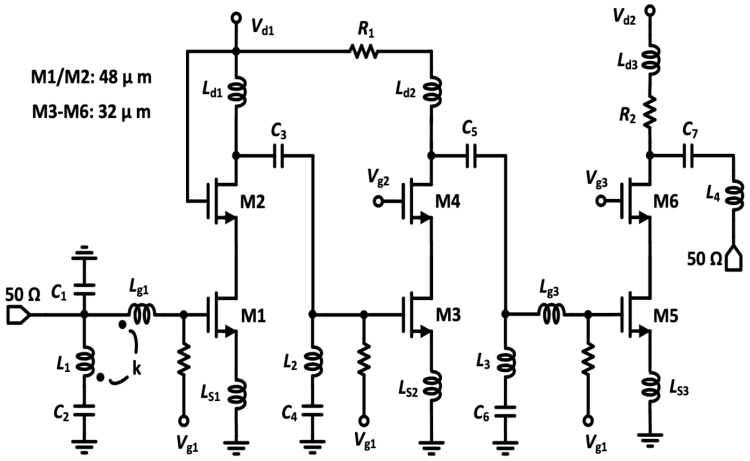


Figure 2.10: Schematic of the wideband LNA in [10] that implements distributed notch filtering.

In summary, both examples in this section have shown that while distributed filtering can achieve high stop-band rejection, the trade-offs include power consumption, noise figure, and additional chip area.

2.2.2 Active Filtering Techniques

The on-chip passive filtering techniques shown in Section 2.2.1 are limited by the low quality factor (Q) of on-chip spiral inductors and transformers. Active techniques can be used to improve the effective quality factor of the notch and thus obtain a higher filtering rejection.

A Feedback Active Notch

One of the earliest occurrences of active filtering in a monolithic LNA is in [11], where an active notch and feedback are used to enhance the quality factor of a notch in a cascode LNA. The schematic of the active filter is shown in Figure 2.11a. The input impedance, Z_{in}, is given by (2.13)[11], where R_{ind} represents the parasitic series resistance of the inductor, r_b represents the parasitic base resistance, C_π is the base-emitter capacitance of Q_2, and g_{m2} is the small-signal transconductance of Q_2. The last term in (2.13) is negative, which

shows how the addition of Q_2 can compensate for the resistances R_{ind} and r_b and effectively improve the Q of the notch.

The quality factor of the notch can further be improved by adding feedback. The concept of this feedback is shown in Figure 2.11b, for which the transfer function is given by

$$H(s) = \frac{v_{out}}{v_{in}} = \frac{1}{1 + B(s)}. \tag{2.12}$$

[11] shows that if the feedback transfer function, $B(s)$, has a pole at ω_0, the closed loop transfer function, $H(s)$, has a very low gain at that frequency. This low gain results in a notch behaviour in $H(s)$.

$$Z_{in} = j\omega L_2 + R_{ind} + \frac{1}{j\omega}\left(\frac{1}{C_\pi} + \frac{1}{C_1}\right) + r_b - \frac{g_{m2}}{\omega^2 C_\pi C_1}. \tag{2.13}$$

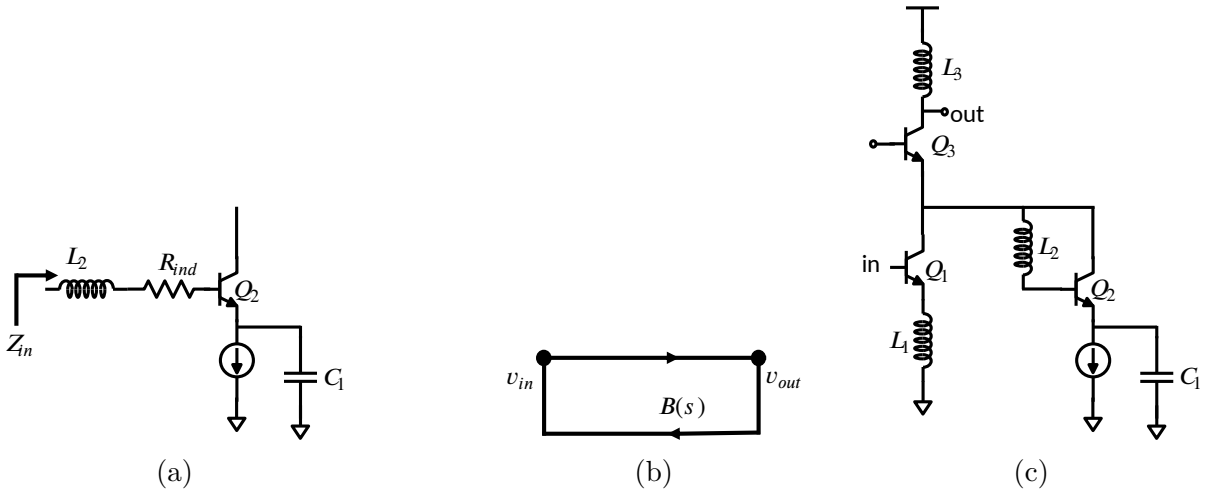


Figure 2.11: Circuit topologies for the LNA with a feedback notch, introduced in [11]. (a) Active notch schematic. (b) Feedback notch block diagram. (c) LNA schematic with an active notch and feedback.

The feedback shown in Figure 2.11b was applied to the active notch in Figure 2.11a to improve its rejection, and embedded in an LNA. The resultant circuit is shown in Figure 2.11c [11]. The circuit topology can be thought of as an active version of the one in Figure

2.5, because the notch is an active shunt LC at the collector of Q_1, similar to the passive shunt LC at the drain of the common-source device in Figure 2.5.

The active feedback technique shown in Figure 2.11 has been used in numerous image-rejecting CMOS/SiGe receivers in the 2-5 GHz range [11][25][26]. The technique without feedback (i.e. Figure 2.11a only) was also applied to an ultra wideband receiver operating between 3.1 and 10.6 GHz in [27] as a means to reject WLAN blockers at 5 GHz.

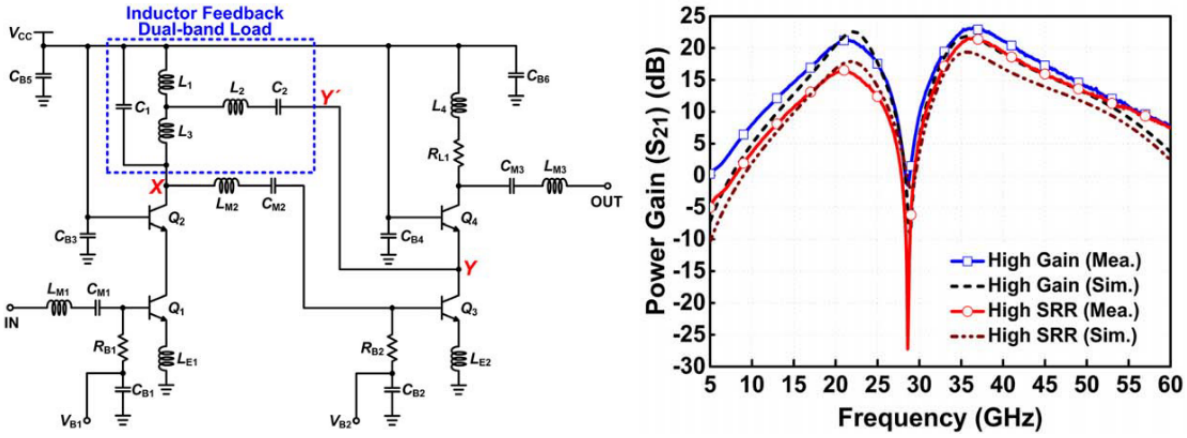
The feedback topology in Figure 2.11c trades off filtering for noise figure, depending on the sizing and biasing of Q_3. It also increase power consumption due to the addition of Q_2. Finally, it must be carefully designed to avoid instability in the feedback loop.

An Inter-Stage Feedback Notch

The concept of using frequency-dependent feedback to introduce a notch into the transfer function can be extended to a multi-stage amplifier. In [12], LC feedback is added between two amplifier stages to achieve a notch response in a dual-band LNA. The schematic and performance of the amplifier are shown in Figure 2.12.

The LNA from [12] is designed for two pass-bands, at approximately 20 and 37 GHz. In between the two pass bands, the amplifier exhibits a notch at 28 GHz in order to reject 5G blockers from that band. The notch is achieved by the feed-forward path formed by L_2 and C_2 to Q_3, shown in the schematic in Figure 2.12a. The frequency of the zero is given by (2.14). At ω_z, the load impedance seen from the collector of Q_3 is small, leading to a low stop-band gain. This can alternatively be understood as the stop-band current feeding forward through L_2 and C_2 and supplying all the stop-band current that the transconductor of Q_3 is sinking. As a result, no stop-band current flows through Q_4, leading to a low gain at the stop-band.

$$\omega_z = \sqrt{\frac{1}{L_2 + \frac{L_1 L_3}{L_1 + L_3} C_3}}. \tag{2.14}$$



(a) Schematic.

(b) Small signal gain.

Figure 2.12: Schematic and gain of the active feedforward notch LNA from [12]

The plot of the gain of the amplifier is shown in Figure 2.12b. The gain exhibits a sharp zero in the frequency response at the notch frequency, and a dual-band response otherwise. By changing the bias voltage of Q_3, gain and stop-band rejection can be traded off, shown by the red vs. blue curves in Figure 2.12b. While this feed-forward notch technique is able to achieve > 40 dB rejection at a pass band, it is relatively narrow-band. The stop-band current only cancels at one frequency at the collector of Q_3, leading to the narrow-band response. In addition, the additional components (L_2 and C_2) and routing needed to implement the feed-forward path increase the area cost of this solution.

Cross-Coupled Differential Pair Negative Resistance

The active notch technique shown in Figure 2.11a improves the quality factor of the notch by the negative resistance introduced by Q_2, as shown in (2.13). Another common technique of generating a negative resistance to improve notch quality factor that has been used in numerous works [8][5][23] is to use a cross-coupled differential pair. The generalized circuit schematic is shown in Figure 2.13. The cross coupled differential pair consisting of M_1 and M_2 form a positive feedback system with input resistance given by

$$R_{in} = -\frac{2}{g_m}, \tag{2.15}$$

where g_m is the transconductance of M_1 and M_2.

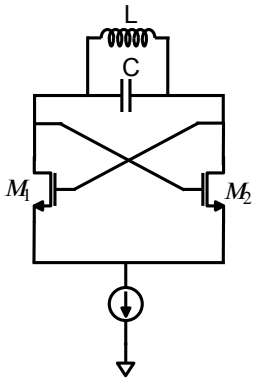


Figure 2.13: LC notch Q enhancement with a negative resistance generator.

One of the consequences of using negative resistance generators, including the cross-coupled differential pair as well as the topology in Figure 2.11a, is the increased power consumption due to the additional device. For example, in [8], the 3-coil transformer-based notch's quality factor is improved with a cross-coupled differential pair. As the current through the differential pair is increased, the negative resistance also increases, which sharpens the notch. This is an example of the trade-off presented by negative resistance generators, which is that more power can lead to a higher quality factor notch.

2.3 Summary of Filtering Techniques in Receivers

In this section, a number of filtering techniques used in LNAs and receivers were reviewed. Filtering on the PCB is an effective solution at improving out-of-band linearity of each receiver chain in the array, but suffers from additional loss and component cost[4].

Passive on-chip filters consisting of LC notches integrated into the LNA can achieve narrow-band out-of-band filtering limited by the quality factor of on-chip inductors. To widen the rejection band, notch filters can be distributed across a multi-stage amplifier. While passive techniques can provide adequate out-of-band filtering in an LNA, their downsides include lower gain and higher noise figure due to the extra losses. These disadvantages can somewhat be compensated by increasing power consumption or adding stages to the amplifier.

Active on-chip filtering has also been achieved. Active filtering generally relies on frequency-dependent feedback, or negative resistance generation. Active filtering can achieve higher stop-band rejection, but at the cost of more power consumption, as well

as noise added due to extra devices. Additionally, the higher effective quality factor of active notches leads to a narrower-band notch compared to low-Q passive notches.

All notches show a trade off between out-of-band linearity and noise figure depending on where, in a multi-stage amplifier, the notch is placed. Notches at the input of the amplifier and in the first stage, such as in [9] and [7] improve out-of-band linearity more than those in later stages of the amplifier. Lastly, all the techniques presented in this chapter increase chip area by adding inductors.

Chapter 3

System Analysis

This chapter presents the system analysis for a Satcom receive phased array operating between 17.7 and 21.2 GHz. The goal of this chapter is to derive the specifications required for the LNA in an interference-rejecting phased array receiver. The system model is presented, which is used to calculate the maximum achievable signal to noise ratio (SNR) given the specifications of the beamformer receiver. The system model is used to choose suitable specifications for the gain, noise figure, and linearity of the LNA. Keysight SystemVue™ is used to implement the system model and determine the required gain flatness of the LNA. Finally, the interference power from both 5G base stations and the Satcom transmitter self-interference is calculated, which is used to determine the out-of-band linearity specification of the LNA.

3.1 System Modelling

Figure 3.1 shows the block diagram of the system model of the phased array. It consists of an incoming signal with a certain power density and sky temperature. The phased array is modelled as N antennas, each of which is connected to a receiver consisting of an LNA, a phase shifter, and a gain control block. This 3-component receiver is modelled as having a gain G, a noise figure F, and a ambient temperature T_0. The signal from each receiver is combined using an N:1 Wilkinson power combiner. After combination, the signal SNR is given by SNR_{out}.

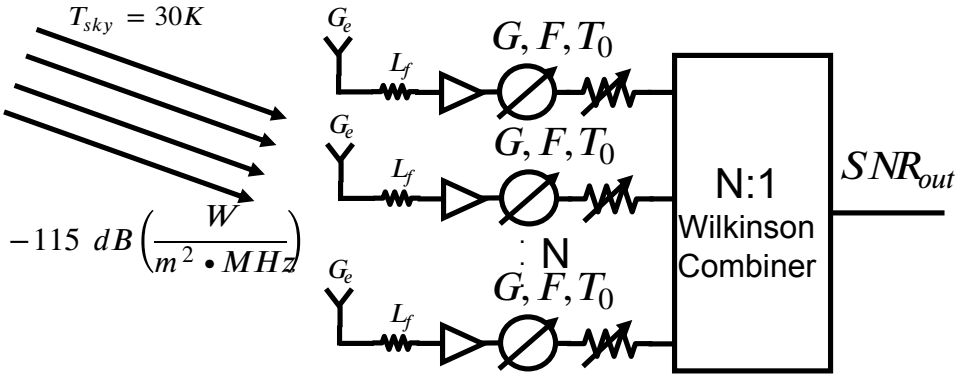


Figure 3.1: Block diagram of the phased array system model.

Figure 3.1 also shows that the assumed sky noise temperature T_{sky} is 30K. This is based on the study conducted in [28], which showed that between an elevation angle of 0^{o} and 65^{o}, the maximum sky noise temperature seen by the array is approximately 30K. It is assumed that the receive array will only scan to 65^{o} because that is a typical maximum scan angle achieved in real phased arrays before there is significant degradation in gain and grating lobe levels [4].

Furthermore, Figure 3.1 shows that the assumed power density of the incoming signal is -115 $dB\frac{W}{m^2 MHz}$, which is a regulation adopted by the International Telecommunications Union (ITU) and the United States Federal Communications Commission (FCC) in order to regulate the amount of interference caused by non-geostationary satellite down-link signals seen by receivers of geostationary signals [29].

The number of elements required for the receive phased array can be derived from the typical beamwidth of a Satcom signal. According to the ITU, a typical downlink 3-dB beamwidth of a Satcom system is 1.6^{o} [30]. The 3-dB beamwidth of an array decreases with an increasing number of elements, so this specification allows for the calculation of the minimum number of elements required for the array. From [18], the beamwidth of a square phased array is given by (3.1), where L represents the length of the array, and the physical area of the array is LxL.

$$\text{beamwidth} = \frac{0.886\lambda}{L}\text{rad}. \tag{3.1}$$

Assuming $\frac{\lambda}{2}$ spacing to minimize grating lobes [18], we can set $\text{L} = n\frac{\lambda}{2}$ where the array is a square array of n by n elements. After those substitutions and converting to degrees, the beamwidth can be expressed in terms of n as in (3.2).

$$\text{beamwidth} = \frac{101.5}{n}\text{degrees}. \tag{3.2}$$

Substituting a beamwidth of 1.6^{o} and solving for n in (3.2) gives an n of 64. Therefore, in order to satisfy the beamwidth requirement of a typical Satcom downlink beam, the receive array should consist of 4096 (64 by 64) elements. With the number of elements known, it is possible to estimate the SNR of the signal after demodulation at the array output using the model in Figure 3.1.

The additional parameters' values shown in Figure 3.1 are defined in Table 3.1. The element gain G_e of 4 dB and the feed loss L_f of 0.5 dB are chosen based on recent work in phased array antennas employing patch antennas PCBs at frequencies between 10 and 30 GHz [4][13][31][32][33]. Beamformers and LNAs operating between 10 and 30 GHz with noise figures between 1.8 and 4 dB have been reported in previous works using modern CMOS and SiGe technologies [3][4][14][24][34][35]. Therefore, a noise figure of 3 dB is chosen for the SNR calculation, as shown in Table 3.1. Finally, a signal bandwidth of 100 MHz is assumed based on example satellite system characteristics provided by the ITU [30].

Table 3.1: Definitions and values of the parameters used for the SNR calculation.

Symbol	Description	Value
P_D	EPFD	-115 dB$\left(\frac{\text{W}}{\text{m}^2\cdot\text{MHz}}\right)$
G_e	Antenna element gain	4 dB
L_f	Antenna feed loss	0.5 dB
F	Beamformer channel noise figure	3 dB
B	Bandwidth	100 MHz
T_0	Array ambient temperature	290 K
N	Number of Elements	4096

The system block digram shown in Figure 3.1 is similar to that in [36], except there is no additional loss modelled due to tapering of the array. The expression for the SNR at the output of array is given by [36] as

$$SNR_{out} = \frac{NS_i}{kTB}, \tag{3.3}$$

where S_i is the input power to one antenna element, B is the bandwidth of the signal, and T is the noise temperature of the array, given in [36] as

$$T = T_{sky} + T_0 \left(L_f F - 1 \right). \tag{3.4}$$

The input power to one antenna element can be calculated by multiplying the input power density S_{dens} by the effective aperture area A_e[37][p. 665]:

$$S_i = A_e S_{dens}. \tag{3.5}$$

The aperture area is dependent on the antenna gain and is given by [37][p. 666] as

$$A_e = \frac{G_e \lambda^2}{4\pi}. \tag{3.6}$$

The input power density can be calculated by multiplying the EPFD P_D (in $\frac{\mathrm{W}}{\mathrm{m^2 Hz}}$) by the signal bandwidth, by the definition of EPFD [29]:

$$S_{dens} = P_D B. \tag{3.7}$$

Combining (3.3) - (3.7) gives the expression for the SNR at the output of the array in terms of the parameters illustrated in Figure 3.1:

$$SNR_{out} = \frac{N P_D G_e \lambda^2}{4\pi k \left(T_{sky} + T_0 \left(L_f F - 1 \right) \right)}. \tag{3.8}$$

Substituting in the values from Table 3.1 into (3.8) gives an output SNR of 20.35 dB. This SNR is sufficient to demodulate digitally modulated signals using constellations such as QPSK, 16-QAM, and 16-APSK [38]

(3.8) shows that the SNR improves by increasing the number of elements, reducing the feed loss, and reducing the noise figure of the beamformer. Since the number of elements is already determined from the beamwidth calculation, the only way to improve the SNR is to reduce the feed loss and the noise figure. However, the feed loss and noise figure will be limited by the PCB and beamformer integrated circuit fabrication technologies, respectively. Therefore, if the values assumed in Table 3.1 are reasonable, then the SNR cannot be much better than 20.35 dB.

A limitation of the calculation in this section is that it does not take into account the noise added due to Ohmic losses in the combining network. This loss depends on the PCB technology used and any buffer amplifiers that are added to the feed network, so it cannot

be estimated without specific knowledge of the array implementation. To compensate this loss, generally the beamformer should have a high gain greater than 25 dB, as in multiple previous works [3][4][14][17][39].

3.2 Component Level Specifications

The system model defined in Section 3.1 can be used to determine component level specifications of the LNA for the interference-rejecting phased array receiver. Specifically, this section will discuss the required gain, noise figure, gain flatness, and linearity of the LNA.

3.2.1 Gain and Small-Signal Rejection

In general, the gain of the LNA should be high enough to compensate the loss or higher noise figure of subsequent blocks to keep the overall gain and noise figure of the receiver within the desired specification. As mentioned in Section 3.1, a beamformer receiver typically needs a gain greater than 25 dB to compensate for Ohmic losses on the PCB and combining network. Without knowing the exact gain specifications of the blocks following the LNA, it is prudent to assume that the majority of that gain should come from the LNA. Therefore, a gain greater than 25 dB is targeted.

An additional specification for out-of-band small signal rejection of 20 dB is added, meaning that the gain out of band should be 20 dB less than the in-band gain. This rejection helps to prevent the saturation of subsequent blocks in the receiver.

3.2.2 Noise Figure

In Section 3.1, a noise figure of 3 dB was assumed for the receiver, which allowed for 20 dB output SNR. It is expected that the addition of the phase shifter and gain control will degrade the chain noise figure, so the LNA noise figure should be lower than that targeted for the chain. Therefore, the targeted noise figure is selected to be less than 2.5 dB.

3.2.3 Gain Flatness

When receiving a signal with a high modulation bandwidth, the frequency response, in particular, the gain flatness, of the beamformer can affect the SNR of the system. This

section presents simulation results that are used to determine a specification for the 3-dB bandwidth of the beamformer.

Figure 3.2 shows example curves of a beamformer's frequency response for different 3-dB bandwidths. In this figure, the gain was assumed to be quadratic over frequency, peaking at a G_0 of 30 dB at a center frequency f_c of 19.5 GHz and reaching 27 dB at $f_c \pm \frac{BW_{3dB}}{2}$. Figure 3.2 also shows an example signal bandwidth between 17.7 and 17.95 GHz, which would correspond to a 250 MHz signal at the edge of the Satcom band. The figure shows that for a low 3-dB bandwidth, the gain for this signal would be lower, and there would be more in-band distortion due to the steeper slope vs. frequency. These effects will degrade the SNR.

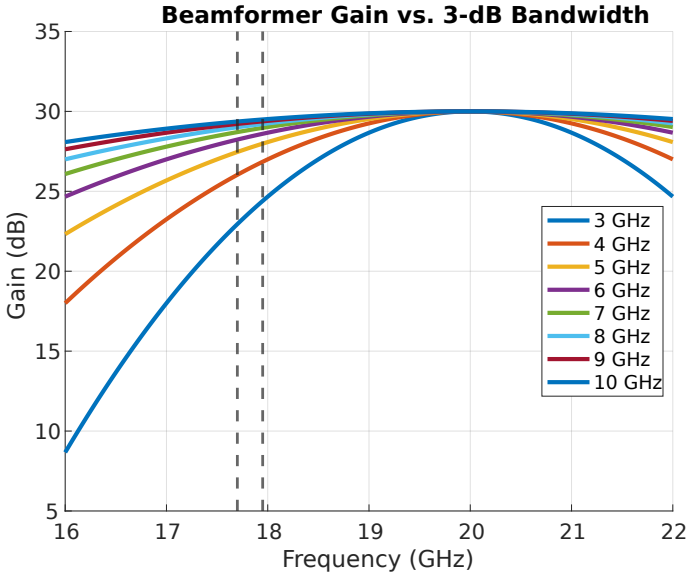
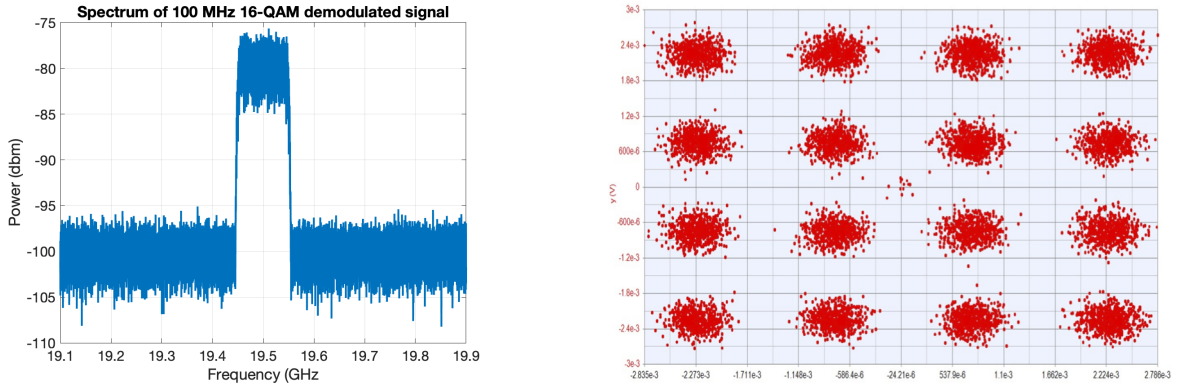


Figure 3.2: Frequency response of a beamformer with different 3-dB BWs.

The effect of the beamformer gain flatness on the output SNR of the array was investigated by simulating the array model of Figure 3.1 in Keysight SystemVue^{TM}. A 16-QAM constellation was used as the test signal for the array.

First, the array was simulated without any gain variation of the LNA over frequency. The simulated spectrum and constellation of the receiver are shown in Figures 3.3a and 3.3b, respectively. The SNR of the demodulated signal is given by SystemVue as 20.3 dB, which matches the 20.35 dB SNR calculated in Section 3.1. The match in results

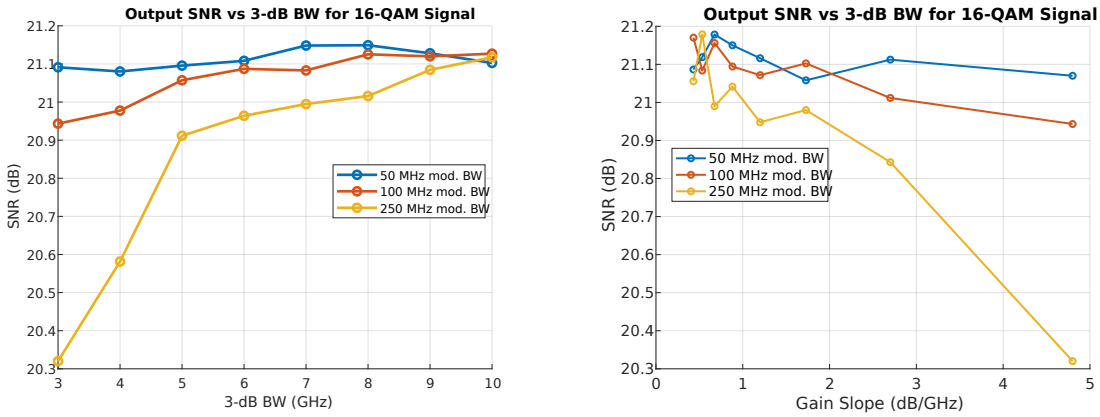
shows that the SystemVue simulation model can be relied upon for other simulations of the array's performance.



(a) (b)

Figure 3.3: Modulated signal simulation results. (a) Spectrum of the modulated signal at the output of the simulated array. (b) Constellation of the demodulated output of the simulated array.

With the SystemVue model validated, it was then used to simulate the effect of gain flatness on the output SNR. The simulation was conducted for 50, 100, and 250-MHz signal bandwidths, where the carrier frequency was chosen to be 17.7 GHz + $\frac{BW_{signal}}{2}$ in each case. Figure 3.4 shows the results of the simulations. Figure 3.4a shows the output SNR of the array vs. beamformer 3-dB bandwidth, while Figure 3.4b shows the same data vs. gain flatness at 17.7 GHz. As expected, the effect of 3-dB bandwidth on the SNR of narrow-band signals is small, as the SNR stays relatively unchanged for the 50-MHz signal. However, for the 100-MHz and 250-MHz signals, narrow beamformer bandwidth degrades the SNR more. To support 250-MHz modulation bandwidths, the beamformer should have a gain flatness of better than 2 dB/GHz at the edge of the band, while to support 100-MHz modulation bandwidths it should have have a gain flatness better than 3 dB/GHz.



(a) (b)

Figure 3.4: Effect of beamformer frequency response on array output SNR with a 16-QAM signal of varying bandwidths. (a) SNR vs beamformer 3-dB bandwidth. (b) SNR vs gain flatness at 17.7 GHz.

3.2.4 LNA Linearity

There are a number of considerations to be made for the linearity requirement of a Satcom receive beamformer. Firstly, the receiver must be able to receive the in-band signal without any compression. It will be shown in this section that the in-band Satcom signal is very weak, so the in-band linearity requirement is not very stringent. The more important consideration to make is the level of interference the receiver sees. As explained in Chapter 1, both 5G signals and the self-interference of the nearby transmitter can be sources of interference for the sensitive Satcom receiver. This section will calculate the beamformer linearity required to withstand these interferers.

In-band Linearity

By combining (3.5)-(3.7), the power at the input of the receiver can be calculated from the incident power density and the aperture area of a single antenna element as

$$S_i = \frac{P_D B G_e \lambda^2}{4\pi}. \tag{3.9}$$

Substituting the values in Table 3.1 into (3.9) gives an input power S_i of -108.5 dBm.

This power level is many orders of magnitude lower than typically reported IP_{1dB} vaules for K/Ka-band LNAs in SiGe and CMOS, which typically range between -35 and -15 dBm [24][34][35]. Therefore, an in-band IP_{1dB} of greater than -40 dBm is targeted.

Another measure of linearity for LNAs is the input third-order intermodulation intercept point (IIP_3). Typically, this value is expected to be about 10 dB higher than the IP_{1dB} [21]. Therefore, an in-band IIP_3 of -30 dBm is targeted.

5G Blockers

One source of intereference that a Satcom receiver may experience is 5G wireless signals from relatively close and high-power base stations. 5G millimeter-wave systems will have cell sizes on the order of hundreds of meters, meaning the base station could be close to to a Satcom receiver and pose a significant threat of saturating the receiver [14]. This section shows the calculation for the blocker power and required out-of-band linearity of the receiver.

The blocker power, in dBm, at the input of the receiver can be calculated as in (3.10), where L_{path} is given by (3.11). These equations are based on the link budget equations in [37][p. 674]. They show that the blocker power depends on the frequency-dependent parameters L_{path} and G_{ant}.

$$P_{block,in}[\text{dBm}] = \text{EIRP}_{\text{BS}} + 10log(\frac{BW}{100\,\text{MHz}}) - L_{path} + G_{ant} + \text{PAPR}. \tag{3.10}$$

$$L_{path} = 20\text{log}\left(\frac{4\pi d}{\lambda}\right). \tag{3.11}$$

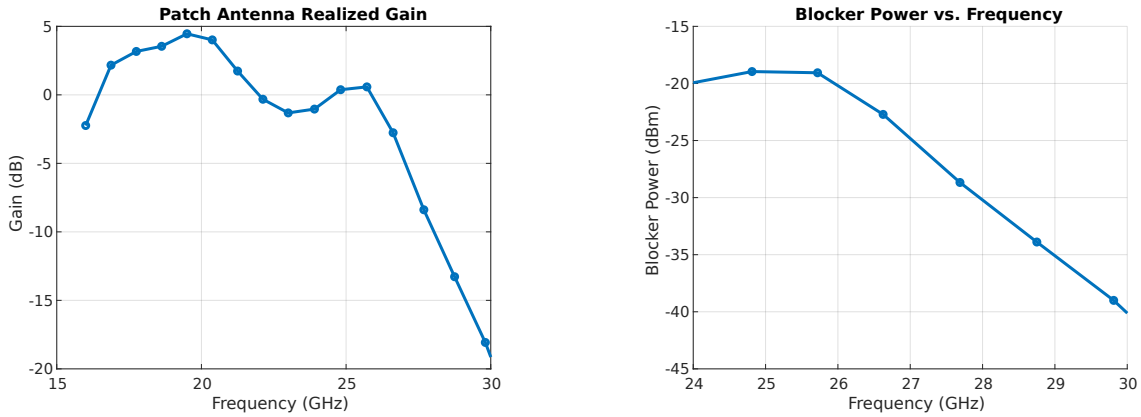
The values used to evaluate the 5G blocker power in (3.10) are shown in Table 3.2. The frequency-dependent antenna gain G_{ant} used in the calculation is shown in Figure 3.5a, which is the response of the patch antenna designed in [13].

The calculated blocker power from evaluating (3.10) is shown in Figure 3.5. With a 100-MHz signal bandwidth, the blocker power can as high as -19 dBm at 25 GHz. At higher frequencies, due to the lower antenna gain and higher path loss, the blocker power is less, dropping to only -40 dBm at 30 GHz. Therefore, the receiver's linearity in the case of a 5G blocker event is the most important at 24-26 GHz, where it must tolerate up to -19

Table 3.2: Example calculation for the 5G blocker power.

Parameter	Description	Value
d	Distance from base station to Rx array (m)	100 [14]
$EIRP_{BS}$	Base station average EIRP (dBm/100 MHz)	75 [40]
BW	Signal Bandwidth (MHz)	100 [41]
G_{ant}	OOB Rx boresight gain (dB)	See Figure 3.5a.
PAPR	Blocker peak-average power ratio	6 dB [14]

dBm in blocker power. To have some margin, a the LNA's IP_{1dB} is targeted to be greater than -16 dBm between 24 and 26 GHz.



(a) (b)

Figure 3.5: (a) Patch antenna gain over frequency from [13] as well (b) the calculated 5G blocker power over frequency.

Satcom Transmitter Self-Interference

The other main source of interference for the Satcom receiver is the coupled signal from a nearby Satcom transmitter operating at 27 - 30 GHz. Typically, in Satcom solutions, a receive and transmit array are placed side-by-side and treated as one full product. The close proximity of the transmitter to the receiver means that the high output power of the transmitter can couple to the receiver and jam it, causing distortion in the desired downlink signal. Therefore, the receiver must have enough out-of-band linearity to tolerate this potential jammer.

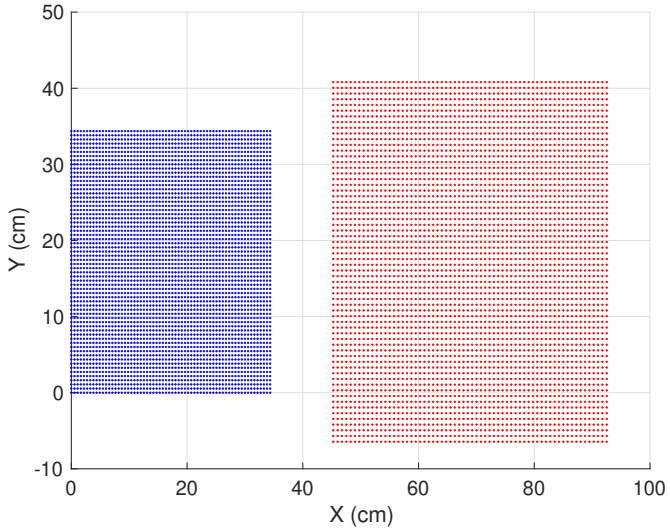


Figure 3.6: Relative positions of two 4096-element transmitter and receiver arrays separated by 10cm.

The coupling between the transmitter (Tx) and receiver (Rx) can be estimated by assuming the size and relative position of each array, and then calculating the distance that a plane wave from each Tx element must travel to a given Rx element. This distance can be used to calculate the magnitude and phase of the plane wave due to each Tx element at the given Rx element. When summed together, it gives the Tx to Rx coupling for one element.

Figure 3.6 shows an example positioning of side-by-side transmitter and receiver arrays. Both arrays are 4096-element arrays with $\frac{\lambda}{2}$ spacing between elements, where the frequency of λ is 27.5 GHz for the transmitter and 20 GHz for the receiver. The $\frac{\lambda}{2}$ spacing is chosen to avoid grating lobes in the array pattern [18]. The arrays are separated by $10\lambda_{tx}$, which is approximately 10 cm.

The over-the-air coupling from all the Tx elements to one Rx element is estimated as follows. First, assume that all the Rx elements are far away enough from each Tx element such that the the far field assumption can be made on the radiation of a single Tx element. Then, the electric field appearing at the j-th Rx element due to the i-th Tx element is proportional to B_{ij}, given in (3.12), which is the electric field of an isotropic radiator [42]. In (3.12), r_{ij} is the magnitude of the distance between the i-th Tx and j-th Rx elements, while $k = \frac{2\pi f_{tx}}{c}$ is the wavenumber at the Tx frequency, where f_{tx} is 27.5 GHz and c is the speed of light in free space. The term is also multiplied by a weighting factor w_i, which

represents the complex weight applied for beam steering. w_i is given in (3.13), where θ and ϕ represent the steering direction and (x_i, y_i) is the position of the i-th Tx element [18].

$$B_{ij} = \frac{e^{jkr_{ij}}}{4\pi r_{ij}} w_i \tag{3.12}$$

$$w_i = e^{jksin\theta(x_i cos\phi + y_i sin\phi)} \tag{3.13}$$

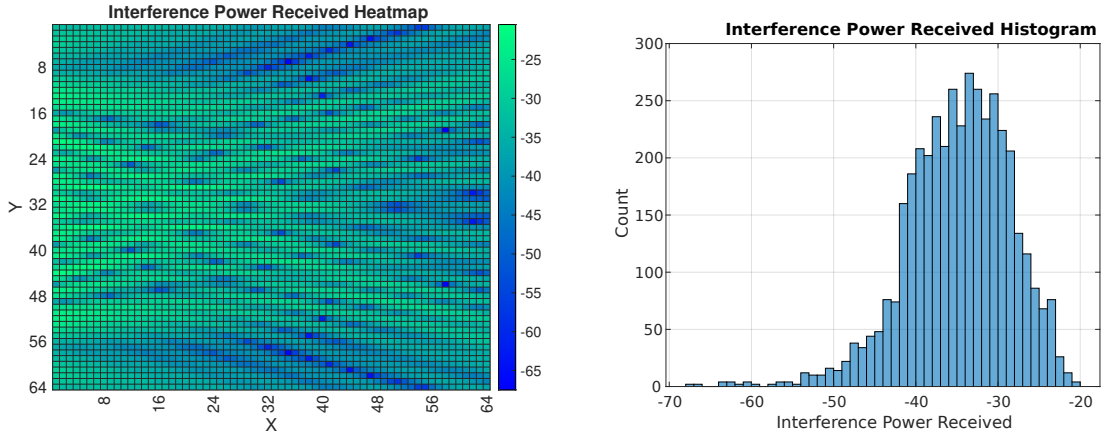
Then, the total power coupled to one Rx element is the summation over all the Tx elements, given in (3.14). In (3.14), P_{out} is the power radiated by one Tx element. It is assumed that this power is the same for every element in the transmit array. $G_{tx,90}$ is the gain of the Tx patch antenna at $\theta = 90°$ at f_{tx} and $G_{rx,90}$ is the cross-polarization gain of the Rx patch antenna at at $\theta = 90°$ at f_{tx}. Cross-polarization gain is used for the Rx patch gain as satcom transmitters and receivers often operate at different polarizations [3].

$$P_j = P_{out} G_{tx,90} G_{rx,90} \left(\sum_{i=1}^{N_{tx}} B_{ij} \right)^2 \tag{3.14}$$

(3.14) is evaluated for the geometry in Figure 3.6, using the values in Table 3.3. The output power of 10 dBm is chosen based on previously reported output 1-dB compression points for Ka-band Satcom phased array beamformers [17][43]. To calculate the worst-case coupling, the transmitter is steered to $\theta = 65°$, which is a practical maximum steering angle of a Satcom transmit array [17]. The patch antenna gains at 90° of -10 dB for the Tx and -45 dB for the Rx were chosen based on simulations of a patch antenna simulated in Ansys HFSS™ using the Antenna Toolkit [44]. The heatmap and histogram of the power received at each Rx element is shown in Figure 3.7. The maximum received power by a given receiver element is approximately -21 dBm.

Table 3.3: Parameters used for the self-interference estimation.

$G_{tx,90}$	$G_{rx,90}$	P_{out}	f_{tx}	f_{rx}	θ	ϕ
-10 dB	-45 dB	10 dBm	28 GHz	20 GHz	65	0



(a) (b)

Figure 3.7: Results of the coupling calculation. (a) Heatmap of received power at 28 GHz. (b). Histogram of received power.

Therefore, the blocker power due to the transmitter is approximately -21 dBm. For some margin, the IP_{1dB} of the Satcom is targeted to be greater than -18 dBm in the 27-30 GHz Satcom uplink band.

3.2.5 Input and Output Return Losses

Since the LNA is designed for Satcom applications, it should be well-matched to an external feed line of an antenna on a phased array PCB, which is typically designed for a 50 Ω input impedance. Therefore, an input return loss of lower than -10 dB is targeted. For the output matching, even though in a receiver, the blocks after the LNA may not have 50 Ω input impedances, the LNA should still be compatible with measurement equipment in order to be tested in isolation. Measurement equipment such as wafer probes, RF cables, and VNAs are typically matched to 50 Ω as well, so an output return loss of -10 dB is also targeted.

3.2.6 Power Consumption

Generally, Satcom beamformer ICs require low power consumption because hundreds to thousands of ICs are placed on a single array with thousands of elements. The LNA's power consumption must be reasonable compared to a typical beamformer IC. Recently

reported beamformers in the K-band frequency in CMOS and SiGe technologies have had DC power consumptions between 30 and 70 mW per channel [45][3][4][46]. In addition to the LNA, these reported receivers also contained phase shifters, variable-gain amplifiers, digital control circuits, and analog blocks for power management, meaning the LNA consumes a fraction of that reported power. As a conservative estimate, the LNA DC power consumption is targeted to be 15 mW.

3.2.7 Chip Area

The chip area for a beamformer IC is limited by the space on the phased array PCB for each IC. A typical phased array may use $\frac{\lambda}{2}$ spacing between elements in a rectangular lattice to avoid grating lobes in the antenna pattern [18]. At 20 GHz, the wavelength λ is 15 mm, giving 7.5 mm between antenna elements. Since some satellite constellations use circularly-polarized signals, each antenna feeds two receiver channels.

One way to symmetrically route these feeds on the PCB is to have an 8-channel beamformer IC for a 2 by 2 dual-polarized antenna element tile [17][13][45]. The beamformer chip floorplan for this tiling style is shown in Figure 3.8. This tiling means each 8-channel beamformer must fit in a 7.5 by 7.5 mm space. Leaving 1 mm of space on each side of the IC for extra routing and packaging, the die size could be 5.5 by 5.5 mm.

Based on the floorplan in Figure 3.8, a suitable area for each receiver channel is approximately 2.5 mm (horizontal) by 1 mm (vertical). As shown in Figure 3.1, the receiver channel needs, at the very least, an LNA, a phase shifter, and a gain control block. The LNA should be allocated a significant portion of this area since it determines the overall receiver noise figure. Therefore, an LNA chip area of less than 1 mm by 1 mm is targeted.

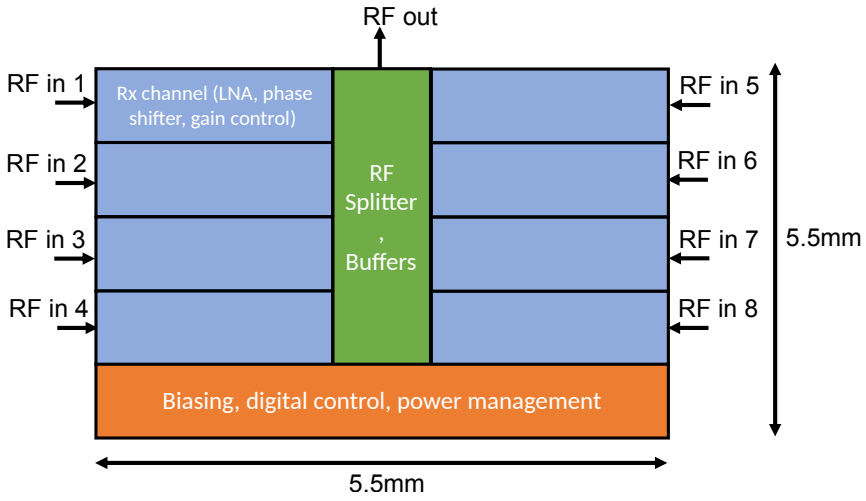


Figure 3.8: Example floorplan of an 8-channel beamformer for a 2 by 2 dual-polarized phased array tile (not to scale).

3.2.8 Summary of Specifications

Table 3.4 summarizes the targeted specifications of the LNA based on the system analysis performed in this chapter. In the subsequent chapters, the LNAs that are designed will target these specifications.

Table 3.4: LNA specifications.

Specification	Value
Frequency	17.7 - 21.2 GHz
Gain	$>$ 25 dB
Small-signal rejection at 24-30 GHz	$>$ 20 dB
Noise Figure	$<$ 2.5 dB
Gain flatness	$<$ 3 dB/GHz between 17.7 and 21.2 GHz
IP_{1dB} in-band	$>$ -40 dBm
IIP_3 in-band	$>$ -30 dBm
IP_{1dB} at 24-26 GHz	$>$ -16 dBm
IP_{1dB} at 27-30 GHz	$>$ -18 dBm
Input Return Loss in-band	$<$ -10 dB
Output Return Loss in-band	$<$ -10 dB
DC Power Consumption	$<$ 15 mW
Small-signal rejection at 24-30 GHz	$>$ 20 dB
Chip Area	$<$ 1 mm x 1 mm

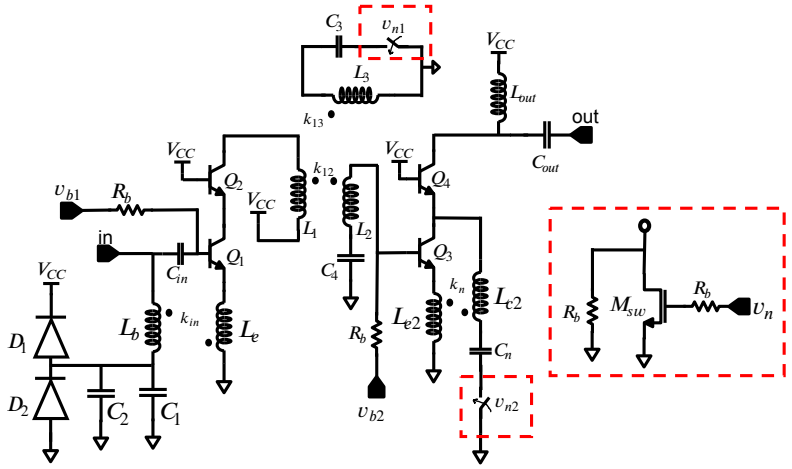
Chapter 4

Interference-Rejecting LNA Design

This chapter addresses the design of two interference-rejecting LNAs for the purposes of improving the tolerance of a satellite communication beamformer to out-of-band interferers. The first LNA (Design 1) is designed to meet the specification for rejecting interference from both 5G wireless signals and Satcom self-interference. The second LNA (Design 2) is designed for an alternative use case, where it only needs to reject Satcom self-interference. Both LNAs are designed and simulated using the GlobalFoundries 8XP 130nm SiGe BiCMOS process [47]. Section 4.1 presents the design and simulation results of LNA 1, while Section 4.2 presents the second LNA. The performance of each LNA is summarized and compared to the target specifications in Section 4.3.

4.1 Design 1: A Single-Ended LNA with 5G and Satcom Self-Interference Rejection

This section will present the first filtering LNA that was designed in this work. The circuit topologies that were used in this LNA borrow from the filtering techniques that were presented in Section 2.2. The schematic of the LNA that implements 24-30 GHz filtering is shown in Figure 4.1.



L_b	753 pH
L_e	127 pH
k_{in}	0.45
C_{dec}	6.5 pF
Q_1	32x0.12 μm^2
Q_2	32x0.12 μm^2
L_1	907 pH
L_2	1.7 nH
k_{12}	0.49
L_3	692 pH
k_{13}	0.36
C_3	55 fF
C_4	2 pF
Q_3	4x0.12 μm^2
Q_4	4x0.12 μm^2

L_{e2}	157 pH
L_{c2}	417 pH
k_n	0.61
C_n	55 fF
L_{out}	693 pH
C_{out}	64 fF
R_b	10 kΩ
v_{b1}	0.94 V
v_{b2}	0.9 V
M_{sw}	$\frac{200\ \mu m}{0.12 \mu m}$
V_{CC}	1.8 V

Figure 4.1: Schematic of the LNA Design 1 with 24-30 GHz filtering designed in this work.

The LNA in Figure 4.1 consists of two cascode stages. Each stage is biased with large 10 kΩ resistors connected to a pad, where a voltage bias is applied. The input matching uses transformer-feedback matching, implemented with the coupled inductors L_b and L_e [48]. The input is also protected from electro-static discharge (ESD) with diodes D_1 and D_2. The inter-stage matching uses the 3-coil transformer matching technique introduced in [8], which introduces one notch into the frequency response of the amplifier. The second stage adds a second notch from the transformer consisting of L_{e2} and L_{c2}, as well as the capacitor C_n. The output matching is a simple one-section LC network consisting of L_{out} and C_{out}. Also, both of the notches are controlled by NMOS switches (M_{sw}) that are controlled by voltages v_{n1} and v_{n2} respectively. In the following sections, the analysis and design of each part of the amplifier will be elaborated upon.

4.1.1 Transistor Sizing, Bias, and Layout

One of the most important steps of the design process of any LNA is the design of the transistor cores of each stage. Of particular interest is the design of the first stage, as it limits the minimum noise figure of the amplifier. First, the transistor's emitter length is sized such that the real part of the optimal source impedance, Z_s is 50 Ω. Then, the bias current of the cascode transistor core is chosen to a value that minimizes the minimum noise figure, NF_{min} of the cascode stage. Finally, the layout of the cascode stage is carefully performed to minimize the parasitic resistances and capacitances that degrade the noise figure and gain of the stage.

First-Stage Device Size

Unlike CMOS transistors, with SiGe HBTs the optimal bias for minimum noise and optimal emitter area for simultaneous noise and conjugate matching depends on whether there is a cascode transistor and whether there is inductive degeneration [20, p. 247]. Therefore, in order to characterize the performance of the transistor in simulation, the cascode transistor is included and its emitter length is swept with the common-emitter transistor. A 100-pH inductive degeneration is added in this simulation to estimate the effects of inductive degeneration. The schematic of this simulation bench is shown in Figure 4.2. In this testbench, $P1$ and $P2$ represent s-parameter simulation ports. Both the input and output of the cascode transistor core are biased with ideal bias-T's consisting of ideal DC blocking capacitors and ideal DC feeding inductors provided available in Cadence Virtuoso™ for the Spectre™ circuit simulator.

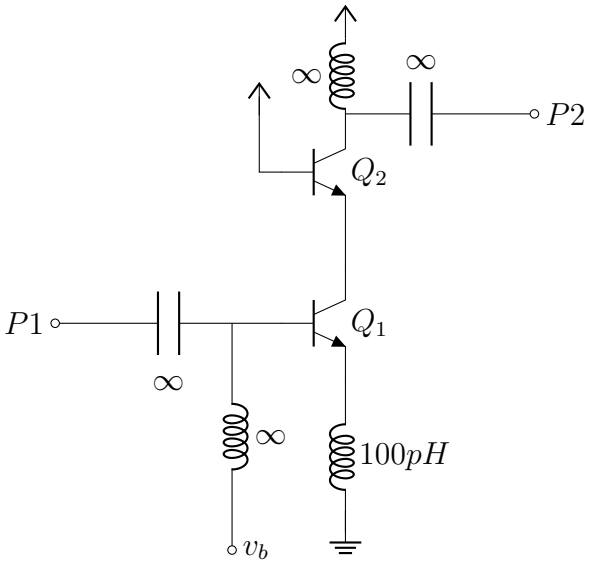


Figure 4.2: Schematic that was simulated to determine the optimal first-stage emitter length. Both devices have the same emitter area, and have a constant emitter width of 0.12 μm.

Using the simulation setup from Figure 4.2, the optimal noise source impedance, Z_{opt}, versus the emitter length of Q_1 and Q_2 is simulated. Both Q_1 and Q_2 have the same emitter area, with a constant width of 0.12 μm. The plot of Z_{opt} verus the emitter length is plotted on the Smith chart in Figure 4.3.

In order to achieve simultaneous noise and conjugate matching, the emitter length of the first stage devices should be chosen such that Re(Z_{opt}) is 50 Ω, where Z_{opt} is the optimal source impedance for lowest noise figure. Figure 4.3 shows that Re(Z_{opt}) is 50 Ω when the emitter length is about 30 μm. However, as will be explained in Section 4.1.1, the layout of the transistor adds parasitics that change the optimal noise impedance. Therefore, after layout and optimization, the final emitter length was selected as 32 μm, consisting of four unit transistors with 8 μm emitter lengths.

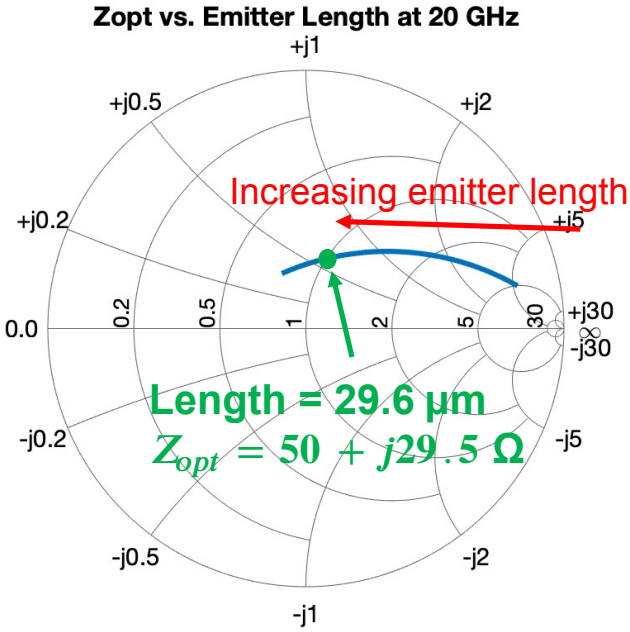


Figure 4.3: Smith Chart plot of the change in Z_{opt} with the emitter length of Q_1 and Q_2 at 20 GHz.

Biasing

The bias for the first stage is chosen to minimize the noise figure of the stage. Figure 4.4 shows the plot of NF_{min} versus the bias current of the 32x0.12μm^2 cascode input stage. It shows that the minimum noise figure of 1.2 dB is achieved at a bias of 0.36 mA/μm, which corresponds to 11.52 mA for an emitter length of 32 μm. With a 1.8 V supply voltage, this leads to over 20 mW of DC power consumption, which is above the target of under

15 mW. In order to achieve a lower power consumption, the LNA was biased at 5.64 mA instead, which results in a 0.1 dB degradation in noise figure but saves 10.5 mW of DC power consumption. This bias results in a first-stage DC power consumption of 10.15 mW.

With the first stage already consuming 10.15 mW to minimize noise figure, less than 5 mW out of the 15 mW power budget remain for the second stage. Therefore, smaller devices of emitter area 4x0.12 μm^2 were chosen. To improve the smaller devices' linearity, they were biased at 2 mA, which corresponds to 0.5 mA/μm. This bias point is closer to the peak-fT bias point of the technology, which results in a higher linearity and gain [20, p. 401]. In addition, the smaller devices have lower collector-base parasitic capacitance (C_μ), which, as will be shown in Section 4.1.4, leads to a better second-stage filtering response.

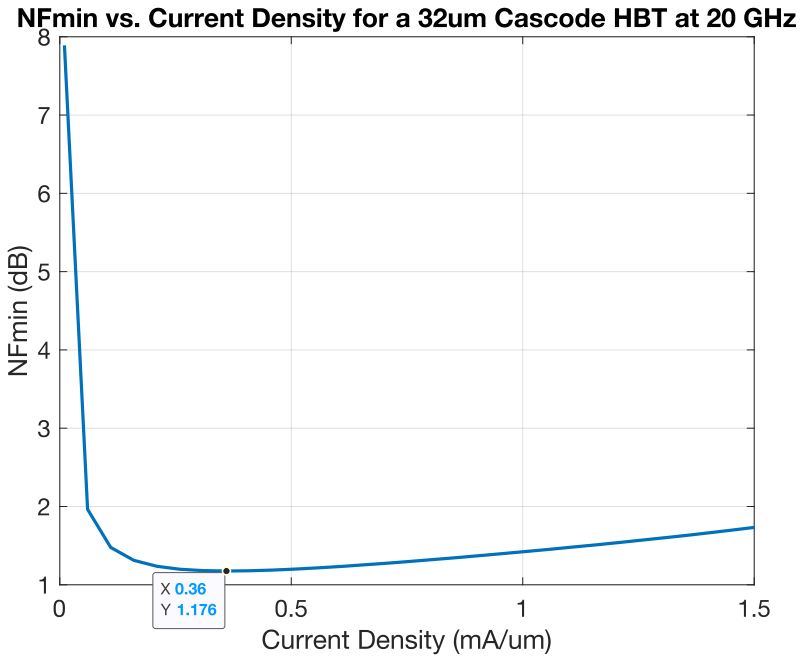


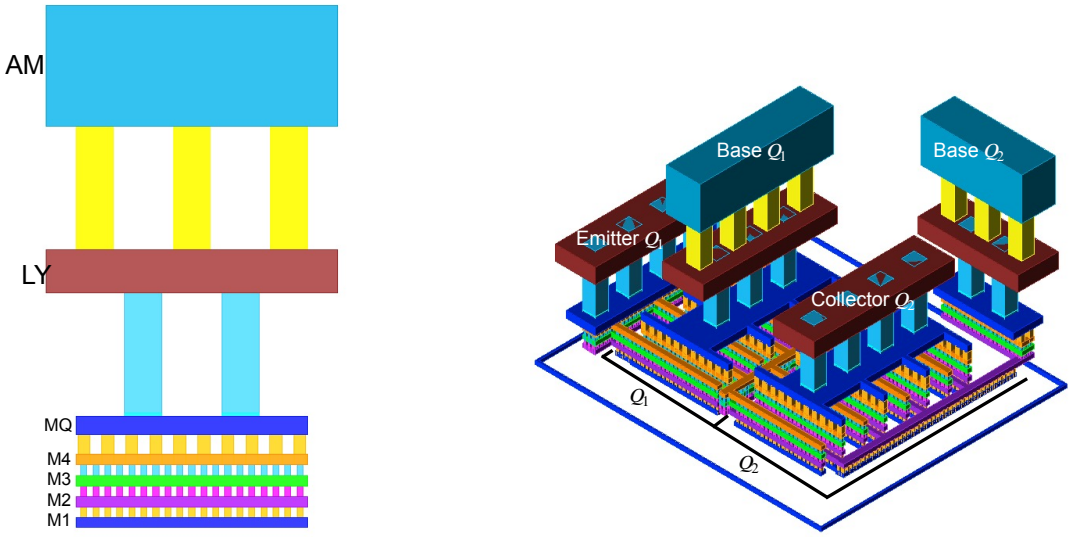
Figure 4.4: Minimum noise figure at 20 GHz vs. current density (in mA per micron of emitter length) for a cascode stage consisting of HBTs with 32x0.12μm^2 emitter area.

Transistor Layout

With the transistors' emitter areas and bias currents chosen, the first-stage transistor core can be laid out. Overall, there were two goals in the layout of the first stage transistor in

order to maximize the performance of the stage: 1) minimize the parasitic resistance to the base of the common-emitter transistor to reduce the noise figure, and 2) minimize the feedback capacitance C_μ to maximize the gain of the stage.

The layout of the stage is shown in Figure 4.5. The 32x0.12 μm^2 transistor is implemented using four 8x0.12 μm^2 HBTs that are placed side-by-side. The cascode transistor, Q_2, is placed right next to Q_1 for compact area and low interconnect parasitics. Q_2 consists of the same number of 8x0.12 μm^2 unit HBTs. To minimize the parasitic resistance to the base of Q_1 the bases are connected together in the middle copper layer, MQ, as defined in the metal stackup in Figure 4.5a.



(a) (b)

Figure 4.5: First-stage active core layout. (a) Metal stack-up of the GlobalFoundries 8XP process. AM and LY are thick aluminium layers for interconnects and RF passives, while the other layers are copper. (b). Layout images of the first stage transistor core.

To minimize the parasitic feedback capacitance C_μ and C_π of Q_1, care is taken to only stack the minimum number of metals on the collector and emitter stripes. Using fewer metal layers reduces the fringing capacitances of adjacent metals, but enough layers must be stacked to satisfy electromigration rules at 100$^{\text{o}}$C; too few metals can reduce the reliability of the transistor to carry its bias current over its operational lifetime.

Finally, the parasitics of the laid-out transistor are extracted using EMX, which is an electromagnetic (EM) simulator. The performance of the transistor is simulated again

using the bench in Figure 4.2 to determine the NF_{min} and the frequency at which Re(Z_{opt}) is 50 Ω. The extracted parasitics changed the performance the transistor, so the emitter length was changed and the process of layout and extraction was repeated until Re(Z_{opt}) was 50 Ω at 20 GHz. The final emitter length of Q_1 and Q_2 after this optimization process was 32 μm.

4.1.2 Input Matching Network

As shown in Figure 4.1, the input matching consists of a feedback transformer formed by the coupling of L_b and L_e. This feedback is presented an analyzed in detail in [48]. It is shown that the input impedance of the amplifier is approximately given by (4.1), where g_m refers to the transconductance of the input device Q_1, $n = \sqrt{\frac{L_b}{L_e}}$ is the turns ratio, and k is the coupling factor. Since all the terms are ideally frequency-independent, it shows that the input match is ideally wideband. Realistically, the transformer has parasitic capacitances that change the effective inductances and coupling of the coils over frequency, restricting the bandwidth of the match.

$$Z_{in} \approx \frac{1}{g_m} \frac{(\frac{n}{k})^2}{\frac{n}{k} + 1} \tag{4.1}$$

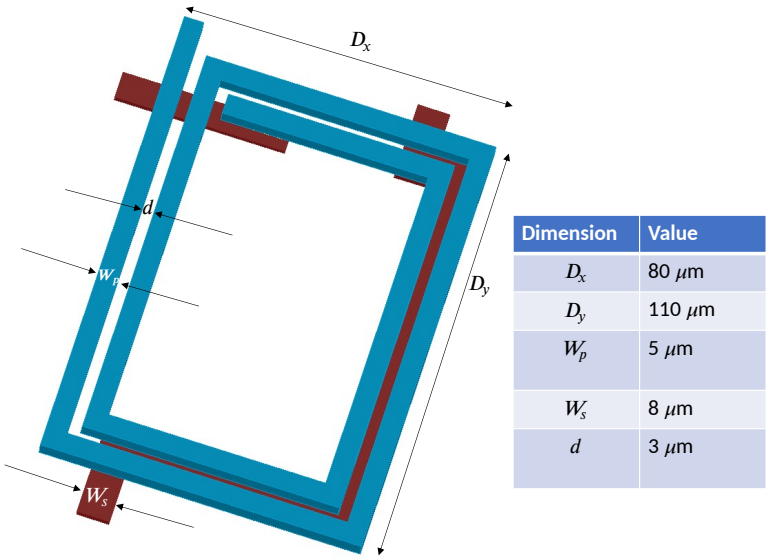
The use of this matching technique is advantageous over the conventional series inductor matching presented in section 2.1.1 because it is wideband. The series inductor match presented in Figure 2.1a is a narrow-band matching technique. A wider-band technique is needed in order to meet the input return loss specification of -10 dB (with 2 to 3 dB of margin) over the Satcom band of 17.7 to 21.2 GHz. With the typical series inductor match, the bandwidth of the input match improves with decreasing quality factor of the series inductor L_s in Figure 2.1a, as this inductor resonates out C_{gs} of the input transistor. In order to improve the bandwidth with the series inductor, it must be designed to have a lower Q, which will degrade the noise figure.

Another advantage of using the transformer match is that it allows for the easy addition of electrostatic discharge (ESD) protection in the form of diodes. This protection is accomplished by putting a double-diode pair in parallel with the decoupling capacitors C_1 and C_2, as shown in Figure 4.1 [48]. From an RF signal point of view, the ESD diodes appear as a parasitic capacitance to ground. Since this capacitance appears in parallel with the already large capacitors C_1 and C_2, it has no effect on RF performance. By contrast, if it was placed in parallel with the v_{in} node in the common-source LNA of Figure 2.1a, it would increase loss and change the input matching.

Input Transformer Design

(4.1) can be used to obtain a first-pass estimate of the required $\frac{n}{k}$ for the input transformer. As described in Section 4.1.1, a 32μm cascode stage biased at 5.64 mA was chosen for the input stage. However, the layout parasitics and series resistance of the degeneration inductor L_e all reduce the effective g_m of the input transistor. To take into account these effects, the low-frequency Y_{21} of the first stage with a 100 pH degeneration inductor of Q = 15 is simulated with a similar testbench as in Figure 4.2. This simulation yields a low-frequency Y_{21} of 0.15 S. Substituting this value of Y_{21} for g_m and $Z_{in} = 50\ \Omega$ into (4.1) gives a required $\frac{n}{k}$ of 8.4.

A parametric sweep of the primary inductance reveals that $L_b = 650$ pH is required to match the transistor at 20 GHz when $\frac{n}{k}$ is 8.4. After layout and EM simulation of the input transformer, it is further optimized such that $L_b = 760$ pH, $L_e = 127$ pH, and k = 0.45. These values give an $\frac{n}{k}$ of 5.4. The transformer is laid out on the top two metal layers of the process, where L_b, and its layout is shown in Figure 4.6.



Dimension	Value
D_x	80 μm
D_y	110 μm
W_p	5 μm
W_s	8 μm
d	3 μm

Figure 4.6: Layout of the input transformer for the LNA.

4.1.3 Interstage Matching Network

As shown in the Figure 4.1, the inter-stage matching network between the two amplifier stages consists of the three-coil notch transformer introduced in [8]. This section will

present the analysis and design of the inter-stage matching network for the filtering LNA.

Inter-stage Noise vs Conjugate Matching

The inter-stage matching network can be designed for either conjugate matching or noise matching. Figure 4.7 shows the block diagram of the 2-stage LNA with an inter-stage matching network (IMN). With conjugate matching, the IMN transforms Z_{out1} to $Z_{s2}*$, which maximizes the gain. However, the second stage, like any amplifier, has a specific source impedance for which its noise figure is minimized, Z_{opt2}. As an alternative to conjugate matching, the IMN can be designed to transform Z_{out1} to Z_{opt2}, which minimizes the noise figure of the second stage and reduces the overall amplifier noise figure. The gain is no longer maximized but the noise figure is minimized.

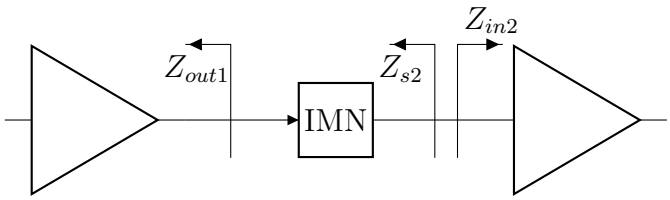


Figure 4.7: Block diagram of the LNA and its inter-stage matching network (IMN).

Figure 4.8 shows a Smith chart plot of Γ_{Opt}, S_{11}, and S_{11}^* of the second stage within the signal band. The normalized impedances Z_{opt} and Z_{in}^* are approximately 5 + j3 Ω and 3 + j3 Ω respectively. In order to achieve a compromise between noise and impedance matching, the targeted source impedance for synthesized by the inter-stage matching network is 4 + j3 Ω.

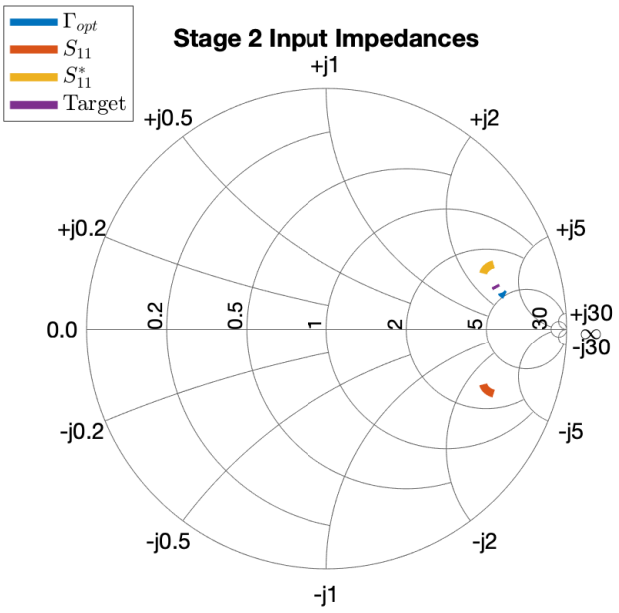


Figure 4.8: Smith chart plot of the second stage's Γ_{opt} and S_{11} from 17.7-21.2 GHz

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Matching Network Design

The equivalent circuit of the inter-stage matching network is shown in Figure 4.9. L_{14}, C_3', L_{12}', k_{12}'', and L_2 represent the equivalent circuit parameters of the three-coil transformer, defined in (2.7) to (2.10). Finally, Z_{out1} is the output impedance of the first stage.

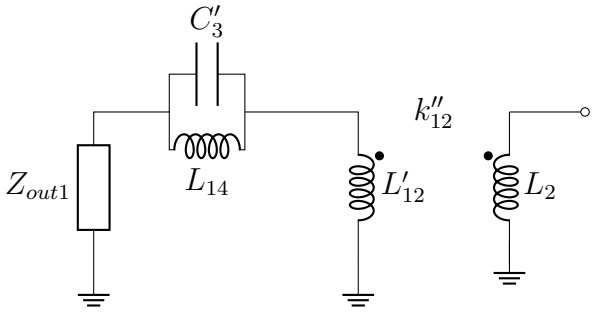


Figure 4.9: Equivalent circuit of the inter-stage matching network of the LNA.

In the equivalent circuit of Figure 4.9, at frequencies below the resonant frequency of $\omega = \frac{1}{\sqrt{L_3 C_3}}$, the parallel tank consisting of L_3 and C_3 looks inductive, so it can be represented by an equivalent inductance L_{eq}. The expression for L_{eq} is found by considering the parallel impedance of L_{14} and C_3', given by (4.2), which simplifies to (4.3). Next, substituting $L_{14} = k_{13}^2 L_1$ ((2.7)) and $C_3' = \frac{L_3}{k_{13}^2 L_1} C_3$ ((2.8)) and simplifying gives (4.4). Finally, letting the notch frequency ω_n be given by $\omega_n = \frac{1}{\sqrt{L_3 C_3}}$ simplifies the equation to (4.5). Thus, the equivalent inductance L_{eq} is given by (4.6).

$$Z_{eq} = sL_{14} || \frac{1}{sC_3'}. \tag{4.2}$$

$$Z_{eq} = s\frac{L_{14}}{1 - \omega^2 L_{14} C_3'}. \tag{4.3}$$

$$Z_{eq} = s\frac{k_{13}^2 L_1}{1 - \omega^2 L_3 C_3}. \tag{4.4}$$

$$Z_{eq} = s\frac{k_{13}^2 L_1}{1 - \left(\frac{\omega}{\omega_n}\right)^2}. \tag{4.5}$$

$$L_{eq} = \frac{k_{13}^2 L_1}{1 - \left(\frac{\omega}{\omega_n}\right)^2}. \tag{4.6}$$

In order to improve the amplifier's $\mathrm{IP_{1dB}}$ at the low end of the 5G band, the notch of this transformer is designed to be at approximately 25 GHz. As a result, the parallel tank looks inductive at the signal frequencies between 17 and 21 GHz. Furthermore, the transformer can be represented by its equivalent T-model [49]. The resultant circuit model for the inter-stage matching network is shown in Figure 4.10. Here, the mutual inductance M is given by (4.7). The resistances R_1 and R_2 represent the series resistances of the primary and secondary coil respectively. The equivalent circuit in Figure 4.10 can be used to design the inter-stage matching network.

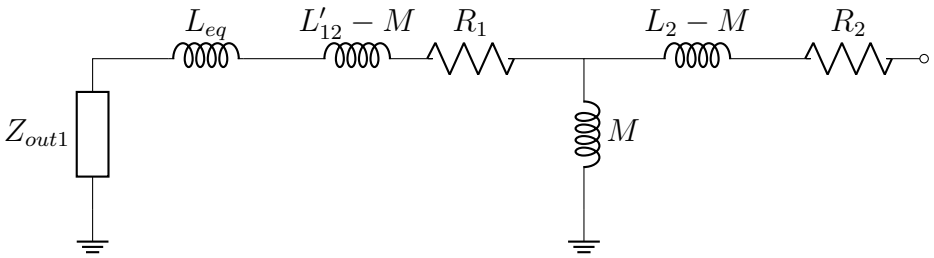


Figure 4.10: Simplified circuit of the LNA inter-stage matching network.

$$M = k''_{12}\sqrt{L'_{12}L_2}. \tag{4.7}$$

The output impedance Z_{out1} of the first stage, without any additional matching networks, is approximately 5 - j100 Ω at 20 GHz. An example trajectory taken by the impedance, using the equivalent circuit from Figure 4.10 is shown in Figure 4.11. Point 1 indicates the start point, which is Z_{out1}, and the trajectory shows the steps to synthesize the desired second-stage source impedance of 4 + j4 Ω. First, the series inductor L_{eq} moves the impedance to point 2. Then, the series inductor $L'_{12} - M$ moves the impedance to point 3. Next, the loss of the primary coil, given by R_1, moves the impedance to point 4. Afterwards, the shunt inductance M moves the impedance along a constant admittance circle to point 5. Finally, the series inductance of the secondary coil, $L_2 - M$, moves the impedance to the target at point 6. The effect of R_2 on the matching is negligible and is not shown.

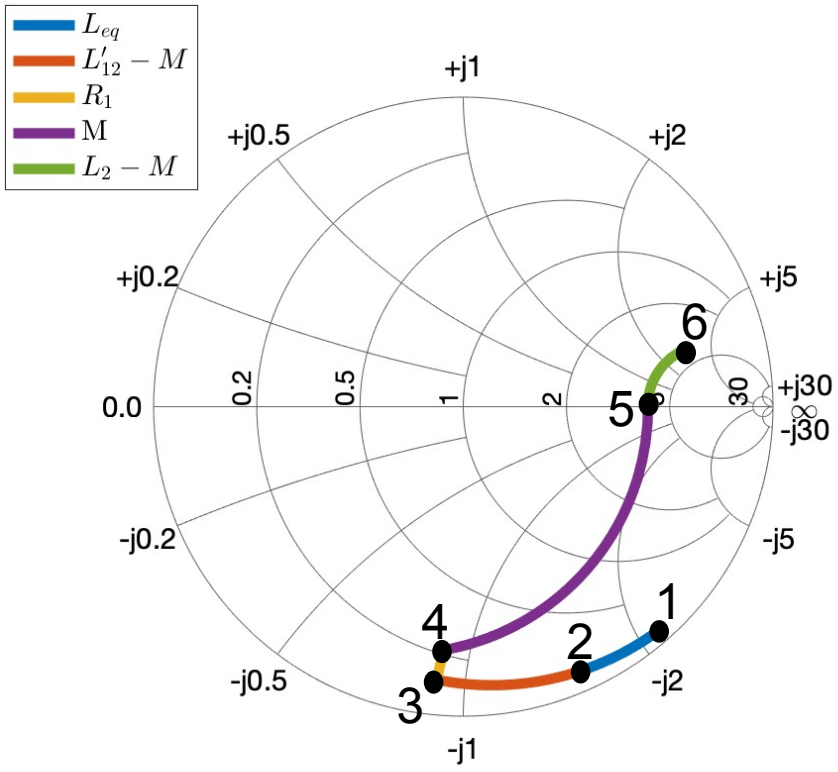


Figure 4.11: Example trajectory of Z_{out1} to the targeted second-stage source impedance.

The component values used in the trajectory in Figure 4.11 are shown in Table 4.1. These values can be used to calculate the physical inductances and magnetic coupling factors of the three-coil inter-stage transformer. Assuming an operating frequency of 20-GHz, a desired notch frequency f_n of 25 GHz, and then solving equations (2.7) to (2.10), (4.6), and (4.7) with the values from Table 4.1 gives an initial starting point for the physical transformer parameters. These values are shown in Table 4.2. All the physical parameters except L_3 and C_3 are determined in this way. L_3 must be determined by experimental EM simulations that give bounds on what values are possible while still satisfying the required k_{13}, given the geometry of the transformer. Finally, given L_3, the value of C_3 can be solved for from (2.11) knowing that the desired notch frequency is 25 GHz.

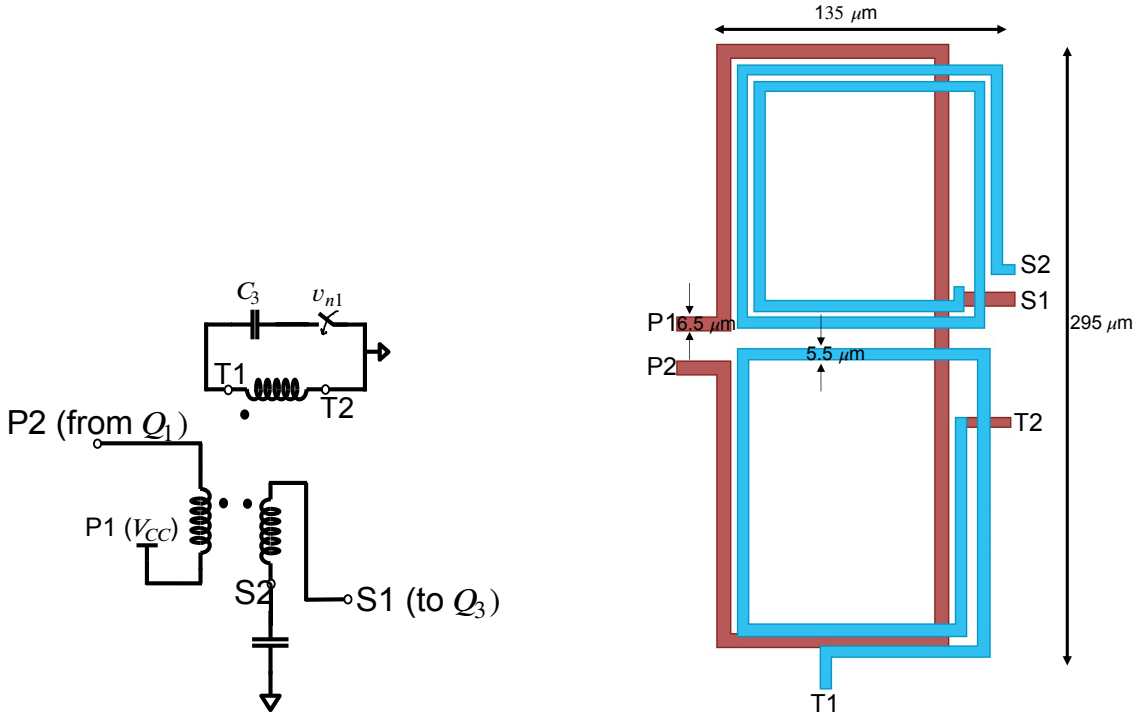
Table 4.1: Component values used in the matching trajectory of Figure 4.11.

Trajectory Step	Parameter	Value
1 to 2	L_{eq}	240 pH
2 to 3	$L'_{12} - M$	225 pH
3 to 4	R_1	5 Ω
4 to 5	M	360 pH
5 to 6	$L_2 - M$	1100 pH

Table 4.2: Initial calculated physical values for the inter-stage transformer.

Component	Initial Value	Optimized Value
L_1	670 pH	907 pH
L_2	1.46 nH	1.7 nH
L_3	N/A	692 pH
C_3	N/A	55 fF
k_{12}	0.34	0.49
k_{13}	0.36	0.36

The model in Figure 4.10 is not adequate for higher frequencies because it does not take into account the parasitic capacitances of the transformer, such as in the double-π model [20]. Therefore, it only serves to provide an initial guess for the transformer's values. The final transformer is obtained through optimization with electromagnetic simulations. The physical structure of the optimized transformer is shown in Figure 4.12b, with its ports defined as in Figure 4.12a. The transformer is implemented on the top two thick aluminium layers (AM and LY in Figure 4.5a), and its optimized values are given in Table 4.2.



(a) Transformer port definitions.

(b) Transformer physical structure.

Figure 4.12: The second stage notch and its small-signal equivalent circuit.

4.1.4 Analysis of the Novel Second-Stage Notch

In addition to the first notch introduced by the 3-coil inter-stage transformer, the second stage degeneration transformer (consisting of coupled inductors L_{e2} and L_{c2} in Figure 4.1) also adds a notch to the frequency response. This section will analyze the second-stage circuit and solve for the notch frequency ω_n. It will also provide an analysis for the gain of the stage. The second stage circuit and its small-signal equivalent is shown in Figure 4.13. In the small-signal equivalent, the load inductor and capacitor are lumped into a single load impedance, Z_L.

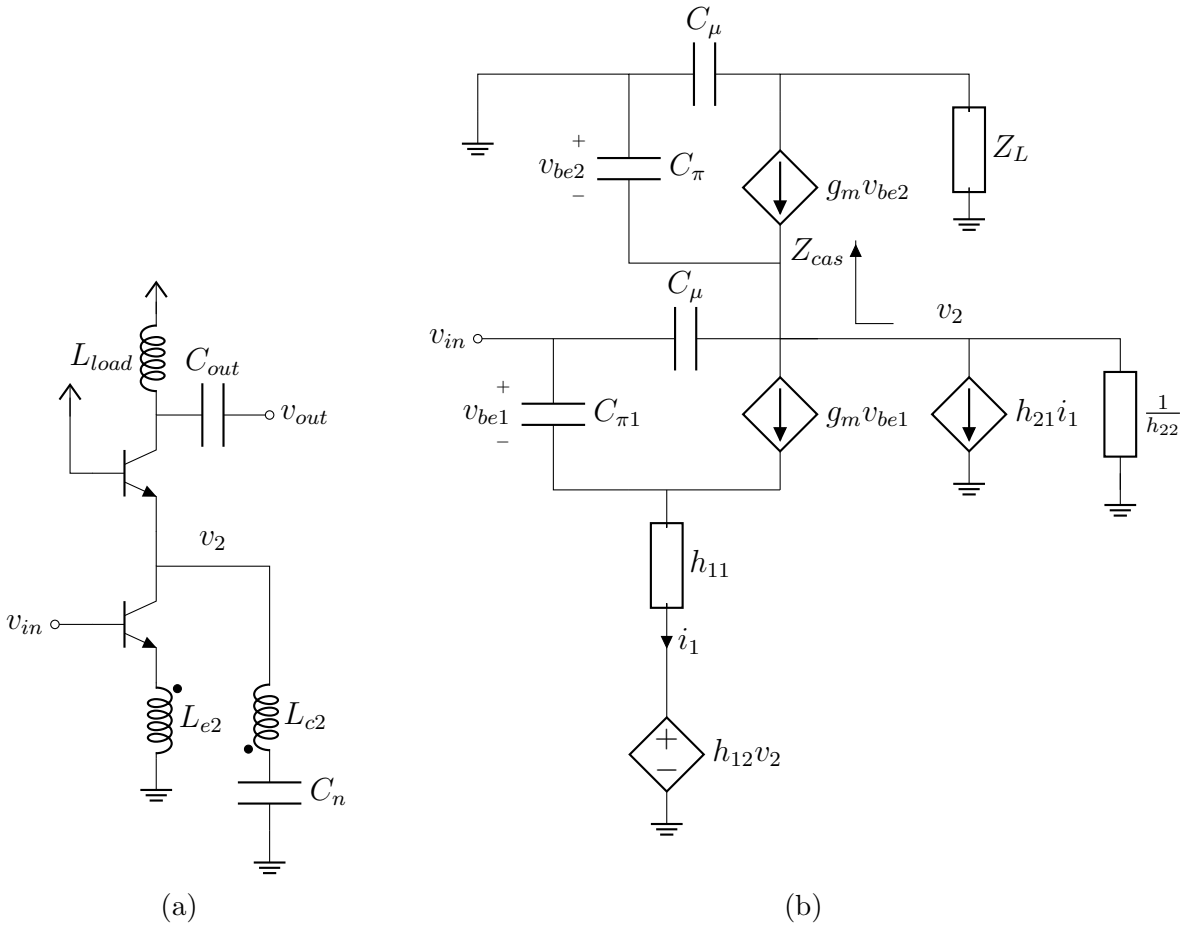


Figure 4.13: The second stage notch. (a) Second-stage schematic. (b) Small-signal equivalent.

The circuit is similar to the drain-source transformer feedback LNA topology introduced in [50]. A similar analysis will be used for the second stage notch. First, as shown in Figure 4.13b, the feedback network consisting of L_{e2}, L_{c2}, and C_n can be represented by an equivalent H-parameter network.

Derivation of the notch frequency

For a first-order analysis, we can ignore the effect of C_μ. For a 4x0.12 μm^2 HBT biased at 2 mA, C_π is 36 fF while C_μ is 6 fF. The zero frequency of the voltage gain can be derived as

the frequency at which $v_2 = 0$, which leads to $v_{be2} = 0$, which leads to no current developed across the load Z_L. This condition occurs when the current due to the transconductor, $g_m v_{be1}$, is completely supplied by the feed-forward current, $h_{21} i_1$. This condition can be expressed as in (4.8).

$$g_m v_{be1} = -h_{21} i_1. \tag{4.8}$$

(4.8) can be simplified, and the expression for h_{21} from (A.8) in Appendix A can be substituted to give:

$$g_m v_{be1} = -h_{21} v_{be1} (g_m + \frac{1}{Z_\pi}). \tag{4.9}$$

$$g_m = -h_{21} (g_m + \frac{1}{Z_\pi}). \tag{4.10}$$

$$g_m = \frac{\omega_n^2 M C_n}{1 - \omega_n^2 L_{c2} C_n} (g_m + \frac{1}{Z_\pi}). \tag{4.11}$$

In (4.9) - (4.11), Z_π is $\frac{1}{sC_\pi}$ and ω_n is the notch frequency, i.e., the frequency at which the voltage gain is 0. At 24 - 30 GHz, for the HBTs available in the BiCMOS 8XP technology, it is reasonable to assume that $g_m >> \frac{1}{Z_\pi}$. This assumption is reasonable because it can be approximately re-expressed as $f << f_T$ by substituting $\frac{g_m}{2\pi C_\pi}$ for f_T [20]. For the second-stage transistors, f_T is about 200 GHz at their chosen bias point, so it is reasonable to make this approximation at 24 to 30 GHz. Therefore, (4.11) simplifies to

$$g_m = \frac{\omega^2 M C_n}{1 - \omega_n^2 L_{c2} C_2} g_m. \tag{4.12}$$

The g_m on each side of (4.12) cancels, and we can solve for ω_n as in (4.13).

$$\omega_n = \frac{1}{\sqrt{(L_{c2} + M) C_n}}. \tag{4.13}$$

(4.13) shows that the addition of the coupling between L_{e2} and L_{c2} shifts the notch frequency from $\omega_n = \frac{1}{\sqrt{L_{c2} C_n}}$ to $\omega_n = \frac{1}{\sqrt{(L_{c2}+M) C_n}}$. Effectively, it increases the inductance of the notch by M, without adding any loss. Therefore, the quality factor (Q) of the notch is improved.

The improvement in Q can be quantified by defining the 'original' quality factor, Q_0, as the Q of the just the secondary coil, given by (4.14), where R_s is the series resistance of L_{c2}.

$$Q_0 = \frac{\omega L_{c2}}{R_s}. \tag{4.14}$$

With the coupling factor, the new quality factor becomes

$$Q = \frac{\omega(L_{c2} + M)}{R_s}. \tag{4.15}$$

The relative improvement in Q can then be calculated as in (4.16), where k is the coupling factor of the transformer and $n = \sqrt{\frac{L_{c2}}{L_{e2}}}$ is the turns ratio. For example, in this work, k is 0.61 and n is 1.8, giving an improvement in Q of 34%.

$$\frac{Q}{Q_0} = \frac{L_{c2} + M}{M} = 1 + \frac{k}{n}. \tag{4.16}$$

(4.16) suggests that a higher coupling factor will give a higher Q of the notch. However, a higher-Q notch will also have a narrower-band frequency response. Therefore, the coupling cannot be made so high that the small-signal rejection does not cover enough bandwidth.

Gain Analysis

The equivalent circuit in Figure 4.13b can be used to create a signal flow diagram, shown in Figure 4.14, similarly to the transformer feedback analysis conducted in [50].

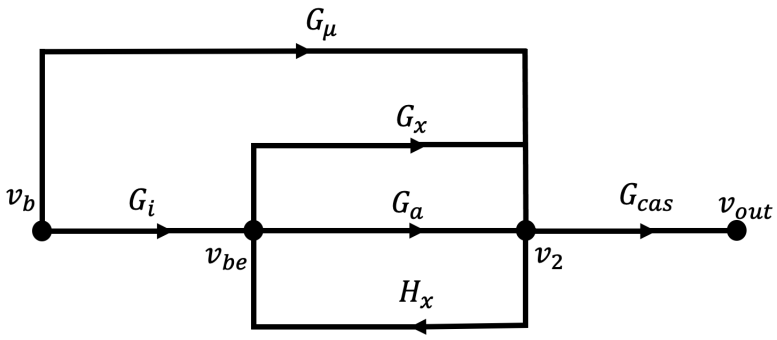


Figure 4.14: Signal flow diagram of the second stage with the degeneration notch.

The expressions for each gain/feedback term of the block diagram are given by (4.17) - (4.23) [50]. G_a and G_x can be thought of the two components of the forward gain, given by (4.24). G_i is the input gain from v_{in} to v_{be}, and H_x is the feedback gain from the intermediate node v_2 to v_{be}. Finally, G_μ can be thought of as the feed-forward gain due to C_μ.

$$G_i = \frac{v_{be}}{v_{in}}\Big|_{v_2=0} = \frac{Z_\pi}{Z_\pi + h_{11}\left(g_m Z_\pi + 1\right)}. \tag{4.17}$$

$$G_a = -g_m\left(Z_{cas}||Z_\mu||\frac{1}{h_{22}}\right). \tag{4.18}$$

$$G_x = -h_{21}\left(g_m + \frac{1}{Z_\pi}\right)\left(Z_{cas}||Z_\mu||\frac{1}{h_{22}}\right). \tag{4.19}$$

$$H_x = \frac{v_{be}}{v_2}\Big|_{v_b=0} = -h_{12}\frac{Z_\pi}{Z_\pi + h_{11}\left(g_m Z_\pi + 1\right)}. \tag{4.20}$$

$$G_\mu = \frac{Z_{cas}||\frac{1}{h_{22}}}{Z_\mu + Z_{cas}||\frac{1}{h_{22}}}. \tag{4.21}$$

$$G_{cas} = \frac{v_{out}}{v_2}\Big|_{v_b, v_{be}=0} = g_m\left(Z_L||\frac{1}{sC_\mu}\right). \tag{4.22}$$

$$Z_{cas} = \frac{1}{g_m}||Z_\pi. \tag{4.23}$$

$$G_{forward} = \frac{v_2}{v_{be}}\bigg|_{v_b=0} = G_a + G_x. \tag{4.24}$$

The signal flow graph can be simplified with Mason's rule [37, p. 196], yielding the equation for the voltage gain in (4.25). If C_μ is assumed to be 0, from (4.21) this corresponds to $G_\mu = 0$. Then, setting A_V to 0 yields the condition $G_a = -G_x$, which can be shown to simplify to (4.10). Therefore, the condition $G_a = -G_x$ can be used as a more general method of deriving the notch frequency.

$$A_V = G_{cas}\frac{G_\mu + G_i(G_a + G_x)}{1 - H_x(G_a + G_x)}. \tag{4.25}$$

(4.25) can be used to consider the effect of C_μ on the notch frequency. At the notch frequency, $G_a + G_x = 0$, so then A_V simplifies to,

$$A_V\Big|_{\omega=\omega_n} = G_\mu G_{cas}. \tag{4.26}$$

(4.26) shows that the non-zero C_μ imposes an upper bound on the gain that can be achieved at the notch frequency. Therefore, in order to maximize the rejection, the second stage transistors should be sized and laid out to minimize C_μ. This was achieved in the second stage by choosing relatively small devices (4 μm), and by avoiding overlap between base and collector metals in the layout.

(4.25) also shows that the feedback gain, H_x, reduces the gain of the stage. (4.20) shows that H_x depends on h_{12}, which, from (A.5), depends on the mutual inductance, M. Therefore, more mutual inductance, given by a higher coupling factor k of the transformer,S will reduce the gain of the stage. However, as shown in (4.16), a higher k is desirable for a higher Q enhancement of the notch. Therefore, there is a trade-off between gain and out-of-band rejection using this feedback technique.

Second-Stage Model Verification

To verify the model derived in this section, the voltage gain, given by (4.25), was calculated using the values in Table 4.3. The transistor parameters (C_π, C_μ, and g_m) were extracted from the DC operating point of the second-stage devices. For comparison, the second-stage was also simulated with the HBT models provided by the process development kit (PDK). The comparison is shown in Figure 4.15. The model has higher gain than the simulation

at frequencies away from the notch. This discrepancy could be due to additional parasitics in the PDK transistor model that are not included in the model in Figure 4.13b, such as the base and collector resistances.

Table 4.3: Values used to verify the second-stage model.

Parameter	Value
g_m	68 mS
C_π	37.4 fF
C_μ	6.8 fF
L_{e2}	157 pH
L_{c2}	417 pH
M	156 pH
k_n	0.61
L_{load}	750 pH
C_{out}	75 fF
Q_3 and Q_4	4x0.12 μm^2

Both the model and the PDK simulation show a notch at 28.6 GHz. This notch frequency is different from what (4.13) would yield, which is 28.35 GHz. Another discrepancy is that the gain at the notch frequency is greater than $G_u G_{cas}$, whereas the model predicted that they would be equal. These two discrepancies can be attributed to the approximation that $g_m >> \frac{1}{Z_\pi}$ that was made in the derivation of (4.13).

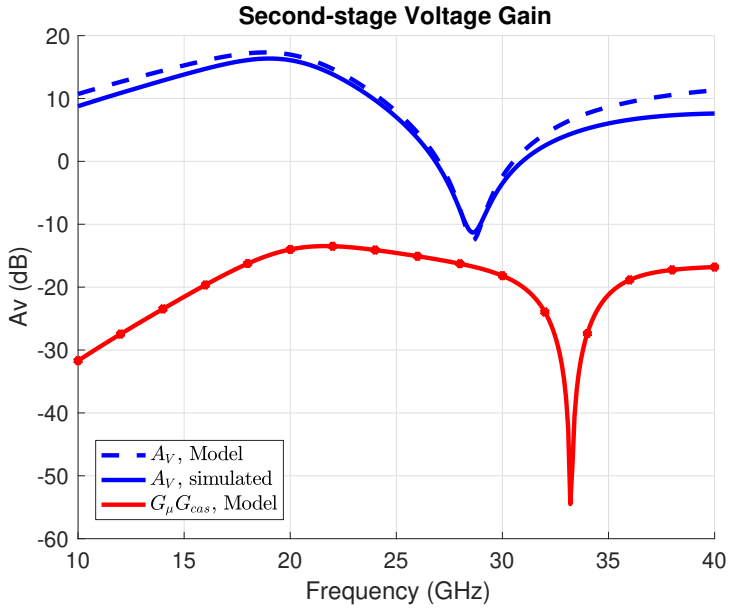
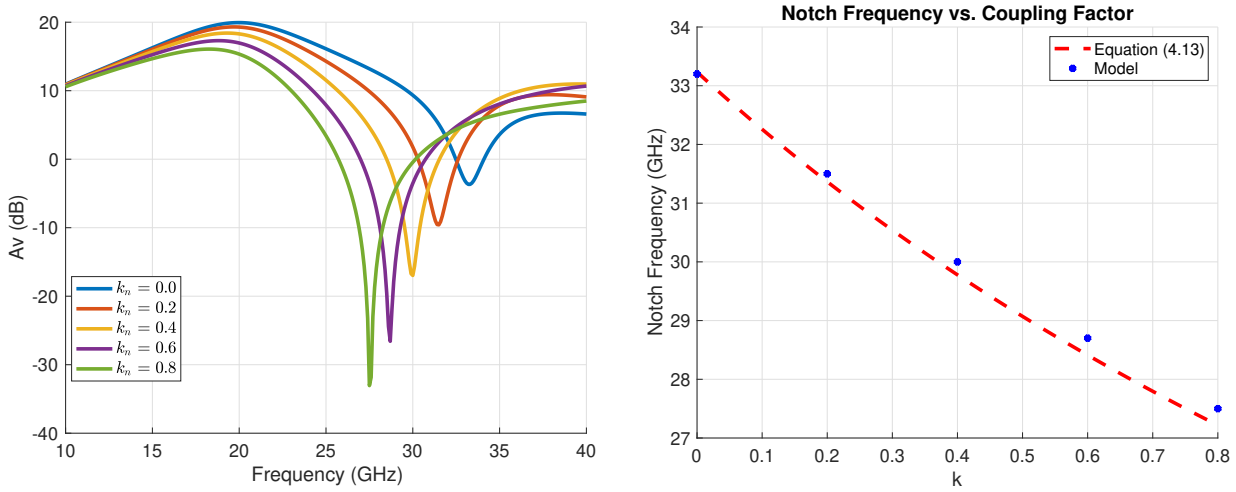


Figure 4.15: Comparison between the second-stage voltage gain as predicted by the model vs. simulation of HBTs.

As predicted by (4.13), the notch frequency depends on the mutual inductance, M. This prediction was verified by varying the coupling factor, k, in (4.25). The frequency response of the voltage gain versus k is shown in Figure 4.16a, and the notch frequency (defined as the frequency of the minimum voltage gain) is compared to the notch frequency as calculated by (4.13) in Figure 4.16b.



(a) (b)

Figure 4.16: Second-stage notch behaviour versus coupling factor k. (a) Frequency response of A_V. (b) Location of notch frequency.

(4.16) suggests that the quality factor of the notch can be improved by increasing the coupling factor k. This property were verified by fixing the notch frequency, f_n, to 28 GHz, and varying k. With all other parameters the same as in Table 4.3, the notch capacitor, C_n, was adjusted to maintain the same f_n for each value of k by setting it to

$$C_n = \frac{1}{4\pi^2 f_0^2 \left(L_{c2} + M\right)}. \tag{4.27}$$

Figure 4.17 shows the voltage gain with the fixed notch frequency versus k. As k increases, the gain at the notch frequency also decreases, verifying the prediction that the effective Q is improved. The trade-off is that there is that in-band gain also decreases. This trade-off was also predicted to occur because the increased k means a higher h_{12}, leading to a higher magnitude of the feedback term H_x.

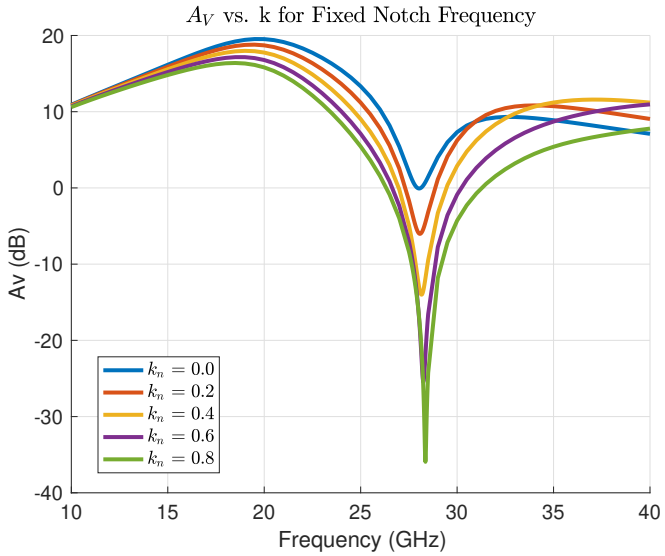


Figure 4.17

4.1.5 Simulation Results

Figure 4.18 shows the final layout of LNA Design 1 from Figure 4.1. The layout includes the pads for probing. Figure 4.18 also shows the location of the transformers. T_1 is the input matching transformer, T_2 is the 3-coil inter-stage transformer, and T_3 is the second-stage degeneration transformer. Decoupling capacitors are implemented using dual metal-insulator-metal capacitors, and are placed near the V_{CC} connections of each stage. The ground plane is implemented with a mid-level copper layer (MQ in Figure 4.5a), shown in dark blue in Figure 4.18. The LNA consumes a total of 13.8 mW from a 1.8 V supply.

The LNA's performance was simulated by performing electromagnetic simulation on the final layout using Cadence EMX^{TM}3. The simulation ports were placed at the pads, and interconnect parasitics due to probes or wire-bonds were modeled by adding a 1 nH inductance to the DC and bias pads (v_{b1}, v_{b2}, V_{CC}, v_{c1}, and v_{c2}) in simulation. Figure 4.19a shows the simulated small-signal gain, input return loss, and output return loss of Design 1. The peak gain is 28.8 dB at 19.4 GHz, and is greater than 24 dB between 17.7 and 21.2 GHz. The input return loss S_{11} is less than -10 dB from 15 to 30 GHz due to the wideband input transformer matching. The output return loss S_{22} is less than -10 dB between 17.65 and 20.8 GHz. The output return loss is more narrow-band than the input return loss because of the single-section LC matching topology used in the second stage. The noise figure is shown in Figure 4.20. The minimum noise figure is 1.85 dB at 18.3 GHz

and it is less than 2.25 dB between 17.7 and 21.2 GHz. The gain between 24 and 30 GHz is less than 7.1 dB, giving a small-signal rejection of 21.7 dB from the peak gain.

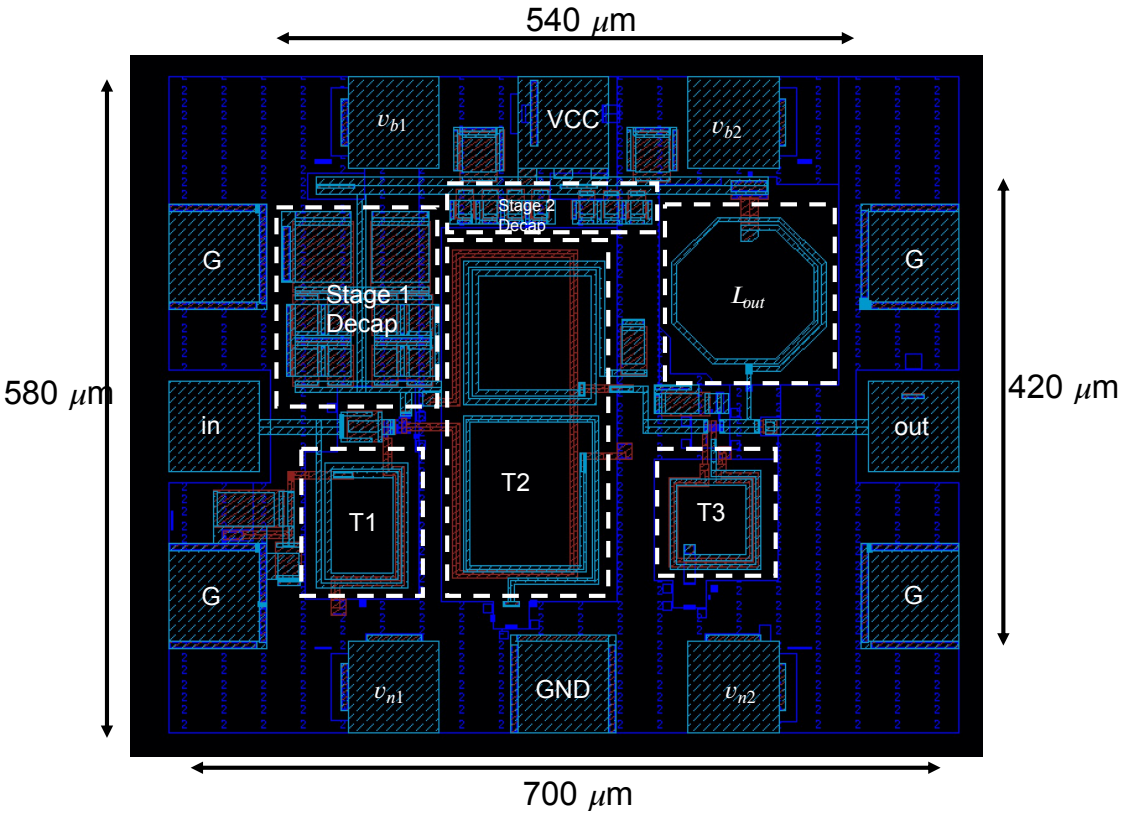
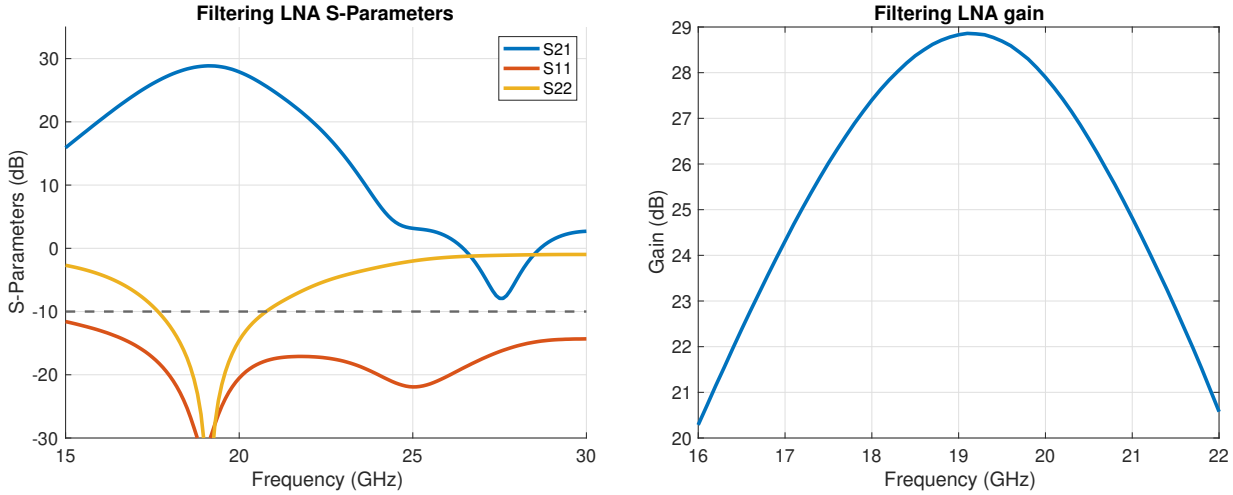


Figure 4.18: Filtering LNA layout. Only the top 3 metals are displayed.



(a) (b)

Figure 4.19: (a) Filtering LNA s-parameters for v_{n1} and v_{n2} = 1.2 V. (b) Zoomed in plot of the LNA gain.

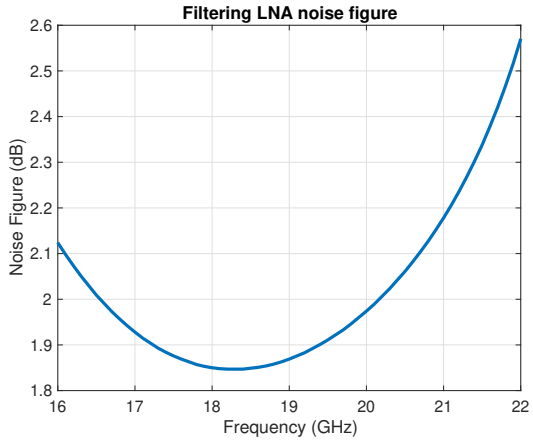


Figure 4.20: Filtering LNA noise figure with v_{n1} and v_{n2} set to 1.2 V.

Figure 4.21 shows the s-parameters and noise figure of the filtering LNA for the four notch control voltage states. The gain plot, shown in Figure 4.21a, shows that as the notches are disabled, the LNA gain flatness near the Satcom band improves because the notches are pushed to a higher frequency. Figure 4.21b shows that the second-stage notch

does not affect S_{11} while the first stage notch does cause a shift in some of the resonances. However, in all cases, the amplifier remains well matched across a wide bandwidth.

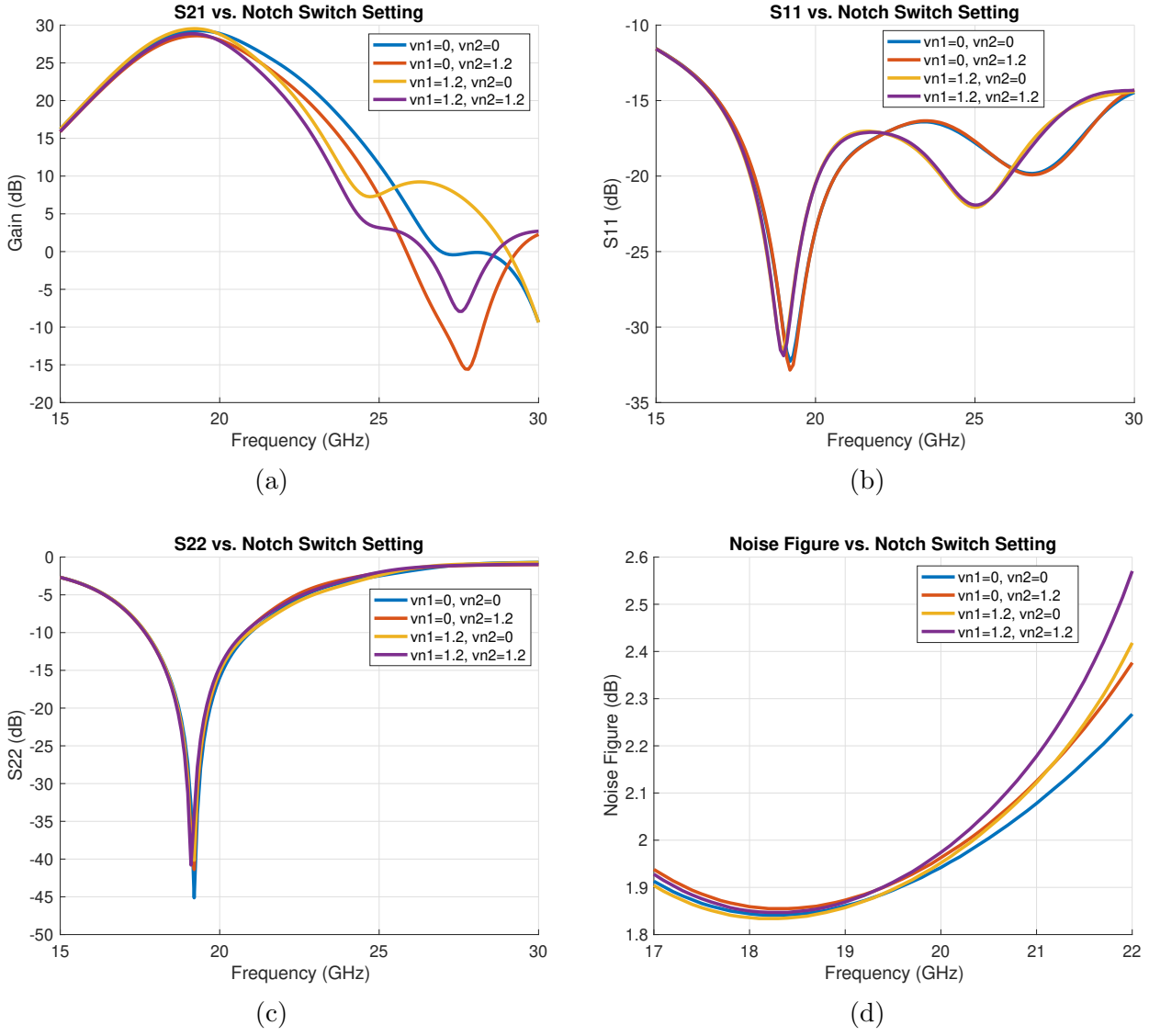


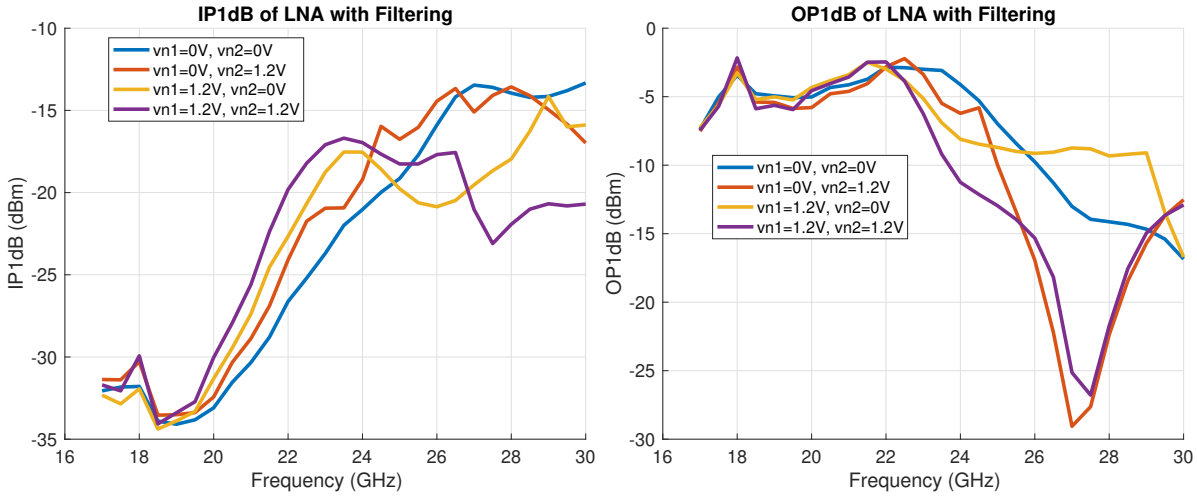
Figure 4.21: Filtering LNA small-signal results vs. notch control voltages. (a) S_{21}, (b) S_{11}, (c), S_{22}, (d) Noise figure.

Figure 4.21c shows that the notch settings have almost no effect on the S_{22}. Finally, Figure 4.21d shows that the state of the notches at mid-band, around 19 GHz, has minimal

effect on the noise figure. At the edge of the band between 20 and 21 GHz, disabling the notches improves the noise figure, e.g. from 2.18 dB to 2.08 dB at 21 GHz. This improvement is due to the higher gain at the edge of the band in both stages as the notches are disabled.

Figure 4.22 shows the large-signal simulation results of the LNA with filtering for the four different notch states. Figure 4.22a shows that in all cases, the out-of-band IP_{1dB} is greater than -23 dBm from 24-30 GHz in all the states, and can be increased to -14 dBm in the 27-30 GHz band by disabling the first stage notch (i.e. setting v_{n1} to 0 V). Disabling the first stage notch improves the IP_{1dB} within this band because the inter-stage notch moves from 24 GHz to 28 GHz. This shift happens due to the notch capacitor appearing in series with the switch's off capacitance, reducing the effective notch capacitance and pushing the notch to a higher frequency.

The OP1dB of the filtering LNA is shown in Figure 4.22b. With both notches enabled, the OP1dB is less than -11 dBm between 24 and 30 GHz, reaching a minimum of -29 dBm at 27 GHz. This low OP1dB means that the LNA will deliver a low power to any blocks that come after it in the receiver, which will ease the out-of-band linearity requirements of those blocks.



(a) (b)

Figure 4.22: Large signal simulation results of the LNA with filtering. (a). Input 1-dB compression point (IP_{1dB}). (b). Output 1-dB compression point (OP1dB)

Figure 4.23 shows the IIP_3 vs. frequency for Design 1. At each frequency, the IIP_3 was simulated with one tone at the center frequency, and another 10 MHz away from the

center frequency. For example, the IIP_3 at 20 GHz was simulated with one tone at 20 GHz and another at 20.01 GHz, and extrapolating the power at 19.99 GHz. Between 24 and 30 GHz, the IIP_3 is greater than -11 dBm, which is about 10 dB higher than the IP_{1dB} as expected.

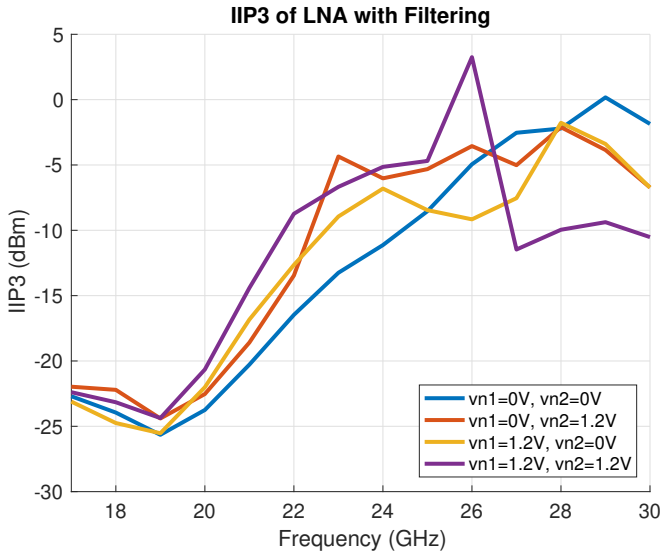


Figure 4.23: IIP_3 vs. frequency of Design 1.

The gain flatness vs. frequency of the LNA is also shown in Figure 4.24. When both notches are enabled, the gain flatness is less than 3 dB/GHz between 17.5 and 20.2 GHz. With the notches disabled, it is less than 3 dB/GHz up to 21.2 GHz. Therefore, as discussed in Section 3.2.3, the LNA can support 100 MHz signal bandwidths with center frequencies at the edges of the Satcom band.

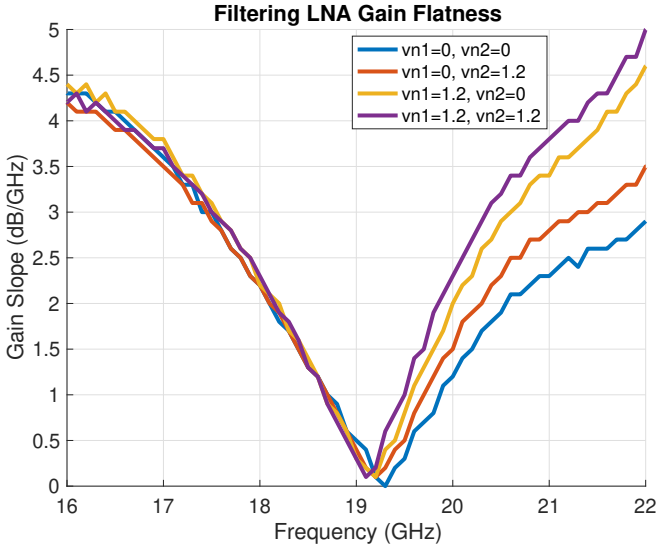


Figure 4.24: Gain flatness vs. frequency for the filtering LNA for the different tuning states.

Stability

Both stages of the LNA shown in Figure 4.1 have feedback networks. The first stage uses transformer feedback for input matching while the second stage uses feedback-based active filtering. Therefore, it is important to check the stability of both stages on their own, as well that of the cascaded amplifier.

The stability of a single-stage amplifier can be verified by checking the μ-factor, given by [37],

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1, \tag{4.28}$$

where Δ is given by,

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1. \tag{4.29}$$

For a multi-stage amplifier, it is necessary to verify this condition for each stage, with and without the inter-stage matching networks. The condition should also be checked for the cascade of the multiple stages. The simulated μ-factors of Design 1 are shown in Figure

4.25. The plot show that the stability condition is satisfied for both stages, as well as the full amplifier.

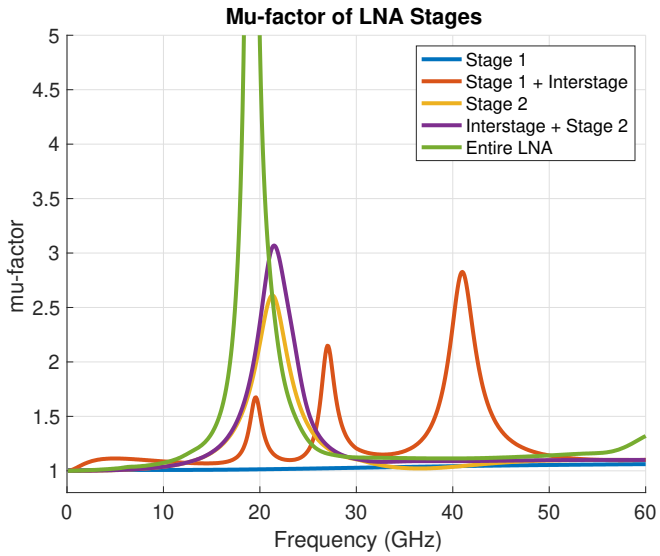
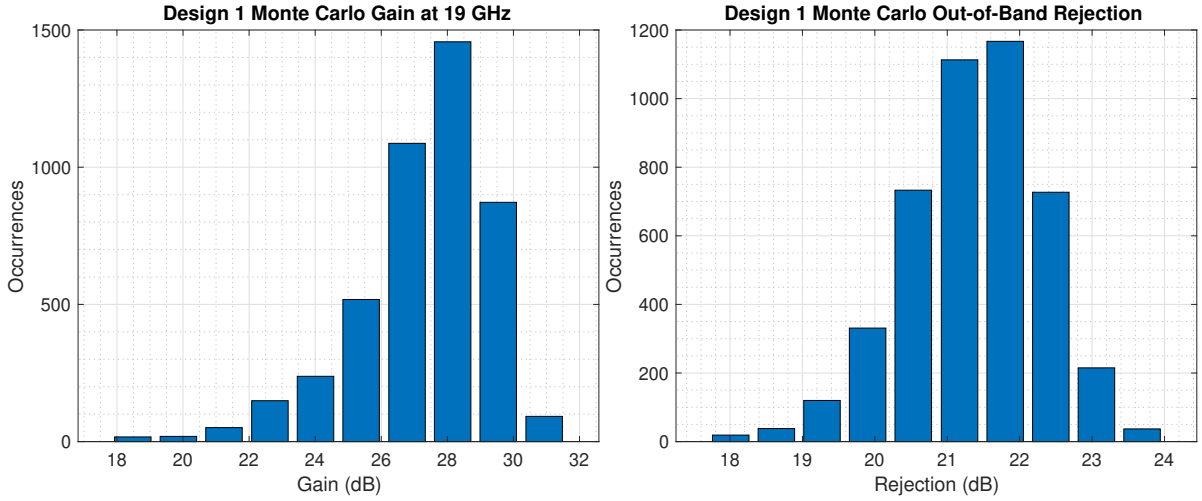


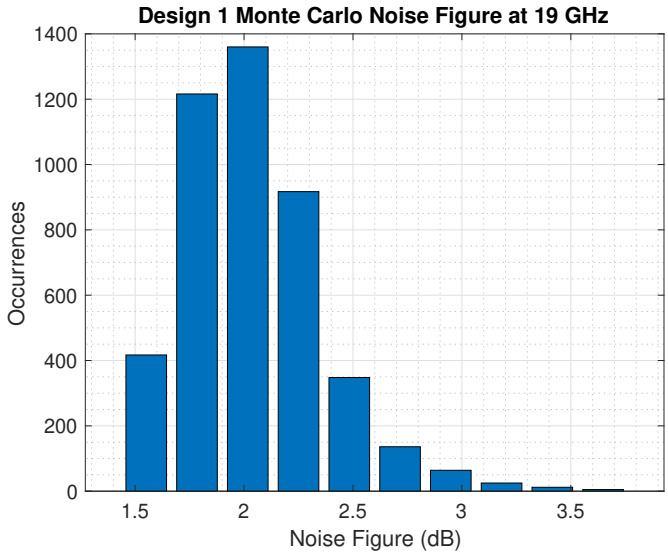
Figure 4.25: μ-factor of each stage, as well as the full ampliifer, for Design 1.

Effects Process Variations

In order to investigate the effects of process, voltage, and temperature (PVT) variations, Monte-Carlo simulations were performed on Design 1. The Monte-Carlo simulation involved 500 iterations across all corners, with the supply voltage varying ±10 %, and temperatures of 25, 55, and 85 °C. The results are shown in Figure 4.26. Figure 4.26a shows the gain of the amplifier at 19 GHz. The overall variation is more than 10 dB, and 10% of iterations had a gain less than 25 dB. Figure 4.26b shows the out-of-band small-signal rejection, defined as the difference between the gain at 19 GHz and 24 GHz. There is a 6-dB variation in the range of rejection, but the rejection is less than 20 dB in only 4% of iterations. Finally, Figure 4.26c shows the distribution of the noise figure at 19 GHz. The noise figure varies between 1.5 and 3.5 dB, but it is only greater than the targeted specification of 2.5 dB in 5% of iterations.



(a) (b)



(c)

Figure 4.26: Monte-Carlo simulation results of Design 1. (a) Gain at 19 GHz. (b) Small-signal rejection between 19 GHz and 24 GHz. (c). Noise figure at 19 GHz.

4.2 Design 2: A Single-Ended to Differential LNA with Satcom Self-Interference Rejection

This section presents and LNA that was designed to only reject Satcom self-interference. This design represents an alternative application case where it is not expected that 5G wireless signals present a serious source of interference. An example application case could be in a rural area where the 5G infrastructure is not as developed as it would be in an urban area, but Satcom arrays are used for internet connectivity. Section 4.2.1 shows the schematic and component values of the LNA, and section 4.2.2 shows its simulation results.

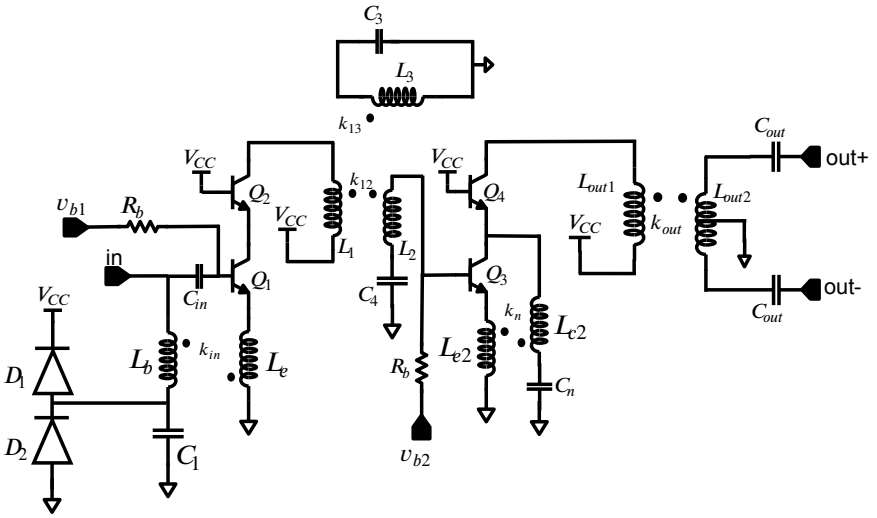
4.2.1 Amplifier Schematic

Figure 4.27 shows the schematic of the LNA. It is similar to the LNA presented in Section 4.1. The first difference between the two designs is that both notches were tuned to be at 27-30 GHz rather than spread between 24 and 30 GHz. The other difference is that the output matching of this LNA is a transformer balun that converts the signal from single-ended to differential. In addition to the different output matching, there are no output pads. The reason for this change in the output is that this LNA is intended for a full beamformer receiver, so its output is designed for a phase shifter to come after it.

Another change made in Design 2 is the device sizes. Both stages uses HBTs with emitter areas of 16x0.12μm^2. Larger second stage devices were chosen to improve the linearity of the LNA. To compensate for the extra power consumption of the larger second-stage devices, smaller devices were needed in the first-stage as well.

Another difference between the two designs is that this LNA does not include tuning switches for the notches as in the LNA of Section 4.1. The reason for this is that 5G wireless interference is expected to be intermittent depending on the receiver's proximity to a 5G base station. Therefore, adding tunability in Design 1 allowed it to recover some of the noise figure degradation due to the 24-26 GHz filtering. On the other hand, it is expected that Satcom self-interference would always be present, and the frequency of the interferer is farther from the Satcom downlink signal at 17.7 - 21.2 GHz. Therefore, there is less benefit to be gained from adding tunability.

The layout of the LNA is shown in Figure 4.28. The layout of Design 2 is different from Design 1. The focus in this layout was for a more compact design to save chip area in a Satcom receiver channel. The DC pad for v_{b2} is not shown as it is outside of the main area of the LNA in the receiver chain.



L_b	753 pH	L_{e2}	157 pH
L_e	127 pH	L_{c2}	417 pH
k_{in}	0.45	k_n	0.61
C_1	5x1 pF	C_n	55 fF
Q_1	16x0.12 μm^2	L_{out1}	1 nH
Q_2	16x0.12 μm^2	L_{out2}	840 pH
L_1	718 pH	k_{out}	0.68
L_2	530 nH	C_{out}	64 fF
k_{12}	0.4	R_b	10 kΩ
L_3	270 pH	v_{b1}	0.89 V
k_{13}	0.38	v_{b2}	0.88 V
C_3	66 fF	V_{CC}	1.8 V
C_4	2 pF		
Q_3	16x0.12 μm^2		
Q_4	16x0.12 μm^2		

Figure 4.27: Schematic and component values for Design 2.

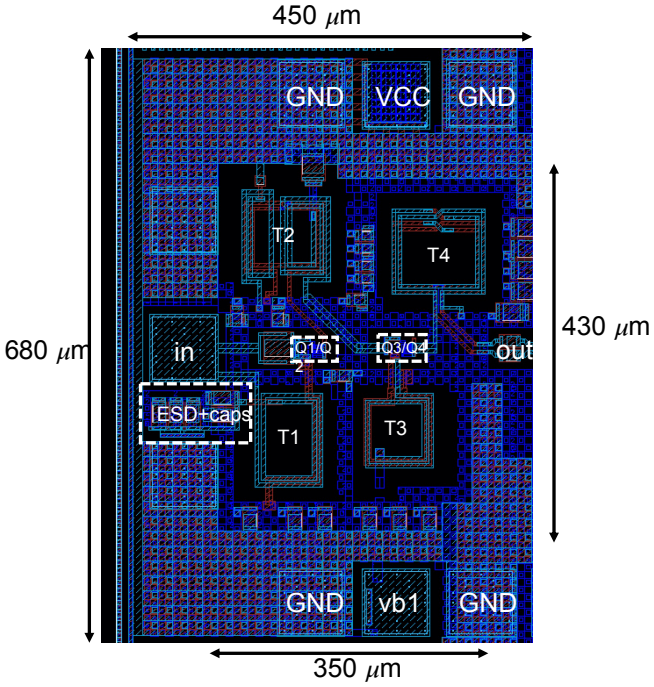


Figure 4.28: Layout of Design 2.

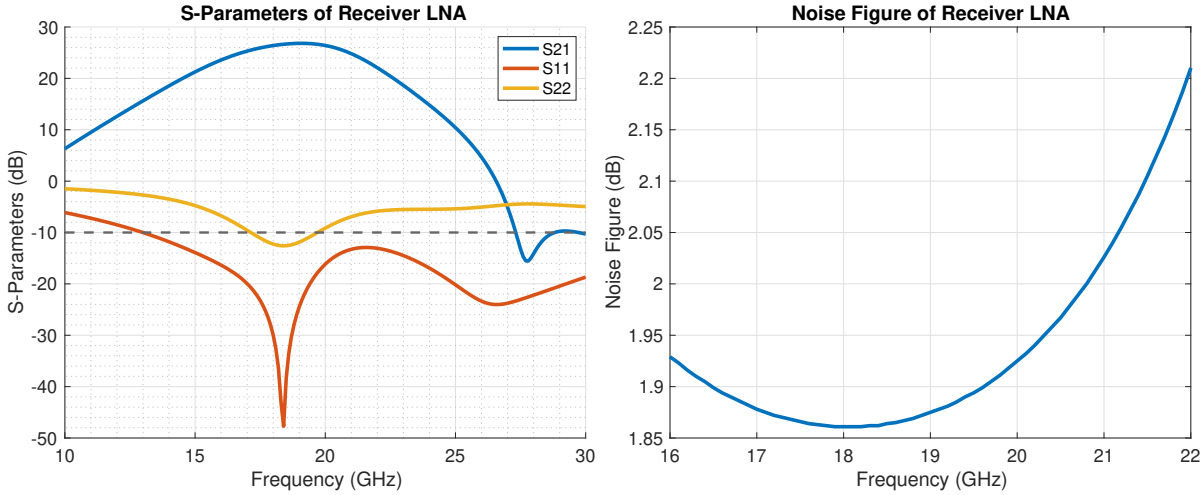
4.2.2 Simulation Results

Similarly to Design 1, Design 2 was EM-simulated with Cadence EMX^{TM}. Simulation ports were placed at the input pads for the RF input, and on the output signal lines for the output ports. To model wirebond inductance, ideal 1-nH inductors were connected, in post-layout simulation, to the DC pads. Figures 4.29a and 4.29b shows the s-parameters and noise figure of the LNA respectively. The gain reaches a peak of 26.8 dB at 19 GHz, and is less than -5 dB from 27-30 GHz. The S_{11} is well-matched across the entire band. The S_{22} is not well matched to 50 Ω. It is less than -10 dB between 17 and 19.7 GHz. The poor S_{22} is due to insufficient optimization of the output matching network. The amplifier consumes 14.9 mW of DC power from a 1.8 V supply.

Figure 4.30a shows the gain flatness of the Design 2 LNA. The gain flatness is less than 2.5 dB/GHz between 17.7 and 21.2 GHz.

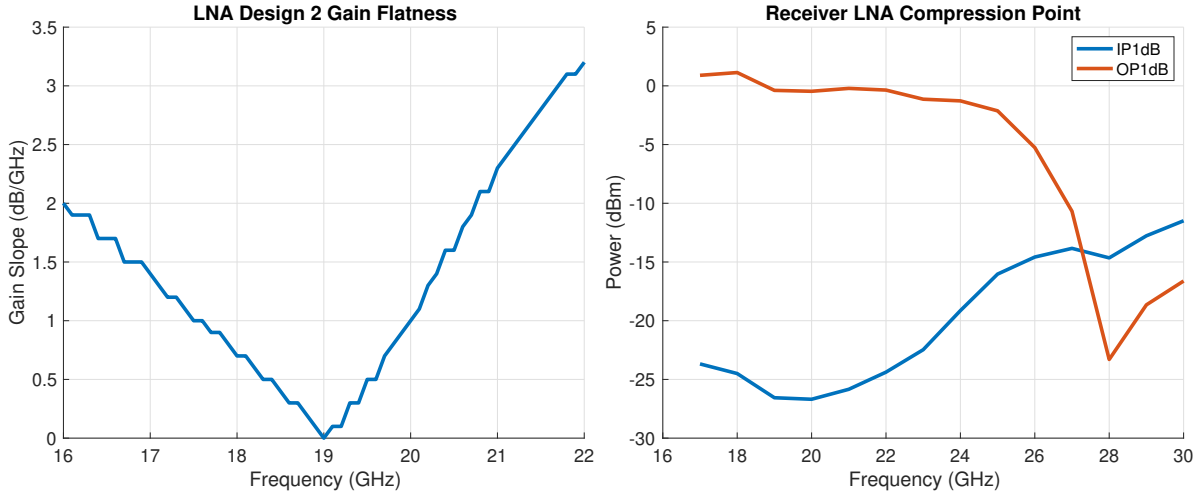
Since Design 2 has a differential output, the mismatch between the two outputs was simulated. There is 0.9 dB of magnitude mismatch, while the phase difference between the outputs deviates by less than 1° from 180° between 17.7 and 21.2 GHz. The high magnitude mismatch can be attributed to the asymmetrical layout of the output transformer.

Figure 4.30b shows the input and output compression 1-dB compression points of the LNA vs. frequency. The OP1dB is less than -14 dBm between 27 and 30 GHz, indicating that the block following the LNA must have an out-of-band IP_{1dB} of at least -14 dBm to avoid compressing during an interference event.



(a) (b)

Figure 4.29: (a) S-parameters and (b) noise figure of LNA 2.



(a) (b)

Figure 4.30: (a) Gain flatness of LNA 2. (b)IP_{1dB} and OP1dB of Design 2.

Figure 4.31 shows the IIP_3 vs. frequency for Design 2. The IIP_3 is defined similarly as in Design 1 (two tones with 10 MHz spacing at each frequency). Between 27 and 30 GHz, it is greater than -6 dBm, which is approximately 10 dB higher than the IP_{1dB} at each frequency.

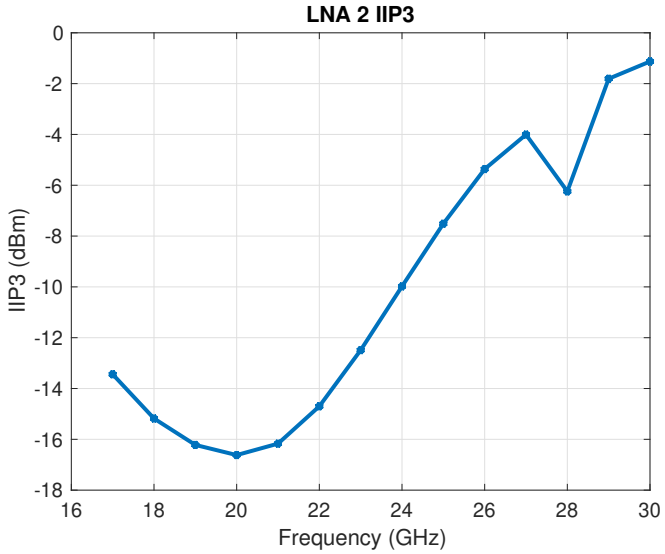


Figure 4.31: IIP_3 of Design 2 vs. frequency.

Figure 4.32 shows the simulated μ-factor of each stage of the amplifier, as well as the cascade of the stages. The μ-factor is greater than 1 between DC and 60 GHz, indicating unconditional stability.

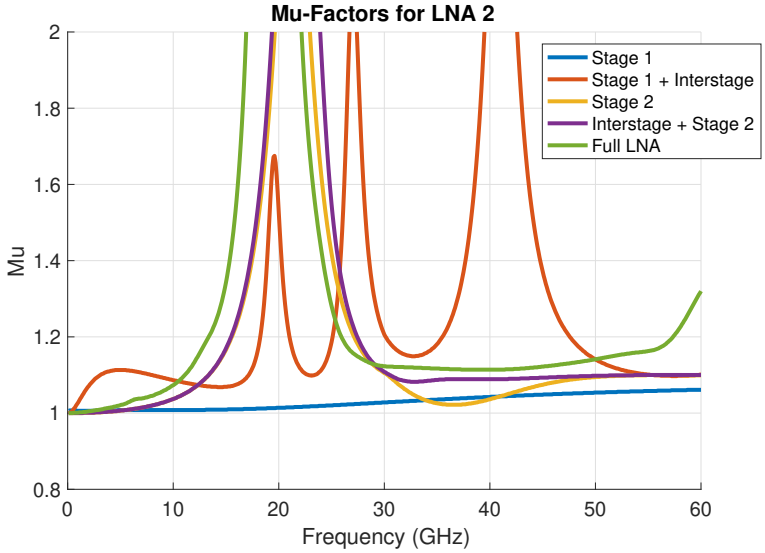


Figure 4.32: μ-factor of Design 2's stages as well as the full amplifier.

4.3 Summary of LNA Performance

Table 4.4 shows the summary of the targeted and achieved specifications of the LNAs designed in this chapter. Both designs meets the targeted gain, noise figure, gain flatness, in-band IP_{1dB}, in-band IIP_3, input return loss, DC power consumption, and chip area. Design 2 does not meet the targeted output return loss specification, as its output transformer was not sufficiently tuned after full EM simulation.

In terms of out-of-band IP_{1dB}, Design 1 achieves between -17 and -15 dBm depending on which notches are enabled, as shown in Figure 4.22. In some notch states, Design 1 does not meet the targeted IP_{1dB} of -16 dBm at 24-26 GHz. Similarly, between 27 and 30 GHz, the LNA in Design 1 achieves an IP_{1dB} of -15 to -14 dBm depending on the notch state used, which is above the targeted specification -18 dBm.

Design 2 also achieves an out-of-band IP_{1dB} greater than -15 dBm between 27 and 30 GHz, which is above the targeted specification. While it does not meet the target IP_{1dB} specification at 24-26 GHz, it was not designed for that frequency. Interestingly, even though Design 2 has a higher in-band IP_{1dB} than Design 1 (owing to the larger second-stage devices), that increase in linearity is not reflected in the out-of-band linearity, which is similar to that of Design 1.

Table 4.4: LNA specifications.

Specification	Target	Design 1	Design 2
Frequency	17.7 - 21.2 GHz	17.7 - 21.2 GHz	17.7 - 21.2 GHz
Gain	$>$ 25 dB	28.8 dB	26.8 dB
Small-signal rejection	$>$ 20 dB	$>$ 21.7 dB (24-30 GHz)	31.8 dB (27-30 GHz)
Noise Figure	$<$ 2.5 dB	$<$ 2.2 dB	$<$ 2.1 dB
In-Band Gain flatness	$<$ 3 dB/GHz	$<$ 3 dB/GHz	$<$ 2.5 dB/GHz
IP_{1dB} in-band	$>$ -40 dBm	$>$ -35 dBm	$>$ -30 dBm
IIP_3 in-band	$>$ -30 dBm	$>$ -25 dBm	>-17 dBm
IP_{1dB} at 24-26 GHz	$>$ -16 dBm	$>$ -17 dBm	$>$ -19 dBm
IP_{1dB} at 27-30 GHz	$>$ -18 dBm	$>$ -15 dBm	$>$ -15 dBm
Input Return Loss In-Band	$<$ -10 dB	$<$ -12 dB	$<$ -12 dB
Output Return Loss In-Band	$<$ -10 dB	$<$ -10 dB	$<$ -8 dB
DC Power Consumption	$<$ 15 mW	13.8 mW	14.9 mW
Chip Area	$<$ 1x1 mm^2	0.7x0.58 mm^2	0.45x0.68 mm^2
Differential Mismatch	N/A	N/A	0.9 dB

Chapter 5

Measurement Results

Both LNAs were submitted for fabrication in the GlobalFoundries 130nm SiGe BiCMOS 8XP process. However, at the time of this writing, only design 1 had finished fabrication and was measured. This chapter will present the measurement results for Design 1, as well as a description of the measurement plan for Design 2. The measurement results for Design 1 uncovered a layout error that was not captured in simulation due to an error with the tools, which is explained in depth in Appendix B.

5.1 Design 1

Figure 5.1 shows the micrograph of the fabricated Design 1 chip. The measurement setup is shown in Figure 5.2. S-parameters were measured using a Keysight™ PNA-X N5245B. 2.4 mm RF cables connected the PNA to the MPI™ ground-signal-ground (GSG) probes. A Keysight Electronic Calibration (E-cal) module was used to calibrate the s-parameters up to the end of the cables. Then, the probes were de-embedded using manufacturer provided s-parameters. Supply, DC ground, and bias connections were made using DC probes connected to a power supply.

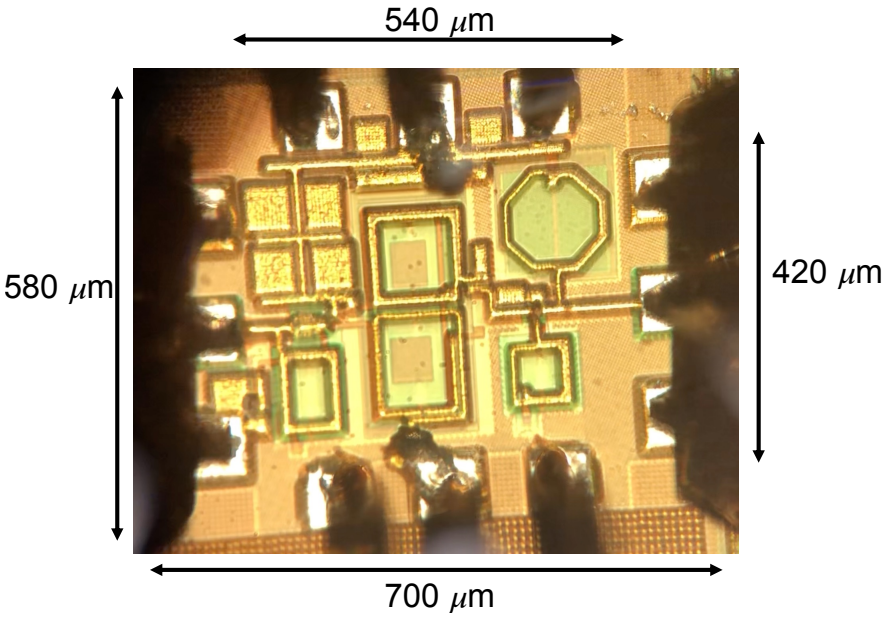


Figure 5.1: Micrograph of the fabricated Design 1 chip.

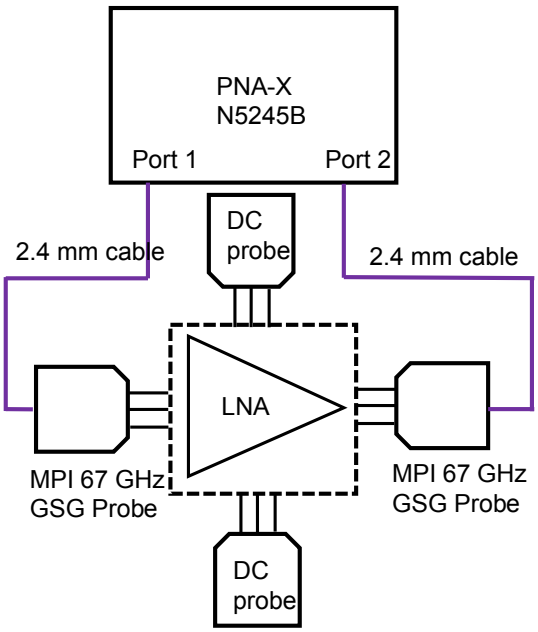


Figure 5.2: LNA measurement setup.

During the verification of the prototype's DC current consumption, a critical short was found in the first stage. The schematic of the first-stage with the short is shown in Figure 5.3. Due to a layout error in the first-stage transistors, the base of Q_1 was shorted to the base of Q_2. This short was not detected with post-layout verification tools such as Layout vs. Schematic (LVS) due to a software bug in the process development kit (PDK) version that was used for the design. The bug is explained in detail in Appendix B.

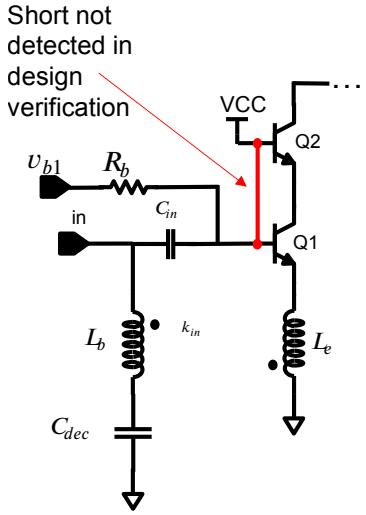
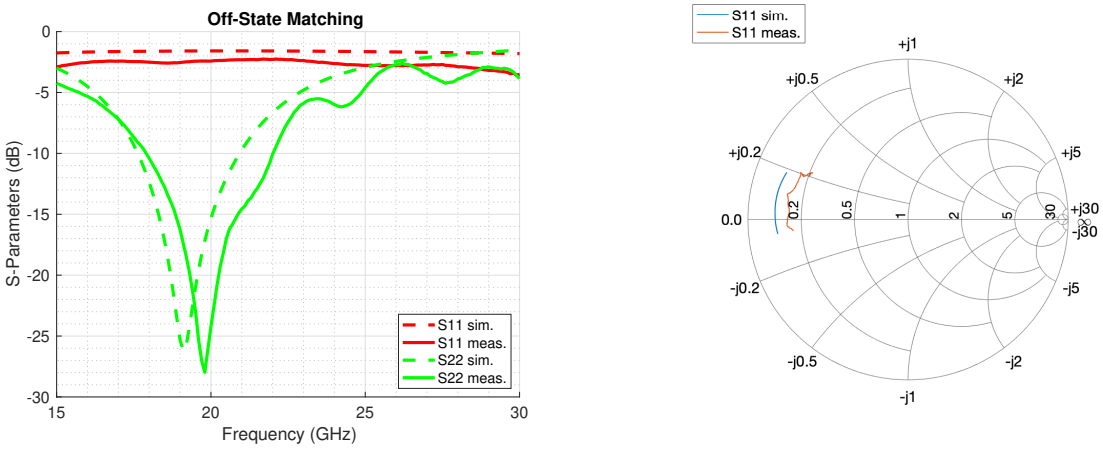


Figure 5.3: First stage short.

Since the base of Q_2 is connected to V_{CC}, which was decoupled to ground on-chip, the short effectively AC-grounded the input of the LNA, leading to very low gain. In addition, if V_{CC} is connected, the first-stage draws a high current (approximately 300 mA in simulation) if V_{CC} is set to its nominal value fo of 1.8V.

While the first-stage short effectively made the LNA non-functional, there were still some measurements that could be made to verify the design. First, the off-state input and output match were measured. These s-parameters were obtained by disconnecting all DC biases and only connecting the RF probes. Figure 5.4a shows the off-state S_{11} and S_{22} magnitudes. There is good agreement between measurement and simulation for S_{22}, save for 1-GHz shift in the lowest point. There is some ripple in the S_{22} after 24 GHz, which could indicate a problem with the calibration. For S_{11}, since it is not well-matched in the off-state, it is hard to discern the match between simulation and measurement in the off-state, so the measurement and simulation are compared in Figure 5.4b on the Smith chart. The measured S_{11} is close to the simulation, but slightly to the right, indicating extra losses in the measurement.



(a) (b)

Figure 5.4: Off-state of the measured LNA. (a) Magnitude of S_{11} and S_{22}. (b) Smith chart plot of S_{11}.

The LNA was also measured with DC supplies connected. The first-stage base bias, v_{b1}, was left floating in order to prevent a current flow between two power supplies. All the other biases were connected. Since the first-stage short causes a large DC current draw with a 1.8-V V_{CC}, a 1-V supply was used, which limited the DC current to 30 mA in total (28 mA from the first stage, and 2 mA from the second stage). To compare to simulation, the LNA was re-simulated with a 2.7 Ω resistor shorting the bases of Q_1 and Q_2. This resistance value was found, by trial and error, to give a close match to the measured gain.

The measured on-state s-parameters are shown in Figures 5.5a - 5.5d. Figure 5.5a, shows the filtering behaviour across all four states. Both notches shifted downwards in frequency. The first notch, enabled when v_{c1} is 1.2 V, shifted from about 24.5 GHz to 23.5 GHz, which is evident from where the gain reaches a plateau. The second notch, enabled when v_{c2} is 1.2 V, shifted from 28.5 GHz to 26 GHz, which can be seen from observing where S_{21} reaches its minimum out-of-band. The on-state S_{11} and S_{22}, shown in Figures 5.5c and 5.5d respectively, show a good match between measurement and simulation. One discrepancy is that the magnitude of S_{11} for frequencies under 19 GHz decreases more than simulated.

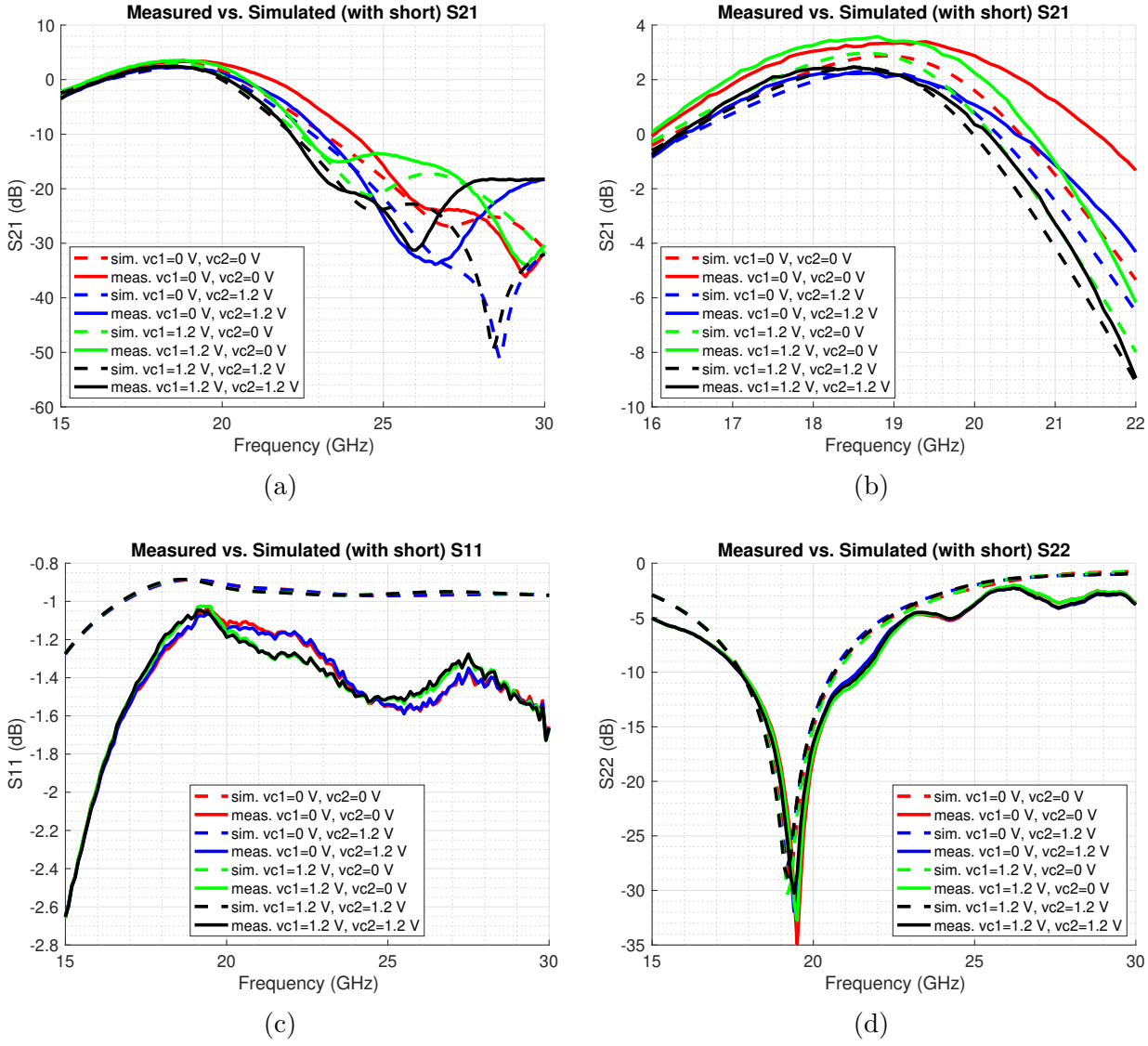


Figure 5.5: Measured on-state s-parameters of the LNA with V_{CC} of 1 V across all 4 tuning states. (a) S_{21}. (b) S_{21} within the Satcom band. (c) S_{11}. (d) S_{22}.

The shift in the notch frequencies could be due to an increase in each notch's capacitance. The notch capacitors were implemented with metal-oxide-metal (MoM) capacitors. Figure 5.6 shows the comparison between simulated and measured gain if each notch capacitor is increased by 15 % in simulation. This additional capacitance results in a closer match between measurement and simulation.

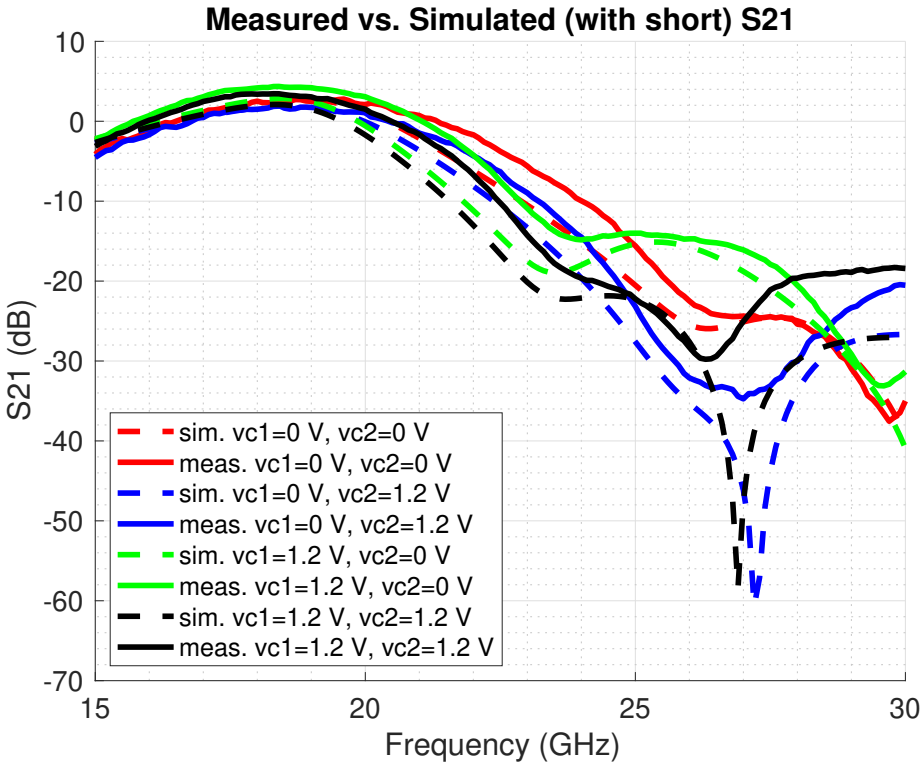


Figure 5.6: Measured vs. simulated S_{21} in all 4 notch states, with 15 % more capacitance at each notch.

5.2 Design 2 Measurement Plan

Design 2 was fabricated as part of an RF front-end for a phased array receiver. The front-end consists of the LNA, a phase shifter, and a variable attenuator. The block diagram of the receiver is shown in Figure 5.7. No standalone test-chip was fabricated for just the LNA, so its performance will be characterized as part of the response of the entire receiver. Additionally, the transistor layout was changed for design 2, and it was verified with a newer version of the PDK that did not have the LVS bug. Therefore, the short is not expected to be present in the measurement of Design 2.

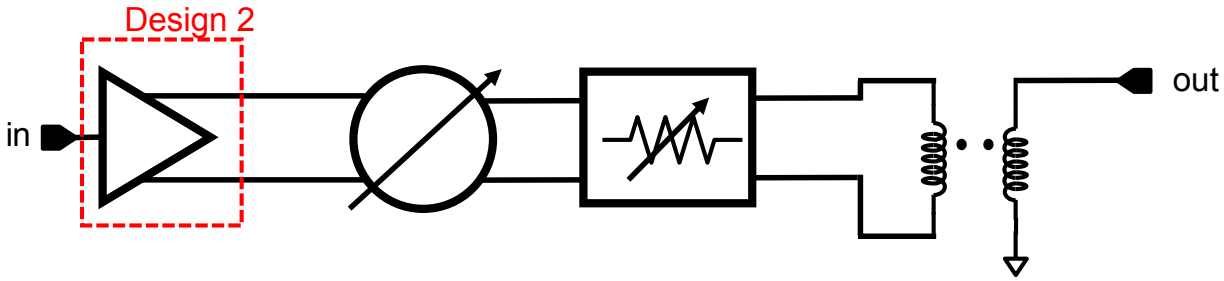


Figure 5.7: Block diagram of the receiver chain containing design 2.

The RF performance of the receiver will be measured by on-wafer probing, similar to Design 1. The difference is that the numerous pads for DC supplies, bias voltages, and digital control voltages will be wire-bonded to a PCB, and brought out with connectors to be connected to external sources.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The push for ubiquitous coverage of high-speed internet has led to the research and development of active phased array antennas for Satcom. One of the challenges in the design of a Satcom receive antenna array is resilience to out-of-band interferers. These interferers can include 5G wireless signals from nearby base stations, and self-interference due to the Satcom transmitter. A potential solution to this problem is to include out-of-band filtering in the LNA of the Satcom beamformer ICs. This thesis demonstrated the design and simulation of two LNAs for a Satcom phased array beamformer receiver with embedded out-of-band filtering. The amplifiers were designed for the 17.7 - 21.2 GHz Satcom downlink band.

Chapter 2 presented an overview of existing circuit techniques to accomplish out-of-band filtering for phased arrays and millimeter-wave LNAs. Common LNA topologies used at mm-wave were reviewed, such as the common-source and cascode amplifiers. Filtering techniques from the literature were also presented, including off-chip filtering, on-chip passive filtering, and on-chip active filtering.

Chapter 3 showed the system analysis that derived the specifications for the LNAs to make them suitable for receiving weak Satcom signals while rejecting strong blockers from the transmitter and 5G base stations. A system model of the RF front-ends of a Satcom phased array receiver was developed. The gain, noise figure, gain flatness, and out-of-band IP_{1dB} specifications were derived.

Chapter 4 addressed the design of the two LNAs using the GlobalFoundries 8XP SiGe BiCMOS technology. The first design is a single-ended LNA with filtering at 24-30 GHz,

allowing it to reject both 5G blockers and Satcom self-interference. The second LNA is a single-ended to differential amplifier, designed to only filter the Satcom transmitter self-interference between 27 and 30 GHz. Both LNAs achieve out-of-band filtering using a 3-coil interstage transformer and a novel second stage transformer feedback technique. Full electromagnetic (EM) simulation results show that the first LNA has an input 1-dB compression point of up to -14 dBm and an output 1-dB compression point as low as -29 dBm between 24 and 30 GHz. The LNA also has a peak small-signal gain of 28.8 dB at 19.4 GHz and a minimum noise figure of 1.85 dB, making it suitable for receiving weak Satcom signals. Finally, four tuning states allow the LNA's out-of-band filtering to be tuned. The full EM simulation of the second LNA shows a peak small signal gain of 26.8 dB, a gain flatness of less than 2.5 dB/GHz in the Satcom band, and a minimum noise figure of 1.85 dB at at 18 GHz. The LNA has an out-of-band IP_{1dB} between 27 and 30 GHz greater than -15 dBm, and more than 31.8 dB of small signal rejection. Both LNAs use wideband transformer-based input matching to achieve an S_{11} less than -10 dB between 15 and 30 GHz, allowing for a easy integration with a 50 Ω receive antenna.

Finally, Chapter 5 showed the measurement results of Design 1. Due to an error in the layout and a bug in the layout verification software, there was a critical short in the first-stage devices. This short drastically reduced the gain of the amplifier. Despite this problem, both the on-state and off-state small-signal measurements showed an agreement between simulation and measurement.

6.2 Future Work

The results in this work offer several promising pathways for further research. These include further explorations on both the circuit and system level.

On the circuit level, it would be valuable to further explore the novel transformer feedback notch introduced in Chapter 4. In this work, the feedback notch was placed in the second stage to improve the out-of-band small signal rejection. But it could also be placed in the first stage to improve the out-of-band IP_{1dB}. However, it is expected that this would degrade the noise figure. Another potential future avenue of research would be to try the feedback notch between a different pair of nodes in the circuit. Also, the feedback notch's rejection could be improved by adopting a differential topology and applying capacitive neutralization to reduce the effect of C_μ, which, according to 4.26, would lower the gain at the notch frequency.

The measurement results of Design 1 showed a shift in the notch frequencies, which may have been caused by variations of on-chip capacitors. To compensate these variations,

a future LNA could have digitally controlled capacitor banks to allow for better post-fabrication tuning of the out-of-band rejection.

The LNA designed in this work could be used to design a multi-channel receiver beamformer for Satcom applications. This beamformer would include a full RF front-end, including the LNA, phase control block, gain control block. The beamformer could be packaged into a bumped, flip-chip IC and be used for a full receiver array as in [3].

The filtering techniques explored in this work could also be applied to an interleaved dual-band Satcom phased array. Such an array would include both transmit and receive antenna elements on the same array. An example of this type of array is shown in [51], where an interleaved array of patch antennas is designed for a Satcom system with the receiver at K-band (17-21 GHz) and the transmitter at Ka-band (27-30 GHz). This array would require the beamformer ICs to include both Ka-band transmitters and K-band receivers on the same chip. Implementing both the transmitter and the receiver on on die, as well as the proximity of the transmit and receive antenna elements, would increase the self-interference seen by the receiver. The receiver would require a stricter out-of-band filtering requirement. An interesting avenue of research would be to design a beamformer IC for such a system, consisting of K-band receivers with out-of-band filtering and Ka-band transmitters in one chip. The beamformers could be used to design a dual-band active phased array with interleaved transmit and receive antenna elements.

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APPENDICES

Appendix A

H-Parameters of Transformer Feedback Notch

A.1 H-Parameter Analysis

The H-parameters can be derived from the 2-port network consisting of the transformer and notch capacitor shown in Figure A.1.

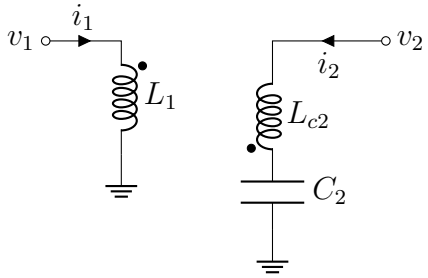

Figure A.1: Circuit for solving for the H-parameters of the notch transformer

Applying Kirchoff's Voltage Law (KVL) on both sides of the transformer gives A.1 and A.2, where $s = j\omega$, $M = k\sqrt{L_1 L_2}$ is the mutual inductance, and k is the coupling factor.

$$v_1 = i_1 s L_1 + i_2 s M. \tag{A.1}$$

$$v_2 = i_2(sL_2 + \frac{1}{sC_2}) + i_1 sM. \tag{A.2}$$

From the definition of H-parameters [20, p. 79],

$$h_{11} = \frac{v_1}{i_1}\Big|_{v_2=0}. \tag{A.3}$$

Setting v_2 to 0 and solving A.1 and A.2 gives h_{11} as in A.4, where $Z_n = sL_2 + \frac{1}{sC_2}$.

$$h_{11} = sL_1 - \frac{s^2M^2}{Z_n}. \tag{A.4}$$

For the remaining H-parameters, we can set v_2 or i_1 to 0 as needed and solve A.1 and A.2, giving the remaining H-parameters as

$$h_{12} = \frac{v_1}{v_2}\Big|_{i_1=0} = \frac{-sM}{Z_n}. \tag{A.5}$$

$$h_{21} = \frac{i_2}{i_1}\Big|_{v_2=0} = \frac{sM}{Z_n}. \tag{A.6}$$

$$h_{22} = \frac{i_2}{v_2}\Big|_{i_1=0} = \frac{1}{Z_n}. \tag{A.7}$$

Furthermore, substituting $s = j\omega$ and $Z_n = sL_2 + \frac{1}{sC_2}$ into A.6 gives

$$h_{21} = \frac{\omega^2 MC_2}{1 - \omega^2 L_2 C_2}. \tag{A.8}$$

Appendix B

Design 1 First-Stage Transistor Short

A stated in Section 5.1, there was a short in Design 1 between the bases of the common-emitter and common-base transistors of the first-stage (Q_1 and Q_2). This short is present due to a layout error in the first-stage devices. Figure B.1 shows the layout of Q_1 and Q_2. Each transistor consists of four 8x0.12 μm^2 in parallel, with deep trenches in the substrate between them. Q_2 is placed to the right of Q_1, separated by a deep trench. The collector, base, and emitter stripes are shown on the first metal layer (M1). Under the base is the base polysilicon, which extends over a larger area than the base metal stripe. The orientation and closeness between the devices in Q_1 and Q_2 led to a short between their respective base polysilicon.

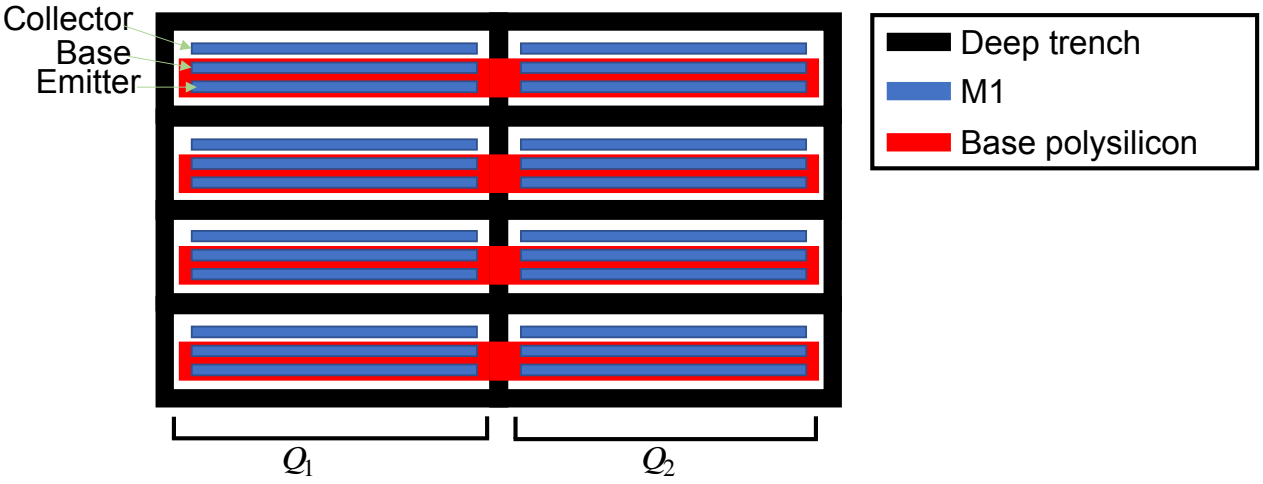

Figure B.1

Normally, layout errors and shorts are detected during design verification with a tool known as Layout vs. Schematic (LVS). In the version of the PDK used to design LNA 1, there was a software bug that did not detect shorts on the base polysilicon layer. Fortunately, a newer version of the PDK that fixed the bug was used for the layout of Design 2, meaning the short will not be present in Design 2's fabricated chip.