The Impact of Lithium Ion on the Application of Resistive Switching Devices

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

With the development of the times, people have higher and higher requirements for storage equipment. Many new storage devices have emerged, such as Magnetoresistive random-access memory(MRAM) and Resistive random-access memory(ReRAM). The junction structure is the basic unit of these two storage devices, and in this paper, the MTJ and resistive switching junction are tuned with lithium fluoride(LiF) to optimize their performance, respectively.

In the first experiment, a magnetic tunnelling junction resembling a battery is developed and proved to be electromagnetically tuneable. In this LiF-based device, reversible non-volatile resistive switching phenomena and tunnelling phenomena coexist, enabling four well-defined groups for each device. The management of the interface enables the spin transfer of actively controlled devices, hence enhancing their application potential.

In the second experiment, 796 devices were measured. For the resistive switching device with TiO as the insulating layer, adding additional LiF layer can significantly increase the probability of resistive switching phenomenon, and adding an appropriate thickness of LiF can also increase the differentiation between high and low group states, which is beneficial for the regulation of resistive switching devices.

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Dedication

This is dedicated to the one I love.

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Chapter 1

Introduction

In today's world, the social changes brought about by information technology are affecting every aspect of our lives, whether it is personal devices such as smartphones and personal computer, or the Internet of Things, e-commerce, cloud computing, etc. represented by the big data information era has greater demand for storage performance. The rapid development of information technology depends on large storage capacity and high access speed storage, so for meeting the requirements of high density, high speed, low power consumption, small size, long life and other characteristics of the high-capacity non-volatile out ride to put forward an urgent demand. The current RAM is mainly oh divided into three categories: static random access memory (SRAM), dynamic random access memory (DRAM) and flash memory, each has advantages and disadvantages, such as flash storage is the only way to make storage in the case of storage without power, but the speed is slow, while dynamic RAM and static RAM will lose information after a power failure, so it does not store information permanently. So driven by this urgent need, major research institutions have researched and proposed some emerging storage concepts and scrambled to meet this information storage need and thus find a solution. Some of the more representative storage solutions in cash include Magnetoresistive random-access memory(MRAM)[5] phase change memory(PCM)[6, 7] and Resistive random-access memory(ReRAM)[1].

ReRAM, also known as RRAM, is a non-linear resistor with memory function. A ReRAM contains top electrode, oxide insulating layer and bottom electrode which is similar as a sandwich structure. This layer of oxide insulation layer can exhibit resistance switching characteristics under the excitation of the two electrode voltages. The earliest studies on the resistive switching phenomenon date back to the 1960s[8, 9], and the recent rise of the resistive transition phenomenon started mainly in the late 1990s and early years of this century, with more research on composite metal oxides at first, such as some pervoskite oxides $SrTiO$,[10], $SrZrO_3$ [11]. In recent years, more research has been done on binary metal oxides, such as TiO_2[12], ZnO[13], Cu_2O[14], Al_2O_3 [15], HfO[16], etc., mainly because of their simple material structure, easy control of stoichiometric ratios, mature preparation processes, and compatibility with the current complementary metal-oxide semiconductor(CMOS) integrated circuit fabrication processes, which have received widespread attention.

In 1817 Arfwedson was the first to discover lithium. The lithium is the third alkali metal element to be discovered in nature. Unlike potassium and sodium, which are found from plants, lithium is found from ores. Lithium is a chemical element with an atomic number of three and an atomic mass of 6.941u. Lithium is a soft, silvery-white alkali metal. With two electrons in the K layer and one in the L layer, it is the lightest of the alkali metals. Lithium and his compounds have a variety of industrial applications, including heat-resistant glass, ceramics, lithium grease lubricants, flux additives for the production of iron, steel and aluminum, lithium batteries and lithium ion batteries. It is known that lithium-containing materials can exchange ions with transition metal oxides, leading to significant changes in their magnetic and electrical properties.

Chapter 2

Fundamentals

2.1 Introduction of several new types of non-volatile storage

Information storage circuit modules are a crucial component of microelectronic integrated circuit systems. However, traditional electronic memory devices such as Static Random Memory (SRAM), Dynamic Random Memory (DRAM), and Flash Memory are facing challenges in breaking through size limitations. These challenges have forced major industry research institutions and research institutes to explore new non-volatile memories[17, 18] that can meet specific requirements, such as long information retention time (over 10 years) [19], fast information access speed (in the order of nanoseconds), low power consumption, high reliability, and high integration of circuit memory cells.

Several emerging memory concepts have been proposed by researchers that can meet these requirements. Representative examples include Magnetoresistive RAM (MRAM) [20], Phase-change RAM (PRAM) [21, 22], and Resistive RAM (RRAM) [23, 19]. These innovative memory concepts are gaining attention due to their ability to meet the aforementioned requirements for modern electronic memory devices.

2.1.1 FLASH memory

The cell structure of flash memory consists of a Metal Oxide Semiconductor (MOS) tube with a floating gate[24]. A dielectric material isolates the top and bottom of the floating gate, forming a capacitor for storing charge. By controlling the amount of charge injected into the floating gate, it is possible to adjust the threshold voltage of the MOS tube, V_T. When there is charge in the floating gate, the reading voltage of the MOS tube increases. Conversely, when the read/write voltage is less than V_T, the MOS tube is turned off, corresponding to logic "0". On the other hand, when there is no charge in the floating gate, the reading voltage is greater than V_T, and the MOS tube is turned on, corresponding to logic "1".

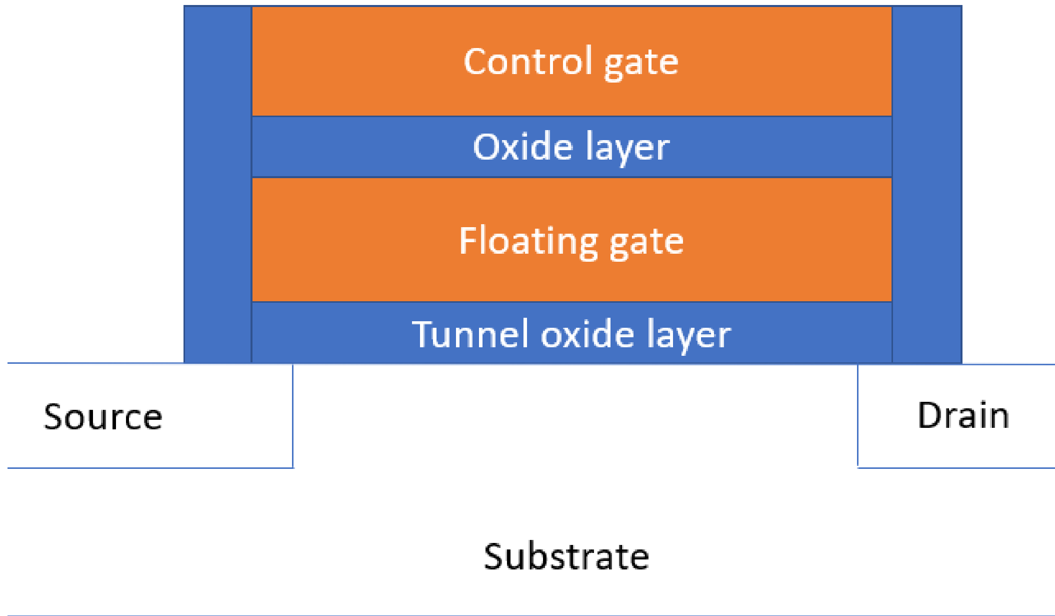

Figure 2.1: The physical structure of flash memory
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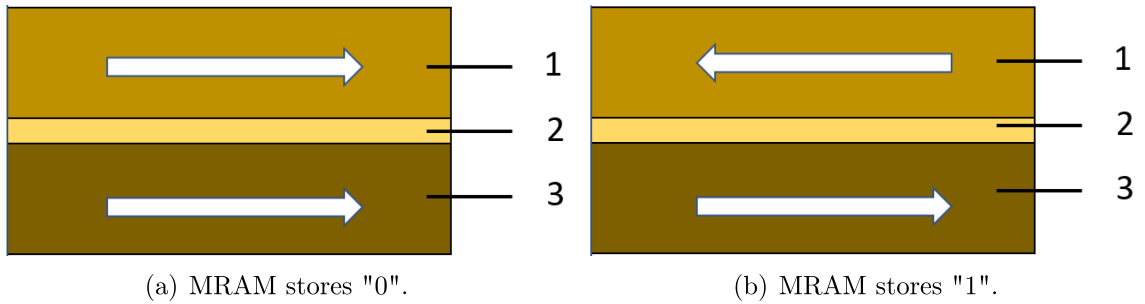
Figure 2.1 shows the schematic of a flash memory cell. After more than 20 years of development, flash technology has become one of the most mature non-volatile memories and is now the mainstream product for commercialization. However, with the continuous progress of the process, as the channel, floating gate, and dielectric layer become proportionally smaller at the 32nm process point, the process difficulty increases, making it challenging for flash technology to continue to advance, and even reach its physical limit. This situation creates a historic opportunity for the development of other storage technologies.

2.1.2 MRAM

Magnetic random memory (MRAM)[25] is a type of memory that stores data by changing the direction of magnetization. Currently, many international semiconductor companies, including Motorola, IBM, HP, and Infineon, are actively developing this technology. The design of MRAM is attractive because it is based on the control of electron spin direction, which allows for the reading of current size and the storage of binary data. In theory, ferromagnetism will never fail, and the number of reads and writes is unlimited.

The initial development of MRAM used a magnetoresistive element known as a giant magnetoresistance (GMR) structure. This structure consists of two layers of magnetic material above and below a metal layer, which is sandwiched between a layer of non-magnetic material. However, the GMR element requires a high current, which is the main drawback of this memory device and makes it unsuitable for high-density memory applications.

A different type of GMR structure used in MRAM development is the magnetic tunnel junction (MTJ). The MTJ structure differs from the GMR structure in that it has a giant magnetoresistive magnetic layer separated by an insulating layer and a non-metallic layer. The magnetization direction of the MTJ elements is determined by the modulation of the upper and lower magnetic layers of the foot parallel or antiparallel to the electronic assembly, creating two stable states, in which the antiparallel state is the larger value. The change in resistance generated by the internal metal conductor creates a different state of magnetic field strength, which constitutes a storage unit for recording "0" to "1" signals.



(a) MRAM stores "0".

(b) MRAM stores "1".

Figure 2.2: A schematic diagram of MRAM cell to store "0" and "1".

MTJ is a crucial component in the magnetic storage cell [26], consisting of three layers: the free layer, insulating layer, and fixed layer. The free layer is thinner and composed of a magnetic film used to store and write information through the magnetic field in either the opposite or same direction as the arrow in Figure 2.2. The insulating layer, with a thickness of only 1 to 2 nm, is a non-magnetic film with a different tunneling potential for electrons with different spin orientations. The fixed layer is thicker, with stronger magnetism and a less easily reversed magnetic moment. The non-magnetic film is sandwiched between the two magnetic films, creating a Tunneling Magneto-resistive Junction (TMJ) or magnetic tunnel junction. MTJ has two states: parallel and antiparallel. In the parallel state, the spins of the free and fixed layers are in the same direction. R_p represents the resistance when the spins are parallel, and R_ap represents the resistance when they are antiparallel. The Tunnel magnetoresistance(TMR) equation is as follows:

$$TMR = \frac{(R_{AP} - R_P)}{R_P} \times 100\% \tag{2.1}$$

2.1.3 PCRAM

In 1968 Ovshinsky proposed the concept of phase change memory. He observed that a material undergoing a phase transition from noncrystalline to crystalline and back exhibits different optical and resistive properties in each state. This led to the idea that the noncrystalline and crystalline states could be used to represent "0" and "1" for data storage purposes.[27, 28].

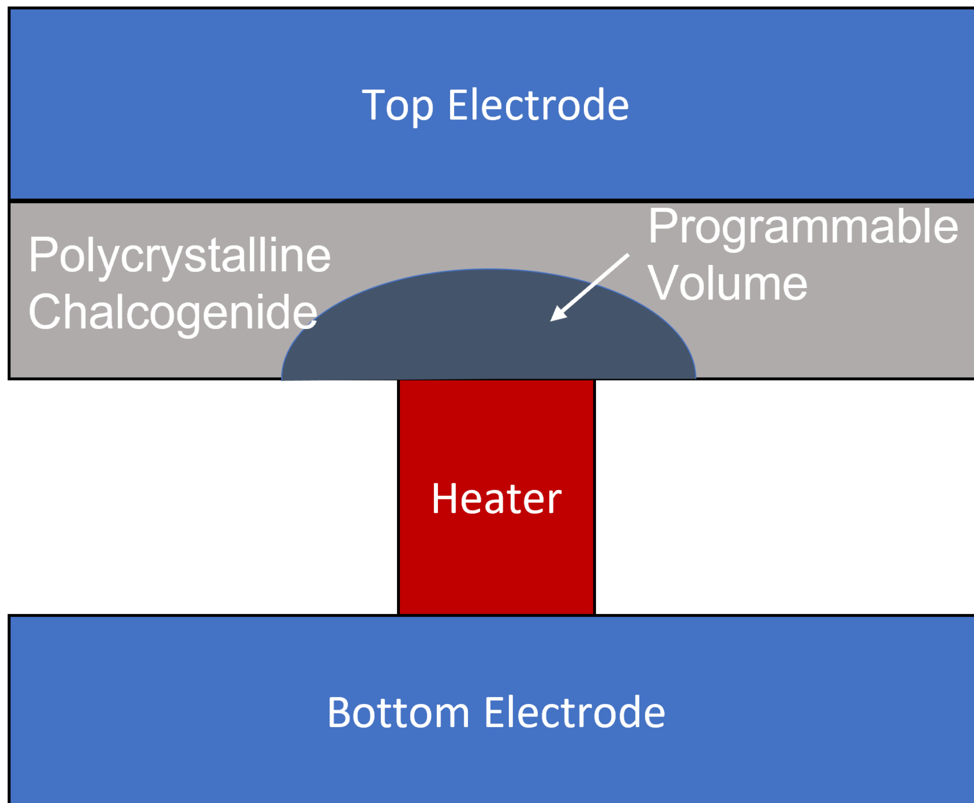


Figure 2.3: A schematic diagram of PRAM cell.

Phase change memory (PCRAM) is a type of non-volatile memory technology that uses a core material based on sulfur compounds (Chalcogenide). The "0" and "1" states of data storage in PCRAM are represented by the disordered and ordered states with a significant difference in resistance. In the unordered state, the material has high resistance, while in the crystalline state, the material has semi-metallic characteristics and low resistance.

The driving force behind PCRAM is an electrical pulse, which is used to heat the amorphous sulfur compound material. By applying a long, moderate intensity electrical pulse, the amorphous material can be heated in the pulse area. If a higher intensity but short duration electrical pulse is applied to the crystalline sulfur compound material, the material is melted and then rapidly cooled to return to the amorphous state. This process is defined as the RESET process[29].

To read the stored data in PCRAM, the resistance of the sulfur compound material is measured. A relatively weak electrical pulse is applied to read the data to ensure that the temperature of the sulfur compound does not rise above the junction temperature, which could result in unnecessary material phase change and incorrect storage information.

PCRAM technology has seen rapid development in recent years and is one of the closest technologies to industrialization. In the International Semiconductor Industry Association planning, PCRAM was included as a priority for industrialization of new storage technology in the 2003-2004 version. Intel launched 0.13 μ m 256MB PCRAM

mass production products and established Numonyx company with ST. Samsung also announced the availability of 512MB PCRAM chips to users on May 4, 2009, which marked a new stage in PCRAM technology with its excellent size miniaturization performance and great potential for mass storage.

One of the biggest challenges of PCRAM is its cost. The current cost per unit of capacity of PCRAM is much higher than NAND flash, and the use of more advanced processes above 45nm still needs to solve some problems, one of which is the power consumption being too large and causing serious heat [30]. As PCRAM requires heating resistors to heat the phase change material, the more advanced the process, the more delicate the unit in the circuit is required [31]. Although experts say that the current technology can guarantee that PCRAM can adapt to the most advanced complementary metal oxide semiconductors(CMOS) production process, the heat and large power consumption will limit the further development of PCRAM.

2.1.4 ReRAM

An ideal non-volatile memory of the future must have high storage density, low production cost, fast read/write speed, low power consumption, good read/write stability, and long-lasting information storage. Currently, silicon Flash memory is the most suitable non-volatile memory in the market due to its high integration and low manufacturing cost. However, Flash memory has drawbacks such as low operating life, slow read/write speed, high read voltage, and the physical limit of IC manufacturing size.

MRAM, although having its own characteristics, has not yet been perfected due to its integration being far from that of Flash. Therefore, it can only be used in a limited market as a special aspect of the application. In recent years, the concept of non-volatile memory based on the resistive switching principle has gained a lot of attention. While the research literature on ReRAM is deep and varied, the working mechanism of ReRAM still needs more research discussions due to uncertainties.

Although the ReRAM device structure follows the traditional semiconductor device fabrication structure: metal-dielectric layer-metal (MIM) structure since the first report of the resistive switching phenomenon, the explanation of the resistance switching phenomenon for different types of dielectric layer materials by scientists is based on different physical principles. In general, the two theories based on the conductive filament model and the interface state model are accepted by most researchers, among which the conductive filament model is the most widely accepted explanation.

The conductive filament model allows for the device size to be small without affecting device characteristics, which theoretically increases the diversity of dielectric layer materials and broadens the application prospects of ReRAM memory technology. Currently, there is widespread interest in memory devices based on the resistive principle, and research on ReRAM memory technology needs further development, with many unknowns and challenges that researchers must actively face. Recent reviews of the current status and working mechanism of ReRAM research [32, 19, 33] have laid the foundation for further in-depth research work.

2.2 Two switching schemes for resistive switching

The resistive switching phenomenon in ReRAM is mainly characterized by its current-voltage (I-V) characteristics. While the I-V characteristics of ReRAM devices based on different dielectric layer materials are generally similar, there are differences in the details. The resistive switching behavior can be categorized into unipolar and bipolar switching, based on the polarity and magnitude of the applied excitation voltage [32, 34]. The polarity of the voltage that needs to be applied to the ends of the ReRAM memory device distinguishes between these two scenarios. In unipolar switching, the occurrence of the switching phenomenon does not depend on the polarity of the write excitation voltage. Bipolar switching occurs when the switch phenomenon is dependent of the polarity of the applied voltage. Different physical mechanisms can be used to explain the resistive switching phenomenon depending on the dielectric material. According to Waser[19, 35], these physical mechanisms include electrochemical metallization, valence change, thermochemistry, electron capture and release, among others. The main mechanisms will be discussed in next section. Depending on the distribution of resistance switching, ReRAM can be divided into the theoretical models of filamentary conductivity and interfacial resistance switching. Resistance switching can also be generated by the dielectric layer or electrodes. Finally, depending on the polarity of the excitation voltage, ReRAM can be divided into unipolar and bipolar resistance switching.

2.3 Mechanism for resistive switching

In this section four different resistive switching mechanism for resistive switching will be introduced.

2.3.1 Electrochemical metallization mechanism

The storage cell consists of a chemically reactive metal electrode, such as copper, silver, or nylon, and another electrode of a non-reactive metal material, such as platinum, tungsten, gold, etc., and a solid dielectric film in between. When a suitable voltage is applied to the reactive metal electrode, the metal electrode atoms decompose into active metal ions:

$$M \rightarrow M^{Z+} + ze^- \quad (2.2)$$

Under positive voltage, these metal ions move towards the cathode, and enter the dielectric layer, and subsequently gain electrons at the cathode:

$$M^{Z+} + ze^- \rightarrow M \quad (2.3)$$

When the reactive metal atoms gradually accumulate at the cathode, and eventually form a conductive metal path in the dielectric layer, the device is in 'On' state. When

a voltage with opposite polarity is applied to the memory device, the opposite process occurs: the conductive metal filament dissolves, the reactive metal ions move in the opposite direction and are deposited in the original metal layer, thus breaking the conductive metal pathway and returning the memory device to the 'OFF' state.

2.3.2 Valence change mechanism

Valence Change Mechanism (VCM) often occurs in memory devices where the dielectric layer material is a transition metal oxide and the valence change is caused by anion migration (e.g. under excitation voltage, oxygen ions in the dielectric layer material migrate and the migration of oxygen atoms often means that a response oxygen vacancy is created in the dielectric layer), usually in the form of a bipolar resistance Transition phenomena. In these transition metal oxides, an increase or decrease in the stoichiometric ratio of oxygen causes a change in the chemical valence of the transition metal, and a change in the valence of the transition metal in the dielectric layer causes a large change in the resistance of the dielectric layer. This change in the valence state of the transition metal is equivalent to the redox reaction of the dielectric layer material under the action of an applied excitation voltage [36].

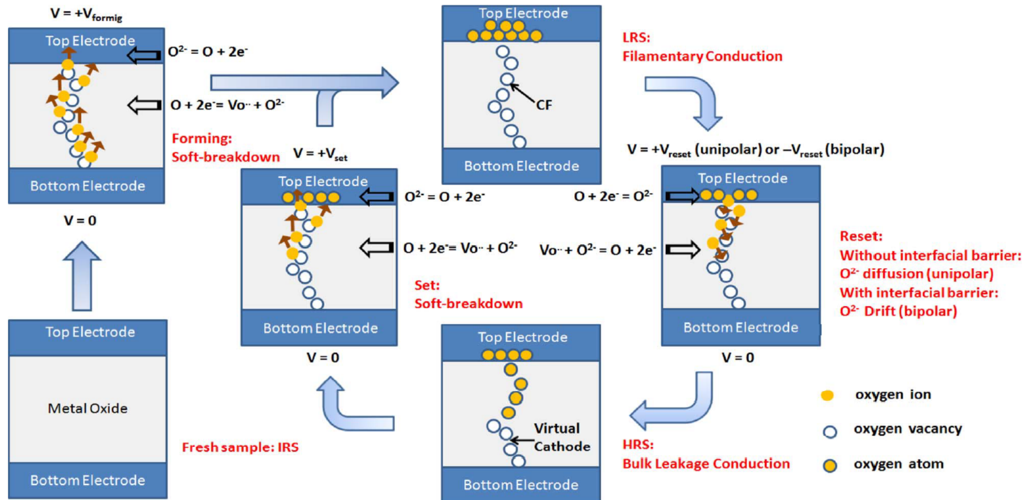


Figure 2.4: A schematic diagram of the switching process of a RRAM[1] Copyright © 2012, IEEE.

2.3.3 Thermochemical mechanism

The thermochemical mechanism (TCM) is based on the initial resistance and turn-off resistance of the cell both in relation to the electrode area of the storage cell, and on the turn-off basis with the initial resistance of the resistive element of the body in the area of the chemical thermal storage cell on the electrode, thus allowing current leakage to occur throughout the area of the electrode. The thermochemical mechanism based on state machines is usually considered to be based on conductive filaments, but specific

or compound filaments, which together complete the opening by a single filament, also require more discussion of conductivity. According to the thermochemical mechanism of temperature change are reflected in the ON state and the disconnected state of the resistance of the storage cell is dependent on the change of the size of a small, thin wire depending on the temperature in the device, this dependence is manifested in the storage device by a different phenomenon, which can be inferred from the mechanism of chemical heat resistance change of the storage cell now dependent on the phase change of the metal with common defects caused by both [2, 37]. Therefore, based on the above experimental results, the researchers hypothesized that the thermal effect of the process based on the chemical mechanism of monopole resistance switching behaviour is determined by the thermal breakdown of the conductive wire caused by the formation of the oxide layer of the SET. And at a large current, for example, the conductive filament is susceptible to thermally induced damage, the conductive filament breaks, the oxide layer partially recovers and thus resets during the occurrence of the situation.

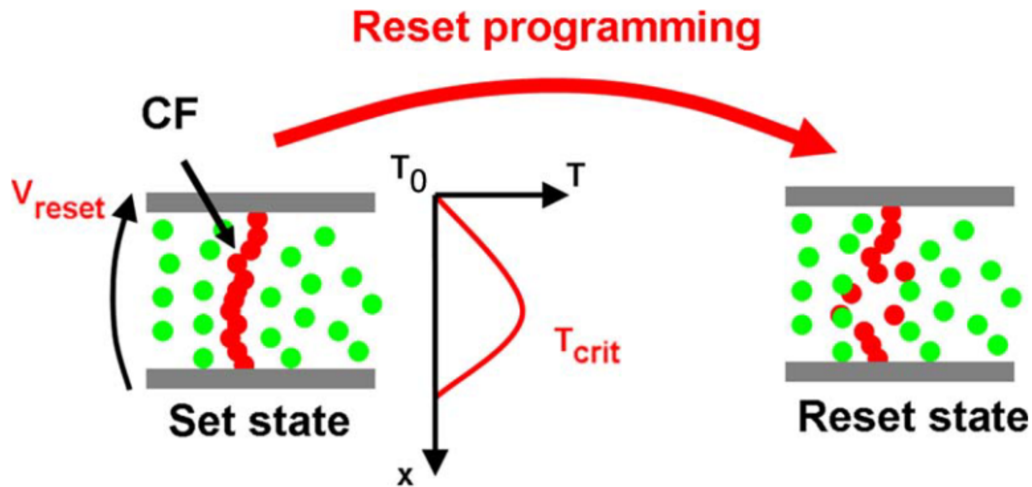


Figure 2.5: A schematic diagram of the reset process of a RRAM, CF rupture occurs when a reset voltage is applied to the CF[2] Copyright © 2009, IEEE.

The high and low resistance states of a TCM based cell are both related to the electrode area of the storage cell, so that the current occurs over the entire electrode area. The transition between the high- and low-resistance states of the thermochemical mechanism-based device cells is generally considered to be based on the conductivity of the filaments, but more discussion is needed as to whether the resistance transition is made by a single filament or a combination of filaments is uncertain[38, 39]. Unlike the temperature dependence of the metal filament-based memory device, the temperature dependence of the OFF-state resistance and ON-state resistance of the thermochemically based memory cell is not obvious, so we can infer that the phase transition caused by both the metal and the defect is simultaneously acting on the resistance change of the thermochemically based memory cell. Therefore, based on the above experimental results, the researcher deduces that the conductive filaments

formed by the thermally induced breakdown in the oxide layer cause the SET process based on the thermochemical mechanism effect of the unipolar resistance transition behavior. At high currents, the heat generated by the current easily destroys the conductive filaments in the SET process, and the oxide layer partially recovers, causing the conductive filaments to break and thus the RESET process occurs.

2.3.4 Electron trapping and detrapping mechanism

Unlike the previously mentioned resistive switching mechanisms, which are based on ion migration, the electron capture and release mechanism is based entirely on the resistive switching behavior of electrons, for which there are some well-established theories. The electron capture and release model is a resistance transformation explanation based on the resistive memory effect of electrons moving in traps and defects and thus causing changes in the electrical properties of the dielectric layer [40]. When traps and deep energy level defects or heavy metal impurities are present in the dielectric layer, the carriers in the traps or deep energy levels are subjected to an applied high electric field and are exposed to the Fowler-Nordheim (FN) electron tunneling effect, i.e. the electrons are trapped by the trap or defect in the dielectric layer under high electrical resistance. The filling of the energy levels in the trap or defect with electrons changes the potential barrier distribution of the dielectric layer material and thus the resistive properties of the layer. In addition, the capture of carriers by the surface state at the position of the gold half contact will also have a significant effect on the height of the Schottky barrier. Therefore, the value of the resistance switching characteristic of ReRAM devices based on the electron capture and release effect is significantly dependent on the electrode area.

2.4 Contact barriers in MIM structures related to the ReRAM memory principle

ReRAM memory devices are metal/insulator/metal (MIM) model structures, while the insulator oxide is generally a divalent metal oxide, chalcogenide oxide, etc. When these materials have a fixed and strict stoichiometric ratio, they are generally insulating, while when used as a resistive material, defects are usually introduced in the dielectric layer (either artificially during fabrication or when an excitation voltage is applied), causing The defects form conductive pathways or new phases under the action of an external electric field or change the potential barrier between the dielectric layer and the metal electrode, thus achieving a memristor function [41].

2.5 Basic conductivity mechanisms associated with the ReRAM memory principle

The observation of the resistive switching behaviour of ReRAM memory devices is simply a matter of measuring the current-voltage characteristics of the device. Based on the properties of the dielectric layer material, the factors influencing the operation of the ReRAM memory device and the resistance switching mechanism can be determined in order to predict the resistive switching behaviour of the memory device, therefore it is necessary to have an understanding of the basic conductivity mechanisms related to resistive memory. The basic conductivity mechanisms associated with metal-semiconductor devices include Schottky Emission, Frenkel-Poole Emission, and Space-Change-LimitCurrent (SCLC).

2.5.1 Schottky Emission

Schottky emission is the effect of an applied electric field, the barrier height changes, electrons directly across the barrier to generate current, the magnitude of the current depends on the height of the barrier and the magnitude of the applied electric field, the temperature will also have an effect on the current current size [36], the mathematical expression of Schottky emission[42] is :

$$J = A^{*}T^{2}exp[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_i})}{kT}] \tag{2.4}$$

where $A^{*} = \frac{qm^{*}k^{2}}{2\pi^{2}\hbar^{3}}$ is Richardson constant,T is absolute temperature,ϕ_B is the Schottky barrier height, ε_i is the permittivity of insulator, K is Boltzmann's constant.

2.5.2 Poole-Frank emission

THe Poole-Frank effect is somewhat similar to the Schottky effect in that it is also associated with traps in the dielectric layer. The basic principle is to use the Coulomb barrier formed by the interaction of electrons and positively charged traps inside the insulator to restrict the electron motion. The Poole-Franco emission is a trap-assisted emission mechanism in which the current density is related to the trap density in the dielectric layer. In addition, changes in the density of states at the interface and the number of defects in the dielectric layer affect the current generated by the Poole-Frank effect [43]. The current density of the Poole-Frank effect is given by:

$$J \sim Eexp[\frac{-q(\phi_B - \sqrt{qE/\pi\varepsilon_i})}{kT}] \tag{2.5}$$

where T is absolute temperature,ϕ_B is the barrier height, ε_i is the permittivity of insulator, K is Boltzmann's constant.

2.5.3 Space change limit current

Space charge limited current (SCLC) is described as a drift current in which the main component of the current through the space charge region is a carrier, and the carrier charge dominates the formation of the electric field of the drift current when the space charge effect is at work. When the carrier concentration injected into the solid dielectric by the electrode is greater than the intrinsic carrier concentration, the conduction current induced in the dielectric will be space charge limited by the carriers, resulting in space charge limitation (SCLC)[44]. The space charge limitation current density equation is expressed as follows:

$$J = \frac{9\varepsilon\mu E^2}{8d} \tag{2.6}$$

2.6 ReRAM Materials

Materials of switching layer

As can be seen from previous articles, many materials can exhibit resistive switching phenomenon, Table 2.1[3] lists the different switching polarities exhibited by different materials when used as electrodes or switching layers. Transition Metal Oxides(TMO) are the most common materials that can exhibit rs phenomena, but since the dominant mechanism of resistive switching is based on redox filamentary switching, other oxides can also exhibit rs phenomena, and in addition nitrides[45, 46] and some chalcogenides [47] with nitrogen and $Te/Se/S$ vacancies can also show resitive switching phenomenon. Materials are intimately related to wafer-level integration in semiconductor fabrication . Because material stacks must be practical and simple for wafer-level integration. Even though considerable technological advances have been achieved, the quantity of materials normally handled in a 12-in fab remains restricted. The majority of the oxide materials in research the are SiO_2. High-k oxides such as HfO_2 are brought into the industry as a result of the scaling of complementary metal oxide semiconductors (CMOS). Despite the fact that HfO_2 has a larger risk of cross-contamination than SiO_2, fabs have the knowledge to incorporate it. Thus, HfO_2 becomes a common candidate for the combined device and array's ReRAM material stack. There are several methods for depositing and integrating HfO_2, under varied temperature budgets. Various processing conditions HfO_2 alter the substance's qualities. During the reaction phase, reactive physical vapour deposition of HfO_2 allows for the adjustment of the $Hf : O$ ratio and the density of defects. Although atomic layer deposition need an additional layer to create enough defects for switching, It still close to stoichimoetry and also provide good uniformity and three- dimensional coverage. As ReRAM research continues, the path of the technology steadily diverges into two applications which are stand-alone and embedded.

Dielectrics	Switching polarity		Electrode Materials	Switching polarity	
	Unipolar	Bipolar		Unipolar	Bipolar
NiO	√ [48]	√[49]	Pt	√ [50]	√ [50]
TiO_2	√ [51]	√[52]	Ag		√[53]
Nb_2O_5	√ [54]	√ [55]	Au	√[56]	
ZrO_2	√ [57]	√ [58]	Ir		√ [38]
HfO_2	√ [50]	√ [59]	Cu		√[60]
Ta_2O_5	√ [61]	√ [38]	Co		√ [62]
MgO	√ [63]	√ [64]	Ru	√[65]	
Al_2O_3	√ [66]	√[67]	Ni	√[68]	√ [69]
CoO	√ [70]	√ [71]	Ti		√[72]
ZnO	√ [73]	√ [74]	Zr		√ [75]
SnO_2	√ [76]	√ [77]	Hf		√[59]
CuO	√ [78]	√[79]	Ta		√ [80]
FeO		√ [81]	TiN		√[82]
CeO	√ [83]	√[84]	Al		√ [85]
WO	√ [86]	√[87]	La	√[88]	
GeO	√ [89]	√ [90]	W		√ [87]
STO	√ [91]	√ [92]	CNT		√ [93]
SiO_2	√ [94]	√ [95]	Graphene		√ [96]
GdO		√ [97]			
BN		√ [45]			
AIN		√ [46]			

Table 2.1: Different materials can be used as dielectric or electrode in ReRAM in literatures[3]. Copyright © 2020, IEEE

Materials of electrodes

Electrodes have many roles to play, not only in providing electrical contact but also in influencing resistive switching. At this stage of research into active electrodes, which is still in its infancy, the diagram summarises some of the electrode materials that have been studied and they can be grouped into three categories.

Table 2.2: Electrode Materials Categories[3] Copyright © 2020, IEEE

Noble metal	Pt, Au, Ir, etc.
Active metal for metal Oxide Resistive Memory(OxRAM)	Ti, Zr, Hf, Ta, Al, Ni, etc.
Active metal for conductive bridge ReRAM(CBRAM)	Cu, Ag, Co, etc.

Consider OxRAM to illustrate the function of the electrodes.From the first few experiments, it can be seen that most of the electrodes used in ReRAM devices contain noble metals. The applied electric field pushes the oxygen atoms out of the position of their lattice and towards the anode, where oxygen vacancies are created. These

oxygen atoms will be used to oxidise oxygen holes in the reset process. Since noble metals do not react with oxygen, these oxygen atoms do not bond to the anode. So the noble metal is suitable as an electrode to retain the oxygen atoms to realize resistive switching.

2.7 ReRAM Benchmark

This sub-section will summarize some articles from 2004 to 2019, listing some of the main characteristic of ReRam that are of mainstream interest.

2.7.1 Switching Current

Figure. 2.6 shows the SET and RESET current trends for the ReRAM device. F represents filamentary switching and A represents Area switching. Most of the maximum switching current of typical filamentary ReRAM are larger than 10 μA and ratio of SET/RESET current is almost fit a linear function. For stand-alone applications, it is desirable to keep the current below $10\mu A$. However, as the switching current increases, the performance of the device in terms of retention and endurance decreases accordingly. This is why most of the articles show switching currents above $10\mu A$, because below $10\mu A$ the symmetry of set and reset is broken, indicating that other mechanisms are involved. The switching current below $10\mu A$ in the diagram is basically not filamentary switching but area switching cells. For non volatile memory(NVM) devices a read test is often done after set/reset to find the latency of the device.

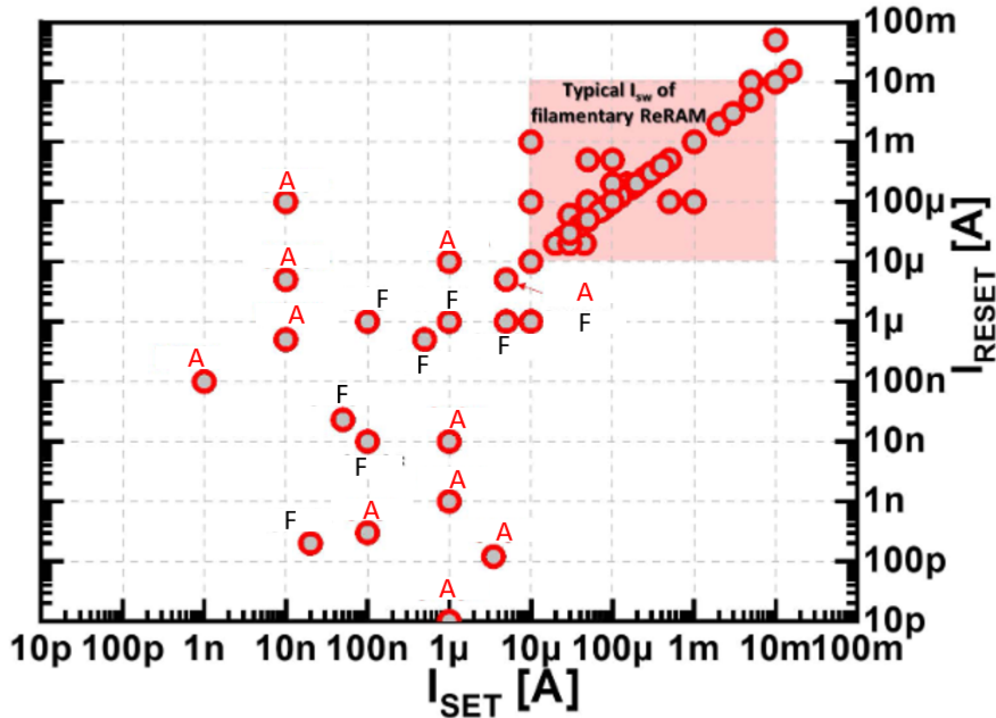


Figure 2.6: SET and RESET switching current[3], "A" represent area switching and "F" represent filamentart switching Copyright © 2020, IEEE.

2.7.2 Switching Speed

The set/reset switching demonstrate the sub-100ns nature of single bits and small arrays due to fast movement of ions in nanometer thin film. But on larger array size the bitline(BL) and word line(WL) are still important factors affecting latency of SET/RESET and READ opreation. The ReRAM unit does not add much latency to the overall system, the latency is also affected by the program scheme.Yu and his colleagues[98] did a read verification of their TMO-based OxRAM at the $50\mu A$, which took about five times.They also made attempts at $10\mu A$ and found that the number of attempts increased as the switching current decreased. When the current increases to $150\mu A$ to $200\mu A$, a single pulse can easily achieve set/reset operation and provide a very differentiated LRS/HRS, so it is easy to achieve READ verification and make it possible to realize fast SET/RESET and READ on array level.

2.7.3 Switching voltage

The switching voltage is affected by many factors, such as ion mobility, material thickness, and parasitic resistance. Since there is a wide range of voltages on various ReRAM devices, it is not meaningful to discuss specific values, but rather to balance voltage and speed to get better regulation.

2.7.4 Endurance

Endurance indicates how many opreations can be done to write and erase the information. In general, enduran cecycles are affected by many factors, such as material, device structure, processing and opreation setting. As the number of cycling increases, the general high resistance state decreases until finally the resistance state stays in the low resistance state and cannot be reset to the high resistance state.

At balanced set/reset situation to get better endurance the current should be higher. For endurance test we always do sampling. It is worth noting that since reram is based on defects, there may be switching failure in the test, many of these failures can be recovered, and we can continue to do endurance testing after recovery. The endurance of ReRAM for low-end embedded application request at least 10^4 cycles. For the NAND replacement, the endurance of ReRAM require 10^6 cycles. Lee[99] and Chen[100] both showed $> 10^{10}$ endurance for HfO based ReRAM in early 2010s. In 2016 Chen[97]pushed the record of endurance to 10^{12} by using hygroscopic oxide,doped $Gd - O$ as resistive switching layer.

The general trend is that for high currents, it is often one of the reasons for reset failures, and as the number of sets/resets increases, soft break down gradually leads to hard breakdown. Both SET and RESET failure also occur while the switching current are in low or medium range. Due to lower current, there are less defects in the filament. So the failure behavior is different.

2.7.5 Retention

Retention refers to the length of time that the information in the device can be retained without power being applied. For NVM, one would expect the data retention time is longer than 10 years. In general, ReRAM requires retention at $85^{\circ C}$ –125 $^{\circ C}$ for 5-10 years to do NVM applications. Since real testing time is not possible with 5-10 years, the resistance of the device is usually monitored by adding temperature and then applying reading pulses and then inferring retention.

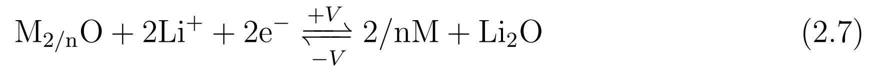
2.8 Experiment Concept

Materials containing Li can exchange ions with transition metal oxides, thus changing their electrical and magnetic properties[101, 102]. So two experiments were proposed to understand the effect of Li ions on materials containing transition metals.

2.8.1 Battery-like magnetic tunnel junctions

Below is a conceptual diagram of our heterojunction, which is composed of a magnetic metal layer, a magnetic metal oxide layer, a thin li-containing dielectric layer, and a magnetic metal The magnetic metal oxide layer and the ultra-thin Li-containing layer

form a composite barrier. The mobile li ions are provided by the li dielectric layer, which is similar to the solid electrolyte in a li ion battery, but it requires a sufficient external electric field to activate the movement of the ions inside. The following equations are for the redox reactions that occur on the surface of the interfacial oxide layer. The interfacial oxide layer releases and traps ions like an ion reservoir by the following reactions.



$$\mathrm{M_{2/n}O + 2Li^+ + 2e^- \underset{-V}{\overset{+V}{\rightleftharpoons}} 2/nM + Li_2O} \tag{2.7}$$

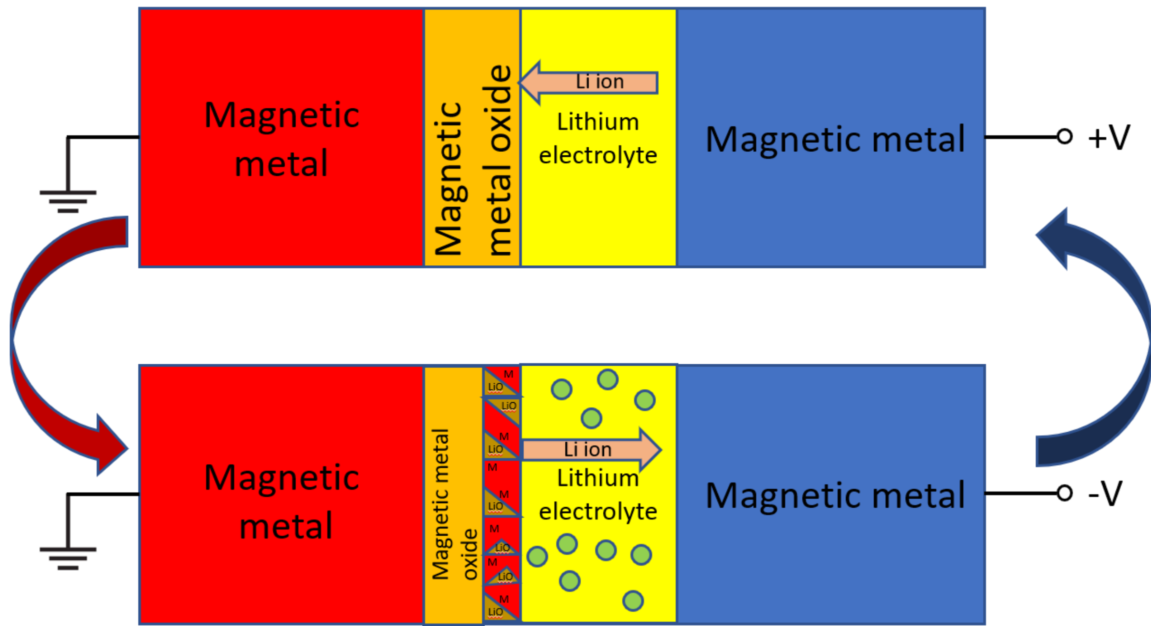


Figure 2.7: Conceptual diagram of a batter-like magnetic tunnel junction. After applying a positive bias the Li ions are push towards the magnetic metal oxide layer and left Li defect(green dot) in the original place and reduction reaction occurs on the interfacial surface. After applying a negative bias voltage, the Li ions were push towards to the Magnetic metal(blue) directions. The oxidation reaction occurs at the interfacial surface. Li ions can reconbine withh the Li defects [4] .
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The reversible ion-exchange exchange of the composite barrier under an electric field has two distinct functions. Firstly ion exchange can enable memristor-like resistive switching [103, 104, 101, 105, 106, 107, 108, 109, 110]phenomena to occur, leading to non-volatile resistance changes. Also the thin tunnel barrier layer can allow quantum tunneling to occur and stabilize the resistive state of the TMR[111, 112, 113, 114, 115, 116].Second, the migration of ions leads to an electrical control of the magnetic properties of the interface, which can also affect the transport of spin polarity or even flip polarity.

LiF is used as a parent compound, which is an inorganic compound that changes

from colorless to white as the size of the crystal decreases and has a structure similar to sodium chloride. It does not cause resistive switching effects itself, as valence breakdown occurs. But the introduction of a cathode layer (oxide layer) to receive these ions can solve this problem. And other methods of obtaining multiple states such as combing tmr withh ferroelectricity, this battery-like concept of ultra-thin layers in electrochemistry can be a promising route to create practical devices with low impedance and low operating voltage with large TMR and large RS.

2.8.2 ReRAM

ReRAM is a new type of non-volatile storage, and there has been a lot of research and development with ReRAM in the last 20 years. People have been wanting to learn more about it and commercialize it. However, since the understanding is not complete, we would like to try to see the impact of Li-ion on ReRAM devices that have a similar sandwich structure to MTJ.

The following figure shows our experimental concept, we grow ReRAM with additional layers on many groups of pre patterned chips from the same batch, then we do the forming, set and reset operation on them with the same parameters and observe the effect of different thicknesses of LiF on the experimental results.

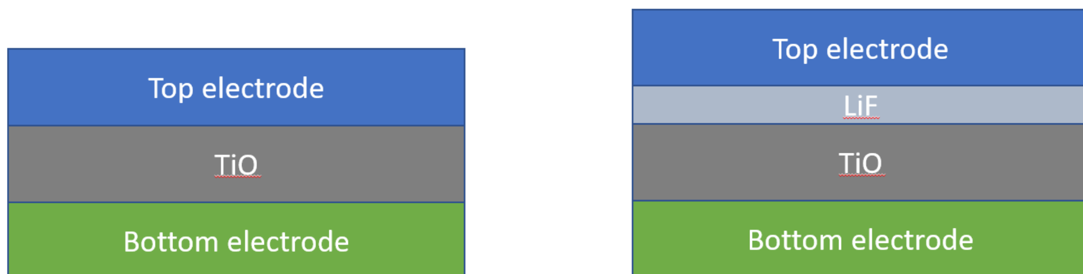


Figure 2.8: A sketch of the structure of a ReRAM, and a sketch of the structure of a ReRAM with additional layers of LiF.

Chapter 3

Experiment

3.1 Physical Vapor Deposition

Conventional PVD technology has different kinds of vacuum deposition methods. Evaporating deposition, and sputtering are two of the most important ones. In PVD, a material is changed into gas phase from its original state then condensed on a wafer to form a thin film. They are used in various fields, such as optical, mechanical, electronic, chemical, etc.

3.1.1 Vacuum vapor deposition

Vacuum vapor deposition is the earliest developed technology in PVD, which essentially uses the phenomenon of evaporation of substances at high temperature to prepare various thin film materials. In the early days, vacuum vapor deposition used resistance heating to generate heat, and then transferred the heat to the adjacent evaporated material to achieve the effect of vapor deposition.

Thermal evaporation

Thermal evaporation is a thin film deposition process that involves vaporizing a target material at high temperature and depositing it on a wafer under high vacuum conditions to ensure good deposition quality. To achieve the high temperature required for melting the material, a resistance coil is used, and a large DC current is applied to generate the necessary heat. The high vacuum environment reduces impurities and gas collisions, facilitating deposition of the target material onto the wafer.

This method has advantages such as simple equipment composition and low evaporation cost, but it also has two significant drawbacks. Firstly, the temperature obtained by resistive heating cannot be too high, which limits the evaporation of high-temperature refractory materials. Secondly, the heat transfer process can cause permeation contamination of device components, heating elements, and crucibles, which

can result in lower purity of the thin film materials obtained. Therefore, this method is more suitable for materials with lower melting points.

A simple schematic of a thermal evaporation system is shown in Figure. 3.1.

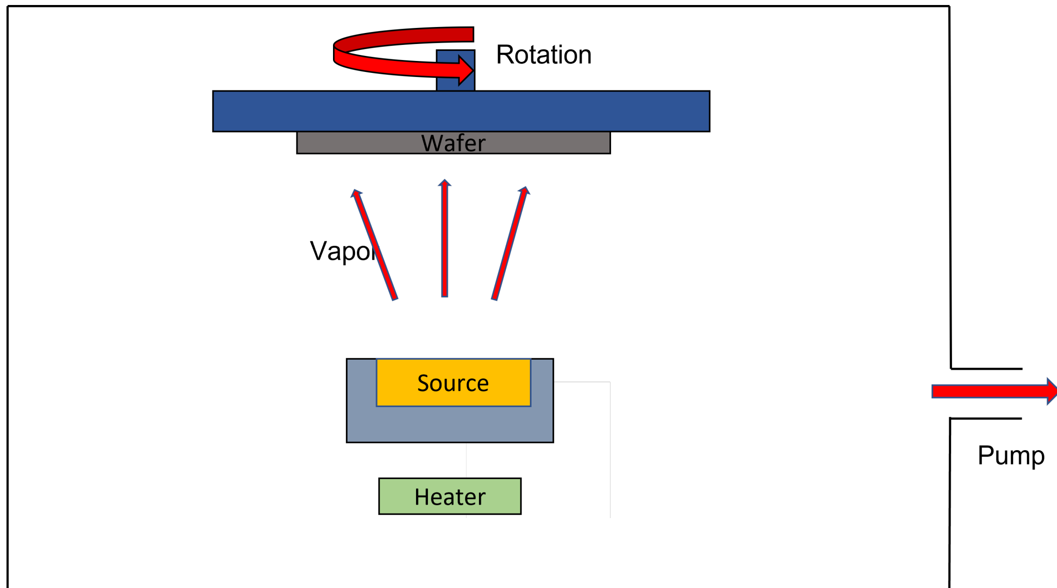


Figure 3.1: A schematic diagram of thermal deposition device.

Electron beam evaporation

The introduction of electron beam evaporation technology can effectively solve the aforementioned defects of thermal evaporation. Electron beam evaporation uses a focused electron beam to bombard the target material, achieving local temperatures of thousands of degrees to vaporize the material. Typically, a current of 1A passes through the filament to generate electrons, which are then accelerated by a voltage of 10KV. To avoid permeation contamination, electron beam magnetic deflection technology is usually used, which deflects the electron beam by 270°. This method can evaporate most materials, but heat utilization is low and most of the heat generated by the electron beam bombardment is carried away by cooling water. To obtain high-purity refractory materials, the laser pulse heating method was later developed. This method uses laser pulses to generate instantaneous high temperatures to evaporate the material. As a non-contact heating method, there is almost no permeation contamination, resulting in high-purity vaporized material. Figure. 3.2 shows a simple schematic of an electron beam evaporation system.

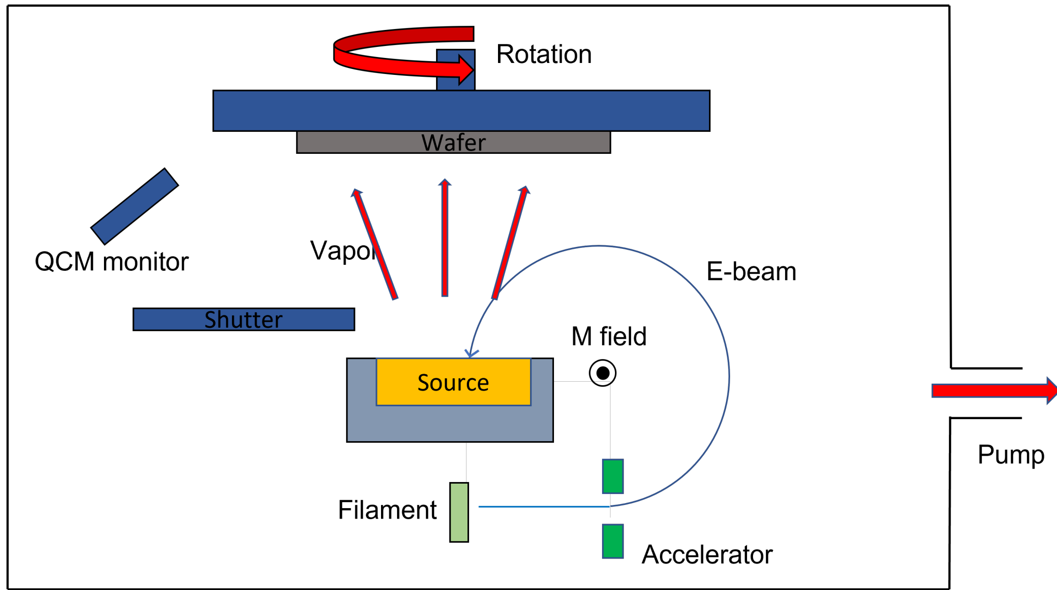


Figure 3.2: A schematic diagram of E-beam deposition device.

3.1.2 Sputtering

With the advancement of vapor deposition technology came the vacuum sputtering coating. Sputtering deposition is a physical process that occurs when ions bombard the surface of an object. The large energy transfer between the incident ions and the target during the sputtering process is a distinctive feature. Compared to evaporation, where atoms acquire kinetic energy of 0.1 ev, atoms from sputtering can acquire kinetic energy up to 5-20 ev, a difference of two orders of magnitude. In sputtering deposition, atoms with high energy play two important roles:

(1) To improve the diffusion ability of the atoms themselves on the surface of the film, which is conducive to improving the film organization and composition, etc.

(2) To cause the substrate temperature to rise, which is conducive to improving the deposition and adhesion of the film.

There are four main early sputtering methods:

(1) Direct Current (DC) sputtering.

(2) Radiofrequency (RF) sputtering.

(3) Magnetron sputtering.

(4) Reaction sputtering.

Each method has its advantages and disadvantages. For example, DC sputtering equipment is simple and easy to use but can only be applied to materials with good electrical conductivity. RF sputtering can deposit a variety of metal and non-metallic materials, and has the advantage of self-biasing effect leading to spontaneous bombardment and sputtering of gas ions. Magnetron sputtering technology has unique advantages in terms of higher deposition rate and lower working pressure. Reactive sputtering

is the process of forming compounds during deposition. Although this method is widely used to prepare compounds, it is prone to target poisoning. A simple schematic of a sputtering system is shown in Figure 3.3.

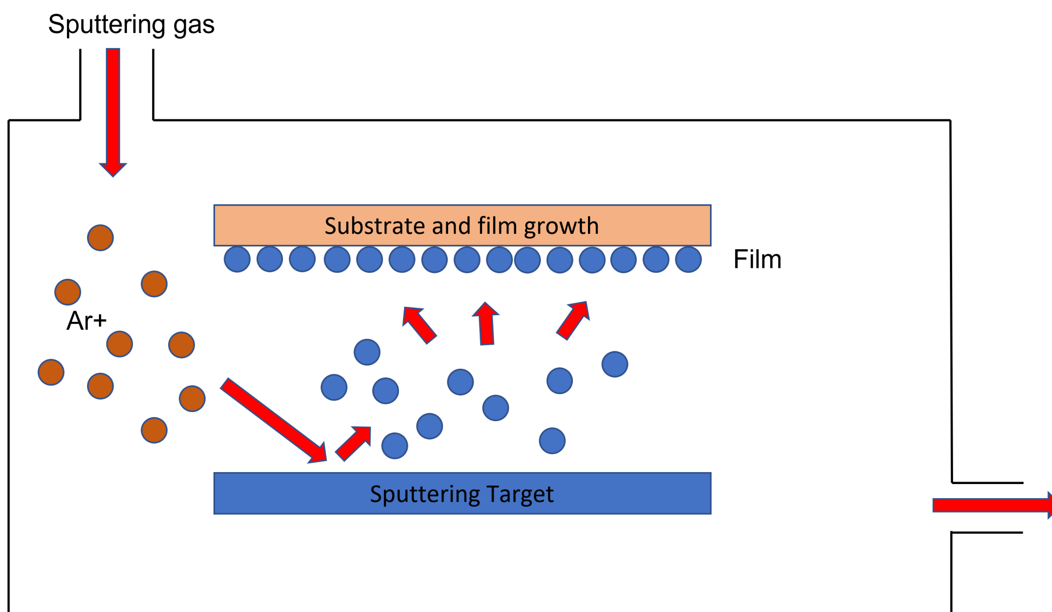


Figure 3.3: A schematic diagram of sputter deposition device.

3.2 Measurement platform

3.2.1 I-V measurement

Flowing cryostat measurement platform

The flowing cryostat measurement platform contains a blue dewar, a probe, an electrical magnet, 2182 nano voltmeter, 6220 current source, electrical magnet power supply and a gauss meter.

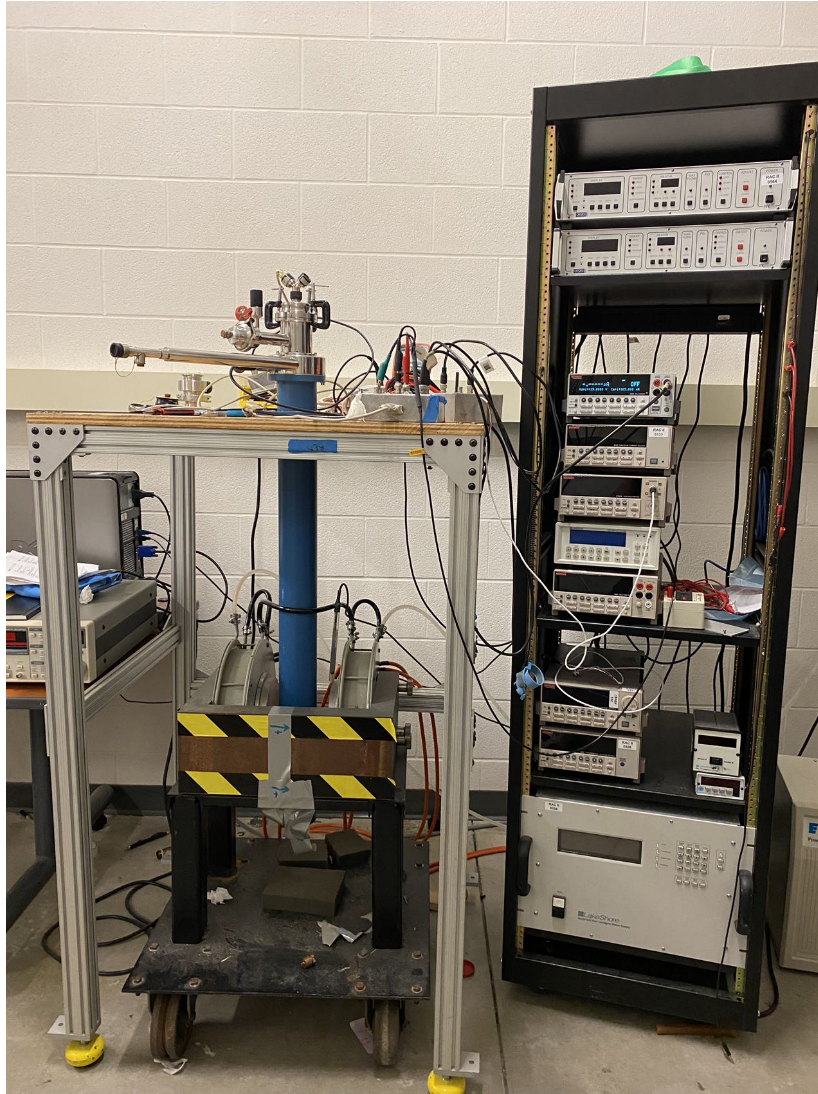
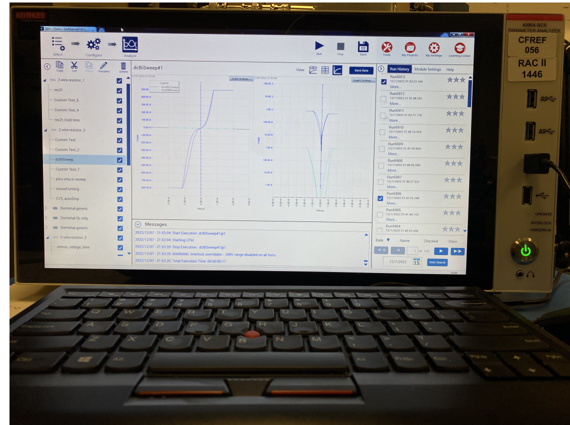


Figure 3.4: Flowing cryostat measurement platform

Probe station with 4200

The I-V characteristic test of resistive switching devices is the most important and crucial step in this experiment, and the resistive switching phenomenon is reflected in the test results of the I-V characteristic curve. Until now, there is no instrument specifically used to test the I-V characteristics of resistive switching devices, and the I-V test platform shown here is built by our research group. The I-V test platform includes a hardware part and a software part, as shown in Figure 2.13. Parameter analyzer 4200A-SCS from Keithley Instruments and Probe station from Cascade Microtech.

(a) Microtech probe station



(b) Keithley Instruments 4200A-SCS parameter analyzer

Figure 3.5: I-V measurement system probe station with 4200A-SCS parameter analyzer

To achieve batch measurements, we use a prepatented chip and then deposite the corresponding film to get our ReRAM device. The detail related to prepatterned chip is in section 4.2.

Chapter 4

Results and Discussions

4.1 Battery-like magnetic tunnel junctions(MTJ)

4.1.1 Devices Fabrication

The battery-like magnetic tunnel junction were fabricated on (100)-Si wafer in a high vacuum system. The stacking layers of MTJ are:

Si wafer/epi-$MgO(10)/Fe_{50}Co_{50}(8)/LiF(2.8)/Fe_{50}Co_{50}(3)/Ti(50)/Pt(5)$.

The process of fabricating MTJ are listed below:

1. Ultrasonic cleaning the Si wafer in isopropyl alcohol(IPA)and dipped in 1% hydrofluoric adid for 90s to remove

2. Using electron beam evaporation deposite MgO buffer layer on Si wafer at $300°C$ to seed the subsequent growth.

3. Using electron beam evaporation deposite $Fe_{50}Co_{50}$ layer at room temperature as bottom electrode.

4. Wait for natural oxidation.

5. Using electron beam evaporation deposite MgO with shadow mask(x-direction).

6. Using electron beam evaporation deposite MgO with shadow mask(y-direction), so MgO layer with a hole at the center can be created.

7. Using electron beam evaporation deposite LiF layer at room temperature.

8. Using electron beam evaporation deposite $Fe_{50}Co_{50}$ layer at room temperature.

9. Using electron beam evaporation deposite Ti and Pt layer as the top electrode and also as a protection layer.

The deposition growth rate of all layers are controlled in range from 0.08Å/s to 0.12Å/s.

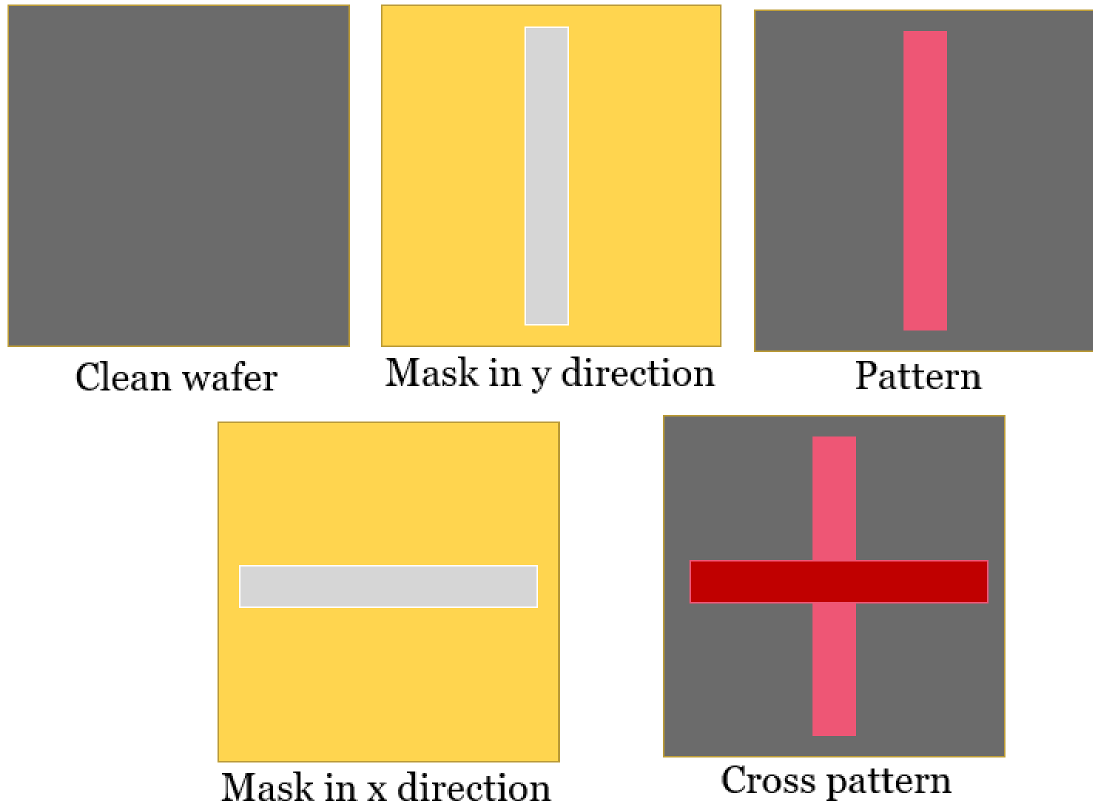


Figure 4.1: A schematic of shadow mask.

A shadow mask is used to deposit a special pattern. Fig. 4.1 shows a simple example. A mask in the y direction is covered on a clean wafer, and then the deposited paatern will be a vertical line and then rotate the mask into the x direction and deposit again on the same wafer, We can get a cross pattern.

4.1.2 Results

The skectch layout of the MTJ is shown in Figure 4.2 a). $Fe_{50}Co_{50}$ was used due to its high intrinsic spin polarization[114]. The top magnetic layer is 8 nm and the bottom magnetic layer is $3nm$. Because the different thicknesses allow us to distinguish them with their switching fields. Figure 4.2 b) is the cross-sectional overview of the device, which shows the well-defined layers. The LiF in the figure is well grown and continuous, and X-ray diffraction(XRD) shows that although there is a little misalignment in the top layer of FeCo, it is still mostly oriented . 2.8 nm is the optimum thickness we found, because LiF that is too thin can easily short the device, and LiF that is too thick can prevent the quantum tunneling effect. A little misalignments were found on the well crystalized lattice structures of FeCo electrodes which were shown in Figure 4.2 c). Figure 4.2 d) shows the Electron energy-loss spectroscopy(EELS) mapping of different elements which are Si, Mg, O, Fe, Co and F, over the highlight area of Figure 4.2 b).

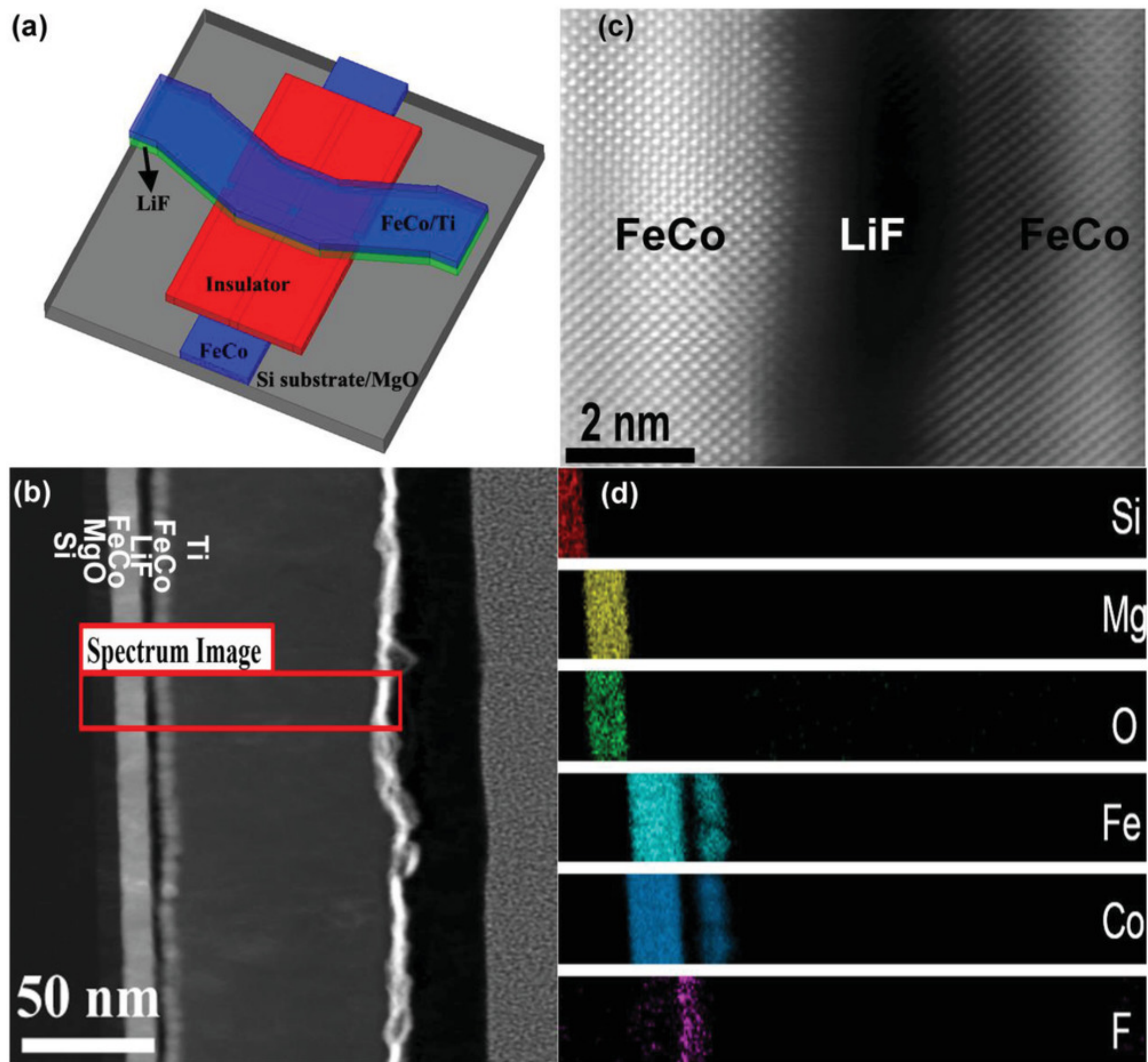


Figure 4.2: a) A sketch layout of an MTJ with layers from bottom to top in nm: Si wafer/epi-$MgO(10)/Fe_{50}Co_{50}(8)/LiF(2.8)/Fe_{50}Co_{50}(3)/Ti(50)/Pt(5)$.Where $Fe_{50}Co_{50}(8)$ is bottom electrode and $Fe_{50}Co_{50}(3)/Ti(50)/Pt(5)$ together are the top electrode. The active junction area are define by a opening hole area with dimension $30\times30\ \mu m^2$ in the red insulating pad. b) Cross-sectional overview of the device. c) STEM image of the main section of the device.d) EELS mapping of different elements across the high light area in Figure 4.2 b)[4] © 2021 Wiley-VCH GmbH.

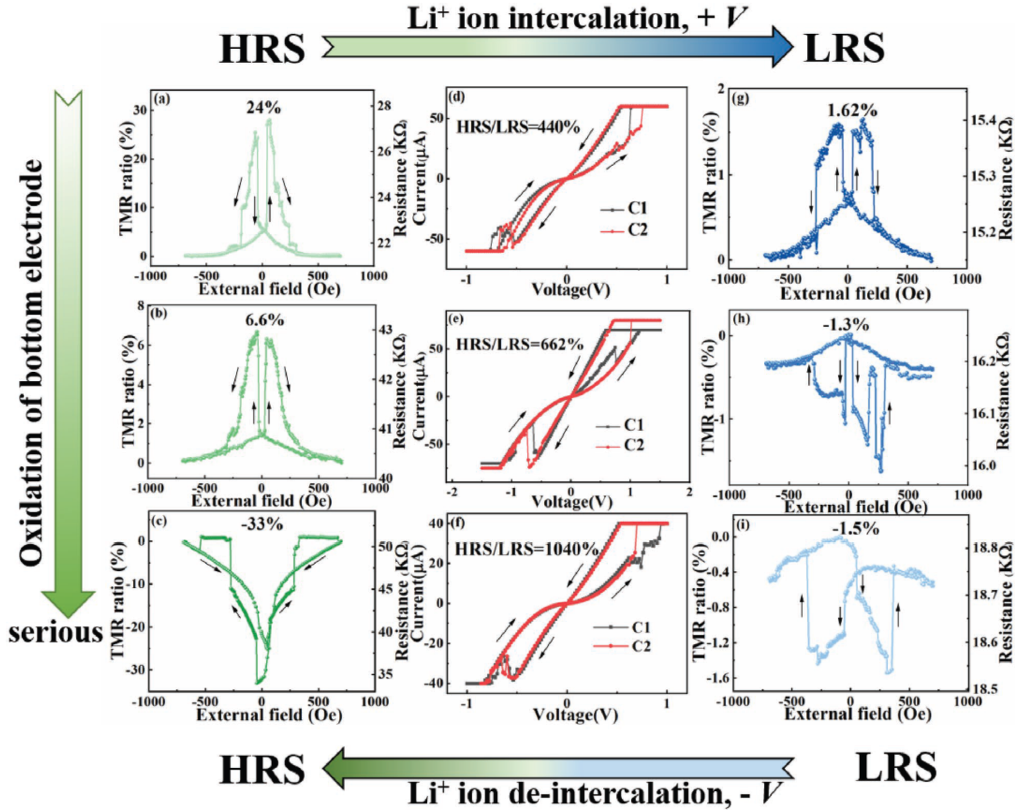


Figure 4.3: TMR loops were measured for the three devices with different oxidation time in the high and low resistance states at 77k and I-V characterization was also done. A limitation of current is set to prevent the permanent dielectric breakdown. (a,d,g) is related to the natural oxidation time with 2 hours, (b,e,h) is related to the natural oxidation time with 6 hours and (a,d,g) is related to the natural oxidation time with 12 hours[4] © 2021 Wiley-VCH GmbH.

Figure 4.3 (a-c) TMR loops of the junctions with the different oxidation time. (d-f) I-V Characteristics of corresponding devices at 77k. (g-i) TMR loops for corresponding devices while they are in LRS.

4.1.3 Discussions

Figure 4.3(a-c) show the TMR loops at different oxidation times of junctions. oxidation times from top to bottom are 3 hours, 6 hours and 12 hours, respectively. The resistance of the device is at a relatively high resistance state due to oxidation. As the oxidation time increases, the resistance of the device increases and is accompanied by a flip in the TMR direction. TMR is weaken as the process of oxidation. In this system, when the oxidation is weak, direct tunneling through LiF still dominates, and TMR remains positive but is weaker due to spin scatterings. As the oxide layer gets thicker and thicker, negative spin polarization from the transition metal oxides becomes more pronounced and TMR eventually turns negative.

Figure 4.3 (d-f) show the i-v curve at 77k. It can be clearly seen from the figure that the device is a bi-state device. When the positive voltage is applied, the device changes from the high resistance state to the low resistance state, and when the reverse voltage is applied, the device returns from the low resistance state to the high resistance state. Here the positive voltage means that the top electrode is on high potential and the bottom electrode is on low potential, and vice versa. In the figure, there is a current jump up at around 1v, which is called "set", and a current pick up at around -0.75V, which is called "reset". The HRS/LRS ratio is more than 1000%. The LRS part of I-V curve is liner which indicates significantly reduced tunnel barriers. The HRS part of I-V curve is noliner which suggest the tunneling effect is dominating the transportation. To confirm that it was the Li ions that were responsible, a comparative experiment with CaF instead of LiF was carried out. The structure is similar, that is, the 2.8 nm LiF in the previous structure is replaced by 2.8 nm CaF_2. Only breakdown was observed at a bias voltage of about 2 V and no bi-stable state was observed in the CaF_2 device. From the comparison experiments, it can be seen that resistive switching is not caused by F ions, but is related to Li ions. According to the study on lithium batteries, the reaction of li ions and Fe/Co occurs at 1.5V to 2.5V [117, 118], while the reaction of Li ions and Fe/Co oxides starts at 0.7 V to 1.1 V[119, 120, 121]. At voltage is higher than 1.5 V the junction will be broken down, so the reaction LiF between will not occurs in our devices. As shown in equ2.7, while applied a strong positive voltage, the Li ions were forced to move to the metal oxides layer to grab O ion from metal oxides layer to form LiO_2. At the boundary between the metal oxide layer and the LiF layer, LiM_xO_y compounds are formed due to mutual competition, and the x and y coefficients are determined by the concentration of various substances[122, 123, 124]. On the modified device we also found that its resistance decreases with increasing temperature, a typical characteristic of tunneling through an insulating barrier. As the temperature rises from 77k to 300k, the change in resistance of the HRS is somewhat different from that of the LRS; for the HRS the resistance drops by a factor of 1.2 to 1.9, while for the LRS the resistance drops by a factor of fully 5-10. This indicates that the tunneling effect is dominant at the time of HRS, while for LRS the sensitivity to temperature is due to the defected-mediated transportation in LiF and Li_2O.

As can be seen in the Figure 4.3 (g-i), the TMR curve shows two another stable resistive states when the device is at LRS. From the two phenomena of resistive switching and the weakening and reversal of TMR, we can say that li ion migration and interfacial oxidation co-exist in this system. When a certain positive voltage is applied, the li ions are forced to the interfacial oxide layer and oxidation occurs. At the same time, as the ions move, more defects are created in the tunnel barrier. This causes the device to show its LRS. If an appropriate reverse voltage is applied, the device can return to the HRS, and this process is reversible and repeatable. It can also be found in the figure (b.e.h) that the sign of TMR can be regulated by adjusting the applied electric field to control the li ion motion. Since the lif is only 2.8 nm, which is far from enough to react with the entire oxide layer, the oxide layer is only partially reduced in LRS, and there are still a large number of defects in the LiF layer. This causes tunneling (for positive TMR) to be weakened and transmission (for negative TMR) to be enhanced, and showing a small negative magnetoresistance.

4.2 Li Enhanced ReRAM

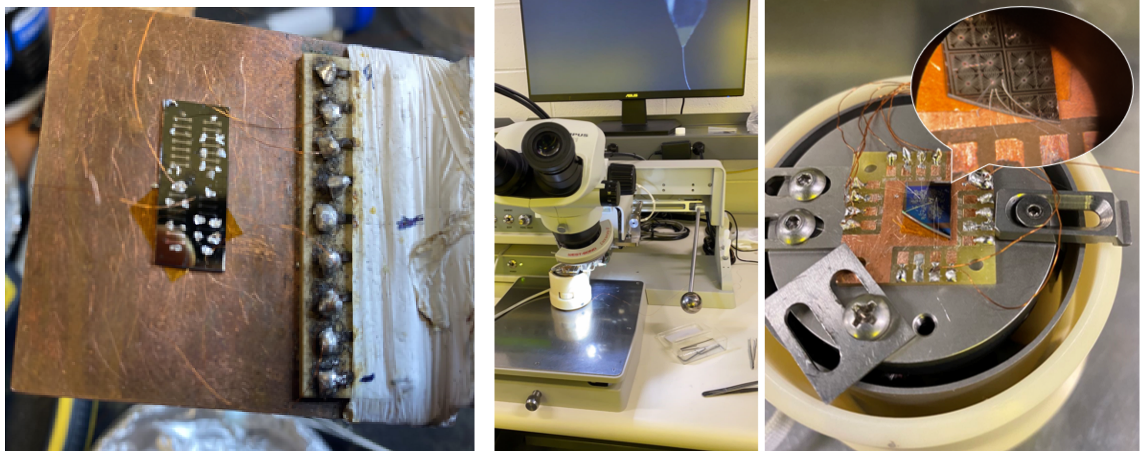
4.2.1 Devices Fabrication

Chip design

After obtaining the devices through shadow-masked electron-beam evaporation, prepatterned chips were designed and fabricated to increase integration and device growth and measurement period. Different chips were designed based on different bonding techniques, as shown in the figures below. The design with the large patterned electrode is for indium bonding, while the design with the small patterned electrode is for wirebonding.

The indium pressing method involves repeatedly pressing and rubbing a small piece of indium wire with a hard object on the sample where the electrode needs to be made, until the local surface layer of the sample breaks down and the indium metal penetrates into the broken gap. Then the wire is placed on the sample, and indium is pressed on top of the wire to keep the wire and indium firmly in contact through the deformation of indium. The advantage of this method is that it is simple and easy, but the disadvantage is that the error rate is high and it destroys the sample, which makes it difficult to operate for smaller and thinner samples.

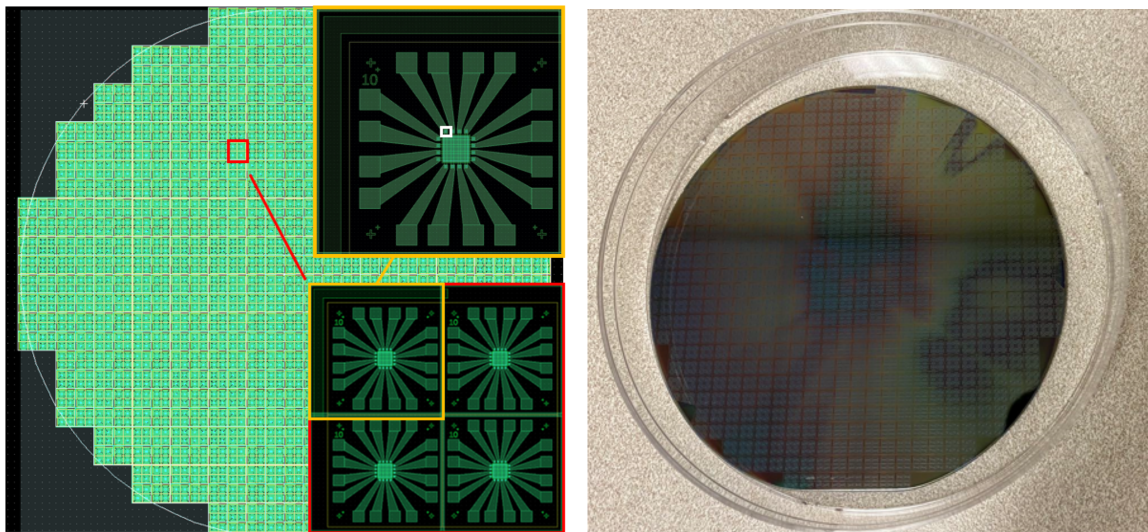
Wirebonding, on the other hand, involves using a wirebonding tool (wirebonder) to make electrical interconnects between integrated circuit packages and integrated circuit dies. Its principle is to convert the vibration of ultrasonic waves into friction movement between the electrode and sample surface. In the process of friction, the oxidation layer of metal on the sample is destroyed, heat is generated to make the metal softer and molecules more active, and pressure is applied to immerse the electrode and metal surface into each other and connect them. The advantages of this method are that the contact resistance can be very small, and the electrode can also be very small (20 microns), making it applicable to very small samples. Additionally, the metal wire and metal film can be selected from the same metal, eliminating hidden problems of contact potential, thermal potential, and thermal expansion and contraction. However, the disadvantages are that production is relatively troublesome, the contact point is not as reliable as the silver glue method, and the production process is slightly more demanding.



(a) Indium bonding: Connecting the electrode with the probe.

(b) Wirebonding: Connecting the electrode with the chip holder.

Figure 4.4: Design drawings and actual chip. The bottom right corner of Figure.4.5(a) is the zoom in view of a red squire zone. It contains 4 units area with same device size as shown at the top left corner of each unit batch, which is 10 μm. Each unit batch has a shared bottom electrode at the center and 16 top electrodes. The white squire zone is the device, the size is $4\mu m$, $6\mu m$, $8\mu m$ and $10\mu m$



(a) Condensed pattern design

(b) prepatterned chip

Figure 4.5: Design drawings and actual chip. The bottom right corner of Figure.4.5(a) is the zoom in view of a red squire zone. It contains 4 units area with same device size as shown at the top left corner of each unit batch, which is 10 μm. Each unit batch has a shared bottom electrode at the center and 16 top electrodes. The white squire zone is the device, the size are $4\mu m$, $6\mu m$, $8\mu m$ and $10\mu m$

The sketch of the side view of device area (white squire zone) are shown in below Figure.4.7

Figure 4.6: Skectch of the side view of device area(white squire zone in Figure.4.7). The TiN is the bottom electrode and the device size is defined by SiO_2.

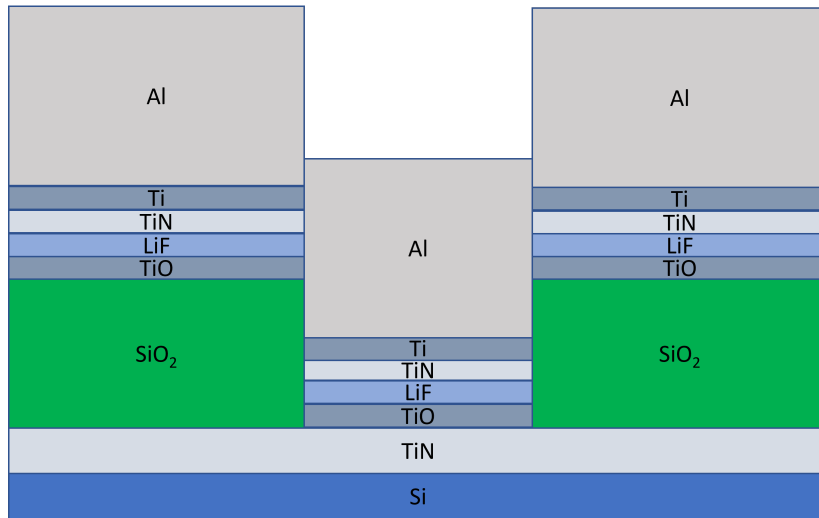
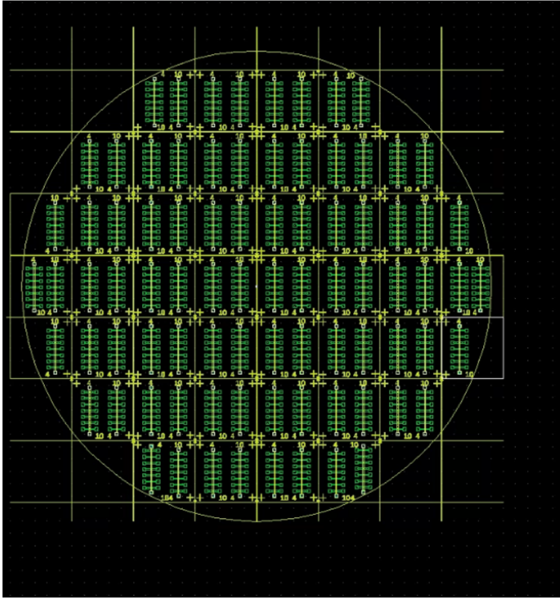
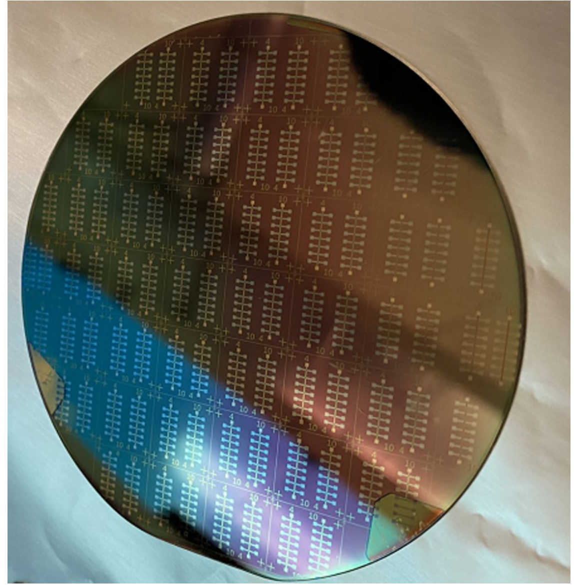


Figure 4.7: Skectch of the side view of device area(white squire zone in Figure.4.7). The TiN is the bottom electrode and the device size is defined by SiO_2 and the S1811 is the photoresist.



(a) Prepatterned chip design with larger top electrode.



(b) Prepatterned chip

Figure 4.8: Design drawings and actual chip. The size are $4\mu m$, $6\mu m$, $8\mu m$ and $10\mu m$ various from top to bottom.

Fabrication of prepatterned chip

In order to get the data efficiently in bulk, prepatterned chips are used. The figure below shows the process flow of prepatterned chip.

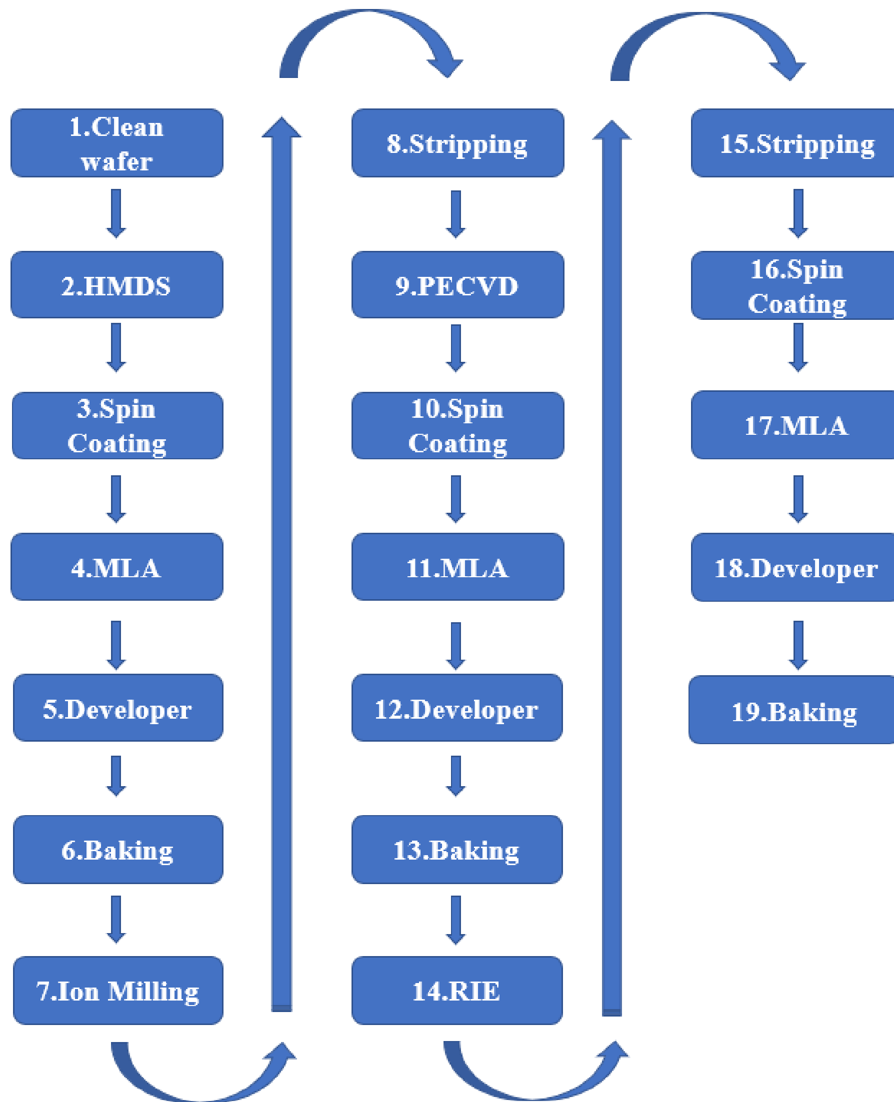


Figure 4.9: Process flow of fabricating prepatterned chip

1. Ultrasonic clean the wafer in isopropyl.
2. Use HMDS to make the subsequent stripping easier
3. Uniform coverage of photoresist on wafer with spin coater
4. Patterning the bottom electrode with MLA
5. Developing the patterned area
6. Baking to make resist resilient to etching
7. Ion milling to etch bottom electrode
8. Stripping off the photoresist
9. Growing SiO_2 with PECVD
10. Uniform coverage of photoresist on wafer with spin coater

11. Patterning SiO_2 with MLA
12. Developing the patterned area
13. Baking to make resist resilient to etching
14. Use RIE to etch out holes in SiO_2
15. Stripping off the photoresist
16. Uniform coverage of photoresist on wafer with spin coater
17. Patterning the top electrode with MLA
18. Developing the patterned area
19. Baking to make resist resilient to etching

Deposition process of ReRAM

The deposition of ReRAM is done on the AJA Twin Chamber sputter and thermal deposition system. It can deposit many materials by magnetron sputtering and thermal evaporation deposition. The deposition chambers have the following features or functions inside.

- Pumping by turbomolecular pump. 685 l/s for the sputtering chamber and 1250 l/s for thermal deposition chamber.
- Heating of the sample up to $800°C$ with a quartz lamp.
- Compatibility with sample sizes as small as 76mm wafer.
- Shared loadlock with a 260 l/s turbo pump to quick pumpdown.
- DC and RF sputtering modes.
- Gas distribution for Ar, N_2 and O_2.

Figure 4.10: AJA Twin Chamber system overview

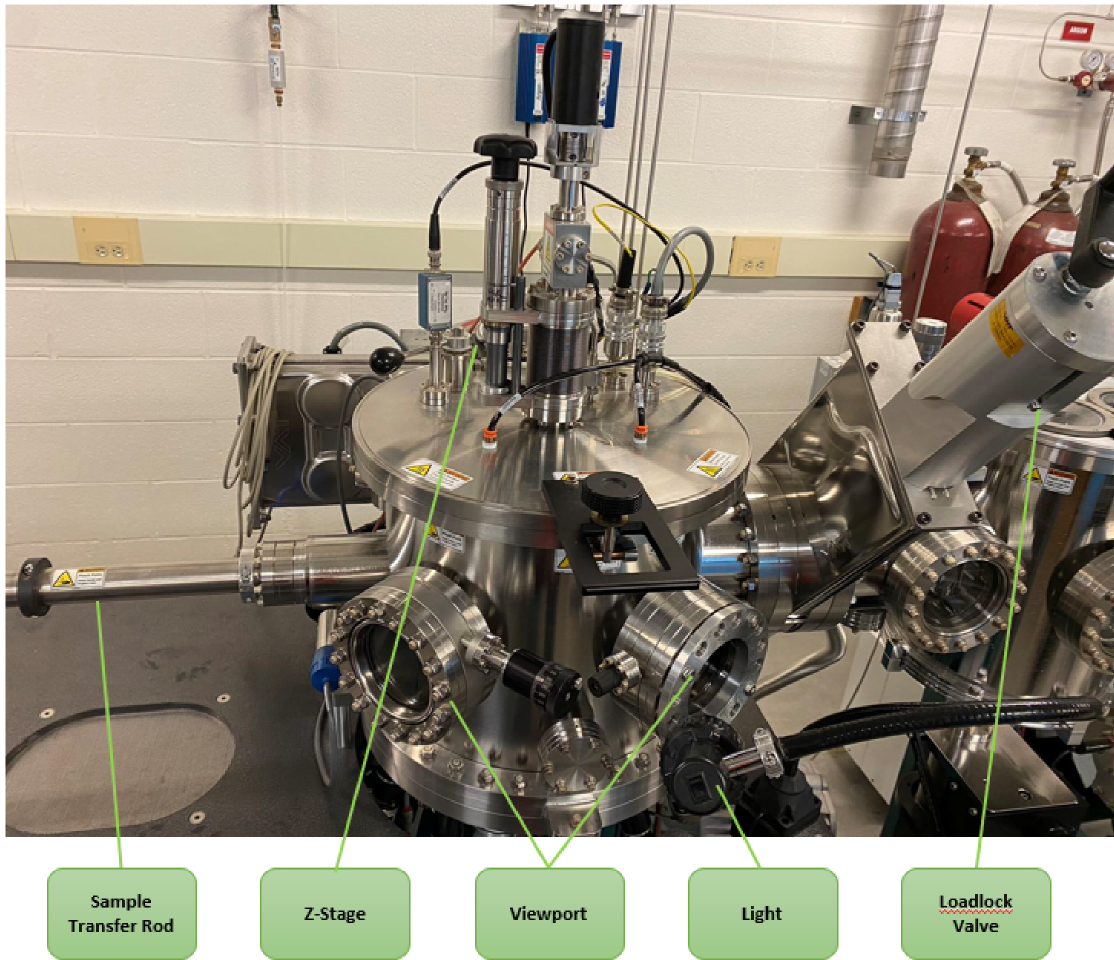


Figure 4.11: Sputter overview

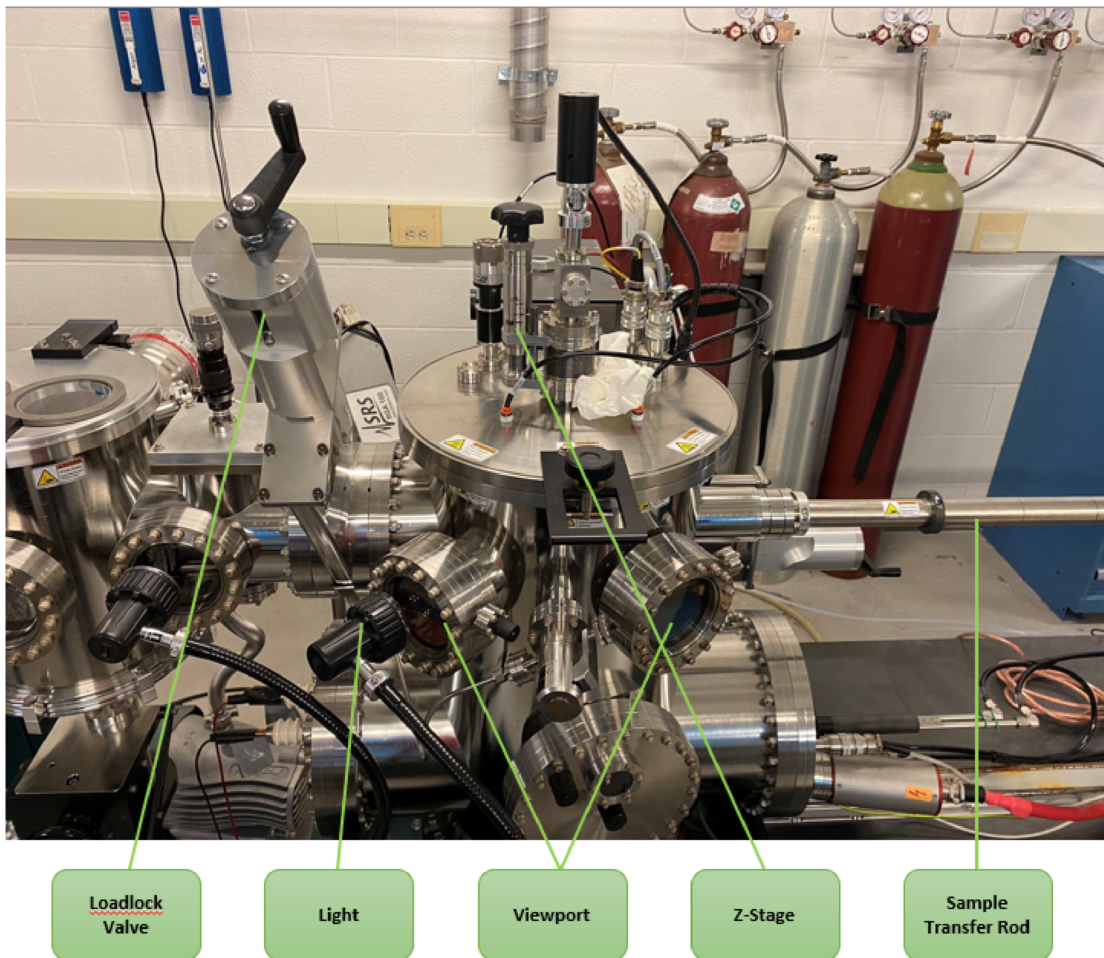


Figure 4.12: E-Beam overview

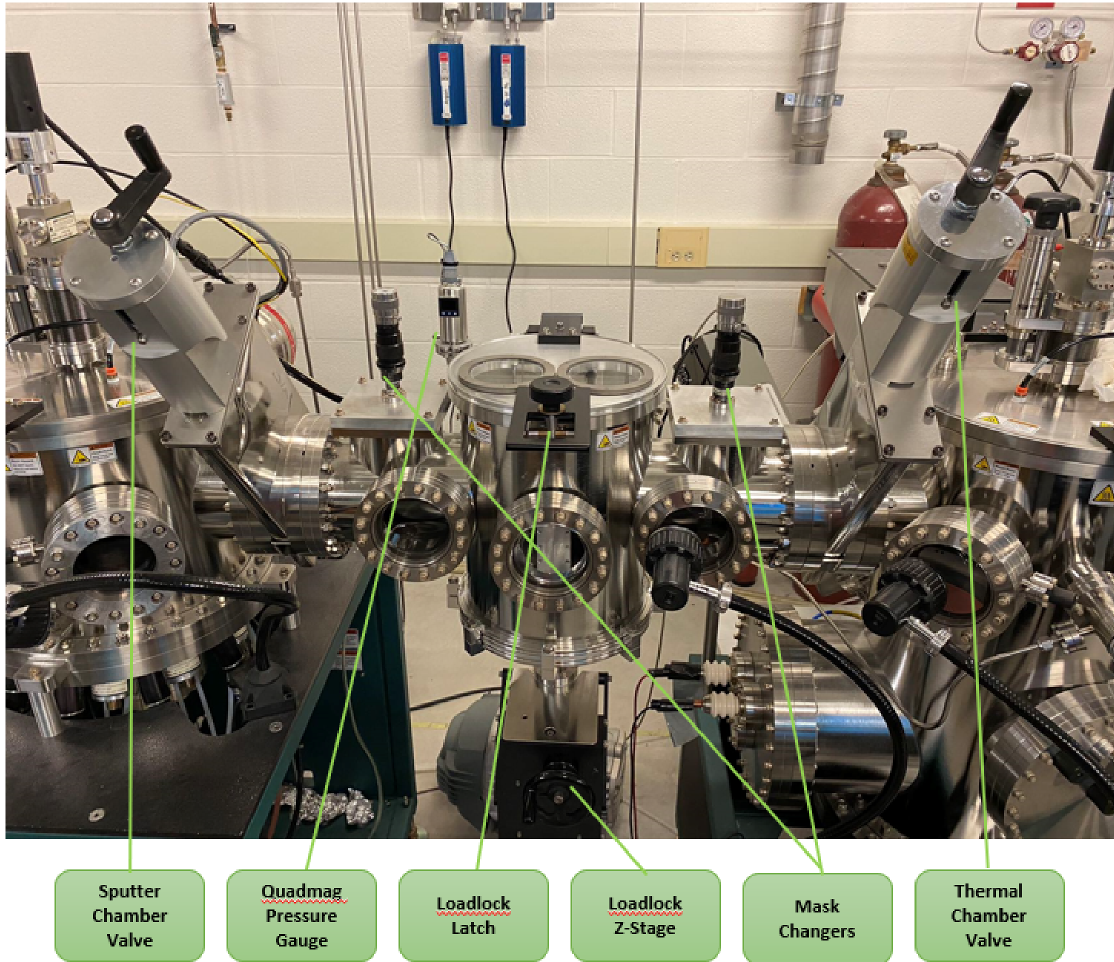


Figure 4.13: Loadlock overview

The deposition process are listed below:

1. Load four pieces prepatterned chips on the chip holder, covered with full mask and mark the position, then put it into loadlock chamber.

2. Transfer the sample into the Sputter chamber and do 1 min back sputtering to make lift off easier.

3. Pre-Sputtering TiO_2 for 10 mins, and then deposite TiO_2 layer.

4. Change the mask from full mask to half mask and transfer into the E-Beam chamber and deposite LiF with average growth rate lower than 0.1 Å$/s$ to get A nm thickness of LiF

5. Change the direction of half mask for 90° and transfer back to E-Beam chamber and deposite LiF with average growth rate lower than 0.1 Å$/s$ to get B nm thickness of LiF. So different thickness of LiF on each pieces are 0 nm, A nm, B nm and $A+B$ nm.

6. Change back to full mask and transfer the sample back into sputter chamber. Pre-sputtering TiN for 10 mins and deposite TiN layer.

7. Pre-sputtering Ti for 10 mins and deposite Ti layer as the adhesion layer.
8. Pre-sputtering Al for 10 mins and deposite Al layer as the protection layer.

4.2.2 Results

From the Figure. 4.14, it can be found the gap between HRS and LRS is larger when the thickness of LiF is increased.

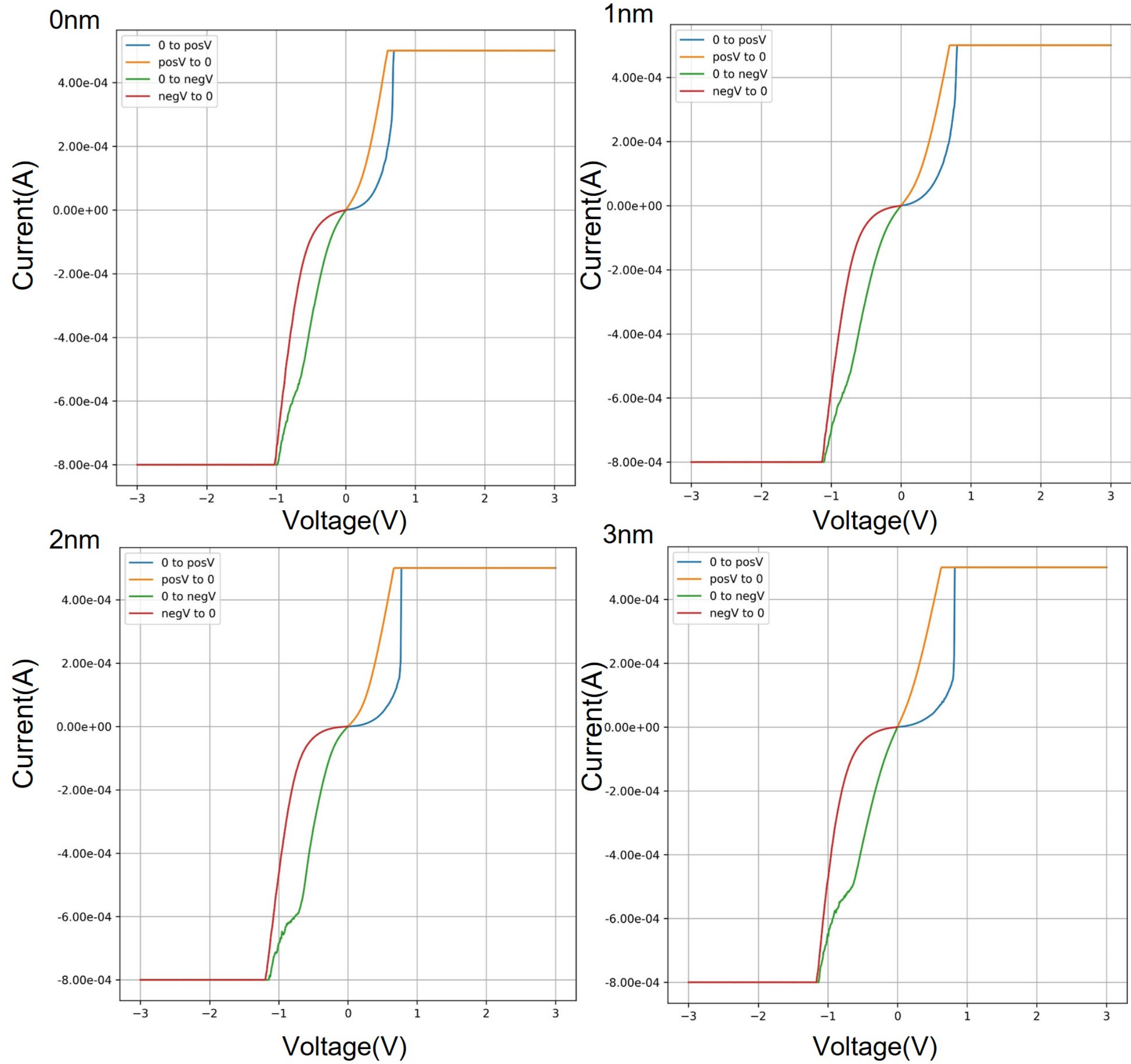


Figure 4.14: I-V curve of $4\mu m$ devices with different thickness of LiF. Where blue line is from 0 to positive, orange is from positive to 0, green is from 0 to negative and red is from negative to 0. blue line and red line indicate the HRS, orange line and green line indicate the LRS.

To obtain objective data, a large batch of streamlined measurements was performed. Initially, a set of devices were measured to determine the preset parameters needed for

the remaining devices. Following the procedures outlined in Figure. 4.15, streamlined measurements were carried out. The measurement process was conducted on four different device sizes and four different LiF layer thicknesses, resulting in a total of 768 devices that were measured and divided into 16 categories.

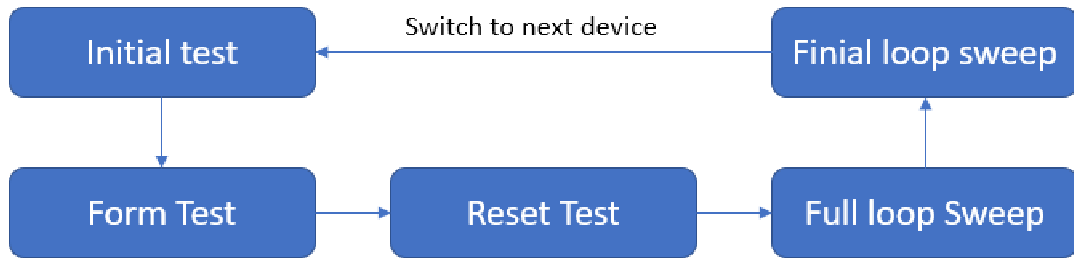


Figure 4.15: Flow chart of measurement

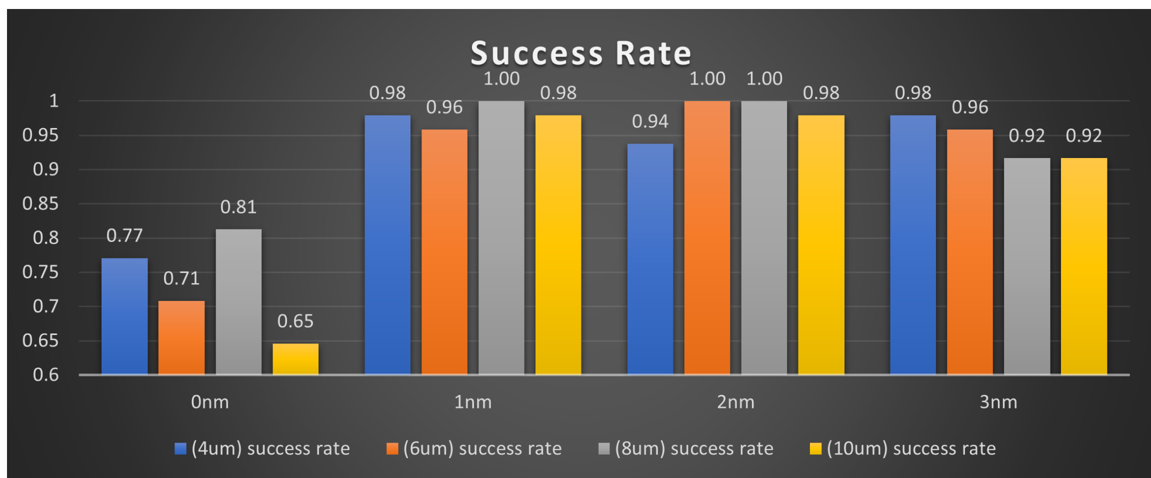


Figure 4.16: Success rate of devices with different thickness of LiF

Figure. 4.16 shows that the device size does not have a significant impact on the success rate, while adding an additional LiF layer greatly improves the success rate. The graph clearly indicates that the success rate of devices without a LiF layer is below 81%. However, once the LiF layer is added, the success rate increases dramatically to over 92%.

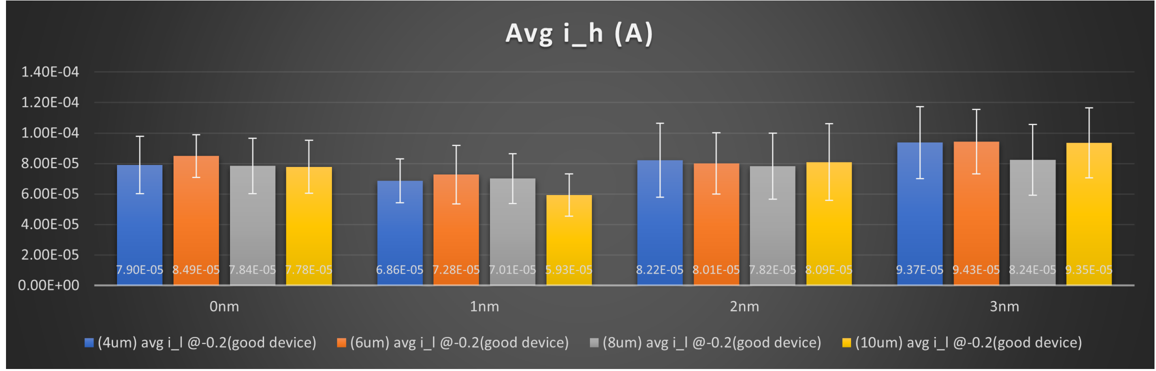


Figure 4.17: Average current for LRS at $V = -0.2V$. (i_h means high current, corresponding to LRS)

From Figure. 4.17, it is evident that in the absence of LiF, the current remains around $8E-5A$ upon the application of a reverse voltage of $0.2V$. However, with the increase in the thickness of the LiF layer, the current initially drops to around $7E-5A$, and then slowly increases to $8E-5A$, and finally to $9E-5A$. This trend remains consistent irrespective of the device size. Additionally, it is observed that for devices without LiF layers, the current decreases with an increase in device size.

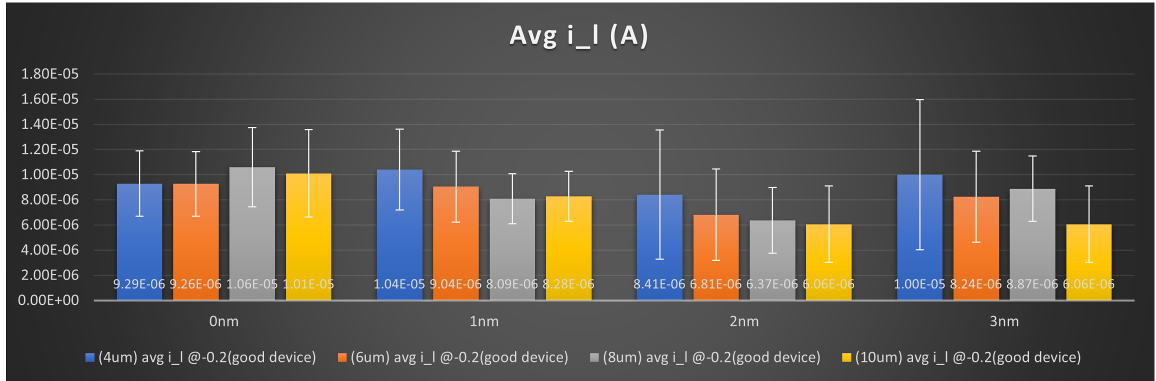


Figure 4.18: Average current for HRS at $V = -0.2V$ (i_l means low current, corresponding to HRS).

From Figure. 4.18, it is difficult to observe a clear trend at first glance. However, upon closer inspection, it can be seen that the histogram of devices with a 2 nm thickness LiF layer is lower compared to its adjacent data points. The H/L ratio is plotted in Figure.4.19 due to the valley in Figure.4.18. It is evident that the H/L ratio tends to increase and then decrease, reaching its maximum when the LiF layer thickness is 2 nm. This suggests that the thickness of the LiF layer can be adjusted to modify the H/L ratio of the device and enhance the differentiation between high and low states.

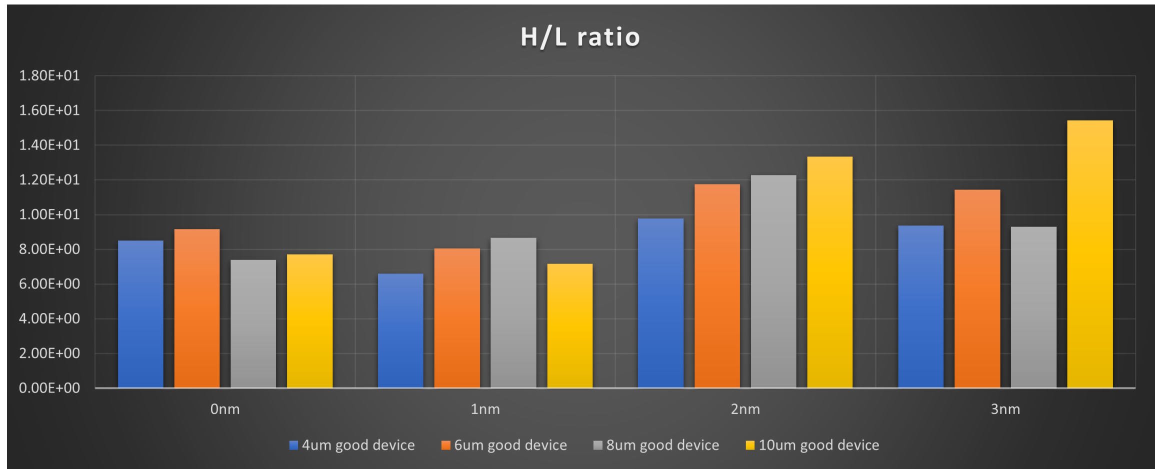


Figure 4.19: HRS/LRS ratio at $V = -0.2V$.

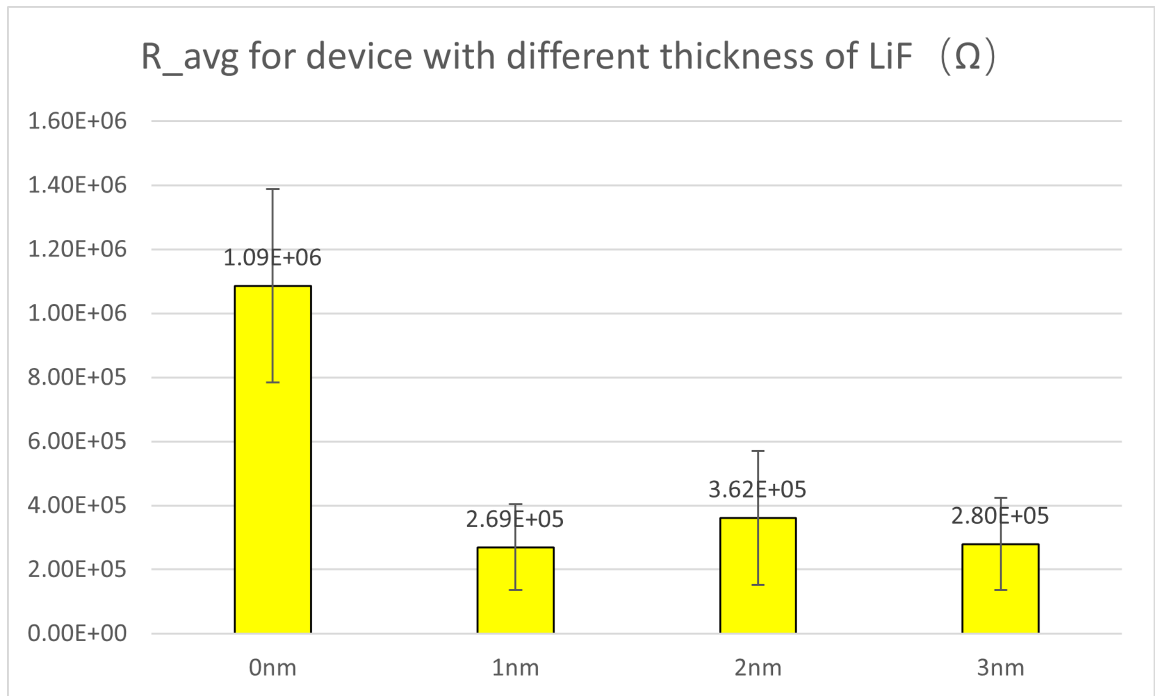


Figure 4.20: The average resistance of fresh devices with different thickness of LiF at I = 1 μ A.

The data presented in Figure. 4.20 suggests that the initial resistance of the device decreases significantly with the addition of lithium fluoride. This implies that the introduction of LiF results in an increase in the number of defects in the device.

4.2.3 Discussions

It can be seen from the Figure. 4.16 that the success rate will be greatly increased with the addition of Li. This is because the introduction of Li is equivalent to the

introduction of more oxygen-hole defects, which can form CF, so the formation of CF will become easier as the number of oxygen-hole defects increases, and another reason is that the resistance will decrease with the increase of oxygen-hole defects, which will also reduce the chance of hard breakdown. Due to the high yield rate, the LiF enhanced ReRAM and its prepatterned chip recipe are ready for the mass fabrication for CMOS.

Based on the data shown in Figure. 4.20, it can be observed that the initial resistance of the device decreases significantly with the addition of lithium fluoride. This is because the introduction of Li increases the number of oxygen vacancies in the material, resulting in increased conductivity.

It can be seen from the Figure. 4.17 and 4.18 that the response of the high and low resistance states to the addition of Li is different. LiF itself is an insulator, and with the addition of LiF, the resistance of the device increases in both the high and low states, and when enough LiF is added, the oxygen-hole defect caused by Li also starts to take effect, which is less for the high resistance state and more for the low resistance state. The effect of hesitant Li on the high and low resistance states is identical, resulting in different and increasing H/L ratios and reaching a relatively high point at 2 nm. Increasing the H/L ratio also helps to improve the performance of the RAM device, making the resistive states easier to distinguish, read and write.

In addition, After adding Li we also observed the volatile behavior, first adding a stable voltage, the device current would slowly increase, withdrawing the voltage, waiting a while and remeasuring, the current would be lower than the previous end state and then would slowly increase. While it may not be suitable for memory devices, it is advantageous for studying neuronal computation.

Chapter 5

Summaries and Prospections

This thesis first introduces the different RAMs and focuses on the recent research results of ReRAM, and describes the relevant equipment and fabrication process of the devices needed for the preparation of the experiments. Then the results obtained from the experimental tests are analyzed.

In the first experiment, a battery-like magnetic tunneling junction is demonstrated and it is shown that it can be electromagnetically tuned. In this LiF-based device, reversible non-volatile resistive switching phenomena, and tunneling phenomena coexist, and it is this coexistence that allows four well-defined groupings of each device. The control of the interface makes the spin transport of actively regulated devices feasible, making them more promising for applications. The disadvantage is that to observe the TMR requires observation at low temperatures.

In the second experiment, Li embedding in a material equivalent to increase in oxygen vacancy defects, leading to a decrease in resistance and an increase in electrical conductivity. Additionally, Li embedding can improve the success rate of the material in achieving the resistive switching phenomenon by reducing dielectric breakdown. Furthermore, Li embedding can affect the ratio, which is the ratio of the resistance of HRS and LRS, affecting the magnitude of the electrical properties of the material.

Overall, Li embedding is a significant material modification technique that can have a significant impact on the electrical properties of the material. However, it should be noted that the incorporation of Li also results in some resistive volatility, which has both positive and negative effects. While it is not ideal for memory devices, it is beneficial for studying neuronal computation. And the recipe of prepatterned chip and Li enhanced ReRAM are ready for mass fabrication of CMOS.

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