Nanocrystalline Silicon Thin Film Transistor

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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I understand that my thesis may be made electronically available to the public.

Mohammad-Reza Esmaeili-Rad

Abstract

Hydrogenated amorphous silicon (α-Si:H) thin film transistor (TFT) has been used in active matrix liquid crystal displays (LCDs) and medical x-ray imagers, in which the TFT acts as pixel switches. However, instability of α-Si:H TFT is a major issue in applications where TFTs are also required to function as analogue circuit elements, such as in emerging organic light emitting diode (OLED) displays. It is known that α-Si:H TFT shows drain current degradation under electrical operation, due to two instability mechanisms: (i) defect creation in the α-Si:H active layer, and (ii) charge trapping in the gate dielectric. Nanocrystalline silicon (nc-Si) TFT has been proposed as a high performance alternative. Therefore, this thesis focuses on the design of nc-Si TFT and its outstanding issues, in the industry standard bottom-gate structure.

The key for obtaining a stable TFT lies in developing a highly crystalline nc-Si active layer, without the so-called amorphous incubation layer. Therefore, processing of nc-Si by plasma enhanced chemical vapor deposition (PECVD) is studied and PECVD parameters are optimized. It is shown that very thin (15 nm) layers with crystallinity of around 60% can be obtained. Moreover, it is possible to eliminate the amorphous incubation layer, as transmission electron microscope (TEM) images showed that crystalline grains start growing immediately upon deposition at the gate dielectric interface.

The nc-Si TFT reported in this work advances the state-of-the-art, by demonstrating that defect state creation is absent in the nc-Si active layer, which is deduced by performing several characterization techniques. In addition, with the proper design of the nitride gate dielectric, i.e. by using a nitrogen-rich nitride, the charge trapping instability can be minimized. Thus, it is shown that the nc-Si TFT is much more stable than the α-Si:H counterpart.

Another issue with nc-Si TFT is its high drain leakage current, i.e. off-current. It is shown that off-current is determined by the conductivity of nc-Si active layer, and also affected by the quality of the silicon/passivation nitride interface. The

off-current can be minimized by using a bi-layer structure so that a thin (15 nm) nc-Si is capped with a thin (35 nm) α-Si:H, and values as low as $0.1\,pA$ can be obtained.

The low off-current along with superior stability of nc-Si TFT, coupled with its fabrication in the industry standard 13.56 MHz PECVD system, make it very attractive for large area applications such as pixel drivers in active matrix OLED displays and x-ray imagers.

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Dedication

To my parents and wife, Zahra

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Chapter 1

Introduction

1.1 Macroelectronics

Microelectronics technology based on crystalline semiconductors, mainly silicon, has revolutionized human life style by offering uncountable products in communication, computation, health, space, and entertainment sectors, to name a few. In microelectronics, the trend has been to follow the Moore's law of scaling by shrinking the length of transistors from several micrometers to several tens of nanometers, in order to increase the speed of transistors and also the number of transistors per unit area. However, there are applications in which sophisticated transistors are not required and low-speed, micrometer-size transistors are sufficient, with the goal to spread electronic components over large area substrates at low fabrication cost. These applications are known as large-area electronics as well as macroelectronics [1, 2]. For example, in a flat panel display, electronics are required to control the operation of individual pixels over areas as large as $1\,m^2$. For comparison, the current crystalline silicon technology is limited to substrate area of around $0.3\,m^2$. Medical x-ray imager is also another important application of macroelectronics.

Implementing macroelectronics using the conventional microelectronics, based on crystalline technologies, becomes cost-prohibitive [2]. Therefore, in response to this shortcoming, thin film technologies have been developed to deposit and process

electronic materials over non-crystalline substrates such as glass, plastics, and metal foils. Among them, several forms of thin film silicon, namely, hydrogenated amorphous silicon (α-Si:H) and polycrystalline silicon (polysilicon), and their associated thin film transistors (TFTs) play a key role in macroelectronics [3].

Thin film technologies and macroelectronics have already grown to a big industry, which is currently centered around flat panel electronics and liquid-crystal displays (LCDs). For example, it has been forecasted that the worldwide market for LCDs will reach \$118 billion in 2010 [4]. On the other hand, the market for a new generation of displays, i.e. organic light emitting diode (OLED) displays, will reach about \$2.5 billion by 2012 [5].

Figures 1.1 (a) and (b) show images produced by an OLED display and an x-ray imager, respectively. On these panels, TFTs control the operation of individual pixels forming the image. Usually, the display or imager panel is designed as a matrix so that pixels are located at row and column intersections and controlled by their dedicated pixel circuit. In this case, the panel is called an *active matrix array*. The concept is the same for both display and imager cases, the only difference is the detail of pixel circuits. In what follows, the concept of an *active matrix array* is discussed in further details.

1.2   Active Matrix Arrays

Figure 1.2 (a) illustrates an active matrix array. It may represent an x-ray imager, LCD, or OLED display. Here, rows are sequentially scanned and activated by row driver circuitry and picture information (video signal) is transferred to pixel circuits row by row, by column driver circuits in the case of a display. If it is an x-ray imager, the image data is read out via column drivers once a row is selected. Row driver circuitry is essentially the same in both display and imager cases.

On the other hand, pixel circuits are application specific as shown in Figs. 1.2 (b),(c), and (d) for x-ray imager, LCD, and OLED display, respectively. In Fig.

<div align="center">(a)   (b)</div>
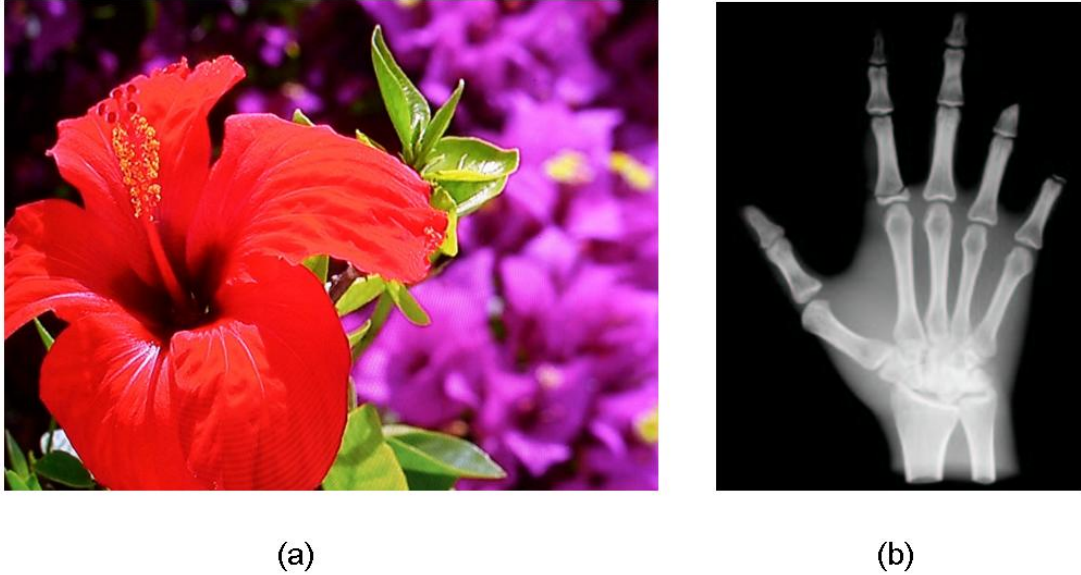
Figure 1.1: The panel outputs generated by an (a) OLED display and (b) x-ray imager. Pictures are from [6] and [7].

1.2 (b), when x-rays are incident on the detector, electrical charges are created and integrated on the storage capacitor (C_S). After a charge integration period, the TFT, labeled as S-TFT, is turned on by the row voltage and the generated signal is passed to the readout (column driver) circuitry. The TFT is then turned off for next integration cycle [8]. Figure 1.3 shows a photomicrograph of a real x-ray active matrix array, showing several rows and columns along with detection area and TFTs [7].

In LCDs, Fig. 1.2 (c), each pixel is a capacitor, labeled as C_{LC}, since liquid crystal (LC) molecules are sandwiched between two transparent electrodes. When the row voltage goes high, the TFT is turned on and the video voltage is transferred to the pixel. The C_S helps to stabilize the voltage across the pixel. Subsequently, the liquid crystal modulates the intensity of light coming from the backlight proportional to its voltage (V_{OUT}) [9]. Here, we notice that the pixel TFT (S-TFT) is simply acting as a switch, and that LCDs are driven by a voltage signal.

In contrast to LCD, which is voltage-driven, OLED is a current-driven device. Hence, the video voltage should be converted into a current signal, which is done by

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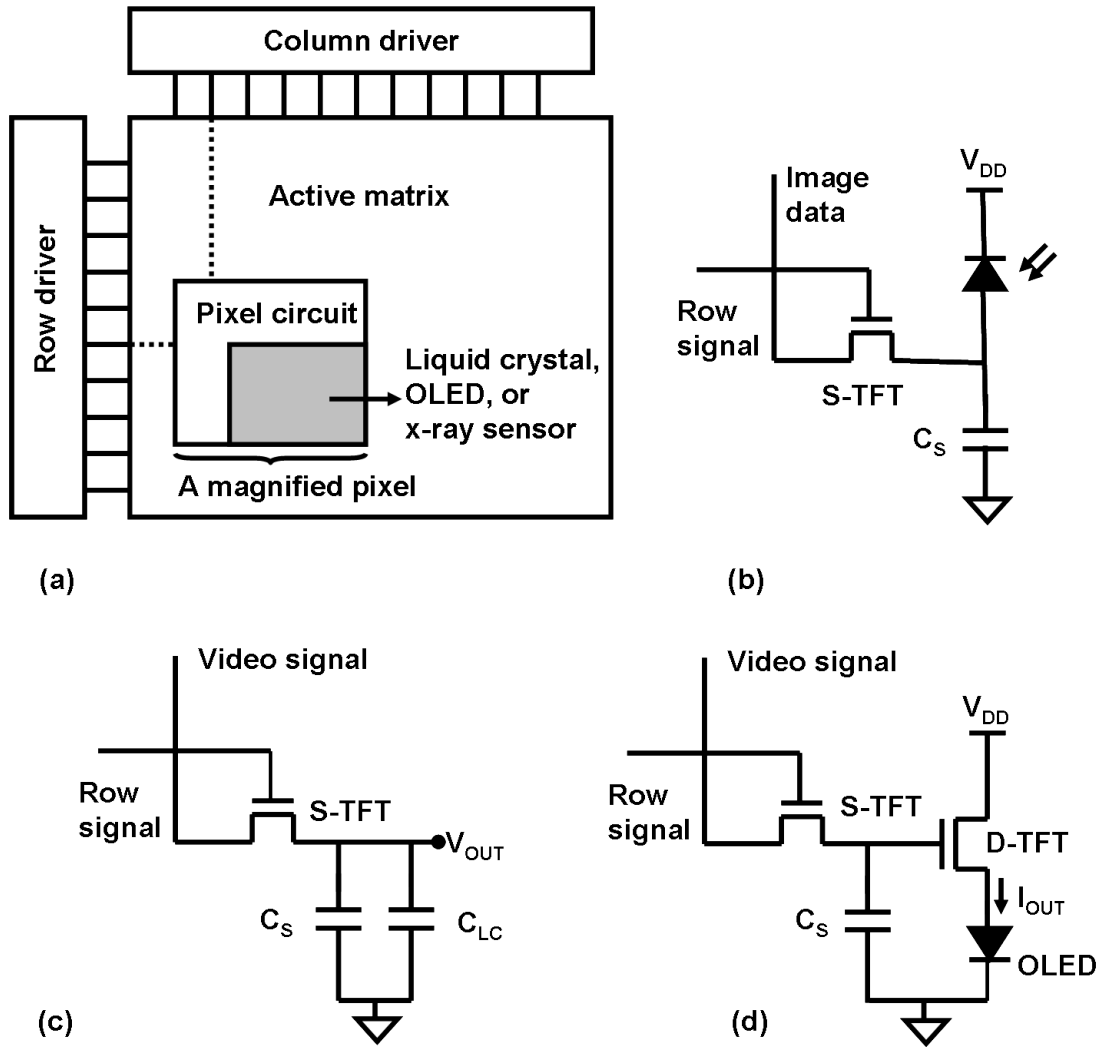
Figure 1.2: (a) The concept of active matrix array, and basic pixel circuits in (b) x-ray imager, (c) liquid crystal display, and (d) organic light emitting diode display.
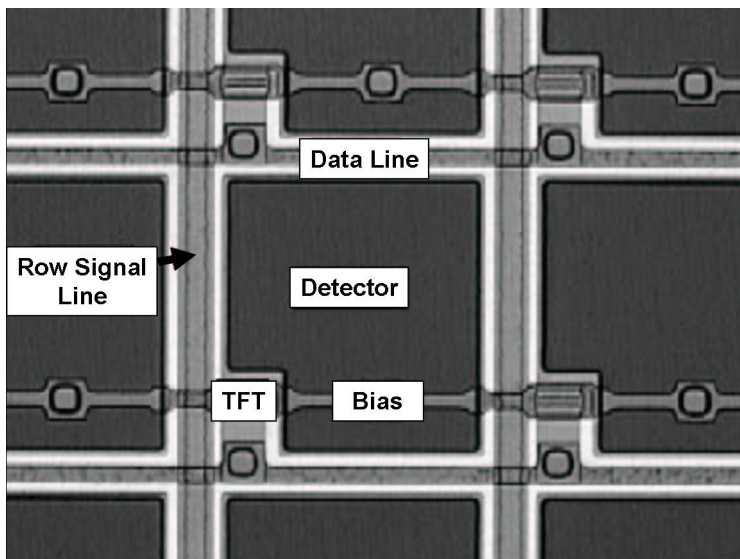
Figure 1.3: Photomicrograph of an x-ray active matrix array. From Ref. [7].

the current-driver transistor (D-TFT) in Fig. 1.2 (d), showing a basic pixel circuit in OLED displays. The other components, i.e. C_S and switching TFT (S-TFT), function similar to those in the LCD pixel circuit. When the row voltage goes high, S-TFT is turned on and the video voltage signal is transferred to the C_S. Subsequently, the D-TFT converts the video voltage to an output current (I_{OUT}) for the OLED pixel. The generated light by OLED is proportional to I_{OUT} and thus to the applied video signal [9].

In this thesis, we will be only discussing TFTs that are used in pixel circuits, shown in Figs. 1.2 (b),(c), and (d). The subject of row/driver circuitry is out of the scope of this research. Pixel transistors usually operate at low frequencies and thus moderate and low performance characteristics, e.g. mobility, are sufficient, since the refresh rate of displays is slow and in the range of 60-120 frames per second. In the next section, several TFT technologies that are under research and development or already matured are introduced, in order to make it clear that what kind of transistors can be used in various pixel circuits on active matrix arrays.

1.3 Thin Film Materials and Transistor Technologies

1.3.1 Hydrogenated Amorphous Silicon

Hydrogenated amorphous silicon (α-Si:H) is deposited by plasma enhanced chemical vapor deposition (PECVD), using silane (SiH_4) or a mixture of silane and hydrogen (H_2) source gases at temperatures of less than 300 °C. This low temperature process along with the amorphous nature of used substrates, e.g. glass, lead to formation of amorphous materials lacking structural order like that of crystalline silicon [11]. Figures 1.4 (a) and (b) show a two-dimensional representation of atomic bonding in α-Si:H and crystalline silicon, respectively [10].

In the crystalline structure, silicon atoms occupy specified locations with a uniform bond length and angle, while in the amorphous case, there are missing atoms and slight variation in bond length and angle. This structural disorder has a strong bearing on electrical properties of the α-Si:H. For example, *deep defect states* in the energy gap of α-Si:H are associated with missing atoms, i.e. dangling bonds, and the deviation in bond length and angle results in states below the conduction band, commonly known as *band tail states*. Figure 1.5 (a) shows an example of distribution of states in the energy gap of the α-Si:H [10, 11].

(a)   (b)
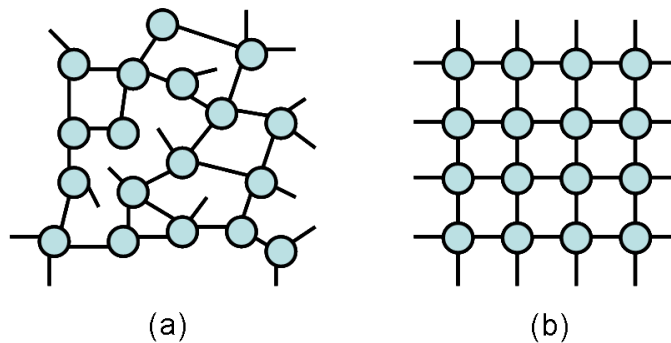
Figure 1.4: Two dimensional representation of atomic bonding in (a) α-Si:H and (b) crystalline silicon (adapted from [10]).

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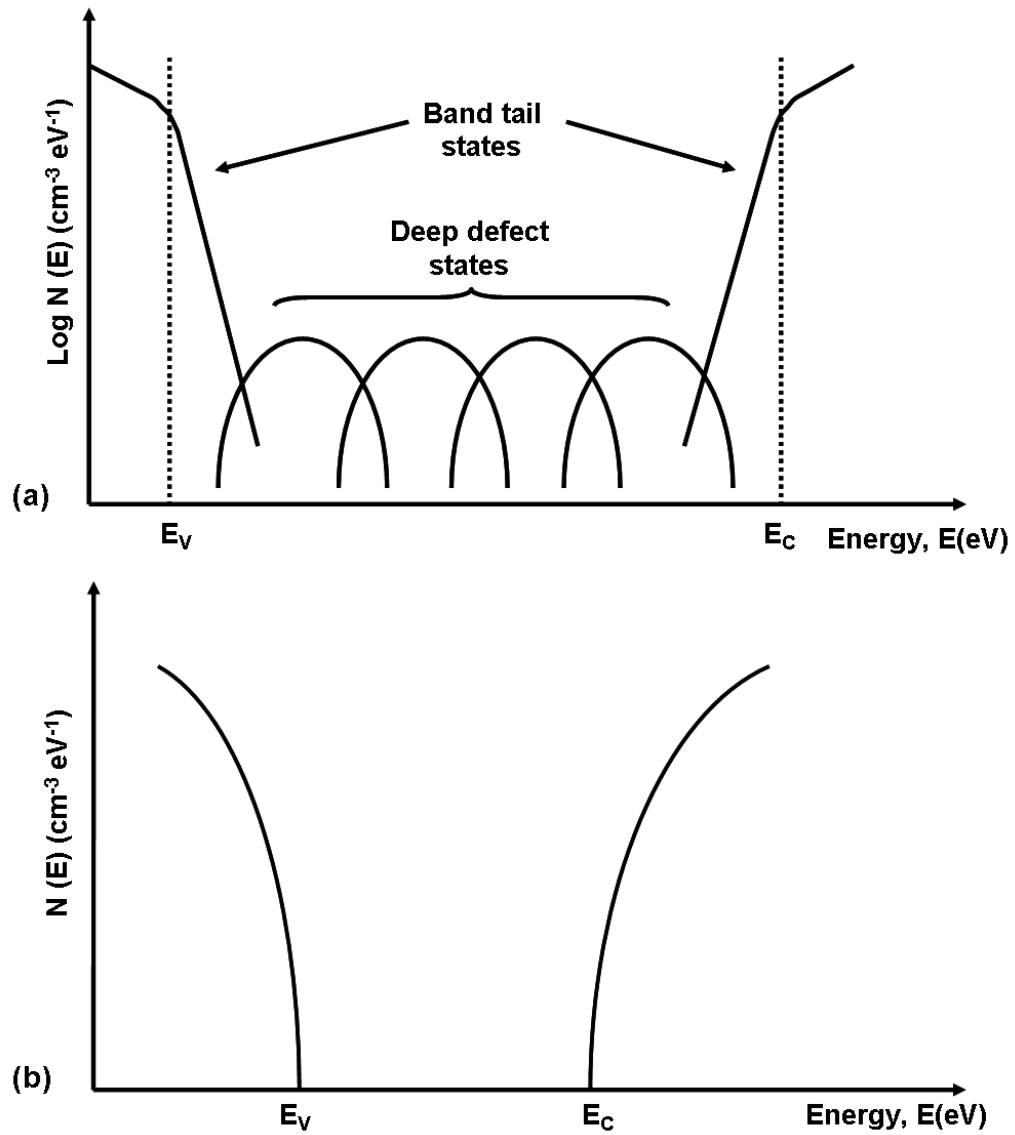
Figure 1.5: Distribution of density of states in (a) α-Si:H and (b) crystalline silicon. Adapted from [10, 12]. $N(E)$ is in log scale in (a), and scaling is not accurate.

The density of *deep defect states* in α-Si:H is in the range $10^{15} - 10^{18}\, cm^{-3} eV^{-1}$, which is largely dependent on PECVD conditions. Fortunately, atomic hydrogen that is generated during PECVD passivates a portion of dangling bonds, reducing the density of defect states [10, 11].

When α-Si:H is used in TFTs as the active layer, the resulting field-effect mobility (μ_{FE}) is in the range of $0.1 - 1\, \frac{cm^2}{V.s}$. The low μ_{FE} is attributed to large density of band tail states; Indeed, electrons are frequently trapped into and released from band tail states leading to the low mobility [11]. This concept will be explained in further details, in chapter two. Consequently, α-Si:H TFTs are inferior to crystalline silicon (c-Si) transistors, although their low mobility is sufficient for LCDs and they are being used in commercial products [13].

Another drawback of α-Si:H TFT is its instability. When it is subject to a prolonged gate voltage, the drain-source current (I_{DS}) is observed to gradually decrease over time, associated with a shift in its threshold voltage (ΔV_T). The causes of ΔV_T will be discussed in chapter two. The instability issue is not a major concern in LCD and x-ray imager pixel circuits, shown in Figs. 1.2 (b) and (c), due to the fact that their TFTs are not subject to prolonged gate voltages. Here, TFTs act as simple switches with a short duty cycle, i.e. they are turned on for several tens of microseconds to pass the video signal and turned off for around ten milliseconds, subsequently. On the other hand, it is very difficult to use α-Si:H TFTs as analog circuit elements, as in this case they have to operate continuously, i.e. they are subject to prolonged gate biases. One particular area of interest is OLED displays. Referring to Fig. 1.2 (d), the D-TFT is an analog current driver. The D-TFT should be able to provide a stable current for OLED for generating a uniform and stable output light. Currently, the instability of α-Si:H TFT is the major issue against implementation of active matrix arrays for OLED displays [14], to which we hope to contribute.

1.3.2 Polycrystalline Silicon

When amorphous silicon is subject to an annealing process, it can be transformed into polycrystalline silicon (poly-Si). Crystallization can be performed either by thermal annealing in furnace at temperatures around $600 - 700\,^\circ\text{C}$ or by laser annealing. Poly-Si can also be formed by a variety of other methods. For example, it can be directly deposited by thermal decomposition of SiH_4 at approximately $600\,^\circ\text{C}$ by a process known as *low-pressure chemical vapor deposition* (LPCVD), and also by *metal induced crystallization* process at temperatures lower than $600 - 700\,^\circ\text{C}$ [10, 13].

In general, poly-Si is viewed as a network of randomly oriented crystalline grains interconnected by thin (only 1-2 atomic layers) grain boundaries, illustrated in Fig. 1.6. Here, the quality of grains can be high and virtually defect-free, while grain boundaries possess large concentration of defects, dangling bonds. The grain size is dependent on the crystallization method and varies from tens of nanometers to several micrometers [13]. From the standpoint of device mobility, larger grains are preferred as the average defect density is smaller [10]. In addition, for a given TFT length, a larger grain size results in fewer grain boundaries across the channel, leading to less trapping of carriers at grain boundaries and, hence, higher mobility. Overall, when an annealing method results in fewer intragrain defects, device mobility is higher [13].

For example, electron mobilities in the range $10 - 50\,\frac{cm^2}{V.s}$ and $50 - 300\,\frac{cm^2}{V.s}$ are easily obtained by thermal and laser annealing, respectively [13]. Developing advanced laser annealing techniques, mobilities as high as $450 - 566\,\frac{cm^2}{V.s}$ and $200\,\frac{cm^2}{V.s}$ have been achieved for electrons and holes, respectively, approaching those of c-Si transistors [15, 16].

Therefore, high mobility poly-Si TFTs can be used for integration of row and column drivers on display panel, as they provide sufficient electron and hole mobilities in n-type and p-type devices for CMOS operation. The integration of row and column drivers is not feasible by α-Si:H TFTs, as carrier mobilities much greater
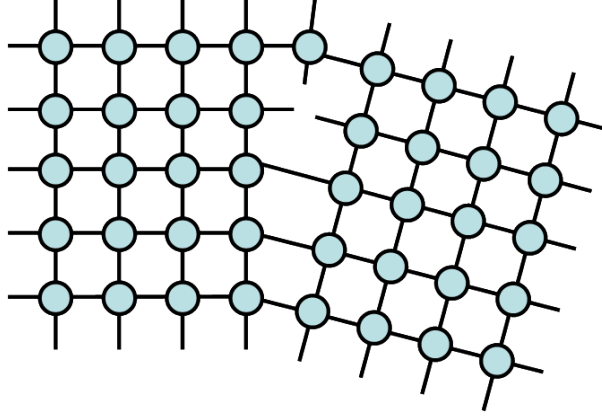
Figure 1.6: Representative 2D atomic bonding in poly-Si (adapted from [10]).

than that of α-Si:H TFT is required [10]. In addition, poly-Si devices are much more stable than the α-Si:H counterpart [14].

Unfortunately, poly-Si technology is not without issue. For example, it is more expensive than α-Si:H, as it needs expensive tools such as excimer laser for annealing, ion implanter for making source/drain doped contacts, and rapid thermal annealing tool for dopant activation. These tools are specific to poly-Si technology. Poly-Si is also suffering from poor spatial uniformity, mainly because of the crystallization step and random positioning of grain boundaries along the transistor channel. For example, one poly-Si TFT may have one grain boundary across its channel, while another one may have three grain boundaries. This non-uniformity leads to mobility and threshold voltage non-uniformity over large area substrates. Currently, this technology has been applied to active matrix arrays of ≤ 11" in diagonal, due to the cost and non-uniformity drawbacks [9, 13].

Table 1.1 summarizes the attributes of poly-Si and α-Si:H technologies [9]. We notice that poly-Si is able to provide n-type and p-type TFTs, while in α-Si:H technology, the only usable device is n-type. Here, the hole mobility is around two orders of magnitude smaller than that of electrons, which is practically useless. As mentioned earlier, poly-Si TFTs have been used in smaller panels (≤ 11" in diagonal) since the overall cost is lower and row/column drivers can be integrated on the panel. However, for larger panels it is preferred to use α-Si:H TFTs as the

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Table 1.1: Attributes of poly-Si and α-Si:H TFT technologies. From Ref. [9].

TFT Attribute	Poly-Si	α-Si:H
Type	N-MOS and P-MOS	N-MOS
Electron Mobility ($cm^2/V.s$)	10-500	0.1-1
Cost (array only)	High	Low
Cost (module)	Low (Built-in row/column driver)	High (External driver)
Overall Cost	Lower for small panels	Lower for large panels
Equipment Investment	High	Low
Uniformity	Worse	Better
Current stability	High	Low

production cost is lower. In this case, we have to use external row/column drivers, which are usually crystalline silicon CMOS chips and mounted on the periphery of the active matrix array.

There have been continuous efforts to improve the performance characteristics of these two technologies. For example, advanced laser annealing methods are being developed in order to increase the carrier mobility of poly-Si TFTs as well as to improve the uniformity over larger areas [15, 16]. For the case of α-Si:H, further improvement seems to be impossible. Thus, research efforts have been directed to newer technologies such as nanocrystalline silicon, also called microcrystalline silicon, in order to boost device parameters such as mobility and electrical stability [3, 17, 18].

Indeed, α-Si:H technology has several appealing attributes; it does not need costly tools such as ion implanter and excimer laser, and can be processed over large areas (over $2m \times 2m$) [19]. For example, currently, eight 46" LCD panels are produced on a single piece of glass by PECVD processes, so called generation (Gen) 8 [20]. Therefore, if a technology compatible with α-Si:H, in terms of fabrication

and facilities, could provide higher mobility and stability, it would be easily adopted by industry. In the next section, we introduce nanocrystalline silicon technology and review its properties.

1.3.3 Nanocrystalline Silicon

Nanocrystalline silicon (nc-Si) technology is fully compatible with the α-Si:H and employs the same tools for device processing. The logical way for boosting device performance parameters is to change the material microstructure and move from the amorphous phase without any structural order, and towards crystalline or poly-crystalline phases with some degree of structural order. To preserve compatibility with α-Si:H, one approach is to only modify the plasma chemistry and PECVD processes. In this case, we avoid using laser annealing as used in poly-Si TFTs and, thus, its associated issues.

Earlier we noted that SiH_4 and H_2 source gases are used in PECVD for α-Si:H deposition. It was found that if the H_2/SiH_4 gas flow ratio becomes large (e.g. ≥ 10), the material microstructure changes and comprises of crystalline grains of less than $50\,nm$ in diameter embedded in an amorphous matrix [21, 22]. Figure 1.7 shows a 2-D representation of atomic bonding in nc-Si. This material is known as nc-Si due to size of crystalline grains. It is interesting to note that although nc-Si contains amorphous phase, it was observed that its electrical stability was significantly improved when the volume fraction of crystalline grains exceeds $60\,\%$ [17, 23].

In designing nc-Si TFTs, we should consider an important feature of nc-Si regarding its structure, shown in Fig. 1.8. When nc-Si grows on an amorphous substrate such as glass, its structure is not highly crystalline in the beginning. It may be entirely amorphous or comprised of very small grains of just a few nanometers with dominant amorphous phase. When the film grows thicker, the grain size increases and the film becomes highly crystalline with very little amorphous phase [22]. This structural difference at the bottom and at the top of the film has
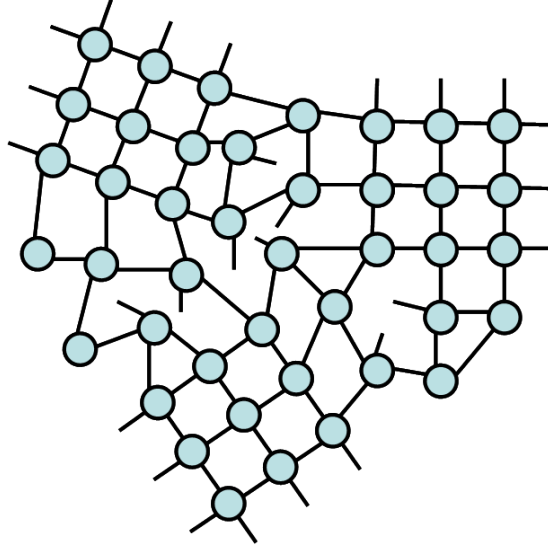
Figure 1.7: Two dimensional representation of atomic bonding in nc-Si (adapted from [24]).

implications for device design.

If one makes a nc-Si TFT with gate metal and gate dielectric at the bottom, as shown in Fig. 1.9 (a), the device performance is determined by the quality of bottom layers of nc-Si, where the conduction channel is formed. Alternatively, it is possible to put the gate dielectric and gate metal on the top and make the so called *top-gate* TFT, shown in Fig. 1.9 (b). In this case, the conduction channel will be formed in the highly crystalline part of the nc-Si film. Hence, it is expected that top-gate nc-Si TFTs render better performance than bottom-gate devices [3].

For top-gate devices, Cheng et al. [25] and Lee et al. [18] have reported field-effect mobility of 40 and 150 $cm^2/V.s$, respectively. For bottom-gate TFTs, mobilities in the range $0.5 - 3\, cm^2/V.s$ have been reported [26, 27]. In the next section, we review issues and challenges of nc-Si TFTs.
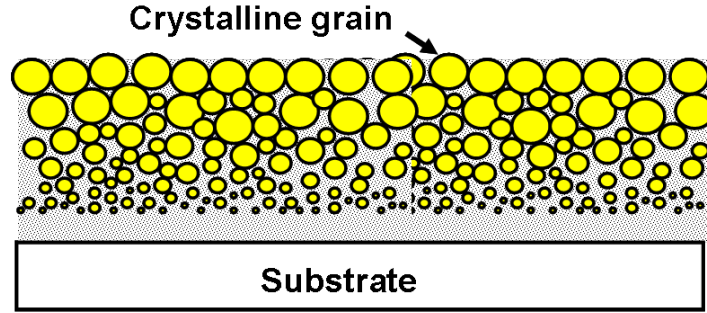
Figure 1.8: Material structure of nc-Si. It is inhomogeneous and comprises of small grains near the substrate and larger grains when thickness increases (adapted from [22]).
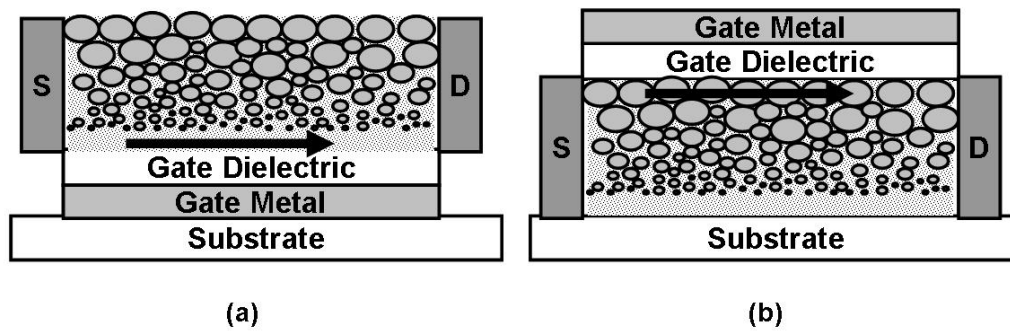
Figure 1.9: Two nc-Si TFT structures, (a) bottom-gate and (b) top-gate. The arrow represents the conduction path.

1.4 Challenges for Nanocrystalline Silicon Thin Film Transistors

1.4.1 Top-gate Structure

In top-gate structure, Fig. 1.9 (b), the gate dielectric can be either silicon dioxide (SiO_2) or hydrogenated amorphous silicon nitride (α-SiNx:H). Thus far, high mobility TFTs have been achieved using SiO_2, not α-SiNx:H. Reported mobilities are in the range of $11 - 150\,cm^2/V.s$ [18, 25, 28, 29, 30] and $0.5 - 2\,cm^2/V.s$ [17, 31, 32] for SiO_2 and α-SiNx:H gate dielectrics, respectively. Hence, SiO_2 is the preferred dielectric for top-gate configuration, as it is for poly-Si and crystalline

silicon transistors, too.

Unfortunately, a major issue with SiO_2, which is deposited by PECVD at temperatures below $300\,^{\circ}\mathrm{C}$, is its poor insulating quality that leads to high gate leakage current and severe charge trapping in SiO_2 and, thus, device instability [18, 33]. In other words, SiO_2 forms a good interface with nc-Si that results in a high mobility, but its bulk insulating quality is poor [33]. On the other hand, α-SiNx:H forms a low quality interface with nc-Si that leads to a low mobility, although it has a good bulk insulating property. For this reason, α-SiNx:H is widely used in bottom-gate α-Si:H TFTs and display industry and has yielded low gate leakage current and device-grade insulating quality.

Another problem is that the top-gate structure, shown in Fig. 1.9 (b), is not commonly used in industrial production lines. Usually, industry is very reluctant to change its working setup, which is currently based on bottom-gate configuration, unless they see a significant shift in performance and benefits.

1.4.2 Bottom-gate Structure

The bottom-gate structure, Fig. 1.9 (a), is the current industrial standard and widely used in the manufacturing of LCDs. For this reason, bottom-gate nc-Si TFT with improved performance compared to its α-Si:H counterpart, would be easily adopted by industry [27].

A major issue with this configuration is the quality of initial layers of nc-Si close to the gate dielectric interface. Often times, it is found that initial layers are fully amorphous, so called amorphous incubation layer [27]. The incubation layer thickness depends on PECVD conditions and could be as thick as several tens of nanometers. Above this layer, small crystalline grains grow and their size gradually increases when the film becomes thicker [22].

If the amorphous incubation layer of considerable thickness exists, the nc-Si TFT behaves the same as α-Si:H devices, since the conduction channel is within $10\,nm$

from the gate dielectric interface [34]. For example, the amorphous incubation layer leads to device instability, similar to that observed in α-Si:H TFTs. Thus, it should be eliminated and crystallinity of initial layers should be high to achieve stable TFTs [27].

Bottom-gate nc-Si TFTs have been reported by several groups [26, 27, 32, 35]. However, there are no comprehensive information on the nc-Si active layer. Indeed, it is unclear whether the amorphous incubation layer exists in the reported TFTs, and what is the relationship between the structure of conduction channel and device performance. Although it is often claimed that nc-Si TFTs are more stable than their α-Si:H counterpart, instability mechanisms are ill-understood and have not been analyzed.

A common issue in both top- and bottom-gate structures is the high drain-source leakage current, when TFT is off (I_{OFF}). This leakage current is important in macroelectronics applications, in which image or video information are stored in pixel circuits and should not be lost. For example, consider the pixel circuit of an OLED display shown in Fig. 1.2 (d). When the video voltage has been transferred to the C_S, the S-TFT is turned off until the next cycle that the video signal is rewritten. During that period, the voltage on C_S should be constant, ideally. However, S-TFT with a high I_{OFF} acts as a charge leakage path that leads to loss of signal and, thus, to a change in the output light intensity.

The required I_{OFF} depends on the application. Calculations show that it should be less than $10\,pA$ in OLED displays [14, 36]. In x-ray imagers, it should be as low as possible and comparable to that of α-Si:H TFTs ($\leq 0.1pA$) [37]. Values in the range $50\,pA - 10\,nA$ have been reported for nc-Si TFTs [25, 32, 38]. There have been attempts to reduce the I_{OFF} and to explain its origin. Thus far, the focus has been on the bulk properties of the nc-Si layer, for example its conductivity and density of states [25, 32, 38]. However, further research is required to better understand the I_{OFF} and its mechanisms in nc-Si devices.

1.5 Objectives of the Research

The focus of this research has been on the bottom-gate structure and its outstanding challenges. Earlier, we mentioned that the nc-Si TFT community is looking for two goals: devices with (i) high mobility and (ii) high stability. Thus far, high mobility has only been achieved in top-gate TFTs. Mobilities in the range of tens of $cm^2/V.s$ are easily obtainable [18, 25, 28, 29]. For bottom-gate TFTs, mobilities are more or less the same as that of α-Si:H devices, and in the range $0.1-3\, cm^2/V.s$ [26, 27, 32, 35, 39]. This difference in mobility, between top- and bottom-gate devices, is due to the structure of nc-Si shown in Fig. 1.8. Therefore, research efforts have been focused on either of these two configurations, depending on goals and requirements of targeted applications.

Currently, instability of bottom-gate α-Si:H TFT, as the industrial TFT, is the primary issue hindering implementation of active matrix arrays for OLED displays [14]. Although high mobility TFTs give flexibility in designing pixel circuits, calculations show that mobility is not a critical factor and values of $\approx 1\, cm^2/V.s$ are adequate [14, 36]. For this reason, we have chosen the bottom-gate structure and our main goal is to develop bottom-gate nc-Si TFT and investigate its instability mechanisms.

We characterize the two most important TFT components, i.e. nc-Si active layer and α-SiNx:H gate dielectric. Their quality, particularly at their interface, determines the device stability. We investigate how PECVD parameters affect the crystallinity of nc-Si films, and whether the amorphous incubation layer can be eliminated.

We are also going to identify the causes responsible for high off-current. Here, we will use a simulation tool, Medici [72], along with experimental data to investigate origins of I_{OFF}, in order to minimize it as far as possible.

1.6 Thesis Organization

In chapter two, we review the basics of TFTs, including their fabrication, operation, and physics. For example, we study how the device operation is influenced by the presence of trap states in the energy gap. We also review sources of instability in TFTs, and introduce widely-accepted models to describe them.

In chapter three, we show the results of our studies on the nc-Si material, and how its crystallinity is affected by PECVD conditions. The focus is on developing a film which is suitable for bottom-gate devices, i.e. crystalline grains grow immediately upon deposition without an amorphous incubation layer. We also characterize several nitride layers to be used as the gate dielectric, in order to study device stability as a function of gate dielectric quality.

In chapter four, we discuss the performance parameters of bottom-gate nc-Si TFTs fabricated in the course of this research. Particularly, our focus will be on the off-current. Its sources will be analyzed by using the Medici numerical simulator, supported by experimental results. Throughout this chapter, we will discuss design considerations and trade-offs in order to obtain a minimum off-current, while not compromising other performance parameters.

Chapter five addresses the stability of nc-Si TFTs. We will evaluate the threshold voltage stability of our devices under different operating conditions. We will also compare their stability with that of α-Si:H counterpart, and will use the attributes of instability mechanisms to justify the experimental data.

Finally, chapter six summarizes results and contributions of this research, and provides suggestions for further studies on nc-Si TFTs and their applications.

Chapter 2

Thin Film Transistors

2.1   Introduction

In this chapter, we discuss the basic concepts of thin film transistors, including their fabrication, operation, and physics, and also mechanisms that contribute to the reliability and stability of TFTs. In the beginning, two widely-used bottom-gate structures are introduced along with their fabrication sequence. We then discuss the electrical operation of TFTs and the current-voltage (I-V) relationships that are used to describe their operation in different regimes, such as linear and saturation as well as when the device is off. We also discuss various mechanisms that are regularly used to explain the device current in the off-state, i.e. drain leakage current or off-current.

Subsequently, the electrical instability of TFTs is reviewed. The instability is related to a shift in the threshold voltage under electrical operation, and is commonly attributed to two mechanisms: defect creation in the channel layer and charge trapping in the gate dielectric. We qualitatively explain how they appear under an applied gate bias along with the widely-accepted models to describe their kinetics. We also address properties and attributes of these instability mechanisms, to be able to distinguish them and to justify our experimental data, later.

2.2 Fabrication of Thin Film Transistors

Figure 2.1 shows cross sections of two processes used in the fabrication of α-Si:H and nc-Si TFTs. These structures in which gate metal is below the active layer and source/drain contacts are on the top are known as *bottom-gate inverted-staggered* [40]. The fabrication sequence for the structure in Fig. 2.1 (a) is illustrated in Fig. 2.2. First, a metal layer is deposited, by sputtering, on a substrate and patterned to define the gate area (steps 1 and 2). Then, a trilayer comprising of hydrogenated amorphous silicon nitride (α-SiNx:H) as the gate dielectric, α-Si:H or nc-Si as the active layer, and another α-SiNx:H as the passivation dielectric are deposited in one PECVD cycle (step 3). The passivation nitride is then patterned to expose selected regions of the active layer (step 4). Subsequently, n^+ doped and metal layers are deposited and patterned to make source-drain contacts (steps 5 and 6) [10, 40]. This structure is commonly known as *trilayer* or *etch stop*, due to the fact that the passivation nitride protects the active layer, on top of gate area, from being exposed to etchants and, thus, being damaged during etching processes. In this research, the trilayer structure was used in the fabrication of TFTs, as its fabrication sequence has already been developed in our group.

Alternatively, in Fig. 2.1 (b), the α-SiNx:H gate dielectric and two α-Si:H layers (undoped active layer and n^+ doped source/drain contacts) are deposited in one PECVD cycle. Subsequently, source/drain metal contacts are deposited and patterned. These contacts are then used as a mask for etching unwanted areas of the n^+ doped layer to separate source and drain terminals. In the end, another α-SiNx:H is deposited and patterned to protect the top surface of the active layer exposed during the previous etching step [10, 40]. This structure, in which the back side of channel (active) layer, on top of gate area, is etched to separate source-drain regions, is known as *back channel etched*.
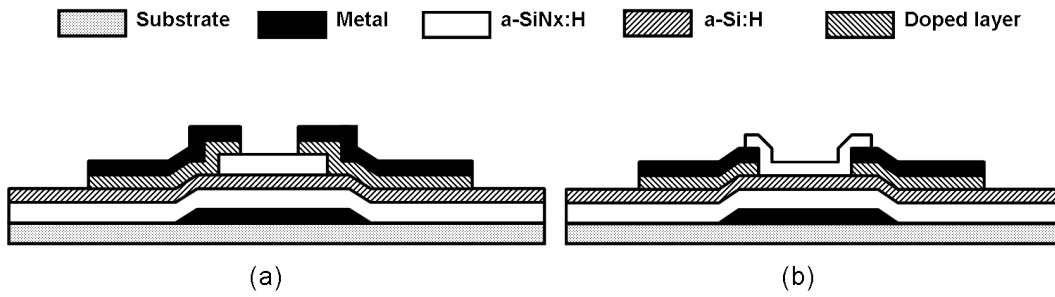
Figure 2.1: Bottom-gate inverted-staggered TFT structures, (a) trilayer and (b) back channel etched. Adapted from [10, 40].
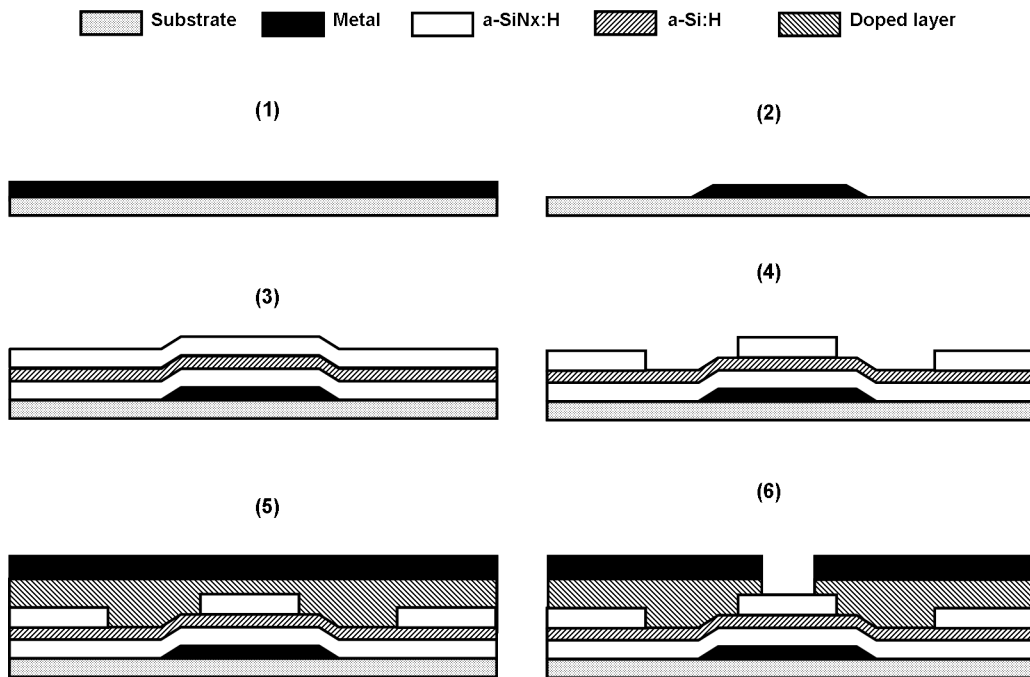
Figure 2.2: Fabrication sequence of the structure shown in Fig. 2.1 (a).
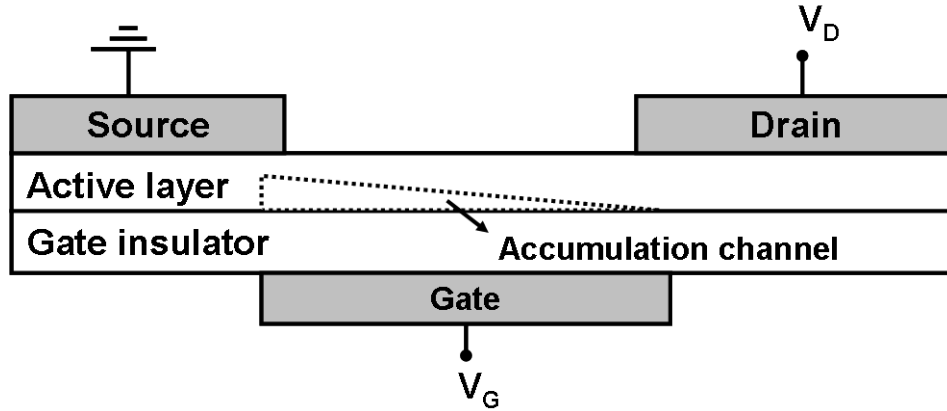
Figure 2.3: Illustration of operation of a bottom-gate TFT when gate and drain biases are applied. Adapted from [13].

2.3 Operation and Physics of Thin Film Transistors

In principle, TFTs are very similar to MOSFETs in terms of electrical operation and the same current-voltage (I-V) relationships can be used in describing their operation. The major difference is that we should consider defect and band tail states in the energy gap of the active layer in TFTs. Here, we review their operation, and methods that are commonly used to characterize them and to evaluate their performance characteristics such as threshold voltage, field effect mobility, and etc.

Figure 2.3 shows a cross section of a bottom-gate TFT when gate and drain biases are applied. If we assume that it is an n-type device, applying a positive gate voltage induces electrons near the semiconductor/gate dielectric interface to form the conduction (accumulation) channel shown in Fig. 2.3 [13]. Therefore, a positive gate voltage increases the conductivity between source and drain, and thus the drain current under a positive drain voltage. The magnitude of drain current in TFTs is considerably smaller than that in MOSFETs, due to the fact that mobility of electrons is much smaller in TFTs than that in MOSFETs.

In TFTs, the electron mobility is degraded by the large concentration of band

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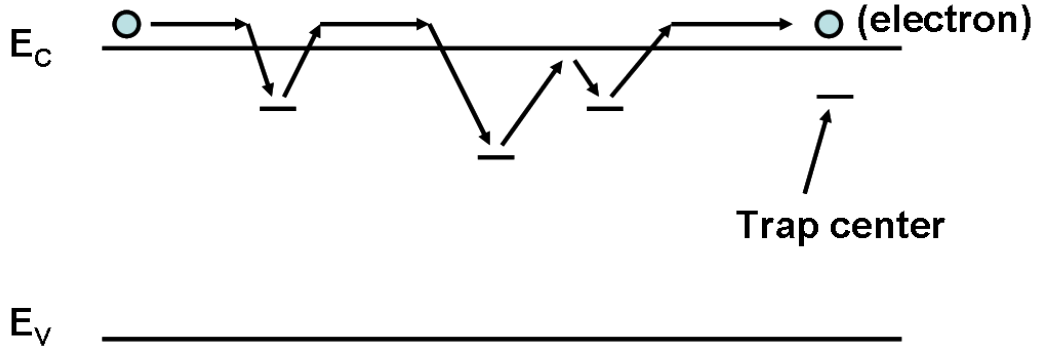
Figure 2.4: A one-dimensional model showing the motion of electrons that are frequently trapped in and released from band tail states. Adapted from Ref. [11].

tail states acting as temporary traps for conduction electrons. A profile of density of states in the energy gap of α-Si:H was shown in Fig. 1.5, and a simple one-dimensional model is shown in Fig. 2.4 [11]. Here, an electron may experience frequent trapping/release events into/from various energy levels within the band gap, during its journey in the channel region. In this case, the effective field-effect mobility (μ_{FE}) can be expressed as

$$\mu_{FE} = \mu_0 \frac{\tau_{free}}{\tau_{free} + \tau_{trapped}}, \tag{2.1}$$

where μ_0 is the band mobility of electrons without trapping, and τ_{free} and $\tau_{trapped}$ are the time intervals that electrons are free and trapped, respectively [11]. Indeed, electrons are trapped much of the time in band tail states and they are usually called band tail electrons.

Figure 2.5 shows a typical transfer characteristic of a bottom-gate nc-Si or α-Si:H TFT. One may distinguish three regions of operation. For small gate voltages around zero, the Fermi level lies in the deep defect states (see Fig. 1.5) and we may assume that energy bands are close to flat-band condition. By increasing the positive gate voltage, band bending close to the gate dielectric interface occurs, or in other words, the Fermi-level moves up through the deep defect states and towards the band tail states [40, 41]. In this case, most of the induced electrons are not free and are trapped in deep defect states; a negligible fraction of them
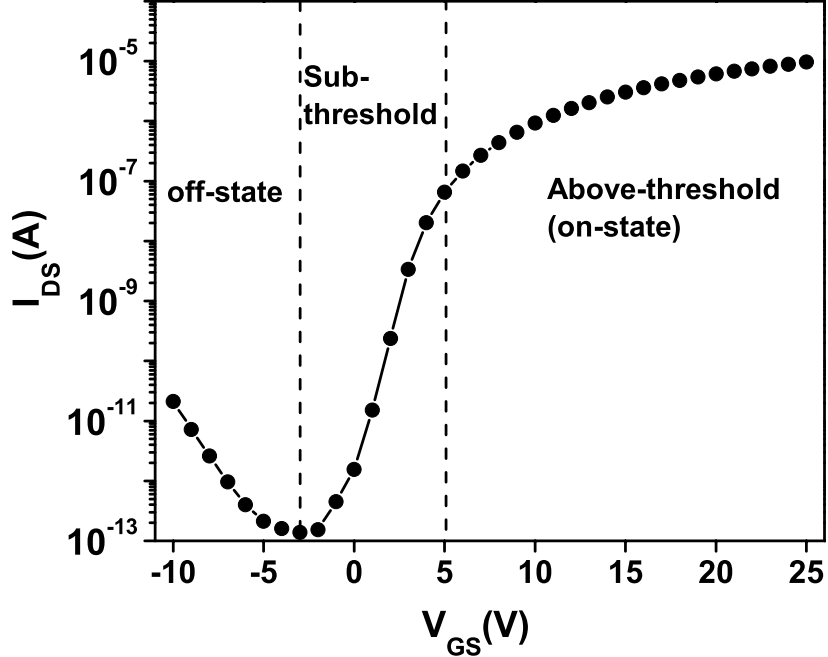
Figure 2.5: Typical I-V curve of a bottom-gate nc-Si or α-Si:H TFT.

may occupy band tail states and thus contribute to drain current. This case is the subthreshold region shown in Fig. 2.5. This situation continues until we fill up all deep defect states with electrons, and the concentration of electrons in band tail states exceeds that of trapped electrons in deep states. It happens when the applied gate voltage exceeds a threshold voltage (V_T) and the Fermi-level now lies in band tail states [40, 41].

This argument implies that V_T is a function of density of deep defect states (N_T). The following relationship has been derived in [10]:

$$V_T = qN_Tt_S(E_F - E_i)/C_{gate}, \tag{2.2}$$

where $E_F - E_i$ is the energy difference between the Fermi level and the intrinsic level at threshold. The t_S and C_{gate} are the thickness of the channel layer and the gate capacitance per unit area, respectively. It should be noted that (2.2) has been derived for a simplified case: it has been assumed that N_T is uniformly distributed in the energy gap [10].

For gate-source voltages (V_{GS}) higher than V_T, TFTs operate in the above-

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threshold regime, i.e. on-state. To simplify their characterization, the same MOS-FET equations can be applied. In the on-state and depending on the drain-source voltage (V_{DS}), linear and saturation regimes can be defined. In the linear regime when $V_{DS} \leq V_{GS} - V_T$, drain-source current (I_{DS}) is nearly linearly proportional to V_{DS}, and can be written as [13]:

$$I_{DS} = \mu_{FE} C_{gate} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right], \qquad (2.3)$$

where W and L are the TFT width and length, respectively.

When $V_{DS} = V_{GS} - V_T$, the accumulation channel is pinched off near the drain terminal as shown in Fig. 2.3, and drain current saturates and becomes independent of V_{DS}, ideally. For $V_{DS} \geq V_{GS} - V_T$, TFTs operate in saturation regime and I_{DS} is given by

$$I_{DS} = \mu_{FE} C_{gate} \frac{W}{2L} (V_{GS} - V_T)^2. \qquad (2.4)$$

Therefore, values of μ_{FE} and V_T can be extracted from experimental I-V curves by using (2.4). One can plot the square root of I_{DS} as a function of V_{GS} and approximate it with a line, where the line slope is proportional to μ_{FE} and x-intercept is the V_T [13].

The third operation region shown in Fig. 2.5 is the off-state when negative gate voltages are applied. In this case, I_{DS} is called off-current as well as drain leakage current. The mechanisms of current conduction in the off-state have not yet fully established, although several mechanisms have been proposed to justify the experimental results. In the following, those mechanisms are briefly reviewed.

2.3.1   Mechanisms of Drain Leakage Current

The first mechanism is the ohmic conductivity of the active layer [12, 41]. When negative gate voltages are applied, the Fermi level moves downward in defect states and towards the midgap [12]. In other words, band tail electrons are depleted by a negative gate voltage and the effective conductivity of the active layer decreases.

This reduction in conductivity results in a lower drain leakage current. Thus, by applying a larger negative gate voltage, the off-current should decrease.

However, this is not always the case and off-current may increase by increasing the negative gate voltage, as shown in Fig. 2.5. In this case, the off-state conduction is usually attributed to various field-assisted and trap-assisted mechanisms that may occur in the so-called drain depletion region, located in between drain and gate overlap area. For example, the electric field increases the rate of emission of electrons that are trapped in deep defect states into the conduction band by the so-called Poole-Frenkel effect. This emission and release of trapped electrons lead to enhanced conductivity of the active layer and thus to higher drain leakage current [37]. It should be noted that the electric field is directly related to gate and drain voltages. The Poole-Frenkel conduction can be expressed as

$$I_{PF} = I_{PF0}\,exp\left(\sqrt{E/E_0}\right), \qquad (2.5)$$

where E is the electric field and E_0 is a coefficient [37]. Therefore, the Poole-Frenkel current increases exponentially with the electric field in the drain depletion region [37].

Figure 2.6 shows the band diagrams of two models, labeled as model 1 and model 2, illustrating several mechanisms of leakage current. These two models are essentially the same, their only difference is that model 1 and model 2 are referring to the band diagram in the drain depletion region along a cross section parallel and vertical to the conduction channel, respectively [42]. Thus, their difference is related to the physical location that the leakage current originates from, however, the explanation is the same for two models.

To cover a wide range of applied electric fields, three cases have been considered in Ref. [42]. When the applied electric field is low as in Fig. 2.6 (a), the leakage current is governed by thermal activation of electrons from valence band to conduction band. When the applied electric field is medium, the electron emission may comprise of two steps: first electrons are thermally excited from valence band into a trap state in the band gap, and second they tunnel into the conduction band as
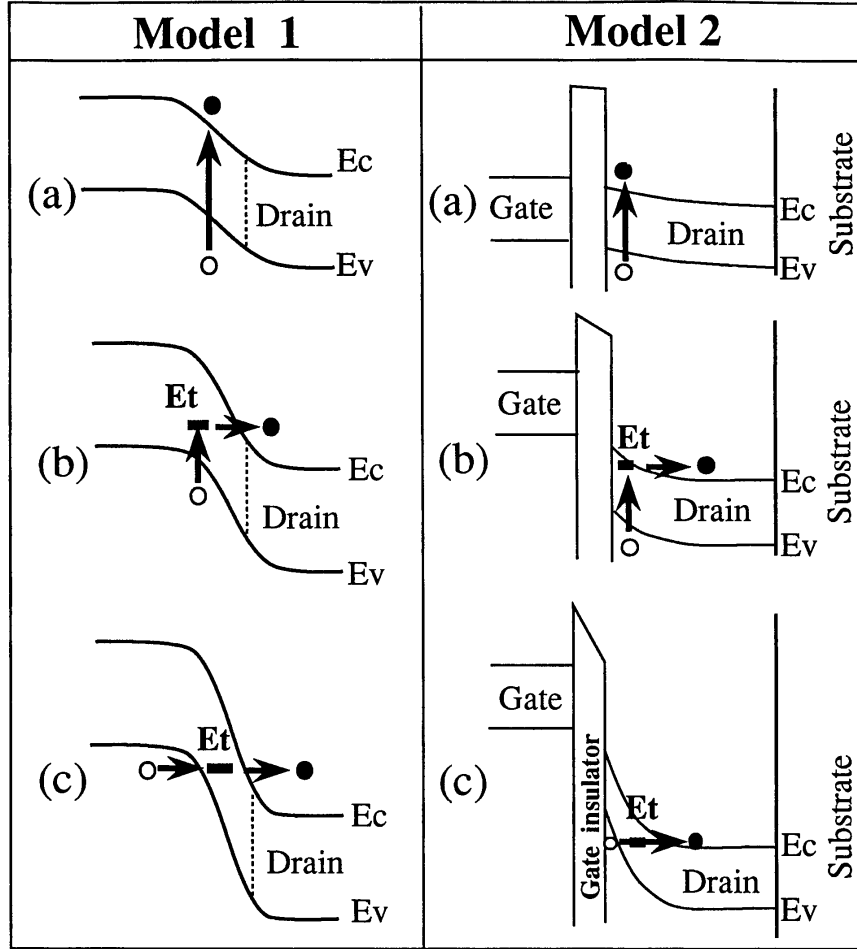
Figure 2.6: The band diagrams for two models illustrating several mechanisms of leakage current, (a) the case of weak electric field, (b) the case of medium electric field, and (c) the case of strong electric field. From Ref. [42].

shown in Fig. 2.6 (b). Here, E_t is the trap energy. Finally, when the applied electric field is strong, the leakage current is governed by field-enhanced emission and tunneling. In this situation, a large electric field decreases the effective tunneling length and the presence of trap states in the band gap assists the tunneling process [42]. Thus, electrons tunnel from valence to conduction band and contribute to a high off-current. The third mechanism shown in Fig. 2.6 (c) is also known as band-to-band tunneling, and has been used to justify the experimental results of nc-Si and α-Si:H TFTs [43].

2.4 Electrical Instability of Thin Film Transistors

In contrast to c-Si CMOS transistors, α-Si:H TFTs are not stable under electrical operation. When we turn on a CMOS transistor, I_{DS} is constant for a given biasing condition. However, in α-Si:H TFTs, it is observed that I_{DS} gradually decreases over time. This instability is commonly attributed to two mechanisms: (1) defect state creation in the α-Si:H active layer and (2) charge trapping in the gate dielectric. These mechanisms cause a shift in the threshold voltage (ΔV_T), and thus I_{DS} changes according to (2.4), assuming that TFT operates in the saturation regime. In the following, we discuss these instability mechanisms and their attributes. Later, we use those attributes to distinguish the instability mechanisms.

2.4.1 Metastability of Amorphous Silicon

Hydrogenated amorphous silicon (α-Si:H) is deposited by PECVD at temperatures of less than $300\,^\circ$C. Due to the low temperature fabrication, it contains large concentration of weak Si-Si bonds as well as dangling bonds. These two kind of bonds are considered as sources of band tail states and deep defect states, respectively. Hydrogen is also available in the material in various forms. It may form Si-H bonds and passivate Si dangling bonds. This reduces the density of defect states. Hydrogen also exists in the form of interstitial atoms and can diffuse within the material and change the electrical properties of α-Si:H, which is often used to explain the experimental results [11].

When an α-Si:H TFT is turned on, the concentration of conduction electrons increases in the α-Si:H channel layer. Conduction carriers are also called band tail carriers as they spend much time in band tail states during frequent trapping and release events that was illustrated in Fig. 2.4. It is hypothesized that band tail carriers interact with weak Si-Si bonds which leads to an energy transfer from carriers to weak bonds. Due to this interaction, weak Si-Si bonds break and new dangling bonds are formed. Consequently, band tail carriers are trapped in the

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newly-created defect states and effectively I_{DS} decreases or V_T increases, as a higher gate voltage is required to maintain the band tail carrier density and drain current unchanged [11, 44, 45].

Kinetics of carrier-induced defect state creation has been studied, and it has been found that hydrogen plays an important role in the metastability of α-Si:H. In the most widely accepted model for the carrier-induced defect creation, a hydrogen atom diffuses to the weak Si-Si bond and participates in the process, where upon the breakage of the weak bond, two dangling bonds are created which one of them is passivated by the hydrogen [44, 45]. Hydrogen diffusion has been found to follow a stretched-exponential time dependence and to be dispersive, similar to the carrier transport in α-Si:H shown in Fig. 2.4. This dispersive motion of hydrogen leads to the stretched-exponential time dependence of carrier-induced creation of defects and, consequently, the shift in threshold voltage [44]. Thus, assuming that defect state creation is the dominant mechanism of the shift in threshold voltage, a relationship has been developed in the form of

$$\Delta V_T = C \left[1 - exp \left[-(\frac{t}{\tau})^\beta \right] \right] \tag{2.6}$$

where $C \approx V_{GS} - V_{T0}$, V_{GS} is the applied gate-source voltage, also called gate bias stress, V_{T0} is the threshold voltage at time $t = 0$, and τ and β are a time constant and fitting exponent, respectively. The parameter β has been found to be around 0.5 at room temperature [44, 45].

It is well known that hydrogen diffusion in α-Si:H is temperature-activated, which renders a highly temperature dependent ΔV_T. When the device operating temperature increases, the rate of hydrogen diffusion increases, which results in an increase in ΔV_T. The temperature dependence is reflected in the parameter τ as

$$\tau = \tau_0 \, exp \left[\frac{E_A}{k_B T} \right] \tag{2.7}$$

where τ_0 has been found to be around $10^{-10} \, sec$ and $E_A = 0.95 \, eV$ is the activation energy [44]. For short stress times, i.e. $t \leq \tau$, equation (2.6) can be approximated

by

$$\Delta V_T = (V_{GS} - V_{T0}) \left[\frac{t}{\tau}\right]^{\beta} , \qquad (2.8)$$

and has been used to model the experimental threshold voltage shifts [44, 45].

It is interesting that the shift in threshold voltage is reversible, meaning that generated defects can be annealed and re-passivated by atomic hydrogen present in the material. For example, it is common to put the electrically stressed TFTs in an oven and anneal them at temperatures around $150\,°C$ for several hours, to obtain more or less the initial I-V characteristics. Here, hydrogen motion and diffusion inside α-Si:H is again the key phenomenon during the defect annealing process [11]. Thus, the kinetics of defect removal can also be formulated by the stretched-exponential time dependence. Assume that we have subjected a TFT to a gate bias stress for some time and generated a defect density of N_{T0}. If we then remove the gate bias and the TFT is relaxed at an ambient temperature of T, the density of defects over time is given by

$$N_T(t) = N_{T0}\, exp \left[-(\frac{t}{\tau})^{\beta}\right] , \qquad (2.9)$$

with similar parameter values as given for (2.7) [11]. As mentioned, defect annealing is usually performed at high temperatures around $150\,°C$. At room temperature, it may take around a year and, for this reason, it is sometimes stated that defect states are permanently stable at room temperature [11].

2.4.2 Thermalization Energy Concept

The defect state creation and thus the shift in the threshold voltage are a function of time and temperature. A common practice to compare the stability of different TFTs has been to evaluate their ΔV_T over time at different temperatures. Thus, a smaller ΔV_T means a more stable TFT. However, recently, a new concept has been developed by Deane et al. [46], in order to describe the instability of TFTs with a deeper physical insight. They introduced a new variable, i.e. thermalization energy, by combining time and temperature variables. The thermalization energy,

defined as $E_{th} = k_B T \, Ln(\nu t)$, means that after time t, stressing at temperature T, all defect creation sites with energy less than E_{th} would have converted into defects [46].

According to this concept, ΔV_T is first measured as a function of time at different temperatures. They are then plotted as a function of thermalization energy. In general, when we plot the data, we obtain several curves associated with each temperature. For example, we get two curves if we perform ΔV_T measurements at two temperatures. However, this depends on the value of the parameter ν in the E_{th} definition. Deane et al. [46], and after them several other groups [47, 48], have found that when $\nu = 10^{10} \, Hz$, the two curves overlay perfectly, i.e. a single curve is obtained. In other words, ν is a fitting parameter to move various curves along the E_{th} coordinate to overlay them and obtain a single curve. It seems that ν is unique to defect state creation, and it has been attributed to the probability that an electron attempts to break weak Si-Si bonds [46, 49]. Therefore, the parameter ν was considered as a merit for device stability. In other words, if ν is smaller it means that electrons attempt to break weak Si-Si bonds less frequently and thus the rate of defect creation and ΔV_T are smaller.

Using the kinetics of defect creation, it was shown that ΔV_T and E_{th} have the following relationship [50]:

$$\Delta V_T = C \left[1 - \frac{1}{(1 + exp[(E_{th} - E_A)/k_B T_0])^{\frac{1}{\epsilon}}} \right]. \tag{2.10}$$

Further details and definition of parameters can be found in Ref. [50]. By fitting the experimental data of ΔV_T to (2.10), one can extract various parameters, including the energy barrier for defect state creation (E_A). It has been found to be ≈ 1 eV [47, 48, 50]. A sample curve along with experimental data are shown in Fig. 2.7 [49].

In general, both charge trapping and defect creation mechanisms exist simultaneously. However, experimental results have indicated that at gate biases of less than 25 V, the defect creation is the dominant mechanism with negligible charge
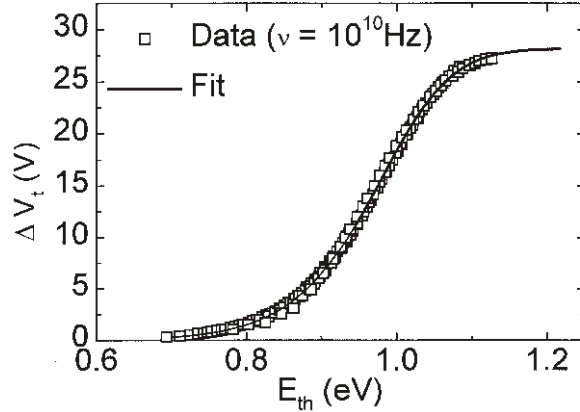
Figure 2.7: Threshold voltage shift of an α-Si:H TFT as a function of the thermalization energy. From Ref. [49].

trapping in a good quality nitride [45]. However, at higher gate biases, it was observed that charge trapping in the gate dielectric increases and it becomes the dominant mechanism at gate voltages greater than 50 V [45]. In the next section, we briefly review the kinetics of charge trapping.

2.4.3   Charge Trapping in Silicon Nitride Dielectric

Several mechanisms of electron injection and trapping have been proposed to explain ΔV_T and the hysteresis in I-V characteristics of TFTs [51]. Figure 2.8 shows the band diagram of a Metal-Insulator-Semiconductor (MIS) structure, with the nitride as the insulator and biased with a positive voltage. The gate/nitride/channel trilayer in TFTs is essentially an MIS capacitor. Once the electron accumulation channel forms near the α-SiNx:H interface, several electron injection and trapping mechanisms may occur. In Fig. 2.8, they are numbered from 1-6, and are direct tunneling from valence band, Fowler-Nordheim injection, trap-assisted injection, constant-energy tunneling from silicon conduction band, tunneling from conduction band into traps close to E_F, and hopping at the Fermi level, respectively [51]. Determining which one is dominant is not easy and, in general, they are dependent on the nitride trap density and the applied electric field. Mechanisms 1-3 are be-

lieved to occur at relatively large electric fields, while others may happen even at low fields [51].

In contrast to the defect state creation which is irreversible and stable at room temperature, charge trapping is reversible even at room temperature [52], and initial drain current can be recovered [53]. Indeed, charge release (detrapping) from the nitride dielectric, back into the TFT channel layer, is energetically favorable when the gate bias is removed. In Fig. 2.8, assume that we apply a gate bias to the TFT or MIS structure and, thus, some amount of charge is trapped in the nitride dielectric. The trapped charges occupy energy levels close to the nitride Fermi level which is below the Fermi level of channel layer. Once the gate bias is removed, the energy of trapped charges lies above the Fermi level in the channel layer. This energy difference favors detrapping and back-tunneling of charges into the channel layer.

Although it is widely accepted that the defect state creation is temperature-activated, there is no such an agreement on the charge trapping case. The experimental results by Powell et al. [45] indicated that charge trapping is weakly temperature-activated. However, the results obtained by Libsch and Kanicki [52] showed otherwise. These two groups justified their observations as follows. Based on arguments in [45], charge injection occurs from the α-Si:H channel layer to the silicon nitride with trapping near the interface, and no further redistribution of the trapped charges deeper in the nitride occurs. This leads to a temperature independent process [45]. They reasoned that their observations of charge trapping in α-Si:H TFTs exhibited the same time and temperature dependency as the one found for charge trapping in MIS structures. They also speculated that their justification could be only valid for moderate temperatures and high quality nitrides [45]. A logarithmic time dependence was proposed, which is seen in metal-nitride-oxide-semiconductor (MNOS) memories where charge trapping takes place, that is:

$$\Delta V_T \approx C \, Log(1 + \frac{t}{t_0}), \tag{2.11}$$
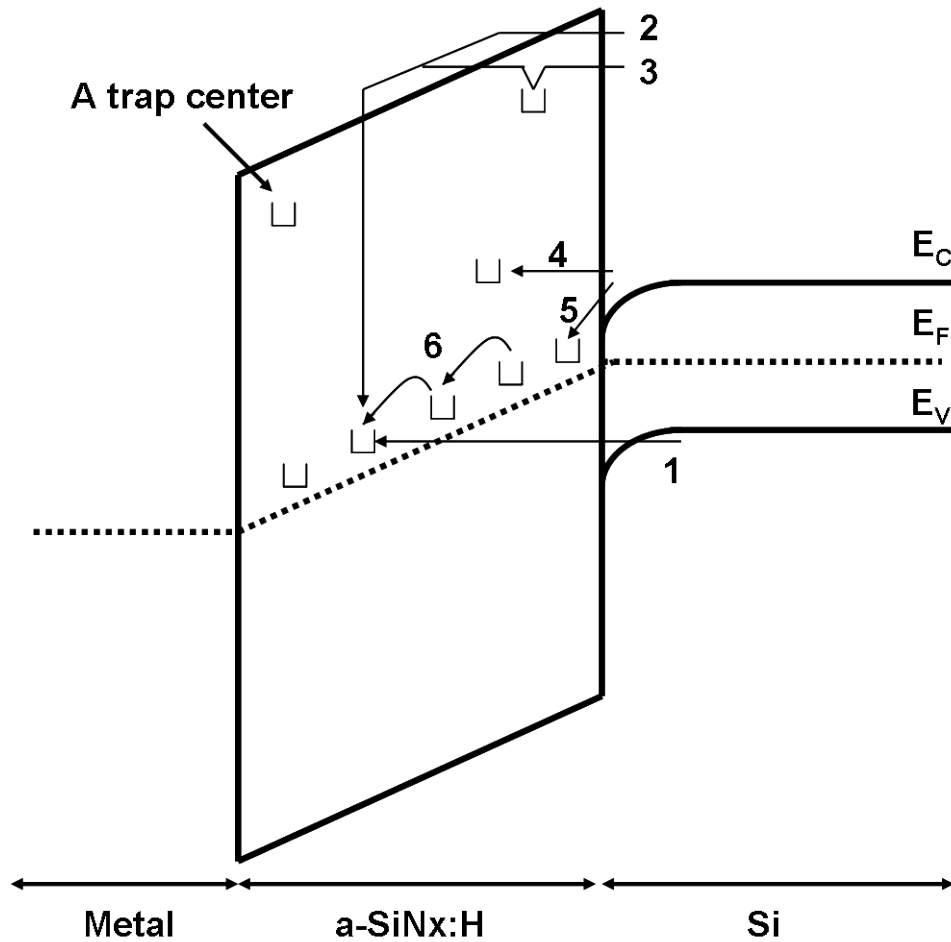
Figure 2.8: Charge trapping mechanisms: 1- direct tunneling from valence band, 2- Fowler-Nordheim injection, 3- trap-assisted injection, 4- constant-energy tunneling from silicon conduction band, 5- tunneling from conduction band into traps close to E_F, and 6- hopping at the Fermi level. Adapted from Ref. [51].

where C and t_0 are a constant and time constant, respectively.

On the other hand, Libsch and Kanicki [52] reasoned that for shorter stress times, smaller gate voltages, or lower temperatures, carriers are injected from the α-Si:H channel layer into energy states located at the α-Si:H/nitride interface and in a transitional layer close to the interface. At higher stress times, larger gate voltages, or higher stress temperatures, a larger fraction of the states near the interface are filled, which increases the probability of re-emission from these filled states, towards those deep in the nitride. They stated that the motion between traps is diffusive superimposed with a drift velocity by the electric field [52]. It was concluded that this kind of carrier transport could be characterized by a stretched exponential function and the same equation (2.6) was used for fitting the experimental data [52].

2.4.4 Constant Voltage and Constant Current Stressing

In general, it is possible to evaluate the V_T stability of TFTs under a constant gate voltage or a constant drain current, which are illustrated in Fig. 2.9. In the former, a constant voltage is applied to the gate and drain terminals with the source terminal grounded, as shown in Fig. 2.9 (a). From time to time, the stress voltages are switched off; the device is placed in the sweeping mode; its I-V characteristic is retrieved, and this cycle may be repeated. In the latter, a constant current is applied to the drain terminal, while drain and gate terminals are shorted in a diode-connected configuration with the source terminal grounded. This configuration is shown in Fig. 2.9 (b).

In previous sections, we have implicitly assumed that devices are stressed under a constant gate bias. In this mode, if we assume that the defect state creation is the instability mechanism, the drain current decreases over time due to the fact that defect density increases and, thus, band tail carriers are trapped in the newly-created defect states. On the other hand, defect creation itself is proportional to

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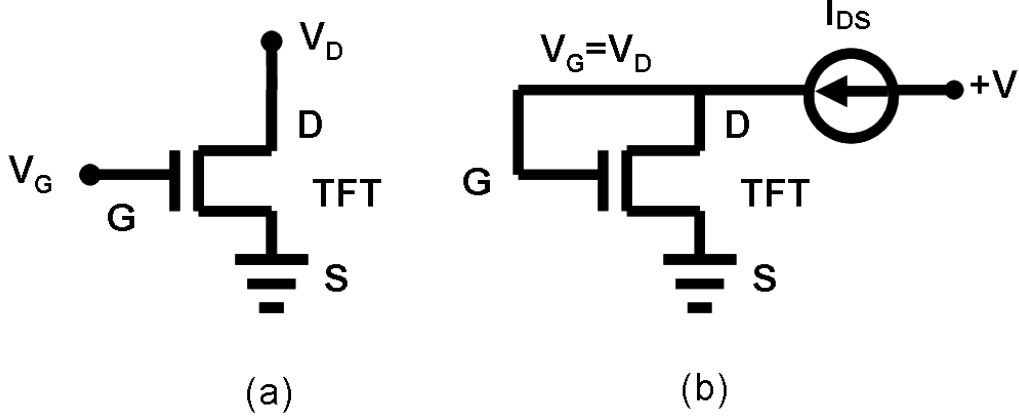
Figure 2.9: A simple representation of the experimental setup, (a) constant voltage stressing and (b) diode connected configuration for constant current stressing.

the concentration of band tail carriers. Thus, there is a kind of negative feedback and defect creation vanishes ultimately, when the concentration of band tail carriers becomes negligible. This is consistent with the stretched-exponential time dependence model, eqn. (2.6), that saturates at long times. According to (2.6), at $t = \infty$, $\Delta V_T = V_T(\infty) - V_{T0} = V_{GS} - V_{T0}$. As the V_{GS} is fixed, this implies that once the $V_T = V_{GS}$, defect creation stops, and according to I-V relationships, e.g. (2.4), drain current and band tail carriers approach zero.

In constant voltage stressing, it is possible to vary the drain voltage in order to change the concentration of band tail carriers and, thus, to change the rate of defect creation and ΔV_T. In the linear regime, i.e. when the drain voltage is small $V_{DS} < V_{GS} - V_T$, there is a uniform concentration of band tail carriers along the TFT channel length. Increasing the drain bias increases the lateral electric field and decreases the carrier concentration in the channel, near the drain terminal [54]. The concentration of carriers in the channel can be expressed as [54]

$$Q_{ch} = \frac{2}{3}C_{gate}WL\frac{(V_{GS} - V_T)^3 - (V_{GD} - V_T)^3}{(V_{GS} - V_T)^2 - (V_{GD} - V_T)^2},$$ (2.12)

where V_{GD} is the gate-drain voltage and other parameters are known. According to (2.12), the concentration of band tail carriers at saturation, $V_{DS} = V_{GS} - V_T$, is around 2/3 of that at deep linear regime, when $V_{DS} \to 0$ [54]. Thus, it is expected

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that the defect state creation and ΔV_T also follow the same relationship; for example ΔV_T in saturation is nearly 2/3 of that in the linear regime [54].

Alternatively, devices can be stressed under a constant drain current, as shown in Fig 2.9 (b). Here, the situation is slightly different. In contrast to the constant voltage stressing, the density of band tail carriers (n_{BT}) remains unchanged as the drain current is kept constant [55]. Assuming a uniform density of carriers in the channel, we can write [55]

$$q\, n_{BT}(t) = C_{gate}(V_{GS}(t) - V_T(t)). \tag{2.13}$$

To keep the drain current constant, the term $V_{GS}(t) - V_T(t)$ should be kept constant according to the eqn. (2.4). Thus, from (2.13) and (2.4), we deduce that n_{BT} remains unchanged during the constant current stressing. Consequently, the rate of defect state creation, which depends on n_{BT}, does not vanish over time. In this case, the threshold voltage can increase indefinitely until the applied gate voltage hits the supply voltage or the density of weak Si-Si bonds (N_{WB}) becomes a rate limiting factor [55]. It should be noted that the gate voltage is automatically adjusted by the semiconductor characterization system. The kinetics of ΔV_T have been given as [55]

$$\Delta V_T \;=\; C \left[\frac{t}{t_0}\right]^{\beta}, \tag{2.14}$$

where C, t_0, and β are a constant, time constant, and fitting exponent, respectively. Their definition and further details can be found in [55]. Thus, we notice that, in this case, the kinetics of ΔV_T is different from that given in (2.6) for the constant voltage case, in which ΔV_T does not and does saturate at longer stress times, respectively.

2.5   Summary

In this chapter, we discussed the fabrication of two widely-used bottom-gate TFT structures, namely, *trilayer inverted-staggered* and *back channel etched*. The devices

investigated in this research have been fabricated based on the trilayer inverted-staggered configuration, where details of its fabrication were shown in Fig. 2.2. We then discussed the electrical operation of TFTs and the current-voltage relationships that are used to describe their operation in different regimes, such as linear and saturation. It was mentioned that TFTs are very similar to MOSFETs in terms of electrical operation and the same I-V relationships can be used in describing their operation. However, the major difference is that we should consider defect states and band tail states in the energy gap of the active layer in TFTs. In other words, in TFTs, the electron mobility is degraded by the large concentration of band tail states acting as temporary traps for conduction electrons. We discussed a simple one-dimensional model illustrating the trapping/detrapping of electrons in band tail states.

We then reviewed several mechanisms of drain leakage current when TFT is in off-state. The first mechanism was the ohmic conductivity of the active layer. When negative gate voltages are applied, the Fermi level moves downward in defect states and towards the midgap. In other words, the band tail electrons are depleted by a negative gate voltage and the effective conductivity of the active layer decreases. This reduction in conductivity results in a lower drain leakage current. In addition, off-current is also affected by various field-assisted and trap-assisted conduction mechanisms that occur in the drain depletion region, illustrated in Fig. 2.6. The Poole-Frenkel effect is one of them, where emission of electrons from trap states increases the off-current exponentially as a function of electric field in the drain-gate overlap region.

We also reviewed the instability mechanisms of α-Si:H TFTs which are defect state creation in the active layer and charge trapping in the gate dielectric. Generally, these two mechanisms are also available in nc-Si TFTs, albeit with different degrees, depending on the quality of nc-Si active layer and nitride gate dielectric. It was mentioned that α-Si:H contains large concentration of weak Si-Si bonds as well as dangling bonds. When an α-Si:H TFT is turned on, band tail carriers interact

with weak Si-Si bonds which leads to an energy transfer from carriers to weak bonds. Due to this interaction, weak Si-Si bonds break and new dangling bonds are formed. Consequently, band tail carriers are trapped in the newly-created defect states and effectively I_{DS} decreases or V_T increases. Indeed, hydrogen diffusion plays a key role in the metastability of α-Si:H, which leads to the stretched-exponential time dependence of carrier-induced creation of defects and, consequently, the shift in threshold voltage [44]. Since hydrogen diffusion in α-Si:H is temperature-activated, so is the shift in threshold voltage, and its activation energy has been found to be around 1 eV [44].

The shift in threshold voltage due to defect creation is reversible, meaning that generated defects can be annealed at temperatures around $150\,^{\circ}$C for several hours, to obtain more or less the initial I-V characteristics. However, annealing at room temperature is very slow and it may take around a year to obtain the initial I-V curves. For this reason, it is stated that defect states are permanently stable at room temperature [11].

The second instability mechanism is the charge trapping in the nitride. Once a TFT is on and the electron accumulation channel forms near the α-SiNx:H interface, several electron injection and trapping mechanisms may happen, as shown in Fig. 2.8. Charge trapping is highly dependent on the quality of nitride and the concentration of trapping centers in nitride and its interface with the active layer. In contrast to the defect state creation which is irreversible and stable at room temperature, charge trapping is reversible even at room temperature [52], and initial drain current can be recovered [53].

Later, when we present our experimental observations, we use these attributes of instability mechanisms to justify our results.

Chapter 3

Materials Optimization for Nanocrystalline Silicon Thin Film Transistors

3.1 Introduction

In this chapter, we discuss processing and characterization of the core materials in TFTs, i.e. nanocrystalline silicon (nc-Si) as the active layer and hydrogenated amorphous silicon nitride (α-SiNx:H) as the gate dielectric, both deposited by plasma enhanced chemical vapor deposition (PECVD). In the first section, we present our studies on obtaining a nc-Si layer which is suitable for high performance bottom-gate TFTs. Particularly, we investigate how PECVD process variables affect the crystallinity of nc-Si films. We use a statistical method based on the Taguchi Orthogonal Arrays for the design of the experiments [56]. Based on the results of this study, we adjust values of PECVD parameters that give us the thinnest possible nc-Si layers with high crystallinity, which is required for bottom-gate TFTs. We used Raman Spectroscopy to calculate the crystalline volume fraction of nc-Si films, and Transmission Electron Microscopy (TEM) to observe crystalline grains near the gate dielectric interface.

In the second part, we present the results of our study on the characterization of several α-SiNx:H layers. We varied PECVD conditions to change the electrical characteristics of the nitride dielectric. Our ultimate goal is to relate performance parameters of TFTs to the quality of their gate dielectric, and to find the best nitride for bottom-gate nc-Si TFTs that yields the highest mobility and stability. To compare the quality of nitrides, we performed characterization techniques and measurements such as current-voltage (I-V), capacitance-voltage (C-V), Fourier-transform infrared (FTIR) spectroscopy, and elastic recoil detection analysis (ERDA).

3.2   Nanocrystalline Silicon Active Layer

In section 1.4.2, we mentioned that in order to reduce the threshold voltage shift in nc-Si TFTs, the conduction channel should be formed within a highly crystalline region. Figures 3.1 (a) and (b) show a simplified bottom-gate TFT structure when nc-Si layer does not and does comprise of crystalline grains near the gate dielectric interface, respectively. The arrow represents the conduction channel when TFT is on, and source/drain contacts are not shown for simplicity. The goal of our research is to develop a deposition process for a nc-Si film with a structure similar to that in part (b). In contrast, in part (a), the conduction channel is formed in a low-quality amorphous region that results in device instability, due to the mechanism of defect state creation in the amorphous silicon. Achieving this is dependent on PECVD conditions and, therefore, we should find how PECVD parameters influence the crystallinity of nc-Si layers.

There are several process parameters that can be changed to manipulate the properties of silicon thin films. They are plasma power, chamber pressure, and hydrogen and silane gas flow rates. The deposition (substrate) temperature can also be a variable, but it was fixed at $250\,°\mathrm{C}$ in this research. To find a suitable process window for a highly crystalline film, we chose the Taguchi statistical method to optimize the PECVD process. The Taguchi method [56] is based on orthogonal
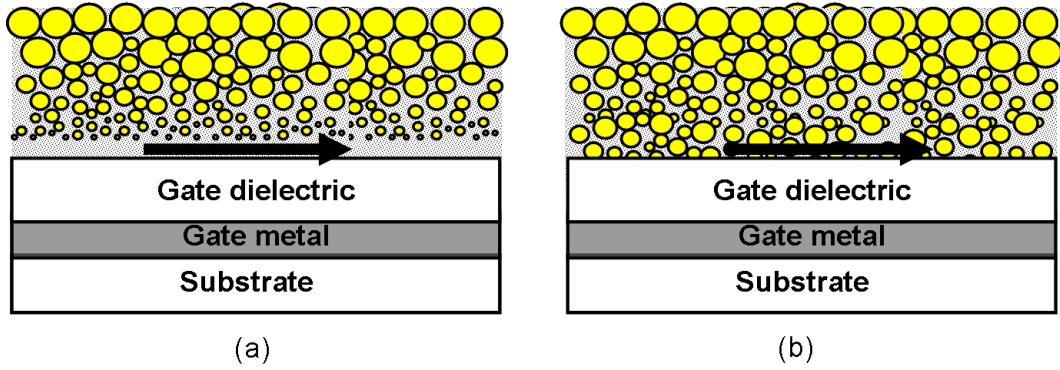
Figure 3.1: The nc-Si active layer in a simplified bottom-gate TFT structure, (a) with and (b) without amorphous incubation layer at the gate dielectric interface. For simplicity, the source/drain contacts are not shown. The arrow represents the conduction path.

arrays (OA) for design of experiments, which allowed us to investigate the effect of process variables with minimum number of experiments, and to estimate the contribution of PECVD parameters to the film crystallinity. It has been applied to process optimization before, with satisfactory results [57, 58].

Table 3.1 shows the set of nine experiments that we performed, in which each of four parameters (plasma power, chamber pressure, and H_2 and SiH_4 flow rates) took three values. For example, the plasma power took values of 30, 65, and 100 W. The choice of parameter values was based on technical specifications of our PECVD tool and our prior experience in α-Si:H deposition, however, their combination was based on the Taguchi orthogonal arrays given in [56].

The layers were deposited on Corning 1737 glass wafers at $250\,^{\circ}$C in a single-chamber 13.56 MHz PECVD system (PlasmaTherm 790 series with an electrode area of 14"$\times$14"). We then characterized the obtained films. The film thickness was measured by patterning them and using a DekTak 8 Stylus Profilometer. The deposition rates (DR) were obtained by dividing the thicknesses by the respective deposition time. Their conductivity (σ) was measured by making test resistors using aluminum co-planar contacts [24]. Their crystallinity (X_C) was evaluated by Raman spectroscopy using a He-Ne laser with a wavelength of $632.8\,nm$. The

Table 3.1: The PECVD parameters for nine experiments, based on the Taguchi orthogonal array [56].

Exp. #	Power (W)	Pressure (mTorr)	H_2 flow (sccm)	SiH_4 flow (sccm)
1	30	300	200	4
2	30	600	300	6
3	30	900	400	8
4	65	300	300	8
5	65	600	400	4
6	65	900	200	6
7	100	300	400	6
8	100	600	200	8
9	100	900	300	4

results are given in Table 3.2.

Raman spectra, shown in Fig. 3.2, showed that four layers out of nine were nanocrystalline. They were obtained from experiment numbers 1, 5, 7, and 9, listed in Table 3.1. Others were amorphous-like with the X_C of zero, meaning that their PECVD conditions are not suitable for achieving high crystallinity. In Fig. 3.2, the peak at $517 - 520 \, cm^{-1}$ is due to crystalline grains. On the other hand, the peak at $480 \, cm^{-1}$ is attributed to the amorphous phase and, for example, the film #6 is amorphous which gave a peak at $480 \, cm^{-1}$ and not at $520 \, cm^{-1}$. To estimate the X_C, we decomposed the Raman signal into two Gaussian peaks centered around $517 - 520 \, cm^{-1}$ (due to the crystalline phase) and $480 \, cm^{-1}$ (due to the amorphous phase), as described in Ref. [59]. An example is illustrated in Fig. 3.3.

The crystallinity was evaluated using

$$X_C = \frac{I_{520}}{I_{520} + 0.8 \times I_{480}} \tag{3.1}$$

where I_{520} and I_{480} are the intensities of the decomposed Raman spectrum at $520 \, cm^{-1}$ and $480 \, cm^{-1}$, respectively [59]. The calculated values of X_C are shown in Table 3.2.

Table 3.2: The results of measurements and characterizations performed on the thin films where their PECVD parameters are given in Table 3.1. Values of deposition rate (DR), film thickness, crystallinity (X_C), and conductivity (σ) are given.

Exp. #	$DR\,(nm/min)$	$Thickness\,(nm)$	$X_C(\%)$	$\sigma\,(S/cm)$
1	0.75	60	40	1.25×10^{-9}
2	1.5	60	0	8.7×10^{-10}
3	2	80	0	1.4×10^{-9}
4	2.25	90	0	6.5×10^{-10}
5	1.15	98	73	4×10^{-6}
6	5	100	0	1.1×10^{-9}
7	2.5	125	62	10^{-6}
8	7.5	150	0	6.8×10^{-10}
9	3.4	170	71	2×10^{-6}

From Table 3.2, it is seen that the conductivity of amorphous layers is in the range $(0.6 - 1) \times 10^{-9} S/cm$, which are typical values for hydrogenated amorphous silicon (α-Si:H) [60]. On the other hand, the conductivity of highly-crystalline layers, obtained from experiments #5, 7, and 9, is several orders of magnitude higher than that of amorphous ones, and is in the range $1 - 5\,\mu S/cm$. These values of conductivity are similar to those reported by others [18, 61]. It is believed that when the material structure changes from amorphous to crystalline, unintentional impurities such as oxygen, which are available in the gas phase during the PECVD processes, are incorporated in the crystalline silicon network and act as electron donors [62]. This unwanted doping increases the conductivity of nc-Si layers, sometimes, to values as high as $10^{-3}\,S/cm$ [62].

Another important attribute of nc-Si layers is their conductivity activation energy (E_A), which has implications for TFTs as we will see in the next chapter. The $E_A = E_C - E_F$, i.e. the energy difference between the conduction edge and the Fermi level, can be found by measuring the temperature dependence of the
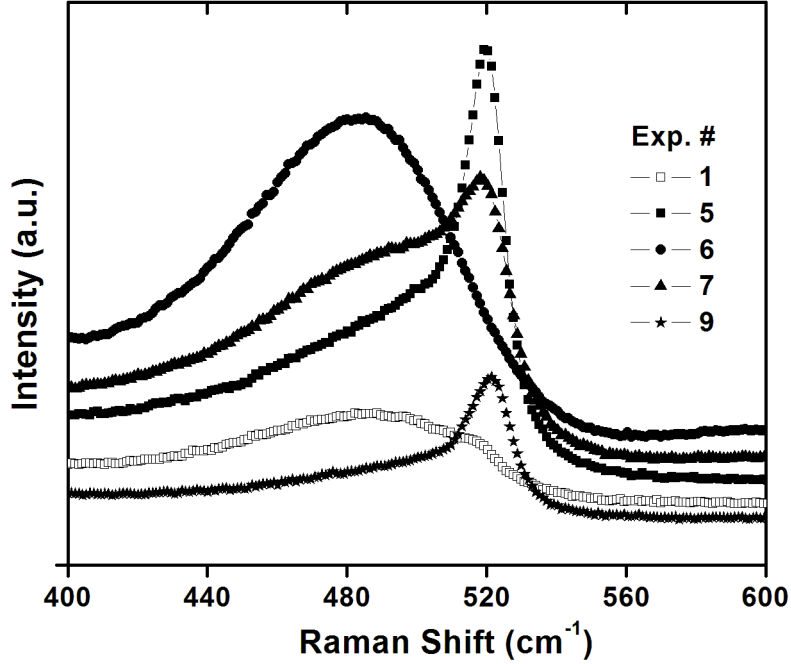
Figure 3.2: Raman spectra of several thin films obtained from the experiments listed in Table 3.1. The Raman signal was measured using a He-Ne laser with a wavelength of $632.8\,nm$.

conductivity and using

$$\sigma = \sigma_0 e^{-E_A/k_B T}, \tag{3.2}$$

where σ_0, k_B, and T are the conductivity pre-factor, Boltzmann's constant, and absolute temperature, respectively [63]. Figure 3.4 shows the temperature dependence of the conductivity of three nc-Si films. It is observed that they exhibit a temperature-activated conductivity, although E_A is not constant and varies with temperature. Such a variation in E_A has been reported elsewhere, and it has been attributed to a change in the carrier transport mechanisms by the temperature [64]. Transport mechanisms include thermionic emission of carriers over the potential barriers between crystalline regions and amorphous phase, tunneling through the potential barrier, and conduction through the band-tail states [64].
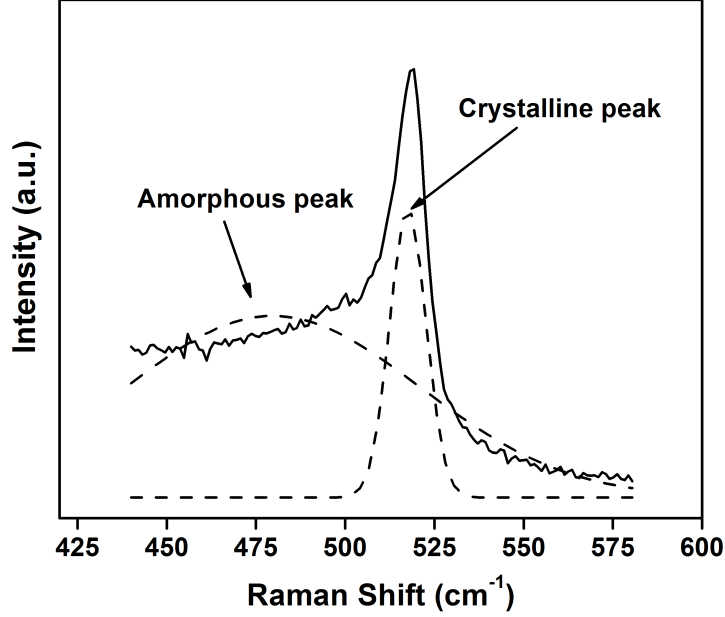
Figure 3.3: Decomposing a Raman signal (solid line) into two Gaussian peaks (dashed lines) centered around $517 - 520\,cm^{-1}$ and $480\,cm^{-1}$, which are due to crystalline and amorphous phases, respectively.

We calculated values of E_A in the temperature range of $280 - 360\,K$. They are $0.43{\pm}0.06\,eV$, $0.43{\pm}0.05\,eV$, and $0.43{\pm}0.03\,eV$ for the samples obtained from experiments #5, 7, and 9, respectively. We notice that activation energies are similar, although processing conditions and film crystallinities are different. Our values are within the range $0.2 - 0.55\,eV$ reported for nc-Si films by others [61, 63, 64, 65].

After calculating the crystallinity of layers from (3.1), we followed the procedure described in [56] to estimate the influence of PECVD variables on the crystallinity. According to [56], the average crystallinity due to each variable at each value is determined by averaging the results obtained with the variable at that value. For example, the average crystallinity at the plasma power of 100 W is

$$X_C = \frac{62 + 0 + 71}{3} \tag{3.3}$$
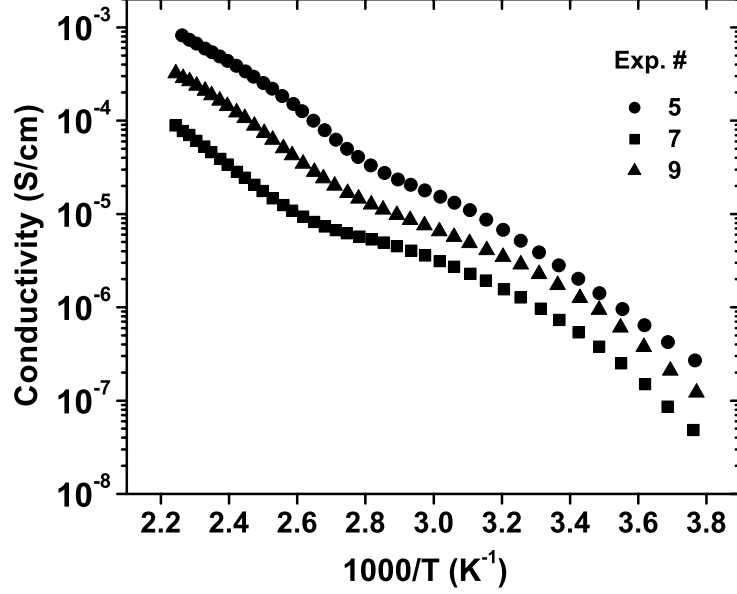
Figure 3.4: Temperature dependence of the conductivity of several nc-Si layers, processed based on Table 3.1. The activation energy varies with temperature.

which is the average of measured values when plasma power is equal to 100 W in experiments #7-9, see Tables 3.1 and 3.2. This procedure was repeated for all variables at their three values. The results are shown in Fig. 3.5.

From Fig. 3.5, we see that with increasing the hydrogen flow rate and decreasing the silane flow the crystallinity improves. The change in average crystallinity is large when silane and hydrogen flow rates are varied from minimum to maximum values. For example, the average crystallinity increases from zero to $\approx 60\%$ when silane flow rate varies from 8 to 4 sccm. Therefore, silane and hydrogen flow rates have a strong influence on film crystallinity, which is in line with results obtained by other research groups [21, 66]. Indeed, the ratio of H_2/SiH_4 flow rates is known as H_2 dilution ratio (HDR), and it is well known that by increasing the HDR the crystallinity increases [21].

The results in Fig. 3.5 (c) indicate that power density, plasma power divided by the PECVD electrode area, is the other important parameter and we can get higher crystallinity at higher powers, which is consistent with the results reported in [21]. On the other hand, from Fig. 3.5 (d), it is observed that the chamber pressure does

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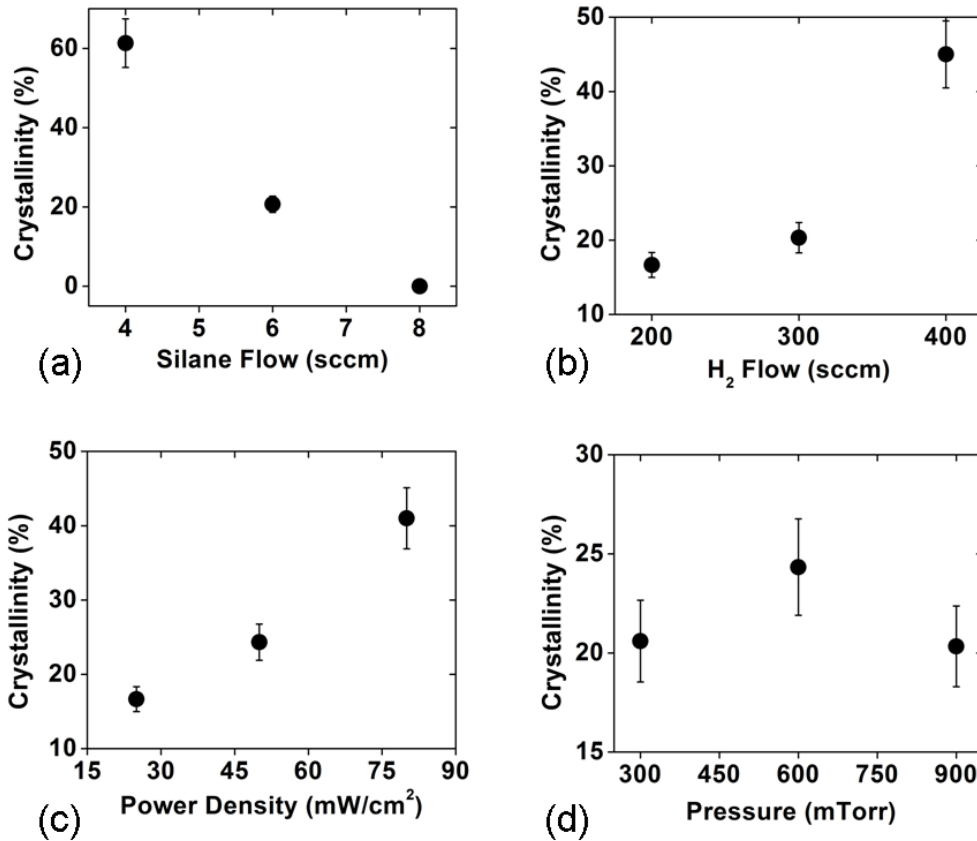
Figure 3.5: The average crystallinity versus PECVD parameters. Here, power density is the plasma power divided by the electrode area of our PECVD tool ($\approx 1264\,cm^2$).
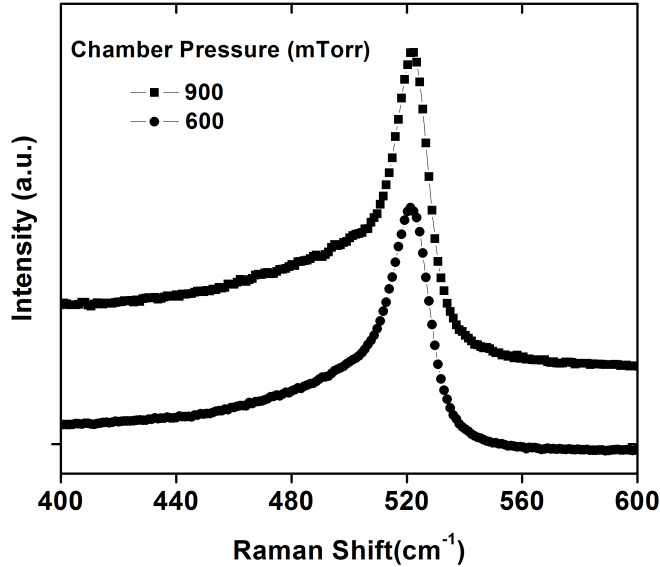
Figure 3.6: Raman spectra of two nc-Si layers deposited at two chamber pressures (900 and 600 mTorr), while kept constant other PECVD variables, i.e. $power = 100\,W$, and $HDR = H_2/SiH_4 = 400/4 = 100$.

not have a significant effect on the crystallinity, as its average is $\approx 20 - 25\%$ when the chamber pressure changes from 300 to 900 mTorr. To validate this conclusion, two additional films were deposited at chamber pressures of 900 and 600 mTorr, while keeping constant other process parameters such as power and HDR at 100 W and 100, respectively. Figure 3.6 shows their Raman spectra, where they have similar X_C of around 78%. It should be noted that the drawn conclusions, based on the results in Fig. 3.5, may be valid only within the window of parameters that we explored.

For bottom-gate TFT applications, the nc-Si layer should not be processed at low pressures and high plasma powers to avoid damaging the sensitive gate dielectric interface [24, 27]. As known, low chamber pressure and high plasma power result in high energy of ions, in the discharge, impinging and damaging the gate dielectric interface, and likely disrupting the crystal growth [67]. Therefore, low plasma powers along with medium or high process pressures are preferred. Indeed, it has

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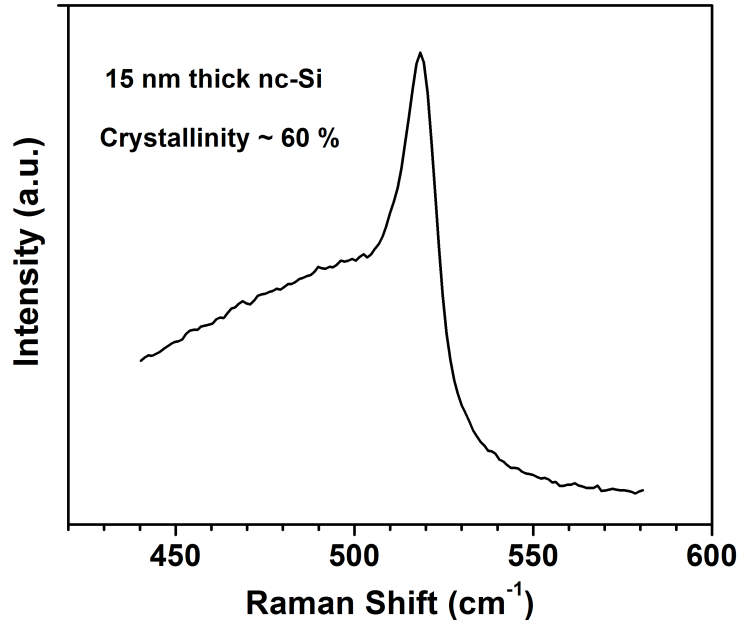
Figure 3.7: Raman spectrum of a 15 nm thick nc-Si film. Its crystallinity is approximately 60%.

been shown that when HDR is high the plasma power can be low, and nc-Si films can still be obtained [21]. Therefore, the combination of low plasma power, high HDR, and high pressure is desirable for nc-Si processing in bottom-gate TFTs.

Following these considerations, we were able to obtain highly crystalline films as thin as 15 nm. Figure 3.7 shows a Raman spectrum of a 15 nm thick layer, deposited at the chamber pressure of 900 mTorr and HDR of 100. The power density was low and $\approx 10 \, mW/cm^2$. Its crystallinity is $\approx 60\%$, implying formation of crystalline grains at the early stages of film growth.

We also used Transmission Electron Microscopy (TEM) to observe the structure of this layer at its interface with silicon nitride. Figure 3.8 (a) shows its TEM cross section. Here, we observe that crystalline grains, e.g. the dark regions highlighted by dashed circles, extend virtually to the nitride interface with no obvious presence of an amorphous incubation layer. Further confirmation of grain growth at the interface can be seen in the magnified image in Fig. 3.8 (b). As seen, the initial

layers consist of crystalline grains, and the material structure is similar to that in Fig. 3.1 (b) that we are looking for.

Therefore, it is possible to eliminate the amorphous incubation layer, which is required for device stability. Indeed, we were able to obtain nc-Si films as thin as 15-20 nm in two PECVD systems that are used in our laboratory. The PlasmaTherm system introduced before is a 13.56 MHz single chamber tool, with the electrode area of 14"×14", which is usually used for initial studies and material characterization. Another system is a 13.56 MHz multi-chamber cluster tool with the electrode area of 6"×6", manufactured by MVSystems Inc, which is mostly used for device fabrication. The results in Figs. 3.7 and 3.8 were actually obtained using the multi-chamber system. Similar results obtained by the single-chamber PECVD system have been published in Ref. [68].

3.3   Silicon Nitride Gate Dielectric

Electrical properties of the gate dielectric affect the device performance, such as field effect mobility and stability. We attempted to optimize the α-SiNx:H gate dielectric by adjusting the PECVD parameters. It is well known that the density of charge trapping centers and leakage current of silicon nitride are a function of its chemical composition, typically described in terms of the nitrogen to silicon ratio ([N]/[Si]). In this research, properties of three films of varying composition were evaluated before incorporating them into real devices.

The 300 nm thick α-SiNx:H layers were deposited in the multi-chamber PECVD system on p-type crystalline silicon (c-Si) substrates from a mixture of silane (SiH_4) and ammonia (NH_3). The NH_3/SiH_4 gas flow ratio was varied in the range 5-20 to obtain different compositions. Table 3.3 shows the PECVD conditions. The substrate temperature was fixed at 280 °C. The composition of layers was obtained by Elastic Recoil Detection Analysis (ERDA) and their chemical bonding was studied by Fourier-transform infrared (FTIR) spectroscopy. The FTIR spectra

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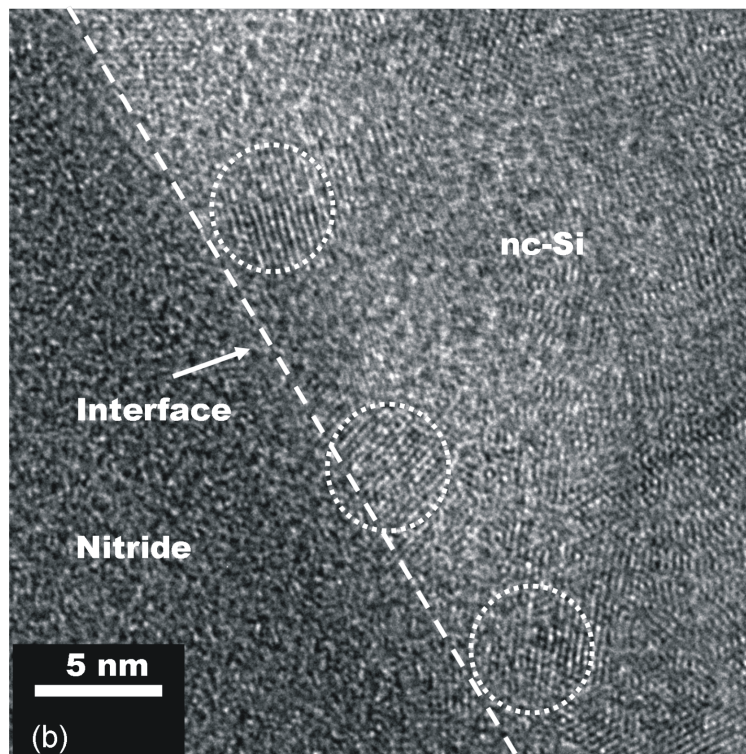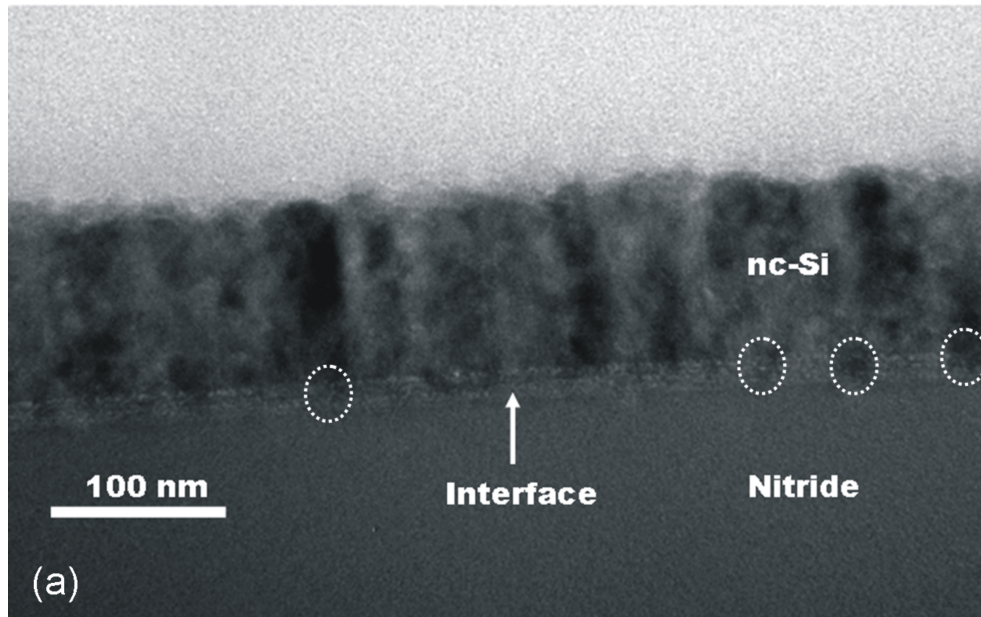
Figure 3.8: Transmission electron microscope (TEM) cross section image of the nc-Si film, (a) 100 nm scale bar, showing the entire cross section, (b) 5 nm scale bar, showing the interface between nitride and the nc-Si layer. Dashed circles show crystalline grains.

Table 3.3: The PECVD parameters for the three silicon nitride films.

Exp. #	$NH_3\,flow$ (sccm)	$SiH_4\,flow$ (sccm)	$Power\,density$ (mW/cm^2)	$Pressure$ $(mTorr)$
1	100	5	10	400
2	50	5	10	400
3	25	5	10	400

were measured by a Shimadzu FTIR-8400S spectrometer in the wavenumber range $600 - 3600\,cm^{-1}$. Their leakage current, breakdown field, and capacitance-voltage characteristics were measured on metal-insulator-semiconductor (MIS) test structures, using a Keithley 4200-SCS semiconductor characterization system. The MIS structures comprised of aluminum/α-SiNx:H/c-Si/aluminum with the nitride layer as the insulator.

Figure 3.9 shows the FTIR spectra of the nitrides. Here, the main absorption peaks are due to Si-N bonds at $880 - 900\,cm^{-1}$, Si-H bonds at $2150 - 2180\,cm^{-1}$, and N-H bonds at $3340\,cm^{-1}$. Usually, when the quality of nitrides is evaluated by FTIR data, the focus is on the peaks related to N-H and Si-H bonds. Si-N bonds are majority in various nitride layers. It is observed that by increasing the NH_3/SiH_4 from 5 to 20, the peak due to N-H bonds becomes stronger. This implies that more nitrogen and hydrogen atoms are incorporated in the material. We obtained the values of [N]/[Si] from ERDA, which is believed to be a very accurate characterization method. The [N]/[Si] increases from 1 to 1.3 when NH_3/SiH_4 increases from 5 to 20. This along with the FTIR data indicate that the nitride is becoming nitrogen(N)-rich, i.e. the nitride layer from experiment #1 in Table 3.3 is N-rich compared to that from experiment #3, which is silicon(Si)-rich. The composition of nitride has a strong bearing on TFT performance. In particular, the rate of charge trapping in the nitride, and hence device stability, is governed by its composition. This will be discussed in greater detail later along with the performance characteristics of fabricated TFTs.
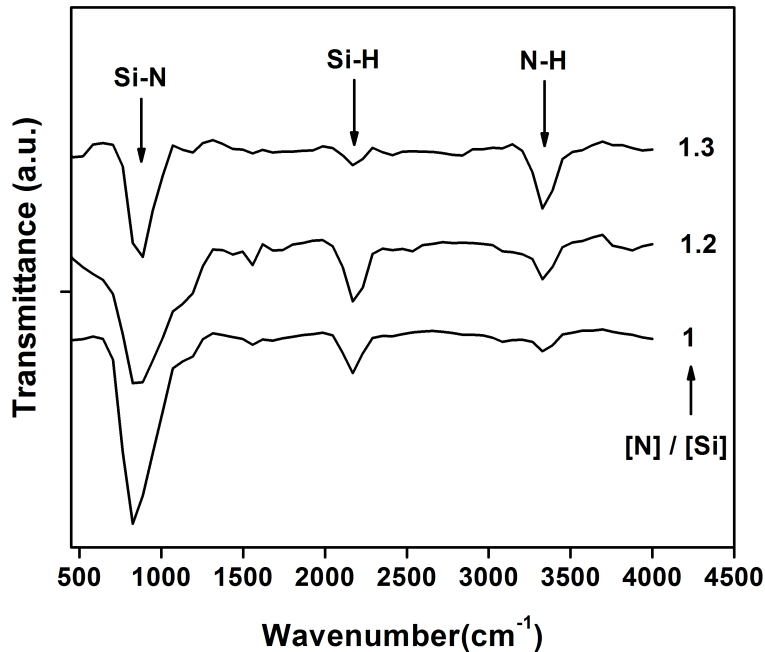
Figure 3.9: FTIR spectra of various nitride films with [N]/[Si] of 1.3, 1.2, and 1, processed at NH_3 to SiH_4 of 20, 10, and 5, respectively.

The electrical properties of α-SiNx:H films were characterized using MIS structures. Depicted in Fig. 3.10 are capacitance-voltage (C-V) curves when the voltage applied to MIS capacitors was swept in forward (negative to positive) and reverse (positive to negative) directions, with the bottom aluminum contact grounded. It is seen that forward and reverse curves are shifted relative to each other, exhibiting hysteresis. This shift is due to charge (electron) trapping within the α-SiNx:H bulk and its interface with silicon [69]. Figure 3.10 shows that the hysteresis width is $\approx$ 2, 14, and 30 V for [N]/[Si] of 1.3, 1.2, and 1, respectively.

Therefore, we observe increased charge trapping at lower [N]/[Si] ratios. This implies that from the device stability standpoint, N-rich α-SiNx:H is preferred over the Si-rich counterpart, which is consistent with previous studies on a-Si:H TFTs [70]. Electron Spin Resonance (ESR) measurements have shown that Si-rich nitrides have higher density of silicon dangling bonds than the N-rich counterpart
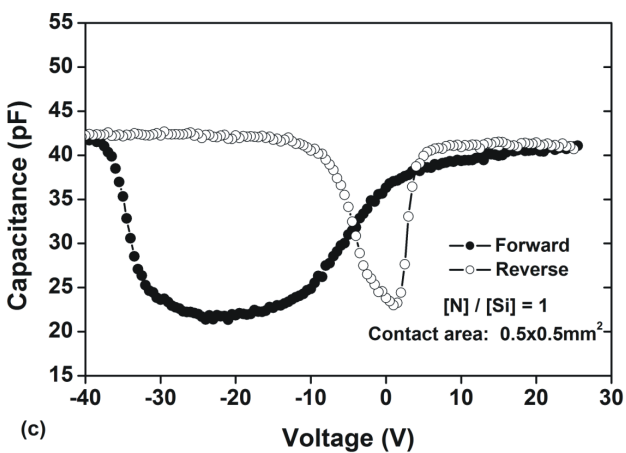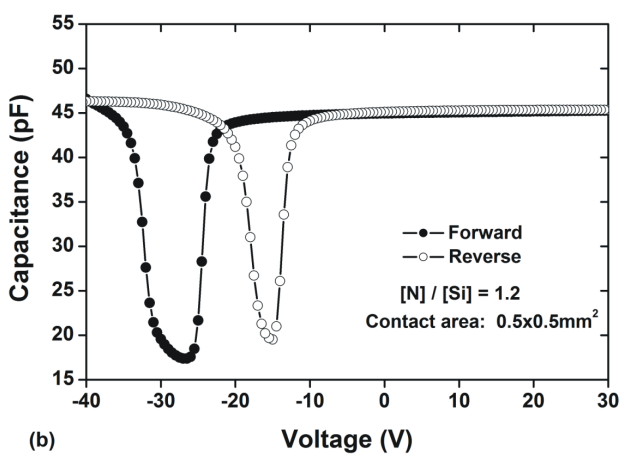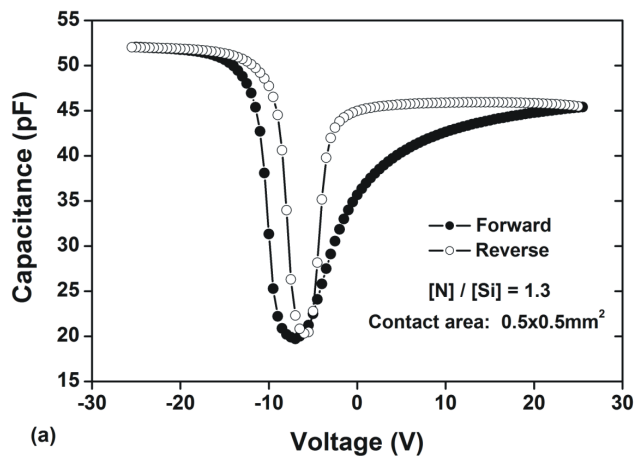
Figure 3.10: Capacitance-voltage (C-V) characteristics of nitrides with [N]/[Si], (a) 1.3, (b) 1.2, and (c) 1. The curves were obtained by sweeping the voltage across MIS capacitors in forward (negative to positive) and reverse (positive to negative) directions.

[70]. Dangling bonds act as charge trapping centers and lead to the observed hysteresis. In chapter two, we addressed various charge trapping mechanisms and showed them in Fig. 2.8, when we discussed the MIS structure.

The leakage current (I_L) of the nitrides were also measured on the same MIS structures. The measurement of leakage current is usually performed before device fabrication, to evaluate the suitability of nitride for the gate dielectric, and to estimate the gate leakage current that may be obtained in real devices. Figure 3.11 shows leakage current density (leakage current divided by MIS area) as a function of the applied electric field (E). It is seen that I_L is about $10 - 40\,nA/cm^2$ for $E{\leq}2\,MV/cm$ in three layers. Usually, in TFTs, the applied E is below $2\,MV/cm$. Now, let us estimate the gate leakage current that may be obtained under similar operating condition. For a TFT with an area of $10^{-5}\,cm^2$, i.e. $W = 100\mu m$ and $L = 10\mu m$, I_L is calculated to be around $10^{-13}\,A$, which is acceptable for TFTs in OLED displays. Later, when we discuss our device characteristics, we notice that the gate leakage currents are even lower than this value. From Fig. 3.11, we also see that I_L gradually increases with electric field, which is attributed to the electron injection and trapping mechanisms shown in Fig. 2.8, particularly, to those that are augmented by larger electric fields, e.g. direct tunneling from valence band, Fowler-Nordheim injection, and trap-assisted injection. As seen, at electric fields $E{\geq}2\,MV/cm$, I_L of the Si-rich nitride is larger than that of the N-rich counterpart. The obtained results are consistent with those reported by others [70, 71]. We also note that the leakage current that saturates at fields greater than $4.7\,MV/cm$ is due to the current compliance setting of our characterization system.

3.4   Summary

In this chapter, we studied how the crystallinity of nc-Si layers is affected by PECVD conditions. We performed the set of nine experiments based on the Taguchi orthogonal arrays that allowed us to investigate a wide process window. We ob-
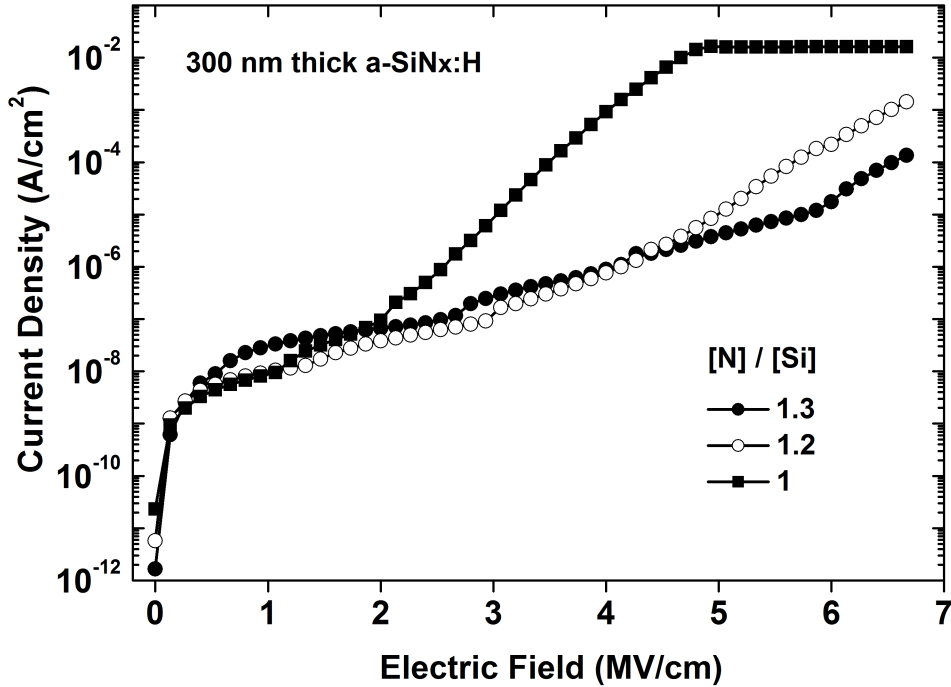
Figure 3.11: Leakage current density as a function of electric field, for the silicon nitrides with [N]/[Si] of 1.3, 1.2, and 1, processed at NH_3 to SiH_4 of 20, 10, and 5, respectively.

tained layers that were amorphous-like (with zero crystallinity) and layers with different crystallinities in the range 40-70%. We then analyzed the results, where we concluded that hydrogen and silane flow rates are the most important parameters in achieving layers with high crystallinity. It was also shown that the chamber pressure does not have a significant effect on the film crystallinity. The conclusions drawn out of this part led us to obtain very thin (15 nm) layers with crystallinity of around 60%. Furthermore, we showed that it is possible to eliminate the amorphous incubation layer, as TEM pictures showed that crystalline grains start growing right from the nitride interface, which is needed for bottom-gate TFTs.

Measurement results showed that the conductivity of nc-Si layers is several orders of magnitude higher than that of the amorphous counterpart. They were

around $1 - 5\,\mu S/cm$ and $10^{-9}\,S/cm$, respectively, which is attributed to unwanted doping by impurities such as oxygen that are incorporated in the film during PECVD processes. We also measured the conductivity activation energy of nc-Si layers, which was around 0.45 eV.

In the second part, we measured I-V and C-V characteristics of three nitride layers, with various compositions [N]/[Si] of 1.3, 1.2, and 1, on MIS structures. In their C-V curves, we saw a hysteresis of around 2, 14, and 30 V, respectively. The hysteresis was attributed to the charge trapping in the nitride. In this regard, various charge trapping and injection mechanisms were introduced from literature. The conclusion of this part was that nitrogen-rich nitrides are suitable for TFT application that can result in less charge trapping and, thus, better device stability.

Chapter 4

Nanocrystalline Silicon Thin Film Transistor Structures

4.1   Introduction

In this chapter, we discuss the performance characteristics of several bottom-gate
nc-Si TFTs fabricated in the course of this research. We investigated the causes
of the high drain-source leakage current (I_{OFF}) in these devices by analyzing ex-
perimental results in conjunction with numerical simulations. We related the I_{OFF}
to the conductivity of the nc-Si channel layer, and to the quality of the channel
layer/passivation nitride interface. Our TFT structure is based on the process pre-
sented in Fig. 2.1 (b). The channel layer either consists of a single nc-Si layer or a
bi-layer of nc-Si/α-Si:H. We call them single-layer nc-Si and bi-layer nc-Si/α-Si:H
structures, respectively. The optimum channel layer that yields the lowest I_{OFF}
comprises of a nc-Si/α-Si:H bi-layer. We show that this structure meets targeted
requirements, while it has its own limitations and the nc-Si/α-Si:H bi-layer should
be designed carefully.

We then used that optimum channel layer as the reference and fabricated several
TFTs with variable nitride gate dielectric. The goal is to find the best nitride that
yields highest possible field-effect mobility and stability. It is well-known that, in

α-Si:H TFTs, the performance parameters are dependent on the composition of the gate dielectric, the ratio of the concentration of atomic nitrogen to that of atomic silicon, i.e. [N]/[Si]. In the second part, we discuss the performance characteristics of the fabricated devices with different nitride compositions.

4.2   TFT Fabrication

The cross section of bottom-gate inverted-staggered TFT structures, i.e. single-layer nc-Si and bi-layer nc-Si/α-Si:H, are shown in Fig. 4.1, which require five lithography process steps. First, 100 nm molybdenum was sputtered on a glass substrate and patterned to define the gate. Then, the trilayer was deposited in one PECVD cycle, which comprised of 300 nm amorphous silicon nitride (α-SiNx:H) as the gate dielectric, active layer, and 300 nm α-SiNx:H as the passivation dielectric. The deposition conditions for both passivation and gate dielectric nitrides are the same as those of the experiment #1 given in Table 3.3. Thus, in the fabrication, the only difference between TFTs is their active layer, also called channel layer. The channel layer comprised of 65 nm nc-Si in one set of TFTs (TFT A), and a bi-layer of 65 nm nc-Si capped with 100 nm α-Si:H in another set (TFT B). Other details of the fabrication sequence was discussed before and can also be found in Ref. [60]. The layers were deposited at 280 °C in the multi-chamber 13.56 MHz PECVD system. The nc-Si layer was deposited by silane highly diluted in hydrogen ($HDR = H_2/SiH_4 = 100$), which was shown to induce microstructural changes from amorphous to the nanocrystalline phases. TFTs with channel length ranging from 25 to 200 μm were fabricated while the channel width was kept constant at 100 μm. Transfer and output characteristics were measured by a Keithley 4200-SCS system.
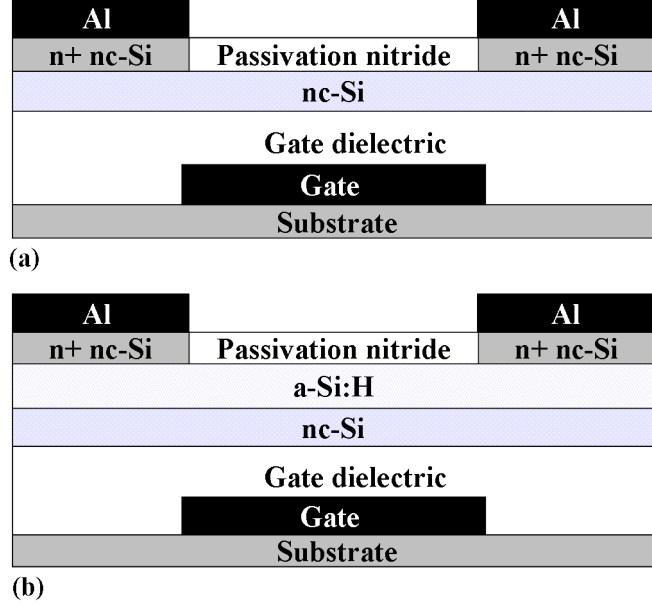
Figure 4.1: Cross section of the inverted-staggered TFT structure, (a) single nc-Si channel layer in TFT A, (b) nc-Si capped with α-Si:H in TFT B.

4.3   Results and Discussion

Transfer characteristics of TFT A and TFT B are shown in Fig. 4.2. It is seen that I_{OFF} is proportional to the drain-source voltage (V_{DS}) at a given negative gate voltage, indicating a resistance that is determined by the effective conductivity of the channel layer. For example, in Fig. 4.2 (a), at the gate-source voltage (V_{GS}) of $-10\,V$, I_{OFF} is around 10^{-10}, 10^{-9}, and $10^{-8}\,A$ at V_{DS} values of 0.1, 1, and 10 V, respectively. Here, the position of Fermi-level, i.e. band bending, in the channel is the determining factor. Specifically, the band bending in the bulk as well as that at the interfaces with the passivation (top) and gate dielectric (bottom) nitrides must be considered. As seen, I_{OFF} in TFT A is nearly two orders of magnitude higher than that in TFT B. For example, at $V_{DS} = 1\,V$ and $V_{GS} = -10\,V$, the off-current is $2\,nA$ and $10\,pA$, respectively. To explain this difference, we consider the nitride interfaces and their effect on the band bending in the channel. The gate dielectric interface is similar in both TFTs, as it is made of the same material deposited under the same process conditions.

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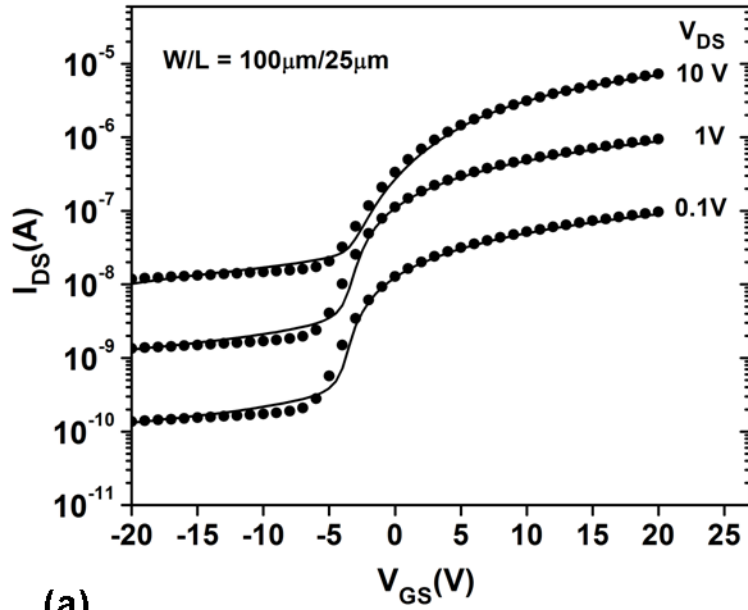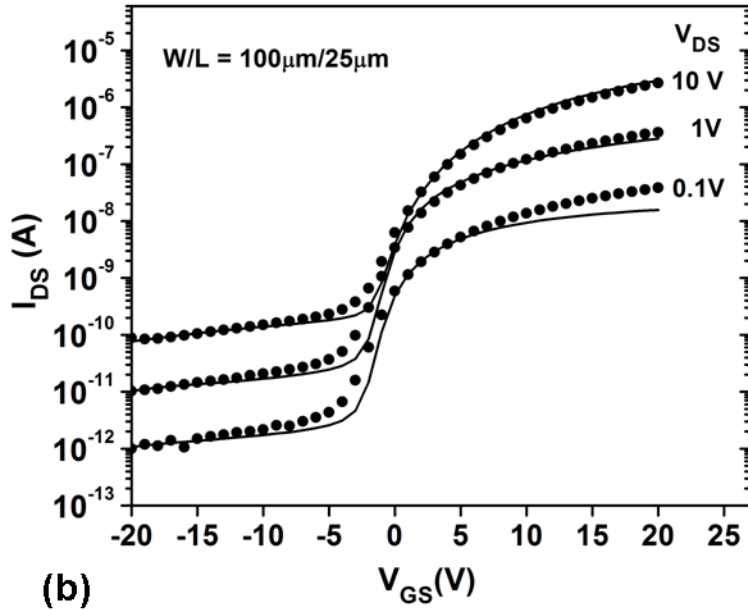
Figure 4.2: Transfer characteristics of (a) TFT A with an all nc-Si channel layer of thickness $65\,nm$ and (b) TFT B with $65\,nm$ nc-Si channel layer capped with $100\,nm$ α-Si:H. The aspect ratio $W/L = 100\mu m/25\mu m$. Dots: experiment, lines: computation.

But the passivation nitride interface is different: it is with the nc-Si layer in TFT A, while in TFT B, it is with the α-Si:H cap layer. The quality of these two interfaces is not necessarily the same. Interfaces are prone to parasitic band bending due to non-idealities such as dangling bonds and fixed charges. Therefore, any conduction due to a parasitic band bending at the passivation nitride interface adds to the bulk conductivity of the channel layer [12]. We decided to investigate this by numerical simulation of the transfer characteristics that provide significant insight on the properties of different layers and the role of interfaces.

4.4   nc-Si TFT Modeling and Simulation of Transfer Characteristics

The numerical simulations were carried out using the package Medici [72], where the channel layer attributes such as density of midgap defect states, electron mobility, and density of active dopants are the input parameters. The former two were estimated from the measured transfer characteristics (values are given later). The latter was indirectly estimated from simulations by fine-tuning the value of the dopant concentration, which is an input parameter, till the measured and simulated values of the activation energy (E_A) of the channel layer are in agreement. This is doable because E_A is determined by the balance between the density of defects and the density of active dopants. Therefore, as we can calculate the density of defects and E_A from experimental results, we are able to estimate the density of active dopants by simulations.

The E_A was retrieved from an Arrhenius plot along the lines reported in [73, 74]. The temperature (T) dependence of drain-source current (I_{DS}), in the range 25 to 100 °C, is shown in Figs. 4.3 (a) and (b) for TFT A and TFT B, respectively. The corresponding activation energies are also indicated. Here, we note that the sheet conductance (σ) of the device at each value of V_{GS} and T is defined as

$$\sigma = \frac{I_{DS}}{V_{DS}} \times \frac{L}{W} \tag{4.1}$$
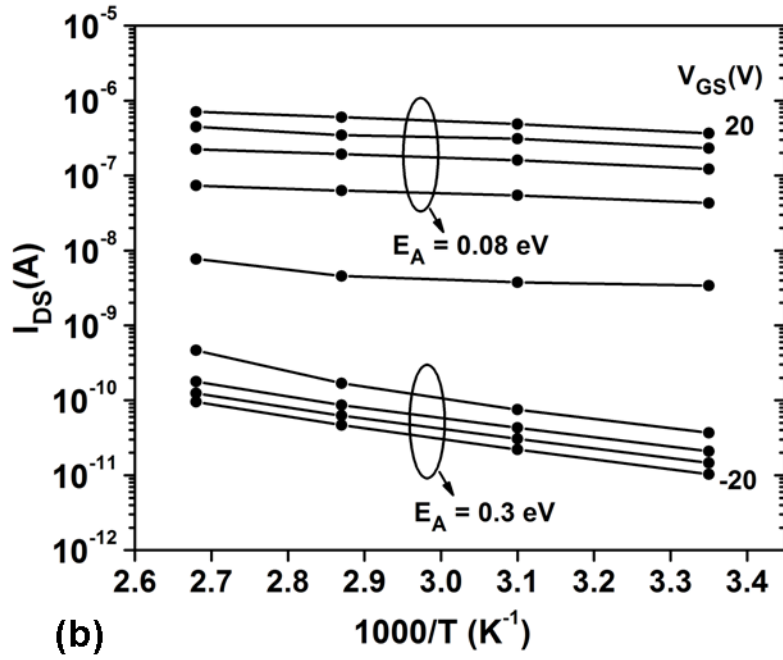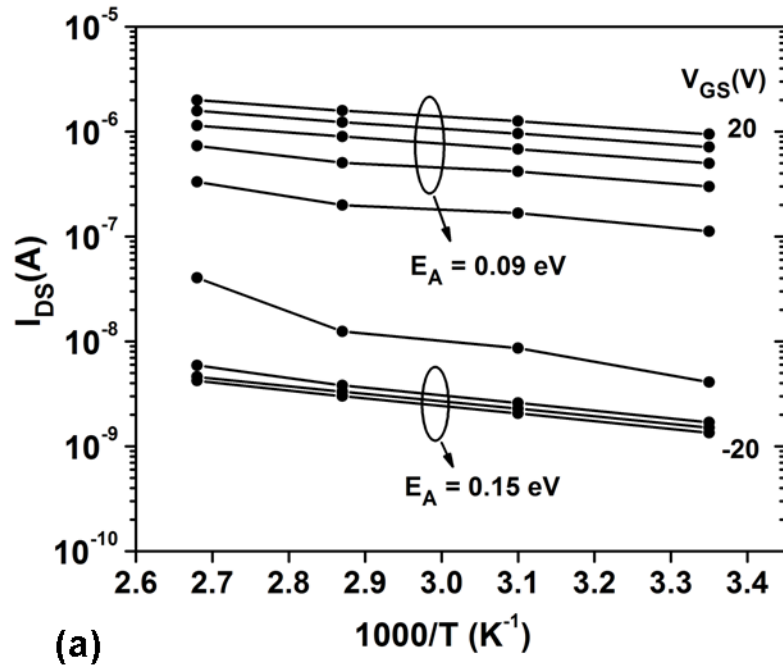
Figure 4.3: Drain-source current of (a) TFT A and (b) TFT B, measured in the range of 25 to 100 °C at a drain voltage of 1 V, and different gate voltages indicated in 5 V steps. The effective activation energy (E_A) is also shown.

where L and W are the device length and width, respectively [74]. From (4.1) and (3.2), we can write

$$I_{DS} = I_{DS0} \times e^{-E_A/k_B T} \tag{4.2}$$

where I_{DS0} is a pre-factor. Thus, the E_A is determined from the slope of the Arrhenius plots. At positive gate voltages, where the channel layer is in accumulation, the E_A is 0.08-0.09 eV in both devices, which is very similar to that in α-Si:H TFTs [73, 74]. But this is different in the off-state. For negative gate voltages, the E_A is 0.15 eV and 0.3 eV for TFT A and TFT B, respectively. We attribute this difference to an additional band bending due to the passivation nitride interface in TFT A, and we attempted to show that this extra band bending exists, by numerical simulations in Medici. In what follows, we show that the passivation nitride interface is slightly in accumulation and, thus, is more defective in TFT A with nc-Si compared to that in TFT B with a-Si:H.

Before showing the final simulation results, we go through a series of discussions to clarify how the simulations were performed and parameters were fine-tuned. At first, we discuss the effect of gate and passivation nitride interfaces on band bending and I-V characteristics of TFTs, in general. As mentioned earlier, nitride layers tend to have large concentration of fixed charges and imperfections, particularly, at their interface with silicon layers. Powell and Pritchard [12] reasoned that the presence of fixed charges at the passivation nitride interface increases the off-state conduction by several orders of magnitude, depending on the amount of charge and due to formation of an accumulation region at the interface. It was also shown that fixed charges at the passivation nitride interface do not affect the on-current considerably [12]. In addition, one should also consider the gate nitride and the likely presence of fixed charges there. Lustig and Kanicki [69] argued that the threshold voltage is affected by the presence of these fixed charges, where they lead to a parallel shift in transfer characteristics. Hence, in a practical TFT, one may see a shift in the transfer characteristics along the V_{GS} coordinate (due to fixed charges at the gate nitride interface) and a shift in the I_{OFF} along the I_{DS} coordinate (due to fixed charges at the passivation nitride interface). Figure 4.4 shows simulated
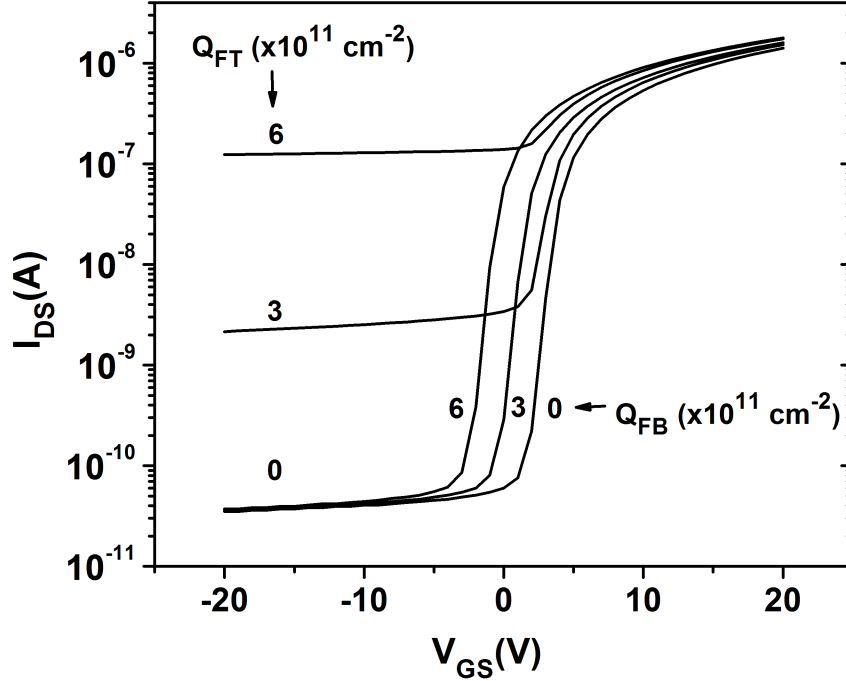
Figure 4.4: Transfer characteristics computed at $V_{DS} = 1V$, when the density of fixed charges at the gate dielectric interface (Q_{FB}) and at the passivation nitride interface (Q_{FT}) vary from zero to $6 \times 10^{11}\ cm^{-2}$ in steps of $3 \times 10^{11}\ cm^{-2}$. The structure is similar to TFT A, shown in Fig. 4.1.

TFT transfer characteristics, at $V_{DS} = 1V$, when the density of fixed charges at the gate nitride interface (Q_{FB}) and at the passivation nitride interface (Q_{FT}) vary from zero to $6 \times 10^{11}\ cm^{-2}$.

We see that increasing the Q_{FB} causes a parallel shift in transfer characteristics, while increasing the Q_{FT} leads to an increase in I_{OFF}, which are in line with previous reports [12, 69]. In Fig. 4.4, an increase in Q_{FB} results in higher off-current at gate biases between -4 to 0 V, due to the higher band bending near the gate dielectric interface. However, at larger negative gate biases, I_{OFF} does not depend on Q_{FB}, indicating that the band bending due to Q_{FB} is modulated by the gate bias, reducing its contribution to I_{OFF}. But this is not the case for Q_{FT} and its associated band bending. As seen, even at negative gate voltages down to -20

V, I_{OFF} does depend on Q_{FT}, and, consequently, on the band bending induced by Q_{FT}. This is illustrated in greater detail in Figs. 4.5 (a) and (b), which depict the simulated band bending across the channel layer as a function of distance (x) from the passivation nitride interface, for a fixed charge density of $6{\times}10^{11}\,cm^{-2}$ at the passivation nitride and gate nitride interface, respectively.

From Fig. 4.5, it is seen that the band bending due to Q_{FT} remains intact when the gate bias is negative, leading to the high off-current in the nc-Si TFT observed here as well as in Ref. [32]. On the other hand, the band bending at the gate dielectric interface is easily modulated and compensated by the negative gate voltage, shown in Fig. 4.5 (b), and the off-current is reduced accordingly.

Now, we should be able to simulate the characteristics of TFT B without considering Q_{FT}, and those of TFT A otherwise. The lines in Fig. 4.2 (a) and (b) display the simulation results where Q_{FT} was set to $6{\times}10^{11}\,cm^{-2}$ and zero, respectively. Therefore, in TFT A, the nc-Si/passivation nitride interface is in accumulation, due to additional fixed charges and an extra band bending there, leading to the increased off-current. On the other hand, the gate dielectric interface cannot be considered ideal, i.e. without any fixed charges. Indeed, for both TFTs, a Q_{FB} of $4{\times}10^{11}\,cm^{-2}$ was also included in simulations. The values of fixed charges are consistent with those reported in Ref. [12].

In this section, we address the model parameters that we used in simulations, particularly the distribution of density of states (DOS) in the energy gap of the nc-Si active layer. The density of states model comprises of a single-exponential distribution of band tail states plus a constant density of deep defect states, shown in Fig. 4.6. This model is essentially the same as that shown in Fig. 1.5, and it has been used by others in the modeling and simulation of α-Si:H TFTs [12, 75]. Indeed, it has been reported that the DOS distribution is not unique and experimental results could be reasonably fitted by using other DOS profiles, too [12]. For example, band tail states can be modeled by the summation of two exponential terms instead of one, or the midgap defect states can be modeled by the summation of several
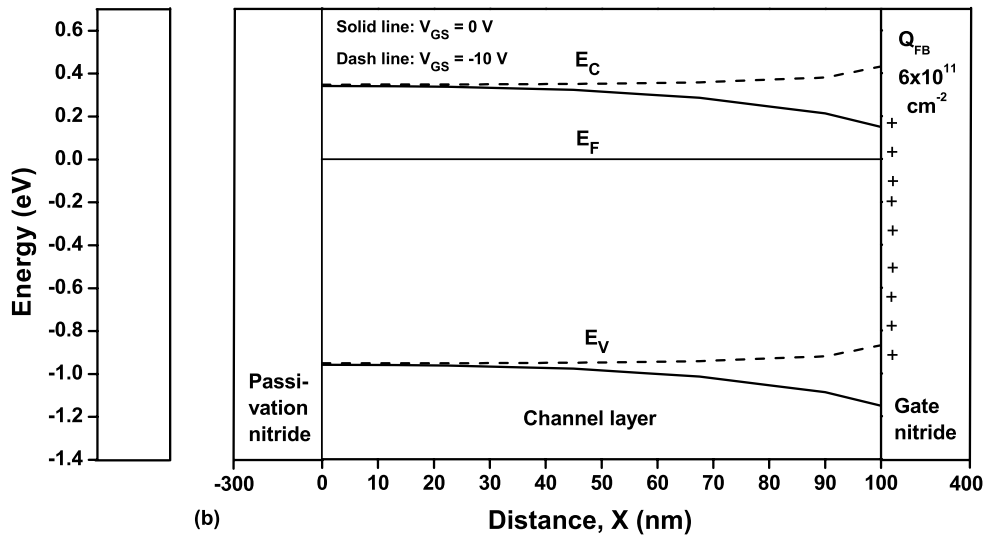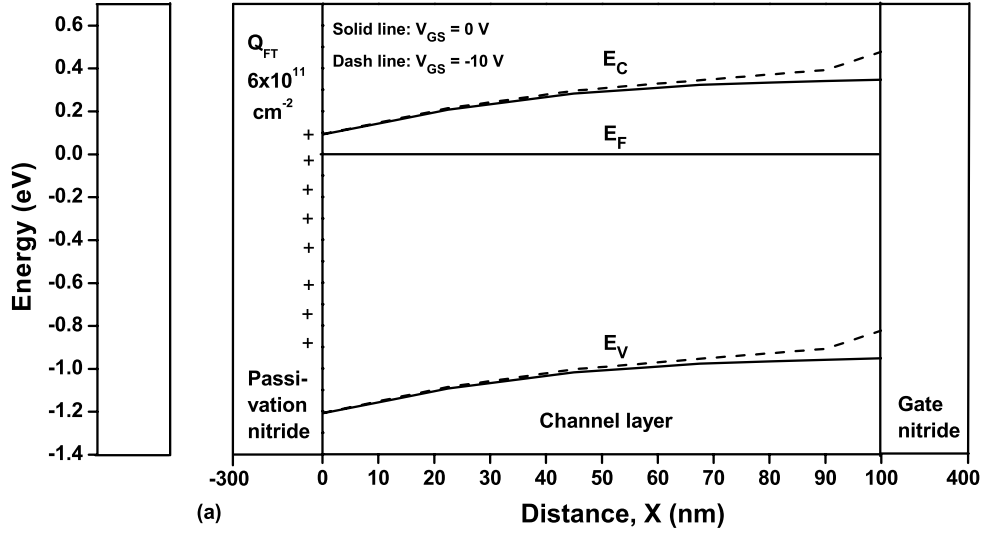
Figure 4.5: Computed band bending profile in the TFT channel layer, (a) $Q_{FT} = 6 \times 10^{11}\, cm^{-2}$ and (b) $Q_{FB} = 6 \times 10^{11}\, cm^{-2}$. The solid and dash lines are for V_{GS} of 0 and -10 V, respectively. The structure is similar to TFT A. For simplicity, the ΔE_C and ΔE_V between the channel layer and nitrides are not shown.

Gaussian peaks centered around the midgap [41, 76]. We chose the simplest case as recommended by Powell [12].

In general, the DOS can be divided into upper midgap states (located above the intrinsic Fermi level at 0 eV) and lower midgap states (located below the intrinsic Fermi level). Here, we only discuss the upper midgap states (Fig. 4.6), as our temperature-dependent measurements (Fig. 4.3) on n-type devices do not provide information on the lower midgap states [40]. In the model, the density of defect states (N_T) was estimated from the subthreshold slope (SS) of TFTs. From Fig. 4.2, we calculated the $SS \approx 2V/dec$. The N_T and SS are related by

$$SS = qk_BT\frac{N_Tt_S + D_{it}}{C_{gate}Log(e)} \tag{4.3}$$

where q, k_B, T, t_S, D_{it} and C_{gate} are the electron charge, Boltzmann's constant, absolute temperature, channel layer thickness, density of states at the gate dielectric interface, and gate dielectric capacitance per unit area, respectively [10]. In (4.3), two unknowns are D_{it} and N_T, and others can be found using device dimensions given before, i.e. $qk_BT = 0.026\,eV$, $t_S = 15\,nm$, and $C_{gate} = 2\times10^{-8}\,F/cm^2$. Putting $D_{it} = 0$, we estimate $N_T \approx 1\times10^{18}\,cm^{-3}$.

In simulations, further fine-tuning of the N_T was required to obtain the best fit to experimental results. Figure 4.7 shows the simulated transfer characteristics when the simulation parameter N_T varies in the range $(0.5-5)\times10^{18}\,cm^{-3}$. As seen, I_{OFF} is a function of N_T, and the best fit in Fig. 4.2 achieved when $N_T = 5\times10^{18}\,cm^{-3}$.

For lower values, I_{OFF} decreases faster, or in other words the Fermi level moves towards the midgap at negative gate voltages. Indeed in the off-state, as the gate voltage decreases, the Fermi level moves from upper midgap and towards the valence band tail states. But it may be pinned at the onset of the valence band tail states or by a large density of defect sates [12]. From Fig. 4.7, we deduce that the Fermi level is pinned by N_T of $5\times10^{18}\,cm^{-3}$, since I_{OFF} is fairly constant. This I_{OFF} dependency is also seen in experimental results in Fig. 4.2. But for smaller values, the simulated I_{OFF} gradually decreases and drops to values around $10^{-28}\,A$ (not shown in Fig. 4.7). For example, this happens at $V_{GS} = -4\,V$ for
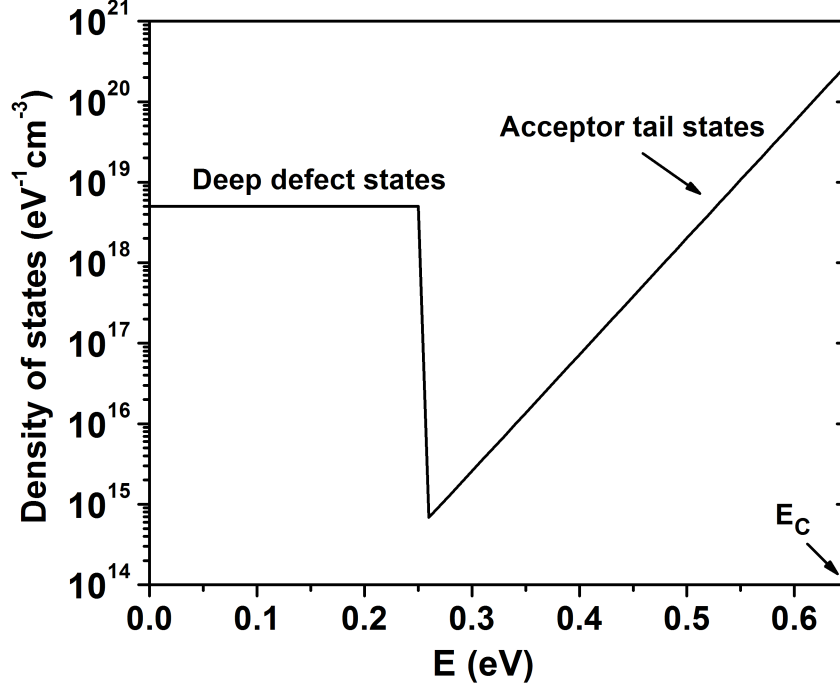
Figure 4.6: Profile of density of states in the nc-Si active layer. The intrinsic Fermi level and conduction band edge energies are at zero and 0.65 eV, respectively.

$N_T = 5 \times 10^{17}\,cm^{-3}$. In this case, the Fermi level moves through defect states and gets closer to the midgap and to the onset of lower midgap states, where there are virtually no conducting electrons to make a significant current. A similar I_{OFF} behavior has been experimentally observed in α-Si:H TFTs [73], implying that the density of defect states in these α-Si:H TFTs is lower than that in our nc-Si TFTs.

Table 4.1 summarizes the key parameters retrieved from measurements and the values used in simulations. Here, the electron field-effect mobility (μ_{FE}) was obtained from the transfer characteristics, depicted in Fig. 4.2, and the N_T was estimated from the TFT subthreshold slope and fine-tuned by simulation, as described earlier. As mentioned before, the simulation parameter N_D (active dopant concentration) was used in conjunction with the measurement parameters N_T and E_A. We varied N_D to obtain the best fit, which gave rise to the value of $1.25 \times 10^{18}\,cm^{-3}$. Subsequently, for validation purposes, the simulation parameter E_A was obtained

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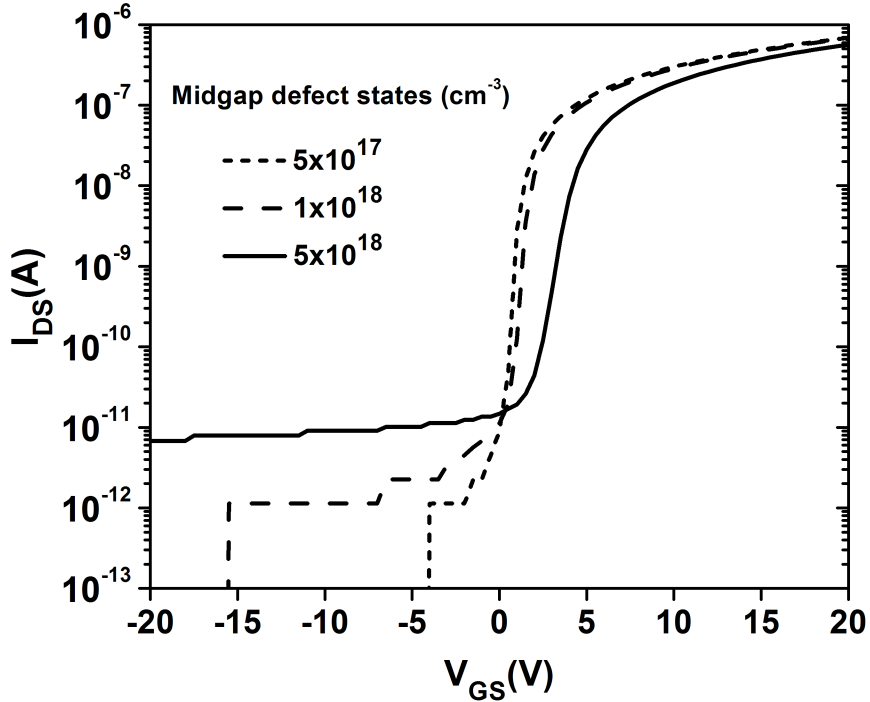
Figure 4.7: Transfer characteristics of a TFT computed as a function of density of midgap defect states (N_T).

as 0.36 eV, which is in agreement with the measured value of 0.3 eV. Overall, the consistency between measurements and simulations appears to be reasonable. A sample Medici code used in numerical simulations, showing details of input statements and model parameters, can be found in Appendix B.

As discussed and seen from Table 4.1, we were able to perform our simulations without having an experimental knowledge of the concentration of dopants (N_D) in the nc-Si active layer. Simulations showed that N_D is around $1.25 \times 10^{18}\, cm^{-3}$.

Table 4.1: Summary of measurement and simulation parameters.

Parameter	$\mu_{FE}\,(cm^2/Vs)$	$N_T\,(cm^{-3}eV^{-1})$	$E_A\,(eV)$	$N_D\,(cm^{-3})$
Measurement	$0.3 - 0.8$	$\approx 10^{18}$	0.3	n/a
Simulation	0.75 ± 0.25	5×10^{18}	0.36	1.25×10^{18}

Later, we did Secondary Ion Mass Spectroscopy (SIMS) on several nc-Si films, which provided information on the concentration of different impurities and atoms that are usually available in PECVD deposited films. Figure 4.8 shows the results, where the structure is 125 nm nc-Si and 250 nm nitride deposited on a crystalline silicon (c-Si) substrate. Here, only oxygen and phosphor atoms may act as donors and hydrogen passivates dangling bonds. Each oxygen and phosphor atom can give two electrons and one electron to the silicon network, respectively. From Fig. 4.8, the concentration of oxygen and phosphor atoms in the nc-Si layer is $3 \times 10^{17} \, cm^{-3}$ and $4 \times 10^{17} \, cm^{-3}$, respectively. If we assume that all these impurities are active (in practice, they are not), we find $N_D \approx 2 \times 3 \times 10^{17} + 4 \times 10^{17} = 1 \times 10^{18} \, cm^{-3}$, which is in agreement with the value obtained from simulations. It should be noted that this rough calculation was done to only verify the simulations, as the concentration of impurities, from SIMS, is not accurate.

4.5   Optimum Structure

In previous section, we saw that the preferred channel layer should comprise of a nc-Si layer with an α-Si:H cap, which allowed us to obtain lower off-current, since the passivation nitride interface with the α-Si:H cap is not in accumulation as opposed to that with the nc-Si layer. But the question remains as to how thick the α-Si:H and nc-Si layers should be to further reduce the off-current and yet preserving a high on-current. Although the cap layer reduces I_{OFF}, it increases the source/drain series resistance seen by electrons flowing to/from the accumulation channel in the on-state, reducing the on-current [34]. The on-current path is shown in Fig. 4.9 (a). In this Figure, the vertical motion of electrons underneath n^+ nc-Si source/drain contacts is being referred, where a series resistance is caused by the α-Si:H cap.

Therefore, the thickness of the α-Si:H cap should be optimized. Figure 4.10 shows the simulated transfer characteristics as a function of the α-Si:H thickness, where both nitride interfaces were considered ideal, i.e. without fixed charges. It
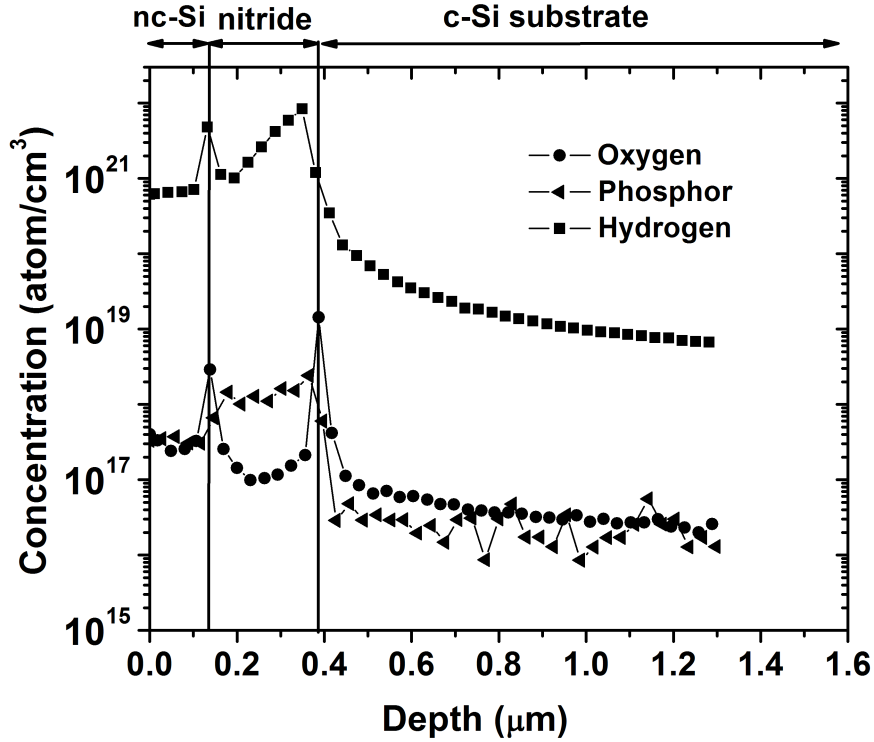
Figure 4.8: Concentration of several impurities in the nc-Si active layer, obtained from Secondary Ion Mass Spectroscopy (SIMS). Here, only oxygen and phosphor atoms act as donors and hydrogen passivates dangling bonds.

is seen that the on-current decreases with increasing the α-Si:H thickness. The reduction is about two orders of magnitude for a 200 nm thick α-Si:H, but only a factor of 2-3 for thicknesses less than 50 nm. This observation is due to the fact that, in the on-state, the mechanism of current conduction through the α-Si:H includes space-charge-limited current (SCLC), which is a non-linear variable of the film thickness [77], as well as regular drift and diffusion components. The SCLC is typically observed in insulators and semiconductor materials with low conductivity, such as α-Si:H, when the number of injected carriers into the material exceeds that at the thermal equilibrium. Once this happens, the charge neutrality is perturbed and electric field distribution becomes non-uniform in the sample and, for example, the current does not obey the Ohm's law anymore [77, 78]. In TFTs, this happens in the on-state as the on-current is orders of magnitude higher than the off-current.

(a)

(b)
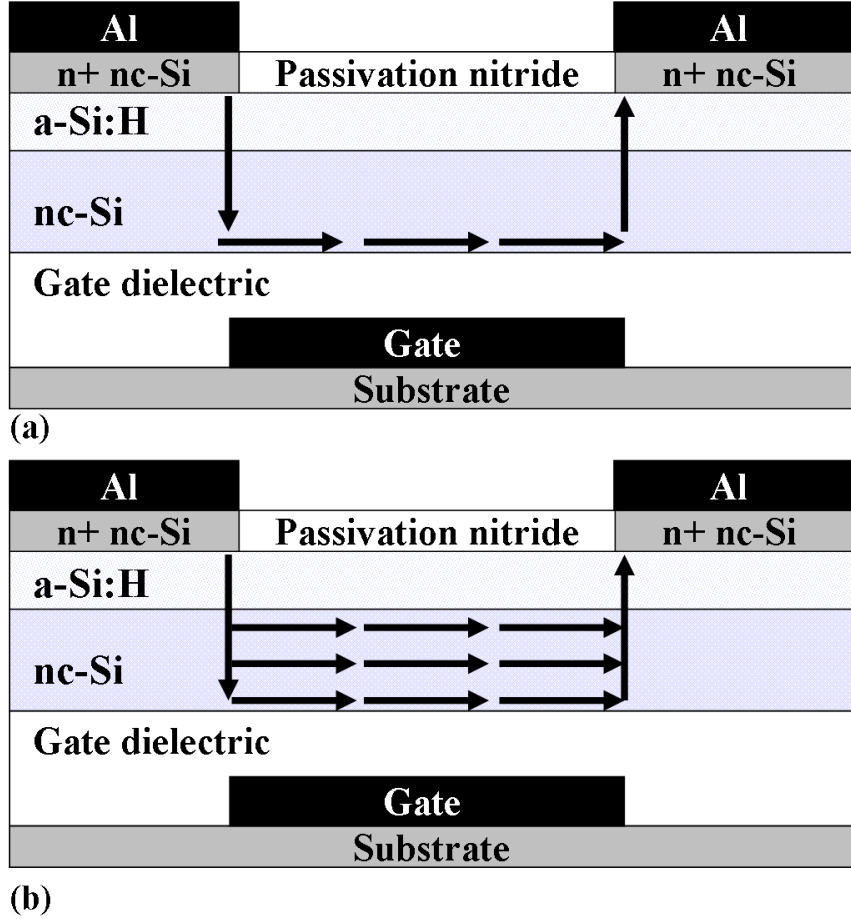
Figure 4.9: Arrows represent the tentative transistor current path, (a) in the on-state and (b) in the off-state. When TFT is on, the accumulation channel is very close to the gate dielectric interface. When TFT is off, the current passes through the whole nc-Si layer.

Indeed, in Ref. [78], it has been concluded that to minimize the SCLC component and to maximize the on-current, α-Si:H layer should be as thin as possible. This is consistent with our results shown in Fig. 4.10.

On the other hand, from Fig. 4.10, we notice that the off-current is insensitive to the α-Si:H thickness. It only varies by a factor of two for thicknesses up to 200 nm. This insensitivity is justified when we compare the conductivity of nc-Si and α-Si:H layers, which are around $1\,\mu S/cm$ and $10^{-9}\,S/cm$, respectively. Because of this difference, electrons tend to flow in the nc-Si instead of the α-Si:H, as shown in
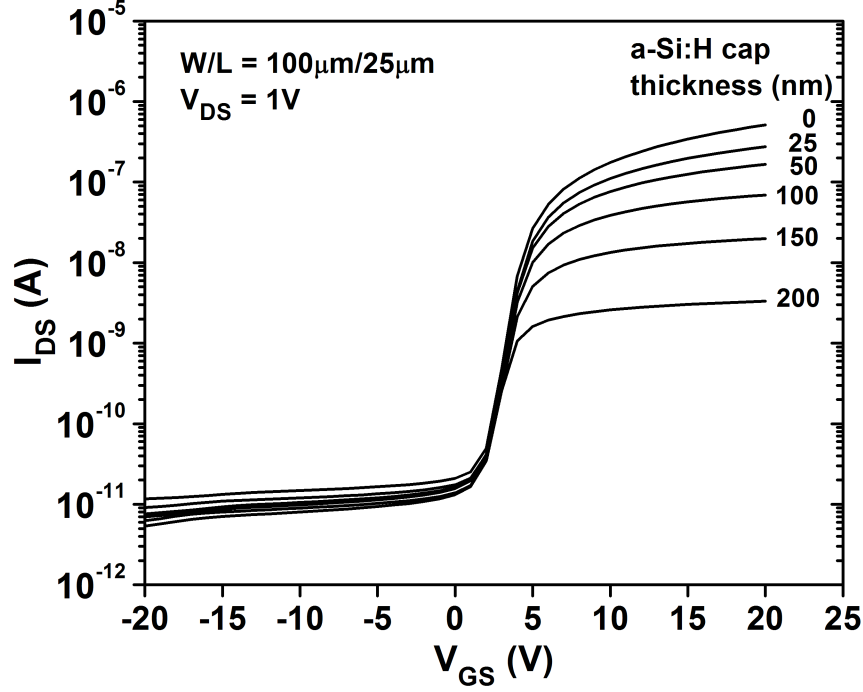
Figure 4.10: Transfer characteristics computed as a function of the α-Si:H thickness. The W/L is $100\,\mu m/25\,\mu m$ and the drain voltage is 1 V. The nc-Si layer is 65 nm thick.

Fig. 4.9 (b). The current path shown here was indeed obtained from simulations, where observed that majority of carriers flow vertically through the α-Si:H layer (beneath the source/drain regions) and then laterally through the nc-Si. However, this observation partially explains why I_{OFF} is independent of α-Si:H thickness. Because carriers have to pass through the α-Si:H when they are moving vertically and, thus, I_{OFF} should be affected. To explain this, we model this part of TFT as a resistor, as we can use the Ohm's law in this case in contrast to the case of on-state. Figure 4.11 illustrates the concept. Here, l is the thickness of the α-Si:H cap and t is the width of the vertical current path. Therefore, the resistance caused by this part is

$$R = \rho l / W t, \qquad (4.4)$$

where ρ is the resistivity of the α-Si:H and W is the width of the TFT. In simula-
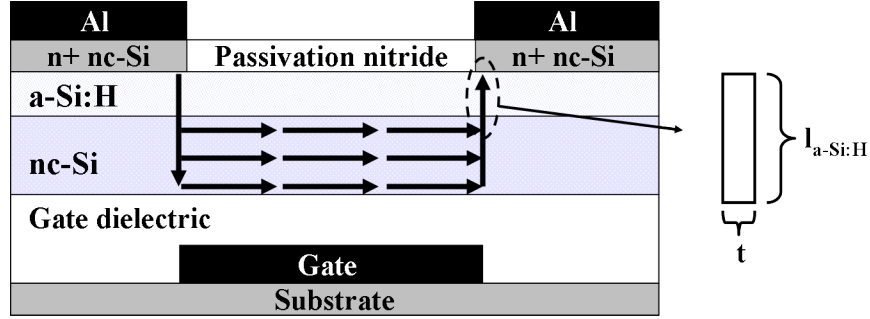
Figure 4.11: Modeling the α-Si:H cap as a resistor when TFT is in the off-state. Here, $l_{\alpha-Si:H}$ is the thickness of the α-Si:H cap and t is the thickness of the vertical current path.

tions, we saw that t is variable, i.e. it increases with the α-Si:H thickness. In other words, carriers adjust their path to experience a minimum resistance. Therefore, the effective resistance due to this part is nearly constant. This justifies the I_{OFF} behavior observed in Fig. 4.10.

Figure 4.12 shows the same concept of I_{OFF} path from slightly different view. It shows the simulated current density across the channel layer as a function of distance from the passivation nitride, where $V_{GS} = 0\,V$ and $V_{DS} = 1\,V$. As seen, current density peaks in the middle of the nc-Si layer and its value is much larger than that in the α-Si:H cap, which carries a negligible current. Thus, I_{OFF} is virtually independent of the α-Si:H thickness.

However, we are looking for to further reduce the I_{OFF}, as the value obtained in TFT B (Fig. 4.2) is still not acceptable. Therefore, we have to focus on the nc-Si layer and its attributes for obtaining a minimum possible I_{OFF}. Referring to Figs. 4.9 and 4.11, we can also consider the nc-Si as a resistor and we should increase it for a lower off-current. From (4.4), we find that in this case the best parameter to vary is ρ, the resistivity of the nc-Si layer. Indeed, there is no flexibility to vary others, because in this case, they are TFT dimensions such as length and width. Thus, we must reduce the conductivity of the nc-Si layer, which is well-known to be thickness dependent, i.e. it decreases at lower thicknesses [18]. The conductivity of a 15 nm thick nc-Si deposited in our PECVD system is around $10^{-8}\,S/cm$, which
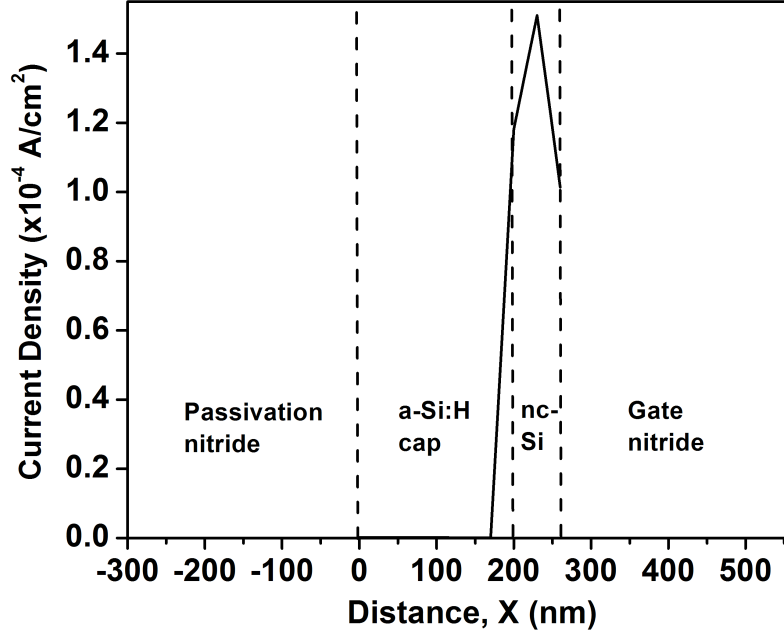
Figure 4.12: Current density computed as a function of distance from the passivation nitride, for a gate voltage of zero and a drain voltage of 1 V.

should result in a lower off-current compared to that in TFT B with the 65 nm thick nc-Si with higher conductivity of $\approx 10^{-6}\,S/cm$.

Figure 4.13 shows experimental I-V characteristics of a TFT with 15 nm nc-Si and 35 nm α-Si:H cap layer, designed by taking into account the conclusions we have drawn thus far. As expected, the off-current decreases further due to the decreased conductivity of the nc-Si. For example, in this case, I_{OFF} is $(2-3) \times 10^{-13}\,A$ at $V_{DS} = 10\,V$, while it is about $10^{-10}A$ in TFT B with the 65 nm thick nc-Si layer with higher conductivity of $\approx 10^{-6}\,S/cm$. This level of off-current is acceptable for targeted applications, including OLED displays and x-ray imagers. On the other hand, the on-current at $V_{DS} = 10\,V$ and $V_{GS} = 25\,V$ is about $10\,\mu A$ in this case (Fig. 4.13) with a 35 nm α-Si:H cap, while it is $3\,\mu A$ in TFT B (Fig. 4.2) with a 100 nm α-Si:H cap, which is consistent with our arguments and simulation results.

In the following discussions, we refer to the TFT whose I-V is shown in Fig. 4.13

Figure 4.13: (a) Transfer and (b) output characteristics of TFT1. The aspect ratio is $100\,\mu m/25\,\mu m$. The gate dielectric [N]/[Si] is 1.3.

as the optimum TFT and we call it TFT1. In TFT1, the channel layer consists of 15 nm nc-Si capped with 35 nm α-Si:H. This nc-Si/α-Si:H bi-layer structure allowed us to obtain very low off-current, which is required for both OLED display and x-ray imaging applications. At the same time, since the electron accumulation channel is only around 10 nm thick in the on state, the 15 nm thick nc-Si is enough so that the accumulation channel is formed within the nc-Si layer with high crystallinity and, hence, yielding electrical stability. In the next section, we present and discuss the performance characteristics of two TFTs with the same channel layer as that of TFT1, but different compositions of the nitride gate dielectric.

4.6   Optimum Structure with Different Nitride Compositions

The field-effect mobility (μ_{FE}), threshold voltage (V_T), and the shift in threshold voltage (ΔV_T) of bottom-gate TFTs is highly dependent on the quality of the α-SiNx:H gate dielectric, i.e. its [N]/[Si]. For example, in α-Si:H TFTs, it has been observed that the μ_{FE} and ΔV_T deteriorate by decreasing the [N]/[Si] ratio, i.e. by moving from a nitrogen(N)-rich to a silicon(Si)-rich gate dielectric [69]. For bottom-gate nc-Si TFTs, there was no such a report, which was the motivation for performing this part of research.

Referring to Table 3.3, we characterized three nitride layers with [N]/[Si] of 1.3, 1.2, and 1, which were processed at NH_3 / SiH_4 flow ratio of 20, 10, and 5, respectively. The first nitride layer, with the [N]/[Si] of 1.3, was used in TFT1. We also used the latter two as the gate dielectric for two additional TFTs, labeled TFT2 and TFT3. Hence, the structures of TFT1, TFT2, and TFT3 are essentially the same, i.e. their channel layer comprises of 15 nm thick nc-Si capped with 35 nm thick α-Si:H. Their sole difference is their gate dielectric stoichiometry with [N]/[Si] of 1.3, 1.2, and 1, respectively. In this section, we relate their μ_{FE} and V_T to their gate dielectric composition. In the next chapter, we discuss their stability

under different operating conditions.

Transfer and output characteristics of TFT2 and TFT3 are depicted in Figs. 4.14 and 4.15, respectively. Their aspect ratio (W/L) is $100\,\mu m/25\,\mu m$. Table 4.2 summarizes the extracted parameters from I-V characteristics, along with information on nitride dielectrics. As seen, in going from an N-rich to a Si-rich gate dielectric, the μ_{FE} decreases from $0.75\,cm^2/Vs$ (TFT1) to $0.2\,cm^2/Vs$ (TFT3). Ideally, the μ_{FE} should be independent of gate dielectric and is only determined by the dispersive motion of electrons in the band tail states of the nc-Si channel layer and its associated free and trapping times [11]. Here, we recall that band tail states frequently trap and release conduction carriers, which effectively decreases their mobility. A simple one-dimensional model was shown in Fig. 2.4 [11]. Hence, the μ_{FE} should be a function of channel layer quality and its density of band tail states. But it is well-known that α-Si:H TFTs with different nitride compositions yield different μ_{FE}, despite an identical channel layer [69], suggesting that μ_{FE} is also affected by the gate dielectric. It is believed that the N-rich α-SiNx:H produces a cleaner, more abrupt interface with the channel layer [69]. Here, we also observed similar behavior for μ_{FE} in our nc-Si TFTs with the different nitride compositions. Another contributing factor can be extra charge trapping at the nitride/nc-Si interface that is caused by the Si-rich nitride, similar to what we saw in the C-V characteristics in Fig. 3.10.

Comparing the threshold voltage values for the three TFTs, V_T becomes negative as we move to Si-rich nitride (TFT3), as shown in Table 4.2. The V_T is determined by the density of bulk traps (N_T) in the channel layer, in which the higher the N_T the higher the V_T [10] according to eqn. (2.2). Values of N_T in the nc-Si layer were calculated from formula (4.3). As expected, V_T decreases from 4 to 3.3 V when N_T decreases from $1.2\times10^{18}\,cm^{-3}eV^{-1}$ in TFT1 to $8\times10^{17}\,cm^{-3}eV^{-1}$ in TFT2. For TFT3, we expect a higher V_T ($\geq 4\,V$) as its N_T is considerably larger than that of TFT1. However, V_T of TFT3 is negative. Studies have reported that V_T is also influenced by the presence of fixed charges in the gate dielectric, where
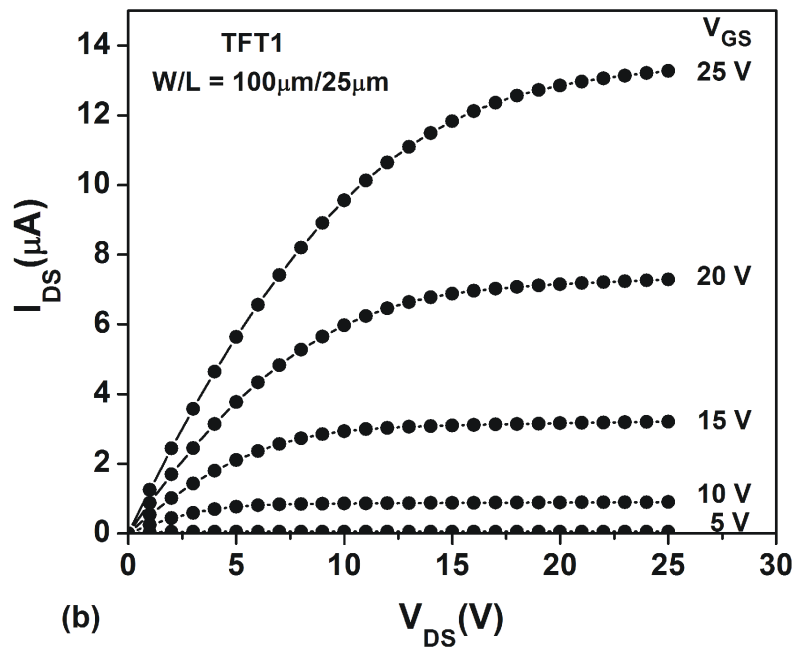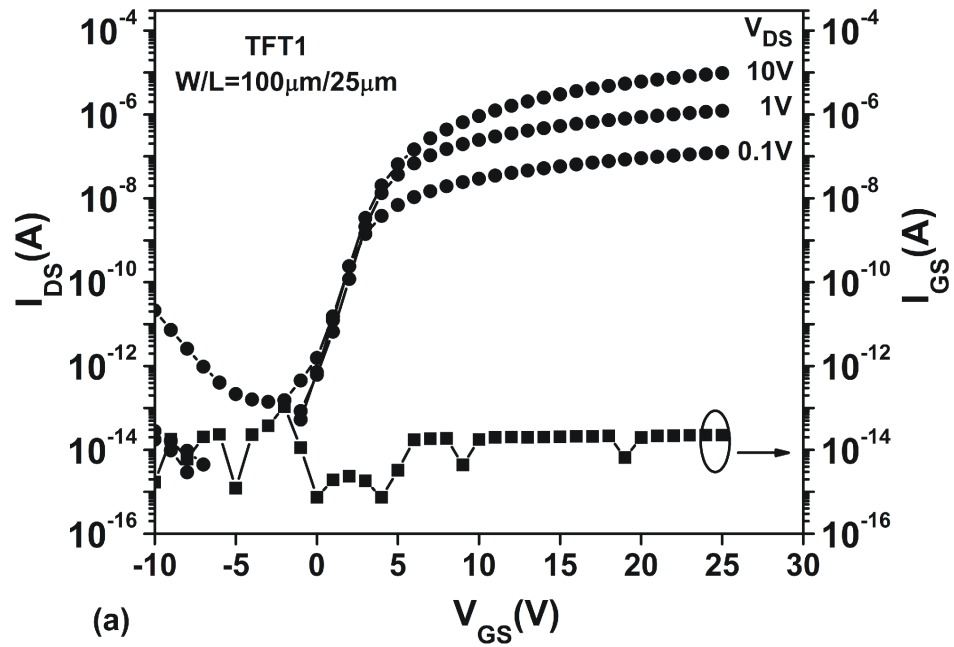
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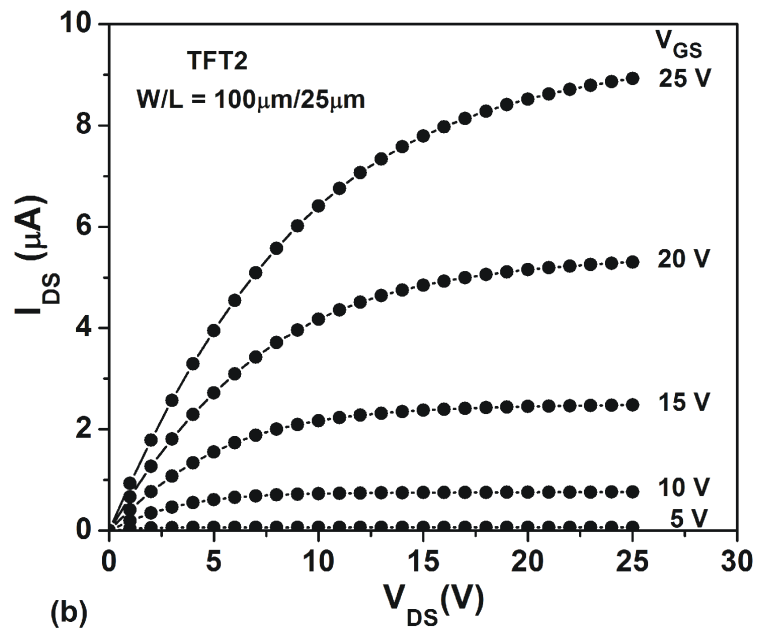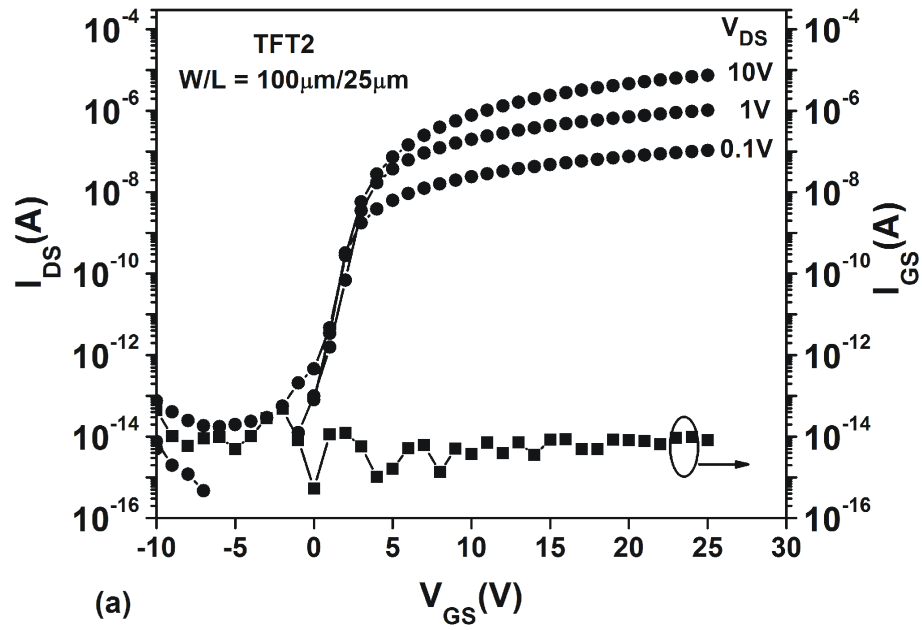
Figure 4.14: (a) Transfer and (b) output characteristics of TFT2. The aspect ratio is $100\,\mu m/25\,\mu m$. The gate dielectric [N]/[Si] is 1.2.
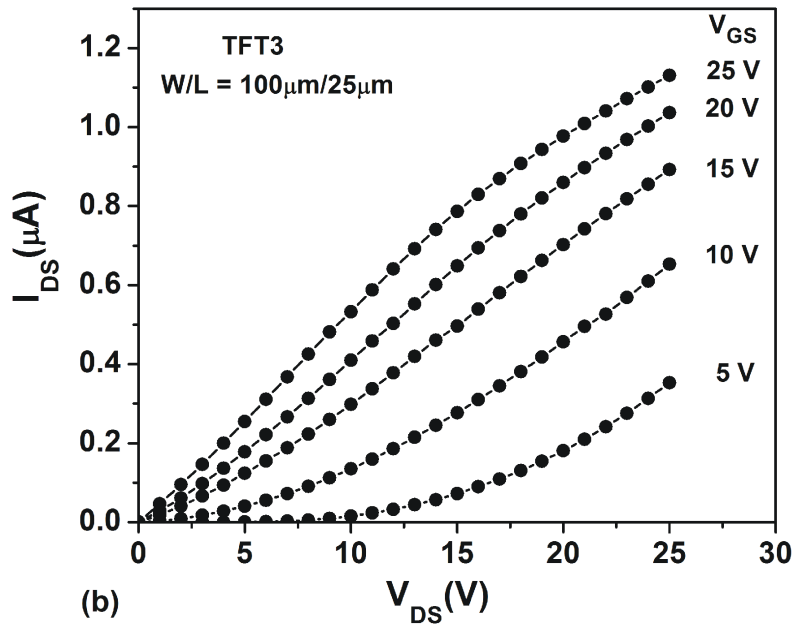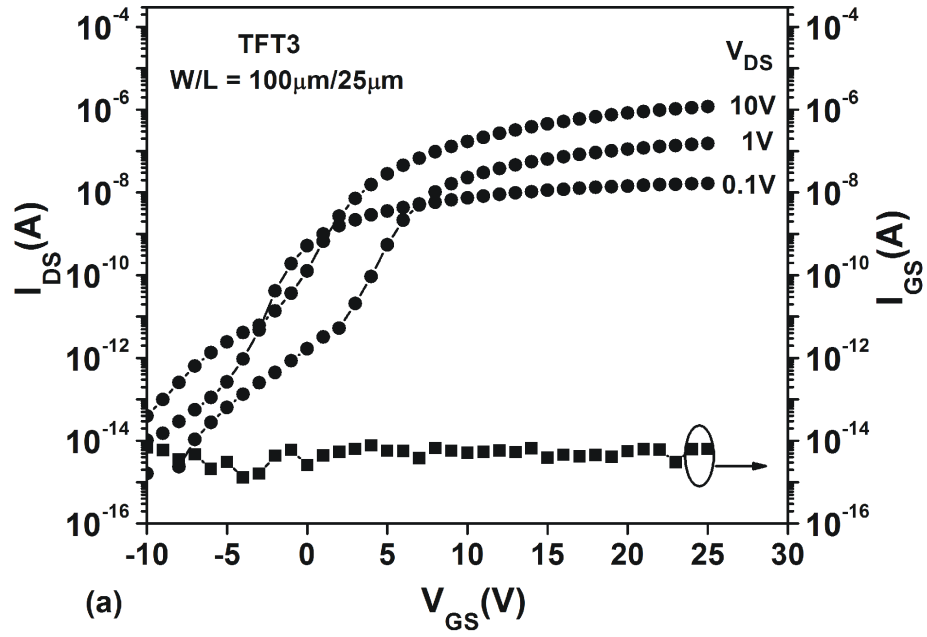
Figure 4.15: (a) Transfer and (b) output characteristics of TFT3. The aspect ratio is $100\,\mu m/25\,\mu m$. The gate dielectric [N]/[Si] is 1.

Table 4.2: Summary of performance parameters of the three TFTs. The SS is the subthreshold slope and the ON/OFF is the ratio of on- and off-currents, defined at gate voltages of +20 V and -5V, respectively.

Parameter	TFT1	TFT2	TFT3
NH_3 / SiH_4	20	10	5
$Nitride\,[N]/[Si]$	1.3	1.2	1
$\mu_{FE}\,(cm^2/Vs)$	0.75 ± 0.05	0.45 ± 0.05	0.2 ± 0.05
$V_T\,(V)$	4 ± 0.3	3.3 ± 0.3	-2 ± 0.5
$SS\,(V/dec)$	0.9 ± 0.1	0.6 ± 0.1	1.9 ± 0.1
$D_{it}\,(cm^{-2}eV^{-1})$	$(1.9 \pm 0.2) \times 10^{12}$	$(1.2 \pm 0.2) \times 10^{12}$	$(3.6 \pm 0.2) \times 10^{12}$
$N_T\,(cm^{-3}eV^{-1})$	$(1.2 \pm 0.2) \times 10^{18}$	$(7 \pm 0.2) \times 10^{17}$	$(2.4 \pm 0.2) \times 10^{18}$
ON/OFF	10^8	$(3-4) \times 10^8$	$10^6 - 10^7$

these fixed charges lead to a parallel shift in the transfer characteristics [69]. Indeed, this is in line with the arguments we gave on Fig. 4.4, and simply shows that in TFT3 the density of fixed charges in the gate dielectric is higher than that in the other two TFTs. Therefore, a Si-rich nitride may contain more fixed charges than an N-rich nitride.

A good quality TFT is typically characterized by drain currents that are independent of the drain voltage in subthreshold such as Fig. 4.13 (a), and saturation of the drain current at high drain voltages such as Fig. 4.13 (b). This behavior is seen in TFT1 and TFT2, as depicted in their respective transfer and output characteristics in Figs. 4.13 and 4.14. However, I-V curves of TFT3 are distinctively different. Here we see that its subthreshold current is strongly dependent on the drain voltage, Fig. 4.15 (a), and its output characteristics, Fig. 4.15 (b), do not saturate. We attribute this to the screening effect of the gate electric field by trapped charges in the low-quality Si-rich α-SiNx:H. The density of charge (Q) induced in the nc-Si channel by a V_{GS} in the range $5-25\,V$ is around $(1-5) \times 10^{12}\,cm^{-2}$ calculated from $Q = C_{gate}V_{GS}/q$, where C_{gate} and q are the gate dielectric capacitance and electron charge, respectively. To screen the gate electric field, the trapped charge density

in the gate dielectric should be comparable to that induced in the channel by the gate voltage. From the C-V characteristics shown in Fig. 3.10 (c), the hysteresis is $\approx 25\,V$. Hence the trapped charge density is calculated as $\approx 5 \times 10^{12}\,cm^{-2}$, which compares well with the induced channel charge density. This suggests that trapped charges can adversely affect the gate field and its control on device operation.

Therefore, it is seen that performance characteristics of TFT3 with the Si-rich nitride deviate from normal TFT behavior. Low mobility, abnormal threshold voltage, and abnormal transfer and output characteristics were produced by the nitride composition [N]/[Si] of 1. On the other hand, the nitrides with higher [N]/[Si] of 1.2 and 1.3 produced devices with normal I-V characteristics.

4.7 Summary

The off-current in bottom-gate nc-Si TFTs was shown to be determined by the conductivity of the channel layer and by the quality of the silicon/passivation nitride interface. In single-layer TFT structures such as TFT A, when the passivation nitride interface is with nc-Si, charge accumulation near that interface, due to the presence of fixed charges, leads to increased off-current. In contrast, when the nc-Si layer is capped with α-Si:H such as TFT B, the off-current decreases and is determined by the bulk conductivity of nc-Si, as the α-Si:H makes a less defective interface with the passivation nitride. The experimental results showed that off-current in TFT A is about two orders of magnitude larger than that in TFT B, under identical biasing conditions, which was shown to be due to an extra band bending at the nc-Si/passivation nitride interface in TFT A. Therefore, the preferred device structure should comprise of a nc-Si/α-Si:H bi-layer like TFT B.

In addition, we performed numerical simulations in order to optimize the nc-Si/α-Si:H bi-layer. The simulation results showed that the off-current is insensitive to the α-Si:H thickness, while on-current decreases at higher α-Si:H thicknesses. Therefore, from an on-current standpoint a thinner α-Si:H cap is desired. On the

other hand, to further reduce the I_{OFF}, we had to redesign the nc-Si layer by considering that its conductivity is thickness dependent, i.e. decreases at lower thicknesses. By employing 15 nm nc-Si and 35 nm α-Si:H cap, we were able to obtain off-currents as low as $10^{-13}\,A$, and to maintain on-currents as high as $10\,\mu A$. This level of off-current is now acceptable for applications such as OLED displays and x-ray imagers. The results presented here contrast with previous claims that the I_{OFF} in nc-Si TFTs is due to the band-to-band tunneling, which is suppressed by the α-Si:H cap due to its larger bandgap [43].

We also studied TFTs with various compositions of α-SiNx:H gate dielectric. We varied the composition of the nitride ([N]/[Si]) from 1.3 to 1, by adjusting the PECVD variable, the NH_3/SiH_4 gas flow ratio. TFTs with a nitrogen-rich nitride ([N]/[Si]=1.3) yielded higher on-current and field-effect mobility than the devices with silicon-rich gate dielectric ([N]/[Si]=1). For example, mobility dropped from $0.75\,cm^2/Vs$ to $0.2\,cm^2/Vs$ when the [N]/[Si] changed from 1.3 to 1. The corresponding threshold voltages were 4 and -2 V, respectively. From the standpoint of I-V characteristics, it was observed that the I_{DS} of the TFT3, with silicon-rich gate dielectric, was highly dependent on the V_{DS} at the subthreshold region. In addition, the output characteristics of TFT3 was abnormal, i.e. its I_{DS} was increasing by increasing the V_{DS}, without becoming saturated. However, TFT1 and TFT2 exhibited normal behavior in their I-V curves, i.e. yielded a drain current independent of the V_{DS} at the subthreshold and an I_{DS} saturation at high drain voltages.

Chapter 5

Stability of Nanocrystalline Silicon Thin Film Transistors

5.1   Introduction

This chapter addresses experimental results of the threshold voltage stability of the nc-Si TFTs. We compare the stability of nc-Si TFTs, fabricated in the course of this research, with that of α-Si:H TFTs that have been fabricated in our group and elsewhere. We evaluate their threshold voltage shift (ΔV_T) under similar biasing conditions and use the attributes of instability mechanisms, reviewed in chapter two, to justify the experimental results. For example, we analyze the experimental data of ΔV_T obtained when we electrically stressed the TFTs under constant drain currents at two temperatures. Here, our goal is to investigate the temperature dependence of ΔV_T as, in chapter two, we mentioned that defect state creation is highly temperature-activated. Thus, by stressing the TFTs at different temperatures, we obtain a better insight into the instability mechanism underlying our observations.

We have also investigated the other attribute of the instability mechanisms, i.e. their reversibility. It is known that charge trapping is reversible, but defect creation is indefinitely stable and irreversible at room temperature. We have performed the

relaxation test, in which a nc-Si TFT was electrically stressed for some time to induce some shift in its threshold voltage. Subsequently, the TFT was relaxed, i.e. bias voltages were removed and device was turned off, and TFT I-V curves were retrieved from time to time to see whether the induced ΔV_T was disappeared. We evaluate our observation from the standpoint of the kinetics of the defect annealing by hydrogen diffusion, given by eqn. (2.9) and discussed in chapter two. We also present the ΔV_T data obtained when TFTs were subject to DC gate voltages in both linear and saturation regimes.

5.2 Results and Discussion

5.2.1 Threshold Voltage Shift under Constant Current Stress

Electrically stressing the TFTs at different temperatures and evaluating the behavior of the shift in the threshold voltage should provide significant insight into the instability mechanisms, as we noted that defect state creation is highly temperature-activated. In this section, we discuss our observations of the temperature dependency of ΔV_T of our nc-Si TFTs. For comparison, we also bring the results of similar experiments that have been performed on α-Si:H TFTs in our group [55].

The TFTs used in this study were samples of TFT1 whose performance characteristics are given in Table 4.2 and its I-V curves are shown in Fig. 4.13. Bias stress tests were performed on TFTs with an aspect ratio (W/L) of $100\mu m/25\mu m$ using an HP4145 semiconductor characterization system. The TFTs were subject to 50 hours of continuous constant drain current stress.

The diode-connected configuration, shown in Fig. 2.9, allows on-line monitoring of the gate voltage and errorless extraction of the threshold voltage shift. In this case, the change in the gate voltage is solely due to and equal to the shift in the threshold voltage [55]. According to equation (2.4), the V_{GS} must be adjusted to

maintain the I_{DS} unchanged. Because the V_T increases due to the current stress and hence V_{GS} should be increased by the same amount, which is done automatically by the semiconductor analyzer. Here, we note that the other variable could be μ_{FE}, but it has been shown that it barely changes under the bias stress [55, 79].

Figures 5.1 (a) and (b) show ΔV_T for 2, 10, and 15 μA stress currents at 22 and 75 °C, respectively. The previously reported data on α-Si:H TFTs are also presented [55]. Here, two fundamental differences are noticeable. First, ΔV_T of the nc-Si TFT saturates at prolonged stress times, but that of α-Si:H does not. Second, ΔV_T is weakly temperature dependent, in contrast to that of the α-Si:H counterpart. For example, after 50 hours stressing at 15 μA, ΔV_T of the nc-Si TFT is 3 V and 4 V at 22 and 75 °C, respectively, while that for the α-Si:H TFT is 7.6 V and 21 V, respectively, suggesting a notable difference in the underlying instability mechanisms between α-Si:H and nc-Si TFTs. Here, we note that the initial V_T of both devices are comparable, 4 V for nc-Si and 2.6 V for α-Si:H, and the initial applied gate voltages are also comparable and less than 25 V [55].

In this range of stress voltages, the instability of α-Si:H TFTs is commonly attributed to defect state creation in the channel [55, 79]. Since the band tail carrier density (n_{BT}) remains unchanged during constant current stress, V_T of α-Si:H TFT may increase indefinitely, till the gate voltage hits the supply voltage or the density of weak bonds (N_{WB}) becomes a rate limiting factor [55]. At higher stress voltages, however, defect state creation in α-Si:H TFTs was no longer dominant [45]. In this case, Powell et al. argued that ΔV_T is governed by charge injection from channel into the gate dielectric interface without subsequent redistribution in the bulk of nitride, and this to be temperature independent process [79]. Libsch and Kanicki also reasoned that trapped carriers first thermalize in a broad distribution of band tail states at the channel/α-SiNx:H interface, and then move to deeper energies inside the α-SiNx:H at longer stress times, higher temperatures, and larger electric fields [52]. However, the measured ΔV_T was highly temperature-dependent [52]. Our measurement results are in favor of the first argument as ΔV_T is only weakly

Table 5.1: Parameter values for equation (2.6) resulting from fit to measured data indicated in Figs. 5.1 (a) and (b).

$Temperature\,(°C)$	$Stress\,Current\,(\mu A)$	$C(V)$	β	$\tau\,(hr)$
22	2	5	0.25±0.01	10000±2549
22	10	10	0.2018±0.001	32422±1894
22	15	14	0.187±0.001	42730±2496
75	2	5	0.268±0.0098	3791±701
75	10	10	0.2374±0.006	3262±446
75	15	12	0.247±0.009	2099±345

temperature-dependent, and consistent with the results reported by Powell et al [79].

To gain quantitative insight, we considered the stretched-exponential model, i.e. equation (2.6), for the charge trapping kinetics in α-Si:H TFTs. Calculations using (2.6) are shown by solid lines in Figs. 5.1 (a) and (b). As seen, the stretched-exponential time dependence corroborates well with the measurement data. Values of the extracted parameters are given in Table 5.1. The parameter C was set to $(2/3)(V_{GS} - V_T)$ in our calculations, as opposed to $(V_{GS} - V_T)$ in Ref. [52]. Here, the difference lies in the device operation regime, which is saturation in our case and linear in the latter. Indeed, ΔV_T appears to follow the channel charge concentration, which at pinch-off ($V_{DS} = V_{GS} - V_T$) is nearly 2/3 that in linear, i.e. $V_{DS} = 0$ [54]. This relationship is nearly valid although $V_{DS} = V_{GS}$ in this series of experiments.

When the temperature increases from 22 to 75 °C, the parameter τ changes in the range $10^8 - 10^7$ sec in nc-Si TFTs and $10^8 - 10^5$ sec in α-Si:H TFTs [52]. A smaller τ leads to a larger ΔV_T for a given stress time, according to (2.6). For example, increasing the temperature reduces the τ in nc-Si TFTs by one order of magnitude, while in the case of α-Si:H, its reduction is by three orders. This implies a higher stability and longer-term reliability of nc-Si TFTs, even at high operation
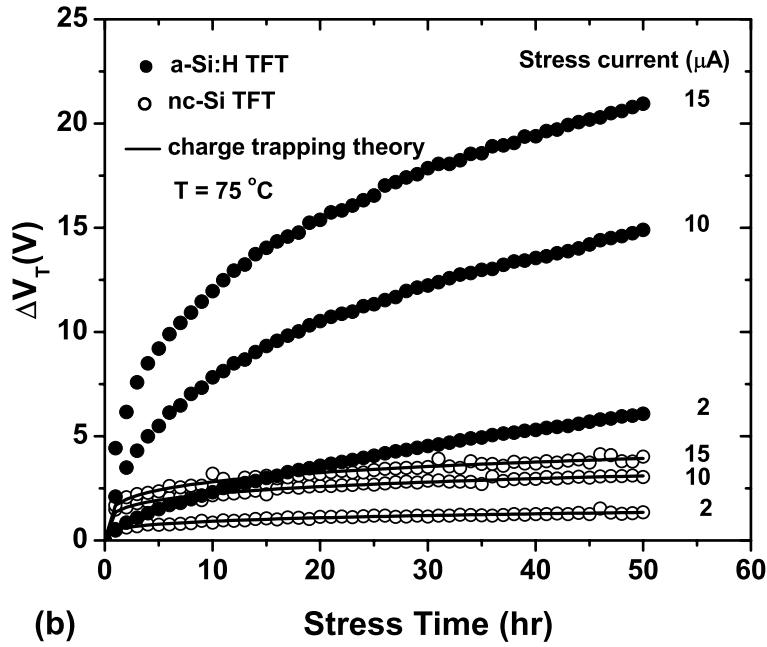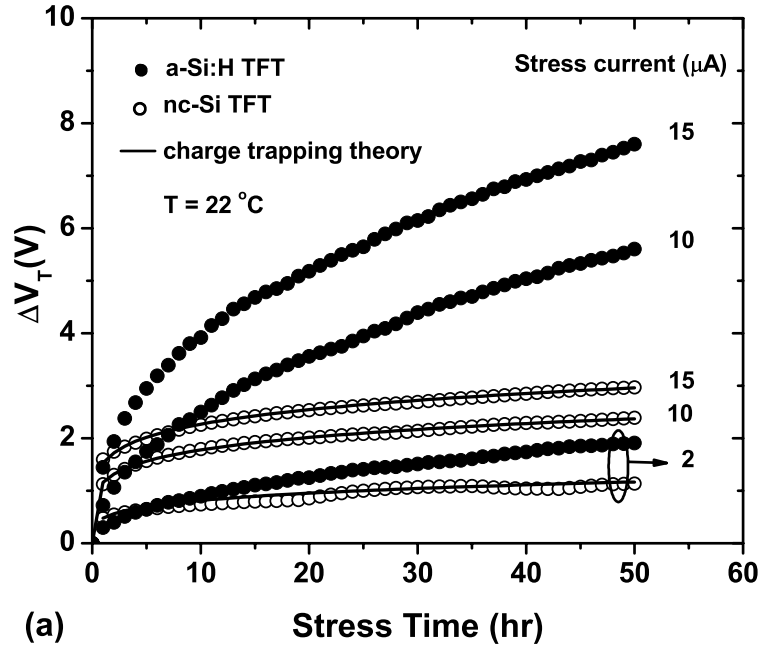
Figure 5.1: Threshold voltage shift as a function of time for different stress currents and temperatures: (a) 22 °C, and (b) 75 °C; filled circles: α-Si:H TFT, open circles: nc-Si TFT, lines: calculations using the stretched exponential equation (2.6) for charge trapping. The α-Si:H data are from Ref. [55].

temperatures. From Table 5.1, one may also find that the parameter β is fairly constant when the stress current and temperature change.

We now evaluate our data from the standpoint of the thermalization energy (E_{th}), the concept developed for α-Si:H TFTs based on the defect state creation model by Deane et al [46]. They showed that ΔV_T and E_{th} follow the relationship (2.10), and that ΔV_T plotted as a function of E_{th} for different temperatures overlay perfectly, in which the attempt-to-escape frequency (ν) is the fitting parameter [50]. In α-Si:H TFTs, ν is $10^{10}\,Hz$ as reported by several research groups [46, 47, 48], and seems to be unique to defect state creation. It is attributed to the probability that an electron attempts to break weak Si-Si bonds [46, 49]. Here, our goal is to show that our experimental data does not fit into the thermalization energy concept.

The theoretical curve is depicted in Fig. 5.2, using eqn. (2.10) and typical parameter values obtained in Ref. [50] for α-Si:H TFTs, i.e. $E_A = 1\,eV$, $k_B T_0 = 0.065\,eV$, $\epsilon = 0.5$ [50], and $C = (2/3)(V_{GS} - V_T) = (2/3)(25 - 4) = 14\,V$, assuming that TFT is operating in saturation. Our measurement data shown in Fig. 5.2 depicts a ΔV_T that is much smaller than that predicted by (2.10), and the curves associated with the different temperatures only overlay when $\nu = 0.1\,Hz$, a value that is not meaningful. Although we argue against presence of defect state creation in our nc-Si TFTs, evidence of such has been observed in nc-Si TFTs fabricated by others, but at a higher value of E_A (1.07 eV) [49]. Even with this value of E_A, the discrepancy between theoretical and experimental values of ΔV_T is high. For example, at $E_{th} = E_A$, (2.10) yields $\Delta V_T = 3C/4 = 3 \times 14/4 = 10.5\,V$, compared to a measured value of 4 V. These observations imply that defect state activation in our devices may only take place at much higher thermalization energies, i.e. at higher temperatures and/or higher stress times. It also goes to show that this process is to a large extent dependent on the growth kinetics of the nc-Si layer.

In summary, the observed behavior of ΔV_T indicates absence of defect state creation in the nc-Si TFTs. Its weak temperature dependence is consistent with the mechanism proposed by Powell et al. [45], implying that the instability mechanism
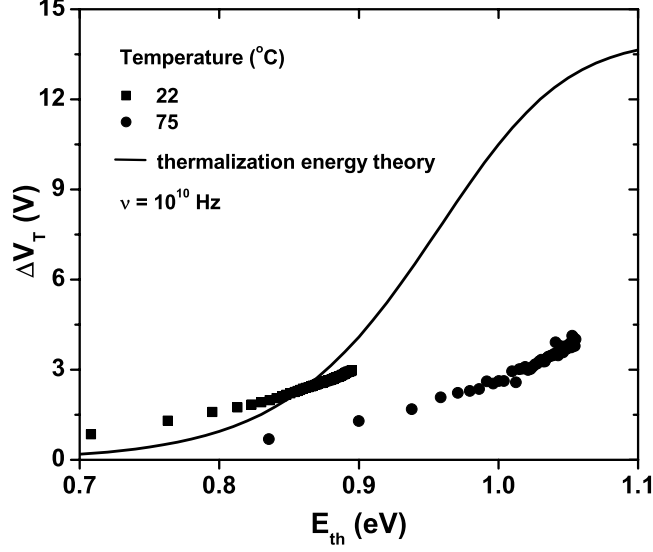
Figure 5.2: Threshold voltage shift of the nc-Si TFT at different temperatures as a function of the thermalization energy, at the stress current of $15\,\mu A$. The solid line denotes theoretical values calculated using equation (2.10).

is charge trapping in the nitride. On the other hand, the kinetics of ΔV_T follows the stretched-exponential dependence predicted for charge trapping [52]. In contrast to the α-Si:H TFT, where its ΔV_T does not saturate over time, that of the nc-Si TFT saturates under constant current stress. Finally, ΔV_T in the nc-Si TFTs does not fit into the thermalization energy concept developed for α-Si:H TFT based on the defect state creation model.

All the observations in this section are pointing to the conclusion that the instability mechanism is charge trapping whereas defect state creation is absent. To further support this conclusion, in the next section, we investigate the other attribute of the charge trapping, i.e. its reversibility. Earlier, we mentioned that charge trapping is reversible, but defect creation is indefinitely stable and irreversible at room temperature.

5.2.2 Relaxation of Threshold Voltage Shift

The way to explore the reversibility of instability mechanisms is called relaxation. In this method, a TFT is electrically stressed for some time to induce some shift in its threshold voltage. Subsequently, the TFT is relaxed, meaning that bias voltages are removed and device is turned off. From time to time, a quick test is done to retrieve its I-V curves to see whether the induced ΔV_T is disappeared and initial I-V curves are obtained.

TFTs used in this study were samples of TFT1. Fig. 5.3 shows its transfer characteristics in three different states: (1) unstressed or initial, (2) gate bias stressed for 5 hours at 25 V, and (3) relaxed for 5 days at room temperature following gate bias removal. Here, we see that after 5 hours of gate bias stress, ΔV_T is around 1.4 V, and the transfer characteristic returns to its unstressed state after 5 days relaxation at room temperature. There are two possible mechanisms underlying this relaxation behavior. First, defect states are created in the channel during the stressing period, and are subsequently annealed during relaxation due to hydrogen motion and diffusion in the channel. Alternatively, charges that are trapped in the gate dielectric are released into the channel, and the initial characteristic is retrieved.

The feasibility of the first mechanism can be evaluated based on the kinetics of defect annealing and structural relaxation developed for α-Si:H. The structural relaxation kinetics and metastability in α-Si:H are closely related to the hydrogen diffusion rate. Hydrogen motion is the key mechanism by which thermal equilibrium takes place [11]. The time dependence of structural relaxation and defect annealing was given by (2.7) and (2.9). At room temperature, which we have performed the relaxation experiments, $\beta = 0.45$ and $\tau_0 = 2 \times 10^{-10}\ sec$. The E_A was also given as 0.95 eV [80]. From (2.7) and (2.9), $N = 0.74 N_{T0}$ after 5 days relaxation at room temperature. This means that within this period, only about 26% of generated defects are annealed and, thus, the induced ΔV_T may recover by the same amount. On the other hand, to anneal 90% of generated defects and achieve more or less
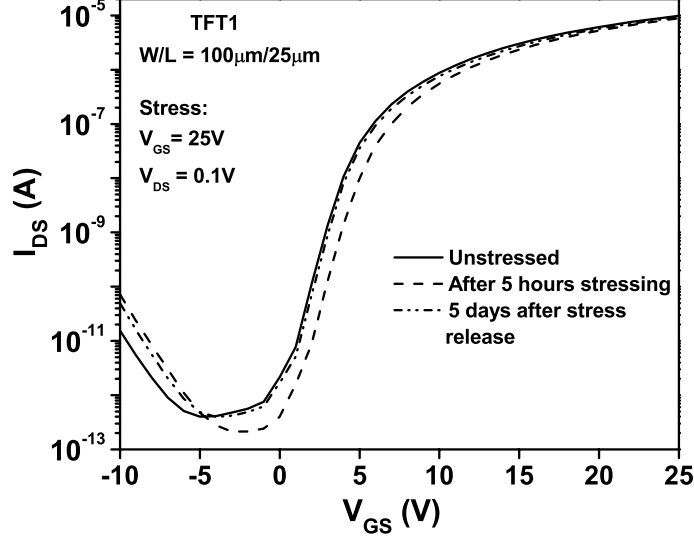
Figure 5.3: Transfer characteristics of TFT1 in three different states: unstressed, stressed for 5 hours at 25 V gate bias, and 5 days after stress release at room temperature. The recovery of the drain current is not consistent with the defect creation and annealing model. It shows that charge trapping is the instability mechanism.

the initial I-V curves, the required time is nearly 3.8×10^7 sec, or 442 days, which is in agreement with the one year estimate given in Ref. [11]. Thus, defect states in the channel are stable at room temperature and can only be removed by annealing above 150 °C for several hours [11].

Therefore, we observe that the induced ΔV_T in our nc-Si TFT is reversible at room temperature and requires much shorter time as predicted by the defect annealing model. This is another evidence that supports the conclusion that the defect creation has been eliminated in our device.

We can also perform another experiment, which is similar to the relaxation with a minor change. Once, we stress the device by a positive gate bias and induce some ΔV_T, we can then subject the TFT to a negative gate bias instead of relaxing it without any applied bias. Earlier, it was reasoned that, under a positive gate bias, trapped charges occupy the energy levels close to the nitride Fermi level which is below the Fermi level of the channel layer. However, once the gate bias is removed,
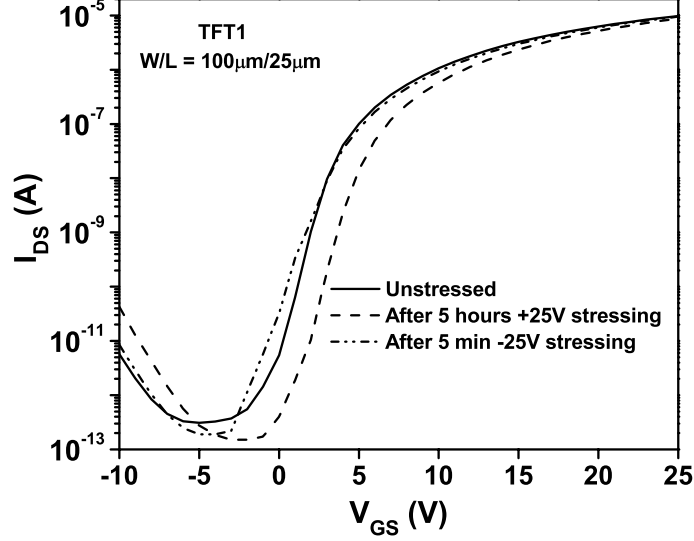
Figure 5.4: Transfer characteristics of TFT1 in three different states: unstressed, stressed for 5 hours at +25 V gate bias, and subsequently biased at -25 V gate voltage for 5 minutes. The fast recovery of drain current is consistent with charge trapping and detrapping mechanisms.

the energy of trapped charges lies above the Fermi level in the channel layer. This energy difference, let us call it E_{TF}, favors detrapping and back-tunneling of charges back into the channel layer. Thus, applying a negative gate voltage, after positive bias stressing, should expedite the recovery process as the energy difference E_{TF} is larger and hence back-tunneling process would be faster.

We tested this idea, where the TFT was subject to +25 V gate bias stress for 5 hours, followed by a -25 V bias for 5 minutes. The retrieved transfer characteristics after stressing and after the negative bias test are shown in Fig. 5.4. As seen, a 5 minute negative gate voltage more or less reproduces the full recovery of the on-current, albeit with a slight change in the subthreshold slope. Overall, we conclude that the observed behavior of threshold voltage shift is due to the charge trapping in and detrapping from the nitride dielectric, which is a fast and reversible process.

5.2.3 Threshold Voltage Shift under Constant Voltage Stress

Threshold Voltage Shift with Variable Nitride Composition

The effect of gate bias stress on V_T stability was evaluated by subjecting the TFTs, labeled as TFT1, TFT2, and TFT3, to DC gate voltages of 15 and 25 V. The drain-source voltage (V_{DS}) was set to 0.1 V to maintain the TFT in the linear operation regime, in which the ΔV_T has been observed to be more profound [54]. The total stress time was 5 hours and the stress test was briefly interrupted three times (after 1 hour, 3 hours, and 5 hours) to retrieve the transfer characteristics. The obtained results are shown in Fig. 5.5. As seen, after 5 hours of stressing at 15 V, the ΔV_T is 0.3 V, 1 V, and 12.4 V for TFT1, TFT2, and TFT3, respectively. The same trend is observed for the 25 V stress voltage. Therefore, we see that device stability is highly dependent on the nitride composition, as reported for α-Si:H TFTs by others [70]. TFT1 with a nitride composition [N]/[Si] of 1.3 exhibits the best stability, with a 0.3 V shift in V_T at a gate voltage of 15 V. However, TFT3 with a Si-rich dielectric ([N]/[Si] of 1) shows a 12.4 V shift at a gate voltage of 15 V.

Interestingly, the trend of the ΔV_T as a function of the nitride composition is similar to what we observed for the hysteresis of the C-V characteristics of the MIS structures in Fig. 3.10. In MIS structures, the defect creation is absent, since we have used the crystalline silicon as the substrate. Consequently, we attributed the hysteresis of the C-V curves to the charge injection into the nitride gate dielectric. The shifts in V_T of TFTs 1-3 can also be explained by the charge trapping in the nitride gate dielectric, as we have shown that the defect creation is absent in our nc-Si TFTs. Indeed, charge injection can occur even at low applied gate voltages in the range 15-25 V that we have applied. For example, among the injection mechanisms shown in Fig. 2.8, mechanisms 4 (constant-energy tunneling from silicon conduction band) and 5 (tunneling from conduction band into traps close to E_F) may occur at low gate voltages [45, 51]. The availability of large concentration of charge trapping
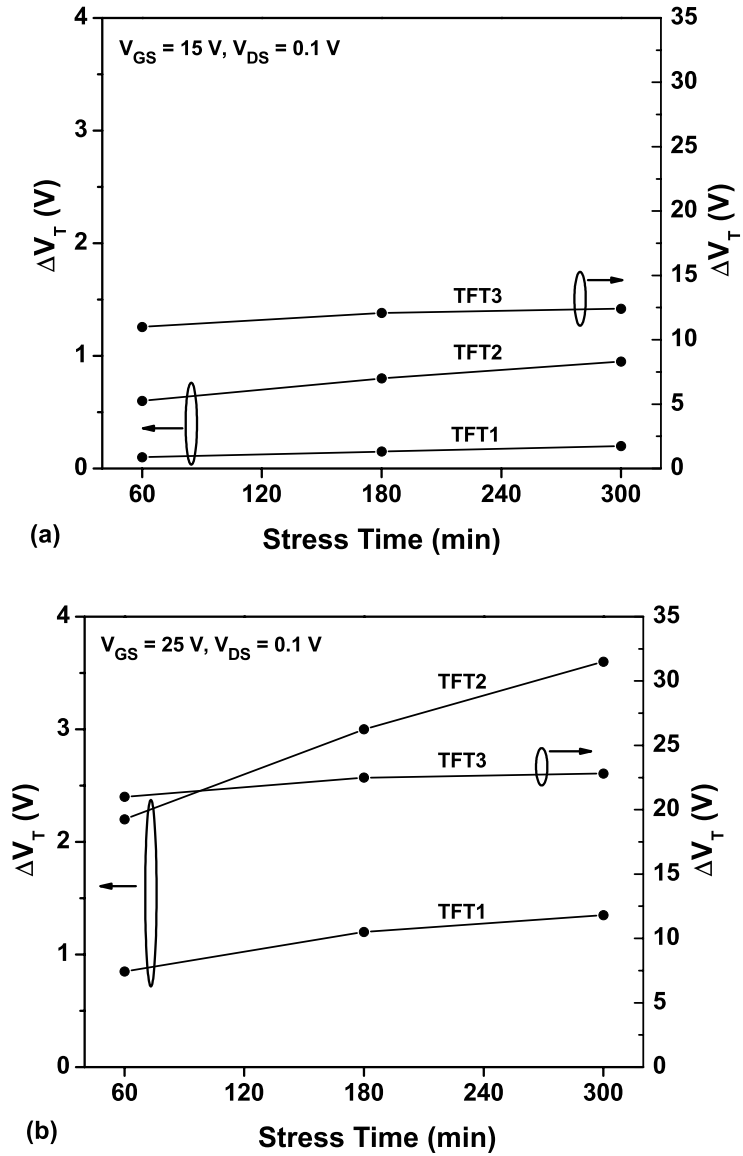
Figure 5.5: Threshold voltage shift as a function of stress time for a gate voltage of (a) 15 V, and (b) 25 V in the linear regime.
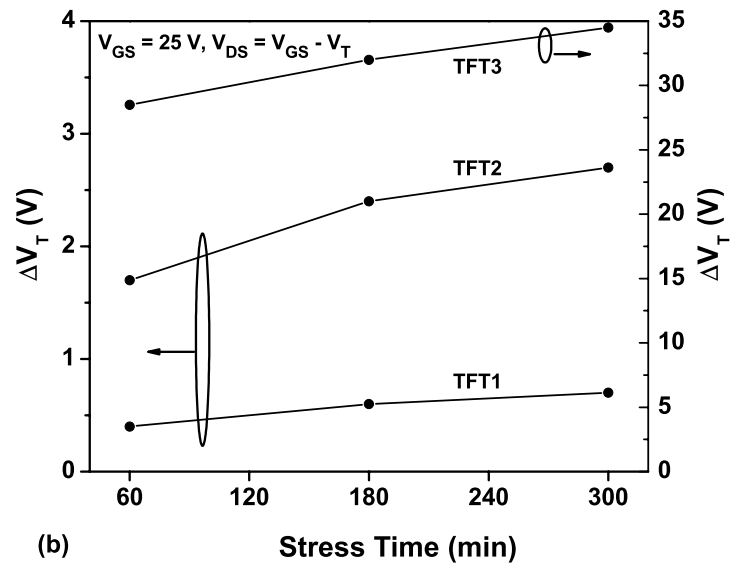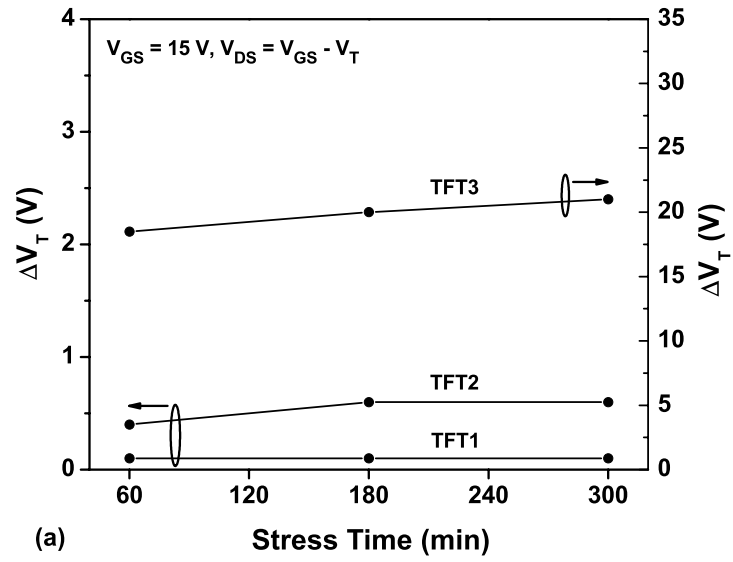
Figure 5.6: Threshold voltage shift as a function of stress time for a gate voltage of (a) 15 V, and (b) 25 V in the saturation regime.

centers around the Fermi level facilitates electron injection from the channel into empty trap states in the nitride. Charge trapping centers are believed to be silicon dangling bonds [45, 70]. TFTs with a Si-rich nitride are expected to possess larger density of trapping centers, and thus show larger shifts in V_T. This observation appears to be irrespective of the channel material as observed here for nc-Si TFTs and elsewhere for α-Si:H TFTs [45, 70]. In contrast, the density of silicon dangling bonds is minimized in an N-rich α-SiNx:H, thus suppressing the rate of charge trapping and the shift in V_T [70].

Regardless of the nitride composition, the degree of V_T shift depends on whether TFTs are operated in the linear or saturation regime. In other words, ΔV_T depends on the concentration of band tail carriers or the induced channel charge given by (2.12). Measurements showed that the presence of a higher V_{DS} reduces the shift in V_T, consistent with the results reported in Ref. [54]. Figure 5.6 shows ΔV_T as a function of stress time when the TFTs were subject to a DC gate bias in the saturation regime, where $V_{DS} = V_{GS} - V_T$. The ΔV_T in the linear regime (Fig. 5.5) is consistently higher than that in the saturation regime. Several reasons have been stipulated for the reduced ΔV_T. First, as the induced channel charge is decreased due to increased V_{DS}, so do defect creation in the channel layer for α-Si:H TFTs [54] and charge trapping in the gate dielectric for both nc-Si and α-Si:H TFTs. At pinch-off, the channel charge is around 2/3 of that at $V_{DS} = 0$, predicted by (2.12) [54]. Second, a non-zero V_{DS} reduces the field-induced stress in the drain to gate region, consequently reducing charge trapping in the nitride close to the drain terminal [39]. Realistically, both mechanisms can occur simultaneously to reduce the degree of threshold voltage shift. From Figs. 5.5 and 5.6, one may also notice that the ratio of ΔV_T in saturation and linear regimes closely resembles the ratio of respective channel charge, i.e. 2/3 [54]. For example, ΔV_T for TFT1 when subject to a stress voltage of 25 V is 1.35 V and 0.75 V in linear and saturation regimes, respectively. Comparing ΔV_T for the TFTs, TFT1 with the N-rich nitride dielectric exhibits the smallest ΔV_T in both linear and saturation regimes, indicating that the gate dielectric plays a critical role in device stability irrespective of operation

conditions.

Threshold Voltage Shift: Comparison with Amorphous Silicon TFTs

Thus far, it is clear that the TFT1 with a nitrogen-rich gate dielectric exhibits the best performance characteristics, and we have shown that defect creation is absent in our nc-Si TFTs. In this part, we further compare the stability of the nc-Si TFT1 with that of the α-Si:H counterpart. Indeed, we have already done a rigorous comparison and the results were discussed on Fig. 5.1. Here, we present the results of additional experiments that were performed under several DC gate voltages in both saturation and linear regimes for shorter times (5 hours).

Figure 5.7 shows the shift in threshold voltage over time when the TFT was subject to DC gate voltages in the range 10-25 V. In part (a), V_{DS} was set to 0.1 V to maintain the TFT in the linear operation regime in which the threshold voltage shift is more profound [54]. In part (b), V_{DS} was set to $V_{GS} - V_T$ to operate the TFT in saturation regime in order to compare ΔV_T in both cases. The total stress time was 5 hours and the test was interrupted three times (after 1 hour, 3 hours, and 5 hours) to retrieve the transfer characteristics. Included for comparison are stress test results for α-Si:H TFTs reported elsewhere [24, 54], and are referred to as "a-Si:H" in the figure.

From Fig. 5.7, it is seen that for gate voltages in the range 10-15 V, ΔV_T of the nc-Si TFT is nearly the same and independent of stress voltage and time. It ranges from 100 to 300 mV. After five hours of stress at 15 V, ΔV_T is around 0.2 V, while that of the α-Si:H device is nearly 1 V. Similarly, for a 20 V gate bias, we obtained a ΔV_T of 0.7 V while that for the α-Si:H TFT is 2.2 V. Therefore, ΔV_T in the nc-Si TFT is 3-5 times smaller than that in the α-Si:H counterpart.

It should be noted that the origin of ΔV_T in two devices is different. In the nc-Si TFT, it is due to the charge trapping which is reversible, e.g. by applying a negative gate bias as shown in Fig. 5.4. However, in the α-Si:H TFT, it is due to the defect state creation which is irreversible. For some applications, it is possible

(a)

(b)
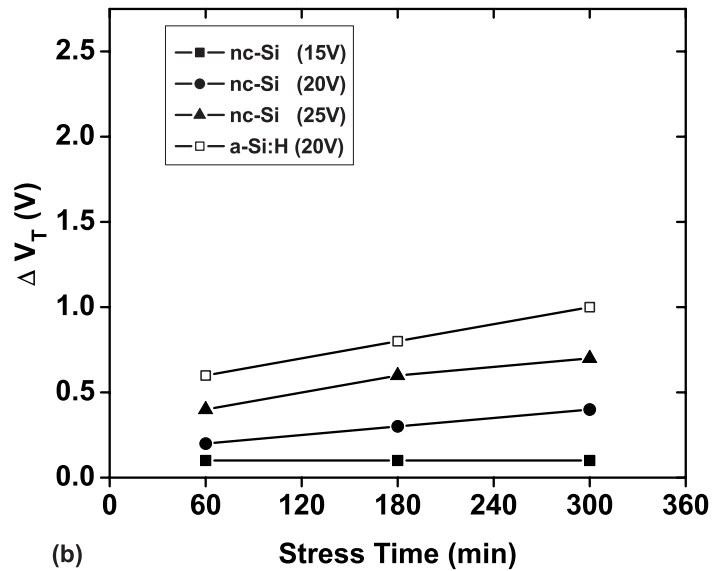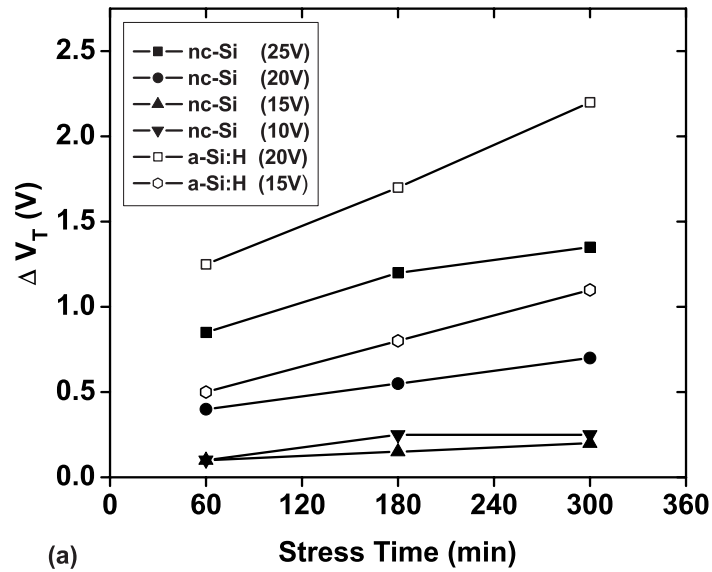
Figure 5.7: Threshold voltage shift as a function of stress time for several gate biases at (a) linear when $V_{DS} = 0.1\,V$, and (b) saturation regime when $V_{DS} = V_{GS} - V_T$. For example, "nc-Si (20V)" means that the TFT under test is the nc-Si TFT1 and the stress voltage is 20 V. The data on α-Si:H are from Refs. [24, 54].

to use this property and change the polarity of the applied gate voltage in order to recover the initial threshold voltage.

As discussed before, the threshold voltage shift in the saturation regime is smaller than that in the linear regime. This is valid for both nc-Si and α-Si:H TFTs, when we compare their ΔV_T shown in Fig. 5.7 (a) and (b) for linear and saturation regimes, respectively. Earlier, we discussed that by increasing the drain voltage, the concentration of band tail carriers in the TFT channel decreases, according to equation (2.12). This reduction leads to a decrease in the rate of defect states creation in the channel layer for α-Si:H TFTs, and a decrease in the rate of charge trapping in the nitride gate dielectric for both nc-Si and α-Si:H TFTs.

Therefore, if we bias the TFTs at small gate biases and large drain voltages, e.g. in saturation, they should exhibit smaller threshold voltage shifts. For example, from Fig. 5.7 (b), it is seen that for a 15 V stress voltage, ΔV_T is constant at 0.1-0.2 V over time. Figure 5.8 shows another example. It shows the transfer characteristics of TFT1 before and after application of a bias stress of 10 V to both gate and drain terminals ($V_{DS} = V_{GS} = 10\,V$) for 36 hours at room temperature. As seen, there is a negligible hysteresis in the I-V curve, despite the extended stress test. It should be noted that this does not mean that TFTs are fully stable, as we have observed some minor charge trapping that occurs during the stressing period. Once the gate bias is removed to retrieve the I-V characteristics, a portion of trapped charges are released back into the channel layer and it looks like that there has been no ΔV_T. We think that there is an error of about 0.1-0.3 V in estimation of ΔV_T.

The result in Fig. 5.8 shows that nc-Si TFTs can be used as pixel drivers in OLED displays with high degree of reliability. This range of biasing condition, i.e. gate voltages of less than 10 V in saturation regime, is commonly employed in OLED displays and, in reality, the TFT duty cycle is much shorter than that we performed in Fig. 5.8.
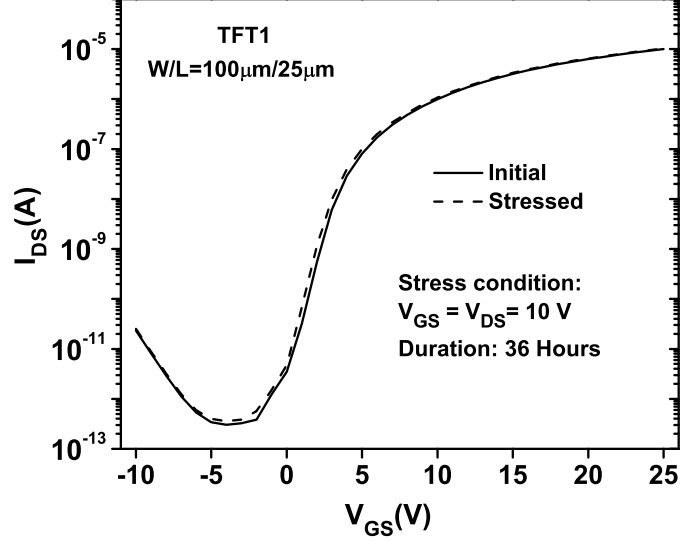
Figure 5.8: Transfer characteristics of the nc-Si TFT1 before and after bias stress for 36 hours ($V_{DS} = V_{GS} = 10\,V$).

5.3   Summary

We discussed the two instability mechanisms, i.e. defect state creation and charge trapping, that generally exist in both α-Si:H and nc-Si TFTs, albeit with different degrees. We compared the threshold voltage shift of the nc-Si TFTs with that of the α-Si:H counterpart, under similar operation conditions. For example, we electrically stressed the TFTs under constant drain currents of 2, 10, and 15 μA at two temperatures of 22 and 75 °C for 50 hours. The same tests have been performed on α-Si:H TFTs fabricated in our group [55]. We found two fundamental differences in the behavior of nc-Si TFTs compared to that of the α-Si:H TFTs. First, ΔV_T in nc-Si TFT saturates at prolonged stress times, but that of α-Si:H TFT does not. Second, ΔV_T in nc-Si TFT is weakly temperature dependent, in contrast to that of α-Si:H device. For example, after 50 hours stressing at 15 μA, ΔV_T in nc-Si TFT is 3 V and 4 V at 22 and 75 °C, respectively, whereas that for the α-Si:H TFT is 7.6 V and 21 V, respectively.

The observed behavior of ΔV_T indicates absence of defect state creation in the nc-Si TFTs. Its weak temperature dependence is consistent with the mecha-

nism proposed by Powell et al. [45], implying that the instability mechanism is charge trapping in the nitride. The kinetics of ΔV_T does also follow the stretched-exponential time dependence predicted for charge trapping [52]. To gain quantitative insight, we performed curve fitting of experimental data to eqn. (2.6), which has been proposed for charge trapping in the nitride. It was calculated that when the stressing temperature increases from 22 to 75 °C, the parameter τ changes in the range $10^8 - 10^7$ sec in nc-Si TFTs and $10^8 - 10^5$ sec in α-Si:H TFTs [52]. A smaller τ leads to a larger ΔV_T for a given stress time, according to (2.6). Thus, increasing the temperature reduces the τ in nc-Si TFTs by one order of magnitude, while in the case of α-Si:H, its reduction is by three orders. This indicates a higher stability and longer-term reliability of nc-Si TFTs, even at high operation temperatures.

To further support the conclusion that defect creation is absent in nc-Si TFTs, we investigated the other attribute of the charge trapping, i.e. its reversibility. It is known that charge trapping is reversible, but defect creation is indefinitely stable and irreversible at room temperature. We performed the relaxation test, in which a nc-Si TFT was electrically stressed for some time to induce some shift in its threshold voltage. Subsequently, the TFT was relaxed, i.e. bias voltages were removed and device was turned off. From time to time, a quick test was done to retrieve its I-V characteristics to see whether the induced ΔV_T was disappeared and initial I-V curves were obtained. We found that after 5 days relaxation at room temperature, the initial I-V curves can be obtained. This observation is another evidence indicating that charge trapping in the nitride causes ΔV_T in nc-Si TFTs. If defect creation were the source of instability, it may take around a year at room temperature to anneal the created defects and retrieve the initial I-V curves.

We also evaluated the V_T stability of TFTs under constant gate voltages in both linear and saturation regimes. For comparison, we brought ΔV_T data on α-Si:H TFT from our group publications. We observed that nc-Si TFTs are consistently more stable than the α-Si:H devices, as they exhibited smaller shift in their V_T. In

constant voltage stressing, it was seen that when the drain bias increases, ΔV_T in both α-Si:H and nc-Si TFTs decreases, which was explained by the reduction in channel charge due to the higher drain bias. This reduction in the channel charge results in a decrease in the rate of defect creation in the channel layer for α-Si:H TFTs, and a decrease in the rate of charge trapping in the nitride gate dielectric for nc-Si and α-Si:H TFTs. In addition, for gate voltages in the range 10-15 V, ΔV_T of the nc-Si TFT was small and in the range of 0.1-0.4 V.

Chapter 6

Conclusions

Thus far, thin film transistors (TFTs) have been primarily used as a pixel switch in the active matrix flat panel electronics such as LCDs and x-ray imagers. Although hydrogenated amorphous silicon (α-Si:H) has been the technology of choice for these applications, the TFT field-effect mobility and stability are limited. Here, disordered Si-Si bonds form shallow trapping states, i.e. band tail states, leading to device mobility in the range of $1\,cm^2/V.s$. Moreover, α-Si:H TFTs show drain current degradation under electrical stress, due to defect creation in the α-Si:H active layer and charge trapping in the gate dielectric. Both low field-effect mobility and drain current degradation are unacceptable for some applications, in which there is a need for on-pixel analog functions, particularly in emerging applications such as organic light emitting diode (OLED) displays. Poly-Si TFTs have been developed for this purpose, although their industrial implementation is limited due to high manufacturing cost, complex process, and non-uniformity in device characteristics over large area.

Nanocrystalline silicon (nc-Si) TFTs have been proposed as a low cost, high performance alternative, where two device configurations, top-gate and bottom-gate, have been studied. While top-gate structure usually renders higher field-effect mobility than the bottom-gate, due to the higher crystallinity of channel layer at the top, the latter represents the current industrial standard for active matrix LCDs.

Thus, bottom-gate nc-Si TFT with improved performance compared to its α-Si:H counterpart, would be easily adopted by industry [27]. Currently, instability of bottom-gate TFT is the primary issue hindering implementation of active matrix arrays for OLED displays [14]. For this reason, the focus of this research has been on the bottom-gate structure and its outstanding challenges, including electrical stability.

A major issue in bottom-gate TFTs is the quality of initial layers of nc-Si close to the gate dielectric interface. Often times, it is found that initial layers are fully amorphous, so called amorphous incubation layer [27]. The incubation layer thickness depends on PECVD conditions and could be as thick as several tens of nanometers [22]. If the amorphous incubation layer of considerable thickness exists, the nc-Si TFT behaves the same as α-Si:H devices, since the conduction channel is within $10\,nm$ from the gate dielectric interface [34]. For example, the amorphous incubation layer leads to device instability, similar to that observed in α-Si:H TFTs. Thus, it should be eliminated and crystallinity of initial layers should be high to achieve stable TFTs [27].

Bottom-gate nc-Si TFTs have been reported by several groups [26, 27, 32, 35]. However, there has been no comprehensive information on the nc-Si active layer. Indeed, it is unclear whether the amorphous incubation layer exists in the reported TFTs. Although it is often claimed that nc-Si TFTs are more stable than their α-Si:H counterpart, instability mechanisms are ill-understood and have not been analyzed.

Another issue with this TFT is the high drain-source leakage current, i.e. off-current. The leakage current is important in flat panel electronics, in which image or video information are stored in pixel circuits and should not be lost. In other words, TFT with a high off-current acts as a charge leakage path that leads to loss of information.

In what follows, results, conclusions, and contributions of this research concerning the challenges of bottom-gate nc-Si TFTs are summarized.

6.1   Conclusions and Contributions

In chapter three, we studied how the crystallinity of nc-Si layers is affected by PECVD parameters. It was found that hydrogen and silane flow rates are the most important parameters in achieving layers with high crystallinity, as reported by others too [21, 66]. It was also shown that chamber pressure does not have a significant effect on the film crystallinity. On the other hand, from the viewpoint of bottom-gate TFTs, the nc-Si layer should not be processed at low chamber pressures and high plasma powers to avoid ion bombardment and damaging the sensitive gate dielectric interface [24, 27]. Applying these conclusions, we were able to obtain very thin (15 nm) layers with crystallinity of around 60%. Moreover, we showed that it is possible to eliminate the amorphous incubation layer, as TEM images showed that crystalline grains start growing right from the gate dielectric interface, which is needed for bottom-gate TFTs.

In chapter four, we studied the off-current of TFTs, where it was shown to be determined by the conductivity of channel layer and by the quality of silicon/passivation nitride interface. Two channel layer structures were studied; it either consists of a single nc-Si layer or a bi-layer of nc-Si/α-Si:H. In both structures, channel layer is sandwiched between two nitrides, i.e. gate dielectric and passivation nitride. In single-layer TFT structure, when the passivation nitride interface is with nc-Si, charge accumulation near that interface, due to the presence of fixed charges, leads to increased off-current. In contrast, when the nc-Si layer is capped with α-Si:H in the bi-layer channel, the off-current decreases and is determined by the bulk conductivity of nc-Si, as the α-Si:H makes a less defective interface with the passivation nitride. The experimental results showed that off-current in single-layer TFT is about two orders of magnitude larger than that in bi-layer TFT, under identical biasing conditions, which was shown to be due to an extra band bending at the nc-Si/passivation nitride interface in single-layer TFT. Therefore, the preferred device structure should comprise of a nc-Si/α-Si:H bi-layer.

In addition, we performed numerical simulations in order to optimize the nc-Si/α-Si:H bi-layer. The simulation results showed that the off-current is insensitive to the α-Si:H thickness, while on-current decreases at higher α-Si:H thicknesses. Therefore, from an on-current standpoint a thinner α-Si:H cap is desired. On the other hand, to further reduce the I_{OFF}, we had to redesign the nc-Si layer by considering that its conductivity is thickness dependent, i.e. decreases at lower thicknesses. By employing 15 nm nc-Si and 35 nm α-Si:H cap, we were able to obtain off-currents as low as $10^{-13}\,A$, and to maintain on-currents as high as $10\,\mu A$. This level of on- and off-current is quite acceptable for applications such as OLED displays and x-ray imagers. The results presented here contrast with previous claims that the I_{OFF} in nc-Si TFTs is due to the band-to-band tunneling, which is suppressed by the α-Si:H cap due to its larger bandgap [43].

We also studied TFTs with various compositions of hydrogenated amorphous silicon nitride (α-SiNx:H) gate dielectric. We varied the composition of the nitride ([N]/[Si]) from 1.3 to 1, by adjusting the NH_3/SiH_4 gas flow ratio. TFTs with a nitrogen-rich nitride ([N]/[Si]=1.3) yielded higher on-current and field-effect mobility than the devices with silicon-rich gate dielectric ([N]/[Si]=1). For example, mobility dropped from $0.75\,cm^2/Vs$ to $0.2\,cm^2/Vs$ when the gate dielectric composition [N]/[Si] changed from 1.3 to 1. It was also observed that device stability is highly dependent on the nitride composition, which is consistent with previous studies on α-Si:H TFTs [70]. TFTs with an [N]/[Si] of 1.3 exhibited the best stability, with a 0.3 V shift in their threshold voltage at a gate voltage of 15 V. However, TFTs with an [N]/[Si] of 1 showed a 12.4 V shift under similar biasing condition.

In chapter five, we further compared the threshold voltage shift (ΔV_T) of our nc-Si TFTs with that of the α-Si:H counterpart, under similar operation conditions. We electrically stressed the TFTs under constant drain currents of 2, 10, and $15\,\mu A$ at two temperatures of 22 and $75\,°C$ for 50 hours. The same tests have been performed on α-Si:H TFTs fabricated in our group [55]. We found two fundamental differences in the behavior of nc-Si TFTs compared to that of the α-Si:H TFTs.

First, ΔV_T in the nc-Si TFT saturates at prolonged stress times, but that of α-Si:H TFT does not. Second, ΔV_T in the nc-Si TFT is weakly temperature dependent, in contrast to that of α-Si:H device. For example, after 50 hours stressing at $15\,\mu A$, ΔV_T in the nc-Si TFT is 3 V and 4 V at 22 and 75 °C, respectively, whereas that for the α-Si:H TFT is 7.6 V and 21 V, respectively. The observed behavior of ΔV_T indicates absence of defect state creation in the nc-Si TFTs. Its weak temperature dependence is consistent with the charge trapping mechanism proposed by Powell et al. [45], and its kinetics does also follow the stretched-exponential time dependence predicted for charge trapping [52].

To further support the conclusion that defect creation is absent in our devices, we investigated the other attribute of the charge trapping, i.e. its reversibility. It is known that charge trapping is reversible, but defect creation is indefinitely stable and irreversible at room temperature. We performed the relaxation test, in which a nc-Si TFT was electrically stressed for some time to induce some shift in its threshold voltage. Subsequently, the TFT was relaxed, i.e. bias voltages were removed. We found that after 5 days relaxation at room temperature, the initial I-V curves can be obtained. This observation is another evidence indicating that charge trapping in the nitride causes ΔV_T in our devices. If defect creation were the source of instability, it may take around a year at room temperature to anneal the created defects and retrieve the initial I-V curves.

We also evaluated the V_T stability of TFTs under constant gate voltages in both linear and saturation regimes, and was compared with that of α-Si:H TFTs. We observed that nc-Si TFTs are consistently more stable than α-Si:H devices, as they exhibited smaller shift in their V_T. In addition, it was observed that for gate voltages in the range 10-15 V, ΔV_T of our devices was small and less than 0.5 V.

In conclusion, we have shown that out of the two instability mechanisms, i.e. defect state creation in the active layer and charge trapping in the gate dielectric, the former can be eliminated by using a highly crystalline nc-Si layer and the latter can be minimized by using a nitrogen-rich nitride as the gate dielectric. The off-

current can also be minimized by using a bi-layer structure so that a thin (15 nm) nc-Si layer is capped with a thin (35 nm) α-Si:H, and values as low as $0.1\,pA$ can be obtained. The low off-current along with superior stability of nc-Si TFT, coupled with its fabrication in a standard 13.56 MHz PECVD system using conventional silane and hydrogen source gases, make it very attractive for large area applications such as pixel drivers in active matrix OLED displays and x-ray imagers.

6.2 Recommendations for Future Work

Although several issues of nc-Si TFTs have been addressed in this research, there are opportunities for further work. For example, we have measured the threshold voltage shifts at a maximum temperature of $75\,°C$, and deduced that defect states are not created. Threshold voltage shift can be evaluated at temperatures higher than $75\,°C$. It is likely that defects can be created and thus further insight into the instability mechanisms can be gained. As well, the interaction of monochromatic light, with variable frequency, with nc-Si material can be investigated. It is well-known that defect states are also created due to photon absorption and energy transfer to weak Si-Si bonds, the so called Stabler-Wronski effect. The results of such experiments will be also valuable for solar cell applications, particularly thin film solar cells with nc-Si as the absorber. Indeed, nc-Si has attracted considerable attention in the photovoltaic community, for stable solar cells on low-cost flexible substrates. Research along this line is currently in progress in our group as well as several other research groups.

The outstanding challenge is the low field-effect mobility of bottom-gate nc-Si TFT. Currently, it is more or less the same as that of α-Si:H devices, as obtained in this research and have been reported by others [26, 27, 32, 35]. The low mobility is attributed to low quality and crystallinity of initial layers of nc-Si, compared to top layers which are highly crystalline. To obtain higher values, PECVD processes should be further optimized in order to increase the crystallinity of initial layers,

and to reduce the density of defects at the gate dielectric interface.

Finally, it would be worthwhile to investigate nc-Si TFT and its performance parameters at lower deposition temperatures. It is well-known that the quality of silicon thin films is affected by the deposition temperature. For example, TFTs may be processed at temperatures around $150\,°\text{C}$. If satisfactory results can be achieved, the TFT can be transferred to cheaper substrates such as plastics for flexible electronics applications.

Appendix A

List of Publications

A.1 Journals

- M.R. Esmaeili-Rad, A. Sazonov, and A. Nathan, "Analysis of the Off Current in Nanocrystalline Silicon Bottom-Gate Thin-Film Transistors," *Journal of Applied Physics*, vol. 103, pp. 074502-1-6, 2008.

- M.R. Esmaeili-Rad, F. Li, A. Sazonov, and A. Nathan, "Stability of Nanocrystalline Silicon Bottom-gate Thin Film Transistors with Silicon Nitride Gate Dielectric," *Journal of Applied Physics*, vol. 102, pp. 064512-1-7, 2007. Also appeared in *Virtual Journal of Nanoscale Science and Technology*, vol. 16, no. 16, 2007.

- M.R. Esmaeili-Rad, A. Sazonov, and A. Nathan, "Absence of Defect State Creation in Nanocrystalline Silicon Thin Film Transistors Deduced from Constant Current Stress Measurements," *Applied Physics Letters*, vol. 91, pp. 113511-1-3, 2007. Also appeared in *Virtual Journal of Nanoscale Science and Technology*, vol. 16, no. 13, 2007.

- M.R. Esmaeili-Rad, A. Sazonov, A. G. Kazanskii, A. A. Khomich, and A. Nathan, "Optical Properties of Nanocrystalline Silicon Deposited by

PECVD," *Journal of Materials Science: Materials in Electronics*, vol. 18, pp. S405-9, 2007.

A.2 Refereed Conference Papers

- M.R. Esmaeili-Rad, A. Sazonov, and A. Nathan, "High Stability, Low Leakage Nanocrystalline Silicon Bottom Gate Thin Film Transistors for AMOLED Displays," in *Technical Digest of IEEE International Electron Device Meeting* (IEDM), pp. 303-6, 2006.

- C.-H. Lee, A. Sazonov, J. Robertson, A. Nathan, M.R. Esmaeili-Rad, P. Servati, and W.I. Milne, "How to Achieve High Mobility Thin Film Transistors by Direct Deposition of Silicon Using 13.56 MHz RF PECVD?," in *Technical Digest of IEEE International Electron Device Meeting* (IEDM), pp. 295-8, 2006.

- M.R. Esmaeili-Rad, C.-H. Lee, A. Sazonov, and A. Nathan, "Nanocrystalline Silicon Films Deposited by RF PECVD for Bottom-gate Thin-film Transistors," in *Proceedings of Material Research Society Symposium*, vol. 910, pp. A22-13-1-6, 2006.

- C.-H. Lee, A. Sazonov, M.R. Esmaeili-Rad, G. R. Chaji, and A. Nathan, "Ambipolar Thin-Film Transistors Fabricated by PECVD Nanocrystalline Silicon," in *Proceedings of Material Research Society Symposium*, vol. 910, pp. A22-05-1-6, 2006.

A.3 Conference Presentations

- M.R. Esmaeili-Rad, A. Sazonov, and A. Nathan, "Nanocrystalline Silicon Thin Film Transistors with High V_T Stability," in *Advanced Workshop on Frontiers in Electronics*, Mexico, December 15-19, 2007.

- M.R. Esmaeili-Rad, A. Sazonov, and A. Nathan, "Hydrogen Passivation and Channel Capping for Threshold Voltage Shift and Off-current Reduction in Nanocrystalline Silicon TFTs," *The Electrochemical Society Transactions*, vol. 3, no. 8, pp. 93-97, 2006.

- M.R. Esmaeili-Rad, A. Sazonov, and A. Nathan, "Optical and Electrical Properties of Intrinsic Nanocrystalline Silicon Deposited by PECVD," *International Conference on Optical and Optoelectronic Properties of Materials and Applications* (ICOOPMA), Darwin, Australia, July 15-22, 2006.

- A.G. Kazanskii, A.A. Khomich, A. Sazonov, M.R. Esmaeili Rad, C.-H. Lee, A. Nathan, V.I. Kovalev, and A.I. Rukovishnikov, "Optical, Electrical and Photoelectrical Characterization of PECVD Nanocrystalline Silicon Thin Films," *6th International Conference of Micro- and nano-electronics*, Moscow, Russia, October 3-7, 2005.

- M.R. Esmaeili-Rad, C.-H. Lee, A. Sazonov, and A. Nathan, "Optimization of Nanocrystalline Silicon Deposition for High Performance Thin Film Circuits," *12th Canadian Semiconductor Technology Conference*, Ottawa, August 15-19, 2005.

Appendix B

Medici Code for TFT Simulation

The following is a sample Medici code used in numerical simulations of TFTs, presented in chapter four. Details of input statements and model parameters can be found here.

```
COMMENT "Code Begins"
MESH OUT.FILE=offcurrent.MSH
X.MESH WIDTH=35 N.SPACES=50
Y.MESH WIDTH=0.5 N.SPACES=20

REGION NAME=nplusS SILICON Y.MAX=0.05 X.MAX=5
REGION NAME=nplusD SILICON  Y.MAX=0.05 X.MIN=30
REGION NAME=SIN NITRIDE    Y.MAX=0.05 X.MIN=5 X.MAX=30
REGION NAME=a-Si SILICON  Y.MIN=0.05  Y.MAX=0.1
REGION NAME=UC-Si SILICON  Y.MIN=0.1  Y.MAX=0.2
REGION NAME=GDSIN NITRIDE    Y.MIN=0.2

ELECT NAME=Drain TOP  X.MIN=30
ELECT NAME=Source TOP X.MAX=5
ELECT NAME=Gate BOTTOM
```

```
COMMENT Specify doping

PROFILE  REGION="UC-Si"  UNIFORM CONC=1.25*1E18 N-TYPE

PROFILE  REGION="a-Si"   UNIFORM CONC=4.5*1E15 N-TYPE

PROFILE  REGION="nplusS"  UNIFORM  CONC=1E20   N-TYPE

PROFILE  REGION="nplusD"  UNIFORM  CONC=1E20   N-TYPE


CONTACT  NAME=Source SCHOTTKY VSURFN=1E7 VSURFP=1E7

CONTACT  NAME=Drain  SCHOTTKY VSURFN=1E7 VSURFP=1E7

CONTACT  NAME=Gate  SCHOTTKY VSURFN=1E7 VSURFP=1E7


ASSIGN NAME=BNDGPUSI N.VAL=1.3

ASSIGN NAME=BNDGPASI N.VAL=1.8


MATERIAL REGION="UC-Si"   AFFINITY=4.1  EG300=@BNDGPUSI

MOBILITY REGION="UC-Si" MUN0=.5 MUP0=.1

MATERIAL REGION="a-Si"   AFFINITY=3.9  EG300=@BNDGPASI

MOBILITY REGION="a-Si" MUN0=.5 MUP0=.01

MATERIAL REGION="nplusS"   AFFINITY=4.1  EG300=@BNDGPUSI

MOBILITY REGION="nplusS" MUN0=1 MUP0=.01

MATERIAL REGION="nplusD"   AFFINITY=4.1  EG300=@BNDGPUSI

MOBILITY REGION="nplusD" MUN0=1 MUP0=.01


COMMENT "defines fixed charges at top/bottom interfaces"

COMMENT "Remove "COMMENT" below to activate"

COMMENT INTERFACE REGION=(GDSIN,UC-Si) QF=5*1E11

COMMENT INTERFACE REGION=(SIN,a-Si) QF=4*1E11


MODELS SRH

SYMB GUMM CARR=0
```

```
COMMENT SYMB NEWT CARR=0

SOLVE  V(Drain)=0 OUT.FILE=offcurrent.INI

LOAD IN.FILE=offcurrent.INI


ASSIGN NAME=EVASI N.VAL=-(@BNDGPASI)/2

ASSIGN NAME=ECASI N.VAL=(@BNDGPASI)/2

ASSIGN NAME=EVUSI N.VAL=-(@BNDGPUSI)/2

ASSIGN NAME=ECUSI N.VAL=(@BNDGPUSI)/2


COMMENT "this section defines trap densities in a-Si layer"

COMMENT Calculates characteristic length for hole states

ASSIGN NAME=PCHRASI N.VAL=0.05

COMMENT Gererate hole traps

TRAP DISTR N.TOT="-(1*1E16+3*1E21*EXP(-(@FENER-@EVASI)/@PCHRASI))"

+ COND="(@FENER<0)&(@Y>0.05)&(@Y<0.1)"

+ MIDGAP TAUN="1E-8" TAUP="1E-8"

COMMENT Calculate characteristic length for electron states

ASSIGN NAME=NCHRASI N.VAL=0.035

COMMENT Generate electron traps

TRAP N.TOT="(1*1E16+3*1E21*EXP((@FENER-@ECASI)/@NCHRASI))"

+ COND="(@FENER>0)&(@Y>0.05)&(@Y<0.1)"

+ MIDGAP TAUN="1*1E-8" TAUP="1E-8"


COMMENT "this section defines the trap densities in nc-Si layer"

COMMENT Calculate characteristic length for hole states

ASSIGN NAME=PCHRUSI N.VAL=0.05

COMMENT Gererate hole traps

COMMENT Gererate hole traps

TRAP DISTR N.TOT="-(1*1E15+3*1E20*EXP(-(@FENER-@EVUSI)/@PCHRUSI))"

+ COND="(@FENER<0)&(@Y>0.1)"
```

```
+ MIDGAP TAUN="1E-8" TAUP="1E-8"

COMMENT TRAP N.TOT="-(5*1E18)"

+ COND="(@FENER<0)&(@FENER>(-0.25))&(@Y>0.25)"

+ MIDGAP TAUN="1*1E-8" TAUP="1E-8"

COMMENT Calculate characteristic length for electron states

ASSIGN NAME=NCHRUSI N.VAL=0.02

COMMENT Generate electron traps

TRAP N.TOT="(4.7*1E12+3*1E20*EXP((@FENER-@ECUSI)/@NCHRUSI))"

+ COND="(@FENER>0)&(@Y>0.1)"

+ MIDGAP TAUN="1*1E-8" TAUP="1E-8"

TRAP N.TOT="(5.075*1E18)"

+ COND="(@FENER>0)&(@FENER<0.25)&(@Y>0.085)"

+ MIDGAP TAUN="1*1E-8" TAUP="1E-8"


PLOT.2D GRID FILL

COMMENT SOLVING AND MODELING BEGIN HERE

SYMB GUMM CARR=0

COMMENT SYMB NEWT CARR=0

SOLVE

SYMB NEWT CARR=2

COMMENT SYMB NEWT CARR=1 ELECTRON

METHOD N.DAMP

SOLVE


COMMENT 0-carrier solution with Vd=0.1v

SYMB CARRIERS=1 ELECTRON

SOLVE INIT V(Drain)=.10 V(Gate)=0 OUT.FILE=TEMPSOL

LOAD IN.FILE=TEMPSOL


PLOT.1D CONDUC BOT=3 TOP=-3 X.ST=15 X.EN=15
```

```
+ OUTFILE=conduc.txt
PLOT.1D VALENC BOT=3 TOP=-3 X.ST=15 X.EN=15
+ UNCHANGE OUTFILE=valence.txt
LOG  OUT.FILE=TFT-NT.IVL
SOLVE  V(Source)=0  V(Drain)=1 V(Gate)=-20
+ ELECTROD=Gate VSTEP=1 NSTEP=40
LOG CLOSE


PLOT.1D   Y.AX=I(Drain)   X.AX=V(Gate)   IN.FILE=TFT-NT.IVL
+SYMB=1  Y.LOGARI  OUTFILE=IV.txt
COMMENT "Code Ends"
```

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