Tunable Superconducting Microwave Filters

by

Paul Laforge

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2010

AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Paul Laforge

Abstract

Adaptive microwave systems can benefit from the use of low loss tunable microwave filters. Realizing these tunable filters that show low loss characteristics can be very challenging. The proper materials, tuning elements, and filter designs need to be considered when creating a low loss tunable filter. The integration of low loss microelectromechanical systems (MEMS) and superconducting circuits is one method of achieving these types of tunable filters. The thesis introduces new multi-layer low temperature superconducting (LTS) filters and diplexers and novel topologies for tunable filters and switched multiplexers. An efficient method of designing such filters is proposed. A fabrication process to monolithically integrate MEMS devices with high temperature superconducting (HTS) circuits is also investigated in this thesis.

The reflected group delay method, usually used for filter tuning, is further developed for use in designing microwave filters. It is advantageous in the design of filters to have electromagnetic simulation results that will correlate well to the fabricated microwave filters. A correction factor is presented for use with the reflected group delay method so the group delay needs to be matched to the appropriate value at the center frequency of the filter and be symmetric about the center frequency of the filter. As demonstrated with an ideal lumped element filter, the group delay method can be implemented when a closed form expression for the circuit is not known. An 8-pole HTS filter design and an 8-pole multi-layer LTS filter design demonstrate the use of the reflected group delay method.

Low temperature superconducting filters, couplers and diplexers are designed and fabricated using a multilayer niobium fabrication process traditionally used for superconducting digital microelectronics. The feasibility of realizing highly miniaturized microwave niobium devices allows for the integration of superconducting digital microelectronics circuits and analog microwave devices on a single chip. Microwave devices such as bandpass filters, lowpass filters, bandstop filters, quadrature hybrids, and resistive loads are all demonstrated experimentally.

New tunable filter designs are presented that can make use of MEMS switches. A manifold-coupled switched multiplexer that allows for 2^N possible states is presented. The tunable multiplexer has N filters connected to two manifolds and has embedded switches, which detune certain resonators within the filters to switch between ON and OFF states for each channel. The new concept is demonstrated with a diplexer design and two 3-pole coplanar filters. The concept is further developed through test results of a fabricated HTS triplexer and electromagnetic simulations to demonstrate a superconducting manifold-coupled switched triplexer. Another filter design is presented that makes use of switches placed only on the resonators of the filters. This filter design has N possible states and the absolute bandwidth can be kept constant for all N states.

Finally, the integration of HTS circuits and MEMS devices is investigated to realize low loss tunable microwave filters. The hybrid integration is first performed through the integration of an HTS microstrip filter and commercially available RF MEMS switches. A fabrication process to monolithically integrate MEMS devices and high temperature superconducting circuits is then investigated. The fabrication process includes a titanium tungsten layer, which acts as both a resistive layer and an adhesion for the dielectric layer, an amorphous silicon dielectric layer, a photoresist sacrificial layer, and the top gold layer. The fabrication process is built up on a wafer with a thin film of a high temperature superconducting material covered with a thin film of gold. Several processes are tested to ensure that the superconducting properties of the thin film are not affected during the MEMS fabrication process.

Acknowledgements

Table of Contents

List of Figures

xiv

List of Tables

Chapter 1
Introduction

1.1 Motivation

Today's microwave systems can benefit greatly from the use of tunable filters, which have some distinct advantages over traditional microwave filters and are continuously being improved. Tunable filters can be implemented in receivers to improve their performance. The phase noise and linearity specifications can be lowered with the addition of a tunable filter to the front end of a receiver.

With the use of a traditional wide band filter at the input of a receiver, signals not interfering with the desired signal at radio frequencies (RF) may interfere after passing through a mixer with a high phase noise local oscillator (LO), as shown in Fig. 1-1 a). At the intermediate frequency (IF), the tail of the interfering signal is at the same frequency as that of the desired signal. For this reason, the phase noise of the LO must be lowered.

(a)   (b)
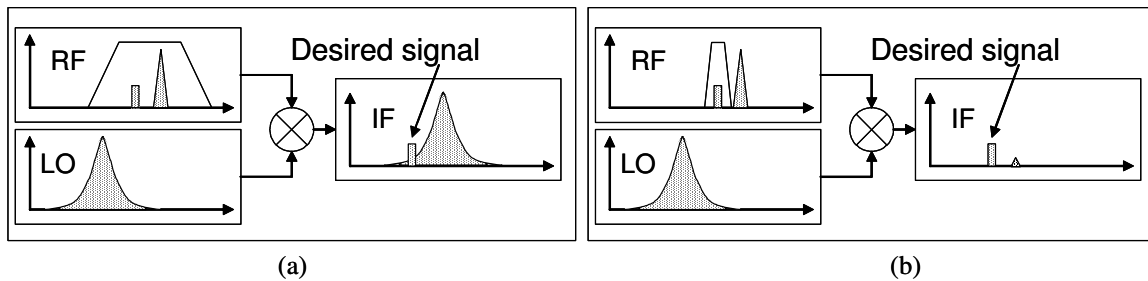
Fig. 1-1: a) Interfering signal caused by the phase noise of the local oscillator, and b) a narrow band tunable filter is used to attenuate the interfering signal.

Instead of having constraints on the phase noise of the local oscillator, a high Q (quality factor) narrow band tunable filter can attenuate the interfering signals before they pass through the mixer, as shown in Fig. 1-1 b). Since the narrow band tunable filter attenuates the interfering signal before the mixer, it does not have a tail end interfering with the desired signal. The phase noise specifications can then be relaxed to a level that will not degrade the desired signal.

1

Lowering the linearity specifications of the low noise amplifier (LNA) of the receiver is another benefit of using a narrow band tunable filter. Interfering signals are attenuated and do not generate other interfering signals after passing through the LNA.

When using a wide band filter at the front end of the receiver, interfering signals may be passed through to the LNA. Since the LNA is a non-linear device, intermodulation signals may be produced at the same frequency as that of the desired receive signal, as shown in Fig. 1-2 a). To reduce this effect, one needs to use an LNA with a good linearity performance.
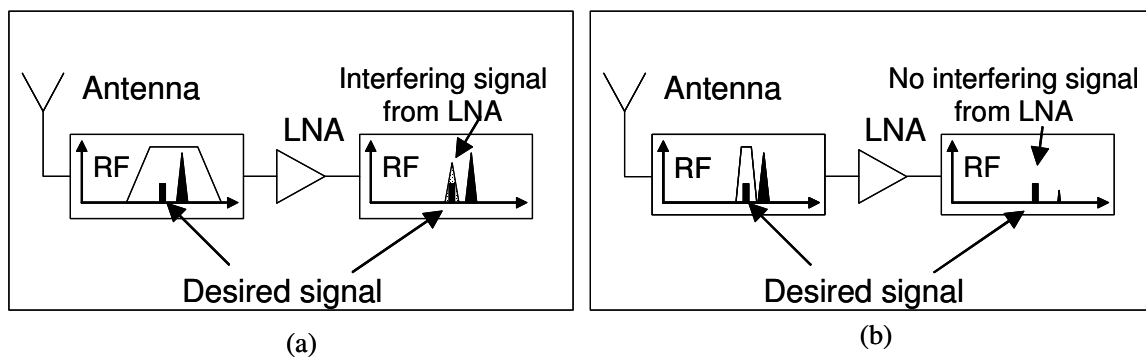
Fig. 1-2: a) Interfering signal generated by LNA. b) There is no signal generated by the LNA.

The use of a high Q narrow band tunable filter instead of a wide band filter at the front end helps in attenuating the interfering signal. The signal is attenuated enough that any signals created by the LNA do not have enough power to interfere with the desired receive signal, as shown in Fig. 1-2 b). Because of this, the linearity specifications of the LNA can be relaxed.

Other more general advantages of using tunable filters are

- radios operate at multiple frequencies,
- component count is reduced,
- system performance is optimized,
- system deployment and maintenance costs are reduced,
- capacity is increased,
- frequencies can be reused,

2

- software control can be implemented,
- out-of-band interfering signals are prevented from entering the receiver, and
- the amount of noise entering the system is reduced.

With the application of a narrow band tunable filter, the performance of a radio will improve. Also, if this filter can be tuned in an open or closed loop fashion, variations due to time and temperature can be compensated.

Since the tunable filter is at the front end of the receiver, it is essential that its noise figure is low. To achieve a low noise figure for a passive filter, the unloaded quality factor of its resonators needs to be very high. The use of thin film high temperature superconductors (HTS) or low temperature superconductors (LTS) can achieve these high quality factor resonators for planar filters. HTS planar filters have been designed with unloaded quality factors as high as 30,000.

To realize this low noise figure, the tuning element of the tunable filter must also have low loss. Microelectromechanical systems (MEMS) technology is an enabling technology to attain the lowest possible loss. MEMS devices can achieve lower loss than other tuning element technologies such as ferroelectric materials and varactor diodes. MEMS technology also has better linearity performance than other technologies such as varactor diodes. A tunable planar filter with HTS resonators and MEMS tuning elements will meet the requirements needed for a tunable filter at the front end of a receiver.

1.2 Objectives

The integration of superconducting circuits with MEMS devices, the two enabling technologies, is the next important step in realizing a low loss tunable planar filter. Improving upon the methods of designing these tunable filters, investigating the characteristics of both HTS and LTS microwave circuits, creating new tunable filter designs, and integrating superconductors and MEMS devices are all subjects investigated within the scope of this thesis. The main research topics investigated in this thesis are:

3

- the implementation of the reflected group delay method for designing LTS and HTS filters,

- the development and characterization of LTS bandpass filters, bandstop filters, couplers and diplexers using a standard niobium multilayer fabrication process used for superconducting digital microelectronics,

- the development and characterization of switched manifold coupled multiplexers, the design of superconducting switched manifold triplexers, and the design of tunable filters with constant absolute bandwidth,

- the investigation of the hybrid integration of HTS circuits and MEMS devices, and

- the investigation of the monolithic integration of MEMS devices with high temperature superconducting filters.

1.3 Thesis Outline

Following the motivation and objectives given in Chapter 1 of this thesis, summaries of tunable filter technologies, tunable filters with constant bandwidth, and the fabrication and performance of MEMS devices for use at cryogenic temperatures are all presented in Chapter 2. Chapter 3 presents a method of designing superconducting filters using the reflected group delay information. Chapter 4 includes designs of low temperature superconducting bandpass filters, diplexers, and bandstop filters. Chapter 5 presents tunable filter designs, switched multiplexer designs, the hybrid integration of an HTS filter and commercially available RF MEMS switches, and the monolithic integration of MEMS devices and high temperature superconducting circuits. Conclusions and suggestions for future work are given in Chapter 6.

1.4 Glossary of Terms

λ	Wavelength
λ_0	Wavelength in Free Space
ADC	Analog-to-Digital Converter
a-Si	Amorphous Silicon

BST	Barium Strontium Titanate
BW	Bandwidth
CCM	Calibrated Coarse Model
CMOS	Complementary Metal–Oxide–Semiconductor
CPW	Coplanar Waveguide
DC	Direct Current
DI	De-ionized
DyBCO	Dysprosium Barium Copper Oxide
EM	Electromagnetic
f_0	Center Frequency of a Filter
HTS	High Temperature Superconductor
IFF	Identification, Friend, or Foe
IPA	Isopropyl Alcohol
LC	Inductor/capacitor combination
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LTS	Low Temperature Superconductor
MEMS	Microelectromechanical systems
MgO	Magnesium Oxide
MMIC	Microwave Monolithic Integrated Circuits
MSSW	Magnetostatic Surface Wave
MUMPs®	Multi-User MEMS Process
PECVD	Plasma Enhanced Chemical Vapour Deposition
Q	Quality Factor
RF	Radio Frequency
RIE	Reactive Ion etcher
S_{11}	Return loss at port 1 of a microwave device

S_{21}	Insertion loss from port 1 to port 2 of a microwave device
SF_6	Sulfur Hexafluoride
SiN_x	Silicon Nitride
SiO_2	Silicon Dioxide
SM	Space Mapping
SME	Superconducting Microelectronics
SPDT	Single-Pole-Double-Throw
SPNT	Single-Pole-N-Throw (for any number N)
SPST	Single-Pole-Single-Throw
STO	Strontium Titanate
TEM	Transverse Electromagnetic
TiW	Titanium Tungsten
TL	Transmission Line
YBCO	Yttrium Barium Copper Oxide
YIG	Yttrium Iron Garnet

Chapter 2
Literature Survey

In this chapter, a literature survey of tunable filter technologies, tunable filters with constant absolute bandwidth, and fabrication of MEMS devices for use at cryogenic temperatures is presented. Tunable filters using active components, ferroelectric materials, ferrite materials, and mechanical methods are all listed. Different methods of maintaining a constant absolute bandwidth for a tunable filter are considered. The current development of MEMS fabrication for operation at cryogenic temperature is also presented.

2.1 Tunable Filter Technologies

Tunable filters can be realized by different types of technologies. Tunable filters with active components, such as varactor diodes, are presented. Another technology to create tunable filters is by mechanical means. This method includes piezoelectric technology and MEMS devices. Ferroelectric and ferrite materials are the final two types of technology to realize tunable filters. A comparison of these technologies is presented while considering the tuning speed, the tuning range, the power handling capability, and the insertion loss of the tunable filters.

2.1.1 Active Components

There are two main types of tunable filters that implement active components. One of these methods uses varactor diodes as tuning elements, and the other method incorporates circuits with active components such as transistors and operational amplifiers.

A variable capacitance can be seen across a reverse biased p-n junction. As the reverse voltage is applied to the p-n junction, the holes in the p-type material move toward the anode, and the electrons in the n-type material move towards the cathode of the diode. This leaves a region with no carriers, and acts as the dielectric of a capacitor. Increasing the external voltage and thus increasing the size of the depletion region will decrease the

7

capacitance. Since the varactor diode is an active device, there will be non-linearities associated with signals that pass through it.

Varactors can be used on filter structures where a capacitor can be adjusted to change the center frequency of the resonators. For example, the interdigital filter [1] and the combline filter [2]-[6] can incorporate tuning capacitors to realize a tunable filter. A design has also been presented that allows for the tuning of the bandwidth while keeping a constant center frequency [7].

First the tunable interdigital filter is investigated [1], which implements a suspended stripline interdigital filter with varactor diodes placed on the open end of each interdigital finger. There is also a bias network associated with each varactor diode. The center frequency of each resonator has the following relationship [1]

$$f_0 = \frac{1}{2\pi Z_s C_0(V) \tan(\theta_0(V))},$$

(2.1)

where Z is the impedance of the resonator, C is the capacitance of the varactor at voltage V, and θ_0 is the electrical length of the resonator of the center frequency. The achievable tuning range of this filter is 60% [1], and the insertion loss and return loss of this structure are shown in Fig. 2-1 a) and Fig. 2-1 b), respectively.
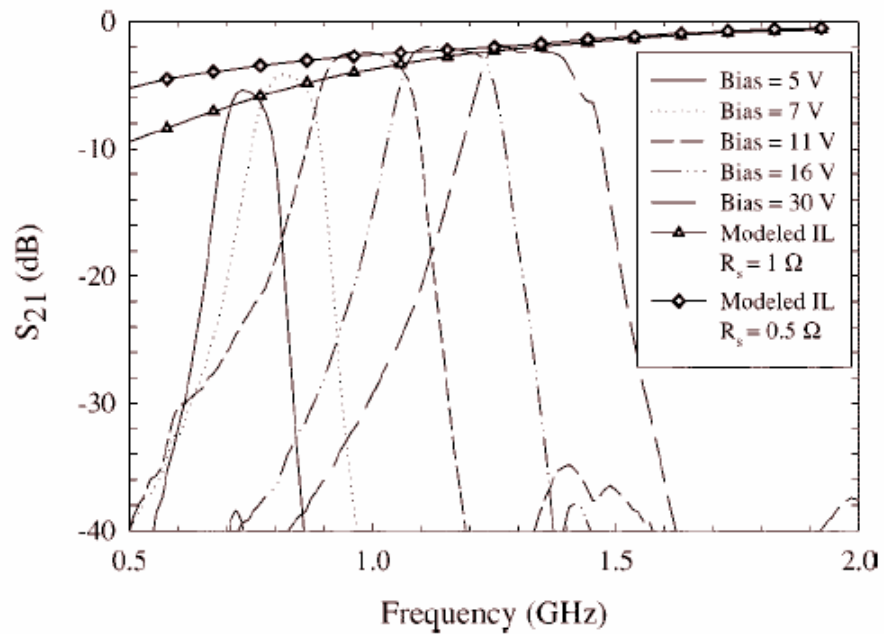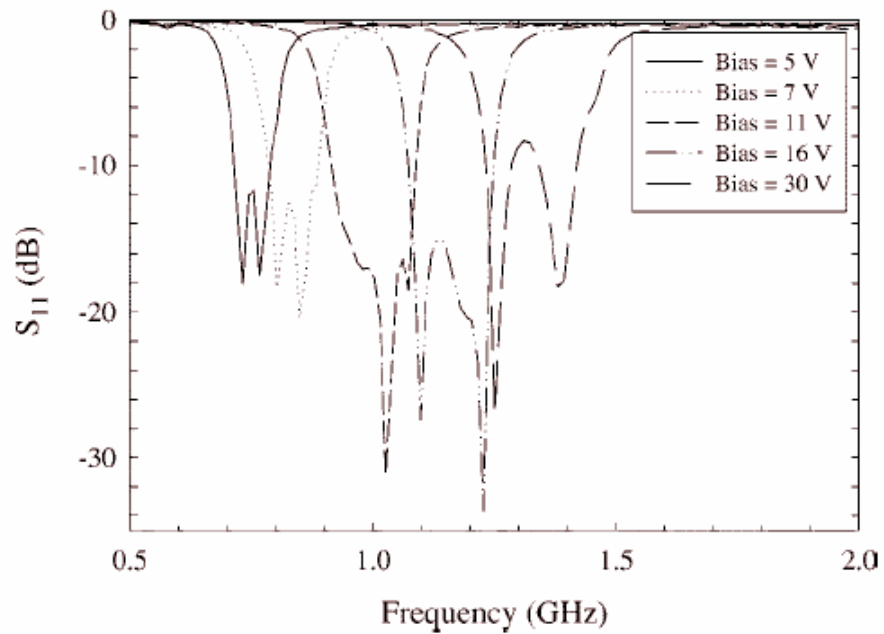
Fig. 2-1: Interdigital RF tunable filter with measured a) insertion loss and b) return loss [1].

Another structure that can be realized is that of a combline filter [2]-[6]. An approach to designing tunable combline filters with varactor diodes is presented in [2]. Improvements

to this approach are made by adding negative resistance in series with the varactor to improve the quality factor of the resonators [3]-[4].

Tunable combline filters can also produce an elliptic function response with the addition of a hairpin resonator [6]. A microstrip combline filter has a transmission zero above its passband at the frequency where the combline stubs become a quarter wavelength. Also, microstrip hairpin resonators show a transmission zero below the designed passband. So a combination of the two types of resonators in one filter design results in a transmission zero on either side of the passband, and therefore, an elliptical function response is seen.

Active filters that make use of transistors and Microwave Monolithic Integrated Circuits (MMIC) are the other type of tunable filters with active components. One type of active filter design allows for the tuning of either the center frequency or the quality factor. A resonator is formed with lumped inductors and an effective capacitance created by a reactance multiplication [9]. This effective capacitance can be varied by a change in the transconductance of a pair of transistors, which is controlled by a bias current. Another bias current in the circuit controls the value of the quality factor.

Other active filters incorporate the use of recursive concepts taken from discrete time filter applications [10]-[13]. Filters using feedback based on recursive principles were first suggested in [10]. Hybrid technologies, such as power dividers [11], first provided the ability to add feedback in these active filters. MMIC technology provided advancement in the design of these recursive active filters [12]-[13].

2.1.2 Mechanical Methods of Tuning

Two different mechanical methods for filter tuning are discussed. Physically moving a material to affect the resonant frequency of a resonator is one method. This can be realized with a piezoelectric transducer and a slab of dielectric for room temperature applications or with a screw and high temperature superconducting (HTS) material to achieve high quality factor tunable filters at cryogenic temperatures. The other method of tuning a filter mechanically is with the use of MEMS capacitors and switches.

The first method to be investigated is that of piezoelectric transducer controlled tunable filters [14]-[16]. In this method of tuning, a dielectric slab can either be moved in the vertical direction above a microstrip filter, or be used to deform a conductive film to tune dielectric resonator filters or evanescent-mode cavity bandpass filters.

The position of the dielectric slab determines the effective permittivity of the structure and thus the response of the filter. This results in resonators having different resonant frequencies at different dielectric slab heights. The slab is moved by a piezoelectric transducer (PET), which is deflected by an applied voltage, as shown in Fig. 2-2.
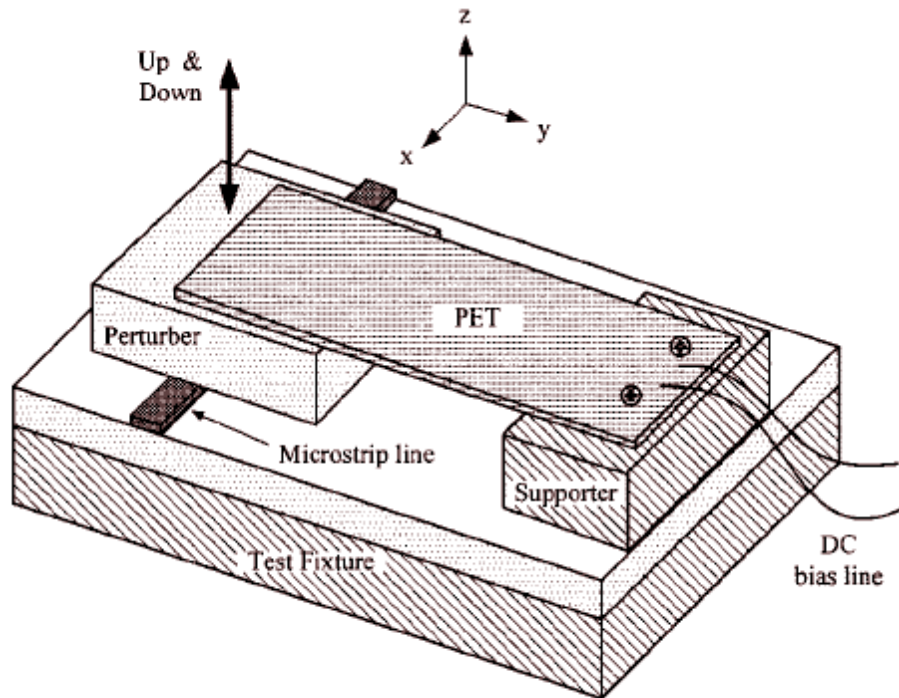
Fig. 2-2: Piezoelectric transducer controlled tunable filter [14].
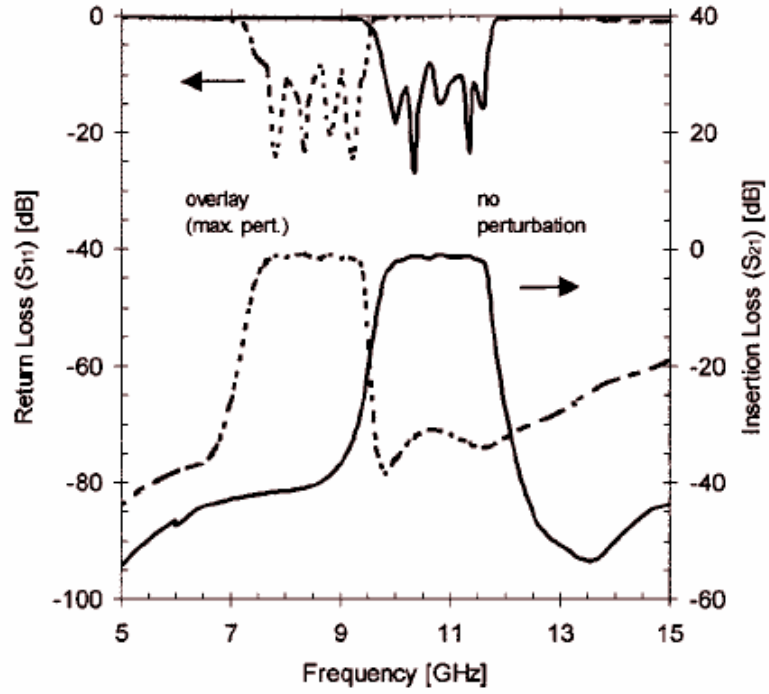
(a)
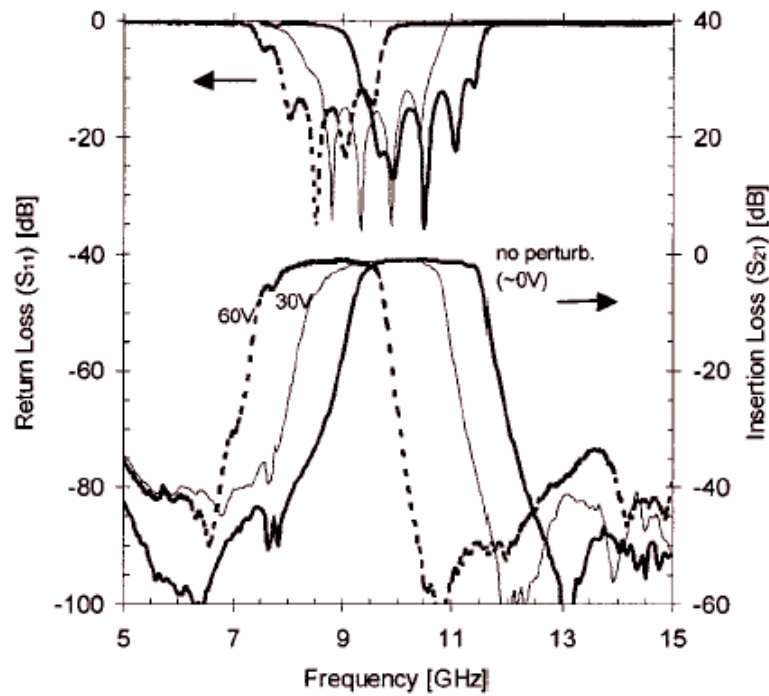
(b)

Fig. 2-3: a) Simulation and b) measured response for the PET controlled tunable filter [14].

The filter designed is that of a seven section parallel coupled filter, and the dielectric slab covers the entire microstrip filter. The simulated and measured responses are shown in Fig. 2-3 a) and Fig. 2-3 b). The simulated results give a tuning range of 24%, and the measured results give a tuning range of 17.5% [14]. Since the tuning range is realized by a moving slab of dielectric, the insertion loss over the tuning range is kept fairly constant. The insertion loss is also fairly low at ~2 dB compared to the other methods presented in this section.

Piezoelectric transducers have also been used in tunable dielectric resonator filters [15]. The piezoelectric transducers move a conductive film, which alters the resonant frequency of the TME mode of the dielectric resonator. This tuning process is shown in Fig. 2-4. By changing the voltage across the piezoelectric transducer from 0V to 180V, the center frequency of the fabricated 4-pole filter shifted from 5.22 GHz to 4.97 GHz and the bandwidth changed from 67 MHz to 65 MHz.
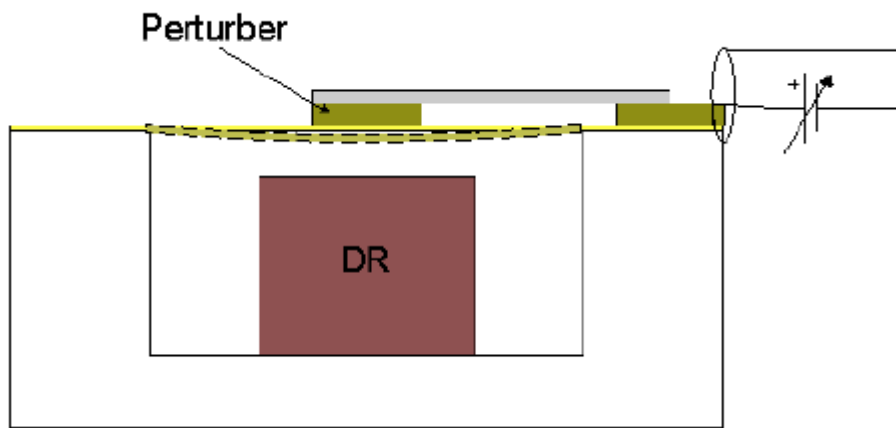
Fig. 2-4: Image of a dielectric resonator tuned with a piezoelectric transducer and a conductive film [15].

Another method of tuning filters by means of a mechanical system is with MEMS components. Generally the MEMS tunable filters are realized with MEMS switches or MEMS tunable capacitors, as shown in Fig. 2-5 a) and Fig. 2-5 b), respectively. The filters with MEMS switches have discrete values of center frequency, while the filters designed with tunable capacitors have a continuous response across the tuning range.
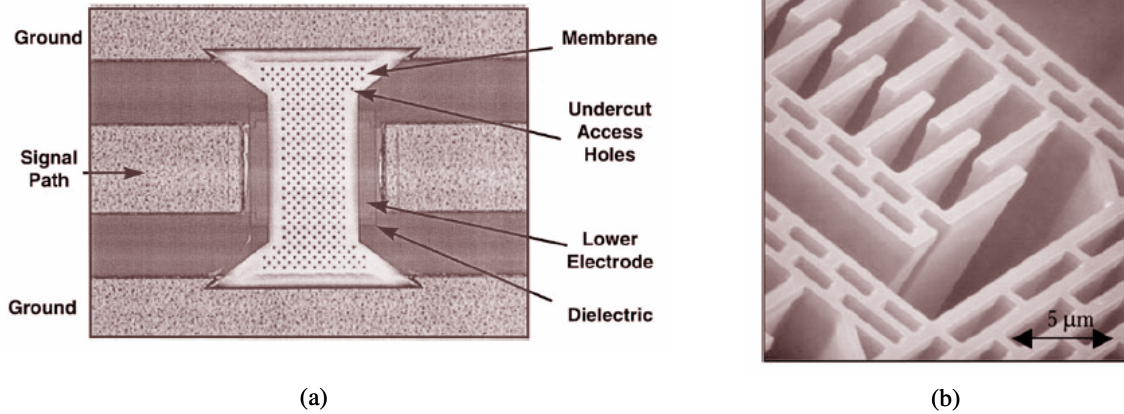
Fig. 2-5: a) Micrograph of a MEMS parallel-configured air-bridge switch [17], and b) SEM image of a MEMS tunable capacitor [18].

Two tunable filter designs are presented as examples of tunable filters with MEMS switches [19]-[20]. The first filter uses MEMS switches and a tunable inductor to get the two center frequencies of 15 GHz and 30 GHz [19]. For operation at a center frequency of 15 GHz, two MEMS switches are in the down position, and another MEMS switch is in the down position for operation at a center frequency of 30 GHz. This method of tuning filters is adequate only if discrete values of center frequency are needed in the design.

Another example of using MEMS switches for tunable filters, involves loading the end of interdigital quarter wavelength stubs with MEMS cantilevers [20]. The MEMS switch acts as a series capacitance between the quarter wavelength stub and the short open-ended transmission line, as shown in Fig. 2-6 a). Three MEMS cantilevers, as shown in Fig. 2-6 b), are used in parallel to ease the release process and to reduce the loss of the series capacitance. The filter is switched between a center frequency of 18.5 GHz with an insertion loss of 3.8 dB, a bandwidth of 2.4 GHz, and a return loss of 12 dB, and a center frequency of 21.05 GHz with an insertion loss of 3.5 dB, a bandwidth of 2.9 GHz, and a return loss of 15 dB.
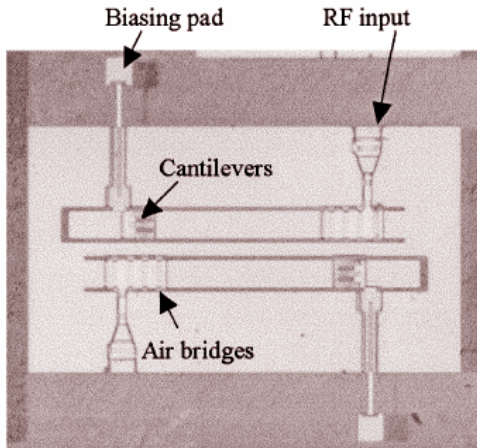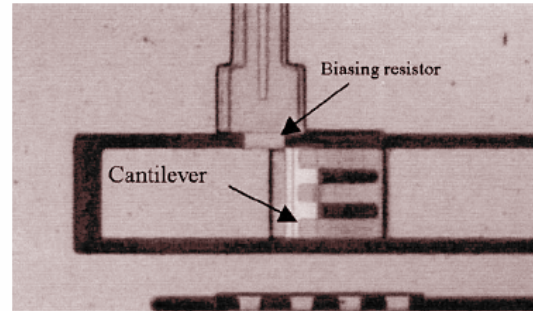
Fig. 2-6: a) Micrograph of the 2-pole filter using MEMS switches, and b) a micrograph of the three parallel MEMS switches [20].

The other method of tuning filters with MEMS components is with MEMS variable capacitors [21]-[23]. One of these examples shows the use of MEMS variable capacitors in a 2-pole lumped element filter and a 2-pole resonator filter [21]. The lumped element filter consists of lumped inductors with the tunable MEMS capacitors. The resonator filter uses MEMS variable capacitors at the end of half wavelength resonators to shift the center frequency.

The response of the lumped element filter is shown Fig. 2-7 a), and the response of the resonator filter is shown in Fig. 2-7 b). The tuning ranges of the two filters are 2.3% for the lumped element filter and 2.5% for the resonator filter. The insertion loss for the filters is 4.9 dB and 3.8 dB for the lumped element filter and the resonator filter, respectively. Also, the simulated unloaded Q of the resonator structure at 32 GHz, is 27.
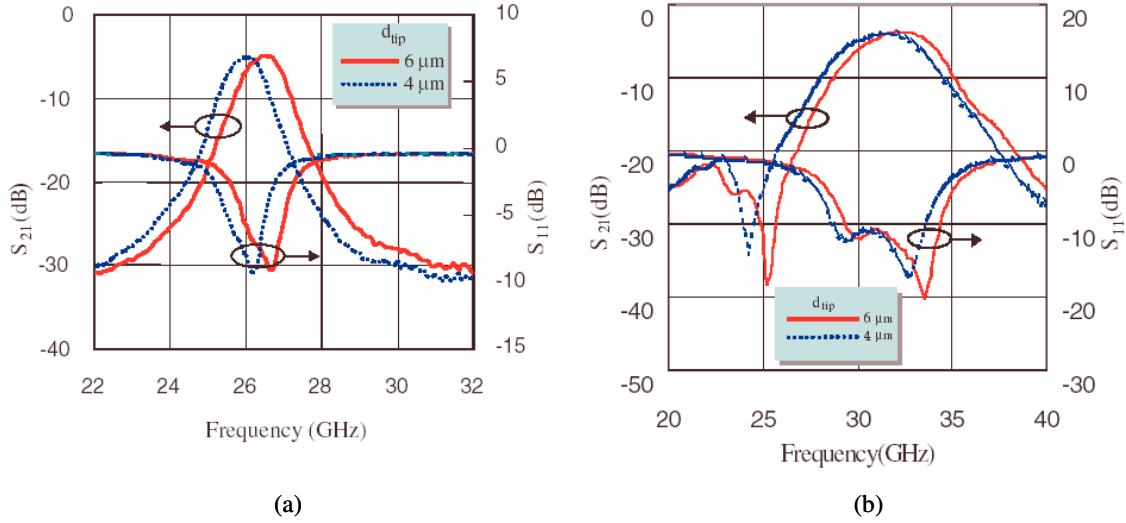
Fig. 2-7: Measured response of filters using MEMS tunable capacitor set up as a) a lumped element filter and b) a resonator filter [21].

Another method of incorporating MEMS tunable capacitors is to design a tunable filter with slow-wave MEMS resonators [22]. A 3-pole filter, as shown in Fig. 2-8 a), uses the slow-wave MEMS resonators for miniaturization and tunability. The loading of coplanar waveguide (CPW) transmission lines with MEMS bridges results in miniaturization by creating a slow-wave resonator with a high effective propagation constant and by lowering the required electrical length at resonance. The filter can be tuned across a range of center frequencies by changing the capacitance of the MEMS bridges. The tuning range of this filter is 18.6 GHz to 21.44 GHz, as shown in Fig. 2-8 b). The insertion loss ranges from 3.85 dB at a bias voltage of 0V to 4.15 dB at a bias voltage of 80V.

16
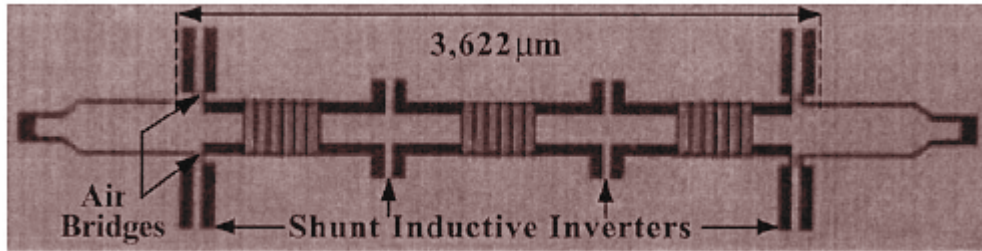
(a)
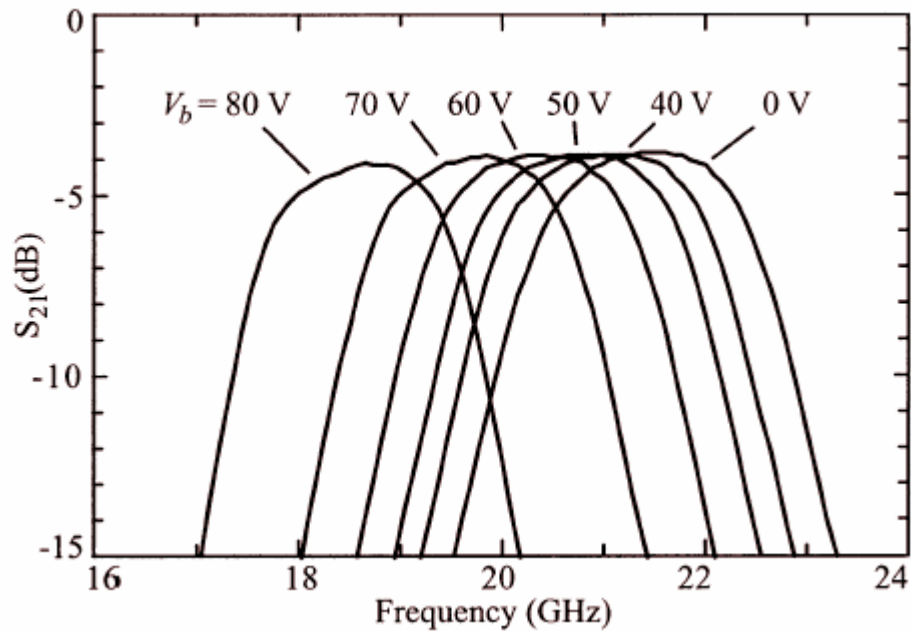
(b)

Fig. 2-8: a) 3-pole filter with slow-wave MEMS resonators, and b) the measured response of the filter at different bias voltages [22].

Another method to realize a tunable filter is to move tuning screws vertically above the resonators of a filter. One example of this method uses a piece of HTS material suspended above an HTS filter to get a high Q tunable filter [24]. A diagram of this tuning structure is shown in Fig. 2-9. Due to the need to move this entire HTS slab above the resonators of a filter, the tuning speed in restricted to the range of approximately 1 second [24].
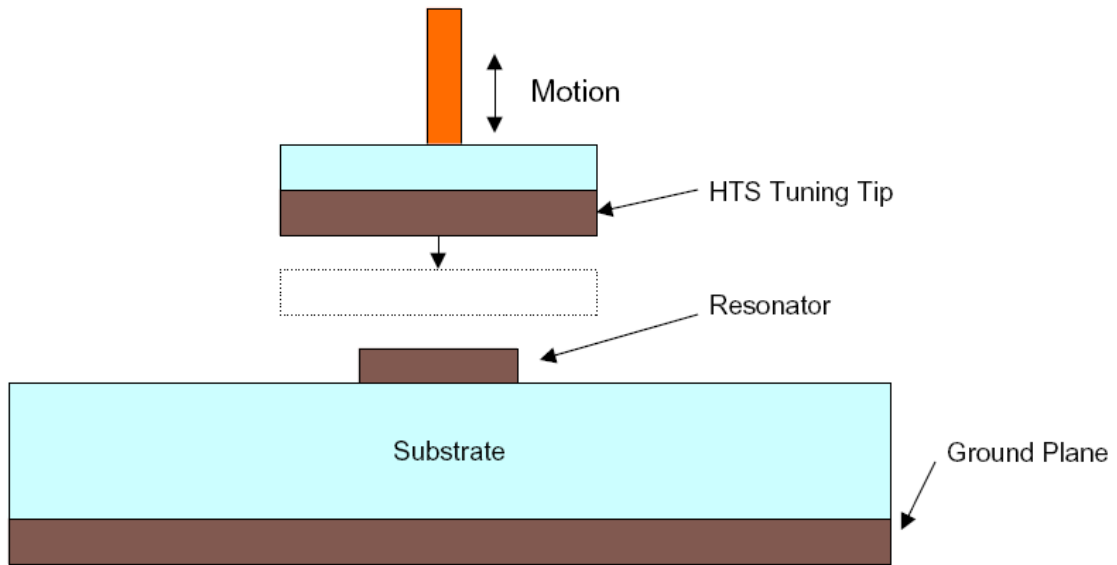
Fig. 2-9: Diagram of a mechanically tunable high Q filter [24].

2.1.3 Ferroelectric Materials

Ferroelectric materials can be used in tunable filters since the permittivity of the material changes with an applied DC electric field. An example of a microstrip line with a ferroelectric substrate is shown in Fig. 2-10. The tunable filter needs some element to deliver this external dc voltage, and this can be done with interdigital electrodes. The ferroelectric material and the dc electrodes can be placed wherever tuning is needed. The ferroelectric material and the substrate contribute to the effective permittivity of the microstrip structure. Changing the permittivity of the ferroelectric material results in tuning the filter as desired.
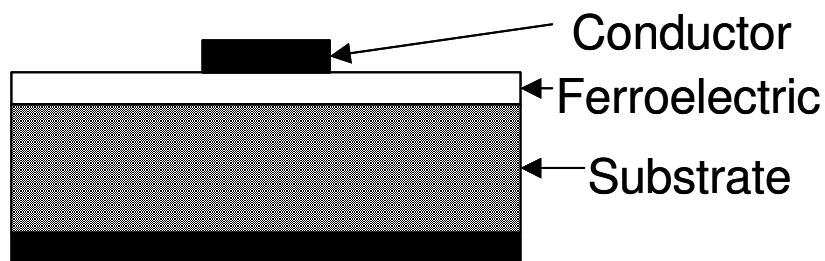
Fig. 2-10: A ferroelectric microstrip structure.

18

Two of the ferroelectric materials used in tunable filters are barium strontium titanate (BST), which can be used for room temperature applications, and strontium titanate, which can be used at cryogenic temperatures along with high-temperature superconductors.

Barium strontium titanate (BST or $(Ba_xSr_{1-x})TiO_3$) is used as a ferroelectric material with tuning filters at room temperature. BST variable capacitors can be implemented in tunable filters [25]-[26].

The BST capacitors are made by depositing a thin film with metalorganic chemical vapour deposition (MOCVD). The thin film is then covered with a deposited layer of metal making a parallel plate capacitor [25]. Lumped elements, including the BST variable capacitors, are used to realize the filter.

The tuning range of the filter is 45%, and the insertion loss is quite high at 7 dB. Only 2.5 dB of this loss is contributed to the BST capacitors and the remaining 4.5 dB is associated with the low Q inductors. At a frequency of 150 MHz, the quality factor of the 135 pF BST capacitor was found to be only 26.

A change in the fabrication process to improve the quality of the ground plane has increased the quality factor of the above BST capacitors by a factor of two [26]. The BST thin film is deposited at temperatures of about 700 °C within an environment composed of chemical precursors. Ground plane degradation can occur in this environment at these high temperatures. The single ground layer of platinum (Pt) is changed by alternating between platinum and IrO_2 layers, which promotes stability during the cooling process and improves the quality of the ground plane. The quality factor of the new capacitor with a capacitance of 65 pF at a frequency of 45 MHz is 63 [26].

Unlike the BST material, the strontium titanate (STO or $SrTiO_3$) ferroelectric material can be used at low temperatures, such as temperatures less than 77 K, and can be used in conjunction with high-temperature superconducting (HTS) material $YBa_2Cu_3O_{7-\delta}$ (YBCO) on a $LaAlO_3$ substrate. A lumped element HTS filter integrated with STO tunable capacitors using flip-chip technology is designed, as shown in Fig. 2-11 a) [27].

19

The differences between single crystal and thin film STO materials are discussed. The thin film materials have higher loss tangents and lower dielectric constants, but are easier to work with and are tunable at temperatures less than 77 Kelvin [27].

The achievable tuning range is approximately 1.3% at 77 Kelvin and 1.7% at 65 Kelvin, as shown in Fig. 2-11 b). This tuning range is lower than that of the other methods presented in this chapter, but the filter exhibited a relatively low insertion loss, as there is a trade-off between tuning range and insertion loss [27]. The achievable insertion loss is less than 1 dB over the tuning range.

Another example of a ferroelectric tunable filter using STO [28], incorporates the layers shown in Fig. 2-10 with a 254 μm thick LaO substrate, a conductor layer of YBCO 0.35 μm thick, a ferroelectric layer 0.3 μm thick, and a ground plane 2 μm in thickness. The layout of the 2-pole filter is shown in Fig. 2-12 a), and the measured response at 24 K is shown in Fig. 2-12 b). The dielectric constant of the STO layer can be varied from 300 to 3000 at a temperature of 77 K. The achievable tuning range of the filter is 14% at 24 K, and the insertion loss is only 1.5 dB at a bipolar bias voltage of ±200 V [28]. The bipolar biasing is achieved by connected nodes A and C of Fig. 2-12 a) to the positive bias and nodes B and D to the negative bias.

The STO capacitors have higher tuning speeds than other technologies and have tuning speeds similar in order to that of the varactor diode. Experiments are performed on the tuning speed of STO capacitors by sending video pulses at different rates through the capacitor [29]. The response time to the voltage bias is found to be less than 30 ns [29].

(a)

(b)
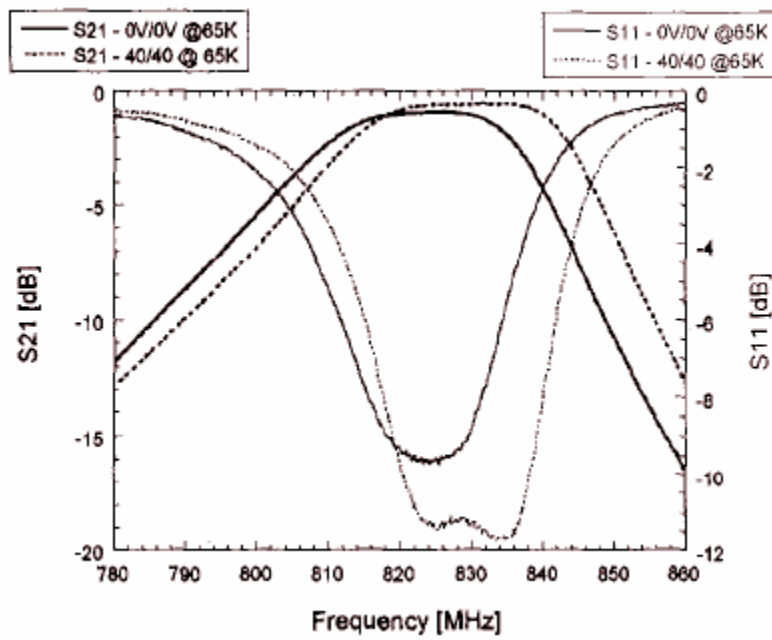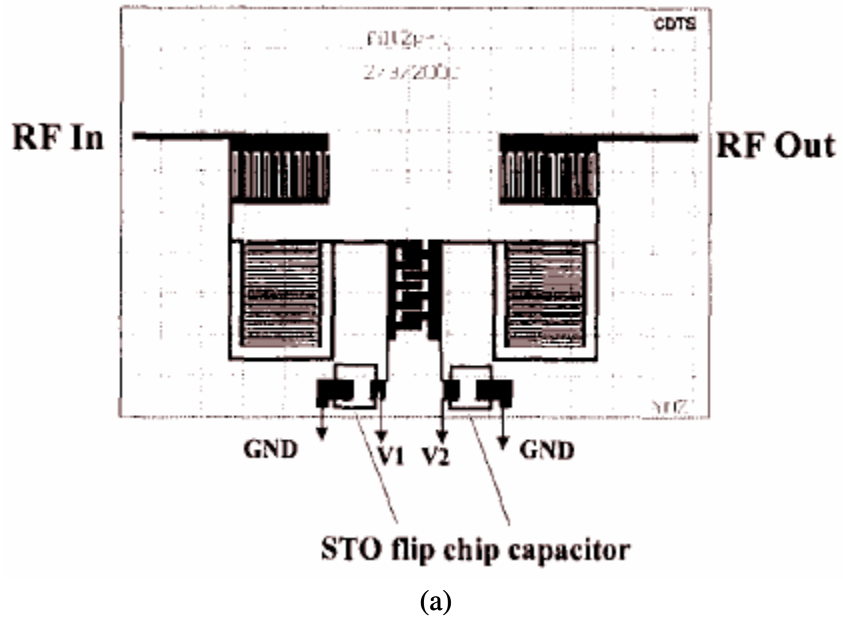
Fig. 2-11: a) Layout of STO tunable filter. b) Measured response of the STO tunable filter [27].
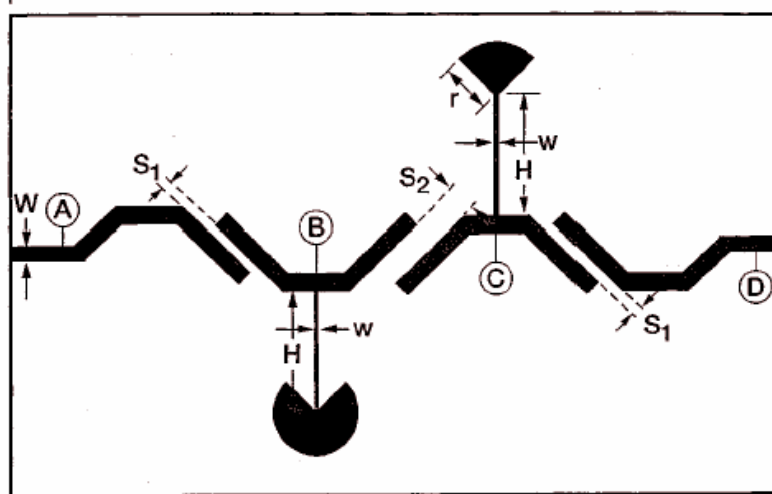
(a)
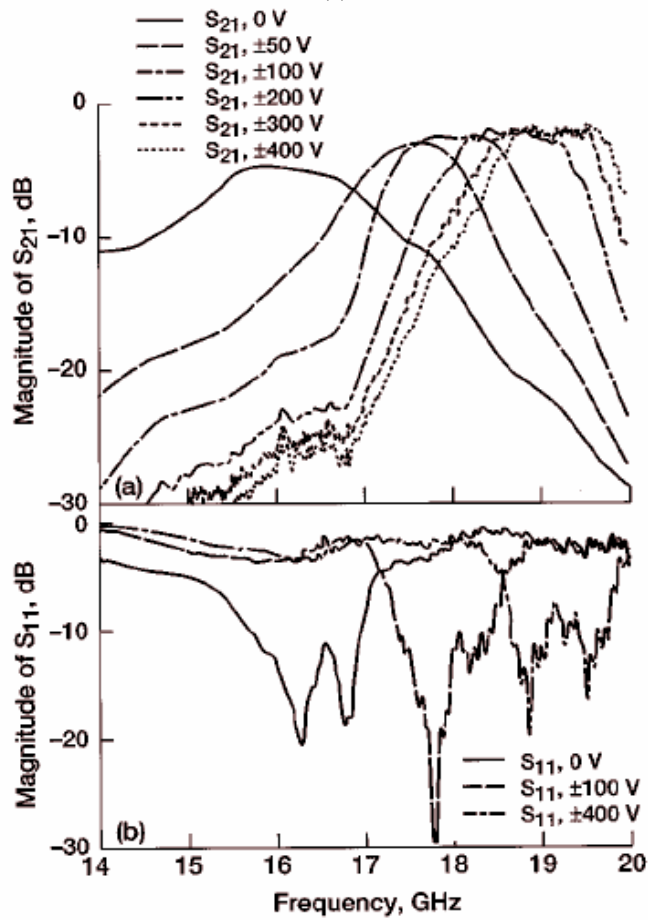
(b)

Fig. 2-12: a) Layout of 2-pole tunable STO filter, and b) the measured response at 24 K [28].

2.1.4 Ferrite Materials

The last method of tuning filters is with the use of ferrite materials. The tunable nature comes from applying an external DC magnetic field to change the effective permeability of the ferrite material. The first ferrite tunable filters implemented single-crystal yttrium iron garnet (YIG) tuning elements [30]-[32].

Both YIG spheres [30] and disks [31] have been used in two resonator filter structures. The single crystal YIG spheres, which were originally used, have a lowest resonant frequency of approximately 1.7 GHz, and lowering this resonant frequency is a desired objective. Doping the spheres with gallium decreases this resonant frequency to about 1 GHz, and the use of YIG disks decreases this further to 500 MHz for practical filters.

Other advancements have been made, such as using YIG spheres with microstrip resonators [32], implementing hexagonal ferrites which reduces the needed external magnetic field [33], and incorporating high temperature superconductors on single crystal YIG substrates [34].

A magnetostatic surface wave (MSSW) is excited by the quasi-TEM mode of the microstrip line [35]. To realize the tuning ability of the ferrite material, a DC magnetic field is applied in the direction perpendicular to the plane of the microstrip line. The value of this dc magnetic field affects the permeability of the YIG thin films. A YIG thin film is epitaxially grown on both sides of a gadolinium gallium garnet dielectric material and is sandwiched vertically between two slabs of dielectric. An air gap is introduced into the microstrip line to cut-off the quasi-TEM mode and to pass the MSSW mode. The tuning range seen by the response is ~5.6%, which is low as compared to the other methods of tuning presented in this chapter. The insertion loss in the passband is approximately 2.6 dB. Also there exists spurious response in the stop band with 20 dB of attenuation.

The tuning speed of YIG filters and MSSW filters are generally slower than the electrical methods of tuning. The tuning speed of these ferrites material filters is in the order of 0.5 to 2 ms [36].

2.1.5 A Comparison of Technologies

Table 2-1 presents a comparison of the different technologies reviewed in this section. The tuning speed, the tuning range, the power handling capability, and the insertion loss are considered when comparing the different technologies to realize tunable filters.

Table 2-1: Comparison of different technologies to realize tunable bandpass filters.

Parameter	Varactor tuned filter	Active filter	PET filter	MEMS tunable filter	STO	BST	YIG	MSW tunable filter
Tuning range	High	High	Medium	Low	Low	Medium	High	Low
Insertion loss	High	High	Low	Medium	Medium	High	Low	Medium
Tuning speed	ns	Ns	Ms	μs	ns	ns	ms	ms
Power handling	Low	Low	High	Low	Medium	Medium	Medium	Low

2.2 Tunable Filters with Constant Bandwidth

Tunable filter structures with improved constant bandwidth performance [37]-[39] are always being investigated. Since many tunable filters have only tuning elements for the center frequency and none for coupling, there is a need to design tunable filters with coupling that will not change at different center frequencies. The input coupling and the coupling between resonators both need to be considered.

One of these tunable filter structures is an improvement on the popular microstrip combline filter [37]. Step-impedances are introduced at the short-circuited end of the microstrip lines, as shown in Fig. 2-13, to keep a constant bandwidth across the tuning range. Unless longer electrical lengths of the microstrip lines are used for the resonators, these step-impedances are implemented to reduce the magnetic coupling near the short circuited ends of the microstrip lines and ensure a constant bandwidth across the tuning range.
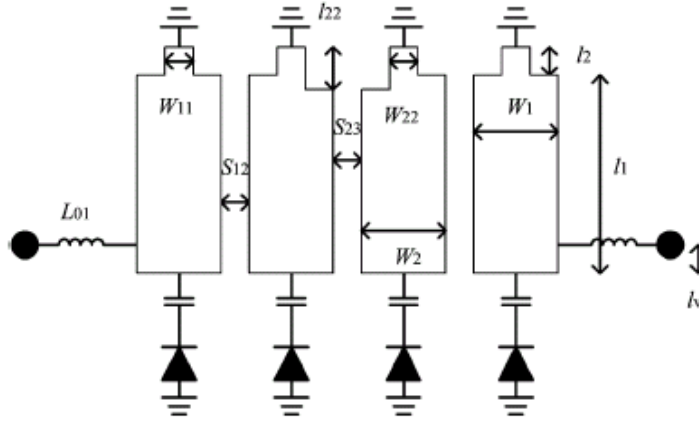
Fig. 2-13: Diagram of a tunable combline filter with step-impedance microstrip lines [37].
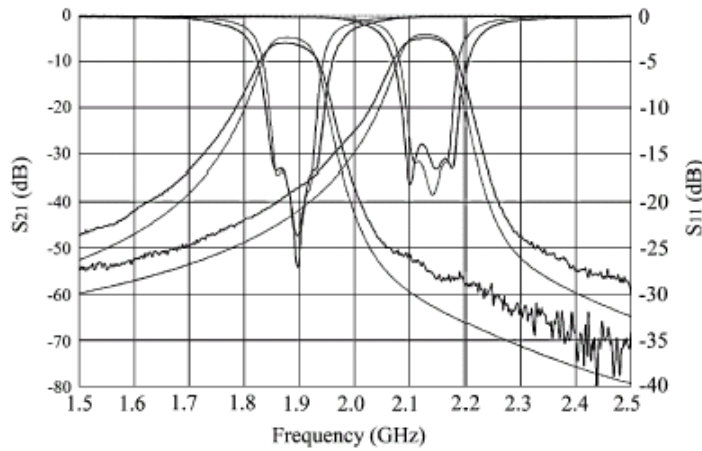
Fig. 2-14: Simulated (thinner lines) and measured (thicker lines) results of the tunable combline filter with step-impedance microstrip lines [37].

The inductance value and the placement of the input inductor determine the input coupling. This input structure allows the external Q to vary directly with the tuning frequency and thus allows for constant bandwidth. The measured and simulated results of this tunable combline filter with step-impedances are shown in Fig. 2-14.

Another structure includes an input coupling circuit to ensure a constant bandwidth across the tuning range [38]. An HTS two pole zig-zag hairpin-comb filter with a tunable capacitor, as shown in Fig. 2-15, is designed to have a constant bandwidth. The HTS tunable capacitor is realized by fabricating a long interdigital capacitor and permanently scribing

25

away parts of the capacitor to tune the capacitor to lower capacitance values. The input coupling circuit consists of a series inductor and capacitor circuit with magnetic coupling. This configuration reduces the effect of the input coupling varying differently with the tuning frequency. The measured results of this filter are shown in Fig. 2-16.
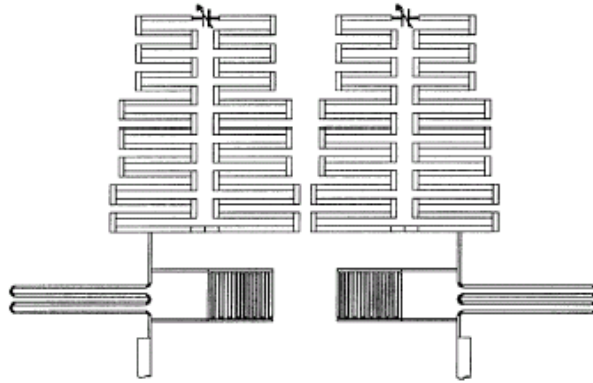
Fig. 2-15: The layout of the tunable two pole zig-zag hairpin-comb filter with constant bandwidth [38].
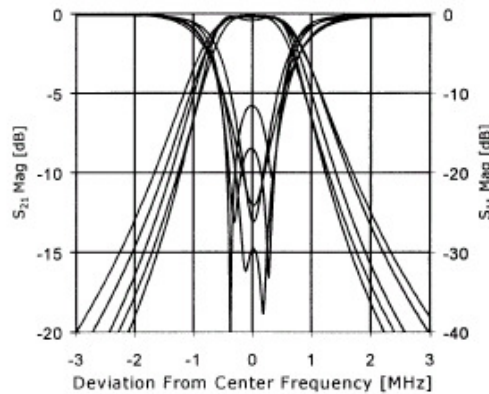
Fig. 2-16: Superposition of the measured results of the two pole zig-zag hairpin-comb filter for center frequencies of 0.498, 0.555, 0.634 0.754, and 0.948 GHz [38].

26

2.3 Fabrication of MEMS for Operation at Cryogenic Temperatures

2.3.1 Integration of HTS Circuits and MEMS Devices

There have been only a few publications regarding the fabrication of MEMS components for use with HTS circuits at cryogenic temperatures. The monolithic design and fabrication of a MEMS switch are presented in [40] and [41], respectively. A MEMS switch is made using the MUMPs® process to function at cryogenic temperatures [42]. A MEMS variable capacitor is also fabricated using a niobium-based process [46].
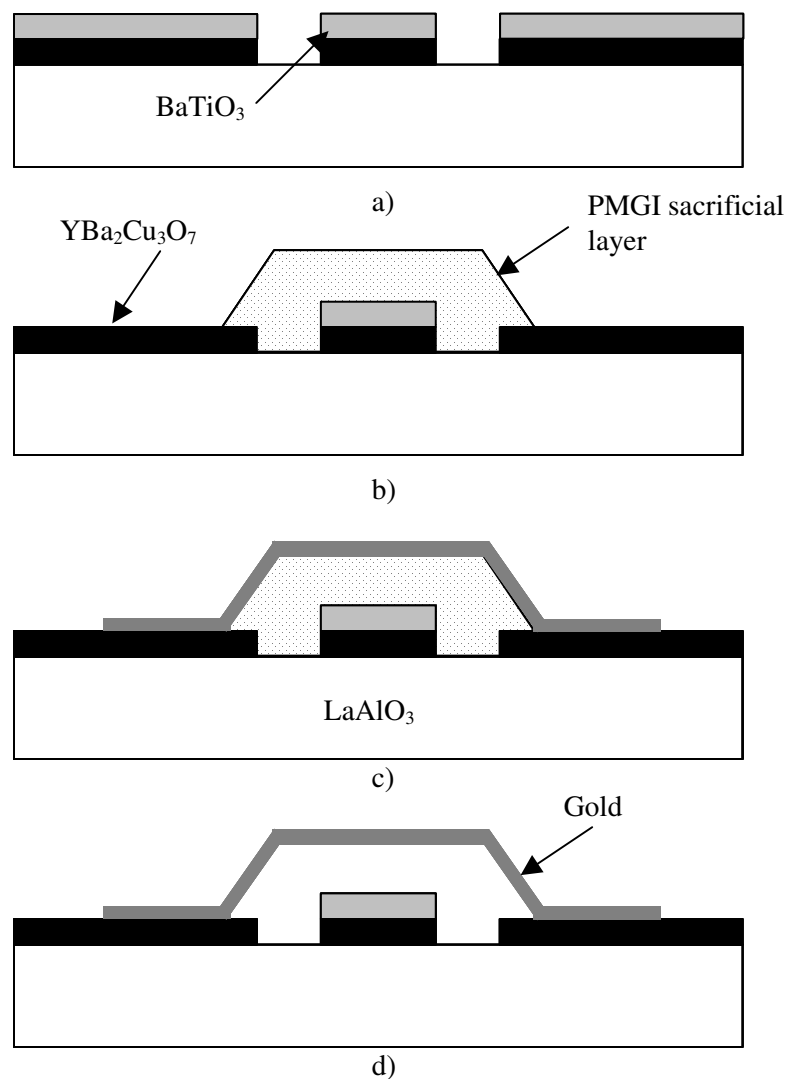
Fig. 2-17: MEMS shunt switch on an HTS transmission line [40].

The fabrication of the MEMS shunt switch on the HTS transmission line, as shown in Fig. 2-17 d), uses a four mask process [40]-[41]. There is one mask for each of the following: the coplanar waveguide transmission line, the $BaTiO_3$ insulating layer, the sacrificial layer under the gold bridge, and the gold bridge. The 0.3 μm thick $YBa_2Cu_3O_7$ layer is first deposited on a 15 mm × 15 mm $LaAlO_3$ substrate at a temperature of 760 °C using a pulsed laser deposition system. The insulating $BaTiO_3$ layer is then deposited using the same pulsed laser deposition system at 700 °C. This $BaTiO_3$ layer is 0.5 μm thick.

A positive photoresist is spun on the substrate, and it is patterned and developed using the coplanar waveguide mask. A 6 minute etch in 10% hydrofluoric acid (HF) removes the $BaTiO_3$ layer, and a 3 minute etch in 3% acetic acid removes the $YBa_2Cu_3O_7$ underneath the previously etched $BaTiO_3$ layer. The substrate is shown in Fig. 2-17 a) after the photoresist is removed. A positive photoresist is again spun on the substrate, and the $BaTiO_3$ insulating layer mask is patterned and developed. A 6 minute etch is also done with 10% HF to remove the $BaTiO_3$ and to leave the desired insulating patch on the center line of the coplanar waveguide as shown in Fig. 2-17 b).

The sacrificial layer of polymide (PMGI SF15) is spun on at a thickness of 3 μm and is baked at 200 °C for 15 minutes. An AZ5214 photoresist layer is spun on, patterned, and developed using the sacrificial layer mask. After the excess PMGI layer is removed the substrates appears as shown in Fig. 2-17 b). A dual layer of photoresist is spun on the substrate to ease the gold liftoff process. The gold deposition is performed by resistive heating evaporation of a tungsten filament. The deposited gold layer has a thickness of 0.15 μm to 0.3 μm. After the gold liftoff process, the substrate appears as shown in Fig. 2-17 c). An oxygen plasma-etch process removes the sacrificial layer and releases the gold bridge as shown in Fig. 2-17 d). The final switch and transmission line are shown in Fig. 2-18.
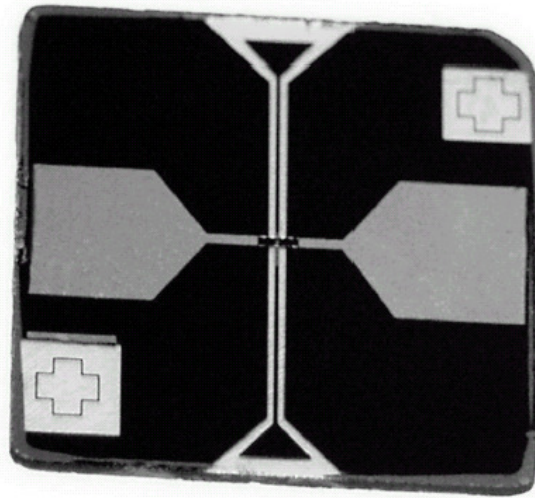
Fig. 2-18: Fabricated shunt switch on a coplanar waveguide transmission line [41].
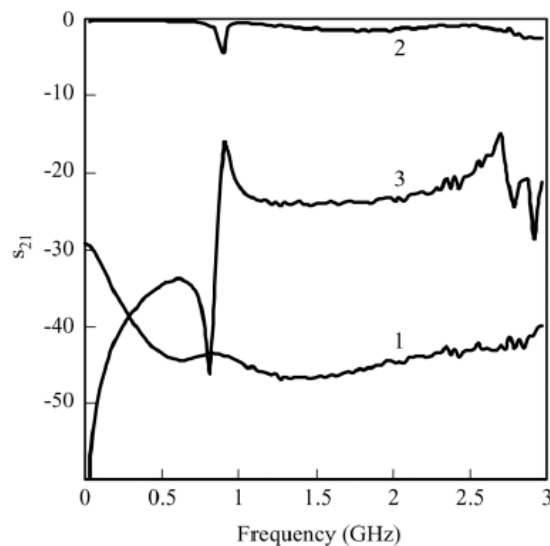
Fig. 2-19: Measured S_{21} results of the shunt switch 1) T = 300K 2) T=14K with the switch in the "up" position 3) T = 14K with the switch in the down position [41].

The design parameters of isolation capacitance (C_{ON}) and unactuated capacitance (C_{OFF}) are considered for this switch. The height of the gold bridge above the transmission line influences C_{OFF} of the switch. With a height of 3 μm, C_{OFF} is found to be 0.89 fF. The thickness and the dielectric constant of the insulating layer determine the value of C_{ON}.

29

With a BaTiO$_3$ thickness of 0.5 µm and dielectric constant of 300, the value of C$_{ON}$ is 159 pF. The measured S$_{21}$ results at a temperature of 14K in the up and down position are shown in Fig. 2-19.

A MEMS switch is designed and fabricated using the MUMPs$^{\circledR}$ process for use at cryogenic temperatures [42]. A cantilever beam is fabricated and is flip chipped onto a CPW transmission line. The beam forms a short from the center line of the CPW transmission line to ground through the solder ball used in the flip chip process. When the switch is in the "OFF" position an insertion loss of 0.8 dB up to 40 GHz is measured at room temperature. The isolation of the switch is measured at room temperature and at a temperature of 60K and is found to be approximately -13 dB from 20 to 40 GHz for both cases of temperature.

2.3.2 Modeling of MEMS Devices at Cryogenic Temperatures

The DC contact resistant of a MEMS contact switch is determined by many factors attributed to the physical, electrical and geometric properties of the switch itself. In [43], a contact MEMS switch is designed, fabricated and tested at cryogenic temperatures. The measured DC contact resistance was found to be much higher than a predicted resistance based solely on the conductivity of gold at cryogenic temperatures. This is in part due to thin adsorbed layers on the gold contacts and condensing nitrogen from the test setup. From the experiments, it was also found that as the switch was held down for enough time that the contact resistance would decrease. It is found that care must be taken in choosing a contact voltage whose subsequent current will remove thin surface films to decrease the contact resistance but will not soften the gold asperities to a point where adhesion failures can occur. The DC contact resistance changed from ~2 Ω at room temperature to ~1.7 Ω and ~1.35 Ω for two different cryogenic temperatures testing cycles [43]. The range of DC contact resistances given for very clean gold layers in [44] is 0.1 Ω to 1 Ω.

Another study was performed on the dc resistance of gold cantilever series switches at cryogenic temperatures [45]. A DC contact switch made of gold was fabricated and characterized at various levels of temperature, bias voltage, and DC through current. An increase in the actuation voltage was reported due to the increase in Young's modulus of the

gold and the upward bending deformation of the cantilever beam at cryogenic temperatures. It is believed that hardening of the gold at cryogenic temperatures is the cause of an additional ~0.2 dB of insertion loss. The insertion loss can be reduced at cryogenic temperatures by increase the bias voltage of the MEMS switch or by allowing a dc current to pass through the switch, which likely causes heating and softening of the gold. The insertion loss of the switch at a temperature of 1.6 K was similar to that when testing at a temperature of 4.2 K. There was more of an improvement in the insertion loss at 1.6 K than testing at 77K due to the increase in conductivity of the gold over that range temperatures [45].

2.3.3 Niobium Based MEMS Devices

A MEMS variable capacitor is also designed using a niobium based process [46]. Niobium is a metal that becomes superconducting below a temperature of approximately 9K. MEMS capacitors are fabricated and integrated with filter designs to create tunable filters. Simulation results of the tunable filters are reported.
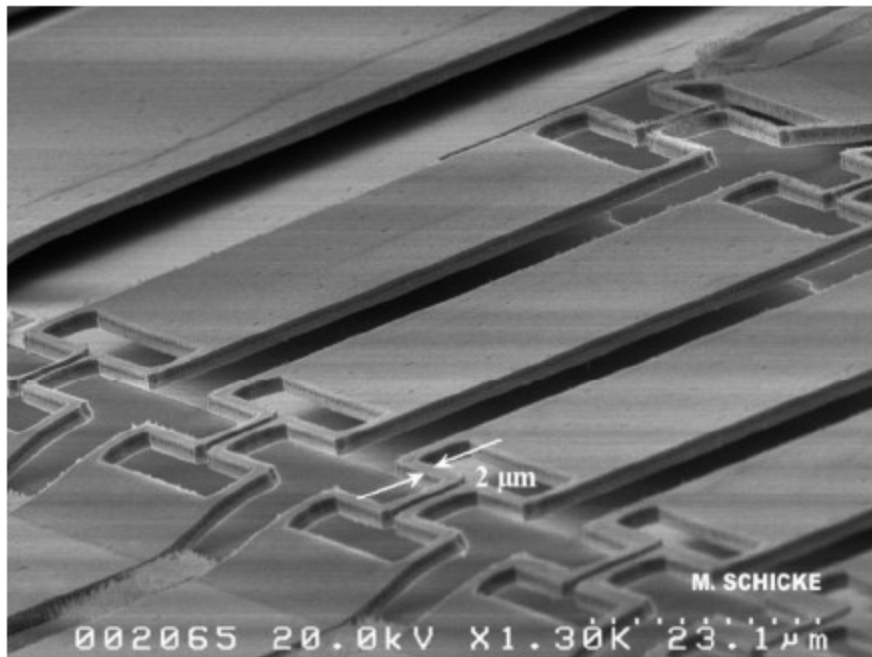
Fig. 2-20: An image of the fabricated niobium based MEMS capacitors [46].

The fabrication process uses niobium for the metal layers and photoresist as a sacrificial layer. The top niobium layer is 1.5 μm thick and the gap between the top and bottom plates is approximately 2.6 μm. The pull-in voltages for the capacitors range from ~25 V to ~50 V for different beam structures. The 0V capacitance of a 100 x 100 μm^2 capacitor is 33.5 fF, and the down state capacitance is approximately 50 fF. An image of the fabricated MEMS capacitors in shown in Fig. 2-20.

Chapter 3

Superconducting Filter Design and Implementation

There are several approaches reported in literature for accurate electromagnetic (EM) based design of microwave filters. The most direct approach is to combine an accurate EM simulation tool with an optimization software package to optimize the physical dimensions to the desired performance. This direct optimization approach however, is very computation intensive and is not practical for application in the design of large order filters. Over the past two decades more advanced techniques, such as the space mapping (SM) technique [47], the calibrated coarse model (CCM) technique [48] and many others, have been reported to help designers in achieving an accurate EM-based design with reasonable computation time. In particular, several publications have been reported on the space mapping technique and indeed the space mapping technique has emerged as the most useful approach for accurate EM-based design of microwave circuits.

However, in large order filters that make use of non-traditional compact resonator designs, such as the miniaturized microstrip filters employed in this chapter, the majority of the EM-based design techniques including space mapping and CCM fail to provide an accurate design. It is difficult to come up with an accurate coarse model due to the compact nature of the resonators.

We propose in this chapter to combine the EM model with a tuning technique to carry out the EM-based design process directly. The reflected group delay method [49] is well known as a technique for tuning fabricated filters. We propose to further develop this group delay method as a technique for designing filters to achieve EM simulation results as similar as possible to those of the ideal filter design. Since, it is well known that the accuracy of fabricated microwave filters is subject to the precision in its fabrication, differences in the measured results due to fabrication tolerances can be compensated by tuning with a method such as that described in [49].
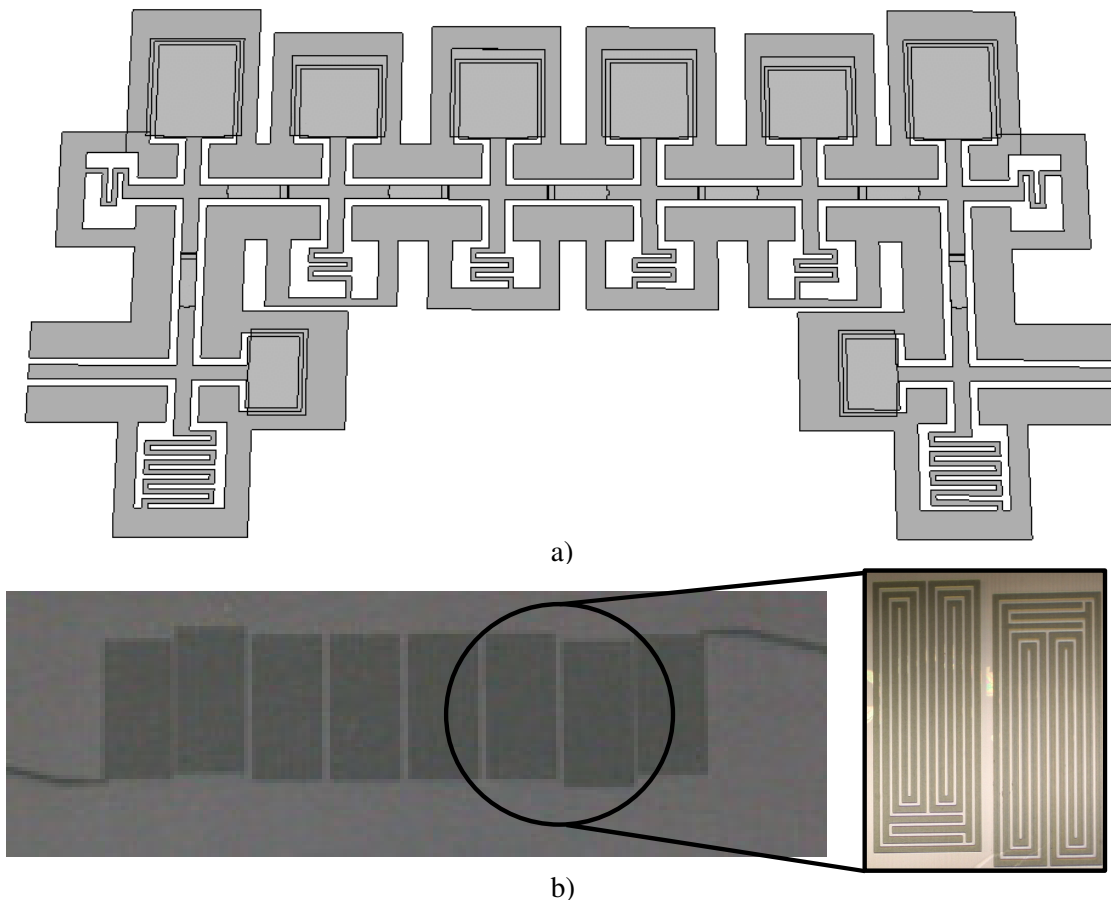
Fig. 3-1: a) An image of the 8-pole lumped element superconducting filter to be described in section 3.3 and b) an image of the fabricated 8-pole superconducting microstrip filter to be described in section 3.4.

The reflected group delay method of designing filters shows distinct advantages over other design techniques for many filter configurations. When using the reflected group delay method, the filter design process is divided into smaller design stages that each requires less computation and optimization time than that of designing the entire filter in one step. Each stage of the design process involves adding one more resonator to the EM simulation. Only a select few parameters need to be optimized, as the loading effects of the newly added resonator do not affect most of the parameters from the previous design stages for filter designs with limited cross couplings. When all design stages are complete the filter design is complete and no further optimization is needed. Also, the design method does not

34

require an accurate coarse model for the filter because all simulations are performed with an EM simulator.

The reflected group delay method is an excellent technique for designing superconducting and other high quality factor filters, and its effectiveness is shown through the design, fabrication and testing of two 8-pole superconducting filters. One filter, as shown in Fig. 3-1 a), is a highly miniaturized low-temperature superconducting lumped element filter. The second filter, as shown in Fig. 3-1 b), is a high-temperature superconducting microstrip filter incorporating compact resonators. The limited cross couplings inherit in the resonator designs of these filters lend to the use of the reflected group delay method.

The analysis of this filter design method starts in section 3.1 with the introduction of a correction factor that needs to be considered when designing higher order filters with larger bandwidths. The process is then demonstrated in section 3.2 with the design of a lumped element filter using a circuit simulator. Sections 3.3 and 3.4 show the design steps for the two 8-pole superconducting filters. Initial designs of these two superconducting filters are fabricated and tested. These initial designs are performed by making the group delay response of each design stage to be symmetric about the center frequency of the filter. It was determined after designing these two initial filters that the correction factor presented in section 3.1 was needed to get the ideal filter response. Comparisons of the simulation results are made between the initial designs and the final designs of sections 3.3 and 3.4.

3.1 Reflected Group Delay Method of Designing Filters

The reflected group delay method of designing and tuning filters was first published in [49]. The method uses the return loss group delay information to design or tune filters in incremental stages. At each stage of the filter design process, the parameters of the filters are optimized to match the ideal group delay response.

The group delay response can be fit to that of the ideal group delay response across the bandwidth of the filter, or the group delay response can be fit at the center frequency while

35

assuring that the response is symmetric about the center frequency. The latter method is mentioned in [49] as the method of designing and tuning filters.

The values at the center frequency to which the simulations should match are given in Table 3-1 for the first 4 resonators of a bandpass filter. The g_0 and g_1 terms are the Chebyshev low pass prototype values, f_2-f_1 is the bandwidth and f_0 is the center frequency. The group delay equation for the first resonator across all frequencies is given as

$$\Gamma_{d1}(f)=\left(\frac{2g_0g_1}{2\pi(f_2-f_1)}\right)\left(\frac{f^2+f_0^2}{f^2}\right)$$
$$\times\left(\frac{1}{1+(g_0g_1)^2\left[\frac{f_0}{f_2-f_1}\left(\frac{f}{f_0}-\frac{f_0}{f}\right)\right]^2}\right). \qquad (5.1)$$

The ideal group delay response, $\Gamma_d(f)$, of any stage of the filter design process is not a symmetric response. A correction, $A(f)$, is introduced in this thesis and is included in the symmetric group delay response, $\Gamma_{d\ symmetric}(f)$. This term is given as

$$\Gamma_{d\ symmetric}(f)=A(f)\,\Gamma_d(f). \qquad (5.2)$$

where

$$A(f)=\frac{2f^2}{f^2+f_0^2}. \qquad (5.3)$$

Table 3-1: Reflected group delay values at the center frequency of an inverter coupled bandpass filter [49].

Resonator number	Reflected Group Delay Value at f_0
1	$\Gamma_{d1}(f_0) = \dfrac{4g_0 g_1}{2\pi(f_2 - f_1)}$
2	$\Gamma_{d2}(f_0) = \dfrac{4g_2}{g_0 2\pi(f_2 - f_1)}$
3	$\Gamma_{d3}(f_0) = \dfrac{4g_0(g_1 + g_3)}{2\pi(f_2 - f_1)}$
4	$\Gamma_{d4}(f_0) = \dfrac{4(g_2 + g_4)}{g_0 2\pi(f_2 - f_1)}$

There are three terms on the right hand side of (1). The first term is a constant, and the third term is symmetric about the center frequency of the filter. The second term is not symmetric about f_0, so the correction factor $A(f)$ must be included. This symmetric group delay equation has the same value at the center frequency as $\Gamma_d(f)$ since $A(f)$ is equal to 1 at a frequency of f_0. Fig. 3-2 shows the group delay response and this new symmetric group delay response for the first two resonators of an 8-pole filter with a bandwidth of 35 MHz and a center frequency of 1.06 GHz. The group delay response in Fig. 3-2 is from

$$\Gamma_{d2}(f) = \left(\frac{2}{2\pi(f_2 - f_1)} \right)\left(\frac{f^2 + f_0^2}{f^2} \right)$$

$$\times \left(\frac{(f^1)^2 g_2 g_1 + 1}{(f^1)^2 g_2 g_0 + \dfrac{1}{g_2 g_0}\left((f^1)^2 g_2 g_1 - 1\right)^2} \right) \tag{5.4}$$

where

$$f^1 = \frac{f_0}{f_2 - f_1}\left(\frac{f}{f_0} - \frac{f_0}{f} \right). \tag{5.5}$$

37

There is a small deviation between the two curves as the frequency increases or decreases from f_0, as shown in Fig. 3-2. When using this reflected group delay method, the symmetric group delay response must be used when optimizing the filter response to meet a symmetric response, as the actual group delay response, $\Gamma_d(f)$, is not symmetric about the center frequency of the filter. This is especially important when designing higher order filters and filters with higher bandwidths. The filters designed in this thesis make use of the symmetric group delay response.
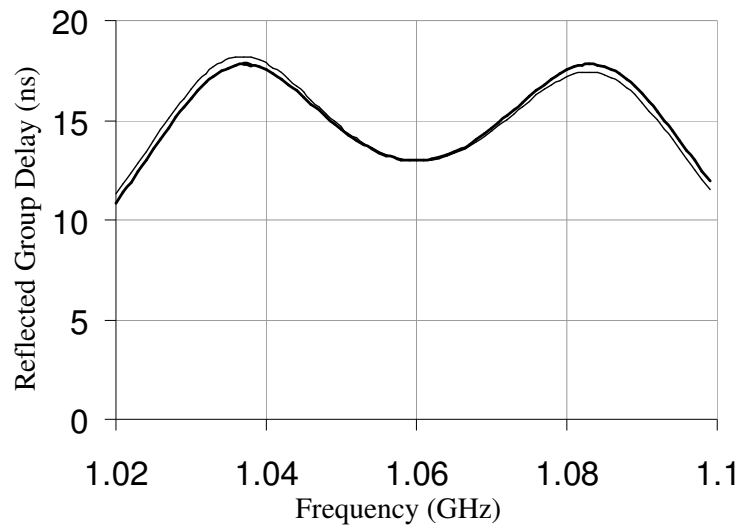
Fig. 3-2: The reflected group delay response, $\Gamma_d(f)$, (thin line) and symmetric reflected group delay response, $\Gamma_{d\,symmetric}(f)$, (bold line) of the first two resonators of an 8-pole filter.

3.2 Design of a Lumped Element 8-Pole Filter Using a Circuit Simulator

An 8-pole lumped element filter is designed using a circuit simulator with ideal capacitors and inductors to demonstrate the reflected group delay design method. The values of the inductors and the capacitors are given at each design stage. The frequency response of the final filter design matches closely with the expected ideal response for an 8-pole filter.

A bandpass transformation can be performed on a low-pass prototype filter to replace the shunt capacitors with shunt capacitors and inductors and the series inductors with series capacitors and inductors. Also, the series resonators can be replaced with shunt resonators

with the addition of impedance inverter pi-networks consisting of series capacitors and two shunt capacitors with a negative value of capacitance.

For small values of bandwidth, the value of the capacitor that makes up the resonators can be quite high. To reduce the value of this capacitor, an inductor can be placed in series with the capacitor. This series inductor also adds a transmission zeros at the resonant frequency of this inductor and the capacitors (or L_{12} and C_{11} as shown in Fig. 3-3). This is the circuit that is used to demonstrate the reflected group delay method and an image of it is shown in Fig. 3-3. The values of the capacitors are reduced to values that can easily be realized in a filter design such as the one presented in section 3.1.
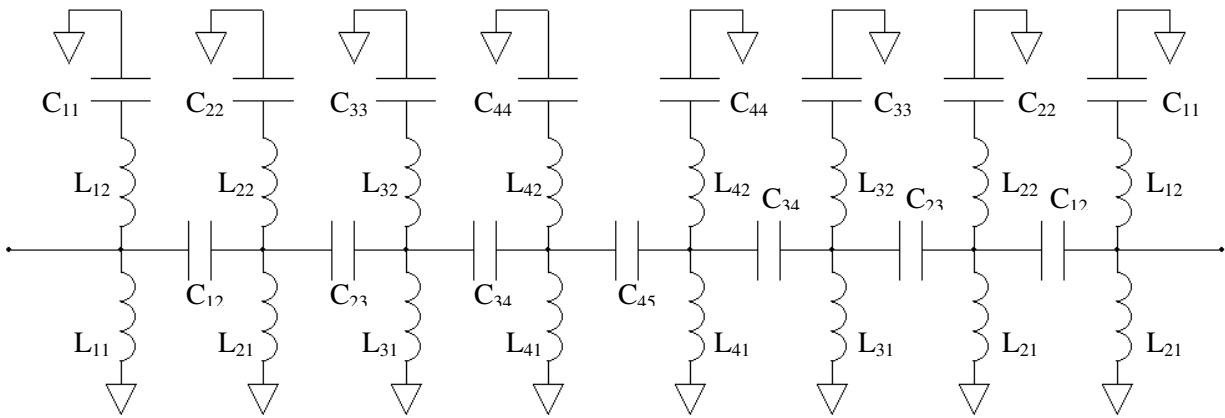
Fig. 3-3: Image of the lumped element 8-pole filter used to demonstrate the design process.

This circuit could be solved mathematically to determine the correct values of the capacitors and inductors for a given center frequency, bandwidth, and return loss, but the reflected group delay design method allows for the design of such a filter without the need for a set of equations fully characterizing the circuit. This is the case when designing most microwave filters. For this filter design, the center frequency is 1.06 GHz, the bandwidth is 35 MHz, and the return loss is chosen to be 25 dB.

From Table 3-1, the values of the reflected group delay at f_0 for the different design stages are Γ_{d1} = 15.39 ns, Γ_{d2} = 25.95 ns, Γ_{d3} = 48.43 ns, and Γ_{d4} = 56.58 ns. To determine the values of

the capacitor and the inductors of the first resonator, only L_{11}, L_{21}, and C_{11} are included in the circuit simulations. Optimization is performed until the reflected group delay has the correct peak value at the center frequency of the filter. The values of the elements are found to be C_{11} = 35.00 pF, L_{12} = 0.2097 nH and L_{11} = 0.4346 nH and are listed in Table 3-2. The group delay response for this first stage of design is shown in Fig. 3-4.
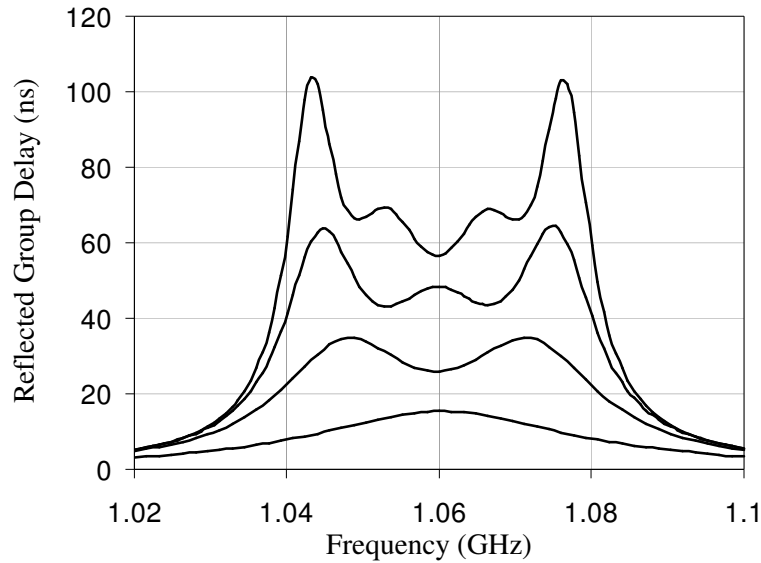
Fig. 3-4: Symmetric reflected group delay response for each stage of the 8-pole lumped element filter design. The response with the lowest value of group delay and one maximum at 1.06 GHz is for the design of the first resonator. The response for the second, third and fourth resonators have increasing values of group delay at f_0.

The values of the rest of the inductors are chosen to be equal to those of the first resonator, so $L_{11} = L_{22} = L_{33} = L_{44}$ = 0.4346 nH and $L_{12} = L_{22} = L_{32} = L_{42}$ = 0.2097 nH. For the following stages of the design, only the values of the capacitors are optimized. For the remaining stages of the design process, the capacitors are optimized so the symmetric group delay response is symmetric about the center frequency with the desired value at the center frequency.
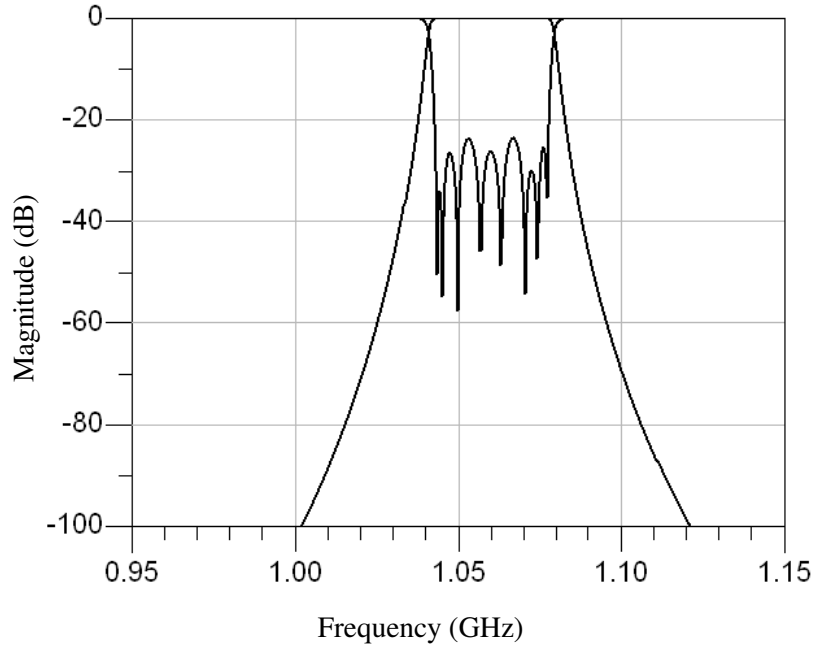
Fig. 3-5: Circuit simulation results of the 8-pole lumped element filter designed with the reflected group delay method.

Table 3-2: Values in (pF) of the capacitors after optimizing each resonator of the 8-pole lumped element filter.

Capacitor	Resonator 1	Resonator 2	Resonator 3	Resonator 4	Full Filter
C_{11}	**35.00**	**33.97**	33.97	33.97	33.97
C_{12}		2.2805	2.2805	2.2805	2.2805
C_{22}		**33.97**	**33.24**	33.24	33.24
C_{23}			1.5311	1.5311	1.5311
C_{33}			**34.30**	**33.65**	33.65
C_{34}				1.406	1.406
C_{44}				**34.37**	**33.71**
C_{45}					1.39

41

During the second stage of optimization, the elements C_{12}, C_{22}, L_{21}, and L_{22} are added to the circuit. The optimized values of the capacitors are found to be C_{11} = 33.97 pF, C_{12} = 2.2805 pF and C_{22} = 33.97 pF. The value of C_{11} has been reduced due to the loading effects of the second resonator. The plot of the symmetric group delay response is shown in Fig. 3-4.

The process is repeated for the third and fourth resonators. The values of the capacitors are listed in Table 3-2. When optimizing the Nth resonator, only C_{N-1N-1}, C_{NN}, and C_{N-1N} need to be changed, and C_{N-1N-1} is always reduced. To determine the value of C_{45}, the entire circuit as shown in Fig. 3-3 is simulated, and the values of C_{45} and C_{44} are optimized. The final values of all the capacitors are listed in Table 3-2, and the frequency response is shown in Fig. 3-5. These simulation results are close to the response of an ideal 8-pole Chebyshev filter with a return loss of 25 dB.

The design of this ideal lumped element filter demonstrates the reflected group delay filter design process. This process is used to design a lumped element superconducting filter and a microstrip superconducting filter in the next two sections.

3.3 Design of an 8-Pole Lumped Element Superconducting Filter

An 8-pole lumped element superconducting filter, based on the design from [50], is designed with the reflected group delay method. Even though this filter is made up of lumped elements, which should produce very little cross-couplings, it is difficult to model the effects of connecting the lumped elements closely together with the coplanar waveguide (CPW) transmission lines. By using the reflected group delay method to design a filter of this type, a designer does not need to accurately model the small parasitic effects of the connecting CPW transmission lines because they are included in the overall impedances and thus reflected group delay response of the resonators and coupling capacitors.

The filter has a center frequency of 1.158 GHz and an absolute bandwidth of 112.5 MHz. The filter is fabricated with a 10 layer niobium based multilayer process. The 10 layers are made up of four niobium layers, a resistive layer, silicon dioxide insulating layers and a gold based layer for contact pads. The fabricated filter is packaged in a housing and reaches

a superconducting state when immersed in liquid helium, as niobium has a superconducting transition temperature of approximately 9.3 K.

Table 3-3: Lengths (in micrometers) of parameters after optimizing each resonator of the 8-pole lumped element superconducting filter

Parameter	Resonator 1	Resonator 2	Resonator 3	Resonator 4	Full Filter
L_{C1_1}	**220**	**185**	185	185	185
L_{C1_2}	**10**	**0**	0	0	0
L_{L1_1}	265	265	265	265	265
L_{L1_2}	80	80	80	80	80
L_{C2_1}		**440**	**415**	415	415
L_{C2_2}		**200**	**170**	170	170
L_{L2_1}		165	165	165	165
L_{L2_2}		65	65	65	65
L_{C3_1}			**350**	**325**	325
L_{C3_2}			**180**	**0**	0
L_{L3_1}			165	165	165
L_{L3_2}			75	75	75
L_{C4_1}				**395**	**375**
L_{C4_2}				**70**	**70**
L_{L4_1}				**165**	**165**
L_{L4_2}				**15**	**10**

The lumped element resonators are composed of a shunt capacitor and a shunt inductor. The coupling between resonators is realized by series capacitors. These series capacitors act as impedance inverters and allow for all resonators to be in shunt form. The series capacitors have a simulated capacitance of 3.48 pF when modeled with an EM simulator. The ratio of the inductance to the capacitance for each resonator and the value of the series

capacitor accounts for the correct bandwidth and return loss of the filter. The impedance inverter can be modeled by a Π-network with a series capacitance and shunt capacitors with negative capacitance.
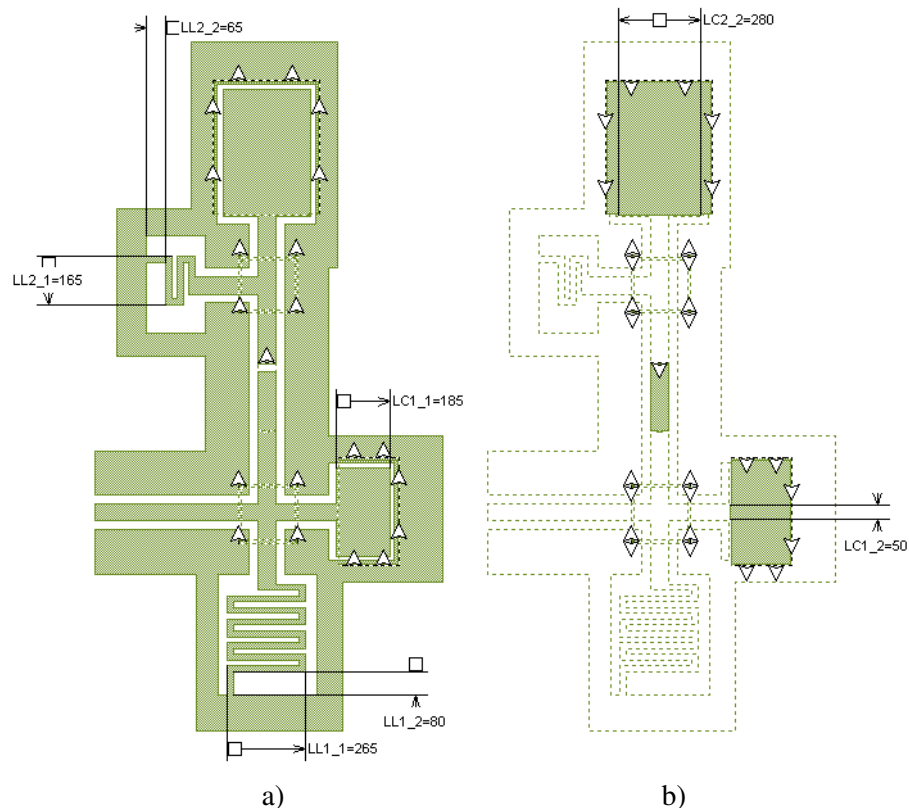
Fig. 3-6: Image of a) the bottom metal layer and b) the top metal layer of the capacitors of the first two resonators during the design process.

The capacitors and inductors have dimensions that can be adjusted for coarse tuning and fine tuning. When designing the first resonator, the coarse and fine tuning parameters for C_1 and L_1 are optimized with the EM simulator Sonnet. The coarse and fine length parameters for the capacitor are L_{C1_1} and L_{C1_2}, respectively. The inductor has L_{L1_1} and L_{L1_2} as coarse and fine length parameters. The values of these parameters are listed in Table 3-3 for the first design stage.
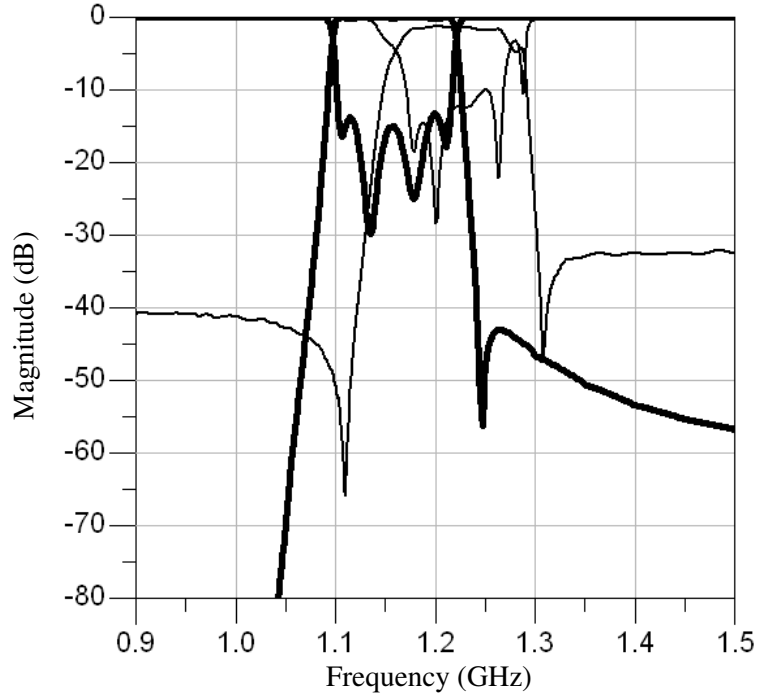
Fig. 3-7: EM simulation results (bold line) and test results (thin line) of an initial design of the 8-pole lumped element superconducting filter.

During the design stage for the second resonator, the parameters for C_1, C_2, and L_2 are optimized. The parameters for L_1 are left unchanged during this design stage and for the remaining design stages. A similar process is performed when determining the parameters for the third and fourth resonators. When performing the design process for the Nth resonator, L_{LN_1}, L_{LN_2}, L_{CN_1}, L_{CN_2}, $L_{C(N-1)\_1}$, and $L_{C(N-1)\_2}$ are adjusted.

An image of the first two resonators is shown in Fig. 3-6. The fine and coarse parameters for the capacitors and inductors are shown for these first two resonators. The third and fourth resonators have similar parameters. When optimizing the final values of L_{C4_1}, L_{C4_2} and L_{C45}, the full filter is simulated and a regular s-parameter optimization is performed to match the bandwidth and the return loss characteristics of the filter. The length of the series coupling capacitor and the parameters associated with L_4 and C_4, which are given in Table 3-3, are optimized to achieve the desired response. The final simulated value of the series capacitor C_{45} is 3.83 pF. An image of the final designed filter is shown in Fig. 3-1 a).
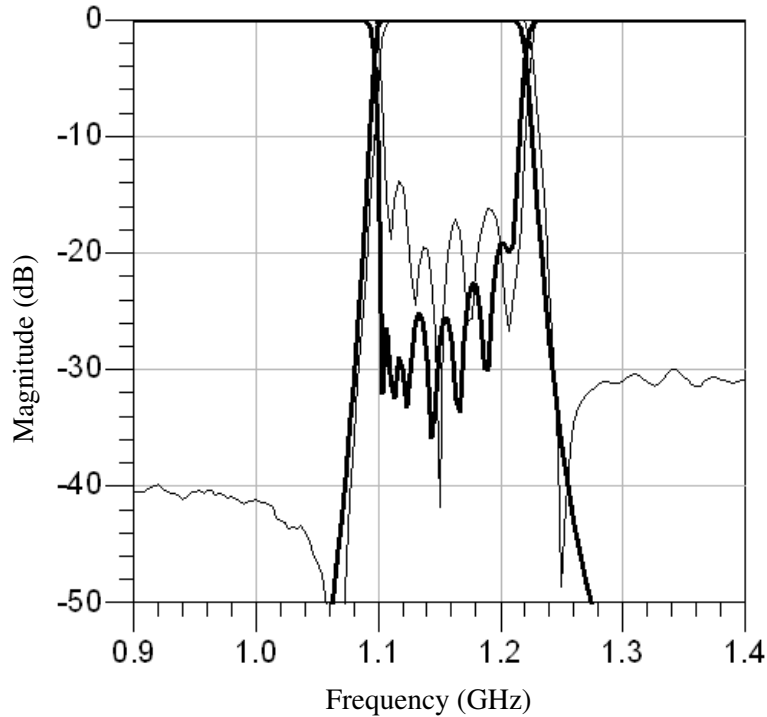
Fig. 3-8: EM simulation results (bold) and measured results (thin) of the 8-pole lumped element superconducting filter designed with the reflected group delay method.

An initial version of the filter was designed without the correction factor presented in section 3.1, and its EM simulations results and test results are shown in Fig. 3-7. By performing the step by step design method, the best return loss achieved was approximately 15 dB. This initial filter was fabricated and tested. To improve the return loss of the initial design, further optimization would need to be performed. The filter, whose final dimensions are given in Table 3-3, was then designed using the reflected group delay method with the correction factor. The EM simulation results and measured results of this filter are shown in Fig. 3-8. The return loss of the final filter design is lower across the passband of the filter. The position of the transmission zeros for this filter design are functions of the values of the input coupling.

3.4 Design of an 8-pole Microstrip HTS Filter

The reflected group delay method is demonstrated with the design of an 8-pole high temperature superconducting (HTS) microstrip filter. It is advantageous to implement the

reflected group delay method for this filter design due to the use of a non-traditional resonator design. The dimensions of the filter are given for each stage of the filter design. An initial version of the filter is fabricated and the test results are shown.

The resonators of the 8-pole filter are based on the compact resonators presented in [51]. For the filter design in this chapter, every other resonator is flipped to achieve the higher coupling needed for the higher percentage bandwidth. The filter has a center frequency of 1.158 GHz, an absolute bandwidth of 112.5 MHz and a relative bandwidth of 9.7%. A 508 µm thick substrate of LaAlO$_3$ coated with 600 nm YBCO is used to fabricate this filter design. After the wafer is processed and diced, the microstrip filter is mounted in a housing with coaxial cable connectors. The filter is then tested in a custom cryocooler at a temperature of 77 K.

To achieve the correct input coupling for the filter design, a tap coupling is made to the first resonator. The correct coupling between resonators is attained by the appropriate spacing between the resonators. Since the EM simulator Sonnet, which is used for this design, restricts the mesh to a grid, the spacing between resonators is adjusted in both the *x*-direction and the *y*-direction. Changing the spacing in the x-direction makes a coarse adjustment in the coupling, and changing the spacing in the y-direction accounts for a fine adjustment in the coupling.
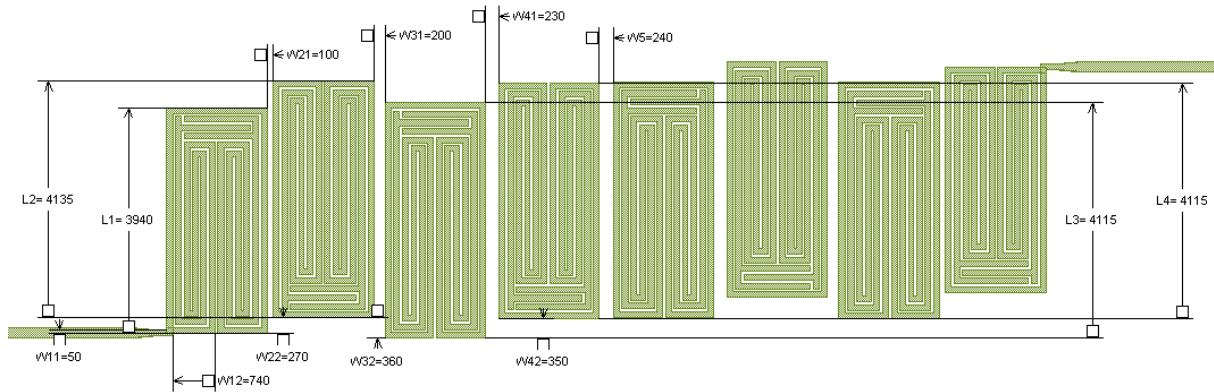
Fig. 3-9: Layout with the final dimensions in µm for the 8-pole HTS filter.

The steps taken to design this filter are the same as those presented in section 3.2. The input transmission line and the first resonator are simulated. The parameters of the first resonator are tuned until the symmetric reflected group delay matches the desired value at the center frequency as determined by Table 3-1. For this step, the parameters are $W_{11} = 50$ μm, $W_{12} = 740$ μm and $L_1 = 3990$ μm. An image of the final designed filter is shown in Fig. 3-9.

The second resonator is then added to the layout in the EM simulator and the parameters are optimized to achieve the desired value of reflected group delay at the center frequency while having a symmetric group delay response about the center frequency of the filter. The parameters associated with the second resonator, W_{21}, W_{22} and L_2, are optimized in conjunction with L_1 in this design stage. The value of L_1 needs to be changed to account for the loading due to the addition of the second resonator. The values of W_{11} and W_{12} remain unchanged and will do so for the remainder of the filter design process. The parameters for the filter are given in Table 3-4 for each step of the design process.

A similar process is performed for the third and fourth resonator. For this filter, only four parameters, L_n, L_{n-1}, W_{n1} and W_{n2}, are adjusted at each stage of the filter design process. This reduces the complexity of the optimizing process. To determine the final values for L_4 and W_5, the entire filter, as shown in Fig. 3-9, is simulated and optimized to meet the return loss and bandwidth specifications of the filter.

An initial version of the filter, as shown in Fig. 3-1 b), was designed, fabricated and tested and its EM simulation results and test results are shown in Fig. 3-10. The return loss of the EM simulation results is higher than desired for this initial design because the correction factor presented in section 3.1 was not used. The final lossless EM simulation results for the filter whose parameters are listed in Table 3-4 are shown in Fig. 3-11. The return loss of this filter is below 20 dB over the band of the filter. The measured results of Fig. 3-10 show similar return loss passband characteristics, though the center frequency is shifted down from that of the simulation results due to tolerances in the fabrication process and to the temperature dependence of the frequency response associated with HTS filters. The

rejection of this type of filter has been found to be 75 dB in fabricated filters [51], so the less than ideal rejection is likely due to aspects of the fabrication and assembly of this particular filter. The transmission zeros of this filter design are attributed to the tap coupling at the input to the filter.

Table 3-4: Values (in micrometers) of parameters after optimizing each resonator of the 8-pole HTS filter

Parameter	Resonator 1	Resonator 2	Resonator 3	Resonator 4	Full Filter
W_{11}	50	50	50	50	50
W_{12}	740	740	740	740	740
L_1	**3990**	**3940**	3940	3940	3940
W_{21}		100	100	100	100
W_{22}		270	270	270	270
L_2		**4160**	**4135**	4135	4135
W_{31}			200	200	200
W_{32}			360	360	360
L_3			**4130**	**4115**	4115
W_{41}				230	230
W_{42}				350	350
L_4				**4125**	**4115**
W_5					240
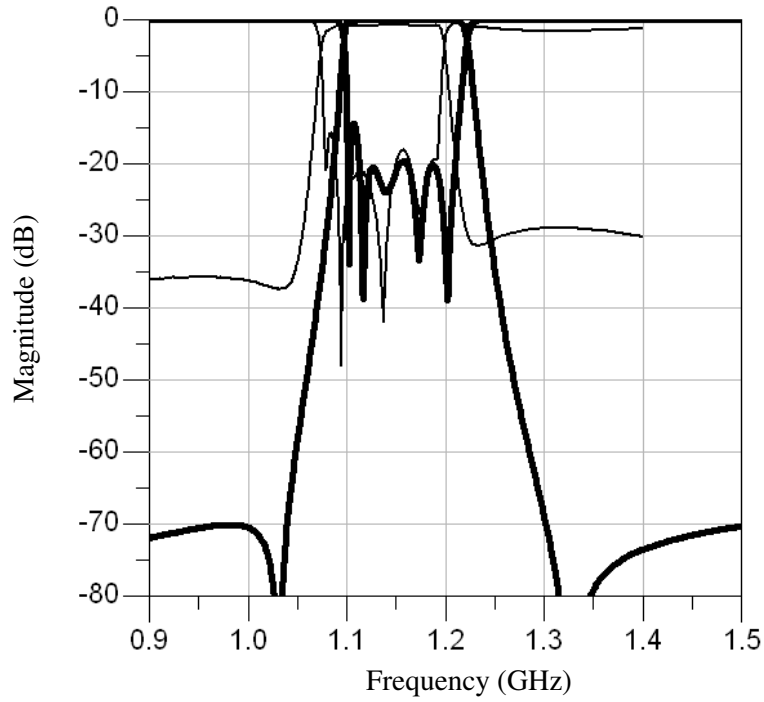
Fig. 3-10: Lossless EM simulations (bold line) and measured results (thin line) of an initial design for the 8-pole high temperature superconducting filter.
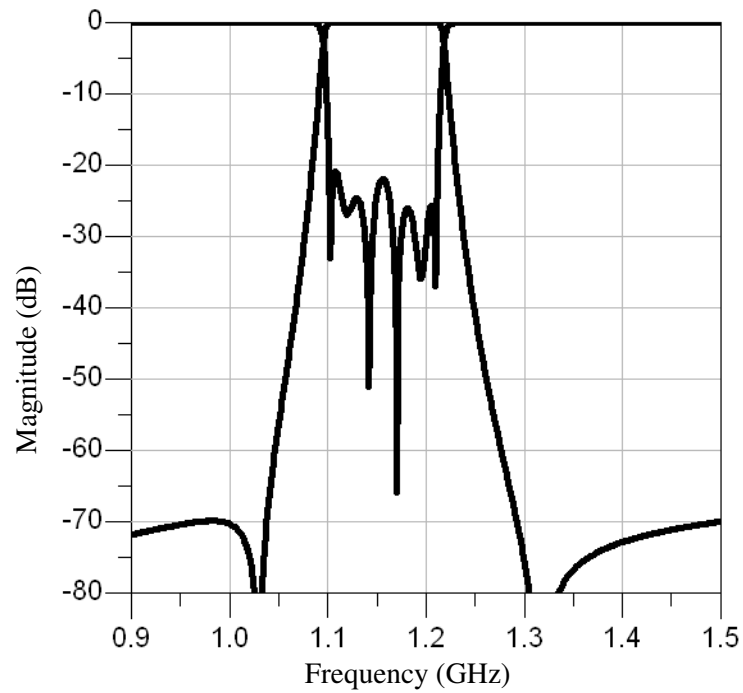
Fig. 3-11: Final lossless EM simulation results for the 8-pole high temperature superconducting filter.

Chapter 4

Highly Miniaturized Low Temperature Superconducting Circuits

Superconducting microelectronics (SME) technology has the potential for the realization of highly advanced programmable software radios. SME circuits can manage digitals signals with clocks speeds of 40 GHz. These high clock speeds also allow for a Digital-RF radio architecture with direct conversion up to 10-12 GHz [1]. RF filters are key components in the front end of the superconducting digital receiver. Fig. 4-1 shows the architecture for the receiver of an SME radio.

The RF signal received by the antenna passes through an RF filter and is sent to an ultra low noise bandpass analog-to-digital converter (ADC). This architecture eliminates the need for the down conversion of the RF signal using a mixer and a local oscillator. The down conversion process is entirely digital, including the local oscillator. The digital signal is then conditioned at ultra fast speeds creating a true software radio.
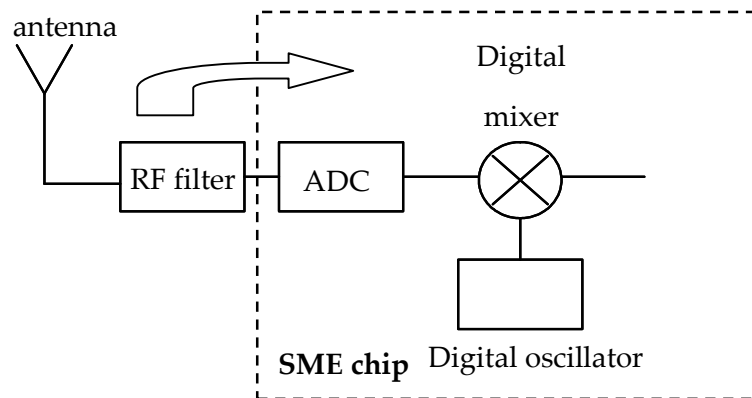
Fig. 4-1: Architecture of the receiver of an SME radio.
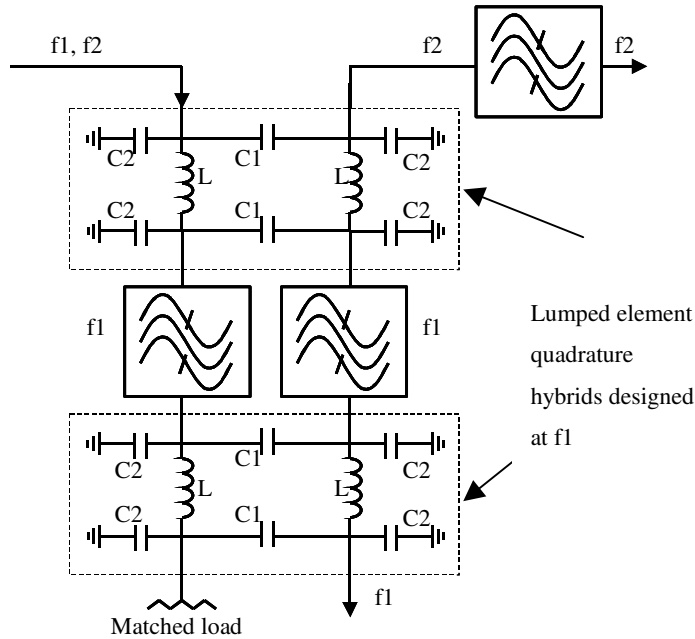
Fig. 4-2: Lumped element hybrid-coupled diplexer architecture.

An RF channelizer, which replaces the RF filter shown in Fig. 4-1, can improve the performance of the SME receiver. There exists a tradeoff between the bandwidth and the dynamic range of the superconducting ADC [53]. The RF channelizer can also reject unwanted signals between narrow sub-bands. The dynamic range and the spur-free dynamic range of the receiver determine whether it can deal with these unwanted signals [53]. Also, for larger bandwidths at higher frequencies, the total noise is increased which decreases the dynamic range. For these wideband applications, an RF channelizer can better manage wideband signals comprised of narrow sub-bands.

The proposed baseline design of the architecture shown in Fig. 4-1 uses high Q (quality factor) room temperature filters. The availability of miniature superconducting microwave components makes it possible to integrate an RF channelizer and the receiver on a single chip.

The design and fabrication of multilayer superconducting quadrature filters and hybrids are presented in this chapter. A diplexer using the hybrid-coupled diplexer architecture

52

shown in Fig. 4-2 is implemented using this multilayer process. The two channels of the diplexer have been designed with center frequencies of 1.0 GHz and 1.15 GHz. A hybrid is designed at each of these center frequencies. The hybrid designed at 1.0 GHz has a more compact spiral inductor than the hybrid designed at a center frequency of 1.15 GHz. A channelizer comprised of two identical filters and two identical hybrids is designed for each of the two channels. A filter designed at the center frequency of the additional channel is placed at the output of the channelizer to demonstrate its application as a diplexer. One diplexer has f_1 = 1.0 GHz and f_2 = 1.15 GHz, as shown in Fig. 4-2, and the other diplexer has f_1 = 1.15 GHz and f_2 = 1.0 GHz. Due to the two channels being near to each other in frequency, both of these diplexer options perform well due to the bandwidth of the hybrids. The filter and hybrids are designed with the benefit of high capacitance parallel plate capacitors and compact spiral inductors allowed by the fabrication process. The diplexers are highly miniaturized with very low loss.

The design of miniaturized bandstop filters is also presented. The 90° transmission line associated with bandstop filters is replaced with a highly miniaturized low-pass filter. A 3-pole bandstop filter design is designed, fabricated, and tested.

4.1 Fabrication Process for Superconducting Filters

HYPRES has a niobium based foundry with wafer processing and micromachining for superconducting integrated circuits. The fabrication process has been used to create superconducting circuits [53]-[56]. This process is implemented in the design and fabrication of passive microwave circuits.

The process offers many possibilities for the fabrication of microwave components. The HYPRES process, as shown in Fig. 4-3, has 10-levels consisting of thin niobium layers, resistive metal layers, insulating layers, and the Niobium/Aluminum Oxide/Niobium trilayer. A 100 nm thick niobium ground plane (M0) is first deposited on the 150 mm diameter oxidized silicon substrate. The ground plane can be patterned and etched, and a

150 nm thick insulating layer of silicon dioxide (SiO_2) is deposited over the ground plane. The M1 niobium layer is deposited next at thickness of 135 nm.
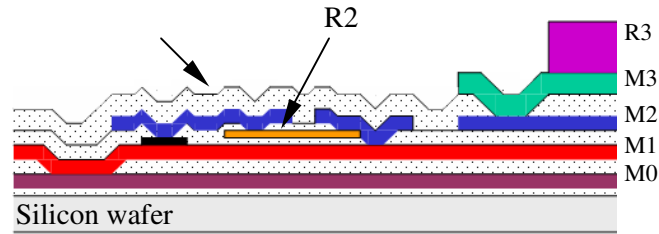
Fig. 4-3: Cross-section of the HYPRES process.

An insulating layer of SiO_2, a resistive layer (R2), and another insulating layer of SiO_2 are then deposited. The two insulating layers both have a thickness of 100 nm, and the resistive layer comprises of a thin layer of either molybdenum or Ti/AuPd/Ti. Another 300 nm thick niobium layer (M2), a 500 nm thick SiO_2 insulating layer, a 600 nm thick niobium layer (M3), and a gold based contact layer (R3) are the last four layers deposited during the fabrication process.

The superconducting nature of the niobium allows for low loss microwave components. High Q parallel plate capacitors with high capacitance values can be designed due to the SiO_2 layer between M0 and M1 being only 150 nm thick. Also, the minimum width of a line and the minimum spacing between lines for the M3 layer are 2.0 μm and 2.5 μm, respectively [57], which allows for the design of very compact spiral inductors. All of these advantages lead to the creation of highly miniaturized, low loss multilayer microwave components.

4.2 Bandpass Filter Design and Measurements

Two different types of filters are considered for design using the above fabrication process. One design takes advantage of the thin dielectric layer between two of the niobium layers to create large capacitances resulting in miniaturized filters. The other design creates a microstrip structure using the top and bottom metal layers as the microstrip conductor and ground layer, respectively.

54

4.2.1 Coplanar Waveguide Lumped Element Filter Design and Measurements

A 3-pole lumped element filter is designed using the multilayer fabrication process for each of the two specified channels. Lumped element capacitors and inductors are designed to realize the bandpass filter. The steps to design the filter are outlined.
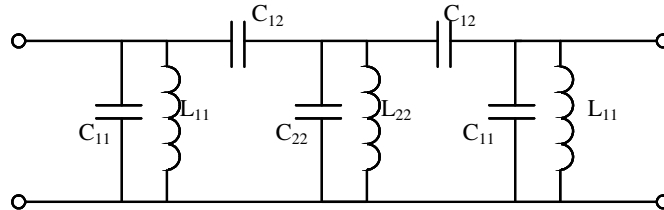
Fig. 4-4: Circuit layout of the lumped element filter design.

The filter design starts with the bandpass transformation from the lowpass prototype filter for the case of a 3-pole filter. A 90° inverter is placed on either side of the middle resonator to make all of the resonators a combination of a parallel inductor and a parallel capacitor. The 90° inverter is realized by a Π-network of a series capacitor and two shunt capacitors with negative capacitance. Fig. 4-4 shows the final lumped element design of the 3-pole filter. An image of the filter layout is shown in Fig. 4-5.

The filter is designed to have a center frequency of 1.156 GHz with a bandwidth of 115 MHz. The capacitance values for the C_{11} and C_{22} capacitors are 15.8 pF and 25.0 pf, respectively. To realize such a high value of capacitance, a parallel plate capacitor is designed using the M0 and M1 layers as the two parallel plates.

Given a 150 nm thick layer of SiO_2, and a capacitance value of 25.0 pF, the width of a square plate can be calculated as being only 300 μm. To keep the filter compact, the series capacitors are also designed to be parallel plate capacitors.
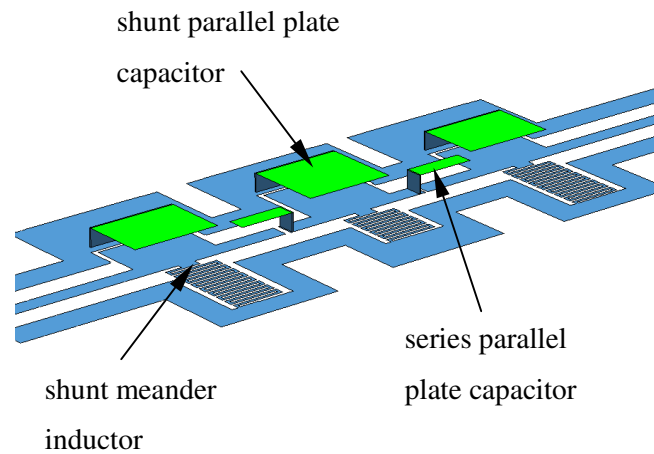
Fig. 4-5: Image of the fabricated 3-pole lumped element coplanar waveguide filter.

The inductors are realized as planar meander line inductors. The simulated resonance frequency for this inductor is above 10 GHz. The simulated resonance frequency of the shunt parallel plate capacitor is 3.44 GHz.

Bridges are needed to short out undesired modes due to the connections from the parallel capacitors and inductors to the center line of the coplanar waveguide. These bridges reside on the M2 niobium layer. Vias are made through the SiO_2 layer complete the connection between the ground lines of the coplanar waveguides.

An image of the fabricated filter is shown in Fig. 4-6, and the lossless EM simulation results are shown in Fig. 4-7. The size of the fabricated filter is only 1.81 mm by 0.65 mm. Since the circuit resides mainly on the M0 layer, transitions by vias are made from the M3 niobium layer to the M0 layer. The R3 layer is used as contact pads for wire bonds.
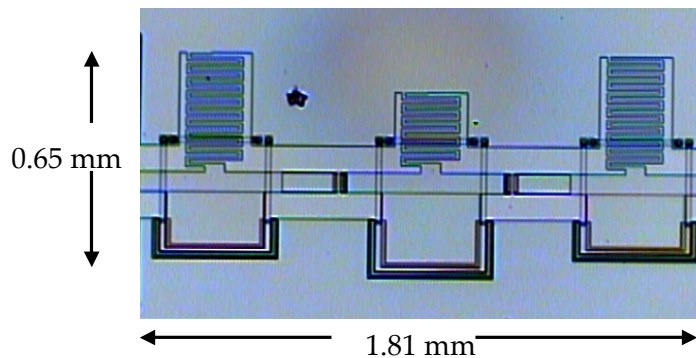
Fig. 4-6: An image of the fabricated multilayer superconducting lumped element filter.
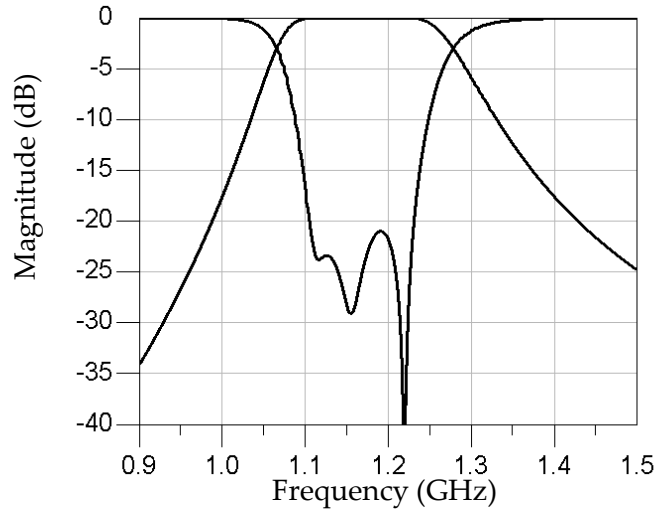
Fig. 4-7: Lossless EM simulation response of the 3-pole lumped element filter.

The circuits are immersed in liquid helium to bring the niobium to a superconducting state. The measured results are shown in Fig. 4-9 and Fig. 4-10. The estimated loss of the filter from the measured data in its pass band is approximately 0.26 dB. There is a shift in the center frequency of the filter from the simulation response, which is likely due to the fabrication tolerances on either the thickness or the dielectric constant of the SiO_2 layer between the M0 and M1 layers. The capacitance of this dielectric layer is given as 0.277 $fF/\mu m^2 \pm 20\%$ [57]. Simulation results with this error considered are shown in Fig. 4-8. These simulations show a shift in center frequency closer to the center frequency of the measured filter. It may be possible to adjust for fabrication tolerances by adding additional metal and insulating layers to the fabrication process to create microelectromechanical systems (MEMS) tunable capacitors.

The wideband measurement results are shown in Fig. 4-10. The response is spurious free up to a frequency of 3.9 GHz. The center frequency of this spurious signal is determined by the self resonance of the lumped elements within the filter. Since the capacitors resonate at a frequency of approximately 3.44 GHz, it is not unexpected to have a spurious signal at 3.9 GHz.
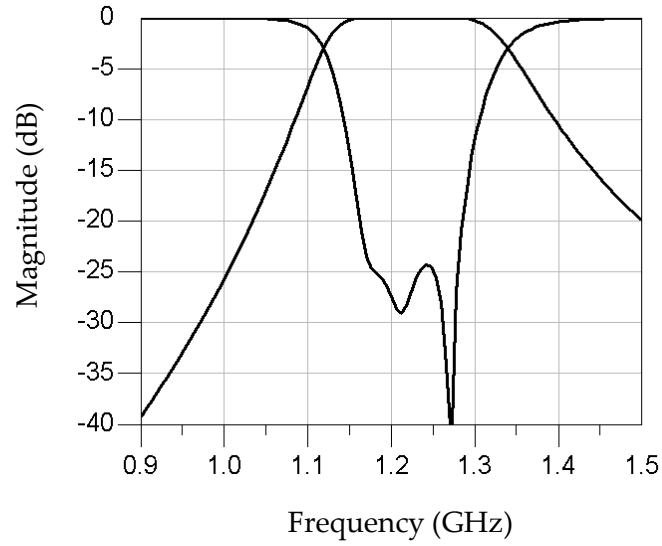
Fig. 4-8: Lossless EM simulation response of the lumped element filter with the estimated

fabrication tolerance of ±20%.
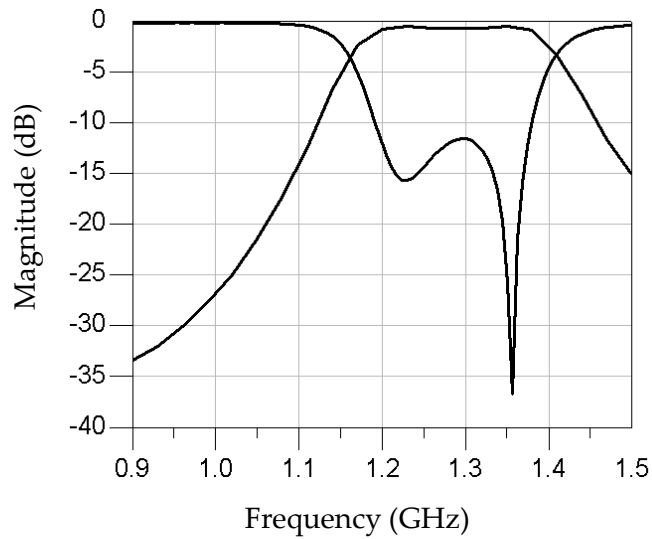
Fig. 4-9: Measured response of the 3-pole lumped element filter.
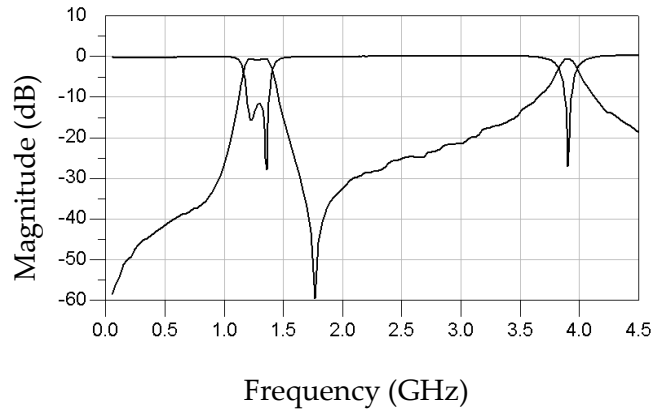
Fig. 4-10: Wideband measured response of the 3-pole lumped element superconducting filter.

4.2.2 Microstrip Filter Design and Measurements

A miniaturized microstrip filter is designed by taking advantage of the multilayer fabrication process. A tap input is used at the input of the filter and the resonator couplings are also achieved by a tap between resonators, as shown in Fig. 4-11.
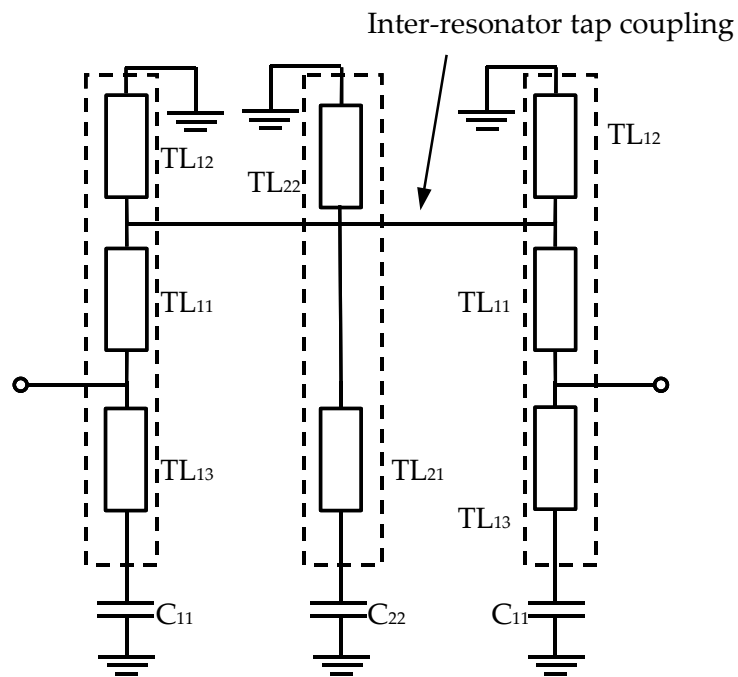
Fig. 4-11: Circuit layout of a three pole microstrip filter with inter-resonator tap connections.

The coupling between resonators for this filter design can be achieved by connecting the two resonators by a wire at a certain point on the inductor. The specific point that the two inductors are tapped determines the coupling coefficient between the two resonators. By determining the magnetic and electric coupling between the two resonators, the coupling coefficient can be determined [58].
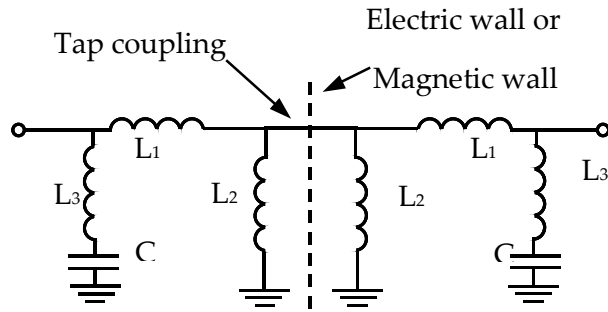
Fig. 4-12: Circuit to determine the coupling coefficient between two resonators.

Using a lumped element model of the resonators, as shown in Fig. 4-12, the magnetic and electric coupling can be determined. For the case of the electric coupling, a short circuit is placed between the two resonators and the resonant frequency of the filter is determined as seen from one of the ports. The effect of magnetic coupling can be similarly determined by placing a magnetic wall, or an open circuit, between the two resonators. The coupling coefficient between the two resonators can be found by [58]

$$k = \frac{f_m^2 - f_e^2}{f_m^2 + f_e^2},$$

(4.1)

where f_m and f_e are the resonant frequencies in the presence of the magnetic wall and electric wall, respectively. The value for f_m will be the same regardless of where the tap input is located on the inductor. The coupling coefficient is determined by the electric coupling and f_e. By substituting in f_m and f_e into (4.1), the coupling coefficient is found to be

$$k = \frac{-L_2}{2(L_1 + L_3) + L_2}.$$

(4.2)

60

By letting the total inductance be L_{tot}, the coupling coefficient becomes

$$k = \frac{(L_1 + L_3) - L_{tot}}{(L_1 + L_3) + L_{tot}}.$$ (4.3)

To demonstrate the design of the filter, a two-pole, a three-pole and a four-pole filter are designed using circuit models of transmission lines and capacitors. All filters are designed to have a center frequency of 1.2 GHz and a bandwidth of 200 MHz. The simulated insertion loss data is shown in Fig. 4-13.
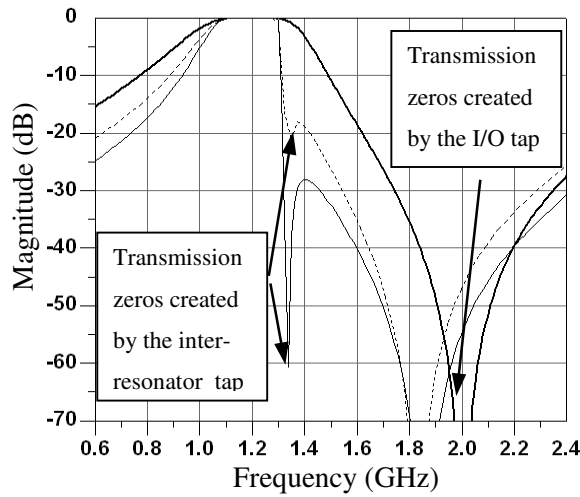
Fig. 4-13: Insertion loss of simulated two-pole (solid bold line), three-pole (dashed line), and four-pole (solid thin line) filters.

It is noted that one transmission zero appears on the high side of passband for all three filters. This transmission zero, which appears between 1.85 GHz to 2 GHz for the different filters, is a result of the tap input coupling [59]. This resonance corresponds to a frequency due to the capacitor C_{11} in series with the section of transmission line TL_{13}. When more resonators are added to the filter, another transmission zero is created very near the high side of the passband creating a very sharp cutoff for narrower band filters. This transmission zero is due to a resonance from the parallel combination of TL_{13}, TL_{12}, C_{11} and TL_{21}, C_{22}.
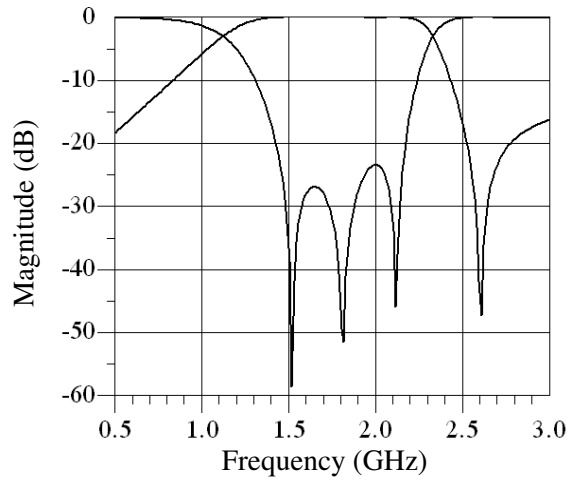
Fig. 4-14: Simulated results of the 42.6% bandwidth filter using the proposed configuration.

This filter configuration is also amenable to wideband filter designs. From (4.2) and (4.3), it is possible to achieve wider bandwidths with a simple position of the tap. A three-pole filter, as shown in Fig. 4-11, is designed using a circuit simulator. The transmissions lines have an impedance of 27 Ω, and the following lengths at a frequency of 1.76 GHz: TL_{11} = 56.3°, TL_{12} = 63.4°, TL_{13} = 22.5°, TL_{21} = 40.8°, and TL_{22} = 46.5°. The capacitors have capacitances of C_{11} = 0.13 pF and C_{22} = 0.69 pF. The simulated response is shown in Fig. 4-14. The filter has a center frequency of 1.76 GHz, and a percentage bandwidth of 42.6%.

A two-pole filter and a three-pole filter are designed and tested to demonstrate this novel filter configuration. The filters are fabricated using a multilayer fabrication process implementing superconducting niobium layers and silicon dioxide insulating layers. The filter is highly miniaturized and exhibits very low loss due to the implementation of the superconducting layers.

62

Coupling between resonators

Transition of CPW to Microstrip

Tap coupling using M2

Via from M3 to M0
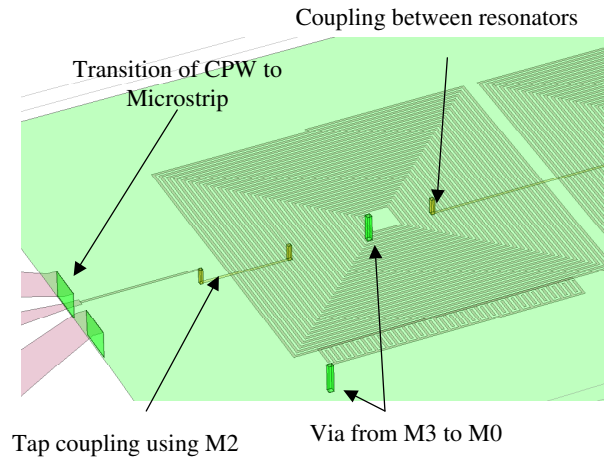
Fig. 4-15: Image of the microstrip filter.

CIRFE   x120   250um
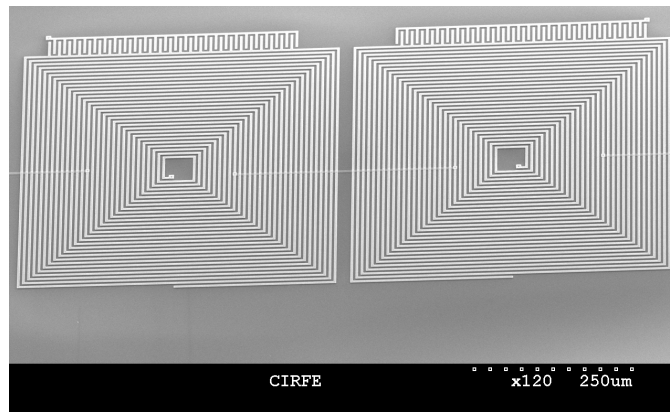
Fig. 4-16: SEM image of the two-pole microstrip filter.

For this filter design, the M0 layer is used as the ground plane for the microstrip filter. The M3 layer is used as the top layer and the input tap and inter-resonator tap connections are made by the M2 layer with via connections between layers. The minimum width of a line and the minimum spacing between lines for the M3 layer are 2.0 µm and 2.5 µm, respectively [57].A transmission line width of 4 µm is used with the dielectric height of 0.85 µm. The dielectric constant of the SiO_2 is assumed to be 4.5. This 4 µm line width results in a transmission line with a simulated characteristic impedance of 27 Ω.

1.0 mm

2.0 mm
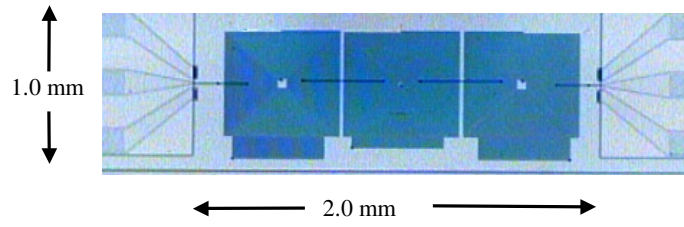
Fig. 4-17: Image of the three-pole microstrip filter.
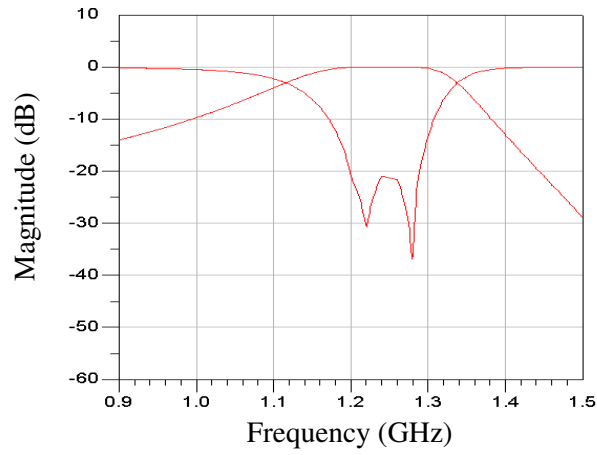
Fig. 4-18: EM simulated results of the two-pole microstrip filter.
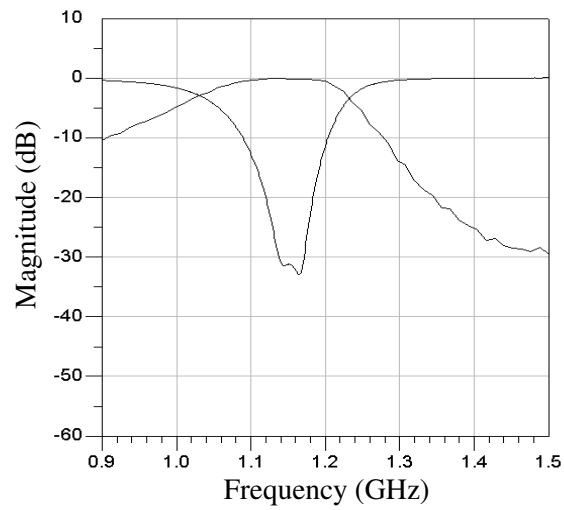
Fig. 4-19: Measured results of the two-pole microstrip filter.
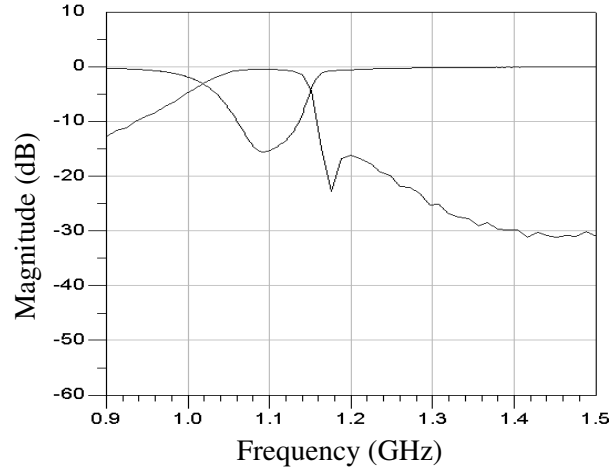
Fig. 4-20: Measured results of the three-pole microstrip filter.

A transition is made from coplanar waveguide transmission line to the microstrip filter, as shown in Fig. 4-15. The transmission line spiral that makes up the resonator has a line width of 4 μm and a spacing of 4 μm. Vias are made from M3 to M0 at the short circuit end of the transmission line and the interdigital capacitor. Vias are made from M3 to M2 to make the tap connections at the input and between resonators.

The two-pole filter, as shown in Fig. 4-16, and the three-pole filter, as shown in Fig. 4-17 have a designed center frequency of 1.25 GHz and a bandwidth of 100 MHz. The filters are simulated using the EM simulator Sonnet, and the EM simulation results of the two pole filter are shown in Fig. 4-18. The measured results for both filters are shown in Fig. 4-19 and Fig. 4-20. The shift in center frequency is due to the kinetic inductance of the superconducting thin film not being considered. A discussion of how to model the kinetic inductance is given in section 4.5.2. As expected, the transmission zero created by the inter-resonator tap coupling appears in the response of the 3-pole filter but not the response of the 2-pole filter. The position of this transmission zero is consistent with its position predicted by the EM simulator. When testing the filters, connections were made with wire bonds from the chip to a CPW transmission line on an alumina wafer. This alumina wafer was placed in a metal housing with connections to coaxial cables, as shown in Fig. 4-21. The coaxial cables and the metal housing were immersed in liquid helium to reach the superconducting state of the niobium. The size of each resonator is only 0.5 mm by 0.55 mm making it highly

65

miniaturized by being only $\lambda_0/500$ in size. When the tap connection is removed, EM simulations show an isolation across the filter of approximately 48 dB. The electromagnetic coupling between resonators is small due to the ground plane being very close to the top metal layer.

Coaxial cable connector

Chip with wire bonds to the CPW transmission line

Metal housing with a CPW transmission
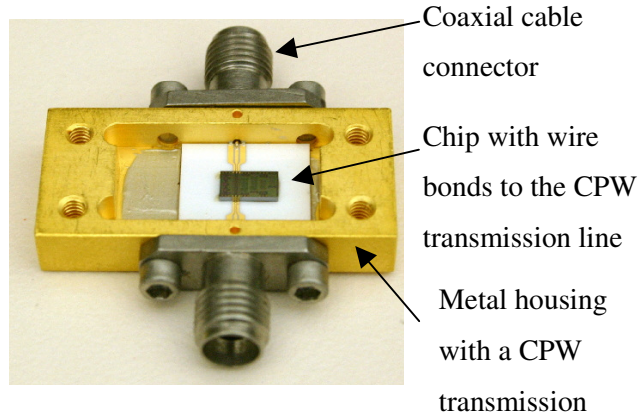
Fig. 4-21: Image of the housing used to test the superconducting chip.

4.3 Quadrature Hybrid Design and Measurements

Lumped element quadrature hybrids allow for miniaturization and ease of design in multiplexer applications. Distributed element hybrids and manifold multiplexers are relatively large at frequencies below 10 GHz [60]. The modular design of hybrid-coupled multiplexers permits the ease in design not seen when compared to the design of manifold-coupled multiplexers. The loss associated with the lumped element components is the main disadvantage of implementing a lumped element hybrid design. Multilayer superconducting lumped element capacitors and inductors allow for a high degree of miniaturization without encountering high losses.

Two lumped element quadrature hybrids are designed using the multilayer fabrication process. Lumped element parallel plate capacitors and compact spiral inductors are designed to realize these two hybrid designs.
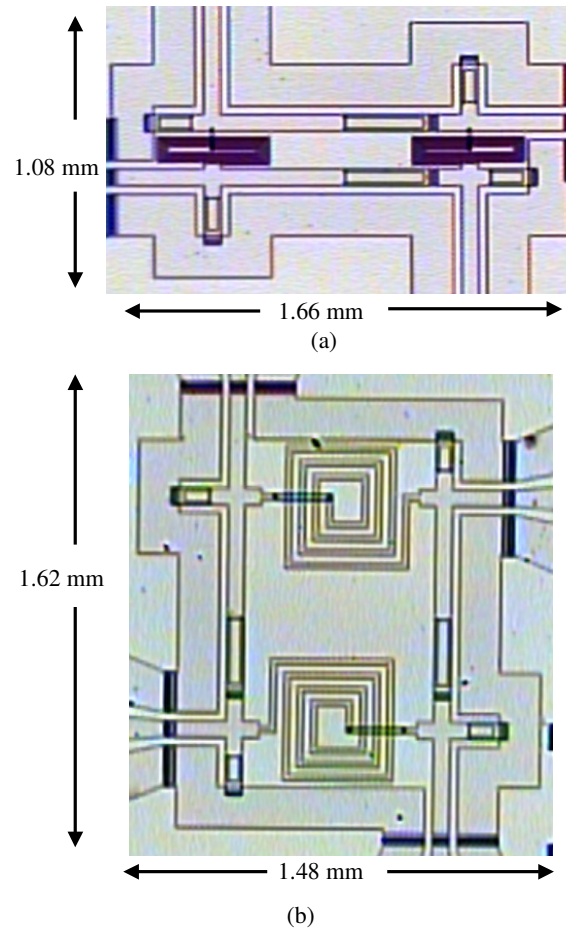
Fig. 4-22: Image of the fabricated quadrature hybrids designed at a center frequency of (a) 1.0 GHz and (b) 1.15 GHz.

The fabrication tolerances need to be considered when analyzing the measured responses. For example, the capacitance of the dielectric layer between M0 and M1 is given as 0.277 $fF/\mu m^2 \pm 20\%$ [57]. Although the hybrid designed at 1.0 GHz is smaller due to its compact spiral inductor, the effect of the kinetic inductance associated with superconducting materials would be more pronounced than in the inductor design used for the hybrid designed at 1.15 GHz.

The hybrid design [61] is based on the circuit diagram shown in Fig. 4-2. For the hybrid designed at 1.0 GHz, the value of C_1 is 3.18 pF, the value of C_2 is 1.31 pF, and the value of L is 5.62 nH. For the hybrid designed at the center frequency of 1.15 GHz, the inductance

value of L is 4.85 nH and the capacitance values of C_1 and C_2 are 2.75 pF and 1.14 pF, respectively.
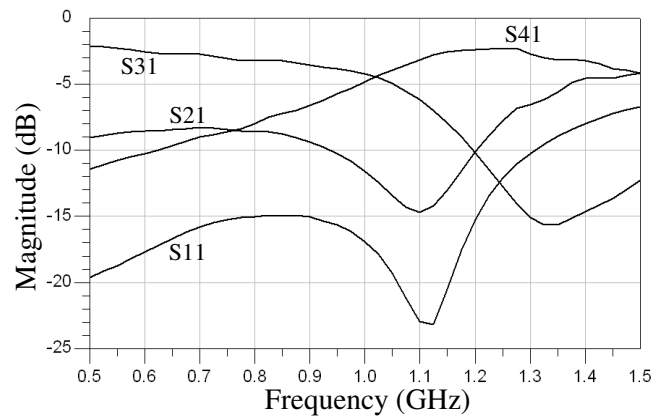
Fig. 4-23: Measured response of the hybrid designed at 1.0 GHz.

The capacitors are realized by parallel plate capacitors using the M0 and M1 niobium layers as the two parallel plates. Since the layer of SiO_2 between these two layers is only 150 nm thick, the capacitors are very small, needing only an area of 40 μm x 280 μm for a capacitance of 3.18 pF. The inductors are realized by spiral inductor designs. The inductor with an inductance of 5.62 nH has an area of only 100 μm x 400 μm. Images of the two hybrids are shown in Fig. 4-22. The measured and EM simulation results using the EM simulator Sonnet of the hybrid designed at 1.0 GHz are given in Fig. 4-23 and Fig. 4-24, respectively.
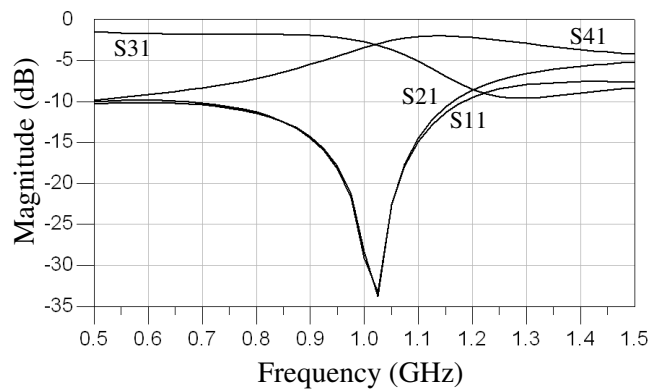
Fig. 4-24: EM simulation response of the hybrid designed at 1.0 GHz.

4.4 Diplexer Design and Measurements

The two channelizers comprised of two hybrids and two filters as shown in Fig. 4-2 at the two distinct center frequencies were designed, fabricated and tested. The filters are 3-pole lumped element filters [62] that were designed at the two center frequencies. Images of these channelizers are shown in Fig. 4-25.

2.47 mm

4.784 mm

(a)

2.38 mm

4.784 mm

(b)
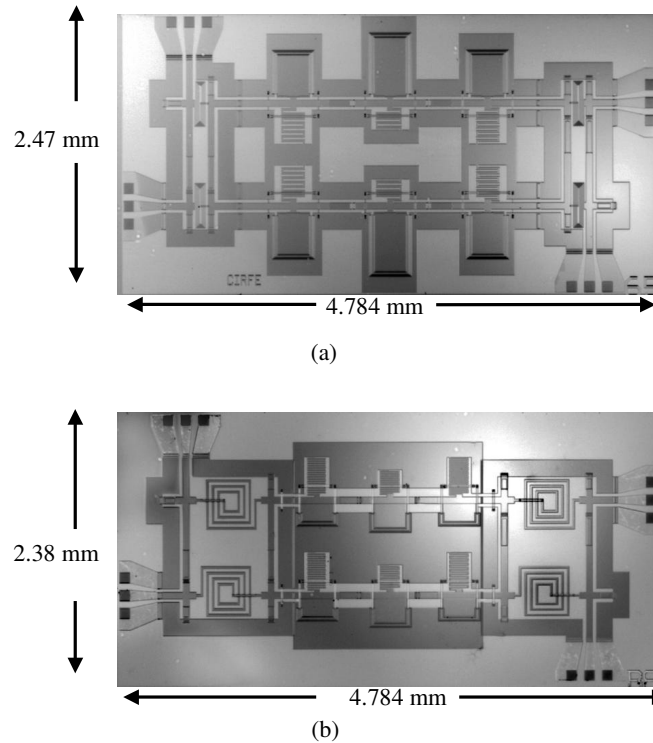
Fig. 4-25: Images of the two channelizers designed at center frequency of (a) 1.0 GHz and at

(b) 1.15 GHz.

The circuits are immersed in liquid helium to bring the niobium to a superconducting state. Matched 50 Ω loads are fabricated using the R2 layer of the fabrication process to connect to the load port in the diplexer design. These loads are connected by wire bond to the channelizer. The measured results of the four port channelizer designed at 1.0 GHz are shown in Fig. 4-26. The desired signal passing through the channelizer is shown as S_{41} in Fig. 4-26. The signal that would be passed on to the next channelizer in a multiplexer design is shown as S_{21}, and the signal sent to the 50 Ω load is shown as S_{31}.
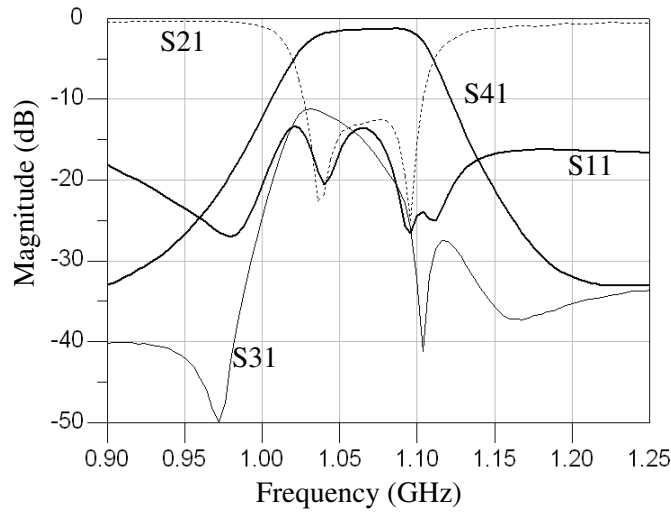
Fig. 4-26: Measured results of the channelizer designed at 1.0 GHz.
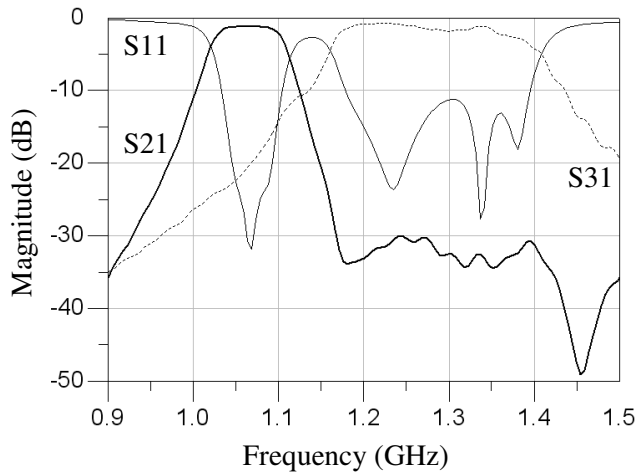
Fig. 4-27: Measured response of the diplexer with the hybrid channelizer designed at 1.15 GHz and the filter designed at a center frequency 1.0 GHz at the channelizer output.

The measured results of the diplexer with the hybrid-coupled channelizer designed at 1.15 GHz with the filter designed at a center frequency of 1.0 GHz at its output are shown in Fig. 4-27. The filter is connected by wire bonds to the output of the channelizer to create the diplexer. The two channelized frequency bands are shown as S_{21} and S_{31} in Fig. 4-27. The measured results of the diplexer with the hybrid-coupled channelizer designed at 1.0 GHz with the filter with a center frequency of 1.15 GHz at its output are shown in Fig. 4-28. The

measured results show the benefits of using high Q filters and high Q lumped element components. A similar diplexer designed using Complementary Metal–Oxide–Semiconductor (CMOS) technology would exhibit an insertion loss of at least 20 dB.
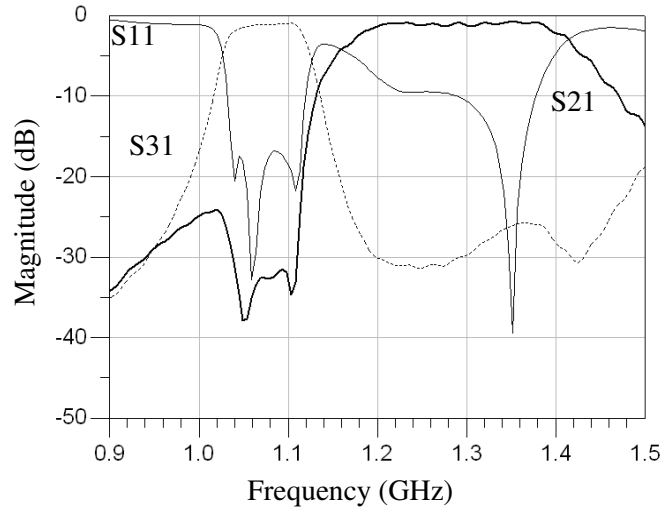
Fig. 4-28: Measured response of the diplexer with hybrid channelizer designed at 1.0 GHz and a filter designed at 1.15 GHz at the channelizer output.

4.5 Bandstop Filter with Low-Pass Filters as Impedance Inverters

The standard niobium fabrication process offered by HYPRES allows for the realization of highly miniaturized microwave bandstop filters. A miniaturized bandstop design is presented that makes use of lumped element low pass filters, which results in a savings in filter size. The 90° transmission lines traditionally used in bandstop filter designs are replaced with a low pass filters. Each of these low pass filters has a cutoff frequency and order that allows for an insertion phase of 90° at the center frequency of the bandstop filter. The bandstop filter then has a usable bandwidth from DC to the cutoff frequency of the low pass filter. A massive savings in size can be achieved over the use of a 90° length of transmission line when the low pass filter can be realized with lumped element inductors and capacitors.

A bandstop filter can be realized without the use of impedance inverters if the resonators alternate between series and shunt configurations. The fabrication process used in the filter

71

design in this chapter lends itself to such a design, though it can be advantageous to have all the resonators be of the same configuration. The main advantages are evident when narrow band bandstop filters are designed. Inconsistencies in the fabrication process and the accuracy of the design show less of an effect on a filter design if all resonators are in the same configuration. For very narrow bandwidths, either the capacitor or inductor will have a large value, which may or may not be realizable with a fabrication process. It can be advantageous to convert all the resonators to the configuration that the fabrication process can allow. Also, in a narrow band design, the loss associated with the inductors and capacitors may determine the choice of resonator configuration based on maximizing the quality factor of the filter. The highly miniaturized, high quality factor lumped elements that can be designed with the low temperature superconducting fabrication process are ideal for designing bandstop filters with low-pass filters used as impedance inverters.
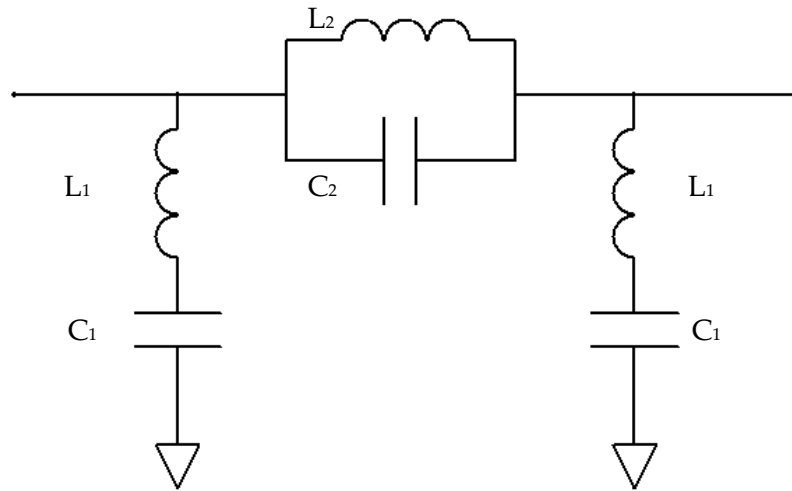
Fig. 4-29: Ideal 3-pole bandstop filter.

The concept of the bandstop filter with low pass filters as impedance inverters is demonstrated through circuit simulations, EM simulations, and measured results. Section 4.5.1 discusses how the impedance inverter can be replaced with a low-pass filter for a bandstop filter design. The design of the low-pass filter and a discussion on how the order of the low-pass filter affects the usable passband bandwidth of the bandstop filter are

introduced in section 4.5.2. Section **Error! Reference source not found.** presents EM simulations and measured results of the bandstop filter with low-pass filters used as impedance inverters.

4.5.1 Bandstop Filter Designs

Three ideal 3-pole bandstop filter designs are presented through circuit simulations. The first bandstop filter design has the first and third resonators as series LC resonators from the signal line to ground and the second resonator as a parallel LC circuit in series with the signal line, as shown in Fig. 4-29. The low-pass prototype Chebyshev values go through bandstop and impedance transformations to generate the inductor and capacitor values. The center frequency and bandwidth of the filter are chosen to be 2.0 GHz and 250 MHz, respectively. The inductor and capacitor values then become $L_1 = L_3 = 50.59$ nH, $C_1 = C_3 = 0.1252$ pF, $L_2 = 0.4826$ nH, and $C_2 = 13.21$ pF. The circuit simulator results for this circuit are shown in Fig. 4-30.
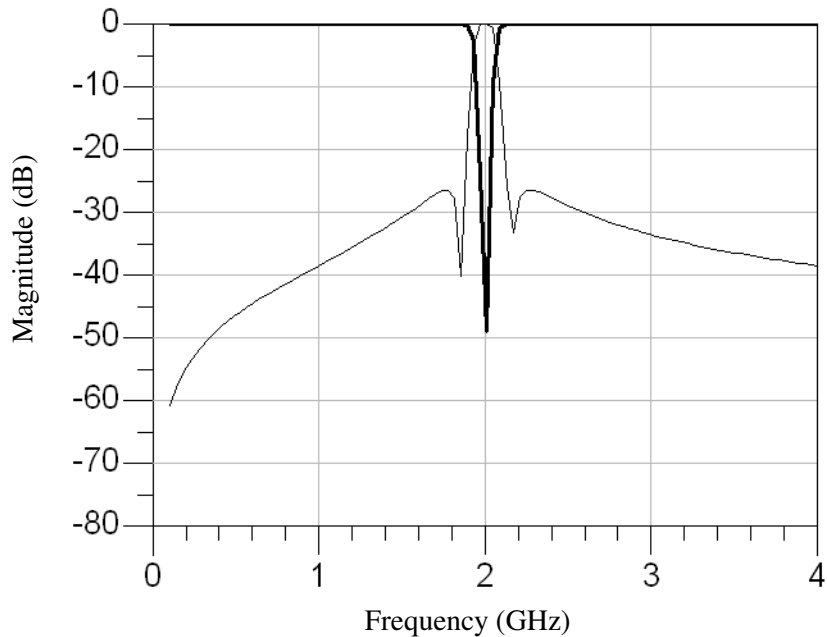
Fig. 4-30: Insertion loss (bold) and return loss (thin) circuit simulator results of the ideal bandstop filter

For many bandstop filter designs, the resonators are all put in the same configuration by adding a 50 Ω transmission line with an electrical length of 90° at the center frequency of the filter to either side of the alternate resonator configuration, as shown in Fig. 4-31. This 90° length of transmission line acts as an impedance inverter. The circuit simulation results of the second bandstop filter, whose circuit is shown in Fig. 4-31 with 90° transmission lines at 2 GHz are shown in Fig. 4-32. The new values of the inductor and capacitor for the second resonator are L'_2 = 32.81 nH and C'_2 = 0.1930 pF. Finally, the third filter design has the 90° transmission lines replaced with ideal 5-pole low-pass filters, and its return loss circuit simulation is also shown in Fig. 4-32. This third filter design is investigated further in section **Error! Reference source not found.**.
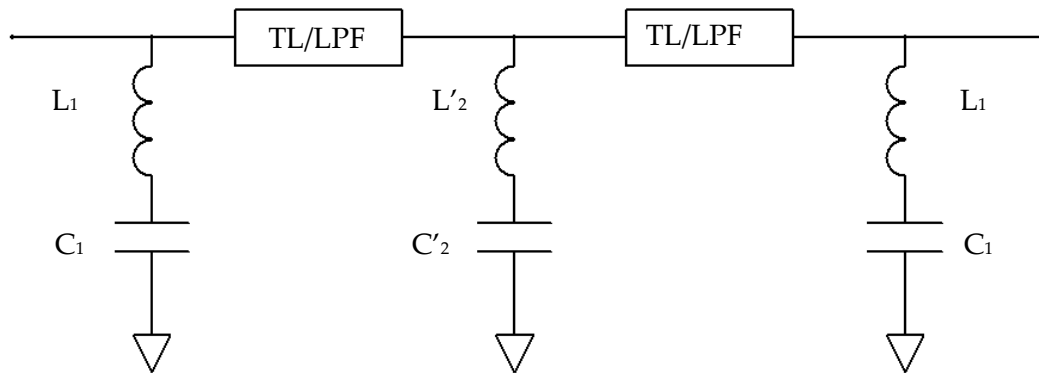
Fig. 4-31: A 3-pole bandstop filter with all shunt resonators and impedance inverters between resonators.

A lumped element low pass filter can replace this long length of transmission line. A low pass filter has similar properties to a transmission line up to the filter's cutoff frequency. A trade off occurs between the length of the transmission line and the bandwidth associated with the low pass filter. The order of the low pass filter determines the usable bandwidth of the system. A 5-pole low pass Chebyshev filter with a return loss of 25 dB and a 90° insertion phase shift at 2 GHz has a cutoff frequency of 3.83 GHz. The bandwidth can be increased by increasing the order of the filter, as 7-pole and 9-pole low pass filters have cutoff frequencies of 6.209 GHz and 8.684 GHz, respectively, under similar design

considerations. A 5-pole filter is the minimum order that should be implemented as a 3-pole filter has a 90° insertion phase shift above its cutoff frequency. The circuit simulator results of the bandstop filter with the low pass filter replacing the transmission line is shown in Fig. 4-32.
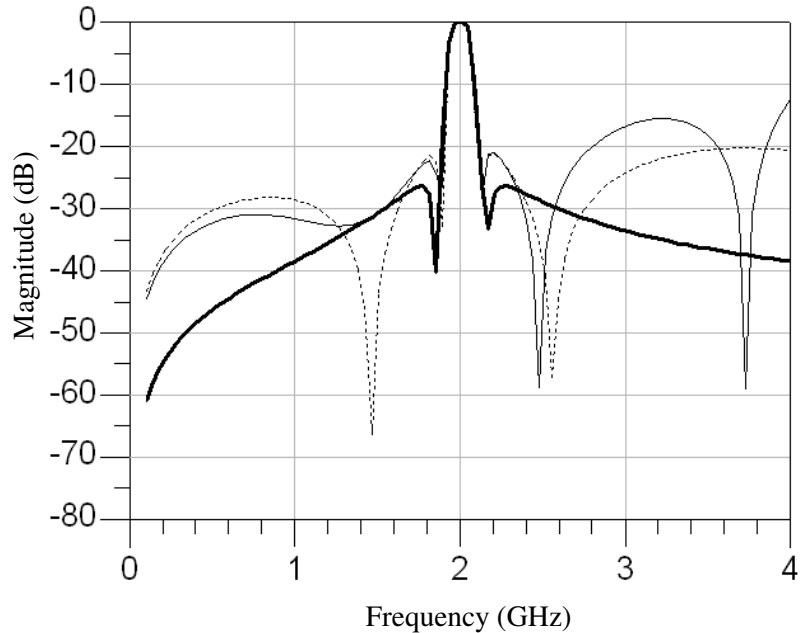
Fig. 4-32: Return loss circuit simulator results of the first bandstop filter (bold), the second bandstop filter with all shunt resonators and ideal transmission lines (dotted), and the third bandstop filter with all shunt resonators and low-pass filters used as impedance inverters (thin).

The bandwidth of the rejection band is similar for the three filters whose circuit simulations are shown in Fig. 4-32. Though, the out of band return loss is different for each of the three filters. The return loss matches that of a low-pass filter for the third bandstop filter that makes use of low-pass filters as impedance inverters. The characteristics of this low-pass filter are further discussed in the following section.

4.5.2 Low-Pass Filter Design

The use of low-pass filters in phase shifter designs is well known, especially in discrete phase shifter designs where single pole double switches are implemented to switch between

either a low-pass filter or a high-pass filter [63]. These filter designs are generally realized as 3rd order lumped element filters in a Π-network. Where the phase shifter designs make use of the difference in phase between the low-pass and high-pass filters, the low-pass filters used in this chapter are implemented for their absolute insertion phase. For this reason, the order and cutoff frequency of the low-pass filter for either Chebyshev or Butterworth designs are investigated as they determine the usable bandwidth from DC that the bandstop filter can pass. The use of the low-pass filter also has the added benefit of rejecting signals at frequencies higher than that of the cutoff frequency.

A coplanar waveguide (CPW) transmission line with an electrical length of 90° at 2 GHz realized with niobium-based fabrication process has a physical length of approximately 15 mm. This length of transmission line is quite long for superconducting microelectronics applications. A highly miniaturized lumped element low-pass filter can replace this long length of transmission line.
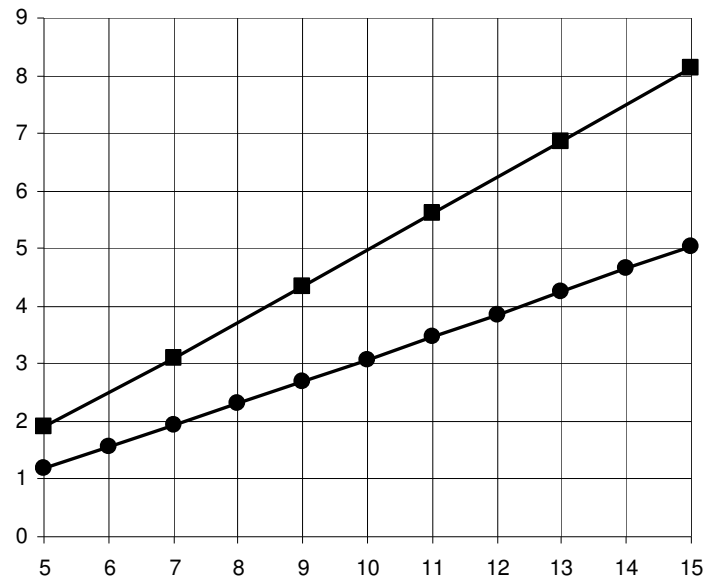
Fig. 4-33: Usable bandwidth of the low-pass filter for a bandstop filter with a center frequency of 1 versus the order of the low-pass filter for a Chebyshev response (square) and for a Butterworth response (circle).

76

A low-pass filter has similar properties to a transmission line up to the filter's cutoff frequency. A trade off occurs between the size and order of the filter, and its bandwidth, as the order of the low-pass filter determines the usable passband bandwidth of the system. A 5-pole low pass Chebyshev filter with a return loss of 25 dB and a 90° insertion phase shift at 2 GHz has a cutoff frequency of 3.83 GHz. The bandwidth can be increased by increasing the order of the filter, as 7-pole and 9-pole low pass filters have cutoff frequencies of 6.209 GHz and 8.684 GHz, respectively, under similar design considerations. A 5-pole filter is the minimum order that should be implemented as a 3-pole filter has 90° insertion phase above its cutoff frequency.

The relationship of the order of the low-pass to the usable bandwidth for the frequency of 1 at which the insertion phase is 90° for Chebyshev and Butterworth low-pass filter responses is shown in Fig. 4-33. For example, a 7th order Chebyshev filter has a bandwidth approximately 3 times that of the center frequency of the bandstop filter. Chebyshev filters demonstrate higher passband bandwidths for a given filter order as compared to Butterworth filters.

A 5-pole Chebyshev low pass filter is used in this bandstop filter design. For a cutoff frequency of 3.83 GHz and a return loss of 25 dB, the series inductors have values of 1.65 nH and 3.37 nH, and the shunt capacitors have a value of 1.101 pF. The low pass filter is designed using the EM simulator Sonnet and its layout is shown in Fig. 4-34.

0.915 mm
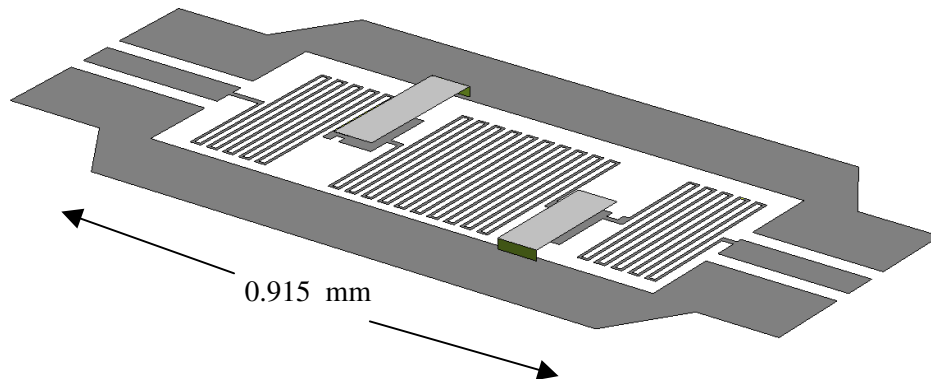
Fig. 4-34: Low-pass filter with a 90° phase shift at the center frequency of the bandstop filter (*z*-direction not to scale).

A surface inductance of 0.126 pH/sq. is included for the metal layers in the simulations to model the effects of the kinetic inductance of the thin niobium layers. The value of the surface inductance, L_s, is determined by [64]

$$L_s = \mu_0 \lambda_0 \quad (\text{pH/sq.}), \qquad (4.4)$$

where μ_0 is the permeability of free space and λ_0 is the penetration depth of the niobium. The penetration depth of the niobium layers is approximately 100 nm [57].

The magnitude and insertion phase EM simulation results are shown in Fig. 4-35. The phase simulation results show a 90° phase shift at 2 GHz, the center frequency of the bandstop filter. The length of this low pass filter is only 0.915 mm, which is obviously a massive reduction in size as compared to the 15 mm transmission line. When implemented at lower frequencies, a bigger savings is made, as a 90° length of transmission line at a frequency of 500 MHz would be approximately 60 mm.
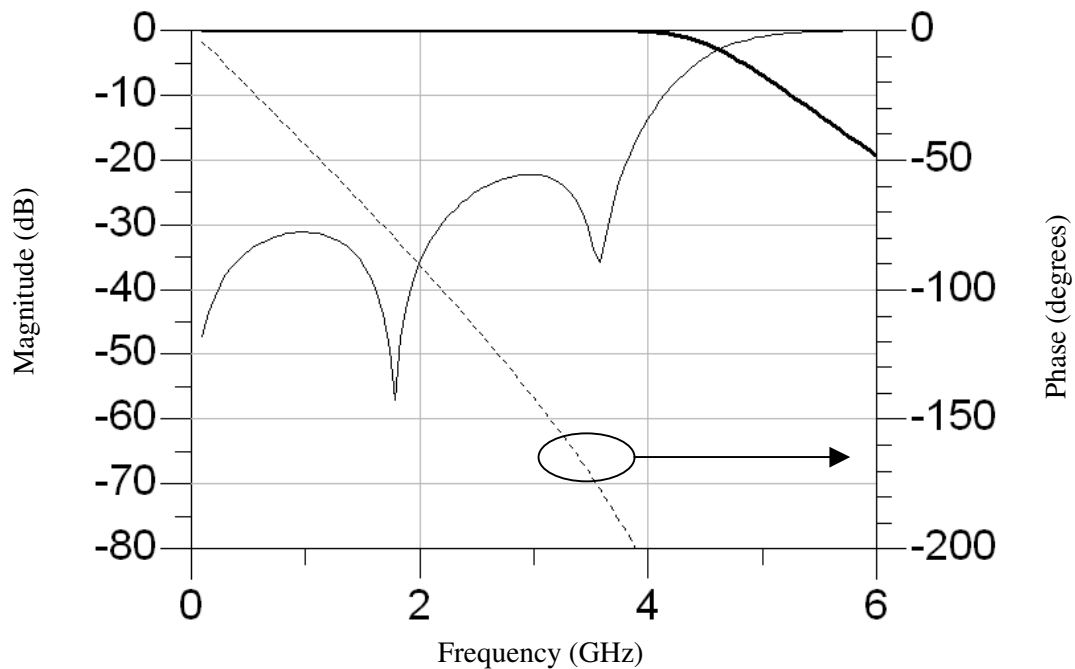
Fig. 4-35: Return loss (thin), insertion loss (bold), and insertion phase (dotted) EM simulation results of the low pass filter.

78

4.5.3 Bandstop Filter Design and Measurements

The bandstop filter is designed with a center frequency of 2 GHz and a bandwidth of 250 MHz. The three resonators are individually simulated to match the response of the ideal lumped element resonators. Due to symmetry, the first and third resonators are identical. The resonators consist of a spiral inductor connected from the signal of the CPW transmission line to a capacitor that is connected to the ground line of the transmission line. A via is made from the center line down to a lower niobium layer to connect to the spiral inductor. The low-pass filter from section 4.5.2 is used as the required impedance inverter. The layout of the 3-pole bandstop, which has a length of 4.65 mm, is shown in Fig. 4-36.
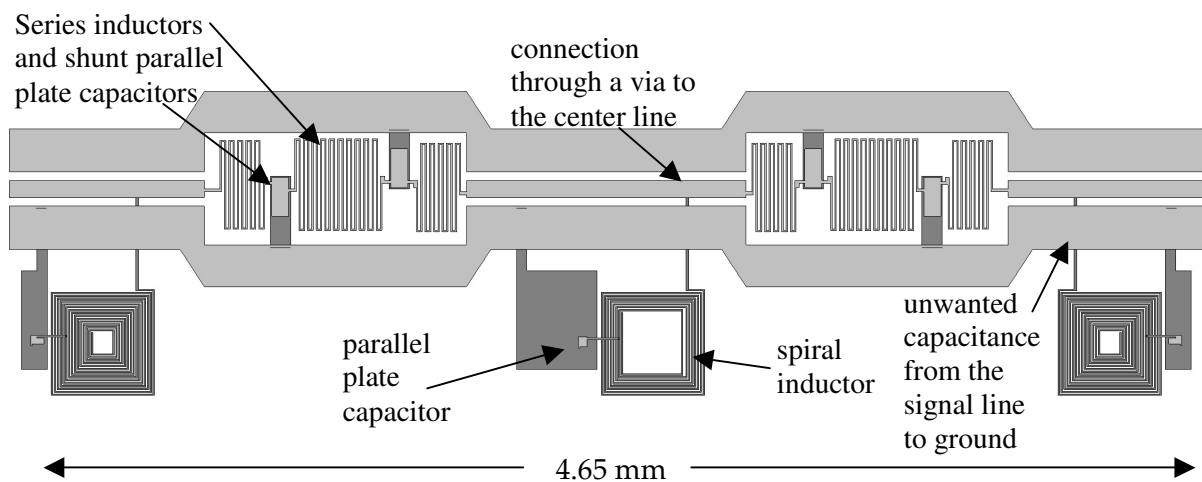
Fig. 4-36: Image of the layout of the bandstop filter with low-pass filters as impedance inverters.

EM simulations are performed by simulating the two resonator designs and the low pass filter design individually and by combining the s-parameter networks in a circuit simulator. These EM simulations of the bandstop filter are shown in Fig. 4-37.

The fabricated bandstop filter is assembled in a metal housing with connections made through 50 W coaxial connectors and cables. The metal housing is immersed in liquid helium to reach the transition temperature of the thin niobium layers. The measured results of the bandstop filter are shown in Fig. 4-38.
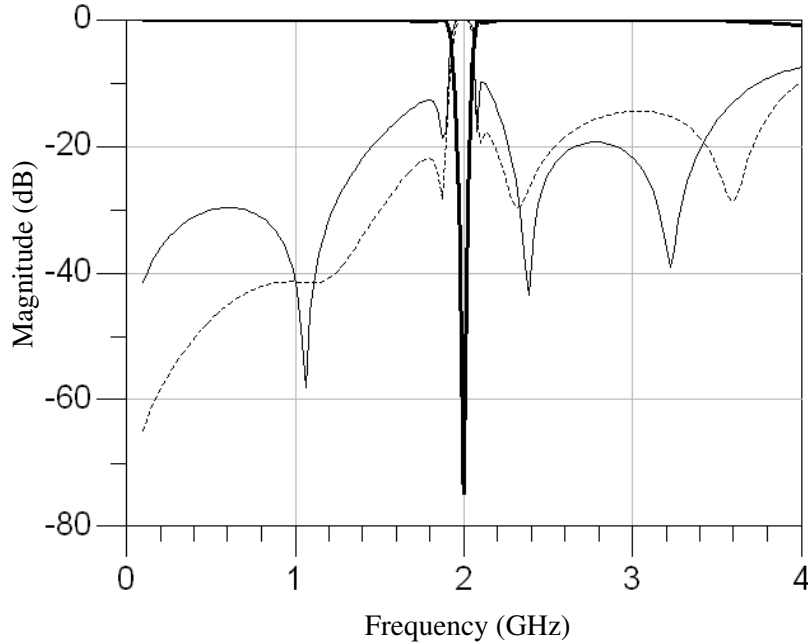
Fig. 4-37: EM return loss (thin) and insertion loss (bold) simulation results of the 3-pole bandstop filter with low pass filters as 90° phase shifters. The return loss (dotted line) EM simulation of a design with revised resonators is also shown.

As shown in Fig. 4-37 and Fig. 4-38, the return loss near the rejection band of both the EM simulation results and the measured results is higher than desired. This is due to the connection from the center line of the CPW transmission line to the inductor of the resonators passing under the ground line of the CPW transmission line. This results in a capacitance in parallel with the resonator. A revised resonator design, as shown in Fig. 4-39, eliminates this capacitance in parallel with the bandstop resonator. EM simulations, as shown in Fig. 4-37, of the bandstop filter with this revised resonator design demonstrate an improvement in the return loss near the rejection band.
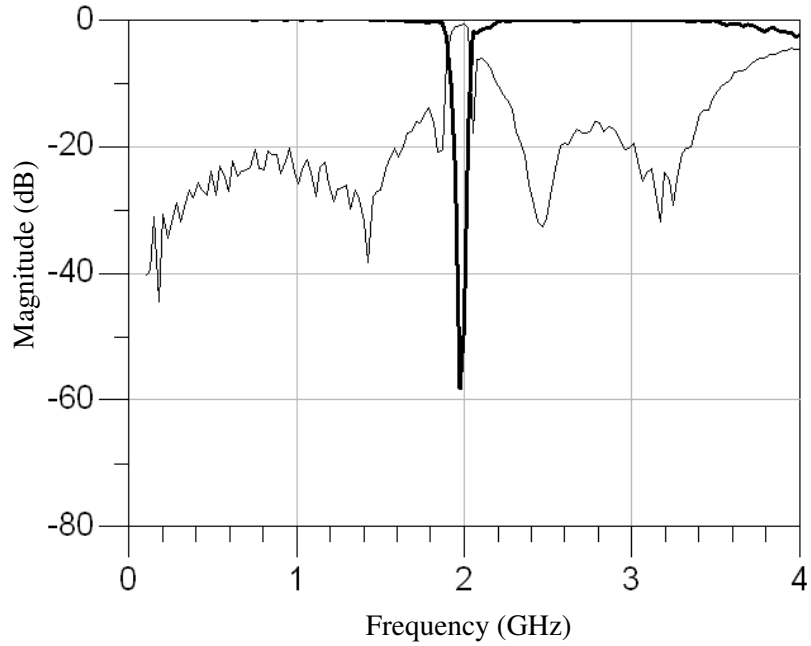
Fig. 4-38: Return loss (thin) and insertion loss (bold) measured results of the 3-pole bandstop filter with low pass filters as impedance inverters.
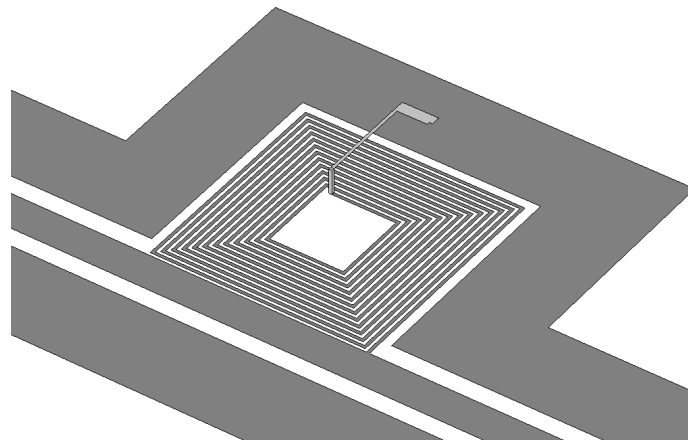
Fig. 4-39: Revised resonator design to improve the return loss characteristics near the rejection band (*z*-direction not to scale)

Chapter 5

Tunable Filter Designs and the Integration of MEMS Devices and HTS Circuits

Three tunable filter designs are presented in this chapter. The manifold-coupled switched multiplexer allows for 2^N filtering options, which is an improvement over the traditional switched filter bank that has $N + 1$ filtering options. The concept of the manifold-coupled switched multiplexer is presented, and a CPW diplexer is simulated, fabricated and tested. This concept is expanded to the design of a superconducting manifold-coupled switched triplexer. The effect of switches is made through EM simulations to achieve the switched triplexer design with 8 possible tuning states. The superconducting triplexers are again implemented to demonstrate a reconfigurable multiplexer design. Finally, a tunable filter design is presented that allows for constant absolute bandwidth to be achieved at discrete values of center frequency.

The hybrid integration of HTS filters and MEMS switches is also investigated A fabrication process for monolithically integrating MEMS devices and HTS circuits is then presented. Care is taken when designing the fabrication process to ensure that the superconducting properties of the thin film HTS material are not degraded. The tunable filter designs in this chapter can be realized with this fabrication process to achieve high Q tunable microwave filters.

5.1 Manifold-Coupled Switched Multiplexers

The spectral efficiency of a microwave system can be improved by implementing adaptive filtering architectures. A switched filter bank allows for bandwidth to be assigned as needed by the microwave system. The filtering provided by a switched filter bank can adapt correspondingly to satisfy the demand in bandwidth.

A diagram of a traditional switched filter bank is shown in Fig. 5-1. This architecture allows for individual bandwidth channels to be selected allowing for a choice of only $N + 1$

filtering options for a system with N channels [65]-[66]. An improvement upon this architecture is to replace the bank of switches with an architecture that allows 2^N filtering options for a system with N channels. These systems provide adaptive filtering while implementing either circulator coupled multiplexers [67] or hybrid coupled multiplexers [68].
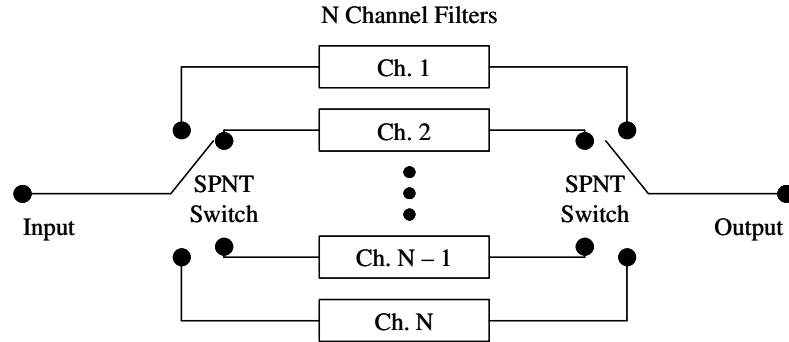
Fig. 5-1: Architecture of a switched filter bank with N + 1 filtering options.
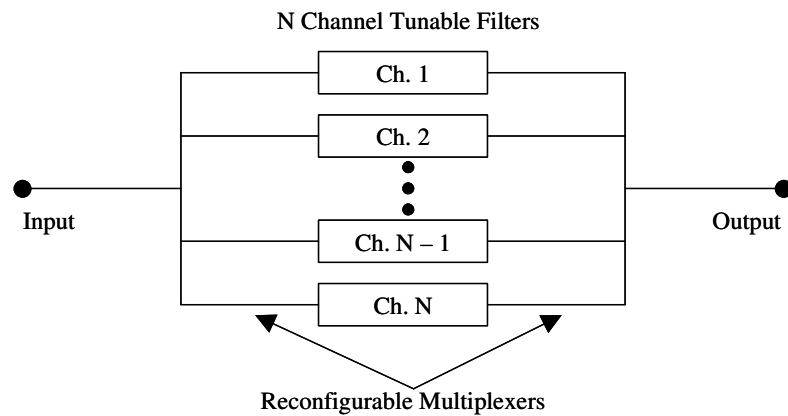
Fig. 5-2: Architecture of a switched filter bank with reconfigurable multiplexers and 2^N filtering options.

In this section, an architecture with reconfigurable multiplexers and tunable filters that can meet the requirement of having 2^N filtering options for a system with N channels is presented. A reconfigurable manifold-coupled multiplexer allows for the channels to be added or removed as determined by the demand for bandwidth. By adding an input

83

multiplexer and an output multiplexer to the channel filters, a two port switched filter bank can be designed with 2^N filtering options, as shown in Fig. 5-2.

This switched filter bank concept is demonstrated by using a reconfigurable diplexer design resulting in four possible states. The three-pole filters and the manifolds are implemented using coplanar waveguide transmission lines. Switches are placed in locations within the filters so as to detune the resonators of the filters while maintaining the out of band reflected phase of the filter.

5.1.1 Reconfigurable Diplexer and Filter Designs

Careful consideration must be taken when designing a reconfigurable manifold multiplexer [69] due to the response of each channel being determined by the response of the other channel filters connected to the manifold. A filter must be switched into a rejection state without affecting the other filters connected to the manifold. It is possible to place switches within the filter itself to achieve this type of tunable filter.

Res. 1   Res. 2   Res. 3   Res. 4   Res. 5   Res. 6   Res. 7

90 degree inverters
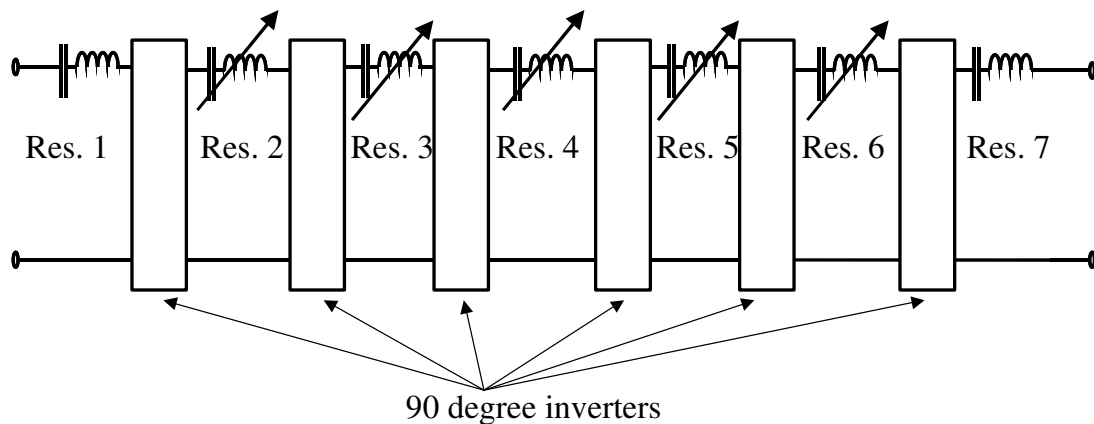
Fig. 5-3: Diagram of a seven-pole filter with its middle resonators made tunable by embedded switches across the capacitors.

In order to not disrupt the other filters connected to a manifold, a filter must be switched off without affecting its out of band phase reflected phase. A switch can be placed on a resonator, which can either bypass a part of the resonator or force it to resonate at a different frequency. To illustrate, Fig. 5-3 shows a circuit model for a seven-pole filter with

embedded switches. A switch can be placed in parallel with either the inductor or the capacitor of these resonators to force the resonator to no longer resonate at the center frequency of the filter.

A lumped element filter, as shown in Fig. 5-3, is designed using a circuit simulator. A seven-pole filter is designed with a percentage bandwidth of 5.8%. The change in out of band phase and the isolation across the filter when bypassing the capacitor of a resonator, as shown in Fig. 5-3, is investigated.
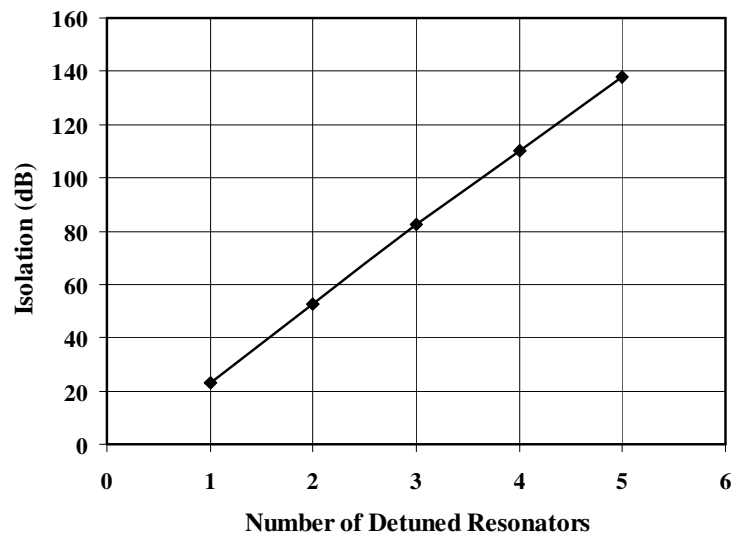
Fig. 5-4: Isolation across a seven-pole filter versus the number of detuned resonators.

First, the isolation across the filter when the resonators are detuned is examined. For a switched filter bank, as shown in Fig. 5-1, the switch alone determines the isolation across the filters. When employing the switched multiplexer design, the isolation across a filter is determined by the number of detuned resonators. The isolation across the filter for the circuit shown in Fig. 5-3 when the resonators are detuned for a different number of resonators is shown in Fig. 5-4. Detuning only one resonator gives an isolation of approximately 23 dB, and detuning two resonators results in an isolation of 53 dB.

Next, the change in out of band reflected phase when the filter is detuned is investigated. The change in phase at the 3 dB, 10 dB and 20 dB rejection points of the filter are shown in

Fig. 5-5. The position of the detuned resonator within the filter has an impact on the response of the switched filter bank. The farther away a detuned resonator is from the input port, the less effect it has on the reflected out of band phase. Position 2 would be the second resonator, as seen from port 1 of the filter. Position 6 would be the sixth resonator as seen from port 1, but it is also the second resonator as seen from port 2 of the filter. When a detuned resonator is further from the input port, it has less effect on the reflected phase. Since there is a manifold on either end of the filter, it is best to detune the resonators symmetrically about the middle of the filter. This results in a trade-off between the number of resonators that need to be detuned to reach an isolation requirement and the position of the detuned resonators within the filter as to not disrupt the manifold design when the filters are switched into their off states.
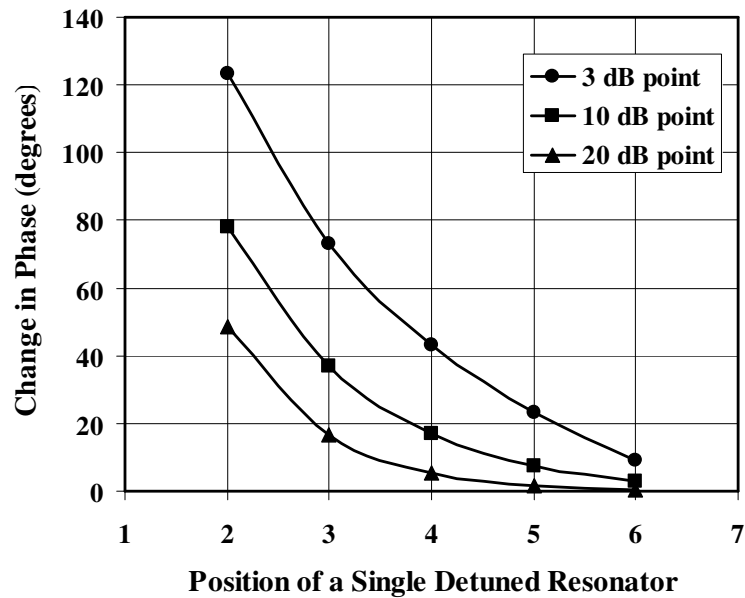
Fig. 5-5: The change in out of band reflected phase for a seven-pole filter at different points of out of band rejection versus which resonator is detuned as seen from port 1 of the filter.

5.1.2 Diplexer and Filter EM Simulations

The filters designed for this switched filter bank are interdigital coplanar waveguide filters. The lower band filter is designed to have a center frequency of 9.5 GHz, and the higher band

filter is designed to have a center frequency of 10.5 GHz. Both filters have a bandwidth of 500 MHz. A single-pole-single-throw (SPST) switch can be incorporated into this design to detune the resonator. In the case of using a $\lambda/4$ transmission line resonator, which is shorted at one end and has a switch placed across its open end to ground, the actuation of the switch causes the transmission line to resonate at its $\lambda/2$ frequency. This new frequency is twice that of the center frequency of the filter, which effectively results in a detuned resonator. The EM simulations include a wire from the open end of the resonator to ground to model the SPST switch.
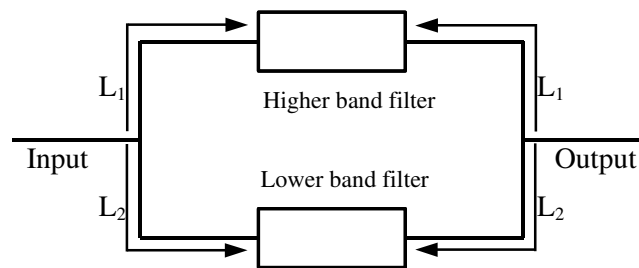
Fig. 5-6: Diagram of the switched diplexer design.

The CPW filters and diplexers are simulated with the EM simulator Sonnet. CPW transmission lines make up the diplexer design. The length of transmission line L_1, as shown in Fig. 5-6, is determined by the reflected phase from the higher band filter at the center frequency of the lower band filter. The length of L_2 is determined similarly, but from the reflected phase of the lower band filter at the center frequency of the higher band filter.

The filter simulations and diplexer simulations are joined together in a circuit simulator to get the overall simulation results of the switched filter bank. The simulation results of the switched filter bank for the four states with the three-pole filters are shown in Fig. 5-7. In the off state of the lower band channel, an isolation of approximately 16 dB is seen across the filter. The leakage of signal in this case is due to the coupling from the first resonator to the last resonator across the detuned middle resonator. The isolation can be improved with different resonator designs, or in the case of using a higher order filter, by detuning more resonators in the filter.

5.1.3 Filter Bank Measurements

The switched filter bank is fabricated on an alumina substrate with gold metallization. A wire bond connected from the open end of the middle resonator to the ground of the CPW transmission line realizes the switch needed to detune a resonator.

a)

b)
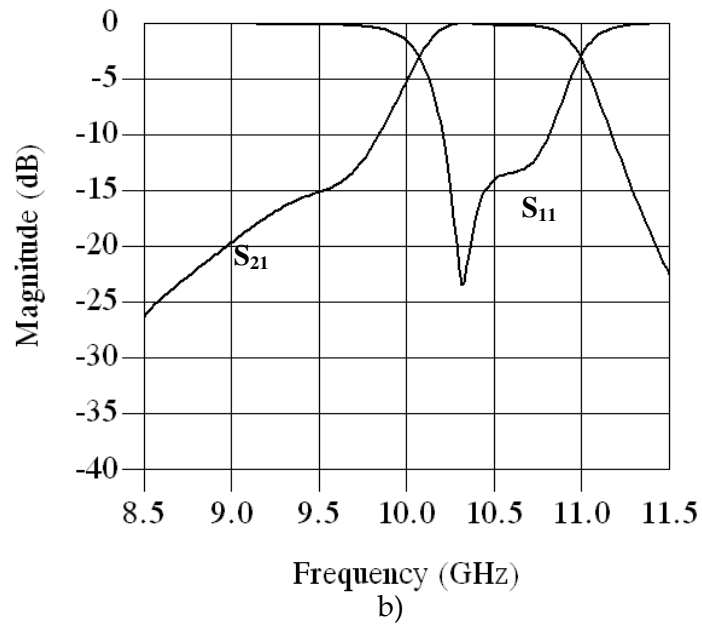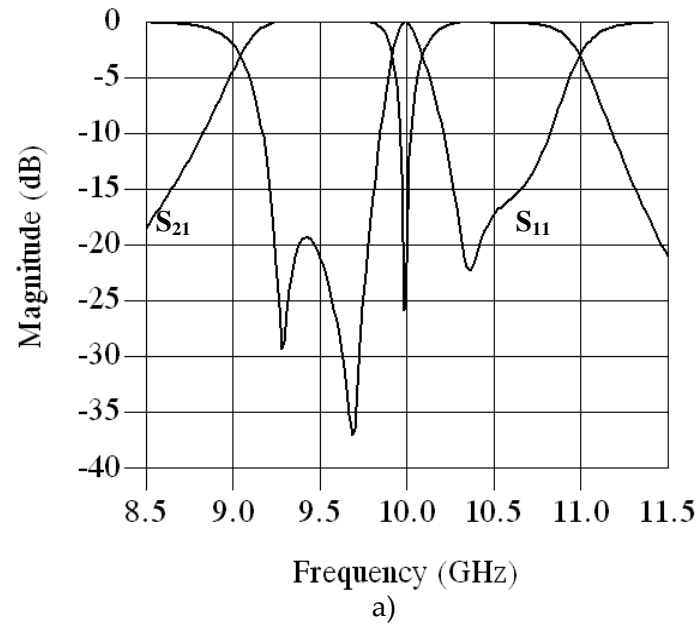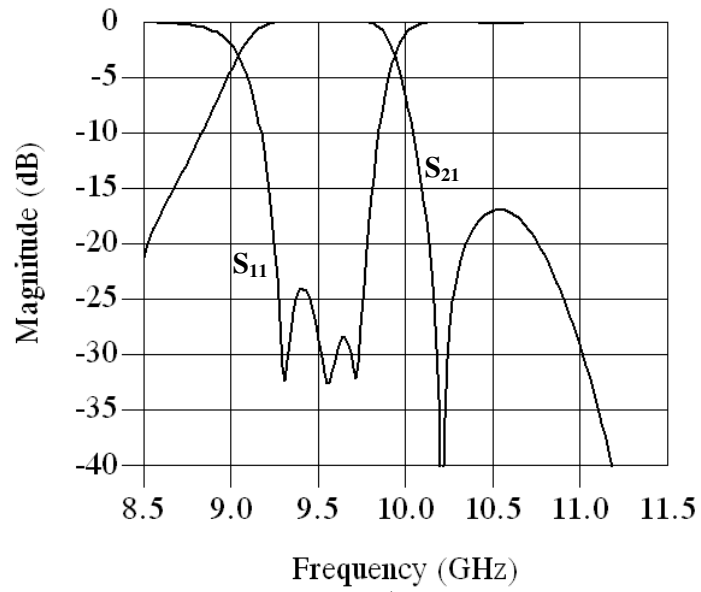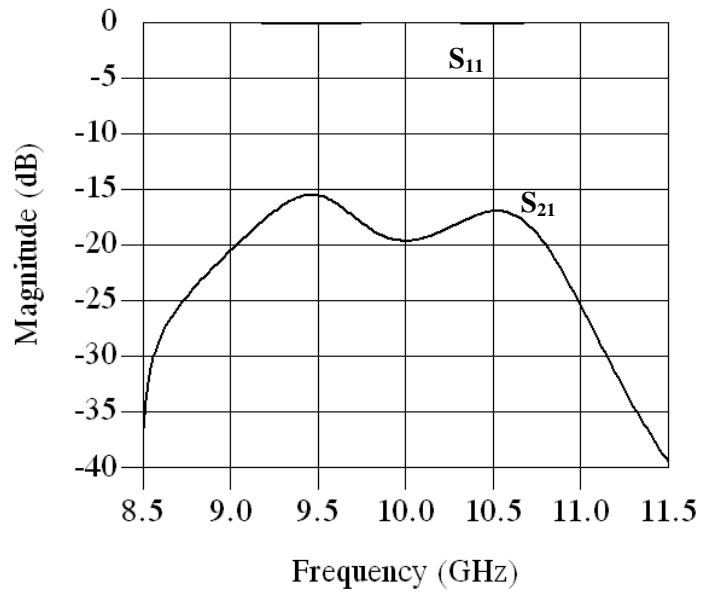
Fig. 5-7: EM lossless response of the filter bank for the 3-pole filters. a) both channels ON, b) only the higher channel ON, c) only the lower channel ON and d) both channels OFF.

An image of the final design is shown in Fig. 5-8. The measured response of the switched filter bank with both channels on and the measured responses of the two individual filters

are shown in Fig. 5-9. The measured responses of the other three states of the switched filter bank are shown in Fig. 5-10.
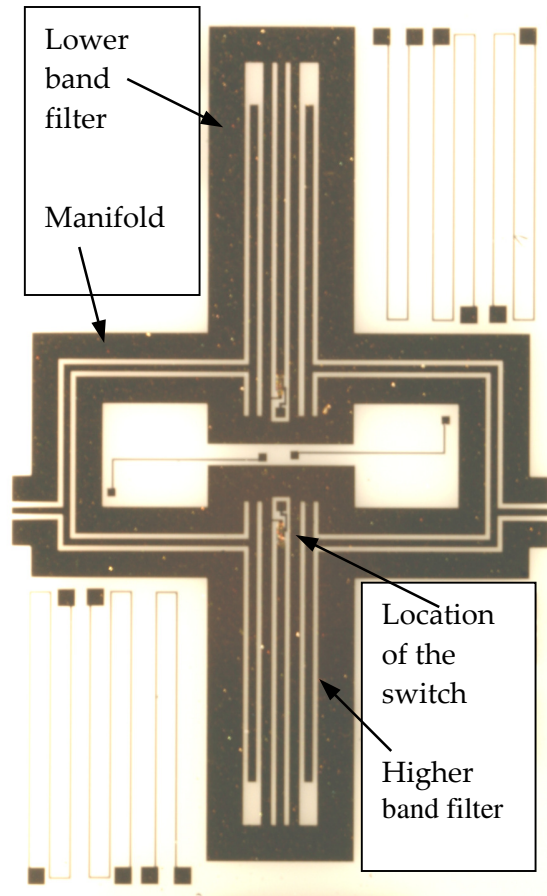
Fig. 5-8: Image of the final switched filter bank design with the diplexers and the two filter channels.

The feasibility of realizing a manifold-coupled switched filter bank with 2^N states has been demonstrated. Switches are embedded in the resonators for detuning. By detuning the middle resonator of a filter, the filter can be in a rejection state while not interfering with the other filters connected to the diplexer. This is due to the out of band reflected phase being maintained when the filter is detuned. As is discussed in the next section, this concept can be expanded to a multiplexer design with multiple channels.
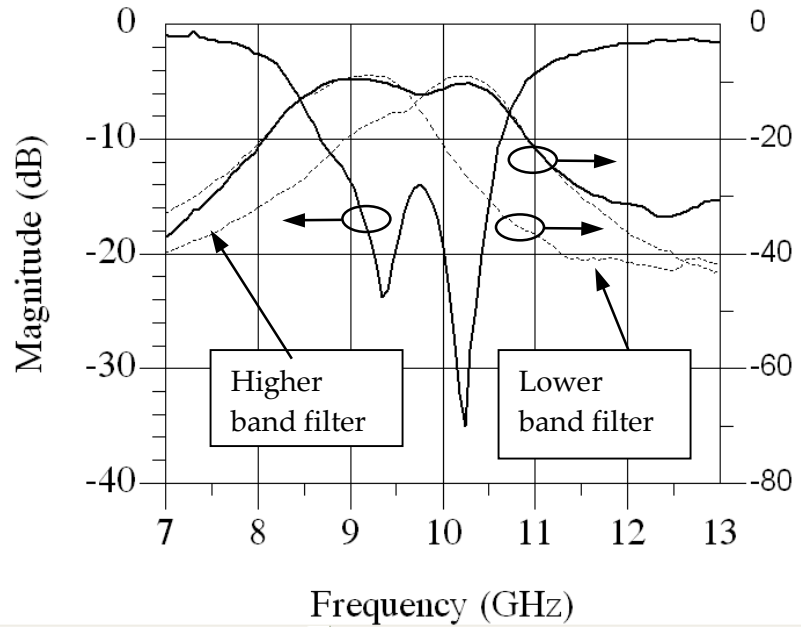
Fig. 5-9: Measured response of the switched filter bank with both channels ON (bold) and the two filters tested individually (dashed) without being connected to the manifold.
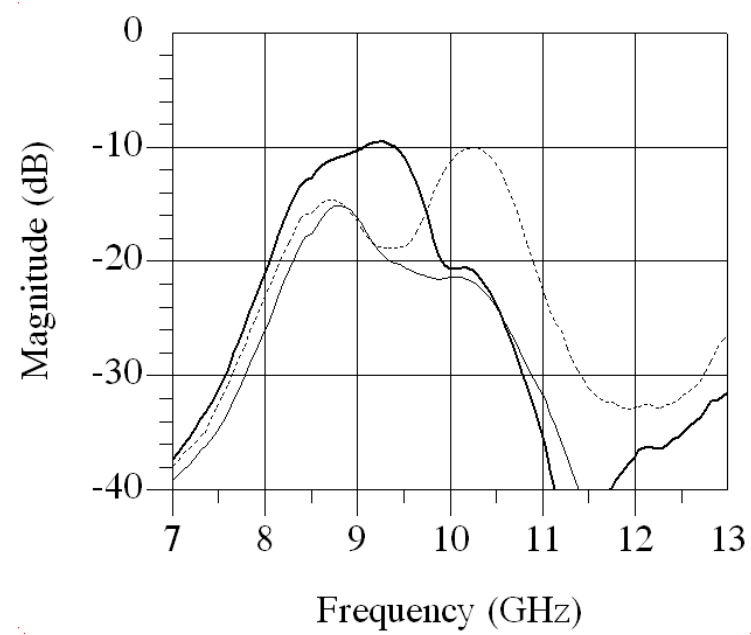
Fig. 5-10: Measured response of the switched filter bank with only the lower channel ON (bold), only the higher channel ON (dashed) and both channels OFF (thin).

5.2 Tunable Superconducting Triplexer

The concept of the manifold-coupled switched multiplexer is expanded with the design of a switched triplexer implementing superconducting filters. A traditional three channel multiplexer with one input and three outputs is designed, fabricated, and tested. Another version of the triplexer is designed with one input and one output. This version of the triplexer demonstrates the concept of the manifold-switched multiplexer. A reconfigurable multiplexer is shown through EM simulations and test results of the traditional multiplexer design.

5.2.1 Triplexer Channels

The three bands of the triplexer are made up of the bands of the Link 16 communication system. The Link 16 system uses one large frequency band from 960 MHz to 1215 MHz made up of smaller sub-bands. The identification, friend, or foe (IFF) transponders used by civilian and military aircraft operate at 1030 MHz and 1090 MHz. These two frequencies fall within the Link 16 frequency band and must be filtered. One method of filtering these two unwanted signals is to implement a triplexer with a manifold at both the input and the output. The three bands of the triplexer are given in Table 5-1.

Table 5-1: Frequency range of the three channels.

Band	Lower frequency range (MHz)	Higher frequency range (MHz)	Center frequency of the band (MHz)
Channel 1	960.0	1017.5	988.3
Channel 2	1042.5	1077.5	1060.0
Channel 3	1102.5	1215.0	1157.4

Eight pole Chebyshev filters are used to achieve the desired rejection between the three filter bands. Each of the three filters is designed using a compact resonator design [51] and is implemented with high temperature superconducting thin films on a 508 µm thick

lanthanum aluminate (LaAlO$_3$) wafer. As mentioned in section 3.4, the resonators of the channel 3 filter are flipped to achieve higher coupling given the wider bandwidth.

5.2.2 Manifold-Coupled Switched Triplexer

The triplexer design starts with the design of three doubly loaded 8-pole filters. Three filters are designed based on the frequency specifications given in Table 5-1 using the reflected group delay design method as described in section 3.4. The next step in this design is to find a first approximation of the manifold as shown in Fig. 5-11.
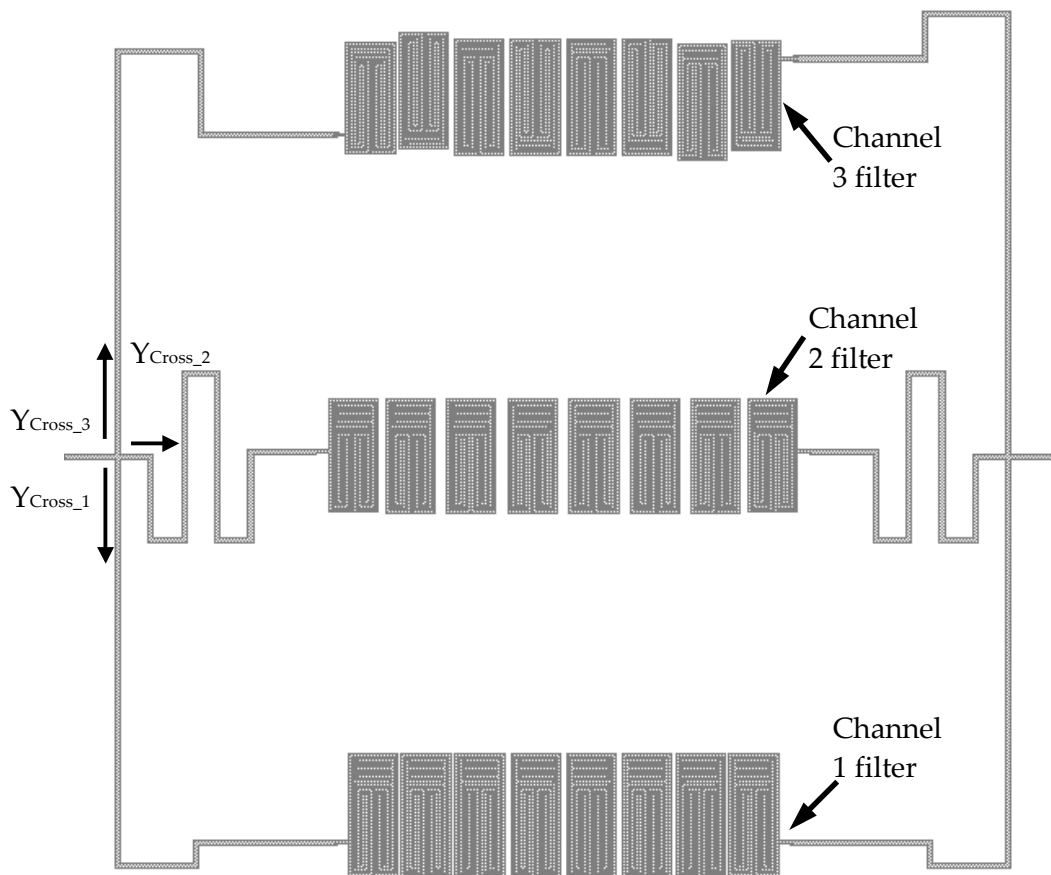
Fig. 5-11: Layout of the two port triplexer.

One can easily get a perfect match at the center frequency of each filter by solving a simple set of equations. At the center frequency of the first filter, the sum of the admittances at the cross-junction of the other two paths must equal zero. This can be written as

$$Y_{Cross\_2f1} + Y_{Cross\_3f1} = 0, \tag{5.1}$$

where Y_{Cross_2f1} is the admittance at the cross-junction of the path to the second filter at the center frequency of the first filter. From transmission line theory, we know that

$$Y = Y_0 \left(\frac{1-\Gamma}{1+\Gamma} \right), \tag{5.2}$$

where Γ is the reflection when looking at the load admittance Y. Putting (5.2) into (5.1), we get

$$Y_0 \left(\frac{1-\Gamma_{Cross\_2f1}}{1+\Gamma_{Cross\_2f1}} \right) + Y_0 \left(\frac{1-\Gamma_{Cross\_3f1}}{1+\Gamma_{Cross\_3f1}} \right) = 0. \tag{5.3}$$

This can be further simplified to

$$\frac{2\left(1-\Gamma_{Cross\_2f1}\Gamma_{Cross\_3f1} \right)}{1+\Gamma_{Cross\_2f1} + \Gamma_{Cross\_3f1} + \Gamma_{Cross\_2f1}\Gamma_{Cross\_3f1}} = 0. \tag{5.4}$$

The denominator cannot make the left hand side of the equation become zero when implementing passive transmission lines and filters, so it can be disregarded. We then have

$$\Gamma_{Cross\_2f1}\Gamma_{Cross\_3f1} = 1 = e^{j0}. \tag{5.5}$$

The reflection coefficient of the transmission line connected to the second filter at the cross junction is

$$\Gamma_{Cross\_2f1} = \Gamma_{2f1}e^{-j2\theta_{TL2f1}}, \tag{5.6}$$

where Γ_{2f1} is the reflection coefficient of the second filter at the center frequency of the first filter having a phase θ_{2f1}, and θ_{TL2f1} is the electrical length at the center frequency of the first filter of the transmission line connecting the second filter to the cross-junction. We then get the following

$$\theta_{2f1} + \theta_{3f1} - 2\theta_{TL2f1} - 2\theta_{TL3f1} = 0 \,. \tag{5.7}$$

At the center frequencies of the other two filters, we get

$$\theta_{1f2} + \theta_{3f2} - 2\theta_{TL1f2} - 2\theta_{TL3f2} = 0 \,, \tag{5.8}$$

and

$$\theta_{1f3} + \theta_{2f3} - 2\theta_{TL1f3} - 2\theta_{TL2f3} = 0 \,. \tag{5.9}$$

Since the electrical length of an ideal transmission line has a simple linear relationship with frequency, there is a set of three equations and three unknowns. The electrical lengths of the three transmission lines, θ_{TL1f1}, θ_{TL2f1}, and θ_{TL3f1}, are easily computed and serve as a good starting point for the multiplexer design. Using this as an initial design gives a good match at the center frequency of each channel, but not a good match across the entire band. Though, this method serves as a very good starting point for non-contiguous narrower band multiplexer designs.

The final design for the triplexer is achieved through optimization. The input coupling and the coupling between the first two resonators are optimized along with the dimensions of the manifold to achieve the final design. The filters and the manifold are simulated separately using the EM simulator Sonnet, and the s-parameters of all of these networks are joined with a circuit simulator to get the s-parameters of the entire triplexer. The insertion loss simulation results are shown in Fig. 5-12, and the return loss simulation results are shown in Fig. 5-13. The filters and manifolds are fabricated, and the triplexer is assembled in a housing as shown in Fig. 5-14. The filters and manifolds are connected together with wire bonds. The filters are cooled to a temperature of 77 K and the insertion loss and return loss test results are shown in Fig. 5-12 and Fig. 5-13, respectively. The measured results are very close to the simulation results.
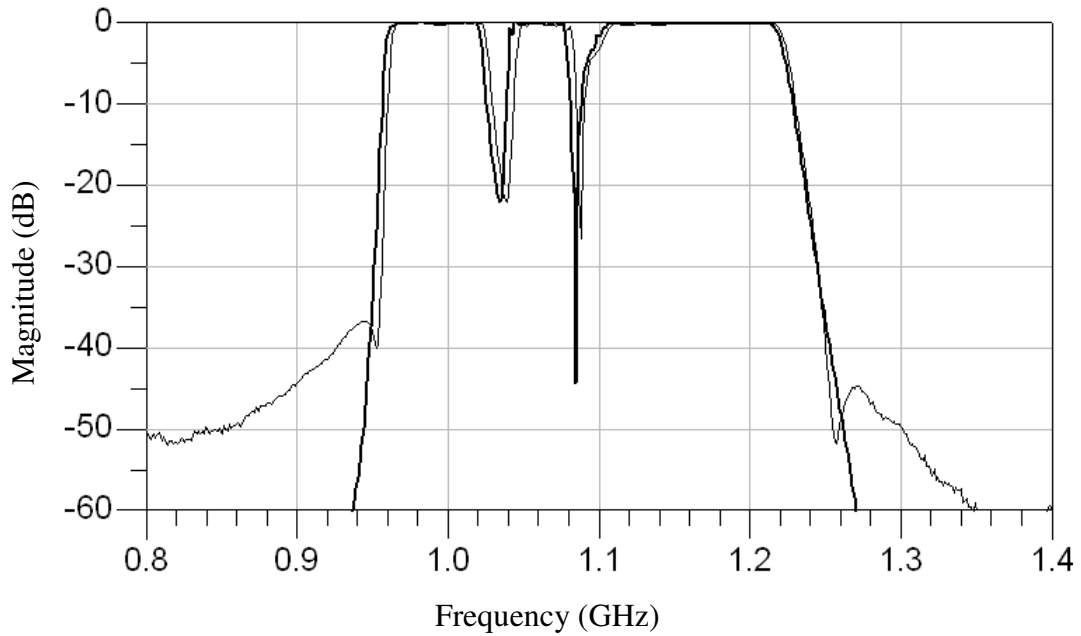
Fig. 5-12: Insertion loss simulation results (bold line) and test results (thin line) of the 1-1 multiplexer.
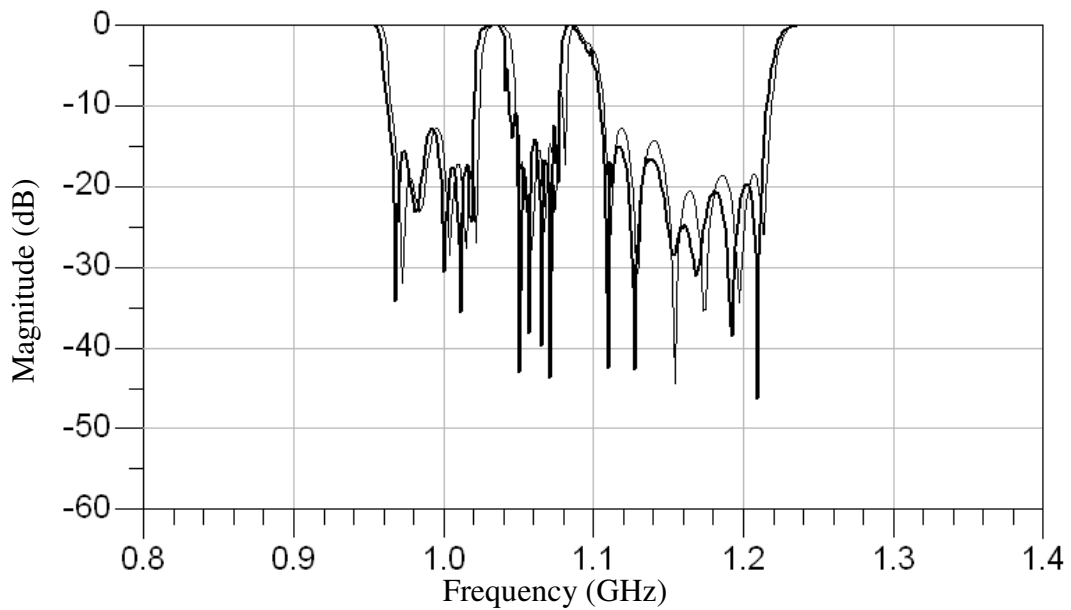
Fig. 5-13: Return loss simulation results (bold line) and test results (thin line) of the 1-1 multiplexer.
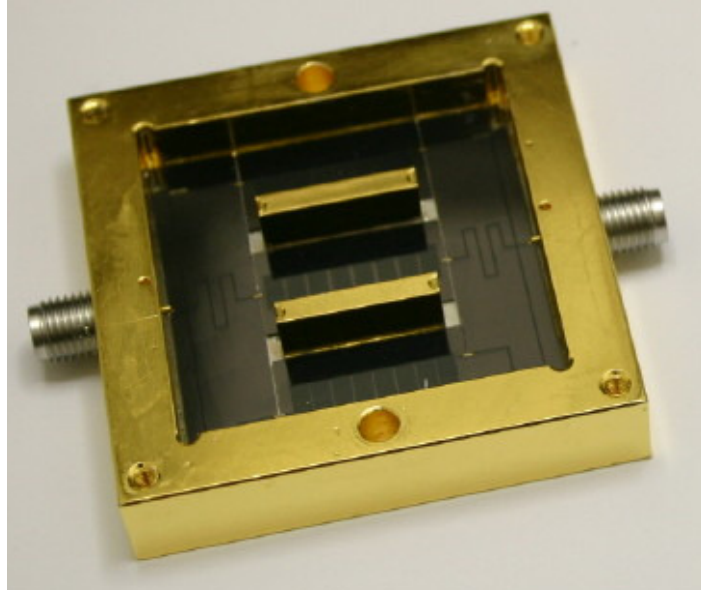
Fig. 5-14: Image of the one input/one output three channel multiplexer.

To further demonstrate the application of the manifold-coupled switched multiplexer, simulations are performed with the above triplexer. To achieve the required detuning of the resonators, a piece of wire is placed across the capacitor portion of the resonator. An image of this shorted wire is shown in Fig. 5-15. Simulations are performed on each filter with a different number of detuned resonators. Since the triplexer is symmetric, the resonators are detuned in pairs. Either the middle two, middle four or middle six resonators are detuned in the simulations. The EM simulations are then added to the EM simulations of the manifold in a circuit simulation. Fig. 5-16 shows the change in rejection of the second channel as the number of detuned resonators is changed. With the two middle resonators detuned, the rejection of the middle channel is approximately 40 dB. By increasing the number of detuned resonators to four, the rejection increased to 60 dB. With the middle six resonators detuned, the rejection is approximately 80 dB. Since this middle filter is a narrow band 8-pole filter, the other two channels are not affected by the detuning of the resonators. This is shown in Fig. 5-17 as the return loss changes very little with the detuning of the middle filter.

A manifold-coupled switched multiplexer is demonstrated with HTS microstrip filters and transmission lines. The test results of the multiplexer are shown to validate the accuracy of the EM simulations. The switch could take the form of a MEMS cantilever beam that is fabricated monolithically with the HTS filters, as described in section 5.4.

Extra piece of metal detunes the resonator
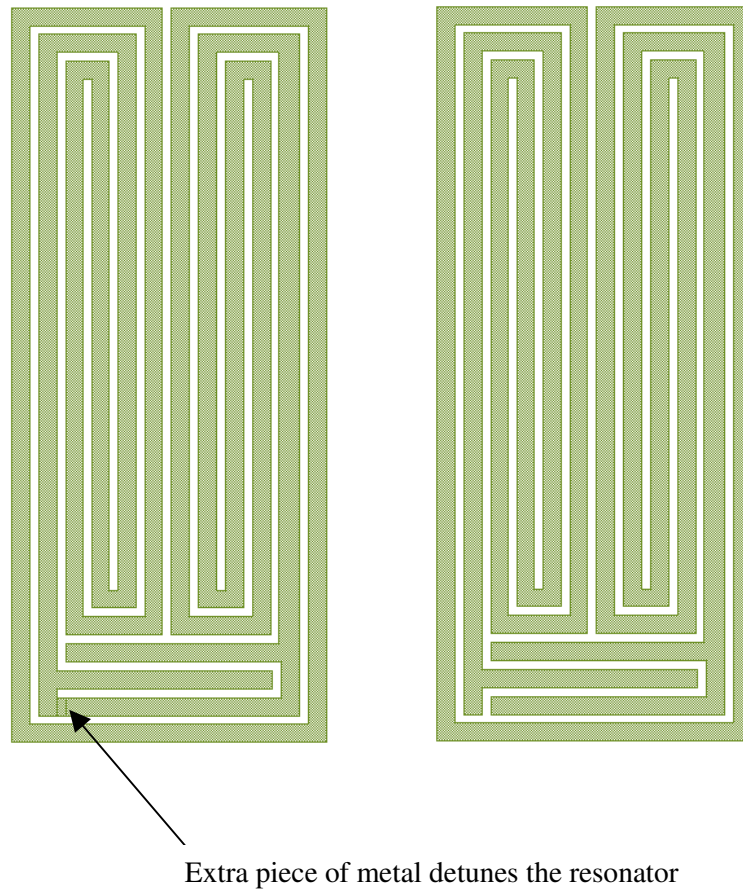
Fig. 5-15: The regular resonator on the right and a detuned resonator on the left.
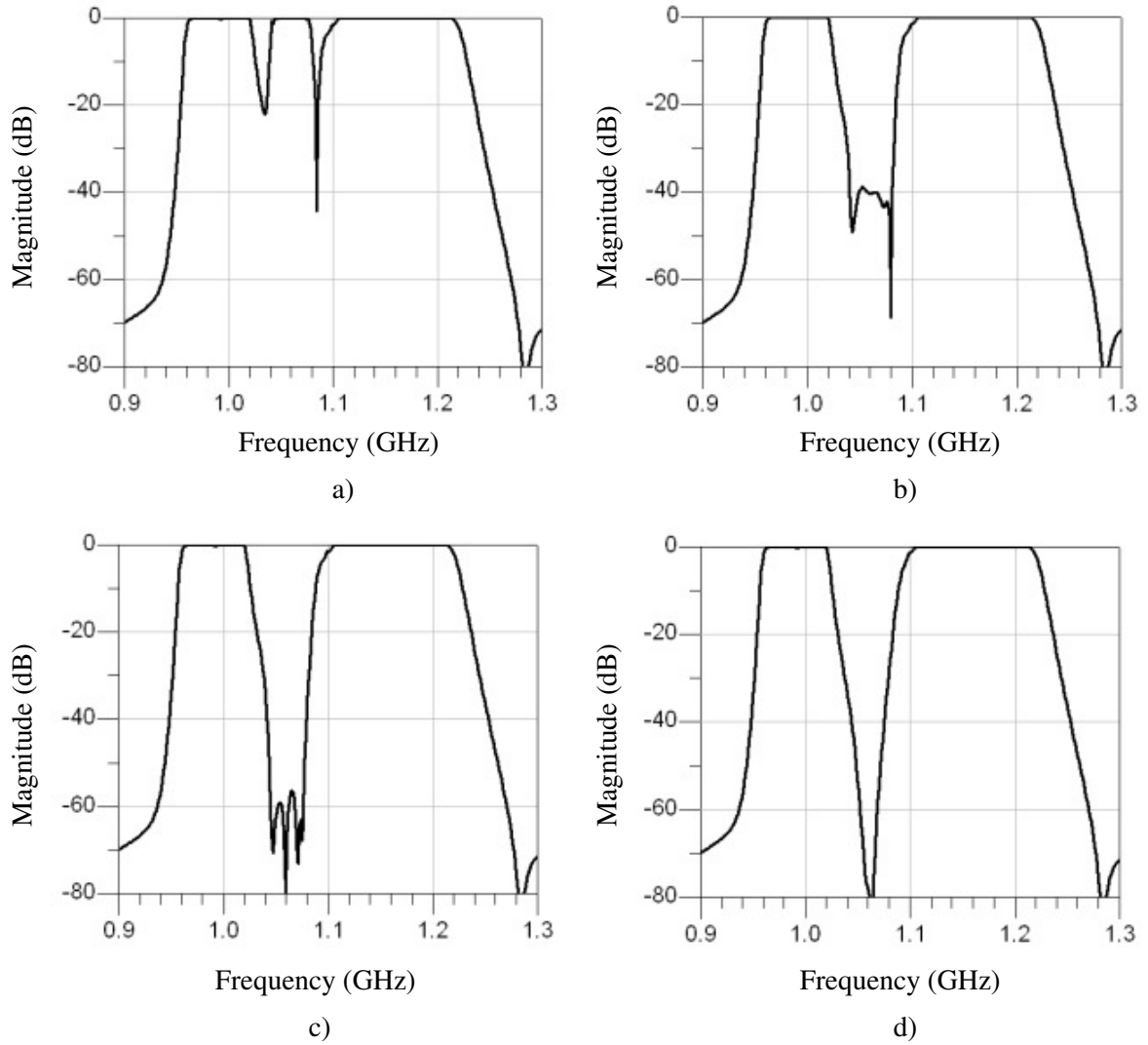
Fig. 5-16: Insertion loss EM simulations results of the manifold-coupled switched multiplexer with a) no detuned resonators, b) the two middle resonators of the middle channel detuned, c) the four middle resonators of the middle channel detuned d) and the six middle resonators of the middle channel detuned.
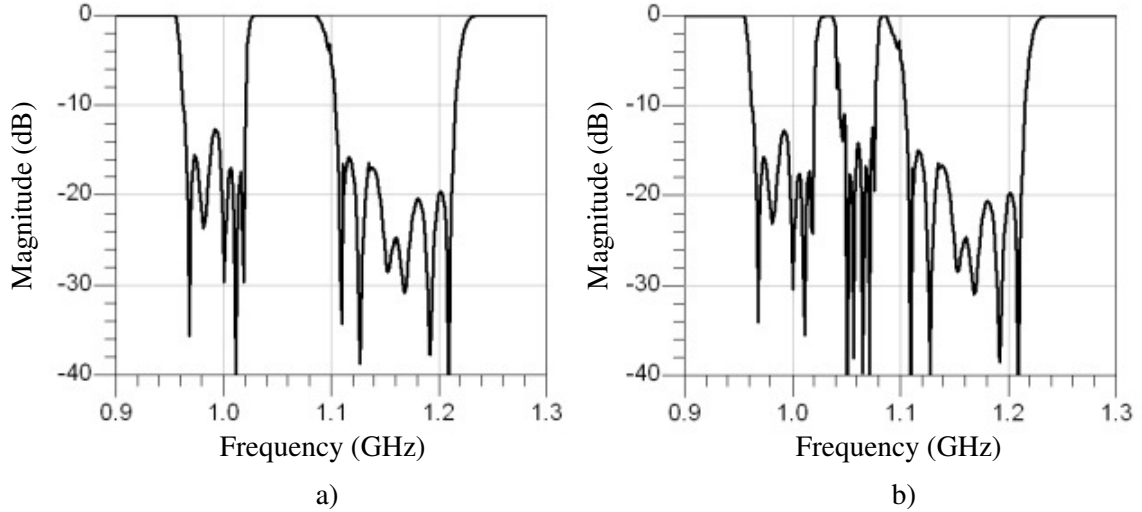
Fig. 5-17: Return loss EM simulations results of the manifold-coupled switched multiplexer
with a) no detuned resonators and b) the six middle resonators of the middle channel
detuned.

5.2.3 Superconducting Reconfigurable Multiplexer

A superconducting reconfigurable multiplexer is also designed using a similar approach to
that of the previous section. The three channels, listed in Table 5-1 from the previous section
are again used to design this reconfigurable multiplexer. Measured results of the
multiplexer and simulated results of the reconfigurable multiplexer are given to illustrate
the design.

A reconfigurable multiplexer is a multiplexer in which the different channels can be
connected or disconnected depending on the demand of the user [69]. The channel filters
are broken into head and tail portions where the head connects to the manifold and the tail
connects to the output of the channel. When disconnecting a channel from the manifold, the
tail of the filter is replaced with a short-circuiting plate, as in the case of a waveguide filter.
The portion of the filter that makes up the head of the filter is determined by what portion of

the filter can be replaced by a short while not disrupting the other channels of the multiplexer. This analysis is similar to that found in section 5.1.1.

The three channel filters are first designed to be matched to an impedance of 50 Ω at both ports. The "heads" of the filters are then connected to a manifold and the manifold and the filters and optimized. The "tail" end of each filter remains connected to a 50 Ω load during the optimization process. The input coupling and the coupling between the first and second resonators are changed during this optimization process. The final assembled multiplexer is shown in Fig. 5-22. The simulation and measured results of the multiplexer are shown in Fig. 5-18 and Fig. 5-19, respectively
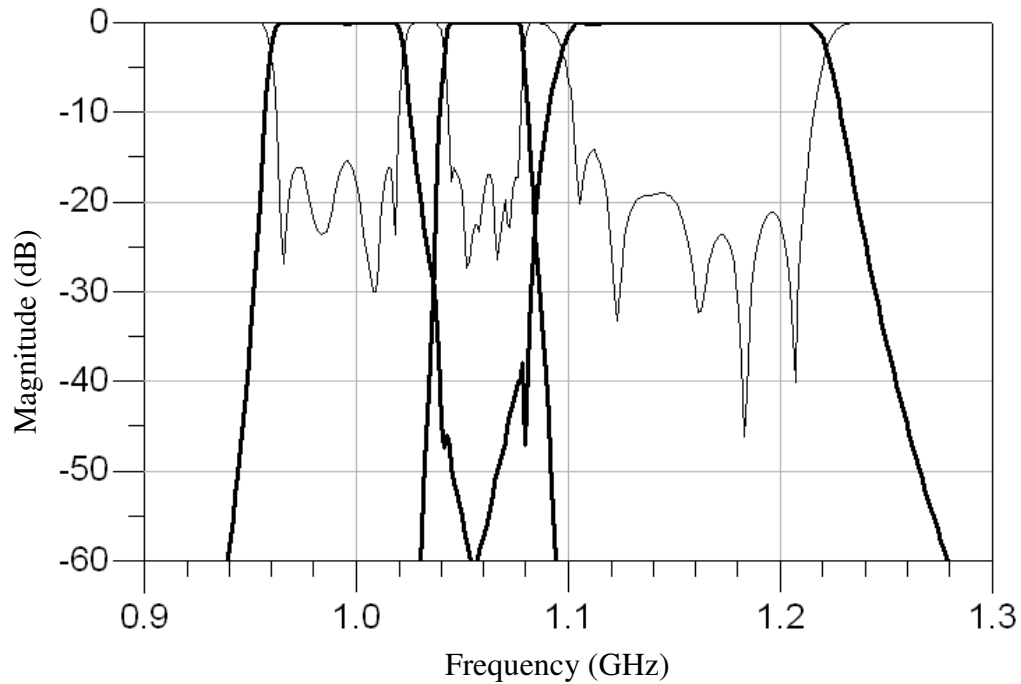
Fig. 5-18: The simulation results of the three channel multiplexer with the return loss of the common port (thin line) and the insertion loss of the three channels (bold lines).
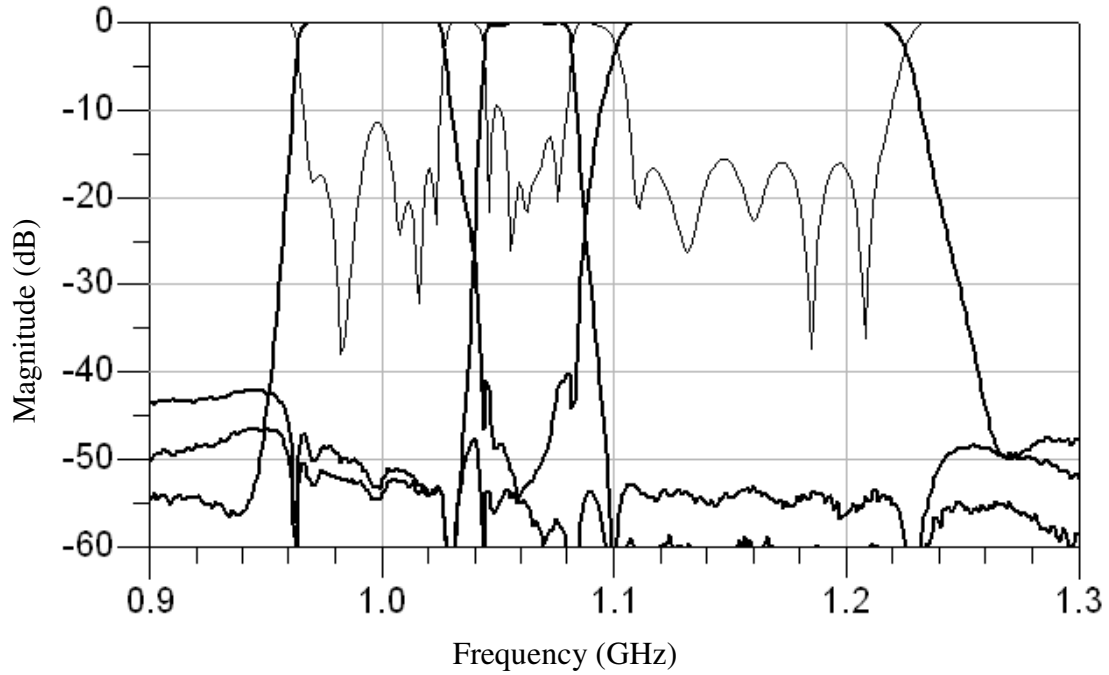
Fig. 5-19: The measured results of the three channel multiplexer with the return loss of the common port (thin line) and the insertion loss of the three channels (bold lines).

The act of replacing the tail end of the filter with a short circuit is achieved by shorting the capacitor of the resonators of the filters. This short circuit is similar the one shown in Fig. 5-16. When detuning the resonators for this reconfigurable multiplexer, the highest priority is in maintaining the response of the all the other channels when one channel is turned off. The resonator connected directly to the manifold and the second resonator, which make up the head portion of the filters, are not detuned to maintain the response of the other channels. The third through eighth resonators, making up the tail end of the filters, are detuned with the short circuit to turn the channel off. The simulation results with the first and third channels turned off are shown in Fig. 5-20 and Fig. 5-21
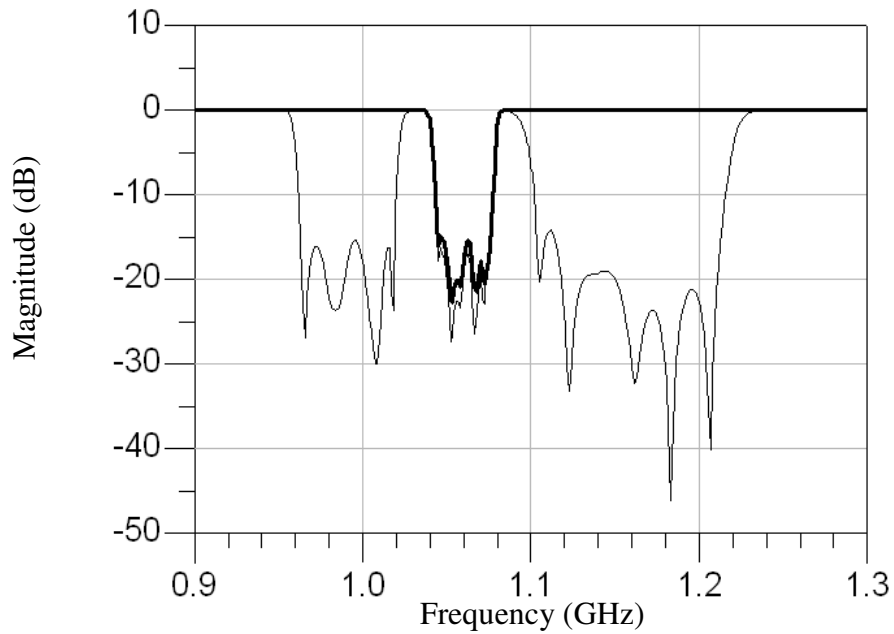
Fig. 5-20: Return loss simulation results of the common port with all the channels on (thin line) and only the second channel on (bold line).
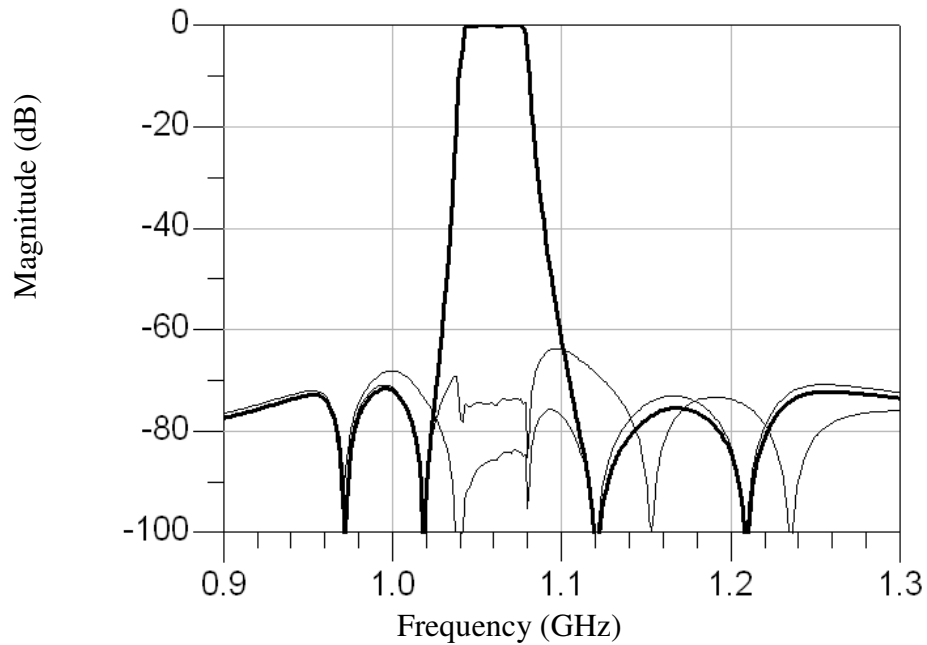
Fig. 5-21: Insertion loss simulation results of the second channel (bold line) which is on and the first and third channels (thin lines) which are off.
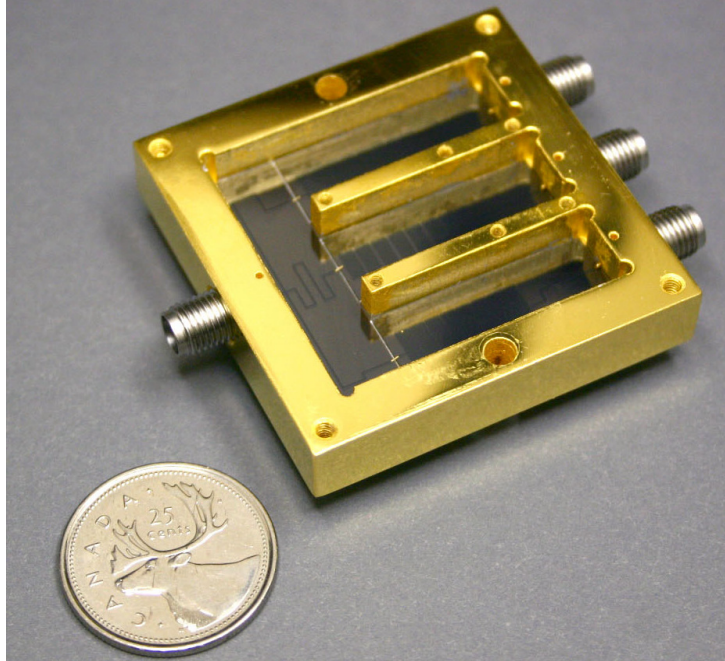
Fig. 5-22:Image of the high temperature superconducting triplexer.

5.3 Tunable Filters with Constant Absolute Bandwidth using Embedded Switches

Embedding switches within the resonators of a filter can be used to realize tunable filters with constant absolute bandwidth or any specified bandwidth. The use of switches results in a fixed number of states, each having a specified center frequency and bandwidth. The space required for all the filters is equal to that of the channel with the lowest center frequency. Switches embedded within the resonators allow for the switching between the different channels. Other methods utilize SPNT switches and a total of N filters, which takes up considerable room as compared to the tunable filter presented in this section. A two state tunable bandpass filter is designed with the concepts demonstrated through EM simulations.

Tunable filters with a constant absolute bandwidth at different values of center frequency are realized with the use of switches embedded within the resonators. The switches allow for the input coupling and the inter-resonator coupling to be tuned resulting in tunable states at different center frequencies and bandwidths. When tuning the filter across

different center frequencies, the absolute bandwidth can be kept constant or it can be designed to have a specific bandwidth at each center frequency. Two switches are used on each resonator for each tuning state of the filter. This is in contrast to other designs that only use one switch or load just one end of the resonators.

The input coupling of a filter can be made to be tunable by using a tap coupling and a switch at each end of the first resonator. The length of a microstrip transmission line resonator mostly affects the resonant frequency of resonator, and the position of the tap mostly affects the bandwidth and return loss value of the filter response. By placing switches at the open ends and the shorted ends of the resonators of an interdigital filter, the filter can have two states that have two different center frequencies and two arbitrary bandwidths.

This concept will be demonstrated with the design of a filter with two states, one with a center frequency of 9 GHz and the other having a center frequency of 10 GHz. Both states have a bandwidth of 1 GHz, thus keeping the absolute bandwidth constant across the tuning range of the filter. The concept is presented by showing EM simulations of interdigital microstrip resonators. A coplanar waveguide filter with MEMS switches is designed with EM simulations for fabrication on an alumina wafer.

5.3.1 Tuning the Input Coupling and Inter-Resonator Coupling with Embedded Switches

The input coupling and inter-resonator need to be adjusted at the different tuning states to achieve the desired filter response. Switches embedded within the resonators allow for this adjustment. EM simulations are performed on microstrip resonators to demonstrate how the ideal coupling values are achieved when tuning the filter.

The simulations are performed for a microstrip interdigital filter using an alumina wafer with a dielectric constant of 9.9 and a thickness of 508 µm. The tunable filter is designed to have two passbands, one at 9 GHz and the other at 10 GHz, each having an absolute bandwidth of 1 GHz. EM simulations are performed to demonstrate how the correct input coupling and the correct inter-resonator coupling can be achieved for both states.

105

The input coupling is realized by a tap input to the first microstrip resonator. When changing from one state to another, the resonator length needs to be changed and the position of the tap needs to be changed. If a switch is used only at one end of the resonator, the length of the resonator will be correct, but the position of the tap will not be correct if the absolute bandwidth is to remain the same. A second switch can be introduced at the other end of the resonator to achieve both the correct length and the correct tap position.

The tap position for the two states and the positions of the two switches are determined with EM simulations. The tap position is determined by matching the reflected group delay at the center frequency of the filter. Since the desired group delay value is independent of center frequency, the reflected group delay should be the same at both center frequencies. For a 3-pole Chebyshev filter with a bandwidth of 1 GHz, this desired value of group delay is 0.417 ns. The input tap position of for each filter is determined, and the layouts for the two filters, which show the dimensions of the resonator for each state, are illustrated in Fig. 5-23.

One switch can be placed approximately 210 μm from the open end of the resonator. This switch could be an SPST switch, which would be in the closed position for the lower band. The other switch can be located at approximately 130 μm from the shorted end of the resonator. This switch could either be an SPDT switch or an SPST switch. The SPST switch would go to ground through a via and would be in the closed position for the higher frequency band. The SPST switch would switch from the small end of the resonator to ground through a via when changing from the lower band to the higher band. This analysis is performed assuming an ideal switch with no physical size. When implementing a real switch, its size and parasitic elements must be considered in the filter design, as they can limit the number of states and the difference in frequency between adjacent channels.
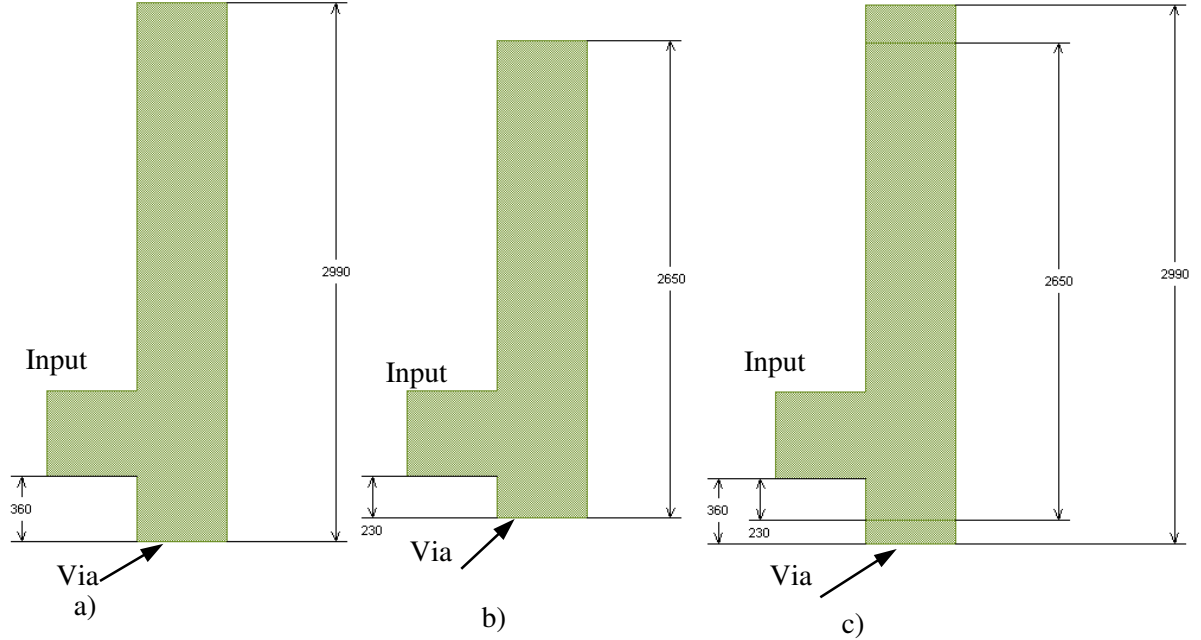
Fig. 5-23: a) Layout of the first resonator at 9 GHz, b) layout of the first resonator at 10 GHz, and c) the two layouts at 9 GHz and 10 GHz imposed on each other to demonstrate the position of the switches (dimensions are in µm).

The proper coupling is determined by weakly coupling into two adjacent resonators and by determining coupling coefficient by simulating the magnetic and electric coupling frequencies. The coupling coefficient is found from

$$k_{ij} = \frac{f_e^2 - f_m^2}{f_e^2 + f_m^2},$$
(5.10)

where f_e and f_m are the electric and magnetic coupling frequencies, respectively. The desired value of the coupling coefficient is

$$k_{ij} = \frac{BW}{f_0 \sqrt{g_i g_j}},$$
(5.11)

where BW is the absolute bandwidth, f_0 is the center frequency, and g_i and g_j are the low pass prototype values of the filter.
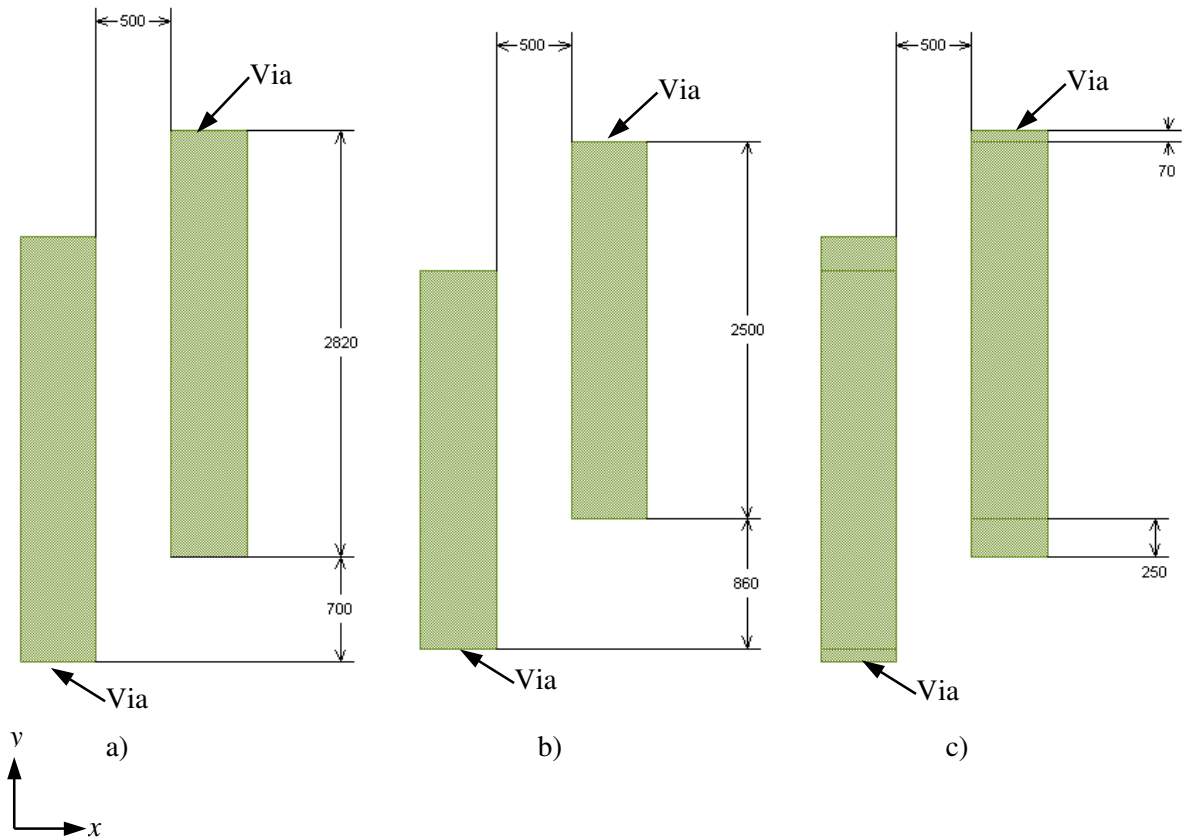
Fig. 5-24: a) Layout of two resonators for the lower band, b) layout of two resonators for the higher for the same absolute bandwidth, and c) the two layouts superimposed to show the position of the switches (dimensions are in μm).

The values of the coupling coefficients are 0.13553 and 0.12197 for the lower and higher frequency bands, respectively. The dimensions of the resonators are determined for the lower band first, then the higher band resonator and made to fit within the dimensions of the lower band filter. For example, the gap separating the two resonators is kept the same. The change in coupling is achieved by changing the offset in the *y*-direction, as shown in Fig. 5-24, between the resonators instead of changing the *x*-direction gap between the resonators. As shown in Fig. 5-24, the higher band resonators fit within the resonator sizes of the lower band filter. Switches similar to those discussed for the case of the input

coupling can be included on these resonators to achieve the two state tunable filter. A two state filter is designed and the simulation results are shown in the following section.

5.3.2 Two State Filter Design and EM Simulations

A tunable two state filter is designed and is demonstrated through EM simulations. The filter with a center frequency of 9 GHz is designed first, with the second filter being designed to fit within the dimensions of the first filter. An iterative process is used to account for the parasitic effects of the MEMS switches. The simulation results of the two states are shown.
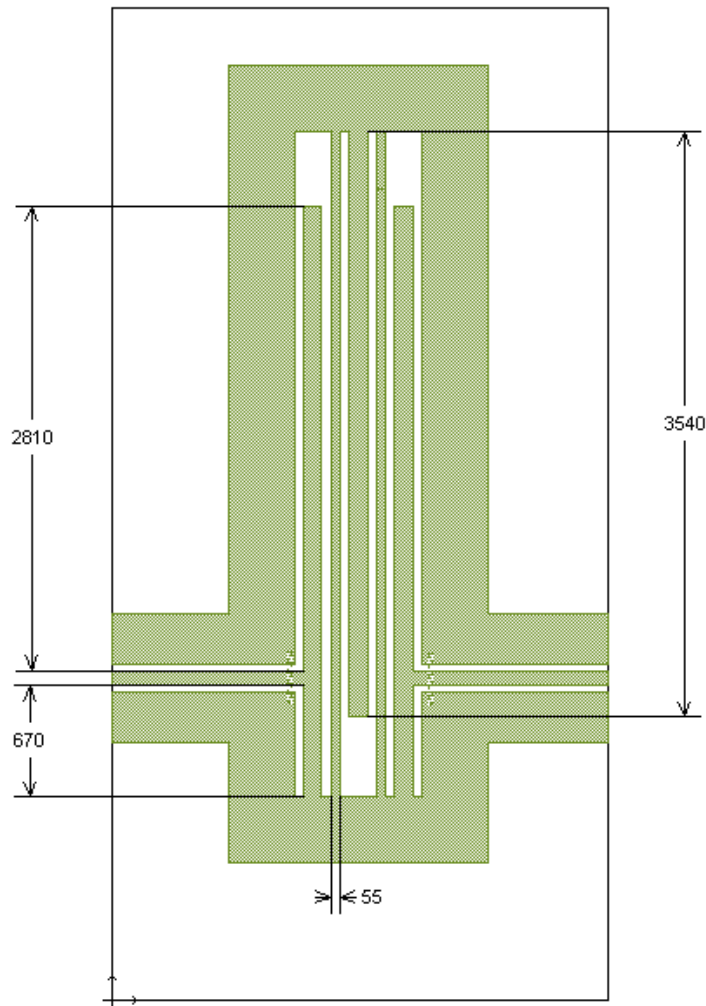
Fig. 5-25: Image of the 3-pole filter designed at 9 GHz with dimensions given in μm.

An interdigital CPW filter with a center frequency of 9 GHz and a bandwidth of 1 GHz is first designed. This filter is shown in Fig. 5-25. The input CPW transmission line has a center line width of 90 μm, a gap of 40 μm, and a ground line width of 300 μm. The EM simulation results of this filter are shown in Fig. 5-26.
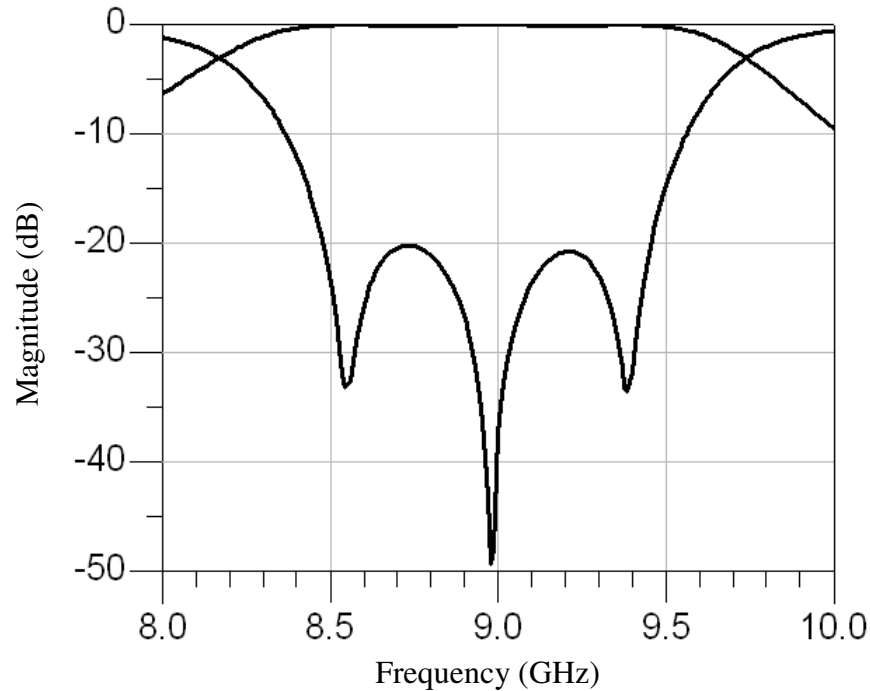
Fig. 5-26: EM simulation results of the 3-pole filter designed at 9 GHz.

The next step of the design process is to add switches to the above design to get a filter response with a center frequency of 10 GHz and a bandwidth of 1 GHz. The resonators at 10 GHz will be shorter than those at 9 GHz, so switches are added to shorten the resonator. A switch is added at each end of the resonator to control the coupling. The switched added to the open circuited end of the resonators are shown in Fig. 5-28. This switch is in the down position for the lower frequency band and is in the up position for the higher frequency band. The switches at the short circuited end of the resonators are shown in Fig. 5-29. These

switches reduce the length of the resonator when in the down position to achieve the state with the higher frequency. In the up position these switches contribute to the lower frequency state. The positions of all the switches need to be optimized to achieve the correct bandwidth at the higher state. The final layout of the filter is shown in Fig. 5-27. The EM simulation results of the two states of the filter are shown in Fig. 5-30. For the lower frequency state, the switches at the open end are in the down state and the switches at the short circuited end are in the up position.
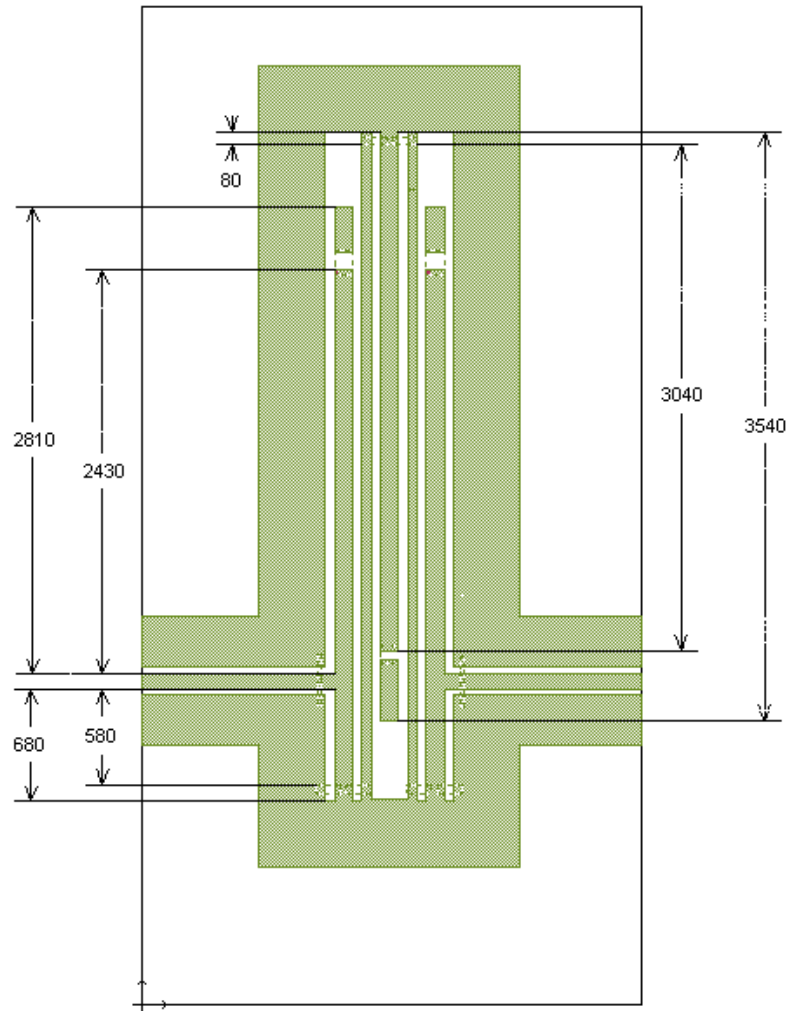
Fig. 5-27: Image of the two state 3-pole filter designed with dimensions given in μm.

The use of embedded switches to reduce the size of tunable filters with constant absolute bandwidth is demonstrated through a two state tunable filter. The CPW filter contains

MEMS switches, which allow the filter to be changed between its two states. The main advantage of this filter design is the reduction in size over the use of SPNT switches and N filters. Arbitrary bandwidths can also be achieved for the various channels of the filter. There are certain limitations to this design that involve the physical size of the switches and the filters themselves. This affects the number of channels, the choice of bandwidth, center frequency, and the difference in frequency between channels.
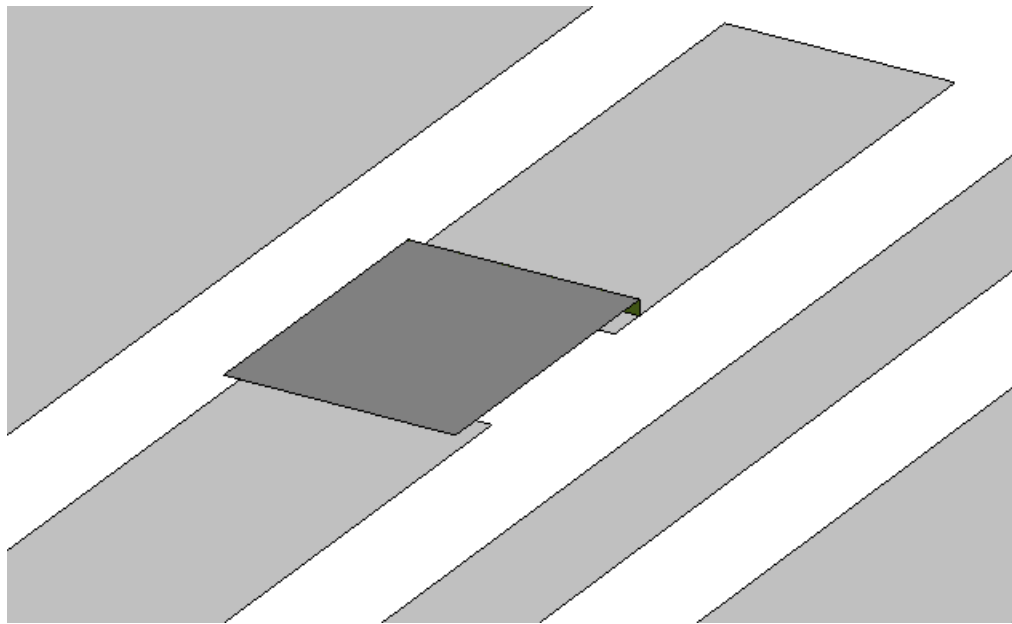
Fig. 5-28: Image of the MEMS switch at the open circuited end of a resonator with the top MEMS layer in dark gray.
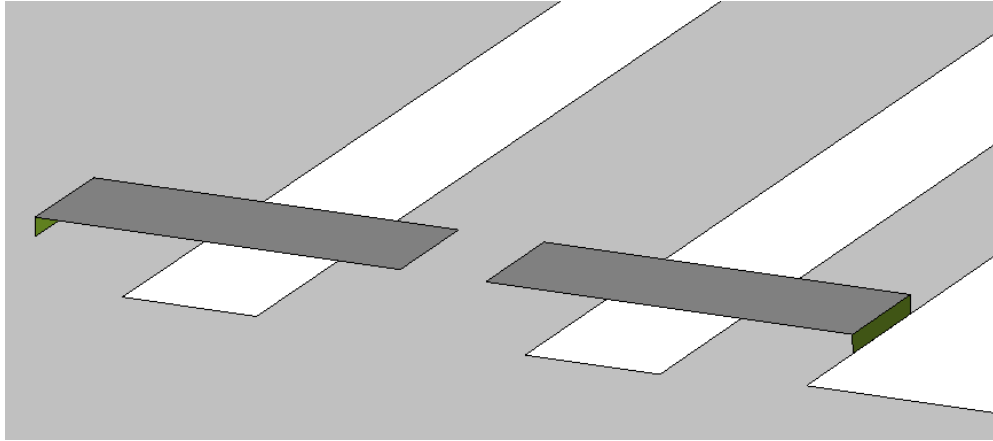
Fig. 5-29: Image of the MEMS switches at the short circuited end of a resonator with the top MEMS layer in dark gray.
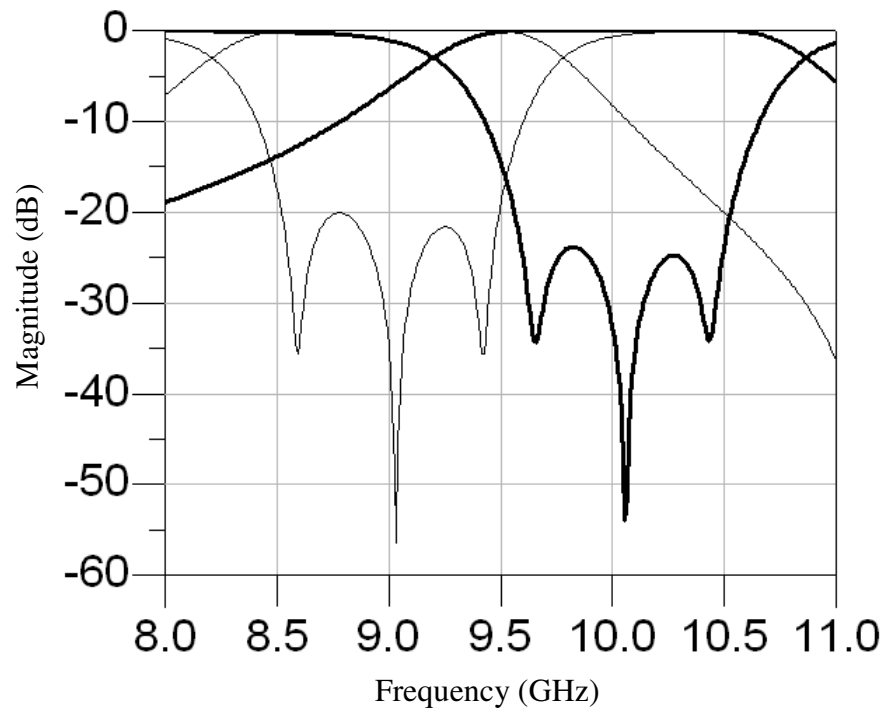
Fig. 5-30: EM simulations results of the two state filter in the lower frequency state (thin line) and the higher frequency state (bold line).

5.4 Hybrid Integration and Monolithic Integration of High Temperature Superconductors and Micro-Electro-Mechanical Systems

The hybrid integration of HTS filters and MEMS switches is first presented through the realization of a filter that can be implemented in a manifold coupled switched multiplexer design from section 5.2. The monolithic integration of HTS circuits and MEMS devices involves fabricating MEMS structures using surface micromachining techniques on a substrate coated with a thin HTS film. The low loss characteristics of the superconductor and the low loss and superior linearity performance of MEMS devices are combined to realize low loss tunable microwave circuits. The details of the fabrication process are first presented, and the deposition of the dielectric layer is demonstrated to not degrade the superconducting properties of the HTS material.

5.4.1 Hybrid Integration of HTS Filters and MEMS Switches

The integration of HTS filters and MEMS devices is first investigated through a hybrid integration approach. In this approach, commercially available RF MEMS switches are integrated, through wirebonds and silver epoxy, with a fabricated and assembled HTS microstrip filter. The benefit of this approach is that the switches are commercially available and a new fabrication process for creating MEMS devices is not needed. Though, the designs are limited to those that only make use of MEMS switches, and the wirebonds introduce parasitics that need to be considered.

A 4-pole HTS microstrip filter, similar to those presented in section 5.2 is designed and fabricated. The filter is fabricated with the patterning and etching processes outlined in 5.4.2, with the addition of the backside of the wafer being protected with kapton tape during the etching process to protect the gold and YBCO layers. The wafer is diced and assembled in a gold plated metal housing. The measured results of the assembled filter are shown in Fig. 5-31.

RF MEMS switches [70] and RF choke inductors are added to the filter, as shown in Fig. 5-32. The two MEMS switches are placed across the capacitive ends of the two middle resonators, as suggested in section 5.2.2 to allow the detuning of these two resonators. With

other filter designs and manifold design, this filter can be used in a manifold coupled switched multiplexer design such as that presented in section 5.2.2. The RF MEMS switches are connected with wirebonds to the HTS filter, where gold pads were left on the ends of the capacitive portion of the resonator to allow for a proper wire bond to occur.
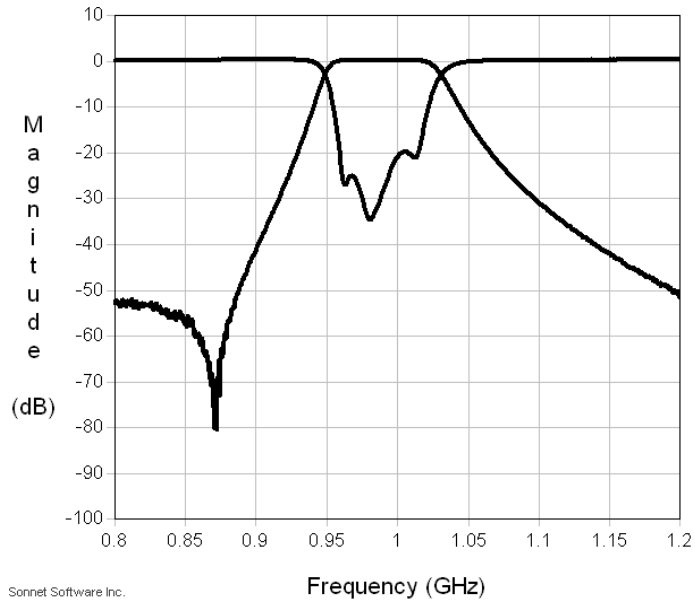
Fig. 5-31: Measured results of the assembled 4-pole filter.
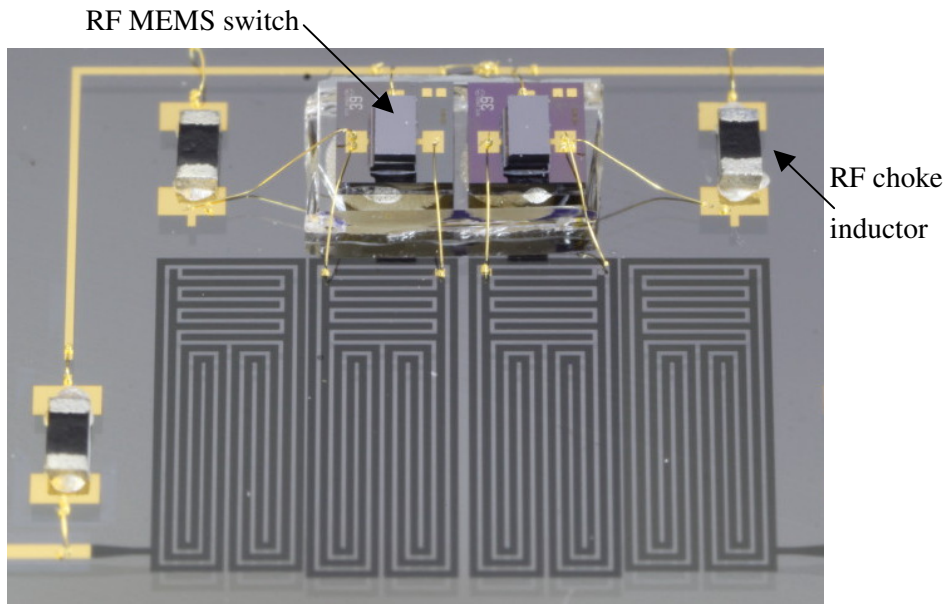
Fig. 5-32: Image of the assembled HTS filter integrated with MEMS switches.

115

The filter is cooled to 77K with a custom table top cryocooler. The voltage of 90V needed to actuate the MEMS switches is placed across the input 50 Ω input microstrip transmission line and the ground of the housing through a bias-T on the connected coaxial cable to avoid damaging the vector network analyzer. The measured results with the MEMS switches actuated with a voltage of 90V are shown in Fig. 5-33. An isolation of approximately 35 dB is seen across the two ports of the filter, which is the expected isolation from the analysis given in section 5.2.2.
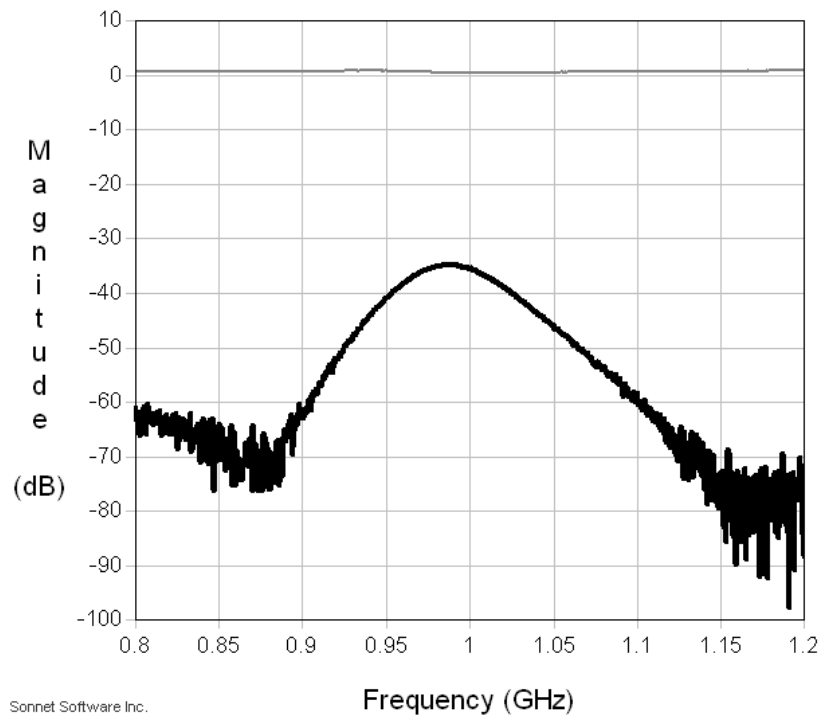
Fig. 5-33: Measured return loss (thin gray) and return loss (bold black) of the 4-pole filter with the MEMS switches in the closed state.

The wirebonds present a parasitic inductance from the resonator to the switch, and the MEMS switch presents a parasitic up state capacitance. The combination of these two parasitic elements can shift the resonant frequency of the two middle resonators down in frequency. The capacitive portions of the resonators can be tuned through laser trimming to increase their resonant frequencies. The MEMS switches also show a parasitic capacitance

to ground through the die of the MEMS switch and through the LaAlO₃ wafer. Further analysis needs to be performed to account for this parasitic capacitance.

5.4.2 Fabrication Process for the Monolithic Integration of HTS and MEMS

The fabrication process is designed to create tunable MEMS capacitors, MEMS contact switches and MEMS capacitive switches. The six mask fabrication process includes a bottom high temperature superconducting layer that allows for very low loss microwave circuits to be designed. A resistive layer is used as a DC bias for the actuation of the MEMS devices. A dielectric layer is used to cover the bottom electrode of the MEMS devices to prevent a dc short from occurring between the top metal layer and the bottom electrode. A top gold layer acts as the movable layer of the MEMS devices. Dimples are made in the sacrificial layer so contact switches can be fabricated. Detailed processes of all of the fabrication steps are listed in Appendix A.

One of the main challenges of creating this monolithic process is to deposit and etch two gold layers, a dielectric layer, and a resistive layer without degrading the thin film superconducting layer. Processes that involve higher temperatures and that include water [71]-[72] can degrade the superconducting film. The oxygen content of the superconducting film needs to remain unchanged through all of the processing steps so the film will act as a superconductor at a temperature of 77 K, or the temperature of liquid nitrogen. Process temperatures above 200 °C can result in the de-oxygenation of the thin film. Also, immersion of the wafer in water can quickly reduce the quality of the superconducting film [71]. All of the processing steps must have an operating temperature below 200 °C and must limit the amount of time the exposed high temperature superconducting film is immersed in water.

The process starts with a 2'' (50.8 mm) in diameter, 0.508 mm thick magnesium oxide (MgO) wafer coated with 0.5 µm of dysprosium barium copper oxide (DyBCO) and 0.2 µm of gold. The thin films are deposited on the MgO wafers by THEVA [73]. The thin gold layer on top of the DyBCO is very important as it acts as a transformer between the normal conductor and the superconductor. The gold layer is deposited in situ after the DyBCO is

117

deposited on the MgO wafer. This results in the best adhesion and electrical connection between the gold and the HTS layers. This first step of the fabrication step is shown in Fig. 5-34 a).

The next step of the fabrication process involves patterning the HTS mask and etching the gold and the HTS film. The HTS mask is the first mask and includes the microwave devices, such as the transmission lines and the filters. The positive photoresist, AZ3330, is spun on the wafer, exposure is performed with the Oriel mask aligner, and the photoresist is developed with AZ300 MIF developer. Gold etching and HTS etching is then performed. The wet gold etching is done with Transene Gold Etchant TFA. Since the HTS under the gold that is etched will also be removed, we are not as concerned with the exposure to water. The HTS wet etching is done with a 1% phosphoric acid solution. The photoresist is then stripped off with AZ Kwik Strip Remover. The wafer after these fabrication steps is shown in Fig. 5-34 b). The gold remains covering the HTS to protect it during the next few processing steps.

The next step of the fabrication process includes the deposition and etching of a titanium tungsten (TiW) layer and an amorphous silicon (a-Si) layer. The TiW layer is used as both an adhesion layer for the a-Si and as a resistive layer. The a-Si layer is used as a dielectric layer that covers the bottom electrode of the MEMS devices. A thin 0.04 µm layer of TiW is sputtered on the wafer using the Intlvac Nanochrome deposition system. After breaking the vacuum of the sputtering system, the wafer is immediately loaded into the plasma enhanced chemical vapour deposition (PECVD) system to ensure good adhesion of the a-Si layer to the TiW layer. A deposition process at a temperature of 150 °C [74] is used to deposit the 0.7 µm thick layer of a-Si. This deposition is performed with a Trion Orion PECVD system. Amorphous silicon was chosen as the dielectric layer due to its ease of deposition at a temperature below 200 °C. Silicon dioxide (SiO_2) and silicon nitride (SiN_x) can also be deposited using this PECVD system. It is possible to use one of these dielectrics as for this process by developing processes that function at a temperature below 200 °C.

The positive photoresist, AZ3330, is again spun on the wafer, the Resistive/Dielectric mask is used for the exposure, and the photoresist is developed. Both the a-Si layer and the TiW layer can be etched in a reactive ion etcher (RIE) with a sulfur hexafluoride (SF_6) as the processing gas. The etching is performed with a Trion Phantom RIE system. The photoresist is then stripped away with AZ Kwik Strip Remover. The wafer after these processing steps is shown in Fig. 5-34 c).

The next step in this fabrication process is the removal of the gold on the HTS film. The AZ3330 photoresist is spun onto the wafer, the Gold Pad mask is during the exposure step, and the photoresist is developed. The Transene Gold Etchant TFA is again used to remove the gold from the wafer. This etching step removes most of the gold covering the HTS and leaves gold pads for probing the wafer and for the anchors for the top gold layer. The time taken to rinse the wafer after etching the gold must be minimized to not degrade the HTS layer with the exposure to water. The photoresist is again removed with AZ Kwik Strip Remover. The wafer then appears as shown in Fig. 5-34 d).

The deposition of the sacrificial layer is the next processing step. The positive photoresist, AZ3330, is used as the sacrificial layer and is spun on at the speed to achieve a thickness of 2.5 μm. This step is illustrated in Fig. 5-34 e). Two exposures are performed with the Anchor mask and the Dimple mask. The Anchor mask exposure is performed for 12 seconds and the Dimple mask exposure is carried out for only 4 seconds. After developing, the openings in the sacrificial layer due to the Anchor mask exposure go through the full 2.5 μm of the photoresist. The openings due to the Dimple mask exposure are only 0.7 μm deep to allow for dimples in the top gold metal layer. After this developing step, the wafer appears as shown in Fig. 5-34 f).

The next step in the process is the deposition of the top gold layer. A seed layer of gold is deposited on the wafer to a thickness of 0.1 μm. The deposition is a sputtering process performed with the Intlvac Nanochrome deposition system. This gold layer is then increased to a thickness of 1.5 μm by a gold electroplating process. This electroplating

process is a non-cyanide process. The wafer appears as shown in Fig. 5-34 g) after this fabrication step.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

(i)
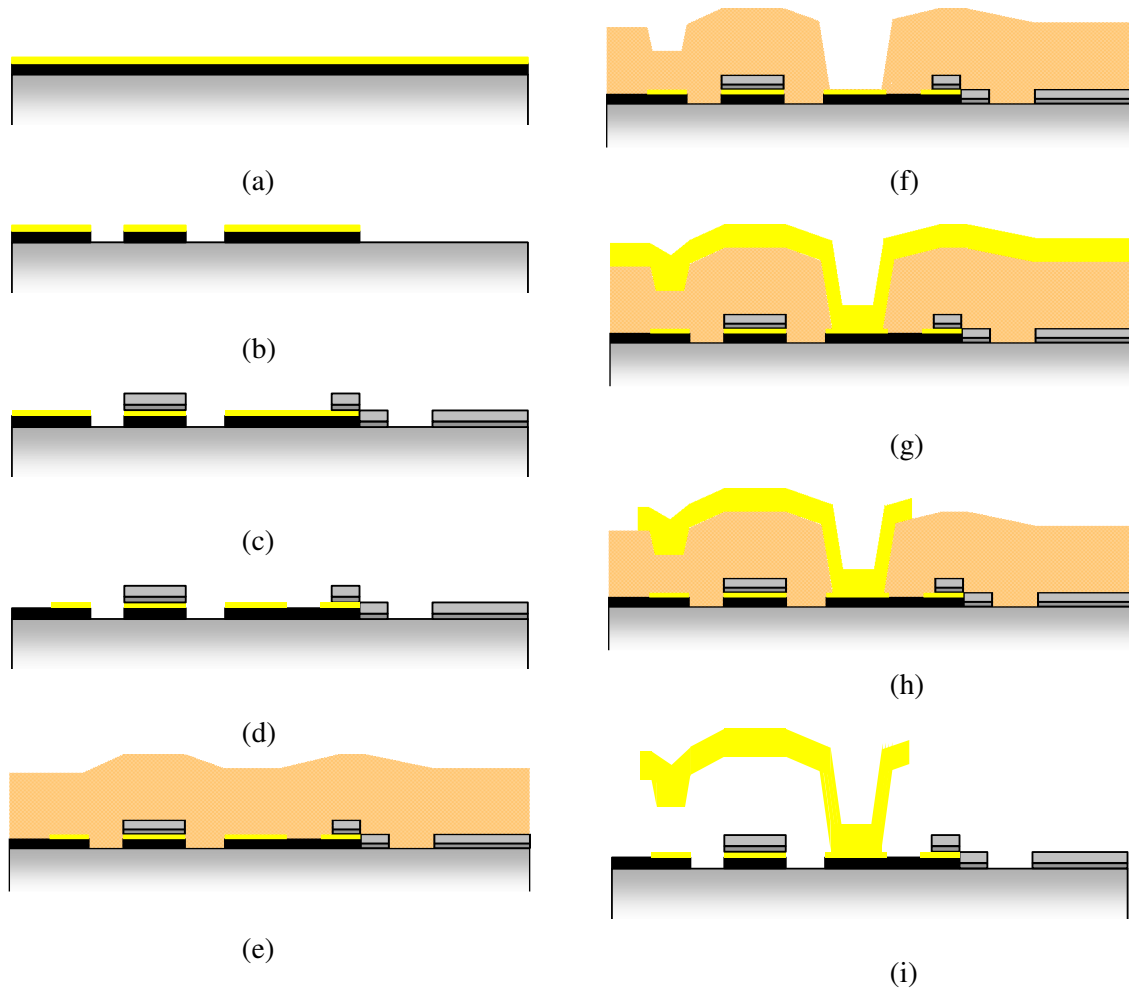
Fig. 5-34: The fabrication steps for the monolithic integration of HTS circuits and MEMS devices.

The patterning of the top gold layer mask and the etching of the top gold layer comprise the next step of the fabrication process. The positive photoresist AZ3330 is spun onto the wafer, the top gold layer mask is used for the exposure, and the photoresist is developed. It is important to note that a post exposure bake is not included in this step of the process. The sacrificial layer tends to bubble during a post exposure bake, which ruins the top gold layer

on the wafer. The top gold layer is etched using Transene Gold Etchant TFA. The wafer appears as shown in Fig. 5-34 h) after the gold etching process.

The final process steps involve the release of the MEMS structures. The removal of the sacrificial layer is a two-step process consisting of a dry etch step and a wet etch step. The top layer of the sacrificial photoresist layer is fist removed by a dry etch process using an oxygen plasma in the Trion Phantom RIE system. The wafer is then placed in a bath of AZ Kwik Strip Remover at a temperature of 65°C for 4 hours. The wafer is then left over night in the stripper. The wafer is then placed in a petri dish with isopropyl alcohol in preparation for the final step using the Tousimis Critical Point CO_2 Dryer. The wafer is then placed in the CO_2 dryer where the isopropyl alcohol is removed from the wafer. After this final process, the wafer appears as shown in Fig. 5-34 i).
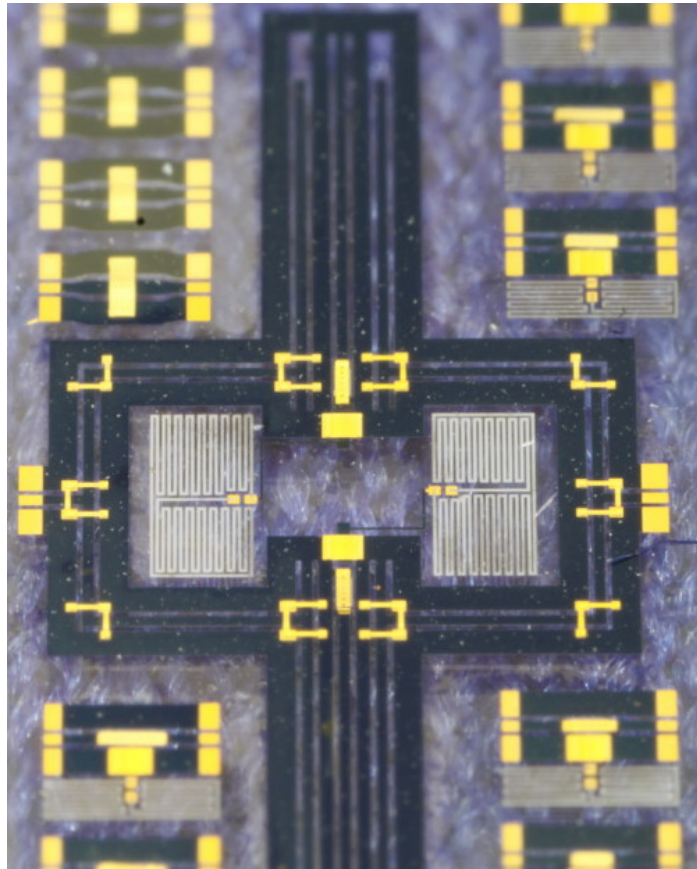
Fig. 5-35: Image of some devices from the monolithically integrated HTS and MEMS wafer.

In this last process step, the wafer was inadvertently placed in a hot water bath at a temperature of 60°C for 1 hour before being place in isopropyl alcohol for the release process. It is believed that this fabrication step changed the superconducting properties of the DyBCO layer. When testing devices on the wafer, as shown in Fig. 5-35, at cryogenic temperatures, the DyBCO showed a large DC resistance. A previous iteration of this fabrication process that included all of the steps shown in Fig. 5-34, except the deposition and etching of the TiW and a-Si layers, showed a CPW transmission line reaching a superconducting state when tested at a temperature of 77 K. The next section outlines the effect of the deposition of the a-Si on the thin film superconducting layer.

5.4.3 Effect of a-Si on an HTS Filter

The effect of depositing a thin layer of amorphous silicon on an HTS filter is investigated [75]. The main purpose of this study is to determine whether the deposition of the thin a-Si layer will significantly affect the superconducting properties of the HTS material from a microwave circuit viewpoint. A 4-pole HTS filter is fabricated, assembled, and tested. A thin film of a-Si is then deposited on the filter and re-tested to determine the effect on the superconductivity of the HTS material.

A 4-pole filter is first designed to have the bandwidth and center frequency of the Channel 1 filter from Table 5-1. The filter is designed using the reflected group delay method described in Chapter 3. The resonator design is also the same as those presented in section 3.4 and section 5.2. A 500 µm thick LaAlO$_3$ wafer with a thin film of YBCO on both sides is used for the filter design. An image of the filter layout is shown in Fig. 5-36.

The filter is fabricated and assembled in a metal housing with high frequency coaxial connectors. The filter is tested in a custom cryocooler at a temperature of 77 K, and the measured results are shown in Fig. 5-37 a). A thin layer of a-Si is then deposited with the PECVD on the assembled filter. The deposition steps are the same as those listed in section 5.4.2 and Appendix A. The deposition time is approximately 2200 seconds to achieve an a-Si thickness of 1 µm. The filter is then re-tested at a temperature of 77 K, and the measured

122

results are shown in Fig. 5-37 b). The loss seen in the out of band return loss and the in-band insertion loss measurements of Fig. 5-37 a) is due to errors in calibration.
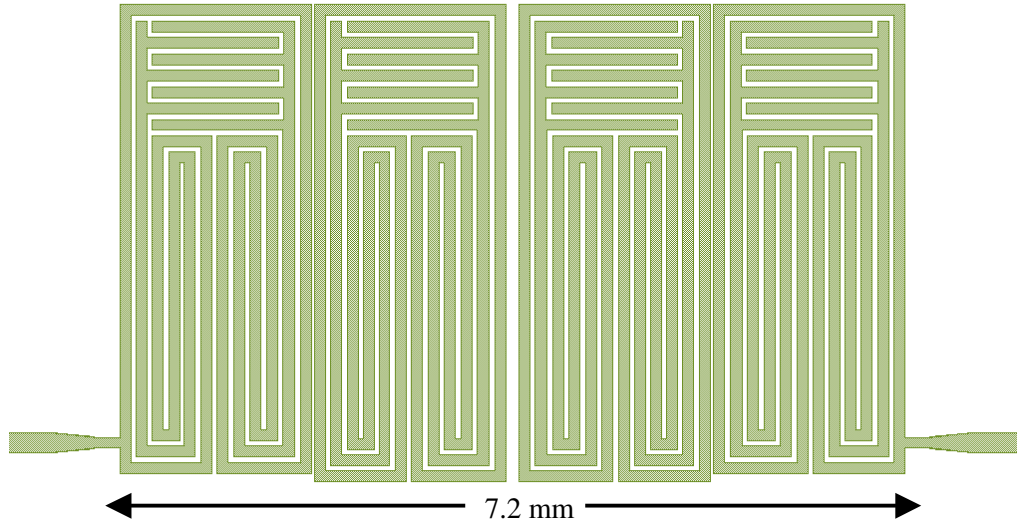
Fig. 5-36: An image of the 4-pole HTS filter used to determine the effect of the a-Si deposition.

The measured results of the filter with the thin a-Si layer shows a shift down in center frequency, as is expected due to the high dielectric constant of the silicon. The return loss of the filter has also become detuned due to the added dielectric layer. There is no significant degradation in the insertion loss of the filter due to the deposition of the a-Si layer. Since the deposition temperature is kept below 200 °C, the superconducting properties of the YBCO are not significantly affected from a microwave circuit viewpoint.
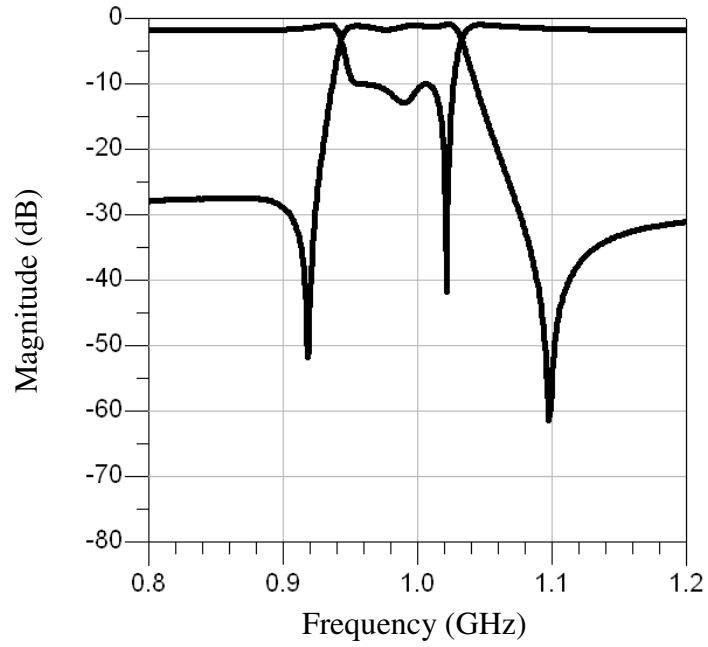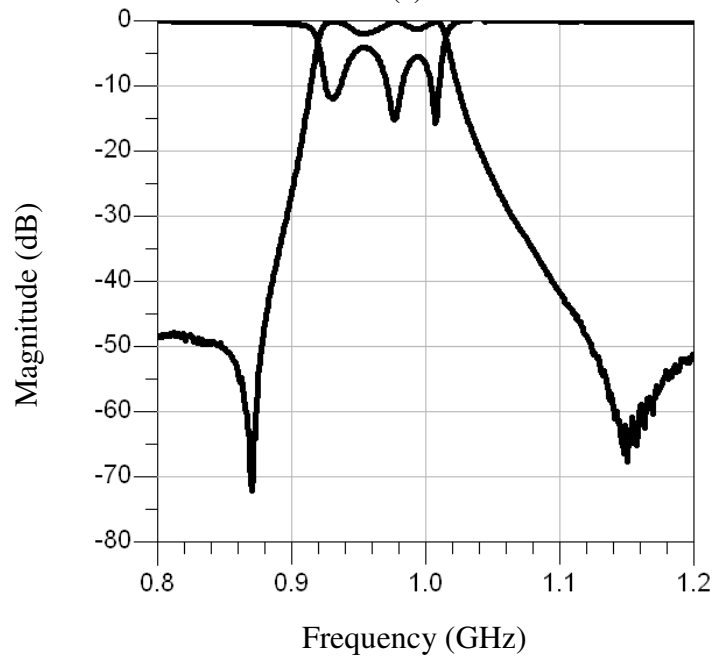
Fig. 5-37: The measured results of a) the 4-pole HTS filter before the a-Si deposition and b)
the 4-pole HTS filter with 1 μm of deposited a-Si.

Chapter 6
Conclusions

The contributions of the research presented in this thesis are summarized and some suggested areas of research are given to further develop upon the contributions.

6.1 Contributions

The major contributions presented in this thesis are as follows:

- The reflected group delay method is demonstrated by the design of higher order superconducting filters. The reflected group method is a well known method for tuning filters, and the method is further developed as a method for designing filters. A correction factor is introduced so the group delay at each stage of the design process needs to match a specific value at the center frequency of the filter and be symmetric about the center frequency. This correction factor is needed when designing filters with higher orders and wider bandwidths. The reflected group delay method is demonstrated by the design of an ideal lumped element filter. The method is then used to design an 8-pole HTS filter and an 8-pole LTS filter. The filter designs are ideal for use with the reflected group delay method as their resonators have limited cross couplings.

- The standard niobium process traditionally offered by HYPRES for superconducting digital electronics is used to design lumped element bandpass and bandstop filters. The niobium process allows for the fabrication of highly miniaturized superconducting lumped element microwave circuits. A three pole bandpass filter is first designed using a shunt LC resonator with series coupling capacitors between the resonators. Another filter structure is proposed for the fabrication process, which makes use of tap couplings between resonators and at the inputs. These filters are very miniaturized having a resonator size of $\sim\lambda_0/500$ at a frequency of 1 GHz. A bandstop filter design is also presented that uses

125

lumped element low pass filters as impedance inverters. A 3-pole bandstop filter with 5-pole low pass filters is designed using a series LC circuit from the signal line to the ground line of a CPW. The implementation of the lumped element low pass filter results in a huge savings in size over the use of a 90° length of transmission line.

- The three pole lumped element filters are implemented in a diplexer design using the standard niobium process offered by HYPRES. Two different lumped element quadrature hybrids are designed at 1 GHz and are incorporated with the lumped element filters to create diplexers. The required 50 Ω loads are realized with the resistive layer available from the fabrication process. These lumped element low temperature superconducting diplexers designs are again highly miniaturized.

- A tunable filter with 2^N possible states that makes use of manifolds and N filters is presented. The manifold-coupled switched multiplexer is an improvement over a switched filter bank in that is offers more possible states and reduced insertion loss due to the use of embedded switches. Both ports of N filters are connected to two identical manifolds creating a two port network. By detuning resonators within a filter with embedded switches, the filter is turned off. There exists a tradeoff in off state isolation and the separation in frequency between each filter due to the number of detuned resonators. This tunable filter configuration is presented with measured results of a diplexer design with three pole filters. The concept is further expanded to a triplexer design with high temperature superconducting 8-pole filters and manifolds. The fabricated multiplexers are measured and through the use of EM simulations, the manifold-coupled switched triplexer with 8 possible states is demonstrated.

- The hybrid integration of an HTS filter and commercially available RF MEMS switches is performed. The two middle resonators of a 4-pole HTS filters are successfully detuned with the MEMS switches for use in a manifold coupled

switched multiplexer application. A fabrication process is investigated to monolithically integrate MEMS devices and HTS circuits to create low loss tunable microwave filters. An MgO wafer with an HTS material and a thin layer of gold is the starting point of the fabrication process. The HTS and gold layer are first patterned and etched, but the gold is left covering the HTS patterns to protect them from the next few fabrication steps. An a-Si dielectric layer with a thin TiW adhesion layer is deposited, patterned and etched. The gold covering the HTS patterns are then patterned and etched to leave gold pads for anchors and areas for probing. A photoresist layer is used as a sacrificial layer for the MEMS devices, and the top gold layer is deposited, patterned and etched. The final partial dry and partial wet release process is then performed. All of the fabrication steps are meant to avoid prolonged immersion in water and to use temperatures below 200 °C so as to not affect the superconducting properties of the HTS material.

6.2 Future Work

The following are suggestions to expand upon the research presented in this thesis:

- The fabrication process to monolithically integrate MEMS devices and HTS materials can be further developed to realize low loss tunable microwave circuits. The process presented in this thesis can be used to develop tunable MEMS capacitors and switches. The effect on the superconducting properties of the HTS due to the fabrication process can be more accurately characterized. The mechanical properties of the deposited top gold metal layer can also be further characterized and improvements can be made to the fabrication process while keeping the process temperatures below 200 °C. An alternative approach is to use temperatures above 200 °C and then to develop a process to restore the optimum oxygen content of the HTS material.

- The standard niobium fabrication process can be used to create other highly miniaturized superconducting microwave circuits. Highpass, lowpass, bandpass and bandstop filters and other microwave passive devices, such as couplers and power dividers, can all be designed and fabricated with this process. The electrical properties of the fabrication process at microwave frequencies should be further characterized to achieve better measured results based on the EM simulations. This is especially important when designing narrow band filters.

- Adding tunability is the next step in the development of the LTS microwave devices. The tunability can be achieved in several ways, such as using the superconducting properties of niobium or by creating MEMS structures with niobium as the metal layers. MEMS structures made of niobium can result in very low loss tunable microwave devices. The MEMS devices can be made using the metal layers from the standard niobium process offered by HYPRES. As an alternative, the MEMS devices can be realized with a custom fabrication process either using a raw wafer or a wafer from the HYPRES standard niobium fabrication process as the base for building the MEMS devices. Tunable capacitors and switches can be designed to realize these superconducting microwave devices and circuits.

Appendix A

Fabrication Process for the Monolithic Integration of High Temperature Superconductors and MEMS Devices

The following are the detailed steps of the fabrication process for the monolithic integration of HTS circuits and MEMS devices.

Before starting any processing, the wafer with the HTS thin film and the gold thin film are cleaned using the following clean recipe:

- Clean the wafer of any debris using the nitrogen gun
- Put the wafer in a petri dish with acetone for 5 minutes
- Put the wafer in a petri dish with isopropyl alcohol (IPA) for 5 minutes
- Dry the wafer using the nitrogen gun

The following are the steps for patterning the HTS mask:

- Spin on AZ3330 positive photoresist with the following parameters:
  - Speed: 3000 rpm; Time: 30 seconds; Acceleration: 30
- Perform a soft bake on a hot plate for 60 seconds at a temperature of 90°C
- Perform the exposure using the Oriel Mask Aligner for 12 seconds using the HTS mask
- Perform a post exposure bake on a hot plate for 60 seconds at a temperature of 110°C
- Develop the wafer in AZ300 MIF developer for 75 seconds (the number of times the developer has been used will affect the developing time)
- Rinse the wafer with de-ionized (DI) water and dry the wafer

The following are the steps for etching the gold layer and the DyBCO layer:

- Etch the gold layer for 20 seconds in Transene Gold Etchant TFA.

- Rinse the wafer with DI water

- Etch the DyBCO in a 1% phosphoric acid solution for 3 minutes and 20 seconds using brisk agitation

- Rinse the wafer with DI water

- Remove the photoresist with AZ Kwik Strip remover for 60 minutes at a temperature of 70°C

- Rinse the wafer with DI water

The following are the steps for performing the deposition of the TiW layer:

- Sputtering of the 0.04 μm thick layer of TiW is performed with the Intlvac Nanochrome deposition system using the following parameters:

  o Deposition rate: 0.0023 μm/minute; Deposition time: 17 minutes.

The following are the steps for performing the deposition of the 0.7 μm amorphous silicon layer:

- Clean the Trion Orion PECVD system using the clean recipe

- Flush the lines of nitrogen and replace with argon

- Load the wafer immediately after finishing the TiW deposition into the PECVD system.

- Deposit the a-Si layer at a temperature of 150°C using the following procedures and parameters:

  o Time: 180 seconds; Pressure: 0 mTorr, Argon flow: 0 sccm; SiH_4 flow: 0 sccm; RF Power: 0 W

  o Time: 180 seconds; Pressure: 250 mTorr; Argon flow: 30 sccm; SiH_4 flow: 0 sccm; RF Power: 0 W

  o Time: 180 seconds; Pressure: 0 mTorr, Argon flow: 0 sccm; SiH_4 flow: 0 sccm; RF Power: 0 W

- Time: 1555 seconds; Pressure: 750 mTorr; Argon flow: 5 sccm; SiH_4 flow: 10 sccm; RF Power: 37 W

- Time: 180 seconds; Pressure: 0 mTorr, Argon flow: 0 sccm; SiH_4 flow: 0 sccm; RF Power: 0 W

- Time: 180 seconds; Pressure: 250 mTorr; Argon flow: 30 sccm; SiH_4 flow: 0 sccm; RF Power: 0 W

- Time: 180 seconds; Pressure: 0 mTorr, Argon flow: 0 sccm; SiH_4 flow: 0 sccm; RF Power: 0 W

- Unload the wafer from the PECVD system

The following are the steps for patterning the Resistive/Dielectric mask:
- Spin on AZ3330 positive photoresist with the following parameters:
  - Speed: 3000 rpm; Time: 30 seconds; Acceleration: 30
- Perform a soft bake on a hot plate for 60 seconds at a temperature of 90°C
- Perform the exposure using the Oriel Mask Aligner for 12 seconds using the Resistive/Dielectric mask
- Perform a post exposure bake on a hot plate for 60 seconds at a temperature of 110°C
- Develop the wafer in AZ300 MIF developer for 75 seconds (the number of times the developer has been used will affect the developing time)
- Rinse the wafer with DI water and dry the wafer

The following are the steps for etching the a-Si and TiW layers with the Trion Phantom RIE system:
- Etch both the a-Si and TiW layers in one single process with the following parameters:
  - Time: 180 seconds; Pressure: 0 mTorr; RF power: 0 W; SF_6 flow: 0 sccm
  - Time: 140 seconds; Pressure: 50 mTorr; RF power: 50 W; SF_6 flow: 30 sccm

- Time: 180 seconds; Pressure: 0 mTorr; RF power: 0 W; SF_6 flow: 0 sccm
- Remove the photoresist with AZ Kwik Strip remover for 60 minutes at a temperature of 70°C
- Rinse the wafer with DI water

The following are the steps for patterning of the Gold Pad mask:
- Spin on AZ3330 positive photoresist with the following parameters:
  - Speed: 3000 rpm; Time: 30 seconds; Acceleration: 30
- Perform a soft bake on a hot plate for 60 seconds at a temperature of 90°C
- Perform the exposure using the Oriel Mask Aligner for 12 seconds using the Gold Pad mask
- Perform a post exposure bake on a hot plate for 60 seconds at a temperature of 110°C
- Develop the wafer in AZ300 MIF developer for 75 seconds (the number of times the developer has been used will affect the developing time)
- Rinse the wafer with DI water and dry the wafer

The following are the steps for the etching of the gold layer:
- Etch the gold layer for 12 seconds in Transene Gold Etchant TFA.
- Rinse the wafer with DI water and dry the wafer

The following are the steps for depositing the sacrificial layer and patterning the Anchor and Dimple masks:
- Spin on AZ3330 positive photoresist with the following parameters to deposit a 2.5 μm thick sacrificial layer:
  - Speed: 2400 rpm; Time: 30 seconds; Acceleration: 15
- Perform a soft bake on a hot plate for 3 minutes at a temperature of 90°C

- Perform the exposure using the Oriel Mask Aligner for 12 seconds using the Gold Pad mask

- Perform an exposure using the Oriel Mask Aligner for 12 seconds using the Anchor mask

- Perform an exposure for 4 seconds using the Dimple mask

- Perform a post exposure bake on a hot plate for 60 seconds at a temperature of 110°C

- Develop the wafer in AZ300 MIF developer for 75 seconds (the number of times the developer has been used will affect the developing time)

- Rinse the wafer with DI water and dry the wafer

- Perform a hard bake on a hot plate for 4 minutes at a temperature of 120°C

The following are the steps for the sputtering of the gold seed layer:

- Sputter a gold seed layer to a thickness of 0.1 µm with the Intlvac Nanochrome deposition system using the following parameters:

  o Deposition rate: 0.03 µm/minute; Deposition time: 200 seconds.

The following are the steps for electroplating the gold layer to a thickness of 1.5 µm:

- Plate an additional 1.4 µm of gold using the Technic electroplating system with a non-cyanide gold solution with the following parameters:

  o Amps per square foot (ASF): 2; approximate area: 0.022 ft²; Current: 44 mA; Time of electroplating: 0.47 A·min or 10 minutes and 27 seconds.

The following are the steps for the patterning of the Top Gold mask:

- Spin on AZ3330 positive photoresist with the following parameters:

  o Speed: 3000 rpm; Time: 30 seconds; Acceleration: 30

- Perform a soft bake on a hot plate for 60 seconds at a temperature of 90°C

- Perform the exposure using the Oriel Mask Aligner for 12 seconds using the Top Gold layer mask
- Do not perform a post exposure bake as the sacrificial layer will bubble and ruin the top gold layer
- Develop the wafer in AZ300 MIF developer for 45 seconds (the number of times the developer has been used will affect the developing time)
- Rinse the wafer with DI water and dry the wafer

The following are the steps for etching the top gold layer:
- Etch the gold layer for 2 minutes and 5 seconds in Transene Gold Etchant TFA.
- Rinse the wafer with DI water

The following are the steps for removing the top layer of the photoresist sacrificial layer with the Trion Phantom RIE system:
- Remove the top layer of the photoresist with an oxygen plasma with the following parameters:
  - Time: 180 seconds; Pressure: 0 mTorr; RF power: 0 W; ICP Power: 0W; O_2 flow: 0 sccm
  - Time: 180 seconds; Pressure: 600 mTorr; RF power: 50 W; ICP Power: 150 W; O_2 flow: 50 sccm
  - Time: 180 seconds; Pressure: 0 mTorr; RF power: 0 W; ICP Power: 0W; O_2 flow: 0 sccm
  - Repeat the above steps three times
- Remove more photoresist with an oxygen plasma with the following parameters:
  - Time: 180 seconds; Pressure: 0 mTorr; RF power: 0 W; ICP Power: 0W; O_2 flow: 0 sccm
  - Time: **TIME** (see below); Pressure: 50 mTorr; RF power: 0 W; ICP Power: 100 W; O_2 flow: 30 sccm

- Time: 180 seconds; Pressure: 0 mTorr; RF power: 0 W; ICP Power: 0W; O_2 flow: 0 sccm

- Perform the above steps six times with **TIME** = 300 seconds, 600 seconds, 300 seconds, 400 seconds, 800 seconds, 1000 seconds

The following are the steps for the release process after the above dry release process:

- Place the wafer in a petri dish with AZ Kwik Strip remover for 4 hours at a temperature of 65°C

- Leave the wafer in the petri dish over night

- **Place the wafer in a petri dish with water at a temperature of 60°C for 1 hour (Note: this step was inadvertently performed for this iteration of the fabrication process and should not be repeated in future iterations)**

- Put the wafer in a petri dish with IPA for 8 minutes

- Put the wafer in a petri dish with fresh IPA for 8 minutes

- Put the wafer in a petri dish with fresh IPA for 8 minutes

- Perform a release with the Tousimis Critical Point CO_2 Dryer with the following parameters:

  - Purge time: 10 minutes; Number of inserts: 2; Volume of IPA in the chamber: 75 mL

Bibliography

[1]   A.R. Brown and G.M. Rebeiz, "A Varactor-Tuned RF Filter," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-48, No. 7, pp. 1157-1160, 2000

[2]   I.C. Hunter and J.D. Rhodes, "Electronically Tunable Microwave Bandpass Filters", *IEEE Trans. Microwave Theory Tech.*, Vol. 30, No. 9, pp. 1354-1360, 1982

[3]   I. Lockerbie and S. Kumar, "A Broadband Tunable Combline Filter using Active Devices", *Proceedings IEEE WESCANEX 93*, pp. 196-200, 1993

[4]   S.R. Chandler *et al.*, "Active Varactor Tunable Bandpass Filter", *IEEE Microwave Guided Wave Lett.*, Vol. 3, No. 3, pp.70-71, 1993

[5]   G. Torregrosa-Penalva *et al.*, "A simple Method to Design Wide-Band Electronically Tunable Combline Filters", *IEEE Trans. Microwave Theory Tech.*, Vol. 50, No. 1, pp. 172-177, 2002

[6]   Xiao-Peng Liang and Yongfei Zhu, "Hybrid Resonator Microstrip Line Electrically Tunable Filter", *2001 IEEE MTT-S Microwave Symposium Digest*, pp. 1457-1460, 2001

[7]   S. Toyoda, "Variable Bandpass Filters using Varactor Diodes", *IEEE Trans. Microwave Theory Tech.*, Vol. 29, No. 4, pp. 356-363, 1981

[8]   H. Joshi *et al.* "High-Q Fully Reconfigurable Tunable Bandpass Filters", *IEEE Trans. Microwave Theory Tech.*, Vol. 57, No. 12, pp. 3525-3533, 2009

[9]   S. Pipilos *et al.*, "1.8 GHz Tunable Filter in Si Technology", *IEEE 1996 Custom Integrated Circuits Conference*, pp. 189-192, 1996

[10]   C. Rauscher, "Microwave Active Filters Based on Transversal and Recursive Principles", *IEEE Trans. Microwave Theory Tech.*, Vol. 33, No. 12, pp. 1350-1360, 1985

[11]   L. Billonnet *et al.*, "Theoretical and experimental analysis of microwave tunable recursive active filters using power dividers", *1993 IEEE MTT-S International Microwave Symposium Digest*, Vol. 1, pp. 185-188, 1993

[12] M. Delmond *et al.*, "Microwave Tunable Active Filter Design in MMIC Technology Using Recursive Concepts", *IEEE 1995 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp. 105-108, 1995

[13] R. Malmqvist *et al.*, "Analysis of tunable narrow-band recursive active MMIC filters for future adaptive on-chip radar receivers", *2000 Asia-Pacific Microwave Conference*, pp. 1073-1076, 2000

[14] T.-Y. Yun and K. Chang, "Piezoelectric-Transducer-Controlled Tunable Microwave Circuits", *IEEE Trans. Microwave Theory Tech.*, Vol. 50, No. 5, pp. 1303-1310, 2002

[15] F. Huang and R.R. Mansour, "Tunable Compact Dielectric Resonator Filters", *European Microwave Conference*, pp. 559-562, 2009

[16] H. Joshi *et al.* "High Q Narrow-Band Tunable Filters with Controllable Bandwidth", *2009 IEEE MTT-S International Microwave Symposium Digest*, pp. 629-632, 2009

[17] E. Brown, "RF-MEMS Switches for Reconfigurable Integrated Circuits", *IEEE Trans. Microwave Theory Tech.*, Vol. 46, No. 11, pp.1868-1880, 1998

[18] J. Yao, "RF MEMS from a device perspective", *J. Micromech. Microeng.*, Vol. 10, pp. R9-R38, 2000

[19] D. Peroulis *et al.*, "Tunable Lumped Components with Applications to Reconfigurable MEMS Filters", *2001 IEEE MTT-S International Microwave Symposium Digest*, Vol. 1, pp. 341-344, 2001

[20] E. Fourn *et al.*, "MEMS Switchable Interdigital Coplanar Filter", *IEEE Trans. Microwave Theory Tech.*, Vol. 51, No. 1, pp. 320-324, 2003

[21] J.-H. Park *et al.*, "Tunable millimeter-wave filters using a coplanar waveguide and micromachined variable capacitor", *J. Micromech. Microeng.*, Vol. 11, pp. 706-712, 2001

[22] A. Abbaspour-Tamijani *et al.*, "Miniature and Tunable Filters Using MEMS Capacitors", *IEEE Trans. Microwave Theory Tech.*, Vol. 51, No. 7, pp. 1878-1885, 2003

[23] P. Blondy *et al.*, "Applications of RF MEMS to Tunable Filters and Matching Networks", *CAS 2001 Proceedings International Semiconductor Conference*, Vol. 1, pp. 111-116, 2001

[24] S. Berkowitz, "Frequency Agile HTS Filters", 2004 *IEEE MTT-S International Microwave Symposium Workshop*, 2004

[25] A. Tombak *et al.*, "Tunable RF Filters using Thin Film Barium Strontium Titanate Based Capacitors", *2001 IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, pp. 1453-1456, 2001

[26] A. Tombak *et al.*, "Voltage-Controlled RF Filters Employing Thin-Film Barium–Strontium–Titanate Tunable Capacitors," *IEEE Trans. Microwave Theory Tech.*, Vol. 51, No. 2, pp. 462-467, 2003

[27] B. H. Moeckly and Yongming Zhang, "Strontium Titanate Thin Films for Tunable $YBa_2Cu_3O_7$ Microwave Filters", *IEEE Trans. Appl. Supercond.*, Vol. 11, No. 1, pp. 450-453, 2001

[28] G. Subramanyam *et al.*, "A K-Band-Frequency Agile Microstrip Bandpass Filter Using a Thin-Film HTS/Ferroelectric/Dielectric Multilayer Configuration", *IEEE Trans. Microwave Theory Tech.*, Vol. 48, No. 4, pp. 525-530, 2000

[29] A. Kozyrev *et al.*, "Ferroelectric Films: Nonlinear Properties and Applications in Microwave Devices", *1998 IEEE MTT-S Microwave Symposium Digest*, pp. 985-988, 1998

[30] P.S. Carter, "Magnetically-Tunable Microwave Filters Using Single-Crystal Yttrium-Iron-Garnet Resonators", *IRE Trans. Microwave Theory Tech.*, Vol. 9, No. 3, pp. 252-260, 1961

[31] L. Young and D.B. Weller, "A 500-1000 MHz Magnetically Tunable Bandpass Filter Using Two Disk Resonators", *IEEE Trans. Microwave Theory Tech.*, Vol. 15, No. 2, pp. 72-86, 1967

[32] C.K. Greene, "A Microstrip Nonreciprocal Tunable YIG Filter", *IEEE Journal of Solid-State Circuits*, Vol. 3, No.2, pp. 146-148, 1968

[33] H. Tanbakuchi *et al.*, "Magnetically Tunable Oscillators and Filters", *IEEE Transactions on Magnetics*, Vol. 25, No. 5, pp. 3248-3253, 1989

[34] D.E. Oates *et al.*, "Tunable YBCO Resonators on YIG Substrates", *IEEE Transactions on Applied Superconductivity*, Vol. 7, No. 2, pp. 2338-2342, 1997

[35] M. Tsutsumi and K. Okubo, "On the YIG Film Filters", *1992 IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, pp. 1397-1400, 1992

[36] J. Uher and W.J.R. Hoefer, "Tunable Microwave and Millimeter-Wave Band-Pass Filters", *IEEE Trans. Microwave Theory Tech.*, Vol. 39, No. 4, pp. 643-663, 1991

[37] B.-W. Kim and S.-W. Yun, "Varactor-Tuned Combline Bandpass Filter Using Step-Impedance Microstrip Lines", *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 1279-1283, 2004

[38] G.L. Matthaei, "Narrow-Band, Fixed-Tuned, and Tunable Bandpass Filters with Zig-Zag Hairpin-Comb Resonators", *IEEE Trans. Microwave Theory Tech.*, vol. 51, pp. 1214-1219, 2003

[39] M. Koochakzadeh and A. Abbaspour-Tamijani, "Design of Band-Select Filters with Arbitrary Characteristics Using Overlapped Loaded Line Topologies", *2009 IEEE MTT-S International Microwave Symposium Digest*, pp. 501-504, 2009

[40] Y.S. Hijazi *et al.*, "Design of a Superconducting MEM Shunt Switch for RF Applications", *IEEE Trans. Appl. Supercond.*, vol. 13, pp. 696-699, 2003

[41] Y.S. Hijazi *et al.*, "Fabrication of a Superconducting MEM Shunt Switch for RF Applications", *IEEE Trans. Appl. Supercond.*, vol. 13, pp. 700-703, 2003

[42] H. Zhang *et al.*, "Mechanical and Electrical Design of a Novel RF MEMS Switch for Cryogenic Applications", *2002 Proceedings of SPIE*, vol. 4931, pp. 372-376, 2002

[43] C. Brown *et al.*, "Cryogenic Performance of RF MEMS Switch Contacts", *J. Microelectromech. Syst.*, vol. 17, pp. 1460-1467, 2008

[44] G. Rebeiz, *RF MEMS: Theory, Design and Technology*, Hoboken: John Wiley & Sons, 2003

[45] S. Gong *et al.*, "Study of Broadband Cryogenic DC-Contact RF MEMS Switches", *IEEE Microwave Theory and Tech.*, vol. 57, pp. 3442-3449, 2009

[46] M. Schicke *et al.*, "Niobium SupraMEMS for Reconfigurable Millimeter Wave Filters", *IEEE Trans. Appl. Supercond.*, vol. 17, pp. 910-913, 2007

[47] J. W. Bandler et al, "Space Mapping Technique for Electromagnetic Optimization", *IEEE Microwave Theory and Tech.*, vol. 42, pp. 2536-2543, 1994

[48] S. Ye and R.R. Mansour, "An Innovative CAD Technique for Microstrip Filter Design", *IEEE Microwave Theory and Tech.*, vol. 45, pp. 780-786, 1997

[49] J.B. Ness, "A Unified Approach to the Design, Measurement, and Tuning of Coupled-Resonator Filters," *IEEE Microwave Theory and Tech.*, vol. 46, pp. 343-351, 1998

[50] P.D. Laforge, R.R. Mansour, and M. Yu, "Diplexer Design Implementing Highly Miniaturized Multilayer Superconducting Hybrids and Filters", *IEEE Trans. Appl. Supercond.*, vol. 19, pp. 47-54, 2009.

[51] J. Zhou et al., "Superconducting Microstrip Filters Using Compact Resonators with Double- Spiral Inductors and Interdigital Capacitors", *IEEE MTT-S Symposium Digest*, pp. 1889-1892, 2003

[52] J. Rosa *et al.*, "SATCOM-on the-Move (SOTM) using Superconductor Microelectronics – a quantum leap in performance", *2004 IEEE/Sarnoff Symposium on Advances in Wired and Wireless Communication*, pp. 95-98, 2004

[53] O.A. Mukhanov *et al.*, "Superconductor Analog-to-Digital Converters", *Proc. IEEE*, Vol. 92, pp. 1564-1584, 2004

[54] A. Kirichenko *et al.*, "Superconductor Digital Receiver Components", *IEEE Trans. Appl. Superconductivity*, Vol. 15, pp. 249-254, 2005

[55] I.V. Vernik *et al.*, "Integrated Millimeter/Submillimeter Superconducting Digital Spectrometer", *IEEE Trans. Appl. Superconductivity*, Vol. 15, pp. 419-422, 2005

[56] D.K. Brock and M.S. Pambianchi, "A 50 GHz Monolithic RSFQ Digital Phase Locked Loop", *2001 IEEE MTT-S Microwave Symposium Digest*, vol. 1, pp. 353-356, 2000

[57] Hypres Inc. (2010, July) Hypres Niobium Integrated Circuit Fabrication Process—Design Rules, New York. [Online]. http://www.hypres.com/pages/download/designrules/DesignRules.pdf

[58] R.J. Cameron, C.M. Kudsia, and R.R. Mansour, *Microwave Filters for Communication Systems*, Hoboken: John Wiley & Sons, 2007

[59] K. Wada and I. Awai, "A λ/2 CPW Resonator BPF with Multiple Attenuation Poles and Its Miniaturization", *1999 IEEE MTT-S Symposium Digest*, pp. 1139-1142, 1999

[60] J. Yamasaki *et al.*, "Design of Broadband Semi-Lumped and Lumped Element Quadrature Hybrids", *2005 IEEE MTT-S Microwave Symposium Digest*, pp. 1247-1250, 2005

[61] I. Ohta *et al.*, "A Design of Lumped Element 3 dB Quadrature Hybrids", *IEEE Proc. Asia-Pacific Microwave Conference*, pp. 1141-1144, 1997

[62] P.D. Laforge, R.R. Mansour and M. Yu., "Highly Miniaturized Multilayer Superconducting Filter", *2006 IEEE MTT-S Microwave Symposium Digest*, pp. 685-688, 2006

[63] P. Onno and A. Plitkins, "Miniature Multi-Kilowatt PIN Diode Mic Digital Phase Shifters", *IEEE GMTT International Microwave Symposium Digest*, pp. 22-23, 1971

[64] Sonnet Software Inc. (2010, July) Sonnet Suites 12 User's Guide, North Syracuse. [Online]. http://www.sonnetsoftware.com/support/downloads/manuals_v12/ guide.pdf

[65] J. S. Martens *et al.*, "HTS-Based Switched Filter Banks and Delay Lines" *IEEE Trans. Appl.* Supercond., vol. 3, pp. 2824-2827, 1993.

[66] I. C. Reines *et al.*, "A Low Loss RF MEMS Ku-Band Integrated Switched Filter Bank," *IEEE Microwave and Wireless Components Letters,* vol. 15, pp. 74-76, 2005.

[67] S. F. Peik *et al.*, "Switched Superconducting Filter Banks," *IEEE MTT-S Symp. Dig.,* vol. 3, pp. 1311-1314, 2004.

[68] C. I. Mobbs, "The Use of Four-Port Filter to Realize Switched Multiplexers Having Low Amplitude and Group Delay Ripple," *IEEE Microwave Theory and Tech.,* vol. 35, pp. 1183-1191, 1987.

[69] A. Morini *et al.*, "Re-configurable Reciprocal Multiplexers (r-mux) for Terrestrial Radio Links", *European Microwave Conference*, pp. 1-4, 2002

[70] RADANT MEMS (July, 2010) RMSW101-SPST RF MEMS Switch DC to 12 GHz [Online]. http://www.radantmems.com/radantmems.data/Library/Radant-Datasheet101_1.1.pdf

[71] R.L. Barnes and R.A. Laudise, "Stability of superconducting $YBa_2Cu_3O_7$ in the presence of water", *Appl. Phys. Lett*. vol. 51, pp. 1373-1375, 1987

[72] M. M. Garland , "Degradation of Y-Ba-Cu-O in a high-humidity environment", *J. Mater. Res.*, vol. 5, pp. 830-831, 1988

[73] THEVA (August, 2009) [Online]. http://www.theva.com

[74] S. Chang and S. Sivoththaman, "Development of low temperature MEMS process with PECVD amorphous silicon," *J. Micromech. Microeng.*, vol. 16, pp. 1307-1313, 2006

[75] P. D. Laforge and R. R. Mansour, "Integration of MEMS Devices and Superconducting Filters for High Q Tunable Filter Applications", *CW MEMS - Canadian Workshop on MEMS and Microfluidics*, 2007