Design and Fabrication of MIM Diodes with Single and Multi-Insulator Layers

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

A Metal-Insulator-Metal (MIM) diode is a device that can achieve rectification at high frequencies. The main objective of this research work is designing, fabricating, and characterizing thin film MIM diodes with single and multi-insulator layers.

$Cr/Al_2O_3/Cr$ and $Pt/Al_2O_3/Al$ MIM diodes have been fabricated to show the impact of the materials on the current-voltage (I-V) curve. It is illustrated that the $Cr/Al_2O_3/Cr$ MIM diode has a symmetrical I-V curve while the $Pt/Al_2O_3/Al$ MIM diode has a very asymmetrical I-V curve.

MIM diodes with single and multi-insulator layers have been fabricated to demonstrate the impact of the number of insulators on a MIM diode's performance. It is found that by repeating two insulator layers with different electron affinities and keeping the total insulator thickness the same, the asymmetry and nonlinearity values show a significant improvement in a MIM diode. While the asymmetry of the diode with a double insulator layer (MI^2M) is 3, it is 90 for the diode with a quadra insulator layer (MI^4M), which 30 times greater than that of the MI^2M diode.

Acknowledgements

I would like to express my very great appreciation to Prof. Mustafa Yavuz and Prof. Omar Ramahi for their patient guidance, enthusiastic encouragement and useful critiques of this research work.

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Finally, I would like to thank to my family and my friends who always encouraged me throughout my studies.

To my family…

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Chapter 1
Introduction

Continuous increasing demand for energy makes it necessary to investigate new energy sources which have to be efficient, safe, and cheap. Although fossil fuels are commonly used due to their efficiency, they are not environmentally friendly and are expensive. Solar cells are one of the more significant energy sources; but they are not as efficient as fossil fuels due to the limited band gaps of the semiconductors and they are not cost efficient. However, the sun is still a significant energy source since the earth receives 1000 W/m^2 from the sun at sea level during clear weather conditions [1]. This huge amount of energy received from the sun lead researches to find new techniques to convert solar energy into electricity. One of the energy harvesting devices is a rectifying antenna, also called rectenna, which directly converts solar radiation into electricity. The rectenna consists of an antenna, a rectifier system, and a DC pass filter as shown in Figure 1.1.

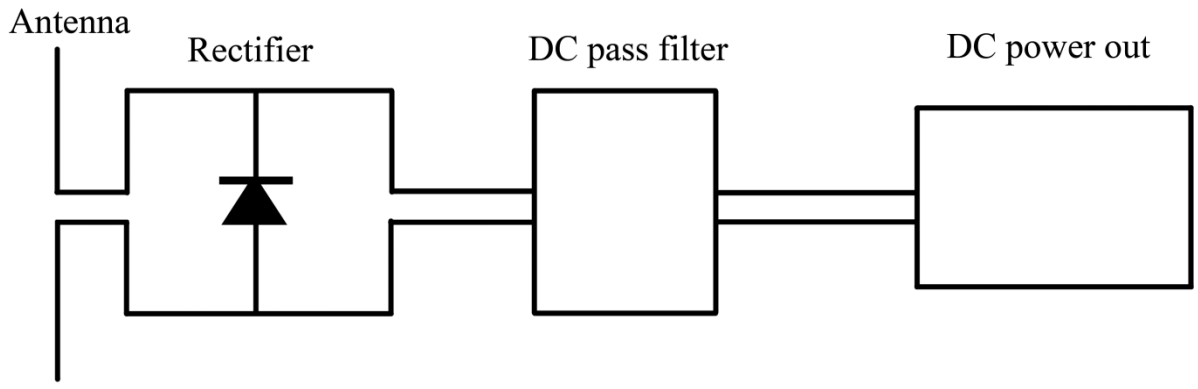

Figure 1.1: A block diagram of a rectenna

In this system, the antenna receives the electromagnetic radiation and then the rectifier directs the current only in one direction. Next, the DC pass filter turns the current into a direct current (DC) to make DC power output possible. The radiation received from the sun is the most intense in the visible and infrared range. The rectifier of the rectenna should have a very fast response time to rectify the current at these high frequency ranges. Tunneling diodes are a kind of diode that can rectify the current at high frequencies due to their fast response time. The first tunnel diode was discovered in 1957 by Leo Esaki who received a Nobel Prize in physics for this discovery in 1973 [2].

A rectifier with high response time is critical for infrared detectors, hot electron transistors [3, 4], liquid-crystal display backplanes [5], macro-electronics [6], field-emission cathodes [7], and switching memories [8]. Schottky diodes are one of the commonly used tunneling diodes in these applications because of their fast response time. Martin [9] used a metal-semiconductor-metal GaAs Schottky diode and shown to perform at 2.7 THz. However, Schottky diodes do not operate efficiently at high THz frequencies. A metal-insulator-metal (MIM) diode, which is a thin insulator layer sandwiched between two metals, is superior to Schottky diodes beyond the 12 THz [10]. MIM diodes have been investigated since the early 1960's [11]. The concept of using a MIM diode for solar energy harvesting was originated by NASA in 1982 [12]. They had a problem with coupling efficiency between antenna and diode [12]. Gustafon [13] has stated that, theoretically, 100% efficiency is possible and he claims that challenges in fabrication process limit efficiency. However, Landsberg [14] says that the coupling efficiency is limited by 93% because of noises. Recently, Bareiß et al. [15] fabricated 93 nm diameter MIM nano-diodes and claimed that these nano-scale diodes can

properly operate up to 219 THz. MIM diodes can operate at the THz range due to their femto-second fast transport mechanism of quantum tunneling [16]. It is valuable to conduct further research on these diodes that operate at high frequencies with significant efficiency.

1.1 Objectives

The key objective of this research work is to increase the asymmetry and nonlinearity characteristics of thin film MIM tunnel diodes. MIM tunnel diodes having two different metals with a single insulator make it possible to have asymmetrical current-voltage (I-V) characteristics. Different metals have different work functions which affects the degree of asymmetry. By changing the thickness of the insulator layer in a MIM tunnel diode, the nonlinearity changes. This work explains both experimental and theorical effects.

Another objective of this work is demonstrating the impact of the number of insulators in a MIM tunnel diode by fabricating MIM diodes with single and multi-insulator layers.

Illustrating the importance of the tunneling phenomenon in MIM diodes is another objective of this work. The tunneling probability has to be considered before fabricating a MIM diode to have a higher current density (J).

1.2 Thesis Organization

In chapter 2, operation theory and I-V, asymmetry, nonlinearity characteristics of the MIM tunnel diode is explained. In this section, the tunneling phenomenon in MIM diodes is elucidated in detail.

Chapter 3 focuses on processing techniques that are used during the fabrication process. There are four main techniques used in thin film technology: lithography; thin film deposition; insulator growth; and etching. In the lithography section, UV and e-beam lithography techniques are explained. E-beam evaporation and magnetron sputtering deposition techniques are detailed in the thin film deposition techniques section. In the insulator deposition section, the insulator deposition techniques for MIM tunnel diodes are stated, and the atomic layer deposition technique is explained in detail. In this chapter, etching and lift-off processes are also explained.

In chapter 4, design parameters of MIM tunnel diodes are illustrated. Capacitance of the diode, cut-off frequency, and the response time of the MIM diodes are explained in this section. This chapter also explains the material selection parameters and fabrication processes of MIM tunnel diodes with a single insulator layer.

Chapter 5 illustrates multi-insulator layer MIM diodes. MIM diodes with double and quadra insulator layers are stated, and the fabrication process is detailed.

In chapter 6, I-V curve, asymmetry, and nonlinearity of the fabricated diodes are stated. MIM diodes with single, double, and quadra insulator layers are compared and the impact of the number of the insulator is discussed in detail.

Finally, in chapter 7, the conclusion and recommendations for future work are presented.

Chapter 2
MIM Tunnel Diodes

2.1 Fundamentals of MIM diode

A metal-insulator-metal (MIM) diode is a thin insulator layer that is sandwiched between two metals. Quantum mechanically, a particle can tunnel through a barrier, which is not possible in classic mechanics. Tunneling becomes more significant when the barrier is in nano-scale. In MIM diodes, the insulator layer is considered to be a potential barrier. The thickness of the potential barrier should be less than 10 nm to achieve tunneling [17]. In a MIM diode, free electrons at metal 1 (M1) can tunnel to metal 2 (M2) when the insulator layer is several nanometers thick. Similarly, free electrons at M2 can tunnel to M1. The tunneling from M1 to M2 causes a current from M2 to M1, and the tunneling from M2 to M1 causes a current from M1 to M2. These current densities (J) are calculated by equations 1-1 and 1-2 [17].

$$J_{2\to1} = \frac{4\pi m_2 q}{h^3} \int_0^\infty T(E_x)[\int_{E_x}^\infty f_2(E)dE]dE_x \qquad (1-1)$$

$$J_{1\to2} = \frac{4\pi m_1 q}{h^3} \int_0^\infty T(E_x)[\int_{E_x}^\infty f_1(E)dE]dE_x \qquad (1-2)$$

where, m is mass of the electron, q is charge of the electron, h is Planck's constant, T(E) is tunneling probability, f_1 and f_2 are Fermi distribution functions which are shown in equations 1-3a and 1-3b.

$$f_1(E) = \frac{1}{\exp\left(\frac{E - E_f}{kT}\right) + 1}, \quad f_2(E) = \frac{1}{\exp\left(\frac{E - E_f + qV_{bias}}{kT}\right) + 1} \quad (1 - 3a, b)$$

where E_f is the Fermi level of the metal, k is the Boltzmann constant, V is the applied bias, and *T* is the temperature. As seen in Equations 1-1 and 1-2, the current density can only be changed by the tunneling probability and Fermi distribution functions. The tunneling probability increases exponentially by decreasing the thickness of the insulator layer in a MIM diode. The Fermi distribution functions change by applied bias and barrier height value (φ), which is the potential difference between two materials. The barrier height value is determined by the difference between the work function (Φ) of the metal and the electron affinity (χ) of the insulator at the metal-insulator interfaces. Therefore, the type of material and the thickness of the insulator are very important in MIM diodes. In Figure 2.1, the energy band diagrams of MIM tunnel diodes with the same metals, different metals and under the negative bias are stated.

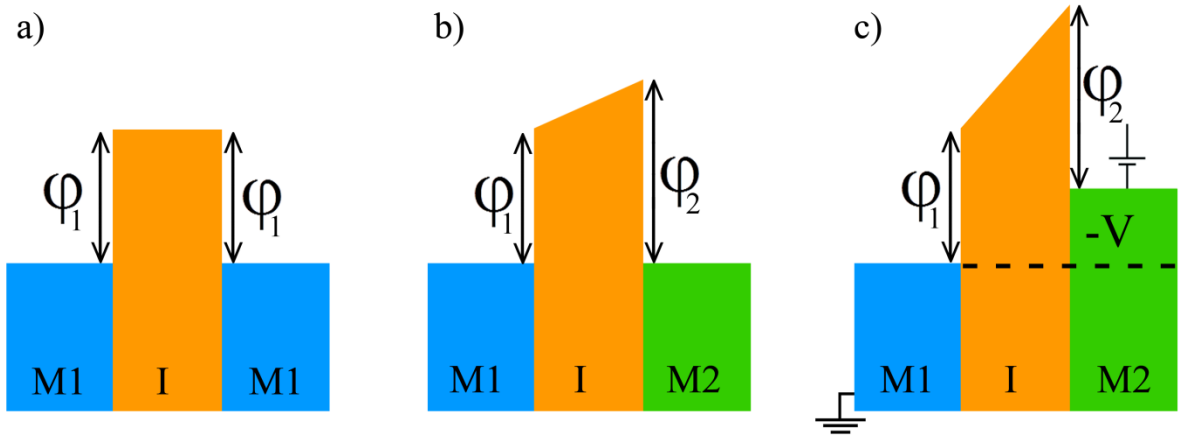

Figure 2.1: Energy Band Diagram of a MIM diode when (a) two metals are the same, (b) metal 1 and metal 2 is different, (c) negative voltage applied to metal 2

The current density that flows from M1 to M2 ($J_{1\rightarrow 2}$) is the same as the current density that flows from M2 to M1 ($J_{2\rightarrow 1}$) when the work functions of the M1 and M2 are the same (Figure 2.1 (a)). The current density in positive direction becomes greater when M2 has a higher work function value than M1 (Figure 2.1 (b)). In this case, energy band diagram of the insulator shows a triangular shape. If a negative bias is applied to M2, this triangular shape becomes sharper (Figure 2.1 (c)), and the tunneling distance becomes less at higher energy levels which makes the tunneling probability higher at those energy levels. Therefore, in the case of Figure 2.1 (c), the current density in positive direction is much higher than negative direction. As well, the positive current density is greater in the case of figure 2.1 (c) than in the case of Figure 2.1 (b) due to a higher energy level in M2.

2.2 Characteristics of the MIM Diode

Current-voltage curve, asymmetry, and nonlinearity are important parameters that show the performance of a diode. These parameters change by the work functions of the metals, electron affinity of the insulator, thickness of the insulator, etc. In the following sections, each of these parameters will be explained.

2.2.1 Current-Voltage Curve

A current-voltage (I-V) curve is a relationship between the electric current and the corresponding voltage in a circuit, device, or material. This relationship is generally represented as a graph which is used to determine some parameters of a device. In MIM diodes, these parameters are turn-on and breakdown voltage values, asymmetry, non-linearity, and responsivity. An ideal diode should transmit the forward current and block the

reverse bias. In other words, an ideal diode should have a turn-on voltage close to zero volts, and a high breakdown voltage to make rectification possible.

Decreasing the thickness of the insulator layer changes the behavior of the I-V curve in a MIM diode. A thinner insulator layer makes higher tunneling probability possible at lower voltages. The turn-on voltage can be close to zero volts in MIM diodes with an extremely thin insulator layer.

2.2.2 Asymmetry

Asymmetry is simply defined as the forward current divided by the reverse current. When the I-V curve in forward direction is different from the reverse direction, this I-V curve is called asymmetric. The asymmetry is high when the difference between the amplitude of the turn-on voltage and breakdown voltage is high. The asymmetry value in a diode should be greater than 1 in order to rectify current. If two metals of the MIM diode with one insulator layer are the same material, the I-V curve shows a symmetrical behavior. The asymmetry value is high when the difference between the work functions of the metals is high in a MIM diode with a single insulator layer. If there is more than one insulator, all interfaces should be considered to determine the asymmetry. The asymmetry of an I-V curve can be simply calculated by the equation 2-1.

$$\left|\frac{I_F}{I_R}\right| \qquad (2-1)$$

where, I_F is the forward current and I_R is the reverse current at a certain voltage.

2.2.3 Nonlinearity

The degree of the sharp turn-on voltage is defined as nonlinearity. High current density can be achieved by high nonlinear diodes at lower voltages. The nonlinearity is calculated by equation 2-2.

$$\frac{dI}{dV} \Big/ \frac{I}{V} \qquad (2-2)$$

The nonlinearity should be greater than 3 for an ideal diode [18]. High nonlinearity can be achieved by using metals with high work functions and a thick insulator layer in a MIM diode [19]. However, increasing the thickness of the insulator decreases the tunneling probability. MIM diodes with multi insulator layers can solve this problem [19].

Chapter 3
Manufacturing Techniques

Deposition, lithography, and etching are fundamental processing techniques in micro and nano-fabrication. Basic processing steps for fabricating metal patterns on a substrate are illustrated in Figure 3.1. First, the desired thin film on a substrate is grown. Next, the thin film layer is covered by a photoresist layer. After the photo-mask alignment, photoresist is exposed by applying ultraviolet (UV) light. An appropriate developer, depending on the photoresist, is applied to the sample to remove exposed areas of photoresist. Finally, the process is completed by etching the thin film and cleaning the remaining photoresist on the sample. In the following sections, lithography, thin film and insulator deposition, etching, and lift-off techniques are stated.

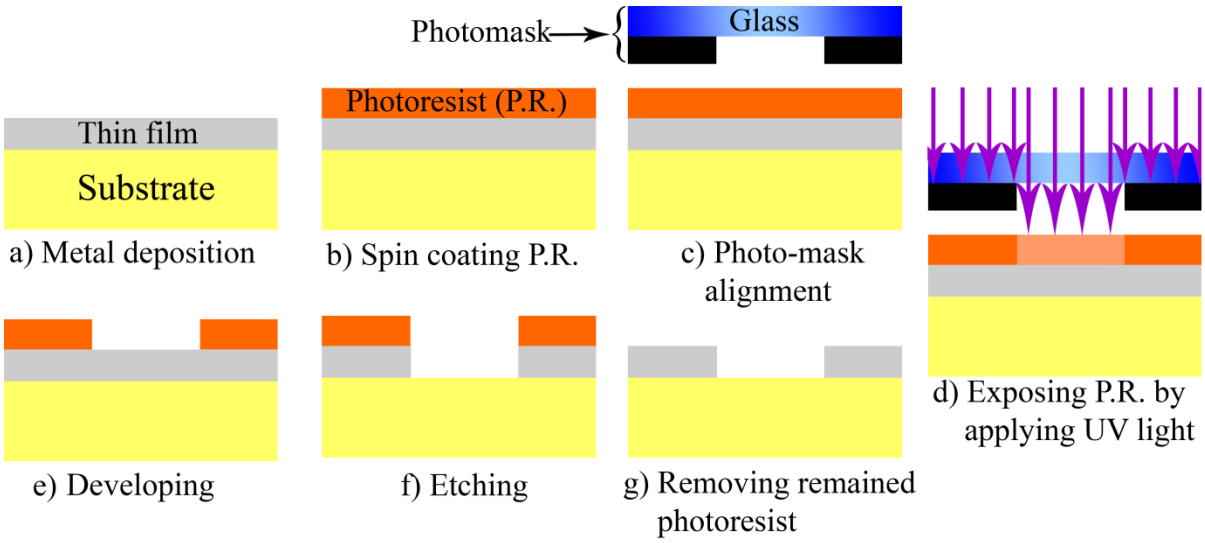

Figure 3.1: Basic processing steps to fabricate metal patterns on a substrate

3.1 Lithography Techniques

Lithography is one of the most important processes in nano and micro fabrication. Ultraviolet (UV) or photolithography, electron-beam (e-beam) lithography, nanoimprint lithography, interference lithography, X-ray lithography, extreme ultraviolet lithography, magnetolithography and scanning probe lithography are some of the lithography techniques that are used in nano and micro fabrication. Photolithography and e-beam lithography are the most common lithography techniques. In the following sections, these two techniques will be introduced.

3.1.1 Photolithography

Photolithography, also called UV or optical lithography, is a process that transfers geometric shapes on a mast to a substrate by ultraviolet light. The purpose of optical lithography is patterning micro-scale structures in the photoresist that can be transferred to a substrate material. The photolithography process includes substrate cleaning, photoresist coating, soft baking, mask alignment, exposure, development and hard baking steps. Each of these steps, positive and negative photoresists, are briefly introduced in the following sections.

3.1.1.1 Substrate Cleaning and Photoresist Coating

First, the substrate, which can be a thin film layer on a wafer, is cleaned by applying appropriate chemicals to make sure there is no impurity. After the cleaning process, photoresist can be applied to the surface of the sample. Next, the substrate is rotated at a high speed to spread the photoresist homogeneously by centrifugal force. The thickness of the

photoresist can be optimized to the desired thickness by managing the duration and speed of the rotation. This process is called spin coating.

3.1.1.2 Soft Baking (Pre-baking)

Soft baking is simply applying heat to the sample to remove the solvent component of the photoresist. The photoresist becomes ultraviolet light sensitive which makes the photolithography possible. After the soft baking process, the thickness of the photoresist generally decreases since the solvent is removed from the photoresist. A short soft baking of the sample blocks ultraviolet light from reaching the sensitizer because most of the solvent remains in the photoresist. Over-baking the sample increases the ultraviolet light sensitivity and generally destroys the sensitizer. Over-baking the sample also causes the reduction of the developer solubility.

3.1.1.3 Mask Alignment and Exposure

A photomask is typically patterned metal film on one face of a glass plate. In photolithography, chromium is generally preferred for the photomask. The mask alignment is one of the most important steps in photolithography process. The photomask should be aligned with the sample before the photoresist is exposed. If there are two different layers designed to fabricate, the first pattern on the sample should be aligned with the second pattern on another photomask. Some marks on the both photomasks can be used to make alignment easier and better. Misalignment causes a shift of the patterns, which is not desired. The sample is ready for applying the ultraviolet light when the alignment is completed. The photoresist is exposed through the pattern on the photomask once the ultraviolet light is

applied to the sample. There are three exposure methods in photolithography: contact printing; proximity printing; and projection printing. A schematic illustration of these three methods is presented in Figure 3.2.

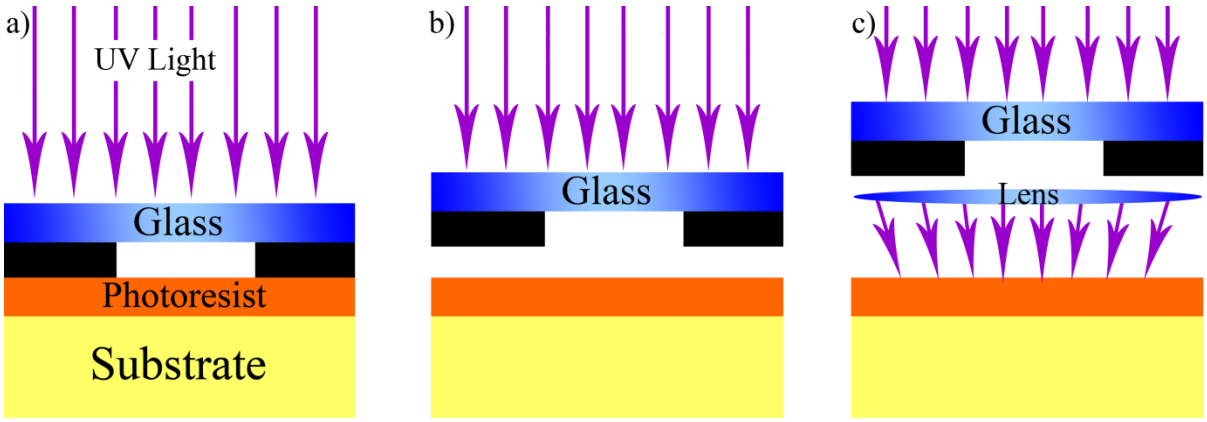

Figure 3.2: A schematic illustration of exposure methods in photolithography: a) contact printing, b) proximity printing, c) projection printing

The contact printing method is placing the photomask in physical contact with the photoresist. In this method, the photoresist is exposed to ultraviolet light while the sample is contacted with the photomask. Contact printing method makes it possible to achieve a very high resolution such as 0.5 micron structures can be created. However, this method causes defects in the pattern and can damage the mask.

The *proximity printing* method is placing the photomask with a few tens of microns gap from the photoresist. In this method, a few microns resolution can be achieved. The gap between the photomask and photoresist decreases the damage in the proximity printing method. However, there still can be a small number of defects if the photoresist on the sample is not uniform.

The *projection printing* method uses a lens between the sample and photomask. In this method, only a small part of the mask is imagined to achieve high resolution. This small part of the photomask is repeated over the sample in projection printing method which makes it possible to achieve approximately a 1 micron resolution. In this method, photomask damage is completely eliminated.

3.1.1.4 Development and Hard Baking

The exposed areas of the photoresist are more soluble than unexposed areas in the proper chemical solution which is called developer. To remove exposed areas of the photoresist, the developer should be applied for a proper time which is called developing time. The developing time changes for different photoresists and different developers. The developing time should be well determined to achieve a high resolution.

After the developing process, a baking step is applied to the sample as a final step of the photolithography which is called hard baking. Hard baking increases the adhesion between two surfaces and the remaining photoresist, and hardens the photoresist that remains.

3.1.1.5 Positive and Negative Photoresist

Positive and negative photoresists are two types of the photoresist. A positive photoresist is preferred to pattern the exact same geometric shapes on the photomask to the thin film by applying an etching process. Once ultraviolet light is applied to the positive photoresist, the light exposes the photoresist in the areas illustrated in Figure 3.3. After the developing and etching processes, the structures on the photomask will be directly transferred to the sample (Figure 3.3).

In the case of the negative photoresist, the patterns on the photomask are removed from the sample and the inverse pattern of the photomask is transferred to the sample. An applied ultraviolet light makes the negative photoresist more difficult to solve. Thus, the negative photoresist remains on the sample when it is developed with a proper developer. The developer removes only the unexposed areas. After the developing and etching processes, the inverse pattern of the photomask will be transferred to the sample as shown in Figure 3.3.

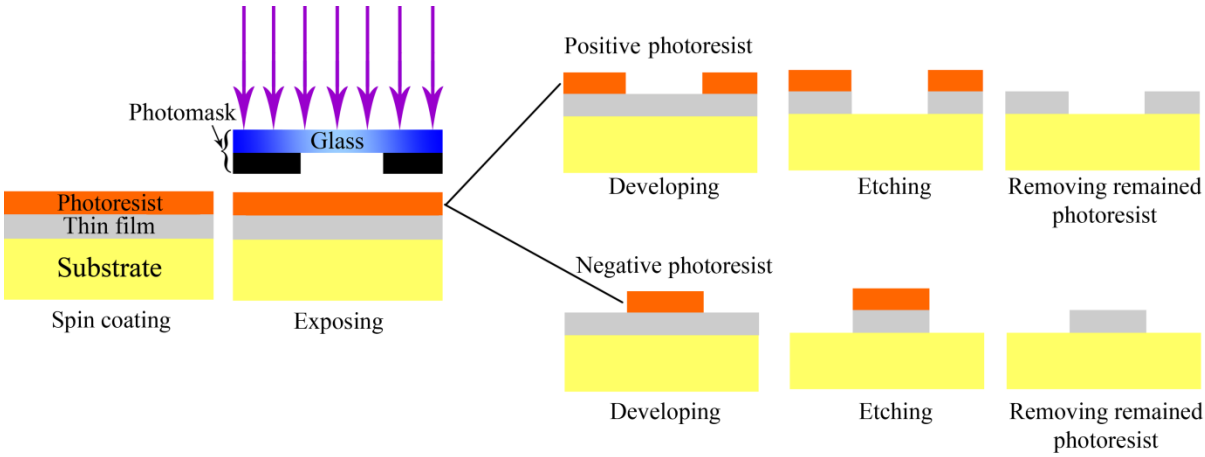

Figure 3.3: A Schematic illustration of the photolithography process with positive and negative photoresists

3.1.2 Electron Beam Lithography

Electron Beam (E-beam) lithography is one of the main lithography techniques for fabricating nano-scale patterns in a resist that can be transferred to a substrate material. In e-beam lithography, the lithography process is similar to the process for optical lithography. However, in e-beam lithography, instead of ultraviolet light, an accelerated electron beam is used for exposing resist which is sensitive to electrons. An e-beam exposes the resist dot by dot to create patterns in this technique. The side and top views of the working mechanism of

e-beam lithography is shown in Figure 3.4 [20]. The e-beam lithography system is usually connected to a scanning electron microscope (SEM) to monitor the sample before writing in order to determine the area that the pattern will be generated. Monitoring becomes significant when there is more than one layer fabricated because the SEM allows for the making of ultra-fine alignment.

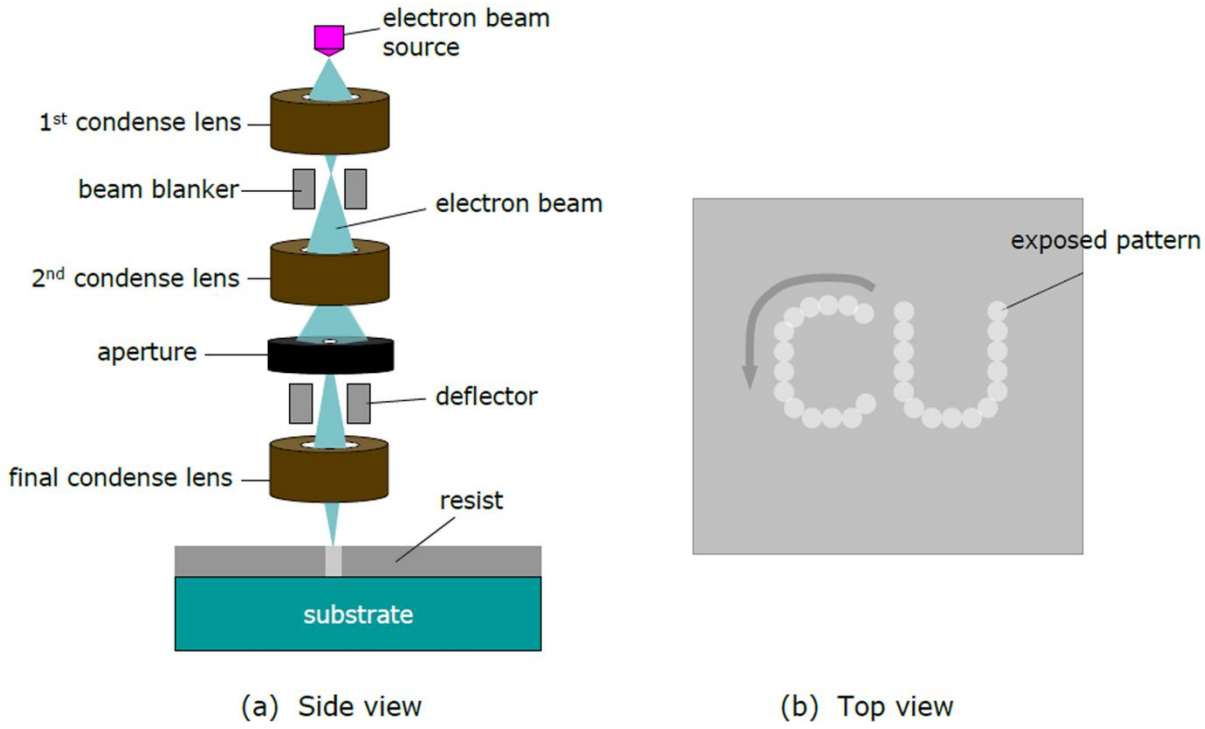

Figure 3.4: A Schematic diagram of e-beam lithography. The e-beam is focused on a resist to generate patterns by exposing dot by dot: (a) side view of the e-beam lithography setup; (b) top view of the exposed pattern by a serial writing [20].

The major advantage of e-beam lithography is to create nano-scale structures that are possible to provide because of the ultra-short wavelength of the electron. E-beam lithography is also a maskless lithography technique which is another advantage of the technique.

The major problem with e-beam lithography is that it has a very low throughput; that is, writing a chip pattern takes eight hours by e-beam lithography [21]. This very long writing time may cause the beam to drift, or instability, which is not undesired.

3.2 Thin Film Deposition Techniques

A thin film is a layer of material which is as thin as a few angstroms to as thick as several micrometers. Thin films have a variety of applications in the fields of optics, chemistry, mechanics, magnetics, and electricity. Providing a thin film to a surface is called thin film deposition. Chemical and physical depositions are two main types of thin film deposition techniques. Plating, chemical solution deposition (CSD), spin coating, chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), and atomic layer deposition (ALD) are types of chemical deposition techniques. Thermal evaporation, electron beam (e-beam) evaporation, molecular beam epitaxy (MBE), sputtering, pulsed laser deposition, cathodic arc deposition (arc-PVD), and electro-hydrodynamic deposition (electro-spray deposition) are types of physical deposition. In the following section, e-beam deposition and sputtering physical deposition techniques are introduced. ALD chemical deposition technique will be stated under the insulator deposition techniques section.

3.2.1 Electron Beam Evaporation

In an evaporation process, a source material is heated to evaporate. When the material that is wanted to deposit is evaporated, it condenses on the substrate. This process takes place inside a vacuum chamber in order to allow the molecules to evaporate freely. For e-beam evaporation, an electron beam is used to heat the source material and cause evaporation. The

deposition chamber should be evacuated to a pressure of at least 7.5 x 10^{-5} Torr for e-beam evaporation [22]. An e-beam evaporation system mainly consists of a deposition chamber, electron gun, source material, target material, and power supply. First, the electron beam is generated by supplying power from tens to hundreds of kW to electron guns. Next, the generated electron beam is accelerated by increasing the applied power to increase its kinetic energy. Then, the electron beam is directed by applying a magnetic field. Once the electrons hit the source material, they lose their energy rapidly. The kinetic energy of the electrons converts to thermal energy after they rapidly hit the source material [23]. This thermal energy causes the source material to melt. If the temperature is high enough, the melted material converts into vapor. Finally, the evaporated material condenses on the substrate. In Figure 3.5, a schematic illustration of the e-beam evaporation mechanism is illustrated.

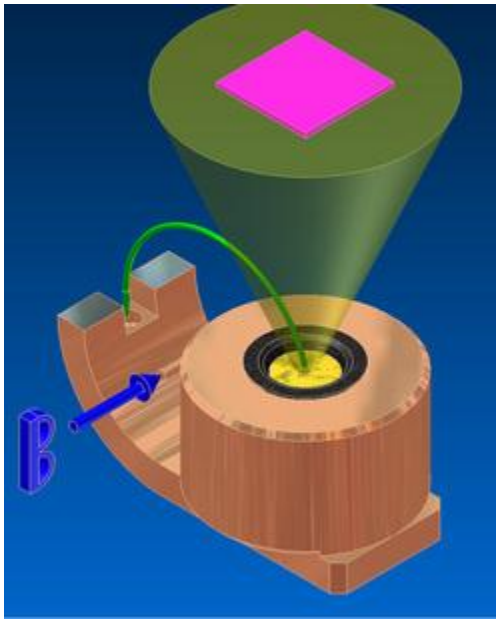

Figure 3.5: A schematic illustration of the e-beam evaporation mechanism [24]

Source material is deposited very directionally in e-beam deposition which makes lift-off possible. A schematic diagram of e-beam deposition on a stepped substrate is shown in Figure 3.6.

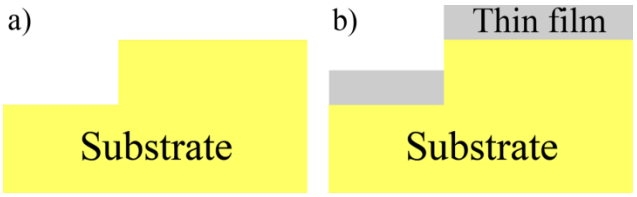

Figure 3.6: A schematic diagram of e-beam deposition on a stepped substrate

3.2.2 Magnetron Sputtering

Sputtering deposition is a type of physical vapor deposition method to deposit thin films by sputtering. Sputtering is simply ejecting particles from the source material (target) onto a substrate. A schematic diagram of magnetron sputtering mechanism is shown in Figure 3.7.

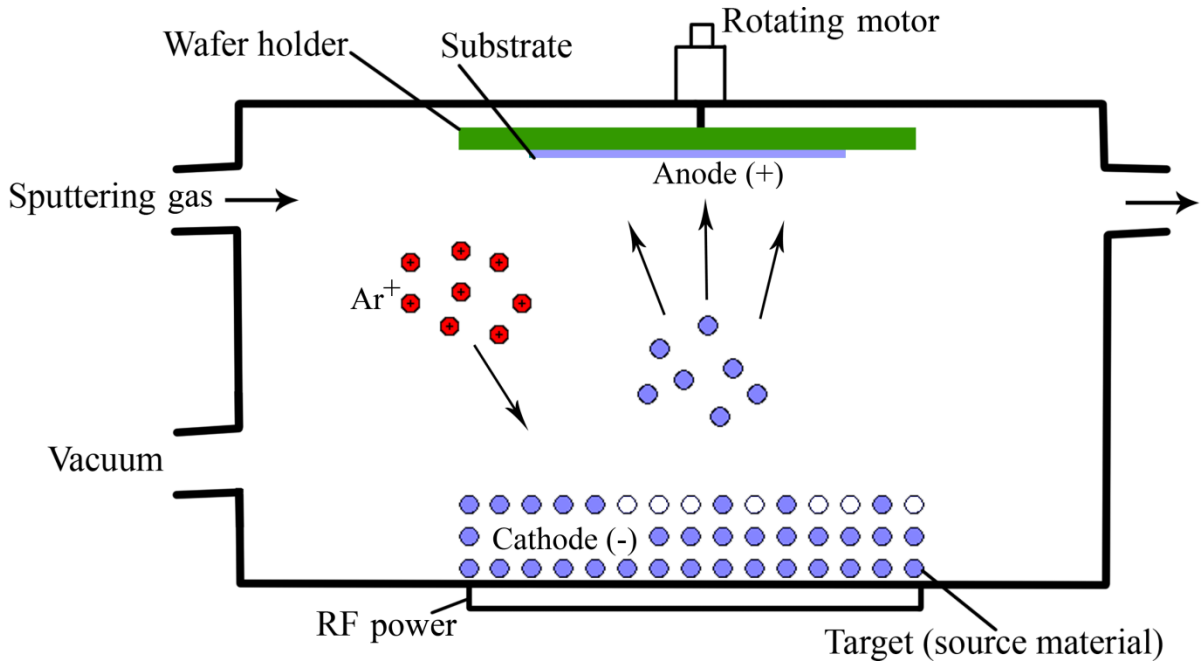

Figure 3.7: A schematic diagram of sputtering mechanism

In sputtering deposition technique, the plasma is created by applying a high negative voltage to the target source at pressure in the mTorr range. The power source can either be a DC or RF power supply. The sputtering gas is usually Argon in sputtering deposition systems. As illustrated in Figure 3.7, Ar^+ ions strike the target, and ejected particles from the target sputter everywhere in the chamber. Sputtered target atoms both form a thin film and release secondary electrons to sustain plasma. In the magnetron sputtering technique, magnetrons are used to supply strong electric and magnetic fields to trap these secondary electrons close to the sputtering target. This makes it possible to run the deposition process at a lower pressure and have a high plasma density that causes higher sputter deposition rates.

One of the important advantages of the sputtering is that materials with high melting points can be easily deposited by sputtering deposition. Nonetheless, evaporation of some materials is almost impossible. Another advantage of the sputtering is that sputtered materials usually have better adhesion to the substrate than evaporated films.

The disadvantage of the sputtering is that the lift-off process is almost not possible with this technique. The reason is because sputtering is not a directional deposition technique like the e-beam deposition. A schematic diagram of sputtering deposition on a stepped substrate is shown in Figure 3.8.

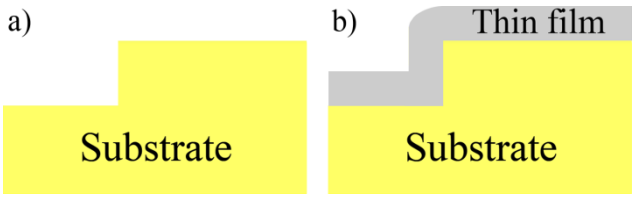

Figure 3.8: A schematic diagram of sputtering deposition on a stepped substrate

The sputtered material also grows at the sidewall which blocks the lift-off material from reaching underneath the film.

3.3 Insulator growth

The insulator layer of the MIM diode can be grown in different ways including: sputter oxidation; vapor deposition; thermal oxidation; anodic oxidation; electron-beam deposition; and atomic layer deposition. Atomic layer deposition (ALD) is considered to be the best way to provide uniform, pinhole free, ultra-thin oxide layers. The insulator growth is made one atomic layer at a time by ALD. This highly controllable deposition process makes this technique highly compatible for the growth of the insulator layer of the MIM diodes. In the following section, the ALD technique will be introduced.

3.3.1 Atomic Layer Deposition (ALD)

Atomic layer deposition is a type of chemical vapor deposition technique. The material grows one atomic layer per cycle, which makes it a self-limiting process. Starting with a conditioned surface, one ALD cycle is completed by four steps. As an example, Al_2O_3 growing steps are stated below and illustrated in Figure 3.9.

1) Pulsing the first precursor into the chamber which is trimethylaluminum (TMA) for Al_2O_3. The following reaction takes in place in this step (Figure 3.9a).

   $Al\text{-}OH + Al(CH_3)_3 \rightarrow Al\text{-}O\text{-}Al\text{-}CH_3 + CH_4$

2) Purging the deposition chamber to remove the gaseous reaction and non-reacted precursors. In the case of the Al_2O_3 deposition, they are CH_4 and TMA, respectively, (Figure 3.9b).

3) Pulsing the second precursor into the chamber which is H_2O for Al_2O_3. In this step, the following reaction takes place (Figure 3.9c).

   $Al\text{-}CH_3 + H_2O \rightarrow Al\text{-}OH + CH_4$

4) Purging the gaseous reaction and non-reacted precursors from the chamber which are CH_4 and H_2O, respectively (Figure 3.9d).

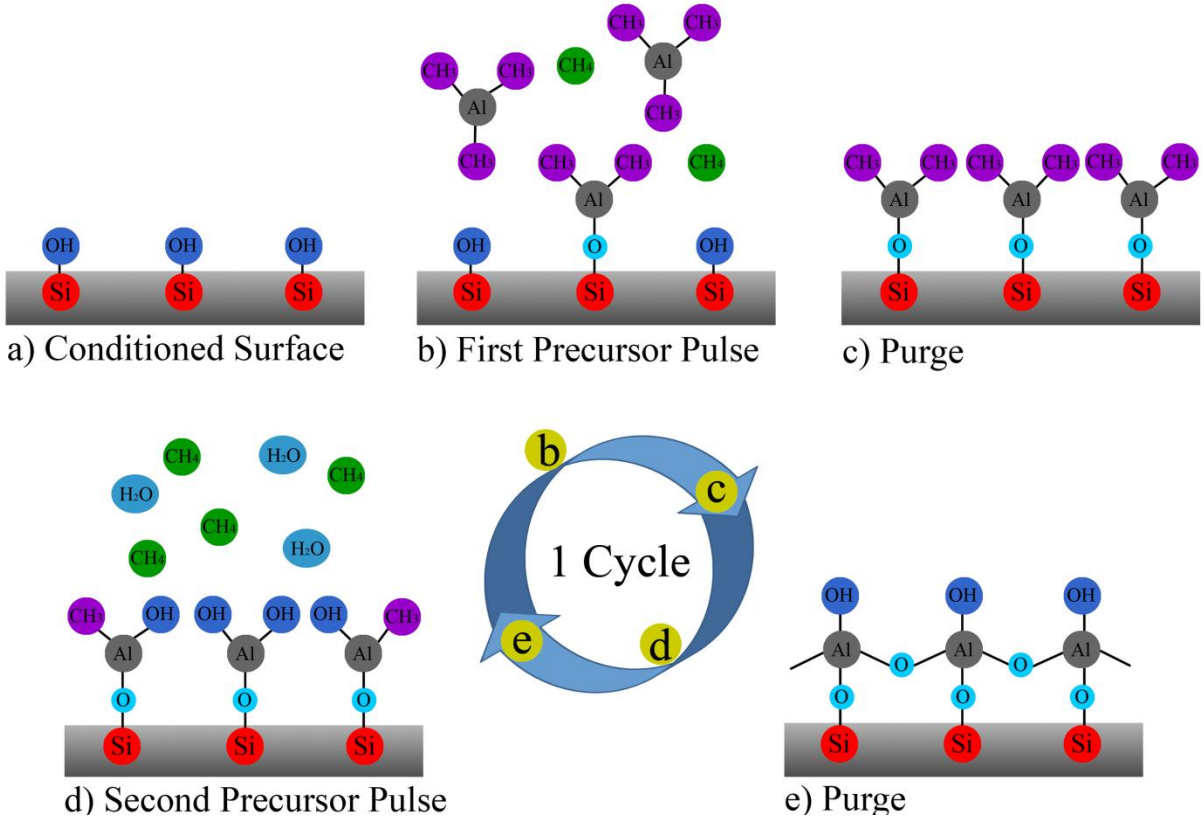

Figure 3.9: A schematic representation of one ALD cycle [25]

In the ALD technique, each cycle adds an amount of material to the surface which is called the deposition rate or growth per cycle. The number of cycles is repeated to grow material. Thin films that are grown by ALD are very uniform in thickness because of the surface-controlled process.

One of the disadvantages of this technique is that the ALD process is not suitable for the lift-off process because thin film grows on all surfaces including the side walls in ALD. In ALD, each cycle takes anywhere from 0.5 second to a few seconds, so the deposition of thicker films takes too long to be deposited which is another disadvantage of the ALD.

3.4 Etching

Etching is one of the fundamental processes in micro and nano fabrication. There are two main kinds of etching: wet and dry etching. Wet etching is typically done using proper chemicals which depend on the material to be etched. Dry etching is basically removing the material by the bombardment of ions. Wet etching is a highly selective etching process which is very useful when there are two different materials on the sample and one of them is not desired to be etched. Wet etching also does almost no damage to the substrate and is cheaper than dry etching. However, some of the etchants are fairly dangerous. Dry etching is easy to start and stop. Instead of wet etching, dry etching is less sensitive to small changes in temperature and is more repeatable. In the following section, reactive ion etching (RIE), which is one of the most common dry etching techniques, is introduced.

3.4.1 Reactive Ion Etching (RIE)

Reactive ion etching (RIE) is one of the commonly used etching techniques in nano and micro fabrication. This technology uses reactive plasma to remove material that was pre-deposited on a sample substrate. Basically, the plasma is created under a low pressure in vacuum chambers by an applied electromagnetic field. Radio frequency (RF) power is generally preferred to create electromagnetic field. Different gasses are used to generate plasma depending on the type of material to be etched. The applied RF power ionizes the gas molecules and creates plasma. The field is typically created at 13.56 MHz and a few hundred watts. Highly energetic ions, which are created from the plasma, strike on the top of the sample surface and react with it. Both etching due to the collision as well as sputtering some material due to transferring some energy during the reaction will be possible. A schematic representation of the RIE mechanism is shown in Figure 3.10.

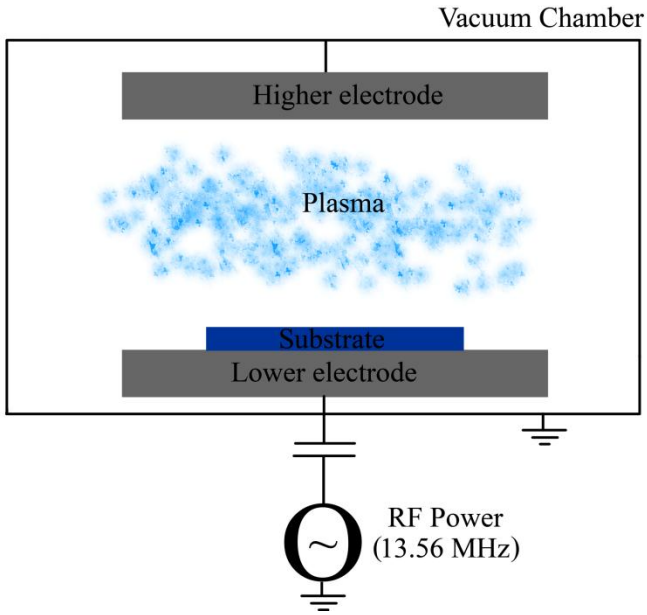

Figure 3.10: A schematic representation of RIE

3.4.2 Lift-Off

Lift-off is a simple method for pattering pre-deposited films. In this method, a substrate is patterned by photolithography before the thin film deposition (Figure 3.11a and 3.11b). Once the film is deposited, unwanted patterns are deposited on the photoresist, and blanked parts of the substrate are deposited by the thin film (Figure 3.11c). A proper chemical, which is called a solvent, is used to remove the photoresist under the thin film in the lift-off process. In this step, the solvent takes the thin film with photoresist, and the thin film on the substrate remains as shown in Figure 3.11d.

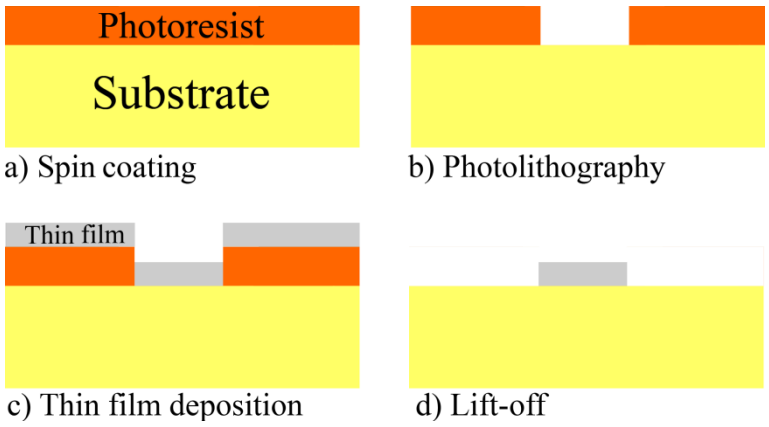

Figure 3.11: A schematic representation of the lift-off process

Chapter 4
Design and Fabrication of MIM Diodes

4.1 Design Parameters

An ideal MIM diode should have good asymmetry, response time, cut-off frequency, nonlinearity, and I-V characteristics. Material type, thickness of the insulator layer, junction area, capacitance, and permittivity are some parameters that determine these characteristics. High operation frequency makes MIM diodes different than others. The cut-off frequency is given by equation 4-1.

$$f_c = \frac{1}{2\pi R_d C_D} \qquad (4-1)$$

where f_c is the cut-off frequency, R_d is the resistance of the device that is connected to MIM diode, C_D is the capacitance of the diode. As seen in equation 4-1, the R_dC_D time constant should be low to have high cut-off frequency. The R_d value is generally constant for most of the devices, that is, antennas, so the cut-off frequency depends significantly on the capacitance of the diode which is given by equation 4-2.

$$C_D = \frac{\varepsilon_0 \, \varepsilon \, A}{d} \qquad (4-2)$$

where ε_0 is permittivity of free space, ε is the permittivity of the insulator layer, A is the junction area, and d is the thickness of the insulator layer of the MIM diode. Low capacitance can be achieved by having a small junction area, an insulator layer with a small permittivity value, and a thick insulator layer. However, permittivity is constant for the chosen insulating

material and having a thick insulator layer decreases the tunneling efficiency. Therefore, the junction area plays an important role in determining the capacitance of the MIM diode. The junction area should be about 20 nm x 20 nm for operating a MIM diode at frequency for 4 F m^{-1}, 3 nm, 50 Ω values of permittivity, insulator thickness and resistance, respectively.

4.1.1 Material Selection

The type of material has a significant impact on the characteristics of the MIM diode. Work function values of the metals are one of the important factors that should be considered. Work function values for different metals are stated in Table 4.1.

Table 4.1: Work Functions of the Metals [26, 27]

Metal	Work function (eV)
Pt	5.65
Ni	5.15
Pd	5.12
Au	5.1
Mo	4.6
W	4.55
Hg	4.52
Cr	4.5
Cu	4.4
Bi	4.4
Sn	4.38
Ti	4.33
Fe	4.31
Al	4.28
Ag	4.26
Zn	4.24
Cd	4.1

Metal	Work function (eV)
Sb	4.08
Pb	4
Nb	3.99
Ga	3.96
Be	3.92
Mn	3.83
In	3.8
Tl	3.7
Mg	3.64
Ca	2.8
Ba	2.49
Li	2.38
Na	2.35
Sr	2.35
K	2.22
Rb	2.16
Cs	1.81

Different work function values causes different barrier heights, which determine I-V characteristics of the MIM diode, between the insulator and metal interface as stated in chapter 2.

In addition to work functions, the electron affinity of the insulators is also important since it determines the barrier height values. The electron affinity of the insulators changes depending on the thickness of the insulator [28] and the deposition technique.

Cost, availability, conductivity, and compatibility with the current fabrication technology are other parameters that should be considered in material selection.

4.1.2 Mask Design

Dimensions of the structures are important since the operation frequency of MIM diodes changes by the junction area. Hence, the mask is critical in the fabrication process. Desired patterns can be designed with mask design software. The mask does not have to be printed in the e-beam lithography technique because the designed patterns can be written directly on the resist. However, after the design, the patterns should be printed on a glass for photolithography.

The fabrication process can be done with either one or two photolithography processes. If contact pads are needed for the MIM diode, the fabrication should be done at least by two photolithography processes which require proper photomasks. In Figure 4.1a, a photomask (Mask A) is illustrated for the first layer of the MIM diode. The photomask (Mask B) for the second metal and the insulator layers is shown in Figure 4.1b. After the fabrication, the diodes are seen as Figure 4.1c. Mask A is designed to have 10 µm x10 µm, 20 µm x 20 µm,

and 30 µm x 30 µm contact areas with Mask B. Four contact pads have been designed for Mask A in order to minimize misalignment. If the contact pads are not necessary, a photomask (Mask C) can be designed as dots (Figure 4.1d). Mask C is designed to have 5 µm, 10 µm, 20 µm, and 30 µm diameter dots.

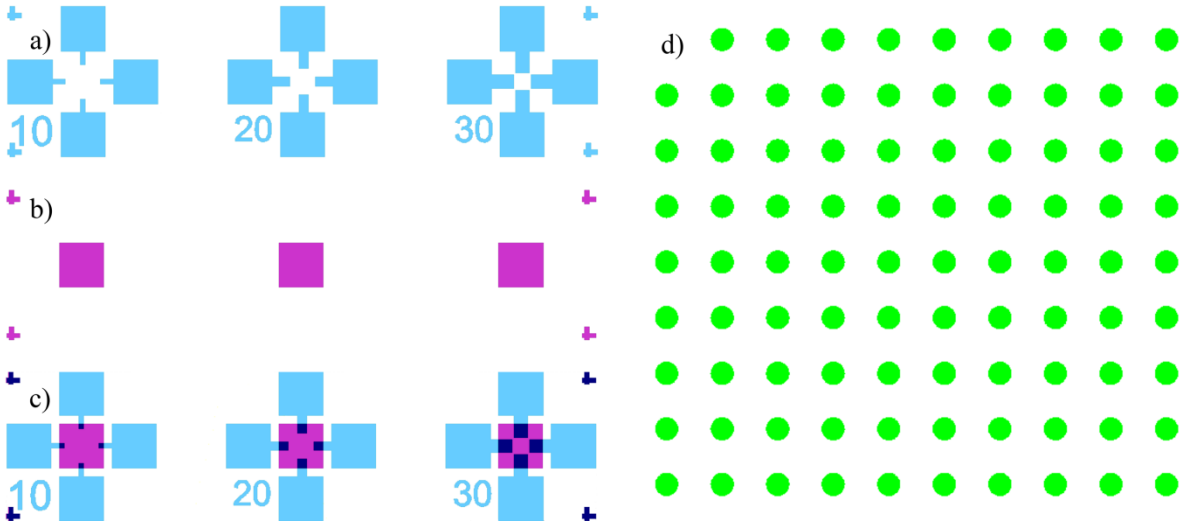

Figure 4.1:a) Mask A, b) Mask B, c) Combination of Mask A and MaskB2, d) Mask C.

4.2 Fabrication Process

Different MIM diodes have been fabricated to illustrate the impact of the type of the materials on a diode's performance. A Platinum-Alumina-Aluminum ($Pt/Al_2O_3/Al$) MIM diode has been fabricated to have a MIM diode with a high asymmetrical I-V curve. A Chromium-Alumina-Chromium ($Cr/Al_2O_3/Cr$) MIM diode has been fabricated to have a symmetrical I-V curve. Chromium/Titanium dioxide/Alumina/Titanium ($Cr/TiO_2/Al_2O_3/Ti$) MI^2M and Chromium/Titanium dioxide/Alumina/Titanium dioxide/Alumina/Titanium ($Cr/TiO_2/Al_2O_3/ TiO_2/Al_2O_3/Ti$) MI^4M diodes have been fabricated to illustrate the impact of the number of the insulators on the diodes' characteristics.

The fabrication process of the $Pt/Al_2O_3/Al$ and $Cr/Al_2O_3/Cr$ MIM diodes is introduced in the next sections. $Cr/TiO_2/Al_2O_3/Ti$ and $Cr/TiO_2/Al_2O_3/ TiO_2/Al_2O_3/Ti$ diodes will be discussed in the chapter 4.

4.2.1 $Pt/Al_2O_3/Al$ MIM Diode

The substrate of the diode was chosen to be a bare silicon wafer. The selected materials used as the top and bottom electrodes were platinum and aluminum, respectively. The reason for choosing these materials is the high difference in the work function of platinum and aluminum which are good candidate metals for the diode. The work function of Pt is 5.65 eV and that of Al is 4.28 eV.

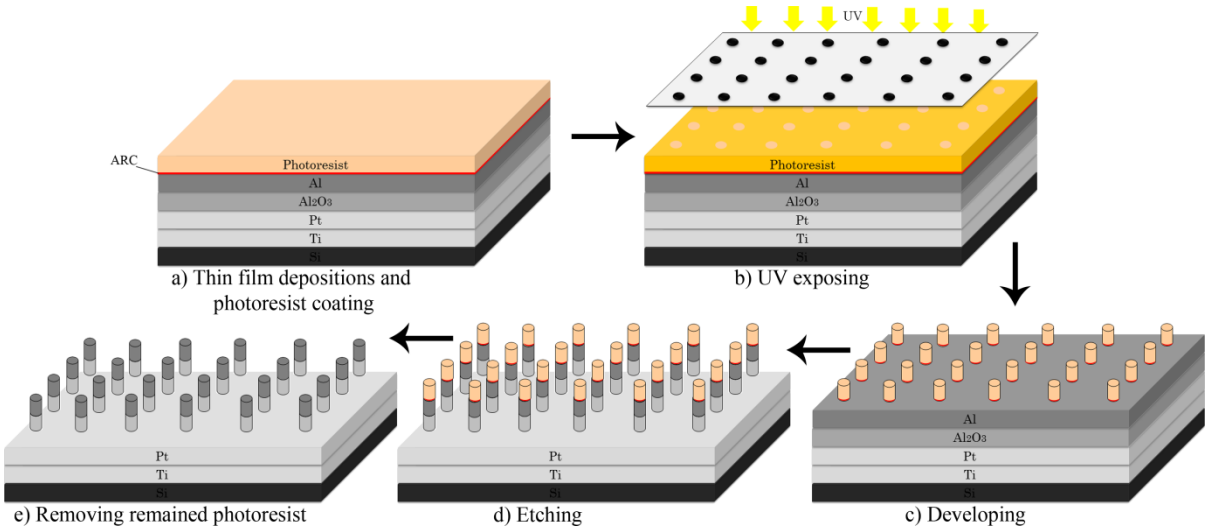

Figure 4.2: Fabrication steps of $Pt/Al_2O_3/Al$ MIM diode

Electron-beam (e-beam) evaporation was used to deposit 50 nm of Ti onto the Si wafer in order to allow the 10 nm Pt layer to adhere to the substrate. Following that, a 4 nm alumina (Al_2O_3) layer was deposited onto the Pt layer using Atomic Layer Deposition (ALD) technique. ALD is more preferred than the oxygen plasma technique since it is more precise

and controllable, and leads to a uniform insulator layer, which is good for the tunneling efficiency. After a 50 nm Al was deposited onto the insulator layer, a thin layer of anti-reflective coating (ARC) was applied to the surface in order to protect Al. A positive photoresist (S1813) was spin coated onto the ARC under layer prior for photolithography. The spin coating conditions were 2000 rounds per minute for 40 seconds and followed by 1 minute of soft baking at 110^{o}C. In Figure 4.2a, a schematic illustration of the sample is shown after the deposition and coating processes. A mask aligner was then used to carry out photolithography to pattern the device with a proper photomask, which is similar to the mask C (Figure 4.1d), that has 5 micron diameter dots with 20 micron spacing. G-line was chosen to expose the substrate using soft contact exposure type and 5 seconds as the exposure time (Figure 4.2b). The photoresist was developed by AZ 300 MIF developer for 1 minute, and Reactive Ion Etching (RIE) plasma-based dry etching system was used for etching the ARC layer (Figure 4.2c). The RIE metal etcher system was used to etch Al (Figure 4.2d). In this step, a laser endpoint system that was connected to RIE was used to minimize the exposure of the platinum. In order to clean the photoresist on the top, acetone was used and a four minute RIE process was applied to clean the rest of the ARC by oxygen plasma. The final schematic of the device is shown in Figure 4.2e.

4.2.2 Cr/Al_2O_3/Cr MIM Diode

A layer of negative photoresist was coated on a silicon dioxide substrate (Figure 4.3a). Next, the photoresist was exposed with UV light by using Mask A (Figure 4.1a) as illustrated in Figure 4.3b. After developing the sample, 50 nm Cr was deposited on the sample as shown in Figures 4.3c and 4.3d. After the deposition, the lift-off process was done to remove un-

patterned areas of the chromium (Figure 4.3e) and then, the second photolithography process (photoresist coating, UV exposing, and developing) was done in order to deposit the second layer of the MIM diode by using Mask B (Figure 4.1b). The schematic illustration of the sample is shown in Figure 4.3f after the developing of the sample. 4 nm Al_2O_3 and then 60 nm Cr as a second layer were deposited onto the sample using e-beam evaporation (Figure 4.3g). Finally, the lift-off process was completed to remove the un-patterned areas of the diode (Figure 4.3h).

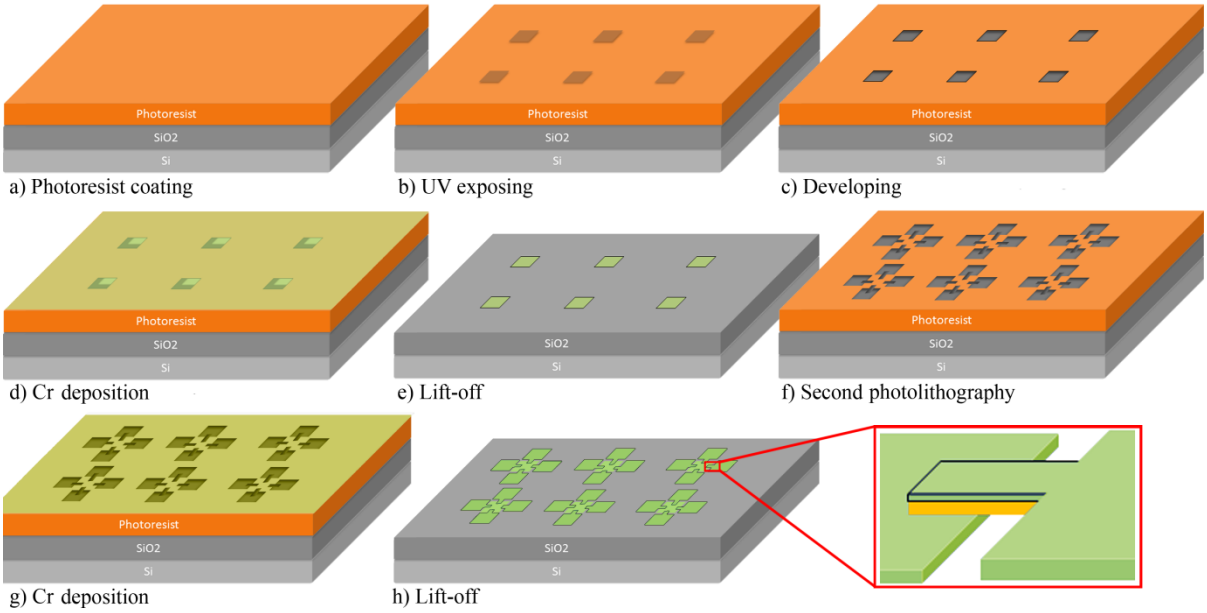

Figure 4.3: Fabrication steps of $Cr/Al_2O_3/Cr$ MIM diode

Chapter 5
Multi Insulator MIM Diodes

High asymmetry is achieved when the difference between the work functions of the metals of the MIM diode is large. High nonlinearity is achieved when the barrier heights at metal-insulator interfaces are high and the insulator layer is thick. Both high non-linearity and high asymmetry cannot be achieved by a single insulator layer in MIM diodes [13]. MIM diodes with double insulator layers can overcome this issue [13]. The barrier height value at each interface plays the key role regarding the tunneling efficiency, asymmetry and non-linearity in MIM diodes. If there is only one insulator used, there will be two different potential barrier values which are between the metal 1 and the insulator, and metal 2 and the insulator. These two interfaces determine the turn on and breakdown voltages depending on the work functions of the metals. If there are two insulators, there will be three different barrier height values. If the order of the insulators is changed, the I-V characteristics will also be changed due to the change in barrier height at each interface. I fabricated and tested MIM diodes with double insulator layers, metal-insulator-insulator-metal (MI^2M), and with quadra insulator layers, metal-insulator-insulator-insulator-insulator-metal (MI^4M), in order to observe the impact of the number of the insulators in a MIM diode.

5.1 Fabrication of $Cr/TiO_2/Al_2O_3/Ti$ and $Cr/TiO_2/Al_2O_3/TiO_2/Al_2O_3/Ti$ MIM Diodes

The MI^2M diode's bottom metal, M_1, Chromium (Cr), and the top metal, M_2, Titanium (Ti), were chosen based on their work functions. The insulator layers, TiO_2 (I_1) and Al_2O_3 (I_2), were preferred due to the difference in the electron affinity. First, a photolithography step

was taken using a negative photoresist with Mask B (Figure 4.1b) to make lift-off possible. Then, 60 nm thick Cr was deposited onto the substrate by e-beam evaporation. Next, the un-patterned areas of the sample lifted-off. 34 cycles of the TiO_2 and 14 cycles of the Al_2O_3 were deposited by ALD onto the substrate. The measured deposition rates of the atomic layer deposited Al_2O_3 and TiO_2 were 0.105 ± 0.001 nm/cycle and 0.0437 ± 0.001 nm/cycle, respectively. The total thickness of the insulator layer in MI^2M diode was approximately 3 nm thick, and each single insulator layer was approximately 1.5 nm thick. After a second photolithography process by a negative photoresist with Mask A (Figure 4.1a), 100 nm thick Ti was deposited by e-beam evaporation. After a lift-off process, Argon (Ar) Reactive Ion Etching (RIE) was applied to remove the oxide layers onto the M_1. Figure 5.1 represents the schematic diagram of the fabricated $Cr/TiO_2/Al_2O_3/Ti$ (MI^2M) diode.

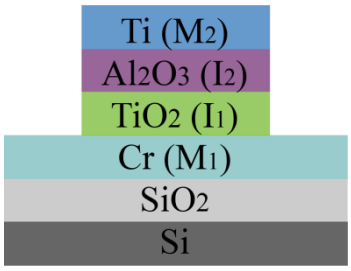

Figure 5.1: A schematic diagram of the MI^2M diode

For the MI^4M diode, the same bottom and top metals have been chosen to make a possible comparison of the impact of the insulator layers. Similarly, 60 nm thick Cr was deposited onto the substrate by e-beam evaporation after the photolithography process by a negative photoresist with Mask B (Figure 4.1b). After the deposition, the lift-off process was completed to remove the remaining photoresist with un-patterned Cr film. Next, 17 cycles of the TiO_2, 7 cycles of the Al_2O_3, 17 cycles of the TiO_2, 7 cycles of the Al_2O_3 respectively were

deposited by ALD. Therefore, in MI^4M, each insulator layer is approximately 0.75 nm thick, and the total thickness of the insulator layer in the MI^4M diode is approximately 3 nm which is the same value with the MI^2M diode. And then, 100 nm thick Ti was deposited by e-beam evaporation after the second photolithography process by the same negative photoresist with Mask A (Figure 4.1a). At the end, the oxide layers on the Cr were etched by Ar RIE after the second lift-off process. A schematic diagram of the fabricated Cr /TiO_2/Al_2O_3/TiO_2/Al_2O_3/Ti (MI^4M) diode is shown in Figure 5.2.

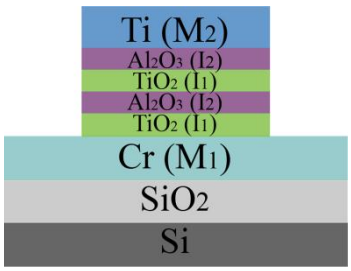

Figure 5.2: A schematic diagram of the MI^4M diode

I repeated the same insulators of the MI^2M diode for the MI^4M diode by keeping the total thickness of the insulator layer the same to observe the impact of the number of the insulators. There are three different interfaces between the two metals in MI^2M. Each interface has a different potential barrier value. Without applying any voltage, the energy band diagram of the MI^2M diode is presented in Figure 5.3a. The shape of the energy band diagram is determined by the work functions and the electron affinities. The electron affinity of the insulators changes according to the thickness [28] or deposition technique. The electron affinities of the 1.5 nm thick ALD deposited TiO_2 and 1.5 nm thick ALD deposited Al_2O_3 are 3.9 eV (χ_1) and 2.8 eV (χ_2), respectively. The work function of the Cr is 4.5 eV (φ_1), and that of Ti is 4.33 eV (φ_2). In this case, the barrier heights are $\Phi_1 = \varphi_1 - \chi_1 = 0.6$ eV,

$\Phi_2 = \chi_1 - \chi_2 = 1.1$ eV, and $\Phi_3 = \varphi_2 - \chi_2 = 1.53$ eV. The shape of the energy band diagram also changes by applying a bias to one of the metals. When a negative bias is applied to the Ti, the probability of an electron to tunnel from Ti to Cr becomes higher than Cr to Ti (Figure 5.3b). The tunneling probability of an electron to tunnel from Cr to Ti becomes greater than from Ti to Cr when a positive bias is applied to the Ti (Figure 5.3c).

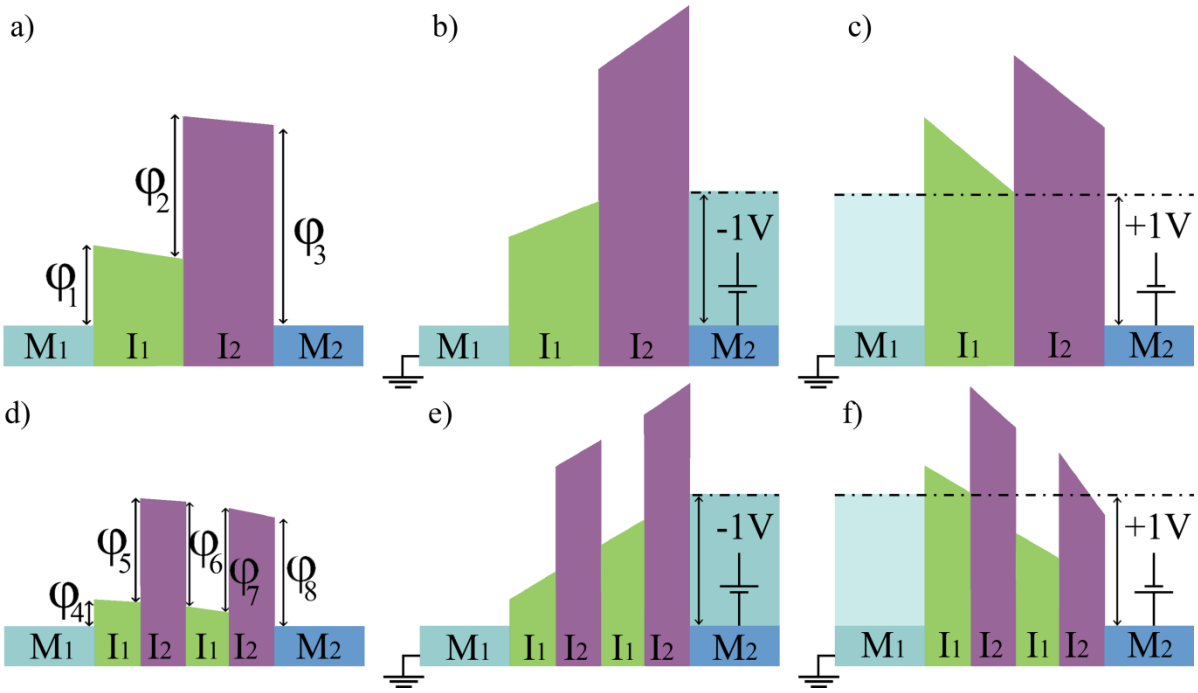

Figure 5.3: Energy band diagram of the MI^2M diode: a) no bias applied; b) negative; c) positive bias applied to Ti. Energy band diagram of the MI^4M diode: d) no bias applied; e) negative; f) positive bias applied to Ti.

In Figure 5.2, a schematic diagram of the MI^4M diode is illustrated. There are five potential barrier interfaces between the Cr and Ti. Under the zero bias, the energy band diagram of the MI^4M diode behaves as shown in Figure 5.3d. The electron affinity of ALD deposited 0.75 nm thick TiO_2 and ALD deposited 0.75 nm thick Al_2O_3 are 4.3 eV (χ_3) and

3.5 eV (χ_4), respectively. In this case the barrier heights are $\Phi_4 = \varphi_1 - \chi_3 = 0.2$ eV, $\Phi_5 = \Phi_6 = \Phi_7 = \chi_3 - \chi_4 = 0.8$ eV, and $\Phi_8 = \varphi_2 - \chi_4 = 0.83$ eV. The shape of the energy band diagram of the MI^4M diode becomes similar to Figure 5.3e when -1 Volt is applied to the Ti and as in Figure 5.3f when +1 Volt was applied to the Ti.

Under the -1 V, while a free electron at Ti is tunneling through the barriers, there is a 1.5 nm thick Al_2O_3 barrier, which has an energy level higher than +1 V in the MI^2M diode. Under the same bias, there are two layers of the 0.75 nm thick Al_2O_3, which have an energy level higher than +1 V in the MI^4M diode. In both cases, there will be a reverse current flow. However, the amplitude of the current is higher in a MI^2M diode than a MI^4M diode due to the tunneling distance. If the applied bias is +1 V to the Ti, the energy levels of the Al_2O_3 and TiO_2 are more than +1 V at the MI^2M diode. At the MI^4M diode, there are fewer barriers above +1 V, so the tunneling probability at the MI^4M diode is higher than at the MI^2M diode. Hence, at +1 V, the positive current density at the MI^4M diode is greater than the MI^2M diode. When Figures 5.3b and 5.3c are compared, under the same amplitude of the bias, the energy band diagram shows difference, which causes asymmetry in the MIM diodes. Similarly, in the MI^4M diode, the same effect is observed (Figures 5.3e and 5.3f).

Chapter 6
Results and Discussion

The fabricated diodes have been characterized by a Keithley 4200-SCS Semiconductor Characterization System that is connected with a probe station. The characterization system is illustrated in Figure 6.1.

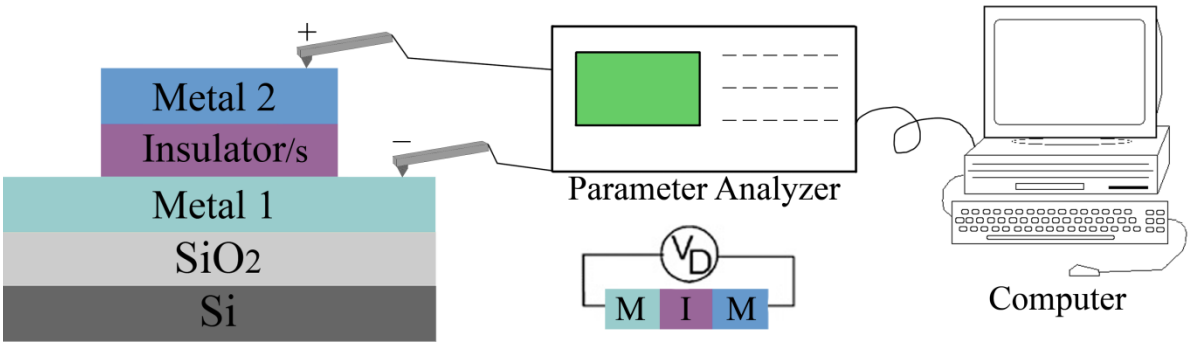

Figure 6.1: A schematic diagram of Semiconductor Characterization System

After the characterization, I-V, asymmetry and nonlinearity curves of the fabricated MIM diodes are plotted. In the following sections, all of these curves are stated.

6.1 $Pt/Al_2O_3/Al$ and $Cr/Al_2O_3/Cr$ MIM Diodes

The Platinum-Alumina-Aluminum ($Pt/Al_2O_3/Al$) MIM diode has been fabricated to achieve a high asymmetrical I-V curve and Chromium-Alumina-Chromium ($Cr/Al_2O_3/Cr$) MIM diode has been fabricated to observe a symmetrical I-V curve. A high difference in the work function of platinum and aluminum makes high asymmetry possible. The work functions of Pt and Al are 5.65 eV and 4.28 eV, respectively. However, a symmetrical I-V curve is expected since both metals of the MIM diode are the same for $Cr/Al_2O_3/Cr$.

The current was measured from -1 Volt to +1 Volt applied bias. As shown in Figure 6.2, the I-V curves of the $Cr/Al_2O_3/Cr$ and $Pt/Al_2O_3/Al$ MIM diodes show difference. At +1 Volt, the current reaches 4µA for $Pt/Al_2O_3/Al$ while $Cr/Al_2O_3/Cr$ the MIM diode has a 7 µA current. There is almost zero current for the $Pt/Al_2O_3/Al$ diode at -1 Volt while the $Cr/Al_2O_3/Cr$ diode reaches -7µA.

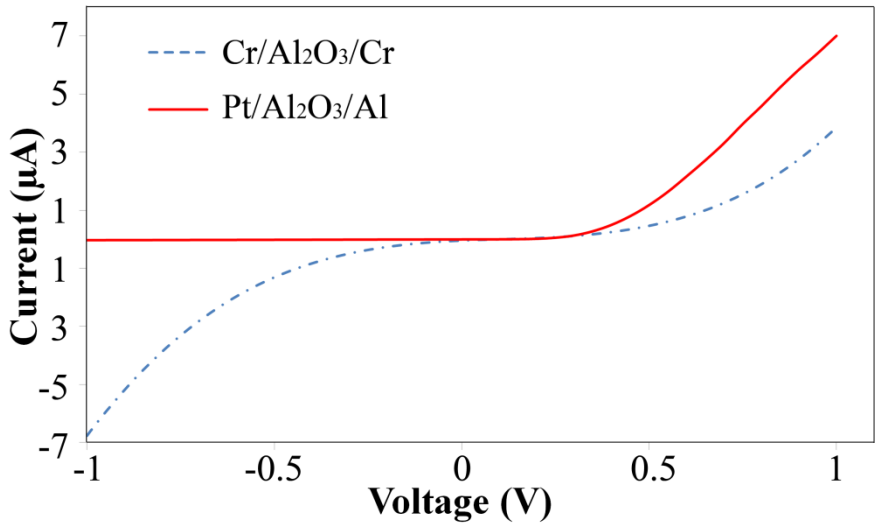

Figure 6.2: I-V curves of $Cr/Al_2O_3/Cr$ and $Pt/Al_2O_3/Al$ MIM diodes

The asymmetry value of a diode should be greater than 1 for rectification. As illustrated in Figure 6.3, the asymmetry value of the $Cr/Al_2O_3/Cr$ MIM diode is between the 0 and 1, which is not desired for a diode. However, the asymmetry of the $Pt/Al_2O_3/Al$ diode reaches 240 at +1 Volt. Therefore, it is illustrated that the asymmetry of MIM diodes highly depends on the work functions of the metals.

The asymmetry value of the $Cr/Al_2O_3/Cr$ MIM diode is not 1 as it can be seen in Figure 6.2. This is because a natural Cr_2O_3 oxide layer could be grown on Cr which makes another insulator layer. If this insulator layer is extremely thin, it slightly affects the result.

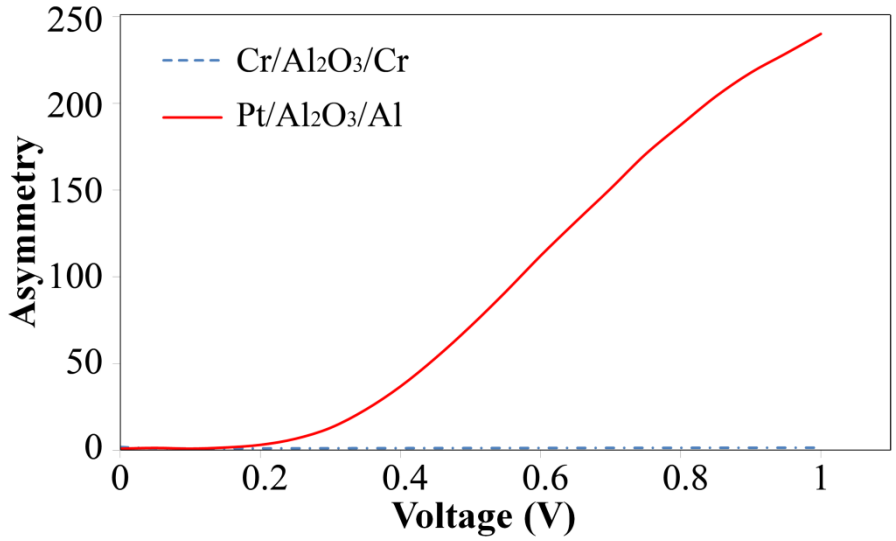

Figure 6.3: Asymmetry curves of $Cr/Al_2O_3/Cr$ and $Pt/Al_2O_3/Al$ MIM diodes

6.2 Cr/TiO2/Al2O3/Ti and Cr/TiO2/Al2O3/TiO2/Al2O3/Ti MIM Diodes

The results for the I-V curve, asymmetry and non-linearity of the $Cr/TiO_2/Al_2O_3/Ti$ (MI^2M)

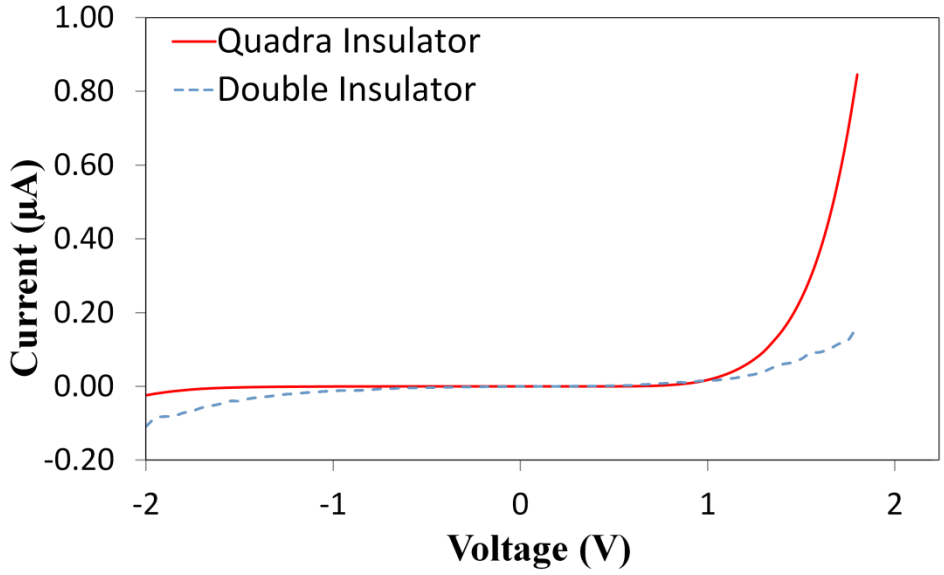

Figure 6.4: I-V curve of MI^2M and MI^4M diodes

and $Cr/TiO_2/Al_2O_3/TiO_2/Al_2O_3/Ti$ (MI^4M) diodes are shown in Figure 6.4, 6.5 and 6.6,

respectively.

The MI^2M diode has more current than the MI^4M diode below -1 V (Figure 6.4), which agrees with the energy band diagram model (Figures 5.3b and 5.3e). This means the MI^2M diode has less breakdown voltage than the MI^4M diode. Similarly, due to the shape of the energy band diagram (Figures 5.3c and 5.3f), the MI^4M diode has more current than the MI^2M diode above +1 V. At +1.8 V, the current at MI^2M is 0.17 µA, and the current at MI^4M is 0.85 µA, so the MI^4M diode also has better turn-on voltage which is illustrated in Figure 6.4.

A figure of merit that is necessary for a diode to rectify is asymmetry value which is approximately 3 at +1.6 V for the MI^2M diode. However, the asymmetry value is approximately 90 at the same applied voltage for the MI^4M diode, which is 30 times greater than the MI^2M diode's (Figure 6.5).

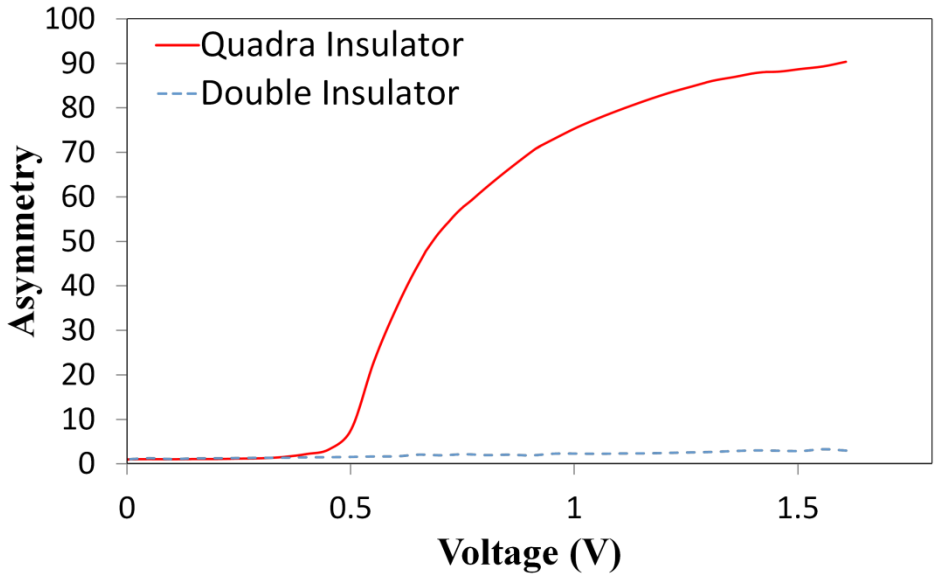

Figure 6.5: Asymmetry of MI^2M and MI^4M diodes

The nonlinearity of the MI^4M diode is also higher than the MI^2M diode from +0.4 V to +2 V as seen in Figure 6.6. Hence, it is proven that the MI^4M diode is superior to the MI^2M diode although the total thickness of the insulator layers and the type of the materials are the same.

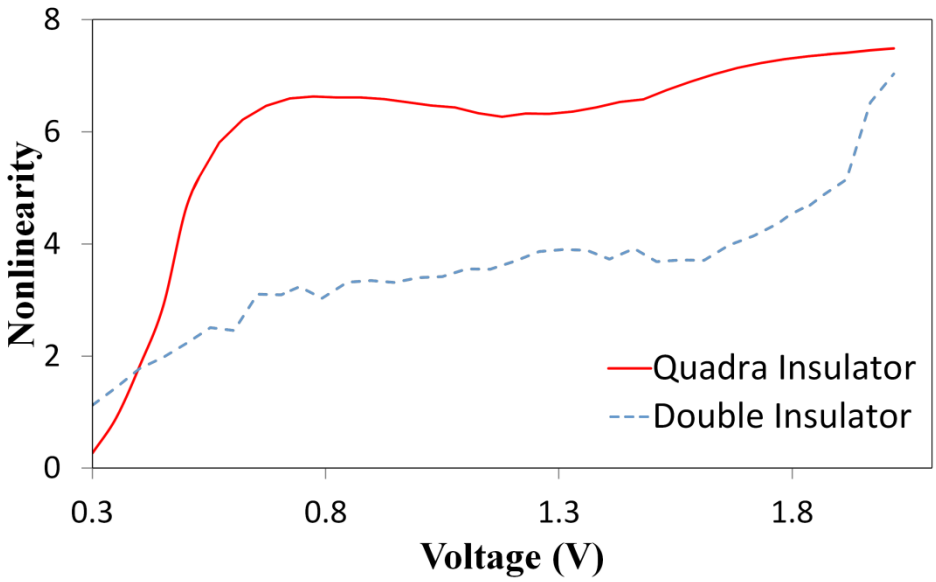

Figure 6.6: Nonlinearity of MI^2M and MI^4M diodes

Chapter 7
Conclusion and Future Work

In classic mechanics, a particle cannot pass behind a potential barrier if the energy of the particle is lower than the potential barrier. In quantum mechanics, a particle has a probability to pass the potential barrier, and this passing probability is called tunneling. The MIM diodes' working principle can be explained with quantum mechanics. The work functions of metals and the thickness of the insulators determine the tunneling probability. The current density is highly dependent on the tunneling probability as is mentioned in chapter 2.

There are some parameters that should be considered before fabricating an MIM diode which are: material type; thickness of the insulator layer; junction area; capacitance; and permittivity. In this work, I focused on different materials to illustrate their impact on I-V curve, asymmetry and nonlinearity. The Cr/Al_2O_3/Cr MIM diode showed a symmetrical I-V curve because the insulator layer is sandwiched between the same metals which cause the current flow to be the same in both forward and reverse directions. The Pt/Al_2O_3/Al MIM diode has a highly asymmetrical I-V curve due to the difference in work functions of the Pt and Al.

In addition to the Cr/Al_2O_3/Cr and Pt/Al_2O_3/Al MIM diodes, the Cr/TiO2/Al2O3/Ti and Cr/TiO2/Al2O3/TiO2/Al2O3/Ti MIM diodes have been fabricated to have both high asymmetry and nonlinearity. To my knowledge, a MIM diode with four insulator layers was fabricated for the first time. I proved that a metal-insulator-insulator-insulator-insulator-metal diode has better performance than a metal-insulator-insulator-metal diode when the I-V curve, asymmetry and nonlinearity characteristics are compared. At 1.6 volt applied voltage,

the asymmetry value is approximately 3 for the MI^2M diode and it is approximately 90 for the MI^4M diode, which is 30 times greater than the MI^2M diode's. Because of the unique feature of the ALD, I was able to deposit extremely thin insulator layers. As future work, a MIM diode with more than four insulator layers is projected by repeating two different insulators.

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Publication List

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F. Aydinoglu, M. Alhazmi, B. Cui, O. M. Ramahi, M. Yavuz, "Higher Performance Metal-Insulator-Metal Diodes using Multiple Insulator Layers" *Applied Physics Letters* (under review, Sep 2013).