# CMOS Transimpedance Amplifier for Biosensor Signal Acquisition

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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# Abstract

A 1-G$\Omega$ CMOS transimpedance amplifier (TIA) suitable for processing sub-nA-level currents in electrochemical biosensor signal-acquisition circuits is presented. Use of a two-stage active transconductor provides resistive feedback in place of a large-area linear resistor. The TIA feedback loop is engineered to suppress output offset caused by DC input leakage currents of $\pm 0.9$ nA. A mechanism to tune the low-frequency cutoff of the TIA from 0.7 Hz to 500 Hz is implemented which permits operation under variable environmental conditions. Simulated and experimental results from a custom TIA fabricated in a 3.3-V 0.35-$\mu$m CMOS process are presented.

# Acknowledgements

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Finally, I am indebted to my parents for their unconditional support in my endeavours. This thesis would not have been possible without them.

# Dedication

This thesis is dedicated to the kids and youth at St. Mary's Coptic Orthodox Church in Kitchener.

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# Chapter 1

# Introduction

Transimpedance amplifiers (TIAs) are integral components of complementary metal-oxide-semiconductor (CMOS) integrated low-current measurement systems. Resistor and capacitor-based TIAs for processing nA-level currents and below have found numerous applications in CMOS electrochemical biosensors, including patch-clamp electrophysiology chips [1][2], integrated nanopore and ion channel sensors [3][4][5], and on-chip electrochemical DNA sensor arrays [6][7].

Patch clamp electrophysiology is a technique used to measure the current that flows through a cell membrane which has applications in drug discovery and research for pharmaceutical development [2]. Ion channels along the cell membrane control the flow of ions in and out of the cell which gives rise to a current. Ion channels are categorized by the way in which they are gated, that is, ion channels are open or closed by different mechanisms. Voltage-gated ion channels react to changes in the membrane potential while ligand-gated channels are open or blocked in response to binding chemical messengers [8]. A single ion channel generates a short current pulse while the sum of multiple ion channels can produce larger pulses as shown in Figure 1.1. These transient signal currents generated by the flow

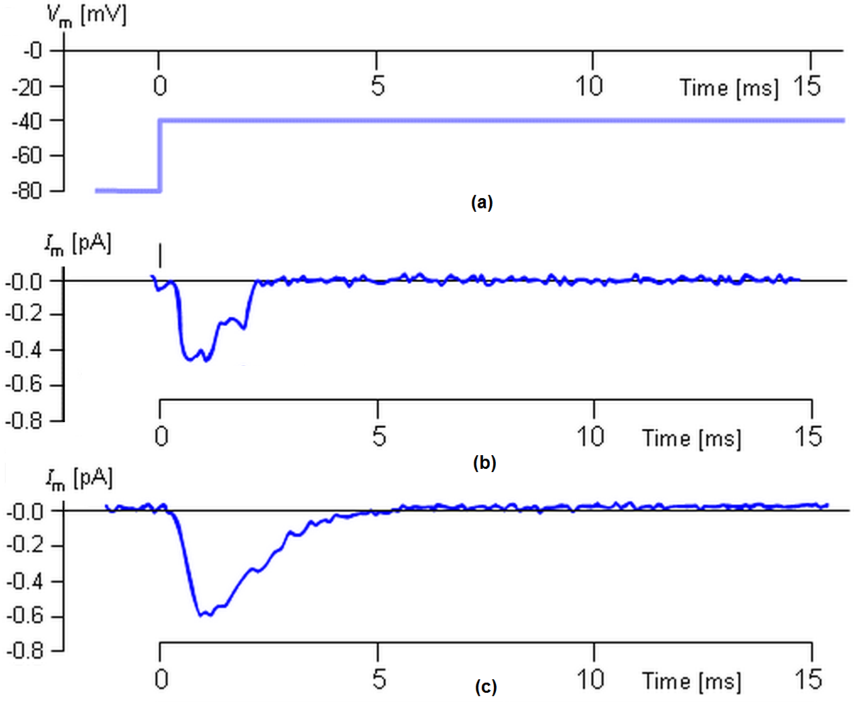


Figure 1.1: Gating in single sodium channels: Patch clamp recording of unitary Na currents in a toe muscle of adult mouse. (a) Applied voltage step from -80 to -40 mV. Ion channels are closed prior to initial voltage step. (b) Current transient response for a single patch containing over 10 sodium channels. (c) The ensemble mean of 352 repetitions of the single patch current [9][10].

of ions are in the pA to nA range and require a typical recording bandwidth ranging from 1 Hz to 10 kHz [11].

Electrophysiologists are interested in measuring the amplitude, duration and frequency of the current pulses generated by ion channels to determine the effects of foreign substances and/or pharmaceutical compounds. Additionally, patch clamp is a primary tool in the study of genetic disorders which disrupt normal functioning ion channels such as cystic fibrosis, fibromyalgia, and epilepsy [12][13][14].

Figure 1.2(a) shows a traditional patch clamp system. The cell of interest lies within an electrolyte that is biased to a reference voltage. A micro-pipette with an embedded electrode is clamped over a single ion channel and is connected to the TIA. Small currents flow through the large feedback resistor in the TIA to develop an output voltage.

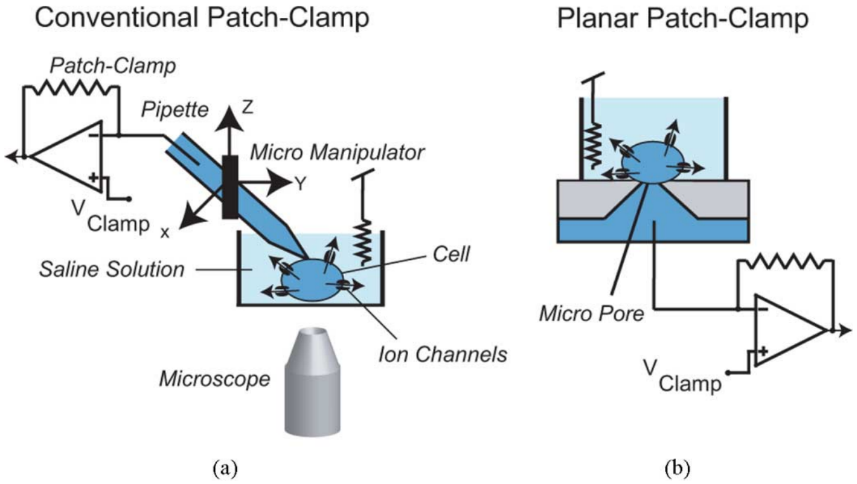

Conventional Patch-Clamp
Patch-Clamp
Pipette
Z
Micro Manipulator
Y
x
V
Clamp
Cell
Saline Solution
Ion Channels
Microscope
(a)
Planar Patch-Clamp
Micro Pore
V
Clamp
(b)

Figure 1.2: (a) Conventional whole-cell patch clamp recording using discrete TIA. A skilled technician uses pipette and micromanipulator to probe the cell. (b) Planar patch clamp system where the pipette electrode is replaced with a CMOS micro-pore electrode. Cells adhere to the aperture using suction. TIA is also integrated in CMOS [1].

Patch clamp systems on chip can be realized by implementing the TIA in a CMOS process. Conventional patch clamping is a labour intensive process is carried out by skilled technicians with the use of micro-pipette to probe the cell membrane and as a result it is a costly and slow process [15]. However, a planar patch clamp system can be developed using CMOS electrodes as shown in Figure 1.2(b) [16]. By integrating the signal acquisition circuitry (TIA and any proceeding stages) with the electrode in CMOS, large arrays of biosensor systems can be developed to reduce costs and increase measurement throughput.

A second application of TIAs for biosensor signal acquisition is in impedance spectroscopy. This is a small-signal technique which involves applying an AC voltage to a biochemical specimen over a range of frequencies while measuring the resulting ac current. Using these quantities, changes in the electrical impedance can be related to physiological changes in the specimen [17].

Figure 1.3 shows a typical electrochemical biosensor signal acquisition system consisting of an electrochemical interface and signal acquisition circuit. The interface is represented by an electrical model of the working electrode, electrolyte which sustains the biochemical reaction of interest, and test specimen [18]. The biochemical reaction or specimen is modeled with the current source $i_s$ which represents the input signal of interest along with parallel resistance and capacitance $R_p$ and $C_p$ respectively which, in the case of patch clamp, models the cell membrane. $R_{WE}$ and $C_{WE}$ represent the impedance of the interface between the biochemical reaction site and working electrode. While the TIA drives the working electrode to virtual ground, $V_{GND}$, a secondary voltage source, $V_{REF}$, is required to bias the electrolyte in order to establish a potential difference between the electrolyte and the working electrode. As a result of the applied potential, freely moving ions readily available in the electrolyte interact with the working electrode and give rise to a standing (DC) current applied to the TIA. This current leakage between the electrolyte and the electrode is illustrated by the signal path from $V_{REF}$ through $R_p$ and $R_{WE}$.

DC currents may be inherent to the signal source $i_s$. For example, in whole-cell patch clamp applications, the total current measured through the cell membrane is a result of the cumulative effect of hundreds of ion channels opening and closing [19]. Each type of ion channel is responsible for regulating the concentration of a particular ion on either side of

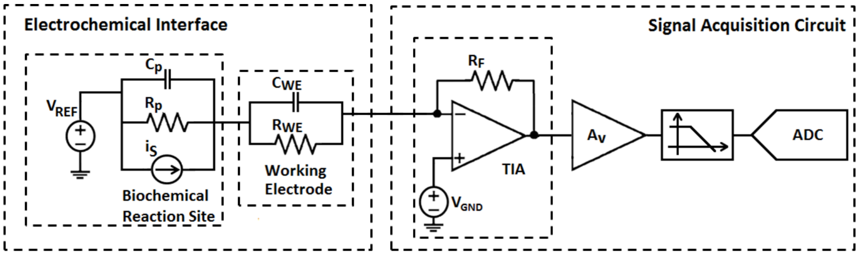


Figure 1.3: Block diagram for a typical electrochemical biosensor.

the cell membrane [20]. There exists passive ion channels which are continuously passing current through the cell membrane that gives rise to an average or DC leakage current on the order of nA [21][22].

In the biosensor signal acquisition circuit shown in Figure 1.3, the TIA holds the working electrode at virtual ground and converts the bidirectional input signal current $i_{in}$ to an amplified voltage. The TIA may be followed by additional gain stages, filters, and an analog-to-digital converter (ADC) to enable further gain and signal processing. Each additional stage injects noise into the system until the measured signal is digitized, at which point it is essentially immune to noise. The TIA must provide high gain to reduce input-referred noise so that an adequate signal-to-noise ratio (SNR) can be achieved.

A desirable function of the TIA is to prevent the passage of large offset voltage caused by DC input current produced by the biochemical process under investigation and external low-frequency interference. Output offset voltage can saturate subsequent amplification stages of the acquisition circuit, reducing the dynamic range of the measurement system. While AC coupling subsequent stages can prevent saturation, integration of large DC-blocking capacitors may be impractical in some applications due to chip area constraints. To combat this issue, a CMOS integrator-differentiator-based TIA with a continuous-time capacitor reset network for impedance spectroscopy has previously been reported which prevents saturation of the first-stage integrator [23]. In addition, a TIA constructed from discrete components for semiconductor radiation detection has been reported which uses a proportional-integral control amplifier in the feedback path to zero the DC level of the TIA output [24].

This thesis presents a 1-GΩ CMOS resistive-feedback TIA with adjustable low-frequency cutoff. The proposed design is intended for use in electrochemical impedance spectroscopy (EIS) biosensor applications to record nA-level AC currents in the 1-Hz to 1-kHz range. Unlike [24], this TIA is amenable to CMOS integration because a two-stage op-amp-based transconductor [25] is integrated in the feedback path to achieve 1-GΩ transimpedance. Use of a single linear resistor to achieve such high gain would consume excessive chip area.

While [23] and [24] are effective in reducing TIA output offset, no mechanism is provided to adjust the low-frequency cutoff in order to adapt to changes in input-signal bandwidth or measurement conditions. However, frequency tuning is supported in the proposed design by adjusting a MOS active resistor through gate-voltage control within the TIA feedback loop. The ability to dynamically adjust the low-frequency cutoff is unique to this design and has several applications in biosensor signal acquisition systems. For patch clamp applications, bandwidth tuning allows for selective measurement of the membrane current by filtering out the effects of passive and other high-conductance ion channels. Additionally, interference can be filtered out, such as 60 Hz line interference that may couple to the electrolyte potential or the TIA bias.

## 1.1 Outline

This thesis is structured as follows: Chapter 2 reviews several TIA architectures and provides background on design considerations and constraints. Popular techniques for current to voltage amplification are also discussed. Chapter 3 builds upon the TIAs discussed in Chapter 2 and other system-level design decisions to present a unique TIA architecture. Circuit design and implementation details of the TIA are discussed in Chapter 4. In Chapter 5, the experimental results from the proposed TIA implemented in a five-metal, double-poly, 0.35-$\mu$m CMOS process are presented. Chapter 6 concludes the thesis and discusses improvements to the chip design and future work.

# Chapter 2

# Review of Transimpedance Amplifiers

TIAs are generally used as the first stage of low-current sensor interfaces like the one shown in Figure 1.3. The TIA is designed to provide sufficient gain so that the input signal is within the input range of the ADC after passing through subsequent gain and filtering stages. The TIA must contribute minimal noise since the first stage of any signal acquisition system has the greatest effect on the SNR [26].

As discussed in Chapter 1, the DC offset at the TIA output must be reduced to prevent saturation of the following stages of the acquisition channel. The input signals for the applications described in Chapter 1 consist of a standing (DC) current $I_{IN}$ and an AC signal current of interest $i_{in}$. In this thesis, $I_{IN}$ is defined for signal currents below 100 Hz while $i_{in}$ represents signal currents above 100 Hz. With respect to TIAs, $I_{IN}$ and $i_{in}$ stimulate the system to produce DC and AC signal voltages $V_{OUT}$ and $v_{out}$, respectively.

This chapter provides background information on TIAs. Sections 2.1 and 2.2 review classical TIAs with resistive feedback and capacitive feedback, respectively. Sections 2.3 and 2.4 comprise a short literature review of two additional TIA architectures that inspired the work of this thesis.

## 2.1 Resistor-Feedback Transimpedance Amplifier

A conventional resistor-feedback TIA (RTIA) is shown in Figure 2.1 where input signal current $i_{IN}$ flows through resistor $R_f$ in the feedback path, providing an output voltage $v_{OUT}$. The operational amplifier (op amp) input resistance is assumed to be large enough such that any input bias current drawn by the op amp is several orders of magnitude less than the input current. The transfer function of the TIA is given by

$$\frac{v_{OUT}}{i_{IN}}(s) = -\frac{A(s)}{1+A(s)}\frac{R_f}{1+sR_fC_p}, \tag{2.1}$$

where $A(s)$ is the op amp open-loop frequency response and $C_p$ is the parasitic capacitance that exists between the inverting input and output. Capacitance $C_p$ can limit the bandwidth of the TIA as suggested by the equation above. For DC input signals, the transimpedance becomes $V_{OUT}/I_{IN} \approx -R_f$.

### 2.1.1 Gain and Bandwidth

To obtain further insight into the frequency response of the TIA in Figure 2.1, $A(s)$ is modeled with a single-pole roll-off:

$$A(s) = \frac{A_0}{1+s/\omega_0}, \tag{2.2}$$

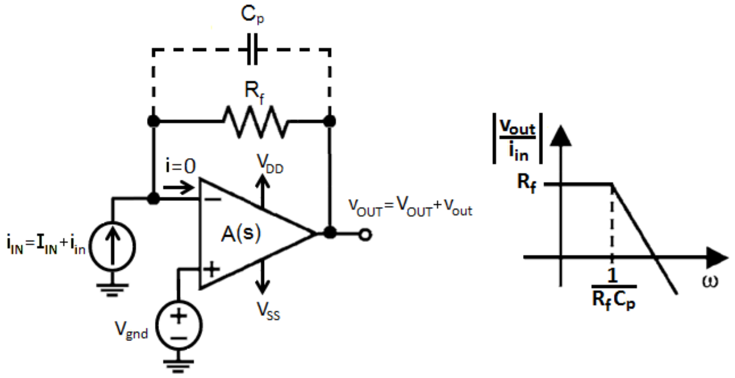


Figure 2.1: Transimpedance amplifier with linear feedback resistor.

where $A_0$ is the open-loop DC gain of the op amp and $\omega_0$ is the -3-dB cutoff frequency. Eq. (3.2) can be rewritten as

$$\frac{v_{OUT}}{i_{IN}} \approx -\frac{A_0}{1+A_0}\frac{R_f}{[1+s/(A_0\omega_0)][1+sR_fC_p]}, \tag{2.3}$$

where $A_0\omega_0$ is the gain-bandwidth product (GBP) of the op amp.

As evident from the denominator of Eq. (2.3), the pole frequencies, $f_{p_1}$ and $f_{p_2}$ (in Hz) of the TIA with resistive feedback are given by

$$f_{p_1} = \frac{1}{2\pi\omega_0 A_0} \text{ and } f_{p_2} = \frac{1}{2\pi R_f C_p}. \tag{2.4}$$

The dominant pole is dependent on the choice of components. If the GBP of the op amp is sufficiently large, which is usually the case, $f_{p_2}$ is lower than $f_{p_1}$ and the 3-dB bandwidth is determined by the choice of $R_f$ and parasitic capacitance $C_p$.

Here the tradeoff between gain and bandwidth is apparent. Increasing $R_f$ will increase the transimpedance of the TIA at the expense of reduced bandwidth. In the case of a discrete component implementation, $C_p$ is mostly a result of the resistor package, circuit board parasitics, and the op amp.

### 2.1.2 Output Voltage Saturation

The non-inverting terminal of the TIA in Figure 2.1 is connected to a constant virtual ground voltage $V_{GND}$ which is often set midway between the op amp power supply rails $V_{DD}$ and $V_{SS}$. If the input current has a zero DC component, then there is no DC voltage drop across $R_f$ and the output voltage node is set to the mid-rail voltage. In this way, signal currents are provided with maximum headroom, assuming the output swing of the op amp is symmetric about zero. However, when a positive DC input current $I_{IN}$ flows, then

$$V_{OUT} = -R_f I_{IN} + V_{GND}. \tag{2.5}$$

$V_{OUT}$ may saturate near $V_{SS}$ depending on the magnitude of $I_{IN}$ and the value of $R_f$. Likewise, $V_{OUT}$ may saturate at $V_{DD}$ when $I_{IN}$ becomes sufficiently negative. In either case, when $V_{OUT}$ has saturated, input signal currents will either be clipped or undetectable by the TIA.

### 2.1.3 Noise Performance

The main source of noise in the RTIA is the thermal noise generated by $R_f$ which is given by

$$\overline{i_{R_f}^2}(f) = \frac{4kT}{R_f}, \tag{2.6}$$

where $\overline{i_{R_f}^2}(f)$ is the current noise power spectral density (PSD) of resistor $R_f$, $k$ is Boltzmann's constant, and $T$ is the absolute temperature in Kelvin (K). Accordingly, the input-referred current noise PSD of the TIA is $\overline{i_{n,RTIA}^2}(f) = \overline{i_{R_f}^2}(f)$.

The spectrum of the noise produced by the resistor is shaped by the frequency response of the system. If the TIA is modeled as low-pass filter (LPF) with a single-pole roll off, the equivalent noise bandwidth $f_n$ [27] is given by

$$f_n = \frac{\pi}{2} f_{p_1}. \tag{2.7}$$

The total input-referred RMS current noise of the system, $\overline{i_{in,RTIA}}$, can now be calculated using

$$\overline{i_{n,RTIA}} = \frac{1}{R_f}\sqrt{\frac{kT}{C_p}}. \tag{2.8}$$

Since $C_p$ may be difficult to control, the total thermal noise can only be reduced by increasing $R_f$.

The input-referred noise of the op amp will also contribute to the total input current noise of the TIA. However, the op amp is usually designed to contribute much less noise than the thermal noise of $R_f$ [27].

The SNR of the RTIA (in dB) is given by

$$SNR_{RTIA} = 10\log_{10}\left[\frac{\overline{i_{in}^2}}{\overline{i_{n,RTIA}^2}}\right] = 10\log_{10}\left[\frac{P_{sig}R_f^2}{kT/C_p}\right], \tag{2.9}$$

where $\overline{i_{in}^2}$ is the input signal power and $\overline{i_n^2}$ is the total input-referred noise power due to $R_f$. Eq. (2.9) illustrates that increasing $R_f$ improves the SNR of the RTIA.

### 2.1.4 Design Tradeoffs

From the analysis above it is clear that the value of $R_f$ simultaneously sets the gain, 3-dB bandwidth, and noise of the circuit. At the same time, $R_f$ influences the amount of DC current the TIA can process while ensuring the output does not saturate. Reducing $R_f$ may increase the bandwidth and allow the TIA to sink more DC current, but this is only possible at the expense of reduced SNR. To keep $\overline{i_n^2}(f)$ at a level of fA$^2$/Hz for applications discussed in [1], [3], and [6], $R_f$ must be on the order of GΩ. While discrete resistor implementations are possible, fully-integrated solutions in CMOS would limit the value of $R_f$ to a few MΩ due to chip area constraints.

## 2.2 Capacitive Transimpedance Amplifier

A conventional capacitive (integrating) TIA (CTIA) consists of a capacitor in negative feedback with a parallel reset switch as shown in Figure 2.2. Similar to the RTIA, the virtual ground at the inverting op amp input ensures that charge is accumulated on $C_f$ due to the input current. This charge develops a voltage across $C_f$ such that $v_{out}$ is non-zero. Once the switch is closed, however, the terminals of $C_f$ are shorted which then reduces $v_{OUT}$ to zero.

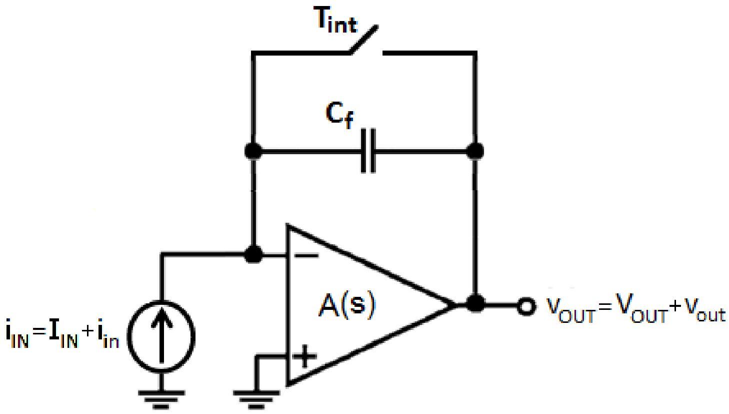


Figure 2.2: A conventional capacitive transimpedance amplifier with a parallel reset switch.

### 2.2.1 Gain and Bandwidth

Current is integrated onto $C_f$ until either the output voltage node saturates as a result of the limited output swing of the op amp, or the switch is closed and $C_f$ is shorted. Assuming that the input current begins to flow at time $t = 0$, the output voltage at the end of the integration period is given by

$$v_{OUT}(t) = -\frac{1}{C_f} \int_{0}^{T_{int}} i_{IN}(t)\,\mathrm{d}t, \tag{2.10}$$

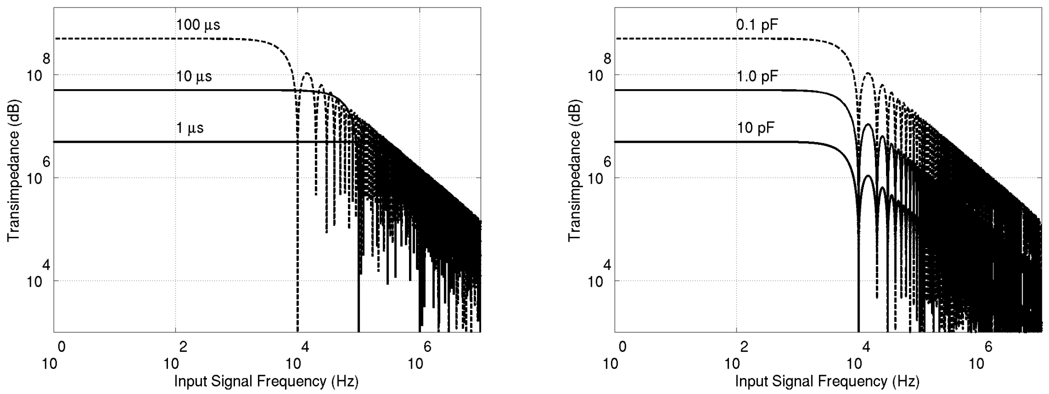
where $T_{int}$ is the integration time (i.e., the time between the opening and closing of the switch). Modeling the op amp in Figure 2.2 with a finite gain and bandwidth as before, and applying the Laplace transform to Eq. (2.10), the CTIA transfer function is given by

$$\frac{v_{OUT}}{i_{IN}}(s) = -\frac{A(s)}{1 + A(s)} \frac{1}{sC_f}(1 - e^{-sT_{int}}), \tag{2.11}$$

Substituting $s = j\omega$, applying Euler's formula, and taking the magnitude yields

$$\left|\frac{v_{OUT}}{i_{IN}}(j\omega)\right| = \left|\frac{A(j\omega)}{1 + A(j\omega)}\right| \frac{T_{int}}{C_f} \operatorname{sinc}(\pi f T_{int}), \tag{2.12}$$

where $\operatorname{sinc}(x) = \sin(x)/x$. For DC input signals, the transimpedance becomes $V_{OUT}/I_{IN} \approx T_{int}/C_f$. Figure 2.3 shows the magnitude of the transfer function in Eq. (2.12) for various values of $C_f$ and $T_{int}$. Given a fixed value of $C_f$, the gain can be adjusted by changing $T_{int}$. Since the transimpedance is proportional to $1/C_f$, high gain can be achieved using a small capacitor instead of a very large resistor as in the RTIA. As shown in Figure 2.3, the gain goes to zero when $f = (nT_{int})^{-1}$, where $n \geq 1$. The -3-dB bandwidth of the CTIA is approximated by $1/T_{int}$, assuming the GBP of the op amp is large.



(a) (b)

Figure 2.3: CTIA transfer function for (a) varying values of $T_{int}$ ($C_f = 100$ fF) and (b) varying values of $C_f$ ($T_{int} = 100\ \mu$s).

### 2.2.2 Output Voltage Saturation

As long as DC current flows through $C_f$, $V_{OUT}$ will continue to rise or fall until it saturates at one of the op amp supply rails. At this point, no more signal current can be integrated. In order to continue operating the CTIA, the switch must be closed in order to discharge $C_f$. This gives rise to a constraint on $T_{int}$. Considering only the DC component of the input current, Eq. (2.10) becomes $V_{OUT} = T_{int}/(I_{IN}C_f)$. It is evident that the amount of DC input current that the CTIA can sink or source depends on the value of $T_{int}$. If the virtual ground is set to $V_{DD}/2$, then the maximum current that the CTIA can process $I_{DC_{max}}$ without saturating the output is given by

$$I_{DC_{max}} = \left| \frac{V_{DD}C_f}{2T_{int}} \right| = \left| \frac{V_{DD}}{2} \left( \frac{T_{int}}{C_f} \right)^{-1} \right|. \tag{2.13}$$

As the equation shows, $I_{DC_{max}}$ is inversely proportional to the DC gain of the CTIA.

When the switch is closed and $C_f$ is discharged, no signal current can be integrated. As a result, a sample-and-hold circuit may be required at the output so that a measurement can be taken at the end of the integration phase.

### 2.2.3 Noise Performance

Although an ideal capacitor does not produce noise, it does accumulate noise generated by other sources. The parallel switch shown in Figure 2.2 is usually implemented using a MOS transistor having an on resistance and a finite off resistance. As a result, thermal noise from this device is integrated onto $C_f$ [28]. Flicker noise is also produced by a MOS switch, however its effect will be neglected in the following analysis for simplicity. Consequently, the MOS switch can be modeled as an ideal switch with a series on resistance as shown in Figure 2.4. Also for simplicity, the off resistance of the switch is assumed to be infinite. The effect of the op amp noise is neglected for the same reasons discussed in Section 2.1.3.

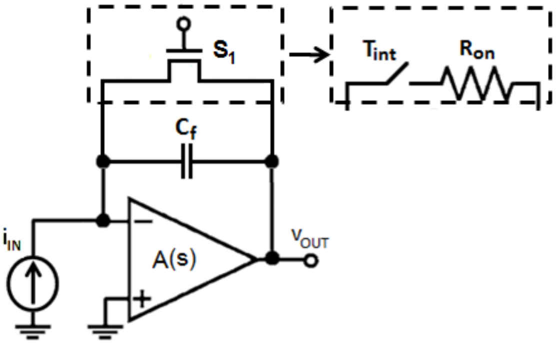


Figure 2.4: Parallel MOS reset switch in CTIA modeled as ideal switch with series on resistance $R_{on}$.

During the reset phase, switch $S1$ is closed and the on resistance of the switch $R_{on}$, appears in parallel with $C_f$. Since the input current is measured during the integration phase and not while the circuit is resetting, only the noise integrated onto $C_f$ will pass from the reset phase into the next integration period. Therefore, the thermal noise voltage PSD $\overline{v_{Ron}^2}(f)$ of $S1$ is given by

$$\overline{v_{ron}^2}(f) = 4kTR_{on}. \tag{2.14}$$

Assuming negligible decay over time $T_{int}$, $\overline{v_{out}^2} = \overline{v_{Ron}^2}$, where $\overline{v_{out}^2}$ is the output referred voltage noise at the end of the next integration period. To calculate the input-referred current noise PSD $\overline{i_{n,CITA}^2}(f)$, $\overline{v_{out}^2}(f)$ is divided by the squared magnitude of the DC gain of the CTIA, which is

$$\overline{i_{n,CTIA}^2}(f) = 4kTR_{on}\left|\frac{C_f}{T_{int}}\right|^2. \tag{2.15}$$

The RMS input current noise of the TIA can then be found using

$$\overline{i_{n,CTIA}} = \frac{C_f}{T_{int}}\sqrt{\frac{2\pi kTR_{on}}{T_{int}}}. \tag{2.16}$$

The input-referred SNR of the CTIA (in dB) is given by

$$SNR_{CTIA} = 10\log_{10}\left[\overline{i_{in}^2}\left(\frac{T_{int}}{C_f}\right)^2\frac{T_{int}}{2\pi kTR_{on}}\right], \tag{2.17}$$

where $P_{sig}$ is the input signal power. The equation above illustrates that increasing the DC gain $T_{int}/C_f$ improves the SNR of the capacitive feedback TIA.

### 2.2.4 Design Tradeoffs

The same tradeoff between gain and bandwidth exists with the CTIA as with the RTIA because $T_{int}$ is directly proportional to the DC gain and inversely proportional to the bandwidth. Decreasing the component value $C_f$ does provide some leeway for increased gain since it does not directly set the bandwidth. However, as before, there is also a trade off between the DC gain and the amount of DC current that the TIA can sink or source.

The CTIA is much more sensitive to DC currents than the RTIA. Even low DC currents over extended periods of time will, eventually, saturate the output since $C_f$ is continuously accumulating charge until the end of $T_{int}$ [29]. The input DC current thus limits how long a single continuous measurement can be taken. For example, for an input DC current on the order of nA and a minimum $C_f$ of 100 fF, the input current can only be measured for several hundred $\mu$s. Moreover, $T_{int}$ must be readjusted each time the DC current changes. For an RTIA, the DC current may give rise to a voltage offset at the output. However, the signal current can still be measured indefinitely as long as the output does not rail.

The primary advantage of using a CTIA is the reduced noise in comparison with the RTIA. If the DC gain for both architectures is equal, then $R_f = T_{int}/C_f$ and the total input-referred current noise of the CTIA will be less than that of the RTIA (assuming the op amp in each circuit is ideal). The current noise generated by $R_f$ is much more significant than the noise presented by $R_{on}$ of the parallel switch in the CTIA.

While minimizing $R_{on}$ improves the SNR, $R_{on}$ also determines the reset settling time of the CTIA. The time constant $\tau = R_{on}C_f$ should be established such that $5\tau \leq T_{rst}$, where $T_{rst}$ is the time allotted for the reset phase. After five time constants the voltage across $C_f$ will have reached 0.993% of its final value [27].

## 2.3 Resistive-Feedback Transimpedance Amplifier with Proportional-integrative Amplifier

A recurring problem with both the standard RTIA and CTIA is saturation of the output voltage due to the standing current $I_{DC}$. In order to address this issue, [24] invokes a discrete-component RTIA with Proportional-Integrative amplifier (RTIA-PI) as shown in Figure 2.5. The frequency response between the input current and the proportional-integrative (PI) amplifier output $V_{PI}$ is identical to that of the typical RTIA discussed in Section 2.1, that is $v_{PI}/i_{IN} = -R_f$. However, unlike the typical RTIA the, the PI amplifier zeroes the DC output voltage $V_{OUT}$ irrespective of $I_{DC}$.

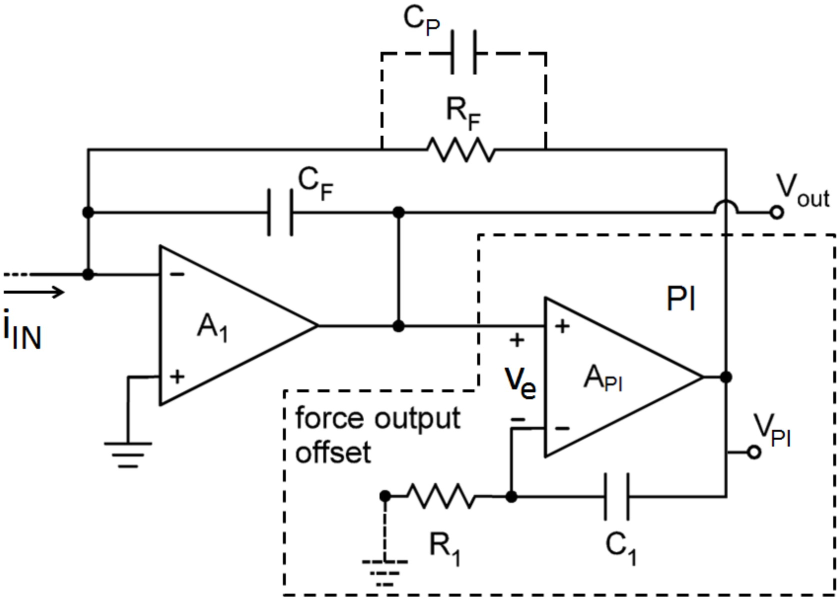


Figure 2.5: RTIA-PI circuit architecture (adapted from [30]). PI controller added in feedback loop to attenuate effects of input DC current at the output.

### 2.3.1 Gain and Bandwidth

Time constant $\tau_1 = R_1 C_1$ of the PI amplifier sets the low-frequency cutoff used to reduce the input effects of DC currents on output node $V_{out}$. The error voltage $v_e$ depicted across the terminals of amplifier $A_{PI}$ in Figure 2.5 is used to explain the frequency response of the system.

For input signal frequencies $f < 1/(2\pi\tau_1)$ no current passes through $C_1$ or $R_1$ and the error voltage $v_e = V_{OUT} - V_{GND}$. $A_{PI}$ drives $v_e$ to zero through the feedback loop consisting of $R_f$ and $A_1$ resulting in $V_{OUT} = V_{GND}$. The transimpedance for $f < 1/2\pi\tau_1$ is given by

$$\frac{v_{OUT}}{i_{IN}}(s) \approx -\frac{R_f}{A_{PI_0}}\frac{1 + s\tau_1 A_{PI_0}}{1 + s\tau_1}, \tag{2.18}$$

where $A_{PI_0}$ is the open-loop DC gain of $A_{PI}$. The PI amplifier has effectively injected a pole and zero into the system. For $f < 1/(2\pi\tau_1 A_{PI_0})$, $v_{OUT}/i_{IN} = R_f/A_{PI_0}$. For $1/(2\pi\tau_1 A_{PI_0}) < f < 1/(2\pi\tau_1)$ $v_{OUT}/i_{IN}$ rises at a rate of 20 dB/decade until it reaches $R_f$. For $f > 1/(2\pi\tau_1)$, current flows freely through $C_1$ and $v_e = V_{OUT} - V_{PI}$. Once again $A_{PI}$ drives $v_e$ to zero resulting in $V_{OUT} = V_{PI}$. At this point the frequency response is limited by the feedback capacitor $C_f$ and the transfer function is given by

$$\frac{v_{OUT}}{i_{IN}}(s) \approx -\frac{R_f}{1 + sR_f(C_f + C_p)}, \tag{2.19}$$

just as with the standard RTIA. The system operates as a bandpass filter with a passband transimpedance of $-R_f$. Since $V_{OUT} = V_{PI}$, $C_f$ and $C_p$ are effectively in parallel. The value of $C_f$ is selected to maintain stability of the overall system. The magnitude response of the RTIA-PI is shown in Figure 2.6.

Note that the RTIA-PI could also be viewed as a bandpass filter implemented using a single biquad stage [31].

### 2.3.2 Output Voltage Saturation

The RTIA-PI can process the same amount of current as that of the standard RTIA since $v_{PI}/i_{IN} = -R_f$. Although $V_{PI}$ is still prone to saturation as a result of input DC currents, $v_{OUT}$ does not saturate as long as $V_{PI}$ does not saturate. As shown by Eq. (2.18), input

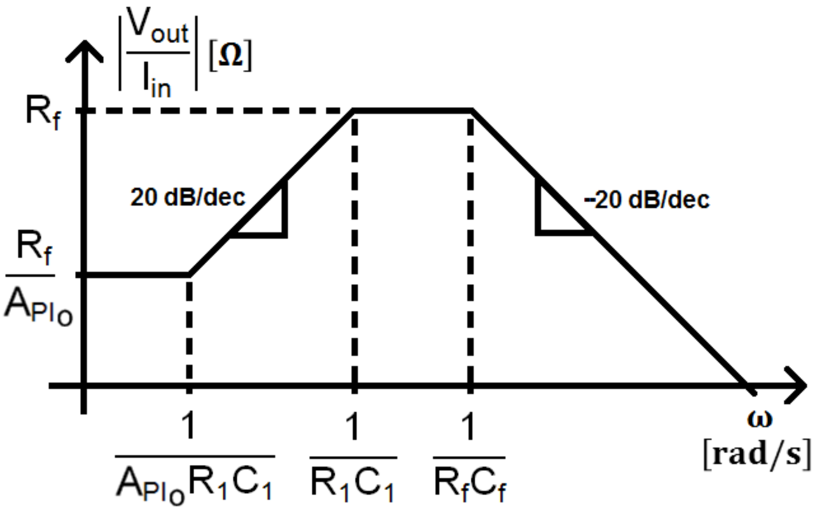


Figure 2.6: Frequency magnitude response of the resistive feedback TIA with PI controller shown in Figure 2.5.

currents at $f < 1/(2\pi\tau_1)$are amplified by a factor $R_f/A_{PI_0}$ at the output. As long as $A_{PI_0}$ is sufficiently high, the voltage offset at the output due to DC input current will be negligible.

### 2.3.3 Noise Performance

The primary contributor to the input-referred current noise is $R_f$ just as it was for the standard RTIA. However, the RTIA-PI architecture utilizes several additional components, including a second op amp and resistor $R_1$, which contribute additional noise. Therefore, the noise performance of the standard RTIA is marginally better.

### 2.3.4 Design Tradeoffs

The tradeoffs among gain, bandwidth, and SNR for the RTIA-PI are identical to those for the standard RTIA in Section 2.1.4. One additional tradeoff exists between the settling time and low-frequency cutoff since both are controlled by $\tau_1$. If $\tau_1$ is set to filter frequencies below 1 Hz, the RTIA-PI output voltage will take several seconds to settle. If the input current changes abruptly, signal measurements made before the system can settle may be clipped or distorted. It is possible to improve the settling time by adding a resistance in series with $C_1$, however this would reduce the passband transimpedance [24].

A large value of for $\tau_1$ can be achieved because $R_1$ and $C_1$ are implemented using discrete components. In a CMOS process, passive resistors are limited to MΩ and parallel-plate capacitors to pF which are not sufficient to set $\tau_1$. Therefore, the circuit presented in Figure 2.5 cannot be integrated on a CMOS chip due to the large chip area occupied by passive components.

## 2.4 Continuous Active Reset TIA

The continuous active reset TIA (CARTIA) presented in [23] uses resistive feedback to shunt DC input currents and capacitive feedback to amplify signal input currents. This requires a two-stage approach as shown in Figure 2.7. The first stage is an integrator consisting of feedback capacitor $C_i$ with an additional parallel feedback loop formed by resistor $R_{DC}$ and a voltage amplifier with transfer function $H(s) = v_B/v_A$, where $v_A$ and $v_B$ are the voltages at nodes A and B, respectively, in Figure 2.7. The latter feedback loop prevents $C_i$ from saturating due to the DC current, $I_{DC}$. In contrast with the standard CTIA which uses a parallel switch, $R_{DC}$ and $H(s)$ actively reset $C_i$ without disrupting the measurement period with an explicit reset phase.

The second stage of the CARTIA TIA is a differentiator with large coupling capacitor $C_d$ and feedback resistor $R_d$. The feedback capacitor $C_{fd}$ is used to set the 3-dB bandwidth of the overall system. $C_{fd}$ is usually a result of the parasitic capacitance across $R_d$.

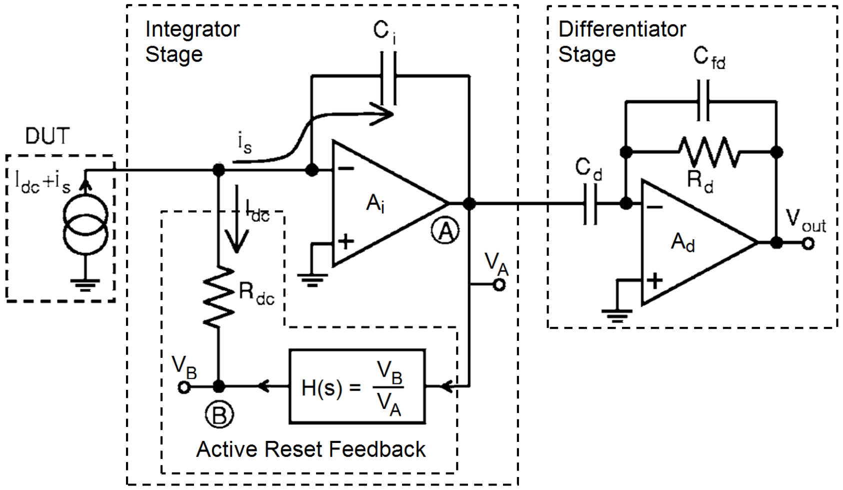

Integrator Stage
C i
Differentiator Stage
C fd
DUT
I dc+i s
i s
A i
I dc
R dc
A
V A
C d
R d
A d
V out
V B
H(s) = V B / V A
B
Active Reset Feedback

Figure 2.7: Continuous active reset TIA schematic (adapted from [30]). Consists of integrator stage similar to the RTIA-PI followed by a second differentiator stage.

### 2.4.1 Gain and Bandwidth

It is first necessary to consider $H(s)$ amplifier before analyzing the frequency response of the complete TIA. As depicted in Figure 2.8, $H(s)$ has a low-pass filter (LPF) response from node A to node B with a single-pole roll-off and a high-frequency zero $f_z$. The DC gain of $H(s)$ is made large so that the DC value of the integrator output $V_A$ in Figure 2.7 is kept regulated at the virtual ground voltage regardless of the input current. The attenuation at frequencies above $f_z$ ensures that the feedback loop composed of $R_{DC}$ and $H(s)$ is inactive for AC input currents so that the signal current $i_s$ passes through $C_i$ towards the output of the integrator. The frequency response of $H(s)$ is given by

$$H(s) = H_0 \frac{1 + s/\omega_H}{1 + sH_0\gamma/\omega_H}, \tag{2.20}$$

where $H_0$ is the open-loop DC gain of $H(s)$, $\gamma$ is the high-frequency attenuation factor (i.e., $1/\gamma << 1$), $\omega_H = 2\pi f_z = 2\pi\gamma f_p$. Effectively the $H(s)$ amplifier performs the same operation as the PI amplifier in the RTIA-PI, that is, DC currents are attenuated by a factor of $H_0$ at the output, while signal currents are allowed to propagate to the output through $R_{DC}$ with a gain of $\gamma R_{DC}$.

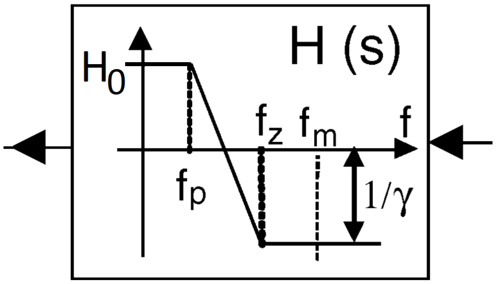


Figure 2.8: Magnitude response of the $H(s)$ amplifier within the integrator stage of the CARTIA in Figure 2.7 [23].

Assuming the integrator amplifier $A_i$ and $H(s)$ provide sufficiently high DC gain, the frequency response of the active reset integrator is given by

$$\frac{v_A}{i_{DC}}(s) \approx -\frac{R_{DC}}{H_0} \frac{[1 + sH_0\gamma/\omega_H]}{[1 + s\gamma/(A_{i_0}\omega_{i_0})][1 + sR_{DC}C_i\gamma][1 + s/\omega_H]}, \tag{2.21}$$

where $A_{i_0}\omega_{i_0}$ is the GBP of amplifier $A_i$. The above equation shows that the pole and zero of $H(s)$ are directly transferred to the zero and pole respectively of the overall integrator. The zero of the integrator lies at an extremely low-frequency as defined by $\omega_H/2\pi H_0\gamma$ as long as $H_0$ is large. The frequency $f_m$ defines the lowest signal frequency that is amplified by integrator stage and is given by

$$f_m = \frac{1}{2\pi R_{DC} C_i \gamma}. \tag{2.22}$$

Amplifier $H(s)$ is designed such that $\omega_H << \gamma R_{DC} C_i$ so that the frequency response shown in Figure 2.8 can be realized. In this way, the frequency response of the integrator stage is shaped as a bandpass filter as shown in Figure 2.9. The low-frequency gain of the integrator is given by $R_{DC}/H_0$, while the passband gain is $\gamma R_{DC}$. For $f < f_m$, $H(s)$ supplies high gain and signal currents are shunted away from $C_i$ and into the active reset feedback loop. $H(s)$ will either sink or source these currents as a result of the voltage rise or fall they induce at node B as they pass through $R_{DC}$. For $f > f_m$, $H(s)$ has strong attenuation thereby shutting off the active reset feedback loop and causing signal currents to flow through $C_i$.

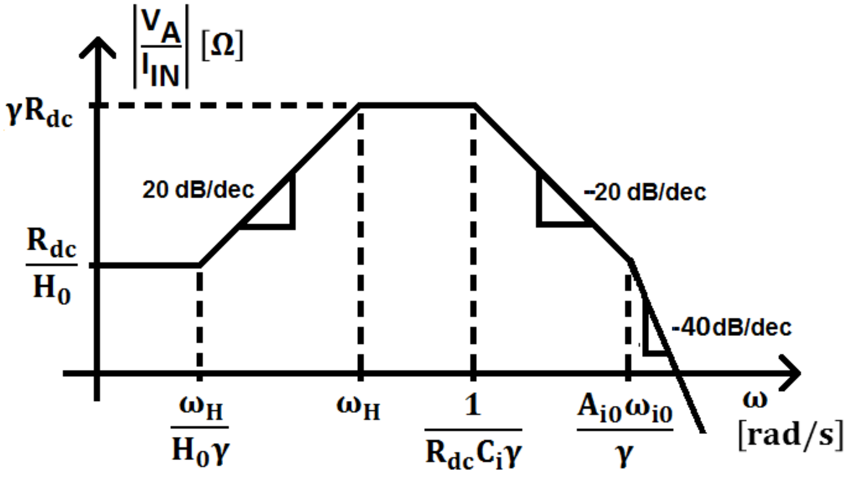

$\left|\frac{V_A}{I_{IN}}\right|$ [Ω]
$\gamma R_{dc}$
20 dB/dec
-20 dB/dec
$\frac{R_{dc}}{H_0}$
-40dB/dec
$\frac{\omega_H}{H_0\gamma}$
$\omega_H$
$\frac{1}{R_{dc}C_i\gamma}$
$\frac{A_{i0}\omega_{i0}}{\gamma}$
ω
[rad/s]

Figure 2.9: Frequency magnitude response of the active reset integrator stage of the TIA in Figure 2.7.

The transfer function of the second-stage differentiator of the TIA in Figure 2.7 is given by

$$\frac{v_{OUT}}{v_A}(s) \approx -\frac{sR_DC_d}{[1+s\gamma/(A_{d_0}\omega_{d_0})][1+sR_DC_{df}]}, \tag{2.23}$$

where $A_{d_0}\omega_{d_0}$ is GBP of the differentiator amplifier $A_d$. The frequency response of the differentiator is depicted in Figure 2.10. The coupling capacitor $C_d$ puts a zero at zero and effectively blocks any DC voltage passed from the integrator stage. The overall shape of the frequency response is that of a high-pass filter (HPF) with a passband determined by the time constant $R_DC_{df}$ and GBP of $A_d$.

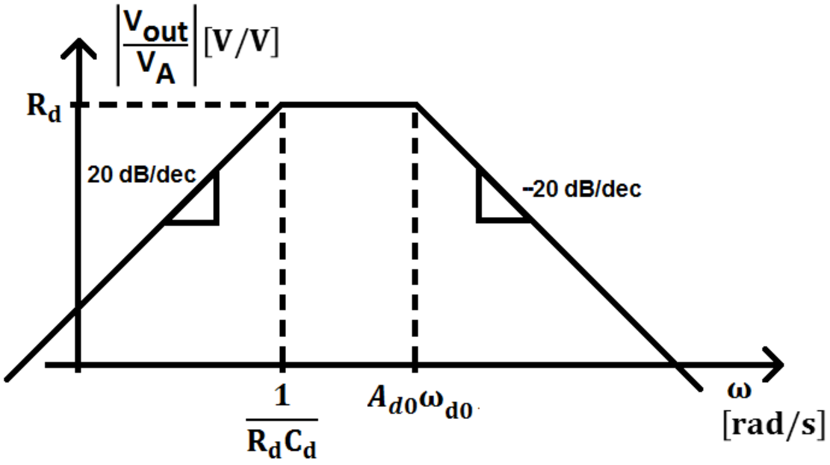


Figure 2.10: Frequency magnitude response of the differentiator stage of the TIA in Figure 2.7.

The overall frequency response of the CARTIA is determined by the product of the transfer functions expressed in Eqs. (2.21) and (2.23) and is shown in Figure 2.11. The passband gain is no longer determined by $\gamma R_{DC}$ but by the $R_DC_d/C_i$. The zero injected into the system by $C_d$ of the differentiator effectively boosts the bandwidth and is now characterized by the low-frequency cutoff $f_m$ and high-frequency cutoff $f_h = 1/2\pi R_DC_{df}$. It is possible that $f_h$ is a function GBP of amplifier $A_i$ depending on the size of $C_{df}$.

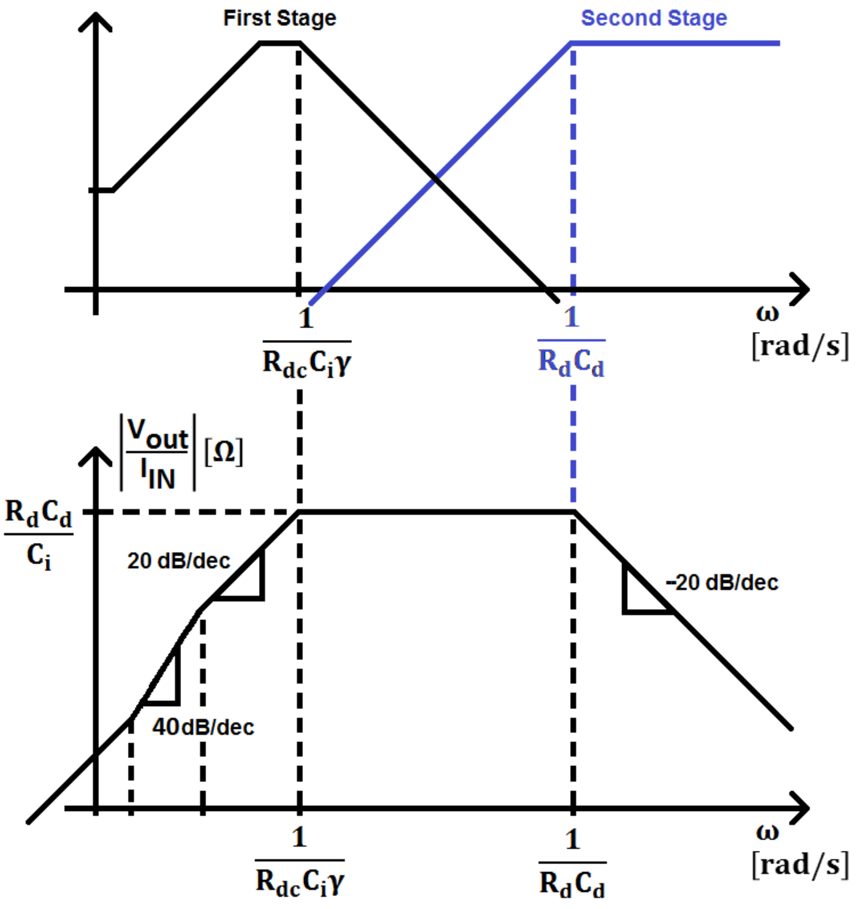


Figure 2.11: Frequency magnitude response of the continuous active reset stage of the TIA in Figure 2.7 as a result of cascading an integrator with a differentiator.

As a stand-alone CTIA, the first-stage integrator of the CARTIA provides a similar response to that of the RTIA-PI discussed in Section 2.3. However, the circuit in Figure 2.7 is more amenable to CMOS integration. The attenuation of the DC output offset is carried out by amplifier $H(s)$ in the CARTIA rather than by a PI amplifier as is the case with the RTIA-PI. Figure 2.12 shows the circuit implementation of the $H(s)$ transfer function. Referring to Eq. (2.20), $\omega_H = R_a C_2$ and $\gamma = C_1/C_2$. Since $f_m$ is a function of $\gamma$, the low frequency cutoff can be adjusted by setting capacitors $C_1$ and $C_2$. Some variability in $f_m$ is achieved using a switch to select between two different capacitors for $C_1$. Rather than using a linear resistor, the large resistances for $R_{DC}$ and $R_a$ in the is implemented using an active resistor that will be discussed in Section 2.4.2. In this way the CARTIA in Figure 2.7 can be implemented in a CMOS process without consuming a disproportionate amount of area on chip unlike the RTIA-PI.

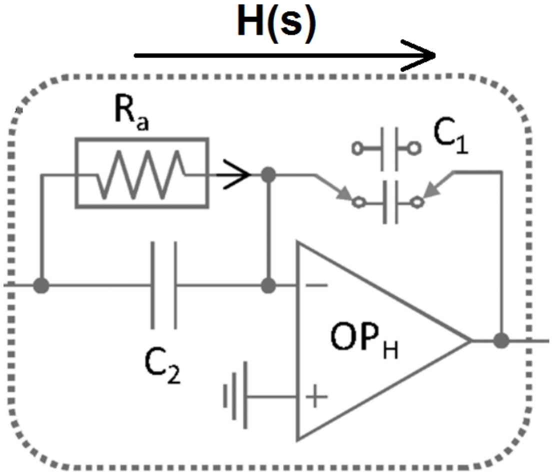


Figure 2.12: Circuit implementation of amplifier $H(s)$ for the CARTIA shown in Figure 2.7 (adapted from [30]).

### 2.4.2 Active Resistor Design

The resistance $R_{DC}$ must have a high value such that $f_m$ is well below 100 Hz and it must also exhibit low noise since it is the primary contributor to the input current noise. The linear transconductor presented in [25] and shown in Figure 2.13 meets these requirements. The foundation of the transconductor is the current divider that consists of PMOS transistors $T_1$ and $T_2$. The source-n-well and drain-gate connections of these devices are shorted together so that they operate as diode-connected PMOS transistors. Both transistors are also biased similarly because they share the same source-n-well node and the drain-gate terminals are tied to virtual ground.

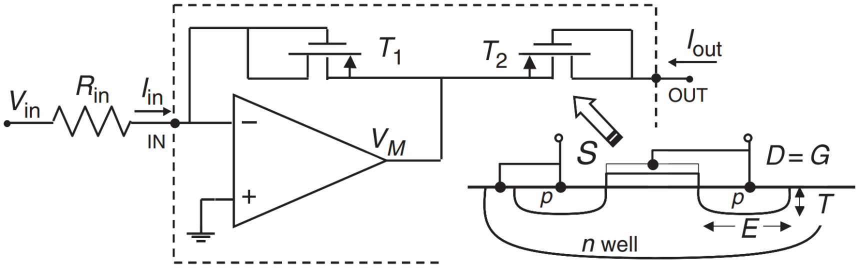


Figure 2.13: Schematic of current divider cell (dashed box, $I_{out}/I_{in}$) as the core of a high-linearity full-swing transconductor circuit $I_{out}/V_{in}$ [25].

By designing the width of $T_1$ to be $M$ times larger than $T_2$, the current through $T_1$ will be $M$ times greater than the current through $T_2$ (assuming the channel lengths of both devices are equal). Additional identical current dividers may be cascaded in order to compound this effect such that $I_{out} = I_{in}/M^N$, where $N$ is the number of cascaded current dividers. Taking $R_{in}$ into account, the transconductance, $g_m$, is given by

$$g_m = \frac{I_{out}}{V_{in}} = \frac{1}{R_{in}M^N}, \tag{2.24}$$

and as a result, the output resistance $1/g_m$ can be made very large.

The thermal noise contributed by $R_{in}$ and the shot noise contributed by $T_1$ at the output of the transconductor are both attenuated by the gain of the current divider, $M^2$. Therefore, the dominant noise source is the shot noise ($2qI_{out}$) contributed by $T_2$ and is therefore a function of the input DC current. Choosing the multiplication factor $M$ can be used as a means of reducing noise since the current through $T_2$ is always $M$ times smaller than the current through $T_1$. The flicker noise generated by both transistors can be reduced by maximizing the the total area of the PMOS devices used (large channel length and width).

### 2.4.3 Output Voltage Saturation

Node B in the integrator stage of Figure 2.7 is vulnerable to saturation. Assuming the virtual ground is set to mid-rail, the maximum current that $H(s)$ can process $I_{DC_{max}}$ is given by

$$I_{DC_{max}} = \left| \frac{V_{DD}}{2R_{DC}} \right| . \tag{2.25}$$

This is unique since $I_{DC_{max}}$ is not a function of the overall passband gain of the system ($v_{OUT}/i_{IN} = R_D C_d / C_i$).

### 2.4.4 Noise Performance

As with the analysis of the previous TIAs, the noise of the input op amp $A_i$ is ignored. The input current noise contributed by the differentiator op amp $A_d$ and resistor $R_d$ is attenuated by a factor of $(C_d/C_i)^2$ and thus negligible in comparison with the thermal noise of $R_{DC}$. Since $R_{DC}$ is implemented using the transconductor discussed in Section 2.4.2, the input-referred current noise PSD $\overline{i^2_{n,CARITA}}(f)$ due to $R_{DC}$ is given by

$$\overline{i^2_{in,CARTIA}}(f) = 2qI_{DC_{max}}, \tag{2.26}$$

where $q$ is the electronic charge. The current noise generated by an equivalently-sized linear resistor would be $4kT/R_{DC}$. In comparison, the transconductor implementation of $R_{DC}$ may exhibit reduced noise for low DC currents.

Ignoring the low-frequency attenuation shown in Figure 2.11 and assuming the bandwidth is limited by $1/(2\pi R_D C_{df})$, the RMS input current noise of the CARTIA can then be found using

$$\overline{i_{n,CARTIA}} = \sqrt{\frac{qI_{DC_{max}}}{R_D C_{df}}}. \tag{2.27}$$

The SNR of the TIA, in dB, is given by

$$SNR_{CARTIA} = 10\log_{10}\left[\overline{i_{in}}^2 \frac{R_D C_{df}}{qI_{DC_{max}}}\right]. \tag{2.28}$$

### 2.4.5 Design Tradeoffs

The active resistor $R_{DC}$ can be adjusted to set $I_{DC_{max}}$ for a given application without affecting the passband transimpedance of the system. This is not so with the TIAs previously discussed where saturation due to the DC current is always dependent on the DC gain.

Due to the complexity of the feedback system, each component value must be considered carefully in order to ensure the system is stable. $R_{DC}$ and the design of $H(s)$ directly impact the stability of the system [30]. In order to provide sufficient phase margin in the integrator stage, $R_{DC}$ should be designed large enough to separate it from the GBP of amplifier $A_i$ (refer to Figure 2.9).

Implementing $R_{DC}$ as a transconductor makes it possible to achieve the large time constants required in a CMOS process. The resulting input-referred current noise, however, is a function of the standing current. The more current that the CARTIA sinks (or sources) the higher the input-referred current noise. Therefore it is possible that $R_{DC}$ exhibits lower noise when implemented as a transconductor rather than a linear resistor as long as $I_{DC}$ is low enough.

## 2.5 Performance Comparison of TIA Architectures

Table 2.1 tabulates the performance of the four TIA architectures discussed in this chapter.

Table 2.1: Summary of performance for various TIA architectures.

| Criteria | RTIA [1] | CTIA [2] | RTIA-PI [24] | CARTIA [30] |
|---|---|---|---|---|
| Supply Voltage | 3.3 V | 3.3 V | – | 3.3 V |
| CMOS Process | 0.5 $\mu$m | 0.5 $\mu$m | discrete | 0.35 $\mu$m |
| Transimpedance | 25 M$\Omega$ | 100 M$\Omega$ | 1.2 G$\Omega$ | 1.8 G$\Omega$ |
| -3-dB Bandwidth | 10 kHz | [a]10 kHz | 250 Hz | [b]100 Hz |
| Input DC Current Range | ±1 nA | ±12 nA | ±0.4 nA | ±25 nA |
| Input Referred RMS Noise (10 kHz BW) | 5 pA | 1.35 pA | 0.8 pA | 0.5 pA |

[a] Integration time ($T_{int}$) is set to 100 $\mu$s.

[b] Bandwidth of the first stage integrator. With the addition of a second stage differentiator, the bandwidth is extended to 4 MHz while the transimpedance is reduced to 20 M$\Omega$.

# Chapter 3

# Proposed Transimpedance Amplifier Architecture

This chapter develops a single stage TIA circuit architecture that has sufficient gain to sense signal currents on the order of tens of pA while maintaining a zero output offset voltage for DC currents on the order of nA and a noise floor within the fA/$\sqrt{\text{Hz}}$ range. The proposed TIA also offers continuous-time measurement of input current signals and an adjustable low-frequency cutoff which is advantageous in several biosensing applications as discussed in Chapter 1.

## 3.1 Selecting the Feedback Type

The first step is to determine whether to use a resistive or capacitive feedback architecture to process the input signal current. In either case, the input DC current can saturate the circuit and the maximum DC current that the TIA can sink or source is proportional to the DC gain (transimpedance). However, the effect on the resistive feedback is subtly different from that on the capacitive feedback. Irrespective of the DC current level, the feedback capacitor $C_f$ must be reset since charge will continuously accumulate until the output node voltage is saturated. Even for small currents that would otherwise result in a negligible DC voltage offset in resistive feedback (for an equivalent DC gain), the capacitive feedback must still be reset eventually. This dependence sets an unnecessary limit on the measurement time allotted for current measurement ($T_{int}$). Moreover, $T_{int}$ must be readjusted for every different DC input current level. While it may be trivial to readjust $T_{int}$ adjusting $C_f$ is not. Since the gain and bandwidth of the system are also dependent on $T_{int}$ and $C_f$, it is impossible to maintain the same frequency response while accommodating for different DC input currents. This is not true for resistive feedback which provides an unlimited measuring time and constant frequency response regardless of the input DC current level and for this reason, resistive feedback is preferable for current sensor applications.

The advantages of capacitive feedback are reduced noise and chip area consumption in comparison with the resistive feedback TIA. In the case of a feedback resistor, these two aspects must be addressed simultaneously. As shown in Section 2.1.3, input-referred current noise is inversely proportional to the resistance $R_f$. Therefore, reducing the noise comes at the expense of chip area. For the applications discussed in Chapter 1 $R_f$ must be set to at least 1 GΩ for the TIA to provide sufficient current sensitivity (in the nA range). The input-referred current noise PSD generated by a 1 GΩ resistor is approximately 4 fA/$\sqrt{\text{Hz}}$ which is satisfactory. However the difficulty lies in implementing such a large resistance on chip. As a result, the TIA with feedback transconductor in Figure 3.1 is considered.

A high transimpedance can be achieved using an active transconductor in the feedback

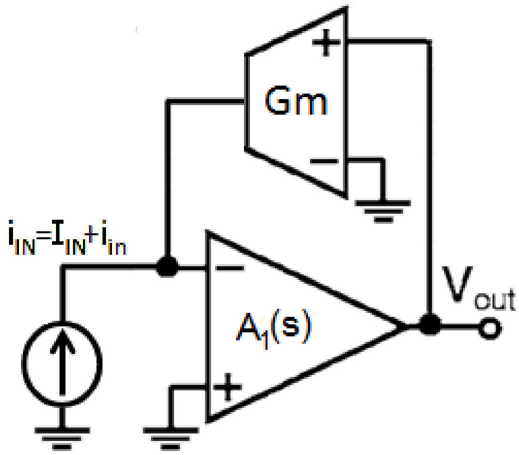


Figure 3.1: Transimpedance amplifier with feedback transconductor.

loop of the TIA instead of a single linear resistor. In the same way a conventional TIA with feedback resistor $R_f$ has an overall transimpedance given by $V_{out}/I_{in} = -R_f$, this TIA architecture, with active transconductor $G_m$, provides a feedback resistance $R_f = 1/G_m$.

## 3.2 Feedback Transconductor Implementation

The transconductor used in the proposed TIA shown in Figure 3.2 is inspired by [25]. As with previous TIA architectures, the transconductor connects amplifier $A_1$ in negative feedback which sets a virtual ground at the inverting input. Since the impedance looking into the inverting input is extremely large, the input current $i_{IN}$ is forced through the feedback branch and into $G_m$.

The two-stage transconductor in Figure 3.2 is formed using amplifiers $A_3$ and $A_4$ and resistors $R_b$ and $MR_b$, where $M$ is a multiplicative factor. Amplifiers $A_3$ and $A_4$ are connected in negative feedback and drive their respective inverting input node voltages

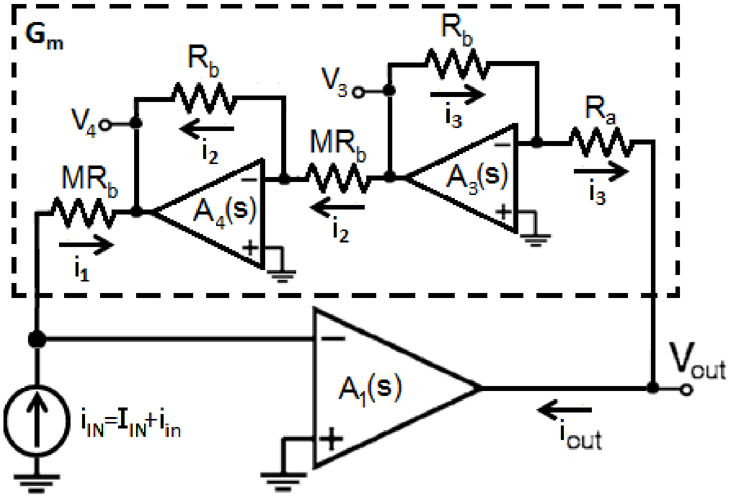


Figure 3.2: Transimpedance amplifier with two-stage feedback transconductor.

towards virtual ground. Therefore, the only node voltages that can vary are $V_{out}$, $V_3$ and $V_4$. In addition, the voltage across each pair of $R_b$ and $MR_b$ resistors is the same. As a result, $i_{IN} = i_1$ flows through the resistor $MR_b$ which raises the output voltage of $A_4$ to $V_4$. Now the voltage across $R_b$ is also $V_4$ and current $i_2$ flows. Currents $i_1$ and $i_2$ can therefore be expressed as follows:

$$i_1 = \frac{-V_4}{MR_b} \text{ and } i_2 = \frac{-V_4}{R_b}. \tag{3.1}$$

Equating $i_1$ and $i_2$ yields $i_2 = Mi_1$. Note that the that currents $i_1$ and $i_2$ have been defined in the schematic to flow in opposite directions since this will always be the case. Nodal analysis is applied to the second stage and gives

$$i_2 = \frac{V_3}{MR_b} \text{ and } i_3 = \frac{V_3}{R_b}, \tag{3.2}$$

which adds another current gain factor of $M$ since $i_3 = Mi_2$. It should be evident at this point that the node voltages $V_{out}$, $V_3$, and $V_4$ may drop below the virtual ground as a result of the input current which is expected to be bidirectional [29]. Therefore, the voltage rails along with the virtual ground must be chosen in order to accommodate for this. This is discussed further in Chapter 4.

Aggregating the effect of these two transconductance stages means that $I_{out} = I_{in}M^2$. This current gain is used to provide a large $1/G_m$ such that the overall gain of the TIA is

$$\frac{V_{out}}{I_{in}} = -\frac{1}{G_m} = -M^2 R_a. \tag{3.3}$$

Therefore, large gain can be achieved by adjusting the factor $M$. This transimpedance can only be obtained as long as the base resistance $R_b$ remains constant over both stages (and any subsequent stages). It is possible however, to use a different $M$ factor across the two stages so that Eq. (3.3) becomes $1/G_m = -M_1 M_2 R_a$ where $M_1$ and $M_2$ are the gain factors for first and second stages of the transconductor respectively.

The fact that $M$ is effectively the ratio of two resistors is advantageous since the specified resistance values for $R_b$ and $MR_b$ are subject to error due to process variation. Considering that $R_a$ is obviously subject to the same error, the design strategy used to implement this TIA is to make $M$ as large as possible by interleaving $R_b$ and $MR_b$ while taking more care with the layout of $R_a$ to ensure negligible error.

In contrast to the transconductor presented in [25], linear resistors are used in the feedback transconductor instead of MOS-bipolar pseudo-resistors in order to improve linearity. In [25], diode-connected PMOS devices with different widths are used in order to obtain the current division behaviour mentioned above. These PMOS pseudo-resistors contribute only shot noise and flicker noise which are, in general, much less significant and more easily remedied than thermal noise as mentioned in Section 2.4.2. For this design linearity is preferred over noise performance.

It should be noted that resistors implemented in CMOS 0.35 $\mu$m technology are not perfectly linear. Integrated resistors exhibit both voltage and temperature dependencies, the extent of which is determined by the mask layer used. The physical layout of each individual resistor will also contribute to the linearity of the system. However, similar dependencies exist for PMOS devices and thus linear resistors are best suited to ensure system linearity.

### 3.2.1 Noise Performance

Resistors $R_b$ and $MR_b$ contribute thermal noise to the total input-referred current noise of the TIA. The input-referred current noise PSD $\overline{i_{in}^2}(f)$ contributed by all the resistors in the transconductor chain is given by

$$\overline{i_{in}^2}(f) = \frac{kT}{MR_b}\left[4 + \frac{1}{M^2} + \frac{1}{M^3} + \frac{1}{M^4}\right] + \frac{kT}{M^4 R_a} \tag{3.4}$$

The above equation has three useful design implications. First, the most significant term is $4kT/MR_b$ which is contributed by the $MR_b$ resistor in the transconductor that is connected to the TIA input. Thus $MR_b$ should be maximized to reduce the thermal noise. Second, the multiplication factor $M$ should be maximized to reduce the effect of each noise term in Eq. (3.4). Finally, the thermal noise generated by $R_a$ is negligible since it is attenuated by a factor of $M^4$.

## 3.3 Low-Frequency Input Signal Suppression

The effects of low-frequency input currents are suppressed by zeroing the output DC level of the TIA using the non-inverting integrator composed of amplifier $A_2$, resistor $R_2$, and capacitor $C_2$ shown in Figure 3.3 [24]. The low-frequency behaviour of the TIA is established by the zero and pole generated by integrator time constant $R_2C_2$. In order to aid in the analysis that proceeds low-frequency cutoff, $f_L$ is defined as

$$f_L = \frac{1}{2\pi R_2 C_2}. \tag{3.5}$$

This frequency characterizes two modes of operation for the system in Figure 3.3, one mode for frequencies below $f_L$, and another for frequencies above $f_L$. The TIA gain for input signals at frequencies near $f_L$ is given by

$$\frac{V_{out}(s)}{I_{in}(s)} \approx -\frac{1}{G_m A_{2_0}} \frac{1 + sR_2C_2A_{2_0}}{1 + sR_2C_2}, \tag{3.6}$$

where $A_{2_0}$ is the open-loop DC gain of $A_2$. As demonstrated by the above equation, the pole and zero are separated by a factor $A_{2_0}$ and the TIA gain is attenuated by the same factor. At input-signal frequencies below $f_L$, the impedance of $C_2$ becomes very large and behaves as an open circuit. In this way amplifier $A_2$ operates in open-loop and the voltage gain $V_x/V_{out}$ is nearly equal to $A_{2_0}$, where $V_x$ is an intermediate node in the TIA feedback loop as shown in Figure 3.3. Since the current through $R_2$ is zero, the voltage at the non-inverting input of $A_2$ is grounded (midway between $V_{DD}$ and $V_{SS}$). As a result, $A_2$ regulates $V_{out}$ through the overall feedback. Note here that the transimpedance $V_x/I_{in}$ is still $1/G_m$ and is prone to saturation due to DC input current.

Conversely, at input signals at frequencies above $f_L$, the impedance of $C_2$ becomes very small and behaves as a short circuit. This allows signals to propagate directly to $V_{out}$ as $A_2$ operates in a unity-gain configuration at these frequencies. However, $A_2$ successfully decouples any voltage amplification due to DC current from $V_{out}$. Figure 3.3 also illustrates the parasitic capacitance $C_p$ in parallel with the feedback transconductor which affects the high-frequency response of the TIA. A reasonable estimate for $C_p$ is on the order of 100 fF. At frequencies greater than $f_L$, the TIA gain is given by

$$\frac{V_{out}(s)}{I_{in}(s)} \approx -\frac{1}{G_m} \frac{1}{1 + sC_p/G_m}, \tag{3.7}$$

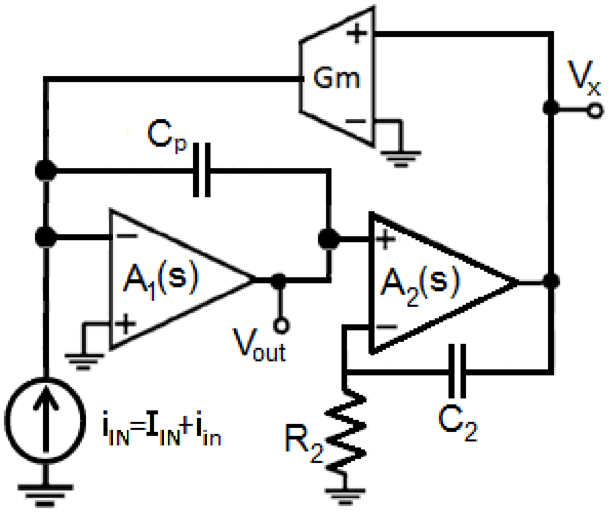


Figure 3.3: Transimpedance amplifier architecture with feedback transconductor and integrator to suppress input currents below the low-frequency cutoff.

which shows the high-frequency cutoff of the TIA. Figure 3.4 depicts the expected frequency response of the TIA.

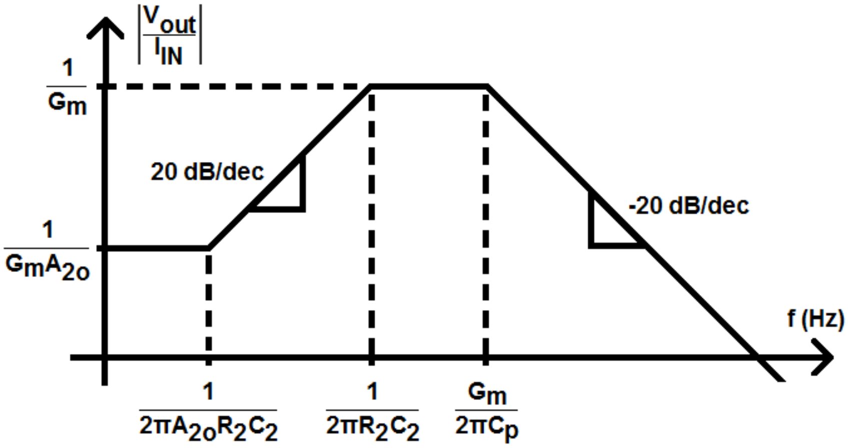


Figure 3.4: Expected frequency magnitude response of the proposed TIA.

### 3.3.1 Bandwidth Tuning

The low-frequency cutoff of the TIA can be adjusted by modifying the zero and pole generated by the integrator time constant $R_2C_2$. In order filter out the effect of the DC current on the output $f_L$ must be 100 Hz or lower. Using Eq. (3.5), this means that $R_2C_2$ must be on the order of ms or lower. The available technology, CMOS 0.35 $\mu$m, limits resistor values to only tens of M$\Omega$ and capacitor values to tens of pF. The solutions discussed in this section addresses this issue by using alternative implementations of $R_2$ to achieve high resistances.

First, it is necessary to show that $R_2$ cannot be implemented using the transconductor outlined in Section 3.2. The reason for this is that the input to the transconductor is set to ground as shown in Figure 3.5. The voltage across $R_a$ is zero since it is grounded on one side ($V_{GND} = 0$) and a virtual ground is regulated by $A_3$ on the other. Consequently, current $i_3$ must be zero and $V_4 = V_{GND}$. By the same logic $i_2 = 0$ and $A_3$ will either sink or source the input current $i_1$. Regardless of the input current $i_1$ to the transconductor, $i_2$ and $i_3$ will remain zero since $V_{GND}$ cannot fluctuate. Therefore, the effective resistance that the transconductor supplies is that of $MR_b$ which is insufficient.

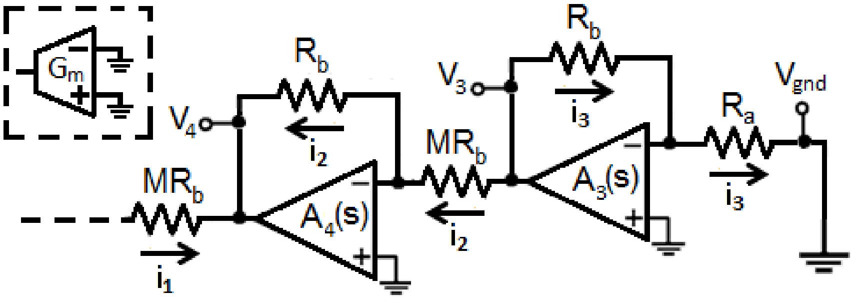


Figure 3.5: Transimpedance amplifier with transconductor feedback and integrator to suppress input currents below the low-frequency cutoff.

A more practical alternative is to use a PMOS transistor as a pseudo-resistor as shown in Figure 3.6 where $I_D$ is the drain current. This device was mentioned briefly in Section 2.4.2 and will now be analyzed further. The PMOS pseudo-resistor has two modes of operation defined by the applied $V_{GS}$. For negative $V_{GS}$, the device functions as a diode-connected PMOS transistor. As long as the PMOS operates in the subthreshold regime ($|V_{GS}| < |V_{tp}|$), the relationship between voltage and current is exponential. For positive $V_{GS}$, the p-n junction diode formed between the drain and the body is forward biased and the device is operating as a lateral BJT [32]. In either case, the incremental resistance is extremely high.

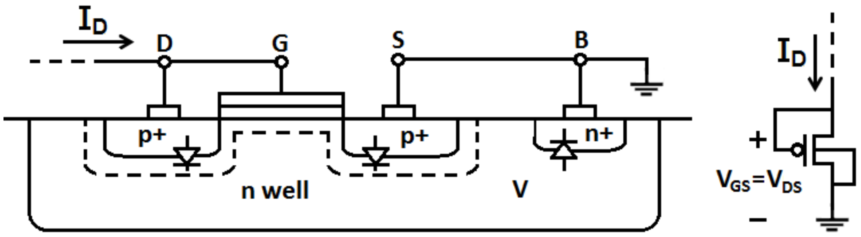


Figure 3.6: Diode-connected PMOS pseudo-resistor, where the gate-drain and source-body terminals are shorted.

Figure 3.7 shows a transient simulation of $I_D$ for a single PMOS pseudo-resistor given a 0.5 V amplitude 1 kHz signal where significant distortion is observed. Large-signal voltages give rise to variations in $V_{GS}$ on the order of mV. This exceeds the linear region of the diode $I_{DS}$ vs. $V_{DS}$ curve shown in Figure 3.8(a). Figure 3.8(b) shows the effective resistance of the diode-connected PMOS pseudo-resistor ($dV_{GS}/dI_{in}$). Variations on the order of tens of mV can cause large scale variations in the impedance of the PMOS device.

In order to reduce this distortion, identical devices are connect in series [33]. The total potential drop across the chain of PMOS devices as a result of the large signal is

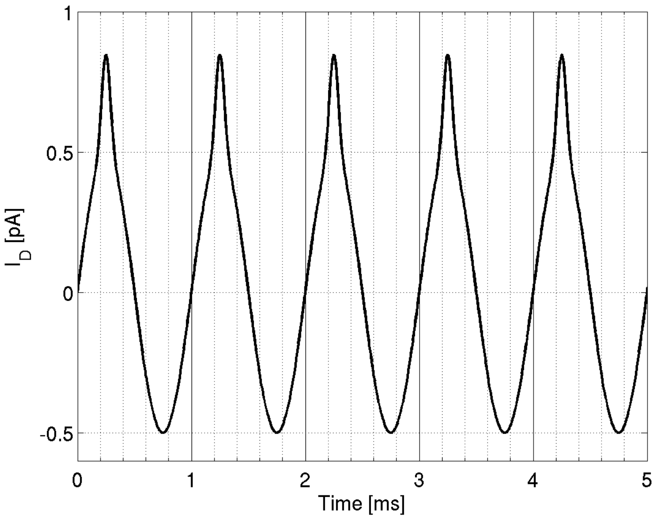


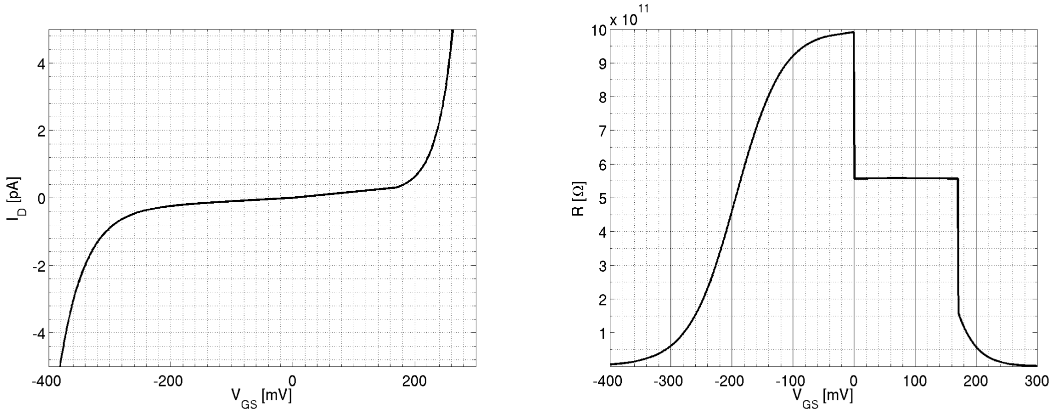
Figure 3.7: Transient simulation of $V_{GS}$ for PMOS pseudo-resistor shown in Figure 3.6.

equally subdivided across individual devices as shown in Figure 3.9(a). Therefore, with every additional PMOS, the potential drop across each individual device is reduced and by extension, the distortion as well.

Although this method does provide sufficient resistance, $f_L$ is not well controlled. While it may be possible to set $f_L$ accurately in simulation using these devices, $f_L$ will vary due to process variations. Also, once the transistors are laid out, $f_L$ cannot be modified.

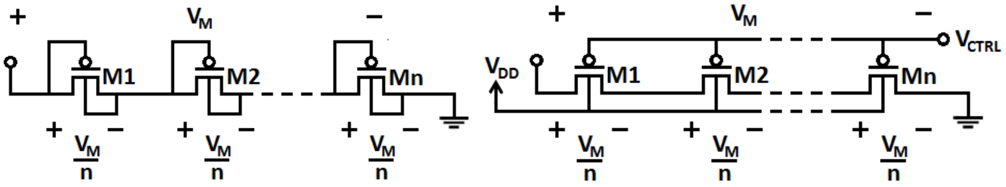
Alternatively, the PMOS devices can be configured as shown in Figure 3.9(b) where the gate terminal of the PMOS devices are shorted together and connected to an I/O pad. To achieve very high on resistance, the PMOS devices can be operated in the subthreshold regime. Figure 3.10 shows the $I_{DS}$ vs $V_{DS}$ curve in the 0.35-$\mu$m CMOS technology of a subthreshold PMOS transistor with width and length of 4 $\mu$m by 2 $\mu$m.

As $V_{ctrl}$ increases the effective resistance will also increase pushing $f_L$ to lower frequencies and vice-versa.



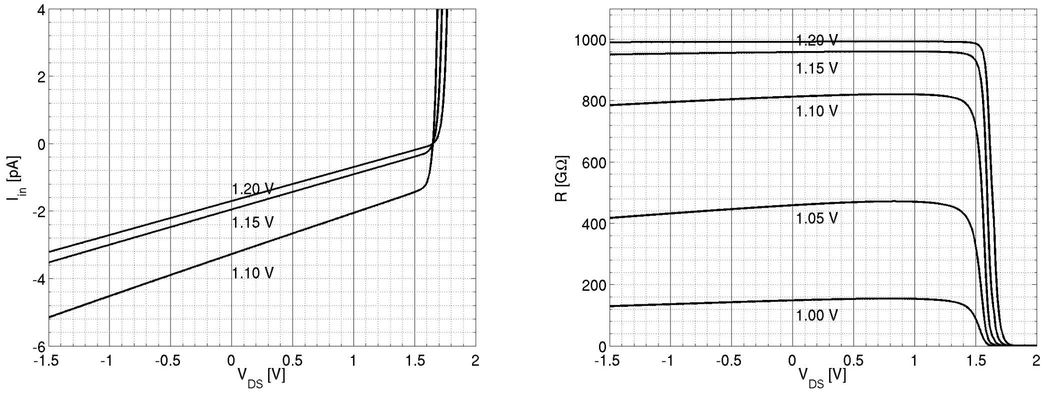
(a) (b)

Figure 3.8: (a) $I_{DS}$ vs $V_{DS}$ curve in the 0.35-$\mu$m CMOS technology of a diode-connected PMOS transistor with width and length of 4 $\mu$m and 2 $\mu$m, respectively. Terminal pairs gate-drain and source-body are shorted. (b) The effective resistance of the diode-connected PMOS. Calculated by taking the derivative of (a) and inverting ($dV_{GS}/dI_{in}$). The sharp drop in resistance at 0 V is a result of the numerical modeling of the simulator.


+
$V_M$
−
M1
M2
Mn
+ $\frac{V_M}{n}$ −
+ $\frac{V_M}{n}$ −
+ $\frac{V_M}{n}$ −
+
$V_M$
−
$V_{CTRL}$
$V_{DD}$
M1
M2
Mn
+ $\frac{V_M}{n}$ −
+ $\frac{V_M}{n}$ −
+ $\frac{V_M}{n}$ −

(a) (b)

Figure 3.9: PMOS devices connected in series to reduce distortion by subdividing applied voltage equally across all devices operating (a) as diode-connected PMOS/lateral BJT devices and (b) in the subthreshold regime with an applied control voltage $V_{CTRL}$.



(a) (b)

Figure 3.10: Simulation of (a) the $I_{DS}$ vs. $V_{DS}$ curve and (b) effective resistance under various control voltages ($V_{ctrl}$) for a single subthreshold PMOS device.

## 3.4 Comparison of Proposed TIA with other Architectures

While the system shown in Figure 3.3 is still subject to saturation at $V_x$, unlike the classical resistive feedback TIA, the effects of the input DC current on $V_{out}$ are suppressed and the voltage swing is maximized. Also, by implementing a transconductor in the feedback path, high gain and low noise are achieved. Though capacitive feedback with switching does have better noise performance, the proposed design is preferable since no constraint exists on the time allotted for current measurement.

In contrast to the RTIA-PI discussed in Section 2.3, the proposed TIA architecture is more amenable to CMOS integration since the transconductor outlined in Section 3.2 is used to achieve the desired gain rather then a single linear resistor. Furthermore, the large time constant invoked by the feedback integrator is controlled and adjustable using subthreshold PMOS devices.

There are two main differences between the proposed design presented above and the continuous active reset architecture [23] discussed in Section 2.4. First, [23] utilizes two stages (an integrator and differentiator) while Figure 3.3 can supply sufficient gain in a single stage. Considering the integrator stage alone, [23] does not provide sufficient gain for the applications mentioned in Chapter 1. However, this reduced gain in the integrator is beneficial for sinking or sourcing large input DC currents. Additionally, the integrator alone is subject to the same bandwidth limitations mentioned in Section 3.3. The differentiator is required in order to provide the necessary gain and extend the bandwidth. A differentiator could be added to the output of Figure 3.3, however, the transimpedance between the input and differentiator output would no longer be $1/G_m$. Second, the TIA in Figure 4.1 has an adjustable low-frequency cut off while [23] does not. The ability to manually tune $R_2$ and adjust the low-frequency cutoff is not available in the implementation of $H(s)$ in [23].

# Chapter 4

# Circuit Design and Implementation

This chapter discusses the design of the TIA architecture proposed in Chapter 3. The complete TIA with active resistor for tuning the low-frequency cutoff is shown in Figure 4.1. This design was implemented using a 3.3-V 0.35-$\mu$m CMOS technology. Accordingly, the positive supply voltage $V_{DD}$ is set to 3.3 V and $V_{SS}$ is 0 V. In order to maximize the available voltage swing and accommodate bidirectional current flow, the virtual ground $V_{GND}$ is set to the mid-rail voltage 1.65 V. On-chip voltage buffers (not shown) transmit the circuit output $V_{out}$ and intermediate node $V_x$ off chip. Capacitor $C_{in}$ in Figure 4.1 represents the pad, chip package, and PCB trace parasitics at the input of the TIA.

The overall transfer function of the TIA, $H(s) = v_{OUT}(s)/i_{IN}(s)$, is given by

$$H(s) = \frac{-MR_b\left[\frac{1+M(1+A_4(s))}{A_4(s)}\right]\left[\frac{R_a(1+A_3(s))+R_b}{R_bA_3(s)}\right]\left[\frac{1+(1+A_2(s))sR_2C_2}{(1+sR_2C_2)A_2(s)}\right]}{1+\left[\frac{1+sMR_b[C_p(1+A_1(s))+C_{in}]}{A_1(s)}\right]\left[\frac{1+M(1+A_4(s))}{A_4(s)}\right]\left[\frac{R_a(1+A_3(s))+R_b}{A_3(s)R_b}\right]\left[\frac{1+(1+A_2(s))sR_2C_2}{(1+sR_2C_2)A_2(s)}\right]}, \quad (4.1)$$

where $R_2$ is the effective resistance of the subthreshold PMOS devices and $A_1(s)$, $A_2(s)$, $A_3(s)$, and $A_4(s)$ are the open-loop transfer functions of each amplifier in Figure 4.1 re-

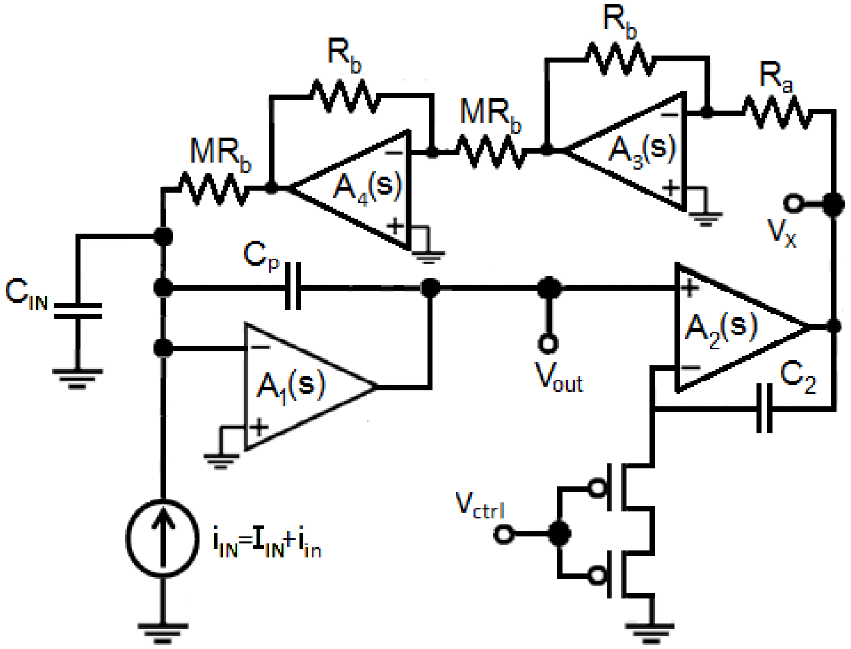


Figure 4.1: Transimpedance amplifier with transconductor feedback and PI controller to suppress input currents below the low-frequency cutoff.

spectively. As the gain of each amplifier becomes large, $H(s)$ is given by

$$H(s) \approx -M^2 R_a \frac{sR_2C_2}{[1+sR_2C_2][1+s(M^2R_a)C_p]}, \tag{4.2}$$

as expected. The desired response in the above equation is achievable only if each amplifier supplies sufficient open-loop gain. Table 4.1 shows the component values selected for the TIA in Figure 4.1.

Table 4.1: Summary of performance for various TIA architectures.

| Component | $M$ | $R_a$ | $R_b$ | $MR_b$ | $C_2$ |
|---|---|---|---|---|---|
| Value | 150 | 50 kΩ | 10 kΩ | 1.5 MΩ | 1 pF |

## 4.1 Bandwidth Tuning

The low-frequency cutoff $f_L$ is tuned by implementing an active resistor comprised of two identical series PMOS transistors operated in the subthreshold regime. Two devices are used in order to minimize the signal distortion as discussed in Section 3.3.1. Each PMOS is sized with width and length of 4 $\mu$m and 2 $\mu$m, respectively.

The effective resistance of these devices is controlled by adjusting the gate voltage, $V_{ctrl}$, supported by an off-chip source. Increasing $V_{ctrl}$ increases the overall resistance of the PMOS devices. Figure 5.5 shows the simulated variation in $f_L$ as the control voltage of the active resistor changes. With $C_2 = 10$ pF, $f_L$ can be varied from less than 1 Hz to more than 10 kHz.

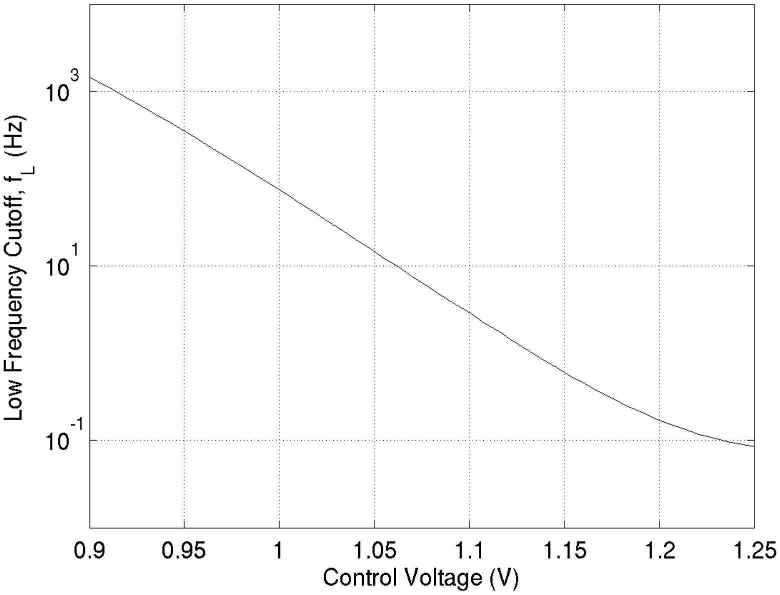


Figure 4.2: Simulated tuning range of the TIA low-frequency cutoff.

Parallel plate capacitor $C_2$ is implemented using two polysilicon layers available in the

CMOS process. A unit-size capacitor of 500 fF with dimensions 26.5 $\mu$m × 26.0$\mu$m, is used to implement all capacitors in the TIA. Therefore $C_2 = 1$ pF consumes a total area of approximately 0.0014 mm$^2$.

## 4.2 Transconductor Design

In order to obtain a nominal transimpedance of $M^2 R_a = 1$ G$\Omega$, the two-stage feedback transconductor has been designed with $M = 150$, $R_b = 10$ k$\Omega$, and $R_a = 50$ k$\Omega$. These values were selected in order to reduce the overall input-referred current noise as discussed in Section 3.2.1. As per Eq. (3.4), the larger $R_b$ the lower the noise. However, the upper limit for the resistance value of $R_b$ is based on the total area that each resistor in the transconductor occupies. Having $R_b = 10$ k$\Omega$ means $MR_b = 1.5$ M$\Omega$ which occupies significant area. Using Eq. (3.4), the expected input-referred current noise PSD is approximately $1.1064 \times 10^{-26}$ A$^2$/Hz or $1.1052 \times 10^{-13}$ A/$\sqrt{\text{Hz}}$.

The CMOS 0.35 $\mu$m technology supports several resistor types, each exhibiting a particular resistivity as well as temperature and voltage dependence. A p+ diffusion resistor is used for $R_b$ and $MR_b$. Although n-well diffusion resistors provide higher sheet resistance per unit area than p+ diffusion (1050 $\Omega/sq$ vs. 150 $\Omega/sq$), $MR_b$ is more area efficient when implemented in p+ diffusion due to the minimum spacing requirement of at least 3 $\mu$m between adjacent n-wells. Resistor $R_a$ is also implemented using a p+ diffusion resistor.

### 4.2.1 Resistor Layout

The margin of error associated with the transconductance $G_m$ lies in the precision of $R_a$ and the factor $M$ and not in the specific resistance values of $R_b$ and $MR_b$. Though process variation will introduce some margin of error in the exact resistance value, as long as $R_b$ and $MR_b$ are affected the same way, the designed value of $M$ will be maintained. However, any variation in $R_a$ will directly affect $G_m$. This is taken into consideration when designing the physical layout of each resistor.

The effect of process variation on $M$ is minimized by interleaving the layouts for resistors $R_b$ and $MR_b$. Having a unit p+ diffusion 20 kΩ resistor of minimum width, $MR_b = 1.5$ MΩ is constructed using a series combination of 75 unit resistors while $R_b = 10$ kΩ is realized using four parallel pairs of two unit resistors in series ([20 kΩ + 20 kΩ]/4 = 10 kΩ). The purpose of breaking up $R_b$ into eight unit resistors is so that $R_b$ can be evenly distributed throughout $MR_b$ as shown in in Figure 4.3. The 20 kΩ unit resistor has dimensions 320 μm × 2.5 μm. Therefore, the chip area consumed by a single $R_b$-$MR_b$ pair, with the necessary spacing between unit resistors, is 0.082 mm$^2$.

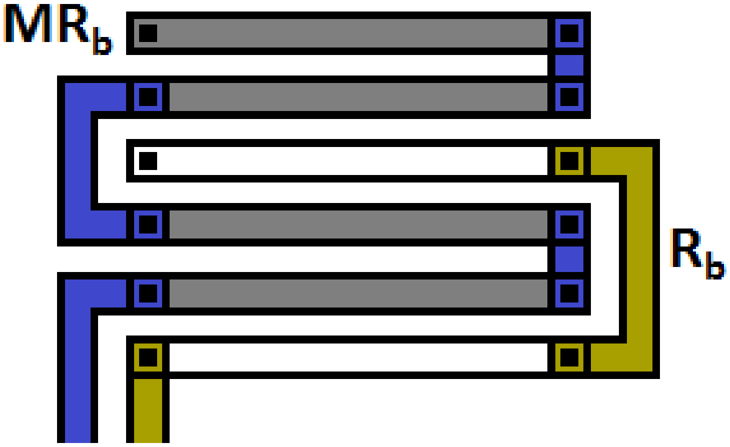


Figure 4.3: P+ diffusion resistor layout of $R_b$ interspersed throughout $MR_b$.

Resistor $R_a$ is implemented using ten unit sized 5 kΩ p+ diffusion resistors connected in series. This unit resistor has dimensions 482.5 μm × 12.8 μm. The layout area of $R_a$, with spacing, is approximately 0.065 $\text{mm}^2$.

The total chip area of all the resistors used in the transconductor ($2 \times R_b$, $2 \times MR_b$ and $R_a$) is approximately 0.23 $\text{mm}^2$. In comparison, a single 1 GΩ on-chip linear resistor would consume an area of around 50 $\text{mm}^2$ using p+ diffusion.

## 4.3 Amplifier Design

A single-ended output folded-cascode architecture with PMOS inputs, shown in Figure 4.4, is utilized as the input stage for each amplifier in the TIA. The tail current $I_{tail}$ supplies a drain current of $I_{tail}/2$ to each of the input PMOS devices while $I_{bias}$ is used to set the drain current of the cascode current mirror devices. The high output resistance attainable by cascoded devices is advantageous in achieving the necessary open-loop voltage gain in a single stage. The load capacitance at this single high impedance node is usually sufficient for stability. This is desirable for the overall stability of the feedback TIA which is dependent on the closed-loop stability of each amplifier. PMOS devices are used at the input as these generally produce less input-referred flicker noise than NMOS devices for a given area. The folded-cascode also provides reasonable voltage swing at the output.

Each amplifier is designed such that $V_{GND} = 1.65$ V lies within the common mode input range. Transistor aspect ratios are selected to reduce the systematic offset voltage at the output. Bias voltages are adjusted ensure transistors operate in strong inversion and to maximize the output voltage swing given by

$$-V_{SS} + 2V_{ov} < V_{out} < V_{DD} - |V_t| - 2|V_{ov}|, \tag{4.3}$$

where $V_{tp}$ is the threshold voltage of PMOS transistors in the CMOS technology used ( ≈-600 mV) and $V_{ov}$ is the overdrive voltage $V_{GS} - |V_{tp}|$. The voltage gain of the cascode

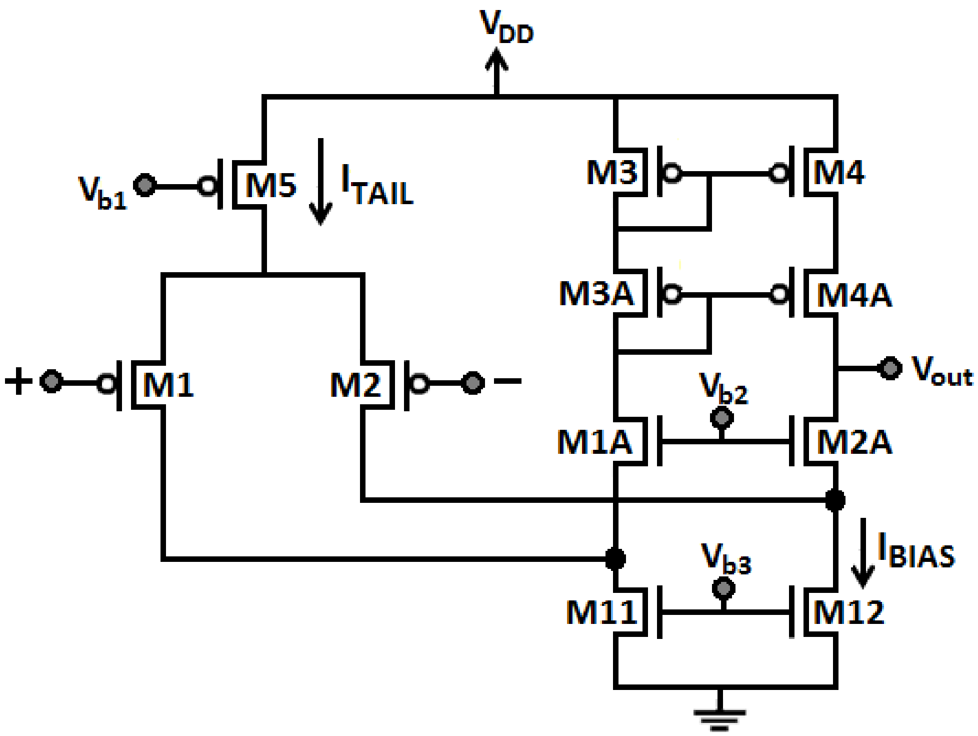


Figure 4.4: Circuit schematic for general folded-cascode amplifier.

amplifier $A_v$ is given by the following simplified expression

$$A_v \approx g_{m1}[g_{m2A}r_{o2A}(r_{o2}||r_{o12})]||[g_{m4A}r_{o4A}r_{o4}] \tag{4.4}$$

where $g_{mx}$ and $r_{ox}$ is the small-signal transconductance and output resistance of transistor M$_x$, respectively. The output resistance of each transistor is set by the bias and tail currents applied since $r_o = 1/(\lambda I_D)$, where $\lambda$ is the channel length modulation parameter. For a given current aspect ratio, $g_m 1$ is a function of the $I_{tail}$ as shown by the following expression

$$g_m = \sqrt{\frac{2I_D}{\mu C_{ox}\frac{W}{L}}} = \sqrt{\frac{I_{tail}}{\mu C_{ox}\frac{W}{L}}}. \tag{4.5}$$

The remainder of this section will summarize the specifications of each amplifier in the TIA and the design decisions required to meet them. A simulation of the open-loop frequency response and differential transfer characteristic curve are provided for each amplifier under the load conditions defined by the TIA architecture. The design of the output buffer used to drive signals off chip is also discussed.

### 4.3.1 Design of Amplifier $A_1$

In general $A_1$ must have sufficient gain to drive the transconductor feedback system. This has implications for the overall transimpedance, bandwidth and stability of the TIA. In order to determine the specifications for $A_1$ Eq. (4.1) can be approximated as

$$H(s) \approx -M^2 R_a \frac{sR_2C_2}{1+sR_2C_2}\left(1+\left[\frac{MR_a}{R_b}\right]\left[\frac{1+sMR_b[C_p(1+A_{1_0})+C_{in}]}{A_{1_0}}\right]\right)^{-1}, \qquad (4.6)$$

where $A_{1_0}$ is the open-loop DC gain of amplifier $A_1$ and $A_2(s)$, $A_3(s)$, and $A_4(s)$ are assumed to be large and $C_{in}$ is the parasitic capacitance at the input of the TIA as shown in Figure 4.1. From Eq. (4.6) it is evident that $C_{in}$ forms an additional pole with resistor $MR_b$. However, this pole can be shifted to very high frequencies if

$$A_{1_0} >> \frac{C_{in}}{C_p} \qquad (4.7)$$

where $C_p$ is the parasitic capacitance between the input and output nodes. It is reasonable to assume that $C_{in}$ will be on the order of tens of pA and $C_p$ on the order of hundreds of fA. As a result $A_1$ must be designed with a DC gain of at least 60 dB in order to regulate the input node at $V_{GND}$.

Using the assumption made in Eq (4.7) and assuming a single-pole roll-off model where $A_1(s) = A_{1_0}/(1+s/\omega_{1_0})$, Eq. (4.6) becomes,

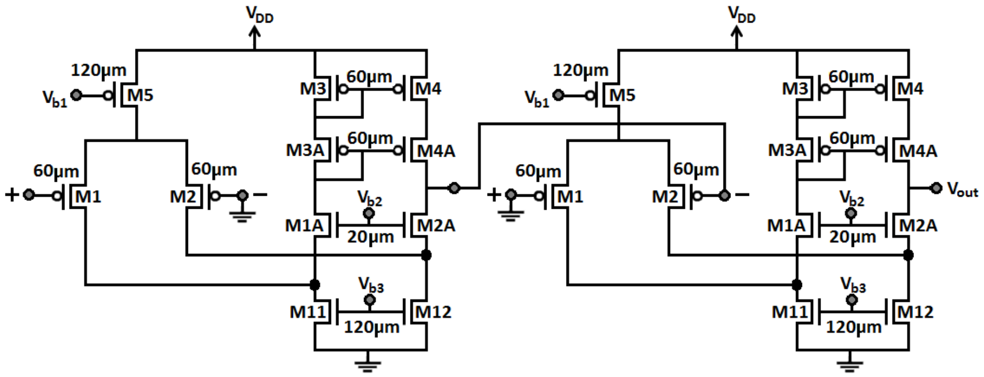
$$H(s) \approx -M^2 R_a \frac{sR_2C_2}{[1+sR_2C_2][1+s(M^2R_a)C_p]}\left(\left[1+\frac{MR_a}{A_{1_0}R_b}\right]\left[1+s\frac{C_p+C_{in}}{A_{1_0}\omega_{1_0}C_p}\right]\right)^{-1}, \qquad (4.8)$$

where $A_{1_0}\omega_{1_0}$ is the GBP of amplifier $A_1$. The above equations illustrates two additional constraints on $A_1$. First, the coefficient $[1 + (MR_a)/(A_{1_0}R_b)]^{-1}$ attenuates the mid-band gain of $H(s)$ and, therefore, $A_{1_0} >> MR_a/R_b$. Given that $M = 150$, $R_a = 50\text{k}\Omega$, and $R_b = 10\text{k}\Omega$, $A_{1_0} >> 750$ V/V. Having already constrained $A_{1_0}$ to a minimum of 60 dB (1000 V/V) this condition is redundant. Second, Eq. (4.8) shows an additional high-frequency pole $f_3 = A_{1_0}\omega_{1_0}C_p/2\pi(C_p + C_{in})$. As this is the third pole of $H(s)$, the TIA may be vulnerable to instability. In order to ensure stability, $f_3$ must lie at least three decades above $1/(2\pi M^2 R_a C_p)$, at approximately 1.5 MHz. Therefore the minimum specified GBP of $A_1$ is 10 MHz. The stability of the TIA is discussed further in Section 4.4.

Figure 4.5 shows the schematic diagram for $A_1$ with the corresponding transistor widths. All transistor channel lengths are 1 $\mu$m to reduce short-channel effects. Amplifier $A_1$ is implemented using two identical folded-cascode amplifiers in cascade, $A_{1a}$ and $A_{1b}$, each with a DC gain of 70 dB and GBP of approximately 128 MHz. Therefore, the total DC gain of $A_1$ is 140 dB while the GBP of $A_1$ only increases slightly to 156 MHz. In this way, sufficient loop gain is provided to regulate the virtual ground at the TIA input while ensuring stability of the system.

Bias transistors M11 and M12 are at least twice as wide as any other transistor in the signal path in order to sink high DC current and push out the 3-dB bandwidth of the open-loop response. Figure 4.6 and 4.7 show the open-loop frequency response of amplifiers $A_{1a}$ and $A_1$ respectively. The widths of M1A and M2A are reduced in order to minimize the capacitance at the high-impedance output node, thereby boosting the 3-dB bandwidth.

Maximizing the voltage swing was not a priority for the design of $A_1$. The non-inverting integrator at the output of $A_1$ ensures low-frequency input signal suppression and regulates the output voltage of $A_1$ at mid-rail 1.65 V. The maximum input signal current expected is 1 nA. With a transimpedance of 1 G$\Omega$, the required voltage swing at the output is only



V_DD
120μm
V_b1
M5
60μm
+
M1
60μm
M2
−
M3
60μm
M4
M3A
60μm
M4A
V_b2
M1A
20μm
M2A
V_b3
M11
120μm
M12
V_DD
120μm
V_b1
M5
60μm
+
M1
60μm
M2
−
M3
60μm
M4
M3A
60μm
M4A
V_out
V_b2
M1A
20μm
M2A
V_b3
M11
120μm
M12

Figure 4.5: Circuit schematic for amplifier $A_1$ with channel widths specified. All transistors have a channel length of 1 $\mu$m.

1 V. $A_1$ supplies an output voltage swing of 1.0 V as shown by the differential voltage transfer characteristic of amplifier $A_1$ Figure 4.8.

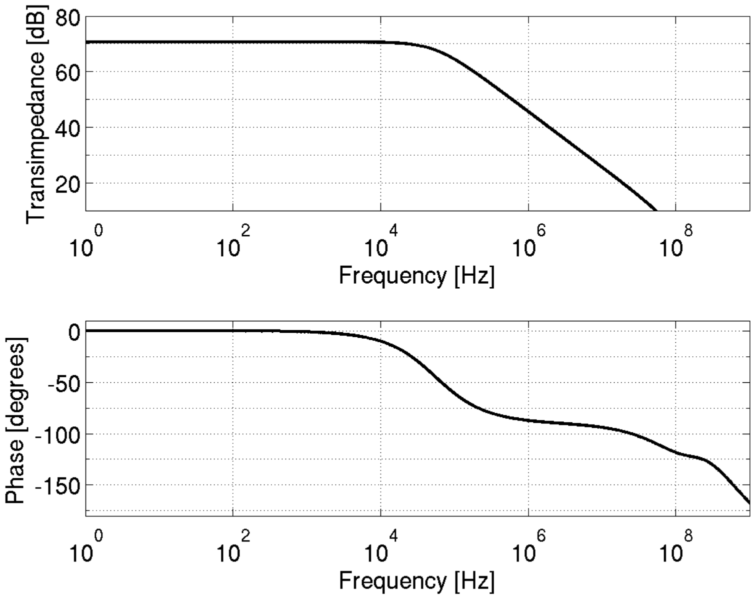


Figure 4.6: Open-loop frequency response of amplifier $A_{1a}$.

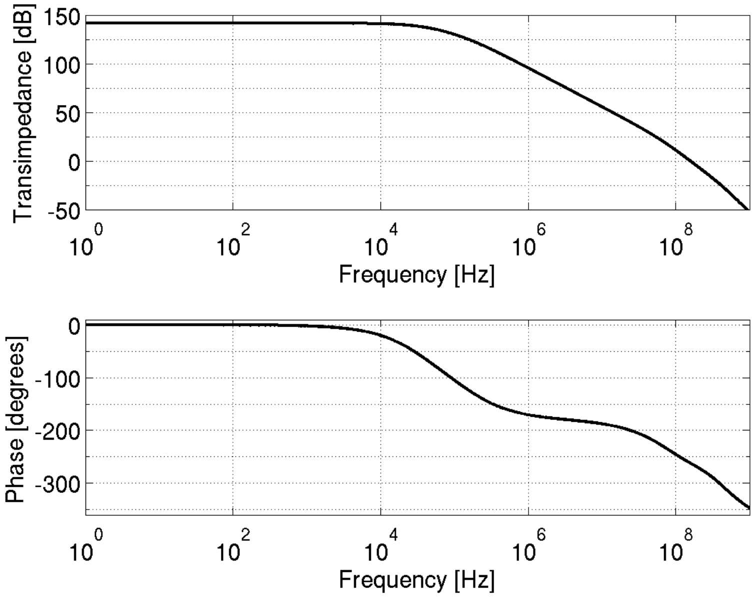


Figure 4.7: Open-loop frequency response of amplifier $A_1$.

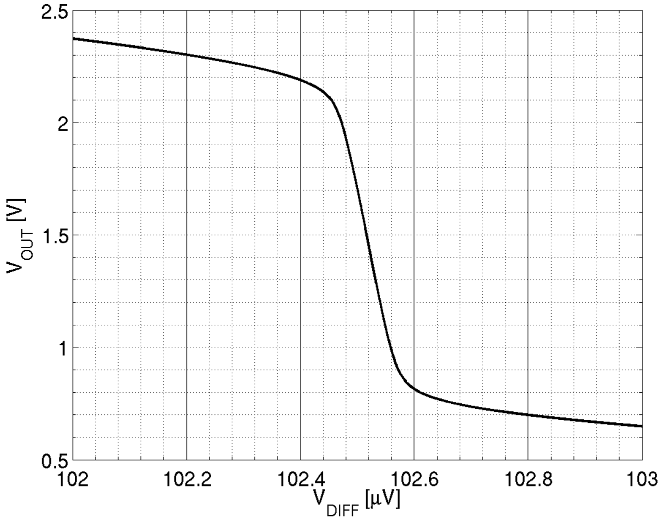


Figure 4.8: Differential voltage transfer characteristic of amplifier $A_1$.

### 4.3.2 Design of Amplifier $A_2$

Amplifier $A_2$ is the core of the non-inverting integrator in the TIA feedback loop used for low-frequency input signal suppression. As before, the specifications of $A_2$ can be identified by re-examining Eq. (4.1). Defining the low-frequency cutoff $f_L = 1/(2\pi R_2 C_2)$, becomes Eq. (4.1)

$$H(s) \approx -\frac{M^2 R_a}{A_{2_0}} \frac{1 + sA_{2_0}/(2\pi f_L)}{1 + s/2\pi f_L} \frac{1}{1 + s(M^2 R_a)C_p}. \tag{4.9}$$

where $A_{2_0}$ is the open-loop DC gain of amplifier $A_2$ and $A_1$, $A_3$, and $A_4$ are assumed to be large. As described in Section 3.3, $A_2$ operates in open-loop for frequencies below $f_L$ and in unity feedback at frequencies above $f_L$. Therefore, the attenuation of the DC currents is directly proportional to the open-loop DC gain of $A_2$ and should be maximized. Additionally, $A_2$ must also be unity-gain stable with a phase margin (PM) of at least 60 degrees. At the same time, $A_2$ drives the internal node $V_x$ which is prone to saturation. Therefore, the output voltage swing of $A_2$ controls the amount of DC current that the TIA can sink or source and must be maximized.

Figure 4.9 shows the schematic for amplifier $A_2$ which consists of three stages: a PMOS input cascode stage, source follower, and PMOS common-source (CS) amplifier. The source follower is used to provide a voltage rise between the cascode output and the gate input of the CS to ensure that this stage operates in saturation. It is sized to reduce the CS overdrive voltage thereby enhancing the output swing. The CS stage contributes extra gain and is also sized to drive the resistive load $R_a$. Transistors M1 and M2 have a width of 10 $\mu$m in order to reduce the capacitance at the output node. By Eq. (4.4) and (4.5), reducing the widths of input devices M1 and M2 (while keeping $I_D$ and $V_{ov}$ constant) increases $g_{m1}$ and $g_{m2}$ and by extension the total voltage gain of the cascode stage.

Miller compensation capacitor $C_z$ is used to separate the poles generated at the output

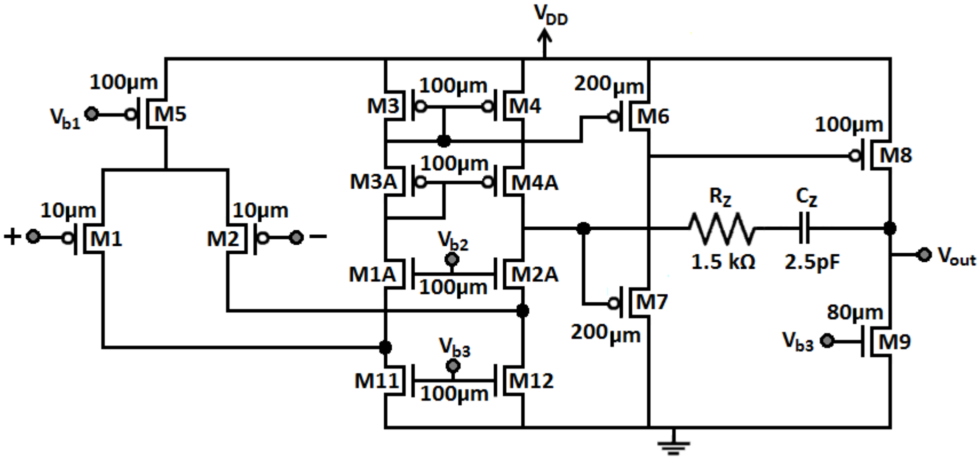

VDD
100μm
Vb1
M5
M3
100μm
M4
200μm
M6
100μm
M8
M3A
100μm
M4A
Rz
Cz
10μm
+
M1
10μm
M2
−
Vb2
M1A
100μm
M2A
1.5 kΩ
2.5pF
Vout
M7
200μm
80μm
Vb3
M9
Vb3
M11
100μm
M12

Figure 4.9: Circuit schematic for three-stage amplifier $A_2$ with channel widths specified. All transistors have a channel length of 2 $\mu$m.

of the cascode and CS amplifiers. However, the zero introduced by $C_{gs8}$ is moved to lower frequencies as a result of the parallel addition of $C_z$. Resistor $R_z$ (implemented using the p+ diffusion layer) is sized such that $R_z = 1/g_{m8}$ in order to move the zero to very high frequencies. Setting $C_z = 2.5$ pF and $R_z = 1.5$ k$\Omega$ yields a phase margin of 68 degrees.

The DC gain of $A_2$ is 100 dB to ensure the attenuation of DC signals between $V_x$ and $V_{out}$. The amplifier gain is enhanced due to the increased output resistance provided by 2-$\mu$m-channel-length devices in the cascode stage. The 3-dB bandwidth of $A_2$ is 56 Hz to ensure this amplifier remains stable under unity-feedback operation. Figure 4.10 shows the open-loop frequency response of amplifier $A_2$. The output voltage swing of $A_2$ is 3.03 V as indicated by Figure 4.11 shows the differential voltage transfer characteristic of amplifier $A_2$.

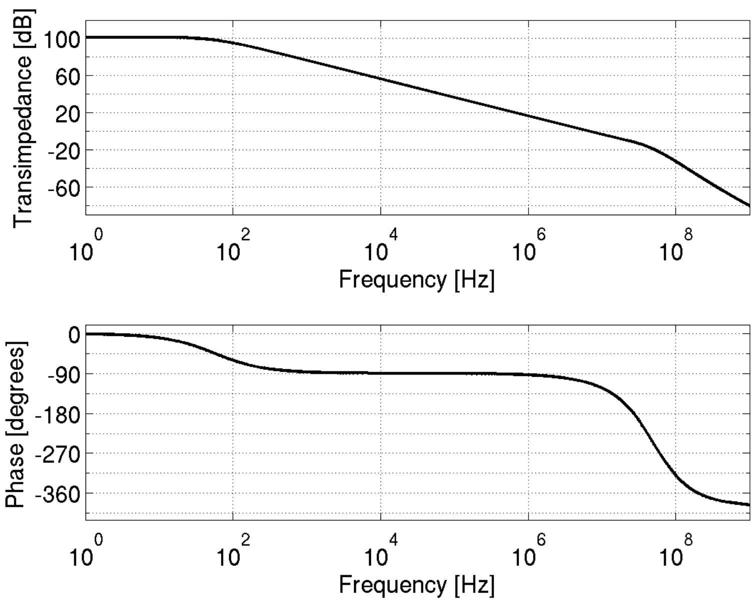


Figure 4.10: Open-loop frequency response of amplifier $A_2$.

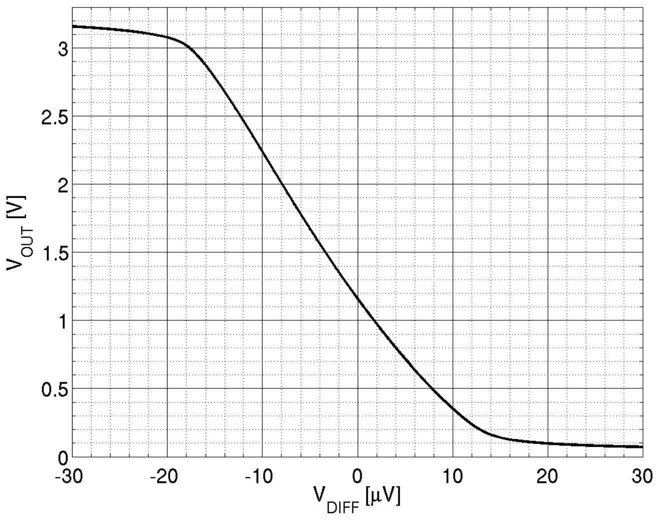


Figure 4.11: Differential voltage transfer characteristic of amplifier $A_2$.

### 4.3.3 Design of Amplifier $A_3$ and $A_4$

The specifications for amplifiers $A_3$ and $A_4$ are not demanding. Analyzing Eq. (4.1) gives the following conditions

$$A_{3_0} >> \frac{R_b}{R_a} \text{ and } A_{4_0} >> 1, \tag{4.10}$$

where $A_{3_0}$ and $A_{4_0}$ are the open-loop DC gains of $A_3$ and $A_4$ respectively. Given $M = 150$, $R_a = 50$ kΩ, and $R_b = 10$ kΩ, $A_{3_0} >> 0.2$ and $A_{4_0} >> 1$ which is easily achieved using a folded cascode.

Amplifiers $A_3$ and $A_4$ have an identical folded-cascode input stage. Amplifier $A_3$ also includes an output stage to drive $R_b$. However, $A_4$ does not require an output stage because it only has to deliver nA-level currents or less. Figures 4.13 and 4.14 show the open-loop frequency response of amplifiers $A_3$ and $A_4$, respectively. Figures 4.15 and 4.16 show the differential voltage transfer characteristic of amplifiers $A_3$ and $A_4$, respectively.

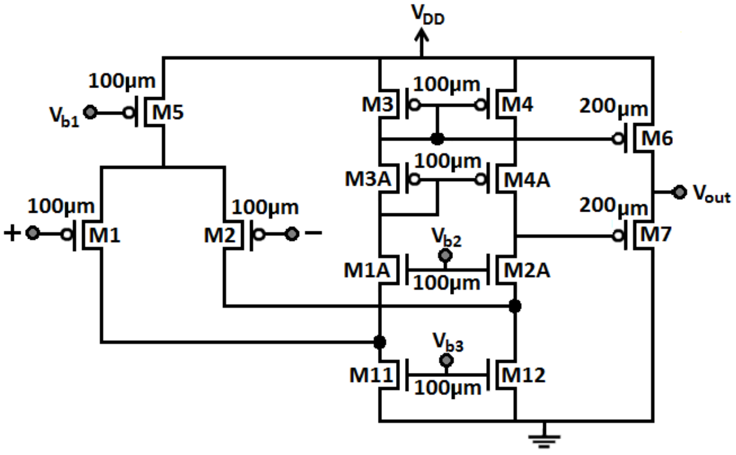

V_DD
100μm
V_b1
M5
M3
100μm
M4
200μm
M6
M3A
100μm
M4A
V_out
100μm
+
M1
100μm
M2
−
200μm
M7
V_b2
M1A
100μm
M2A
V_b3
M11
100μm
M12

Figure 4.12: Circuit schematic for cascode amplifier $A_3$ with output buffer stage. Amplifier $A_4$ is identical except without the buffer stage composed of M6 and M7. Channel widths are specified. All transistors have a channel length of 1 $\mu$m.

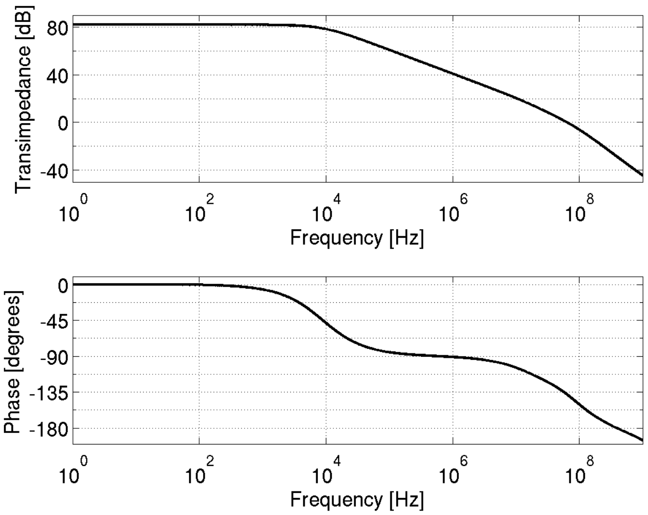


Figure 4.13: Open-loop frequency response of amplifier $A_3$.

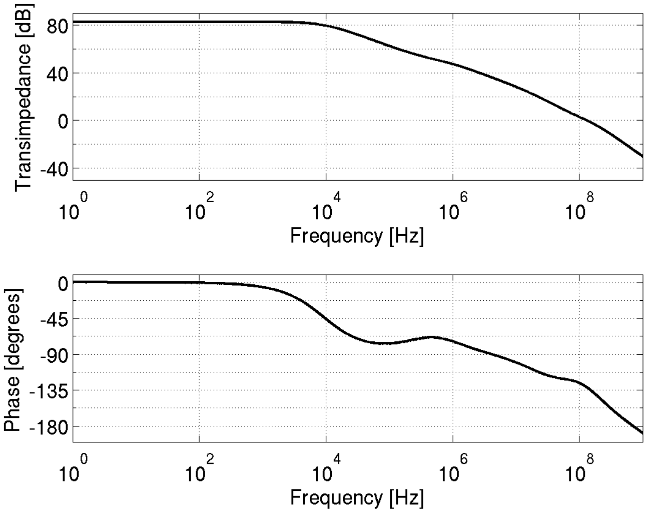


Figure 4.14: Open-loop frequency response of amplifier $A_4$.

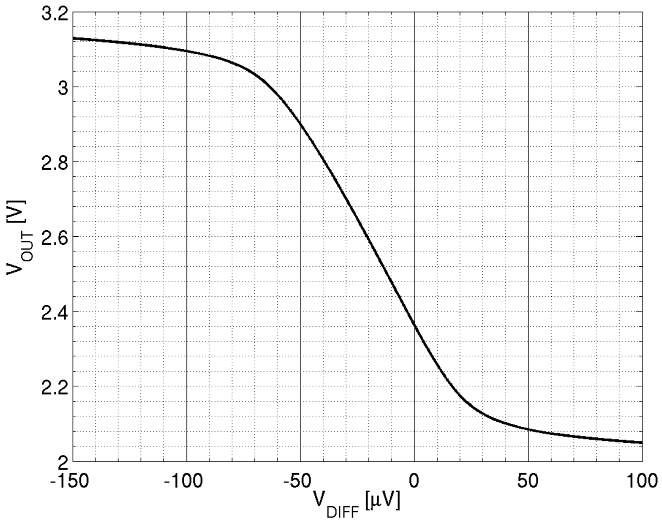


Figure 4.15: Differential voltage transfer characteristic of amplifier $A_3$.

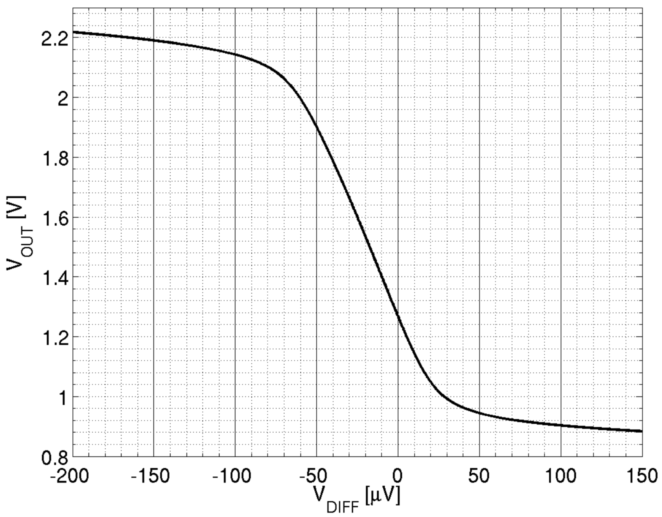
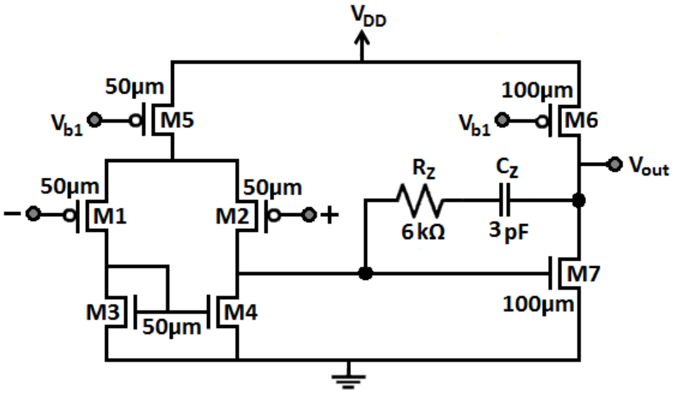


Figure 4.16: Differential voltage transfer characteristic of amplifier $A_4$.

### 4.3.4 Output Buffers

Two identical unity-gain buffers are used to reduce loading effects at $V_{out}$ and $V_x$ presented by the I/O pads and other off-chip elements. A standard two-stage op amp, consisting of a differential amplifier with current mirror load first stage and CS amplifier second stage is used as shown in Figure 4.17. As with amplifier $A_2$, $C_z$ and $R_z$ are used for Miller compensation in order to achieve unity-gain stability with a phase margin of 63 degrees. Figure 4.18 shows the open-loop frequency response given a 50 pF capacitor load.



VDD
50µm
Vb1
M5
100µm
Vb1
M6
Vout
Rz
Cz
50µm
M1
−
50µm
M2
+
6kΩ
3pF
M7
100µm
M3
50µm
M4

Figure 4.17: Circuit schematic for two-stage amplifier used for unity-gain feedback buffers at TIA output nodes $V_{out}$ and $V_x$. All transistors have a channel length of 1 $\mu$m.

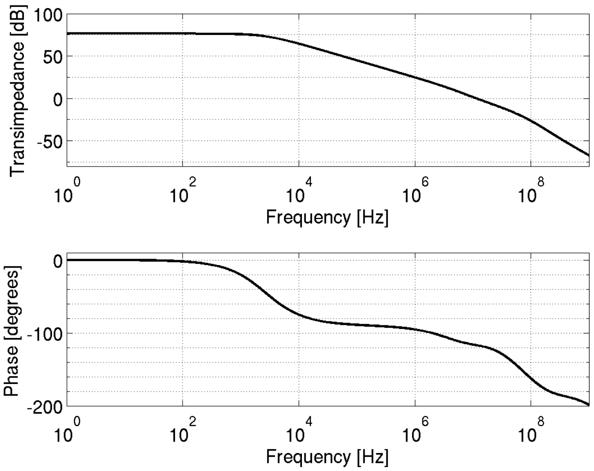


Figure 4.18: Open-loop frequency response of unity-gain buffer.

### 4.3.5 Bias Circuit

The bias circuit architecture shown in Figure 4.19 is used for amplifiers $A_1 - A_4$. A PMOS current mirror is used since all folded cascodes have a PMOS differential input. Transistor Mb1 is loaded with two diode-connected NMOS transistors, Mb2 and Mb3, which provide the bias voltages $V_{b2}$ and $V_{b3}$. Transistor Mbias and variable off-chip resistor (potentiometer) $R_{bias}$ are used to set the current that will be mirrored over to Mb1 and M5 of the associated cascode (or two stage) amplifier to provide the appropriate tail current, $I_{tail}$. According to Eqs. (4.4) and (4.5), increasing the tail current increases the $I_D$ through the input PMOS devices and thus increases the transconductance and overall cascode gain.

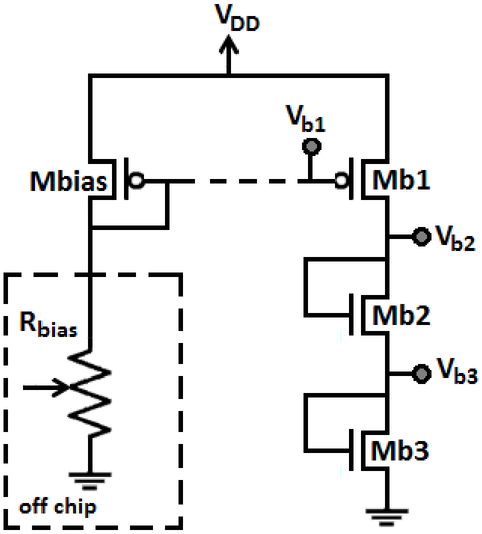


Figure 4.19: Current mirror circuit used to bias cascode amplifiers $A_1$, $A_2$, $A_3$, and $A_4$

The dotted line between transistors Mbias and Mb1 is used to illustrate the substantial distance that may exist between their associated gates. Mbias is kept in close proximity to the pad that will drive $R_{bias}$ while the physical layout of Mb1 is interleaved with M5 of the associated amplifier. Metal traces and vias exhibit a sheet resistance and, therefore, the voltage along a long trace may vary as a result of the current that flows. However, this arrangement of transistors ensures that the voltage set by $R_{bias}$ at the gate of Mbias is the same at the gate of Mb1 since the current through the trace connecting the gates is negligible. If Mbias had been interleaved along with Mb1 where the amplifier is located, and the trace between the drain of Mbias and $R_{bias}$ were extended, the voltage difference between the $R_{bias}$ pad and the gates of Mbias and Mb1 could be several milli-volts. Transmitting a the gate voltage rather than the drain current reduces this discrepancy.

The unity-gain buffer amplifiers only require a single bias voltage for the tail current. In this case, transistors Mb1, Mb2, and Mb3 in Figure 4.19 are not required and only Mbias and $R_{bias}$ are used. Table 4.2 specifies the transistor dimensions used for each amplifier.

Table 4.2: Aspect ratio of bias transistors for each amplifier. All dimensions in $\mu$m.

| Amplifier | Mbias | Mb1 | Mb2 | Mb3 |
|---|---|---|---|---|
| $A_1$ | 100/1 | 120/1 | 50/1 | 100/1 |
| $A_2$ | 100/2 | 120/2 | 50/2 | 100/2 |
| $A_3$ | 100/1 | 120/1 | 50/1 | 100/1 |
| $A_4$ | 100/1 | 120/1 | 50/1 | 100/1 |
| $A_{buff}$ | 100/1 | – | – | – |

### 4.3.6 Summary

Table 4.3 summarizes the simulated performance of each amplifier used in the TIA under typical process corners.

Table 4.3: Simulated performance of individual amplifiers in TIA.

| Parameter | $A_{1a}/A_{1b}$ | $A_2$ | $A_3$ | $A_4$ | Buffer |
|---|---|---|---|---|---|
| Architecture | folded cascode | 3-stage | folded cascode 2-stage | folded cascode | 2-stage |
| Open-loop DC gain (dB) | 70 | 100 | 82 | 83 | 76 |
| 3-dB bandwidth (Hz) | 5600 | 56 | 1130 | 1020 | 2660 |
| Phase margin (deg) | 59 | 68 | 46 | 40 | 63 |
| Load capacitance (pF) | 0.3 | 1 | - | - | 50 |
| Load resistance (kΩ) | - | 50 | 1500 | - | – |
| Power (mW) | 1.38 | 1.11 | 1.85 | 1.18 | 0.988 |
| Output swing (V) | 1.0 | 3.03 | 1.3 | 1.3 | 3.27 |

## 4.4 Stability

From the transfer function of the TIA given in Eq. (4.1), the loop-gain of the system, $A\beta$, is given by

$$A\beta = \left[\frac{A_1(s)}{1+sMR_b[C_p(1+A_1(s))+C_{in}]}\right]\left[\frac{A_4(s)}{1+M(1+A_4(s))}\right]\left[\frac{A_3(s)R_b}{R_a(1+A_3(s))+R_b}\right]\left[\frac{(1+sR_2C_2)A_2(s)}{1+(1+A_2(s))sR_2C_2}\right]. \quad (4.11)$$

In order to simplify the analysis, $A_3$ and $A_4$ are assumed to be very large and the loopgain becomes,

$$A\beta = \frac{R_b}{MR_a}\left[\frac{A_1(s)}{1+sMR_b[C_p(1+A_1(s))+C_{in}]}\right]\left[\frac{(1+sR_2C_2)A_2(s)}{1+sR_2C_2(1+A_2(s))}\right]. \quad (4.12)$$

From the above expression, the poles and zeroes of the loop-gain are evident. The phase shift injected by the pole associated with the $R_2C_2$ time constant have a canceling effect. This zero will always be five decades above the pole as a result of $A_{2_0} = 100$ dB ($= 10^5 V/V$).

Figure 4.20 shows the loopgain magnitude and phase of the TIA as $R_2$ is varied using $V_{ctrl}$. As $V_{ctrl}$ decreases, $R_2$ decreases, and the pole and zero move to to higher frequencies. The phase margin is approximately $90^O$ for $V_{ctrl} = 1.20V$ or higher. If $V_{ctrl}$ is decreased to the extent that $1/(R_2C_2)$ ¿ $1/(MR_bA_{1_0}C_p)$ then the system will become unstable.

## 4.5 System Simulation

The entire TIA in Figure 4.1, including the buffers (not shown), was simulated in Cadence Spectre. Figure 4.21 shows the transimpedance magnitude with variable low-frequency cutoff as set by $V_{ctrl}$. As $V_{ctrl}$ increases, the low-frequency pole moves closer to zero. Signal frequencies below the pole set by $V_{ctrl}$ are attenuated by 100 dB, the open-loop gain of $A_2$, at which point the gain rises at a constant slope of 20 dB/decade. The pass-band gain is 180 dB which is equivalent to a 1 GΩ transimpedance indicating that the effective output resistance of the transconductor is in fact $1/G_m = M^2R_a$. We estimate $C_p$ to be on the order of 100 fF. This leads to a high-frequency cutoff of approximately 1 kHz.

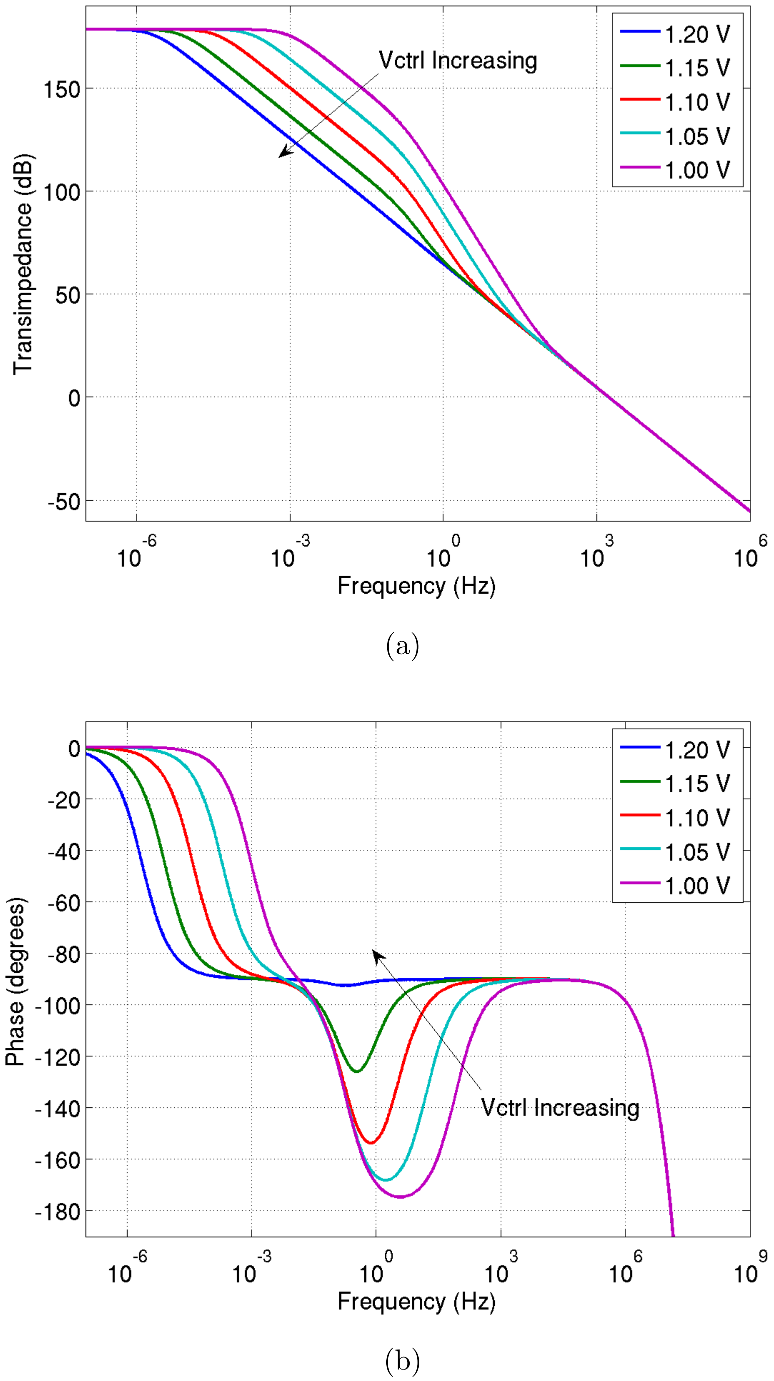


Figure 4.20: Loop gain magnitude (a) and phase (b) of the system shown in Figure 4.1 for various values of $V_{ctrl}$

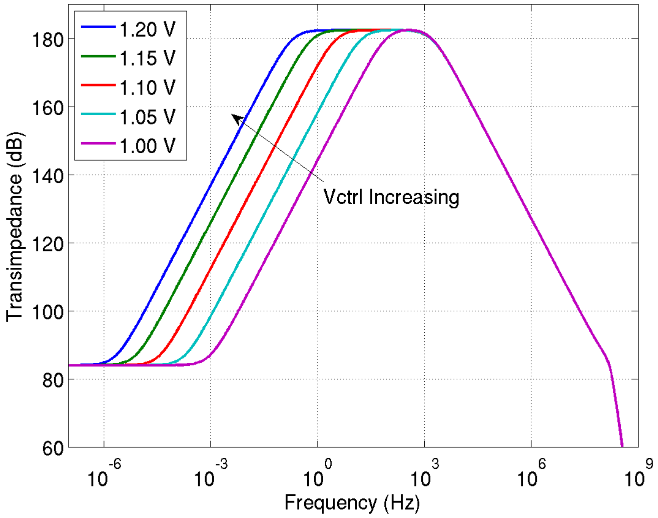


Figure 4.21: Transimpedance magnitude of the system shown in Figure 4.1 for various values of $V_{ctrl}$.

# Chapter 5

# Experimental Results

The TIA has been implemented in a five-metal, two-poly, 3.3-V 0.35-$\mu$m CMOS process. The fabricated chip is shown in Figure 5.1 where the TIA occupies an area of approximately 0.68 mm$^2$. The input node of the TIA is tied to a pin and the input signal current is supplied

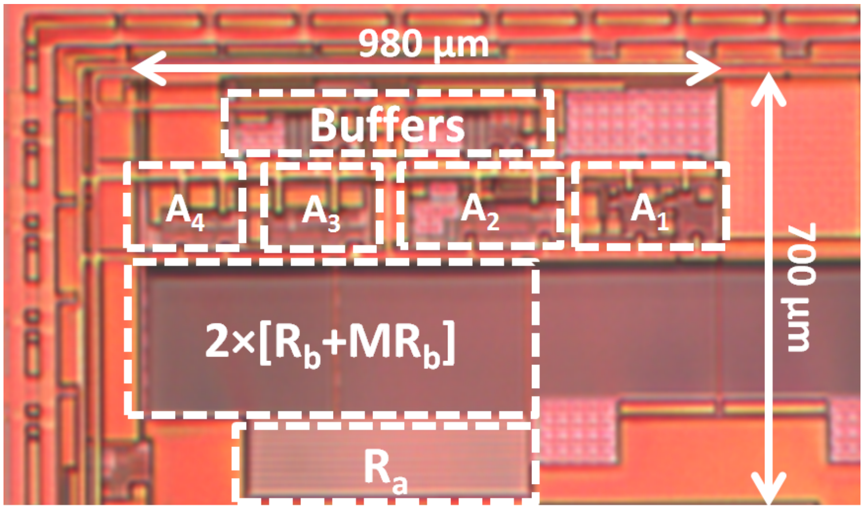

980 µm
Buffers
A4
A3
A2
A1
700 µm
2×[Rb+MRb]
Ra

Figure 5.1: Chip photo showing key TIA components.

by an off-chip current source to test the chip.

## 5.1 Test Apparatus

Generating the low currents required to test the proposed TIA is non-trivial given that its transimpedance is on the order of GΩ. Figure 5.2 shows the circuit schematic of the external discrete-component current source used to test the TIA. The current source operates by applying voltage $v_IN$ across a large resistor $R$ to generate the test current.

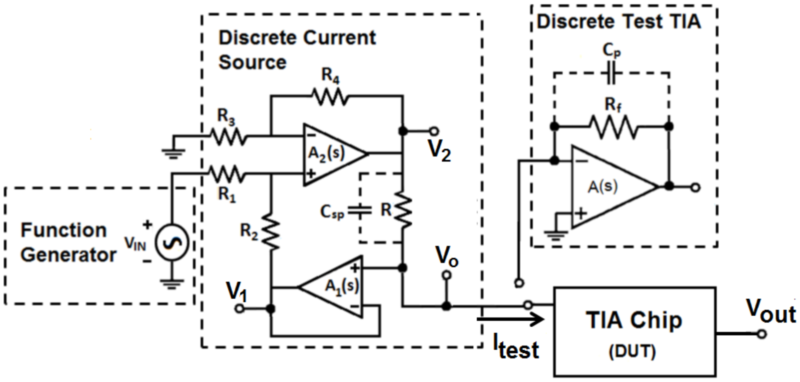

Discrete Current Source
R₄
R₃
R₁
A₂(s)
V₂
Cₛₚ
R
R₂
V₁
A₁(s)
Vₒ
Function Generator
V_IN
Discrete Test TIA
Cₚ
R_f
A(s)
I_test
TIA Chip
(DUT)
V_out

Figure 5.2: Discrete current source used to provide a controllable current to the TIA under test. A discrete TIA to calibrate current source is also shown.

The transconductance of the current source $I_{test}/V_{in}$ can be found by first applying nodal analysis at $V_1$ and $V_2$ yields,

$$I_{test}R\frac{[1+A_2(s)]R_3+R_4}{A_2(s)(R_3+R_4)} = \left[\frac{A_1(s)}{1+A_1(s)}\frac{R_1}{R_1+R_2} - \frac{[1+A_2(s)]R_3+R_4}{A_2(s)(R_3+R_4)}\right] V_o + \frac{R_2}{R_1+R_2}V_{in}. \quad (5.1)$$

The output voltage node $V_o$ is regulated at virtual ground, $V_{GND}$ by the TIA, which is buffered by op amp $A_1$ to node $V_1$. If $A_1$ does not supply ample gain, or if $V_o$ is not held precisely at $V_{GND}$, then some additional current will flow as a result of the $V_o$ term. Otherwise Eq. (5.1) simplifies to,

$$\frac{I_{test}}{V_{in}} \approx \frac{1}{R}\frac{R_2}{(R_1+R_2)R_3}\left[\frac{R3+R_4}{1+\frac{s}{\omega_0 A_{2_0}}\frac{R_3+R_4}{R_3}}\right], \tag{5.2}$$

where the response of amplifier $A_2$ has been approximated such that $A_2(s) = A_{2_0}/(1+s/\omega_0)$, where $A_{2_0}$ is the DC gain of the op amp $A_2$. Eq. (5.3) shows that the bandwidth of the current source is limited by the GBP of $A_2$. Table 5.1 summarizes the specifications of the amplifiers used for the current source in Figure 5.2. The low-input bias current of $A_1$ is highly desirable since $I_{test}$ is on the order of nA or less.

Table 5.1: Specifications for amplifiers used in discrete current source of Fig 5.2.

| | $A_1$ | $A_2$ |
|---|---|---|
| Part Number | LMP7715MF/NOPB | MAX4490AXK+T |
| Supply Voltage | 5.0 V | 5.0 V |
| Gain-Bandwidth Product | 17 MHz | 10 MHz |
| Output Voltage Noise PSD | 5.8 nV/$\sqrt{\text{Hz}}$ | 12 nV/$\sqrt{\text{Hz}}$ |
| Input Bias Current | 100 fA | 50 pA |

Provided that GBP of $A_2$ is sufficient, the relation of output current to input voltage is given by

$$\frac{I_{out}}{V_{in}} \approx \frac{1}{R}\frac{R_2}{R_3}\frac{R_3+R_4}{R_1+R_2}. \tag{5.3}$$

By choosing the resistor values appropriately, the input voltage can be attenuated to supply the desired current to the TIA. Resistors $R_1 - R_4$ are chosen as 10 kΩ while $R = 1$ GΩ such that $I_{out}/V_{in} = 1/R = 1$ GΩ. It is necessary for $R$ to be as large as possible in order to maximize the output resistance of the current source. However, there is a parasitic capacitance $C_{sp}$ associated with R as shown in Figure 5.2 that injects a zero at $1/(2\pi RC_{sp})$. This low-frequency zero makes testing difficult since the zero adds a linear error to all measurements. In order to characterize this behaviour an on-board TIA made of discrete components is implemented as shown in Figure 5.2. Figure 5.3 shows the measured frequency response of the current source when applied to the test TIA. A low-pass filter (LPF) response is expected, however, due to the zero injected by the current source at low frequencies the response is irregular. From this it can be shown that the zero lies at approximately 300 Hz and $C_{sp} \approx 500$ fF. Therefore all measurements from the TIA chip must be post-processed to account for this zero results.

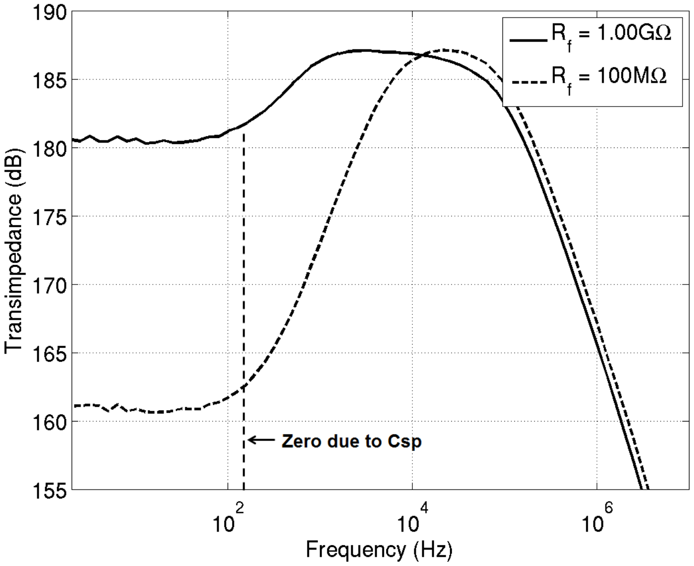


Figure 5.3: Frequency response of the discrete test TIA driven by current source in Figure 5.2.

## 5.2 Measured Results from TIA Chip

### 5.2.1 Frequency Response

Figure 5.4 shows the frequency response of the TIA for different $V_{ctrl}$ values. As $V_{ctrl}$ increases, the resistance of the PMOS active resistor also increases which reduces $f_L$. The measured passband gain of the system is approximately 1.71 G$\Omega$. This is greater than the desired 1 G$\Omega$ transimpedance due to mismatch between resistors $R_b$ and $MR_b$, as well as deviation in $R_a$ due to tolerances inherent in the fabrication process. Input current signals at frequencies below $f_L$ are attenuated at a rate of 20 dB/decade. This decay should continue steadily to a minimum of approximately 84 dB (the passband gain minus the open-loop gain of $A_2$). This is not apparent in the measured data since the output signal drops below the noise floor of the system at very low frequencies. As $V_{ctrl}$ increases from

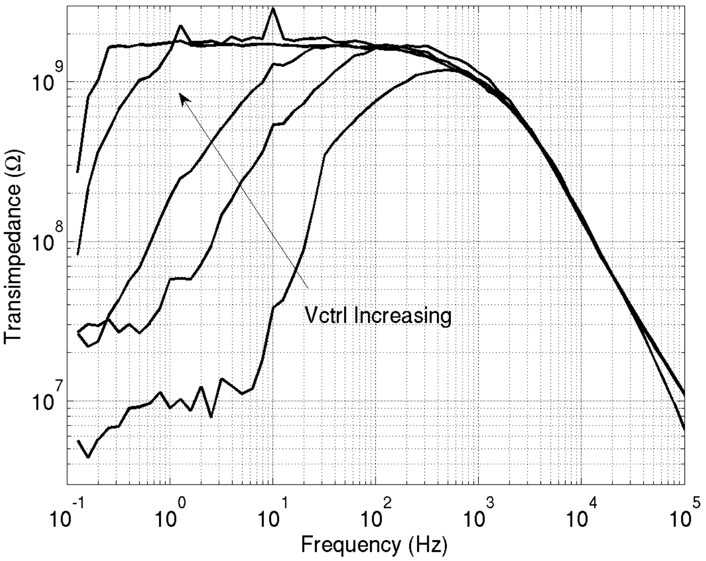


Figure 5.4: Measured transimpedance over frequency with variable low-frequency cutoff.

about 0.85 V to 1.2 V, $f_L$ decreases from 500 Hz to 0.7 Hz. This variation is in agreement with the simulated results in Figure 5.5 where the small discrepancies can be attributed to process variation. The measured high-frequency cutoff of the TIA is approximately 650 Hz. With the measured transimpedance of 1.58 G$\Omega$, $C_p$ is estimated to be 150 fF. For impedance spectroscopy applications requiring higher input signal frequencies, the TIA bandwidth can be increased by effectively reducing $1/G_m$.

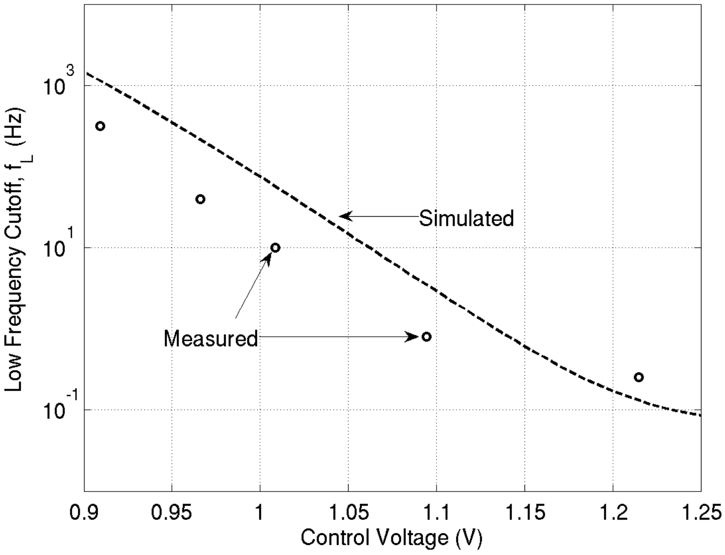


Figure 5.5: Simulated and measured tuning range of the TIA low-frequency cutoff.

### 5.2.2 Linearity

Figure 5.6 shows the ac output voltage as a function of a 200-Hz input current signal to illustrate the TIA linearity. At an input current of approximately 0.8 $\text{nA}_{\text{pp}}$, the output voltage $V_{out}$ begins to saturate. This occurs due to the nonlinear behaviour of the active resistor for large output voltage swings. The slope of the best-fit line to the measured data indicates a transimpedance of approximately 1.79 GΩ before saturation occurs, which is nearly that measured from the frequency response in Figure 5.4. Figure 5.6 also shows that the relative linearity error does not exceed 1.1% over an input current range from 0.2 $\mathrm{nA_{pp}}$ to 0.8 $\mathrm{nA_{pp}}$.

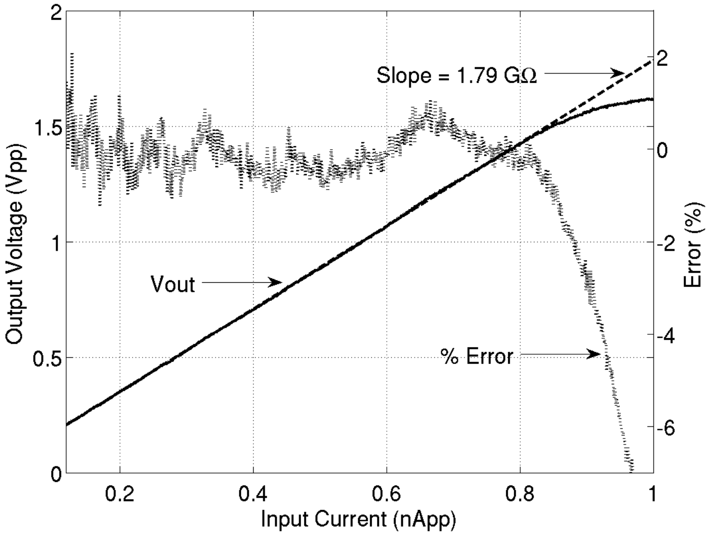


Figure 5.6: Measured relative linearity error of the TIA with an ac input current.

Figure 5.7 shows the measured $V_{out}$ and $V_x$ for positive and negative dc input currents. The $V_x$ output follows the current with a constant slope equal to the transimpedance gain because the low-frequency part of the input signal is not attenuated at this node. The TIA can process a dc current of ±0.9 nA before $V_x$ saturates at the supply rails. However, $V_{out}$ is regulated at the 1.65-V common-mode level over the input current range due to the low-frequency suppression. The slope of the $V_x$ curve in Figure 5.7 represents the DC transimpedance of the system.

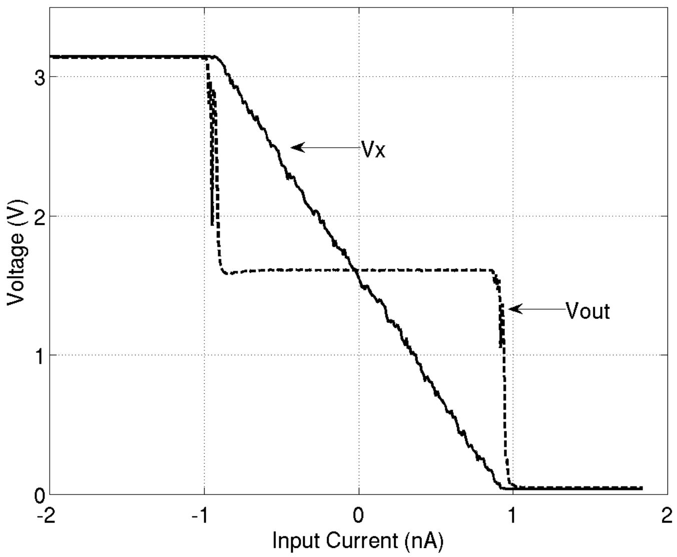


Figure 5.7: TIA output voltage $V_{out}$ and internal node $V_x$ as a function of dc input current.

### 5.2.3 Noise

Figure 5.9 shows the PSD of the input-referred current noise of the TIA. The total integrated noise is 26.7 $\mathrm{pA_{rms}}$ from 1 Hz to 1 kHz and 27.8 $\mathrm{pA_{rms}}$ from 1 Hz to 10 kHz. The thermal noise generated by the feedback transconductor is 10 $\mathrm{pA_{rms}}$ over a 10 kHz bandwidth and accounts for a little more than a third of the total input-referred current noise. The remainder of the noise is likely a result of the flicker noise generated by the input stages of amplifiers $A_1$ and $A_2$. This is supported by the fact that the majority of the noise measured lies at low frequencies within the first 1 kHz bandwidth.

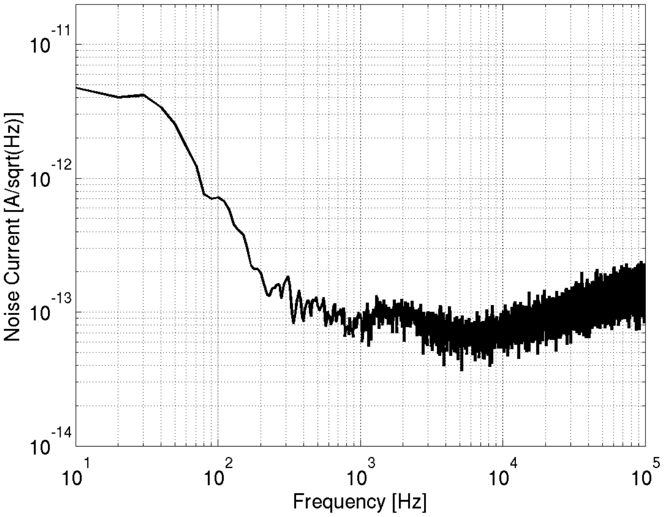


Figure 5.8: Measured input-referred current noise PSD of the TIA.

### 5.2.4 Transient Response

Figure 5.9 shows the output voltage transient of the TIA chip as a result of a step input. A 40 mV input square wave is applied at the input of the discrete current source described in Section 5.1 to generate a 40 pA step input. As a result of the negative feedback of the TIA, sharp drops in the input current correspond to large spikes at the output voltage node. Given enough time the output voltage will settle to virtual ground, at 1.65 V. The settling time of the system is set as a function of the $V_{ctrl}$ which controls the location of the low-frequency pole.

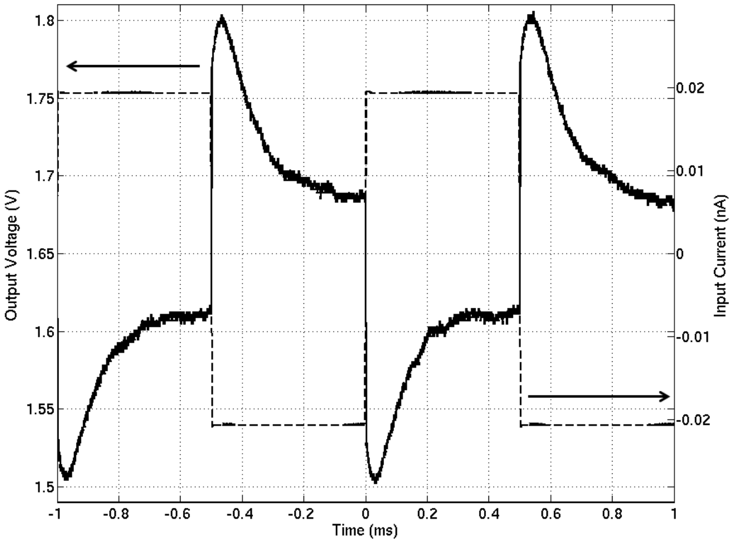


Figure 5.9: Response of the TIA as a result of a 40 pA step input current. The low-frequency cutoff of the TIA has been set to 200 Hz.

## 5.3 Performance Comparison

Table 5.2 tabulates the performance of the work presented in this thesis with that of the four TIA architectures discussed in Chapter 2.

Table 5.2: Summary of performance for various TIA architectures in comparison with the presented work.

| Criteria | RTIA [1] | CTIA [2] | RTIA-PI [24] | CARTIA [30] | This Work |
|---|---|---|---|---|---|
| Supply Voltage | 3.3 V | 3.3 V | – | 3.3 V | 3.3 V |
| CMOS Process | 0.5 $\mu$m | 0.5 $\mu$m | discrete | 0.35 $\mu$m | 0.35 $\mu$m |
| Transimpedance | 25 MΩ | 100 MΩ | 1.2 GΩ | 1.8 GΩ | 1.71 GΩ |
| -3-dB Bandwidth | 10 kHz | [a]10 kHz | 250 Hz | [b]100 Hz | 900 Hz |
| Input DC Current Range | ±1 nA | ±12 nA | ±0.4 nA | ±25 nA | ±0.9 nA |
| Input Referred RMS Noise (10 kHz BW) | 5 pA | 1.35 pA | 0.8 pA | 0.5 pA | 51.8 pA |

[a] Integration time ($T_{int}$) is set to 100 $\mu$s.

[b] Bandwidth of the first stage integrator. With the addition of a second stage differentiator, the bandwidth is extended to 4 MHz while the transimpedance is reduced to 20 MΩ.

# Chapter 6

# Conclusion

A CMOS TIA having a measured gain of 1.58 GΩ suitable for low-current electrochemical biosensors was presented. Use of a feedback transconductor instead of a single linear resistor to achieve high gain results in chip area savings. The TIA suppresses the effect of undesirable low frequency input leakage currents on the output. By using an active resistor in the feedback path, a tunable low-frequency cutoff ranging from 0.7 Hz to 500 Hz is achieved. A test chip was designed, laid out, and fabricated in a 0.35 $\mu$m CMOS process.

## 6.1 Contributions

The TIA topology introduced in this dissertation is unique in several ways. Unlike the classical resistive-feedback TIA, the effect of low-frequency currents on the output voltage is suppressed. Although a capacitive feedback TIAs may provide higher gain for an integrated solution, the TIA presented in this thesis supplies sufficient transimpedance without limiting the measurement time.

The charge-sensitive preamplifier presented in [24] was improved in this thesis by making it more amenable to CMOS integration by implementing subthreshold PMOS pseudo-resistors. These devices enable an adjustable low-frequency cutoff demonstrated in Chapter 4. This additional enhancement also sets this TIA apart from [23]. Though [23] does provide a larger bandwidth, it makes use of an additional differentiator stage. Taking the the first stage integrator of [23] alone, the TIA presented in this thesis offers increased gain, a tunable low-frequency cutoff, and similar bandwidth restrictions.

## 6.2 Future Work

### 6.2.1 Additional Transconductor Stages

The advantages of using a transconductor in feedback may be investigated further. It may be possible to utilize additional transconductor stages in order to further reduce the chip area required to obtain the necessary transimpedance. In this case the multiplication factor $M$ may be reduced. However, care must be taken in order to ensure that the overall feedback of the TIA is negative to avoid issues with stability.

### 6.2.2 Parasitic Capacitance

Further examination is required in order to identify the parasitic capacitance that contributes to $C_p$. It may be possible to reduce $C_p$ and thereby increase the overall bandwidth of the system. However, there will always be a trade-off between gain using the topology presented in this thesis.

## 6.3 Improvements

Several methods to improve the performance of this TIA were noted during the design process. This section will discuss several possible design alternatives that may be incorporated but were not due to time constraints.

### 6.3.1 Reduced Noise

Two methods are now described for reducing the overall noise of the TIA. First, the primary contributor to the input-referred current noise is the thermal noise generated by resistor $MR_b$ as discussed in Section 3.2.1. It may be possible to replace all the $MR_b$ and $R_b$ resistors with subthreshold PMOS devices. The non-linearity of the system may be mitigated using the methods discussed in Section 3.3.1. Using this technique, the thermal noise of $MR_b$ is replaced by the much lower shot noise of the subthreshold devices.

Second, the input PMOS devices of amplifier $A_2$ in Figure 4.9 are likely contributing unnecessarily high flicker noise since they are directly connected to the output node of the TIA. The primary contributors of the flicker noise are the transistors M1 and M2 since they are 10 $mu$m in width. $A_2$ can thus be redesigned to achieve a lower overall input-referred current noise by using non-minimal PMOS area for the input devices.

### 6.3.2 Transimpedance Variation

The precision of the pass-band transimpedance can be improved by addressing the layout of resistors $R_a$, $MR_b$ and $R_b$. P-diffusion resistors were favoured in this design because it accommodated the high resistance and low area restrictions of $R_b$ and $MR_b$. However, these same restrictions do not apply to $R_a$ which is almost two orders of magnitude less than $MR_b$. An n+ diffusion base resistor is a better choice for $R_a$ as its resistance is less dependent on the voltage across it as demonstrated by its reduced voltage coefficients in comparison with the p+ diffusion resistor. As for $R_b$ and $MR_b$, p-diffusion is adequate but the physical layout of these resistors can be improved in the following way. Although $R_b$ and $MR_b$ are already interleaved to avoid error on $M$ due to process variation, the $M$ generated by both stages must also match for $1/G_m = M^2R_a$ to hold true. Since each $MR_b - R_b$ transconductor pair is separate, it is possible that the multiplication factor introduced by the first stage does not match the second. This can be avoided by interleaving both $MR_b - R_b$ pairs within one another.

# APPENDICES

# Appendix A

# Design of PCB for Testing

Supply and reference voltages are generated off chip using a simple discrete voltage divider circuit consisting of resistors $R_c$ and $R_{var}$, capacitors $C_{cer}$ and $C_{tant}$, and unity-gain buffer $A_{buff}$ as shown in Figure A.1. Resistor $R_c$ remains constant at 10 kΩ while $R_{var}$ is a 20 $k\Omega$ potentiometer. By increasing or decreasing $R_{var}$, the output voltage $V_n$ can be increased or decreased. Ceramic and tantalum capacitors, $C_{cer}$ and $C_{tant}$, are used to filter high frequency noise from $V_n$.

Amplifier $A_{buff}$ is used to avoid loading the voltage divider, to buffer the chip from undesirable parasitic capacitance, and to supply the necessary bias current for the chip. An external DC source followed by a low-dropout (LDO) voltage regulator to generate the 5 V rail that is divided down to produce $V_{DD}$.

A voltage divider similar to that of Figure A.1 is also used to set the control voltage $V_{ctrl}$ off chip for low-frequency bandwidth tuning. In this case, $V_{DD} = 3.3V$ is divided down and $R_{var}$ is set to 100 kΩ to provide a wide voltage tuning range.

Figure A.2 shows the pin layout of the TIA chip presented in this thesis. The chip was

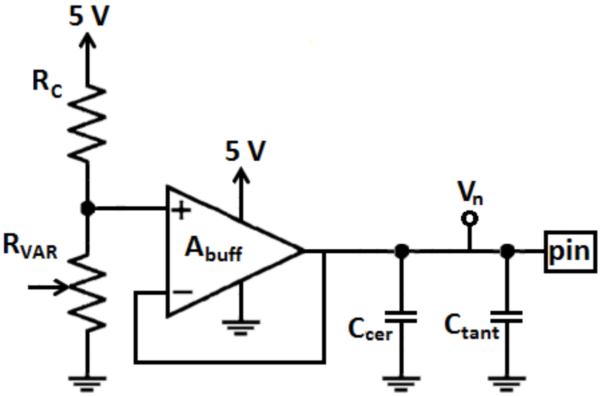


Figure A.1: Discrete voltage divider circuit used to generate off chip voltages.

packaged in the CQFP44A package to be interfaced with the PCB.

Table A.1 maps each of the pins in Figure A.2 to a particular input signal. The package contains two TIAs with separate bias circuits as well as on additional $A_1a$ amplifier for testing.

Figure A.3 shows the circuit schematic of the test board used for testing the fabricated chip.

Figure A.4 shows the physical layout of the test board.

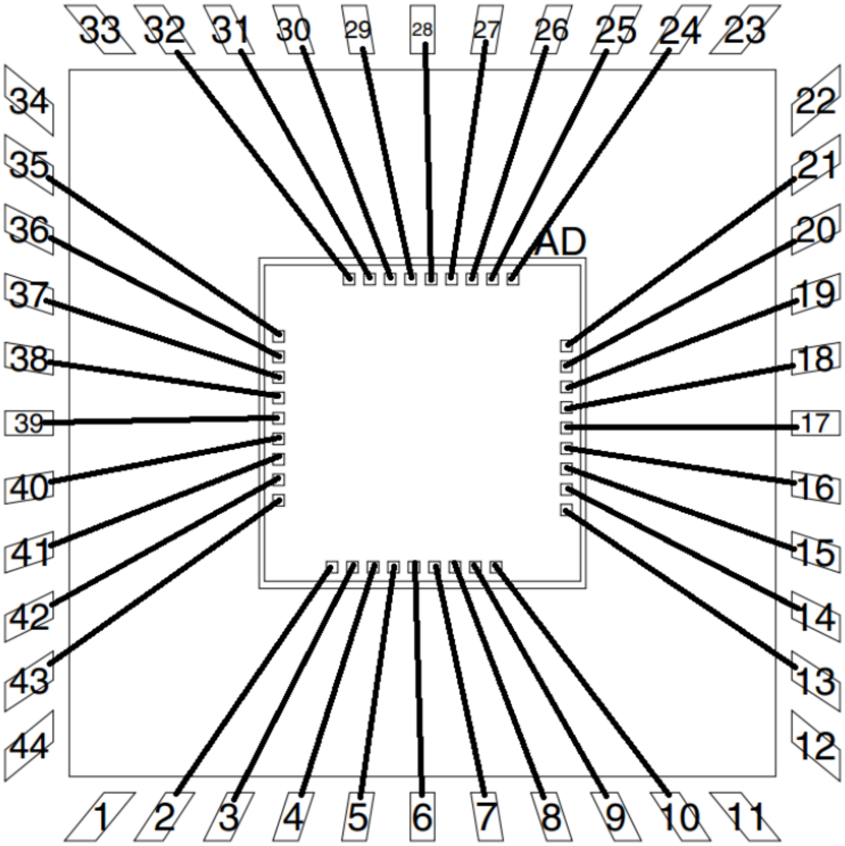

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Figure A.2: Bonding diagram of TIA for CQFP44A package.

Table A.1: Mapping table for chip pins.

| Pin Number | Signal | Pin Number | Signal |
|---|---|---|---|
| 1 | – | 23 | – |
| 2 | vb21 | 24 | vb22 |
| 3 | vb31 | 25 | vb32 |
| 4 | vb41 | 26 | vb42 |
| 5 | vbuff1 | 27 | vbuff2 |
| 6 | avn | 28 | avp |
| 7 | vin1 | 29 | vin2 |
| 8 | vgnd1 | 30 | vgnd2 |
| 9 | vout1 | 31 | vout2 |
| 10 | vnode1 (vx1) | 32 | vnode2 |
| 11 | – | 33 | – |
| 12 | – | 34 | – |
| 13 | vsscore1b | 35 | vsscore2b |
| 14 | vsscore1a | 36 | vsscore2a |
| 15 | vddcore1b | 37 | vddcore2b |
| 16 | vddcore1a | 38 | vddcore2a |
| 17 | vssring1 | 39 | vssring2 |
| 18 | vddring1 | 40 | vddring2 |
| 19 | vst (vctrl) | 41 | avout |
| 20 | vgnda2 | 42 | vgnda1 |
| 21 | vb12 | 43 | vb11 |
| 22 | – | 44 | – |

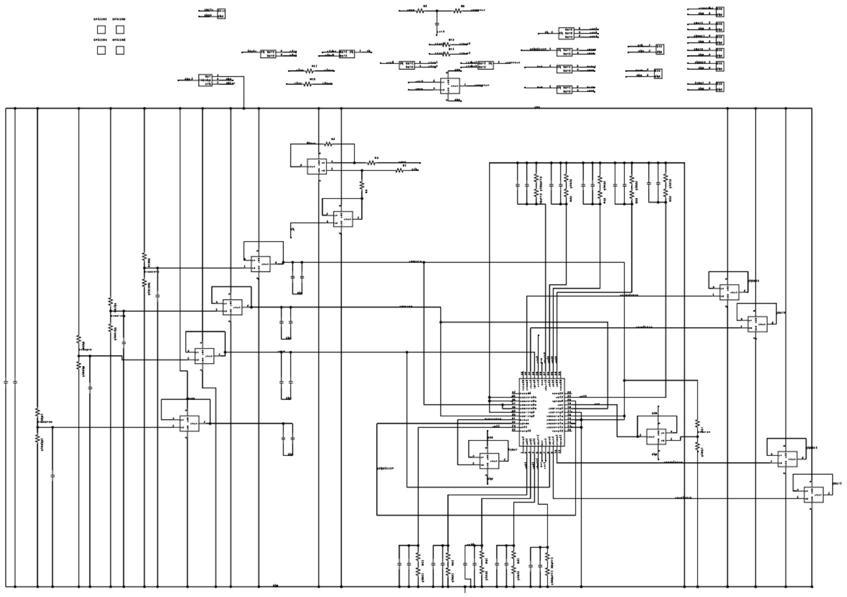
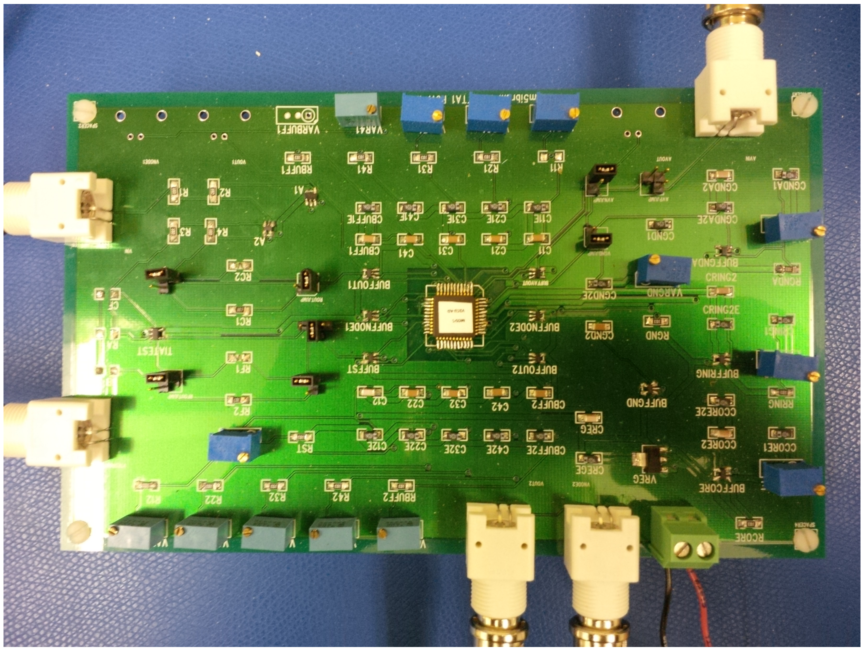


Figure A.3: Test board circuit schematic the fabricated chip.



VARBUFF1
VAR41
RBUFF1
R41
R31
R21
R11
CGNDA2
CGNDA1
CGNDA2E
CBUFF1E
C41E
C31E
C21E
C11E
CBUFF1
C41
C31
C21
C11
CGND1
BUFFOUT1
BUFFNODE1
BUFFNODE2
BUFFST
BUFFOUT2
CGND2
RGND
BUFFGND
BUFFRING
RRING
CRING2
CRING2E
RGNDA
C12
C22
C32
C42
CBUFF2
C12E
C22E
C32E
C42E
CBUFF2E
CREG
CREGE
VREG
CCORE2E
CCORE2
CCORE1
BUFFCORE
RCORE
RST
R12
R22
R32
R42
RBUFF2
RC1
RC2
RF1
RF2
TIATEST
A1
A2

Figure A.4: Physical layout of PCB for testing the fabricated chip.

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