

# Low Temperature Superconducting RF MEMS Devices

by

**Sara Sharifian Attar**

A thesis  
presented to the University of Waterloo  
in fulfillment of the  
thesis requirement for the degree of  
Doctor of Philosophy  
in  
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2014

© Sara Sharifian Attar 2014

## **AUTHOR'S DECLARATION**

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

## Abstract

Superconducting microelectronics technology (SME) has the potential of realizing high speed digital receivers capable of performing direct digitization of radio frequency signals with very low power consumption. An SME receiver is implemented on a single chip using low-temperature superconducting (LTS) Josephson junctions (JJs). The technology provides ultrafast digital switches and logic circuits along with high linearity analog-to-digital converters (ADCs). However, SME technology offers limited choices for realizing reconfigurable analog front-ends. While a tunable inductor using a string of JJs or superconducting quantum interference devices (SQUIDs) can be realized using the SME technology, the main problems with these tuning inductor elements are poor linearity performance and low power handling. RF MEMS technology has the capability to offer highly linear and high power handling tuning elements such as switches and varactors.

To integrate a receiver with radio frequency (RF) front-end on a single chip, MEMS devices need to be fabricated using the same fabrication process as SME technology. In this study, a post-processing technique is developed and optimized to release the MEMS parts of the SME chip while keeping the SME electronics intact. Another challenge is to design MEMS structures that can handle extreme low-temperature working environments. For the first time, superconducting niobium-based RF MEMS dc-contact switches, capacitive-contact switches and varactors are developed employing the SME technology, operating at 4K. The loss in all of the devices is extremely low and the quality factor is quite high when niobium superconducts. The mechanical performance of the MEMS structures are investigated at liquid nitrogen and liquid helium temperatures of 77k and 4K, respectively. The deformation of the MEMS structures and material stiffness at cryogenic temperature are also investigated.

Additionally, more advanced tunable RF circuits are developed, fabricated and characterized, implementing the primary devices. Two types of MEMS capacitor banks are designed, post-processed and characterized using the dc-contact and capacitive-contact RF MEMS switches. The capacitor banks show a very high quality factor at 4K. As well, a single-port-double-throw switch is developed and measured as the building block for switch matrices, showing extremely low insertion loss, and tunable resonators are presented that implement both varactors and dc-contact RF MEMS switches as the tuning elements. The resonators are extremely miniaturized, with a size of  $\lambda_0/1600$ , and tunable filters are developed and characterized using these resonators.

While niobium-based RF MEMS can be integrated within the niobium-layers of the SME technology, designers often do not have the flexibility to select the thickness of the MEMS structural layers. Also, since the fabrication process of SME technology is not specifically designed for MEMS technology, there are limitations in designing more reliable RF MEMS devices. A novel niobium-based micro-fabrication process is developed to integrate gold-based MEMS structures with niobium-based RF circuits. This method benefits from the very low-loss characteristic of superconducting metal niobium while implementing a more matured technology for MEMS structures.

An 8-mask fabrication process is developed that allows the monolithic integration of superconducting niobium-based RF circuits with gold-based MEMS structures. By developing this fabrication method, many low-loss and high quality factor tunable RF devices can be achieved. The challenge is to maintain the quality of the niobium metal layer so that there is no degradation in the critical temperature of the niobium after going through all of the 8-mask process steps. Niobium RF devices integrated with gold-based dc-contact and capacitive-contact RF MEMS switches are fabricated and characterized on alumina substrates using the proposed fabrication process. All devices demonstrate insertion loss reduction due to the superconducting nature of niobium. The measurements of coplanar

waveguide transmission lines and low-pass filters demonstrate that the critical temperature of the niobium metal layer is not degraded during the process steps. A capacitor bank is designed, fabricated and characterized showing a very high quality factor. Finally, two types of niobium tunable bandpass filters are presented that employ gold-based dc-contact RF MEMS switches as the tuning elements.

## Acknowledgements

I would like to express my gratitude to all those who helped me all these years through the graduate schools. Without them it would have not been possible.

I would like to express my deepest appreciation and thanks to my advisor Professor Raafat Mansour, you have been a tremendous mentor for me. I would like to thank you for encouraging my research and for allowing me to grow as a research scientist. Your advice on all aspects of life has been priceless. I will always look up to you as my role model.

I would also like to thank my committee members, Professor Safavi-Naeini, Dr. Majedi and Professor Khajepour for serving as my committee members even at hardship. I would also like to thank Professor Scott Barker from University of Virginia for taking the time to serve as my external examiner. I also want to thank you for letting my defense be an enjoyable moment, and for your brilliant comments and suggestions.

It was a great pleasure for me to work in the Centre for Integrated RF Engineering (CIRFE) with so many talented individuals. I would especially like to thank Bill Jolley, the CIRFE lab manager. He was a great mentor and wonderful friend to me. I won't forget the number of times that I knocked at your door and just saying "Bill, please help! I really need your help!" Special thanks to my dear friend Sormeh Setoodeh, without your great ideas and encouragement I would not be able to accomplish it. I will always remember the exciting moments that we had in the lab while cooling down the chamber and were worried about it not to freeze or we had to start all over again. All the weight lifting and tank moving and nitrogen filling were so fun. The great part was when we got good results and were so excited and screaming and couldn't wait to show the results to Professor Manosur.

I would also like to thank Dr. Siamak Fouldai and Dr. Arash Fomani for being so patient with me while training me in the cleanroom and the RF lab.

I would also like to recognize my colleagues Dr. Nino Zahirovic, Dr. Paul Laforge, Dr. Neil Sarkar, Ahmed Abdel-Aziz, Geoffery Lee, Saman Nazari, Oliver Wong and Scott Chen. I would also like to thank Roger Grant for dicing so many wafers for me.

Finally I would like to thank my family. Words cannot express how grateful I am to my mother and my father for all of the sacrifices that you've made on my behalf. Your prayer for me was what sustained me thus far. I would also like to thank my brothers for always make fun of me for becoming a doctor. You made this journey fun.

Last but not least I would like to express appreciation to my beloved husband Farhad who spent sleepless nights with and was always my support in the moments when there was no one to answer my queries. Without you it would have been impossible for me to achieve this. Thank you!

## **Dedication**

To my dear husband, Farhad, who has been a constant source of support and encouragement during the challenges of graduate school and life, and to my lovely son Milad, whom I look forward to coming home to and see his beautiful smile and forget about all the problems during the day.

# Table of Contents

|  |            |
|--|------------|
| <b>LIST OF FIGURES.....</b>  | <b>IX</b>  |
| <b>LIST OF TABLES.....</b>   | <b>XIV</b> |
| <b>CHAPTER 1 INTRODUCTION.....</b>   | <b>1</b>   |
| 1.1    MOTIVATIONS.....  | 1          |
| 1.2    OBJECTIVES .....  | 2          |
| 1.3    THESIS OUTLINE .....  | 3          |
| <b>CHAPTER 2 LITERATURE SURVEY.....</b>  | <b>4</b>   |
| 2.1    RF MEMS SWITCHES .....  | 4          |
| 2.2    RF MEMS VARACTORS .....   | 7          |
| 2.3    SUPERCONDUCTIVITY .....   | 9          |
| 2.4    SUPERCONDUCTING RF MEMS SWITCHES .....  | 11         |
| <b>CHAPTER 3 CRYOGENIC PERFORMANCE OF GOLD-BASED RF MEMS DEVICES .....</b>                 | <b>15</b>  |
| 3.1    DESIGN AND FABRICATION .....  | 16         |
| 3.1.1    Switch I with Fixed Supports .....  | 19         |
| 3.1.2    Switch II with Flexible Supports.....   | 23         |
| <b>CHAPTER 4 ANALYSIS OF SILICON AND ALUMINA SUBSTRATES AT CRYOGENIC TEMPERATURES.....</b> | <b>25</b>  |
| 4.1    THERMAL ANALYSIS .....  | 25         |
| 4.2    RF ANALYSIS .....   | 33         |
| <b>CHAPTER 5 DEVELOPMENT OF RF MEMS DEVICES USING NB-BASED MULTILAYER PROCESS .....</b>    | <b>37</b>  |
| 5.1    HYPRES FABRICATION TECHNIQUE.....   | 37         |
| 5.1.1    Traditional Post-Processing Technique .....                                       | 38         |
| 5.1.2    Stress Analyses .....   | 41         |
| 5.1.3    Forming Dimples.....  | 45         |
| 5.2    NB-BASED RF MEMS SWITCHES .....   | 46         |
| 5.2.1    DC-Contact RF MEMS Switch .....   | 47         |
| 5.2.2    Capacitive-Contact RF MEMS Switches .....   | 57         |
| 5.3    NB-BASED RF MEMS VARIABLE CAPACITORS .....  | 65         |
| 5.1    NB-BASED RF MEMS DEVICES .....  | 71         |
| 5.1.1    Single-Port-Double-Throw RF MEMS Switch.....                                      | 71         |
| 5.4.1    Capacitor Bank.....   | 73         |
| 5.4.2    Tunable Resonator Using Switched Capacitor Bank.....                              | 76         |
| 5.4.3    Tunable Bandstop Resonator Using Varactor.....                                    | 80         |
| 5.4.4    Tunable Bandstop Filter Using Varactor .....                                      | 82         |
| <b>CHAPTER 6 THE DEVELOPMENT OF AN NB-BASED FABRICATION TECHNIQUE .....</b>                | <b>86</b>  |
| 6.1    NB FABRICATION PROCESS.....   | 86         |
| 6.2    SINGLE-LAYER NB DEVICES.....  | 89         |
| 6.3    MULTI-LAYER NB DEVICES.....   | 91         |
| 6.3.1    DC-Contact RF MEMS Switch .....   | 93         |
| 6.3.2    Capacitive-Contact RF MEMS Switch.....  | 96         |
| 6.3.3    Capacitor Bank.....   | 99         |
| 6.3.4    Tunable Bandpass Filter.....  | 101        |

|                   |                          |            |
|-------------------|--------------------------|------------|
| <b>CHAPTER 7</b>  | <b>CONCLUSIONS .....</b> | <b>111</b> |
| 7.1               | CONTRIBUTIONS .....      | 111        |
| 7.2               | FUTURE WORK .....        | 112        |
| <b>APPENDIX A</b> | <b>.....</b>             | <b>114</b> |
| <b>APPENDIX B</b> | <b>.....</b>             | <b>119</b> |
| <b>REFERENCES</b> | <b>.....</b>             | <b>125</b> |



# List of Figures

|  |    |
|--|----|
| Fig. 1.1 Schematic block diagram of the SME digital receiver.....  | 2  |
| Figure 2.1 Circuit model of an ideal dc-contact series switch in the down-state and up-state positions.<br>.....   | 5  |
| Fig. 2.2. (a) is a dc-contact series switch by Analog Devices and (b) is a dc-contact series switch by Lincoln Laboratory [6]. .....   | 5  |
| Fig. 2.3 Circuit model of an ideal capacitive-contact shunt switch in the down-state and up-state positions.....   | 6  |
| Fig. 2.4 Capacitive-contact shunt switch by Raytheon [6]. .....  | 6  |
| Fig. 2.5 Capacitive-contact shunt switch designed by the University of Michigan [6]. .....   | 7  |
| Figure 2.6 MEMS varactor [6]. .....  | 7  |
| Fig. 2.7 Varactor series model.....  | 8  |
| Fig. 2.8 First parallel plate varactor by UCLA, Berkeley [6]. .....  | 8  |
| Fig. 2.9 SEM image of the University of Michigan high-Q varactor [6]. .....  | 9  |
| Fig. 2.10 Equivalent circuit of complex conductivity of a superconductor [5]. .....  | 9  |
| Fig. 2.11 Variation of surface resistance of copper as a normal conductor and different superconductors vs. frequency [5]. .....   | 11 |
| Fig. 2.12 Steps of the fabrication process of Nb air bridge [8]. .....   | 12 |
| Fig. 2.13 SEM image of Nb-based air bridge by [8]. .....   | 13 |
| Fig. 2.14 SEM image of Nb-based air bridge by [9]. .....   | 13 |
| Fig. 3.17-mask fabrication process used to fabricate the tested gold-based RF MEMS switches [13].<br>.....   | 17 |
| Fig. 3.2 Dimensions and layout of the CPW TL [13]. .....   | 18 |
| Fig. 3.3 Group I, fixed supports. ....   | 18 |
| Fig. 3.4 Group II, flexible supports. ....   | 18 |
| Fig. 3.5 3D optical profiler image of Switch I.....  | 19 |
| Fig. 3.6 The gold beam deformation before and after the release process. (a) Before removing the sacrificial layer, (b) Beam deformed after removing the sacrificial layer due to the tensile stress, (c) The tensile stress distribution in section A-A' after removing the sacrificial layer. .... | 20 |
| Fig. 3.7 The stress distribution in section A-A' of the beam after the temperature decrease. ( $\sigma_0$ is the applied compressive stress due to the temperature variations. $\sigma_1$ is the stress due to localized effect in the gold layer. $\sigma_2$ is the final residual stress.) .....   | 21 |
| Fig. 3.8 COMSOL simulation of the initial displacement of Switch I at room temperature.....  | 21 |
| Fig. 3.9 3D optical profiler image of Switch II (The supports are not shown properly in the image due to the amount of the initial deflection.) .....  | 23 |
| Fig. 3.10 COMSOL simulation of the initial displacement of Switch II at room temperature. ....   | 24 |
| Fig. 4.1 Schematic of the four thermal shields of the Lakeshore cryogenic chamber and its typical temperature [17]. .....  | 26 |
| Figure 4.2 Image of chips mounted on the chuck in the Lakeshore cryogenic probe-station. ....  | 27 |

|  |    |
|--|----|
| Fig. 4.3 Comparison between the insertion loss of two identical 7-pole BPFs at 4K. One is mounted on the chuck using a clamp and Apiezon-N grease, and the other is mounted on the chuck using only silver paint. ....   | 27 |
| Fig. 4.4 A 3D model used to simulate temperature distribution across the device in COMSOL. It includes the adhesive material, the substrate, fabricated RF devices, and RF probes. ....  | 28 |
| Fig. 4.5 Temperature distribution across the substrate and the fabricated RF devices using two types of adhesive: a) Apeizon-N grease, and b) silver paint. ....   | 29 |
| Fig. 4.6 COMSOL simulation results of the comparison of temperature distribution along the signal line for silver paint and Apiezon-N grease on silicon substrate. ....  | 30 |
| Fig. 4.7 Thermal simulation in COMSOL for a 3D model in which the Nb-based TLs are connected to the probes through a set of gold wirebonds and Ti-based TLs. ....  | 31 |
| Fig. 4.8 A temperature comparison between the Ti-based TL and Nb-based TL, when the probes are touching the Ti-based TL. ....  | 32 |
| Fig. 4.9 COMSOL simulation results of temperature distribution across the signal line of a CPW TL on silicon and alumina substrates. ....  | 33 |
| Fig. 4.10 The measured and fitted results of the capacitance variation of the G/S/G pads vs. frequency at room and cryogenic temperatures. ....  | 34 |
| Fig. 4.11 Circuit model of the G/S/G pads at room temperature. ....  | 35 |
| Fig. 4.12 The measured and fitted simulation results of the gold-based transmission line at 293K and 4K, to demonstrate the effect of the silicon substrate loss. ....   | 36 |
| Fig. 5.1 Cross Section of the Hypres Process [4]. ....   | 38 |
| Fig. 5.2 The post-processing steps to release the MEMS structure [25]. ....  | 39 |
| Fig. 5.3 SEM images of several cantilever beam test structures with release hole dimensions varying from $2\ \mu\text{m} \times 2\ \mu\text{m}$ and spacing of $2\ \mu\text{m}$ between each two holes, to $6\ \mu\text{m} \times 6\ \mu\text{m}$ and spacing of $7\ \mu\text{m}$ . .... | 41 |
| Fig. 5.4 The SEM image of an array of released cantilever beams. ....  | 42 |
| Fig. 5.5 Measured deflection results of the cantilever beam and FEM simulation results for 10 KPa residual stress. ....  | 43 |
| Fig. 5.6 The SEM image of an array of released restrained beams. ....  | 44 |
| Fig. 5.7 Measured deflection results of the fixed-fixed beam and FEM simulation results for 10 KPa residual stress. ....   | 45 |
| Fig. 5.8 SEM images of several designs to develop dimples using the fabrication process offered by Hypres. ....  | 46 |
| Fig. 5.9 The top view (a) and the cross-section (b) of the superconducting RF MEMS switch in the 'off' and 'on' states. ....   | 48 |
| Fig. 5.10 Circuit model of the RF MEMS switch in the 'off' (a) and 'on' (b) states: $R_b$ is the DC bias line resistivity and $l$ is the length of the DC bias line. ....  | 49 |
| Fig. 5.11 The SEM image of the niobium superconducting RF MEMS switch after release. ....  | 50 |
| Fig. 5.12 FEM simulation results for the fabricated superconducting switch with warped plates using the determined residual stress value; the maximum beam deflection is $8.9\ \mu\text{m}$ . ....   | 51 |
| Fig. 5.13 Simulated results in COMSOL showing the effect of the substrate thickness on the beam deflection along the beam length when temperature changes from 293K to 4K. ....  | 52 |
| Fig. 5.14 Cross-section of the cantilever beam and the applied forces to the beam due to temperature variation. ....   | 53 |

|  |    |
|--|----|
| Fig. 5.15 The measured and simulated S-parameters of the superconducting RF MEMS switch at room temperature.....   | 54 |
| Fig. 5.16. The measured and simulated S-parameters of the superconducting RF MEMS switch performance at 4K. ....   | 55 |
| Fig. 5.17 SEM image of several designs of superconducting dc-contact RF MEMS switches fabricated using the Hypres foundry. ....  | 57 |
| Fig. 5.18 The top view (a) and the cross-section (b) of the superconducting RF MEMS capacitive-contact switch. ....  | 59 |
| Fig. 5.19 The SEM image of the niobium superconducting RF MEMS capacitive-contact switch after release and its circuit model. ....   | 60 |
| Fig. 5.20 The measured and simulated S-parameters of the superconducting RF MEMS capacitive-contact switch performance at cryogenic temperature. ....  | 61 |
| Fig. 5.21 The top view (a) and the cross-section (b) of the superconducting $\pi$ -match type capacitive-contact switch. ....  | 62 |
| Fig. 5.22 The SEM image of the superconducting $\pi$ -match type capacitive-contact switch.....  | 63 |
| Fig. 5.23 Measured results of the RF performance of the superconducting $\pi$ -match type capacitive-contact RF MEMS switch at room temperature. ....  | 63 |
| Fig. 5.24 Simulated and measured results of the RF performance of the superconducting $\pi$ -match type capacitive-contact RF MEMS switch at cryogenic temperature. ....                             | 64 |
| Fig. 5.25 SEM image of several designs of superconducting capacitive-contact RF MEMS switch fabricated using the Hypres foundry .....  | 65 |
| Fig.. 5.26. The top view (a) and the cross-section (b) of the superconducting RF MEMS varactor [39]. ....  | 66 |
| Fig. 5.27. The SEM image of the niobium superconducting RF MEMS varactor after release.....  | 67 |
| Fig. 5.28. FEM simulation results for the fabricated superconducting varactor with buckled plate. Using the determined residual stress value, the maximum plate deflection is 5 $\mu\text{m}$ . .... | 68 |
| Fig. 5.29. Measured results of the extracted capacitance value variation versus the actuation voltage at room temperature at 2 GHz for the Nb-based varactor. ....                                   | 69 |
| Fig. 5.30. Measured results of the extracted capacitance value variation versus the actuation voltage at cryogenic temperature, at 2 GHz for the Nb-based varactor. ....                             | 70 |
| Fig. 5.31. Quality factor comparison of superconducting and semiconductor varactors at room and cryogenic temperatures.....  | 70 |
| Fig. 5.32. SEM image of several designs of Nb-based varactors fabricated using the Hypres foundry. ....  | 71 |
| Fig. 5.33. The measured results of the superconducting SPDT RF MEMS switch S-parameter performance at cryogenic temperature. ....  | 73 |
| Fig. 5.34. (a) The circuit model and (b) the SEM image of the niobium superconducting capacitor bank implementing four DC contact RF MEMS switches .....   | 74 |
| Fig. 5.35. The extracted capacitance value from the measured S-parameters of the superconducting RF MEMS capacitor bank implementing dc-contact RF MEMS switches at cryogenic temperature. ....      | 74 |
| Fig. 5.36. (a) The circuit model and (b) the SEM image of the niobium superconducting capacitor bank implementing three capacitive contact RF MEMS switches. ....                                    | 75 |

|  |    |
|--|----|
| Fig. 5.37. The extracted capacitance value from the measured S-parameters of the superconducting RF MEMS capacitor bank implementing capacitive contact RF MEMS switches at room temperature. ....               | 76 |
| Fig. 5.38. Picture of the miniaturized superconducting 7-pole BPF. ....  | 77 |
| Fig. 5.39. Measured results of the RF response of the miniaturized superconducting 7-pole BPF at 4K ....   | 77 |
| Fig. 5.40. The circuit model of the superconducting tunable bandstop resonator with switched capacitors. ....  | 78 |
| Fig. 5.41. Picture of the fabricated superconducting tunable resonator with monolithically integrated capacitor bank and superconducting MEMS switches. ....   | 79 |
| Fig. 5.42. Measured results of the three states of the superconducting tunable bandstop resonator when switches are off (State I), first switch is on (State II) and second switch is on (State III) at 4K. .... | 79 |
| Fig. 5.43. SEM image of the integrated Nb-based MEMS tunable bandstop resonator. The varactor includes a fixed capacitor ( $C_{\text{fixed}}$ ) and a variable ( $C_{\text{tunable}}$ ) capacitor. ....          | 80 |
| Fig. 5.44. Measured results for the tunable resonator implementing MEMS varactor at 4K. ....   | 81 |
| Fig. 5.45. Variation of the centre frequency of the resonator versus the actuation voltage applied to the varactor. ....   | 82 |
| Fig. 5.46. Circuit model of the lumped element fixed BSF. ....   | 82 |
| Fig. 5.47. Photograph of the fabricated fixed bandstop filter. ....  | 83 |
| Fig. 5.48. Simulation and measured results of the superconducting BSF at cryogenic temperature. ....   | 84 |
| Fig. 5.49. Circuit model of the tunable lumped element BSF. ....   | 84 |
| Fig. 5.50. Measured results of the insertion loss of the tunable BSF at 4K. ....   | 85 |
| Fig. 6.1. The fabrication process steps to integrate Nb-based RF circuits with gold-based MEMS structures ....   | 88 |
| Fig. 6.2. Photograph of the Nb-based BPF with gold pads. ....  | 90 |
| Fig. 6.3. The measured results of the RF response of Nb-based BPF at 4K with Au pads and Cr/Au pads. ....  | 91 |
| Fig. 6.4. The measured results of the RF response of Nb-based TL with gold pads at room temperature and 4K. ....   | 92 |
| Fig. 6.5. The measured results of the RF response of Nb-based LPF with gold pads at room temperature and 4K. ....  | 92 |
| Fig. 6.6. The top view of the superconducting dc-contact RF MEMS switch fabricated using the 8-mask process in the CIRFE lab. ....   | 93 |
| Fig. 6.7. SEM image of the superconducting dc-contact RF MEMS switch. ....   | 94 |
| Fig. 6.8. The measured and simulated S-parameters of the superconducting dc-contact RF MEMS switch at room temperature. ....   | 94 |
| Fig. 6.9. The measured and simulated S-parameters of the superconducting dc-contact RF MEMS switch performance at cryogenic temperature. ....  | 95 |
| Fig. 6.10. SEM image of several designs of gold-based dc-contact RF MEMS switches monolithically integrated with Nb-based RF circuits. ....  | 95 |
| Fig. 6.11. The top view of the superconducting capacitive-contact RF MEMS switch fabricated using the 8-mask process in the CIRFE lab. ....  | 96 |
| Fig. 6.12. SEM image of the superconducting capacitive-contact RF MEMS switch. ....  | 97 |

|   |     |
|---|-----|
| Fig. 6.13. The measured and simulated S-parameters of the superconducting capacitive-contact RF MEMS switch at room temperature.....  | 97  |
| Fig. 6.14. The measured S-parameters of the superconducting capacitive-contact RF MEMS switch at cryogenic temperature for different actuation voltage values including: 0 V, 41 V, 76 V and 92 V... ..                       | 98  |
| Fig. 6.15. SEM image of several designs of gold-based capacitive-contact RF MEMS switches monolithically integrated with Nb-based RF circuits.....  | 99  |
| Fig. 6.16. The circuit model and the SEM image of the niobium superconducting capacitor bank implementing four dc-contact RF MEMS switches. ....  | 100 |
| Fig. 6.17. The extracted capacitance value from the measured S-parameters of the superconducting RF MEMS capacitor bank implementing dc-contact RF MEMS switches at cryogenic temperature. ....                               | 101 |
| Fig. 6.18. Layout of the 3-pole BPF showing three different states of the filter for three different configurations of MEMS switches [42].....  | 102 |
| Fig. 6.19. The measured and simulated results of the insertion loss of the 3-pole gold-based BPF [42]. ....   | 102 |
| Fig. 6.20. The measured and simulated results of the return loss of the 3-pole gold-based BPF [42]. ....  | 103 |
| Fig. 6.21. SEM image of the fabricated Nb-based 3-pole tunable BPF. ....  | 104 |
| Fig. 6.22. Measured results of State I and State II of the Nb-based tunable BPF at cryogenic temperature. ....  | 104 |
| Fig. 6.23. 2D and 3D model of the tunable BPF, which is magnified 20 times in the Z direction: (a) specifies MEMS switches used for input/output and inter-resonator couplings; (b) shows locations of the MEMS switches..... | 105 |
| Fig. 6.24. Simulation results of the fabricated Nb-based 3-pole tunable BPF at cryogenic temperature. ....  | 106 |
| Fig. 6.25. SEM image of one of the dc-contact RF MEMS switches integrated with the BPF as a tunable element.....  | 107 |
| Fig. 6.26. Measurement results of the fabricated gold-based tunable BPF at room temperature. ....   | 107 |
| Fig. 6.27. Measurement results of the Nb-based tunable BPF at cryogenic temperature.....  | 108 |
| Fig. 6.28. SEM image of part of the Nb-based tunable BPF that shows the air bridges without release holes.....  | 109 |
| Fig. 6.29. Simulation results for State I of the Nb-based tunable BPF with and without PI residues under the bridges. ....  | 109 |

# List of Tables

|   |    |
|---|----|
| Table 3.1. Simulation and measured results of $V_{PI}$ for Switch I. ....   | 22 |
| Table 3.2. Simulation and measured results of $V_{PI}$ for Switch II. ....  | 24 |
| Table 5.1. S-parameters and pull-in voltage comparison between two commercial RF MEMS switches and the Nb-based dc-contact RF MEMS switch. .... | 55 |
| Table 6.1. Critical temperature of Nb deposited in the four available centres. ....   | 89 |

# Chapter 1 Introduction

## 1.1 Motivations

Superconducting Micro-Electronics (SME) technology has the potential for realizing very high speed digital receivers capable of performing direct digitization of radio frequency signals with extremely low power consumption. SME circuits can manage digital signals with clock speeds of up to 40 GHz. SME technology offers limited choices for realizing reconfigurable analog front-ends, such as constructing a tunable inductor using a string of Josephson junctions (JJs) or superconducting quantum interference devices (SQUIDs) [1]. The primary problem with this approach is the intrinsic nonlinearity of JJs and limited power-handling capability. On the other hand, SME digital technology offers ultrafast digital switches [2] and logic circuits, along with high-linearity analog-to-digital converters (ADCs). Therefore, the monolithic integration of a reconfigurable high quality factor (Q) analog front-end, based on RF MEMS switches and capacitors, one or more ADCs, and fast digital circuitry for switching, distributing, and processing digitized RF data, makes the best combination for building interference-tolerant receivers for a variety of applications [3]. A single chip implementation of SME receivers is possible using the Hypres [4] process, which is based on niobium (Nb) Low-Temperature Superconductive (LTS) JJ technology.

Analog RF filters are required at the receiver front-end and are key components of the overall superconducting digital receiver. Superconducting RF filters have several advantages over conventional filters that use non-superconducting materials. For instance, they have near-zero insertion loss, better roll-off, and are capable of having narrow bandwidth. The superconducting characteristics allow for filter miniaturizations without sacrificing filter performance [5]. Being able to design miniaturized superconducting tunable filters will allow for the integration of an RF filter within the receiver chip to achieve a single chip solution, as shown in Fig. 1.1.

Tunability will make it possible to eliminate interference and will allow optimal use of the receiver's analog-to-digital converter (ADC) resources.

Radio Frequency Micro-Electro-Mechanical Systems (RF MEMS) have several advantages, including low insertion loss, zero or very low dc power consumption, small size, and low cost. Superconductive MEMS switches and varactors can be designed to have a very high Q at high frequencies, while maintaining excellent linearity performance.

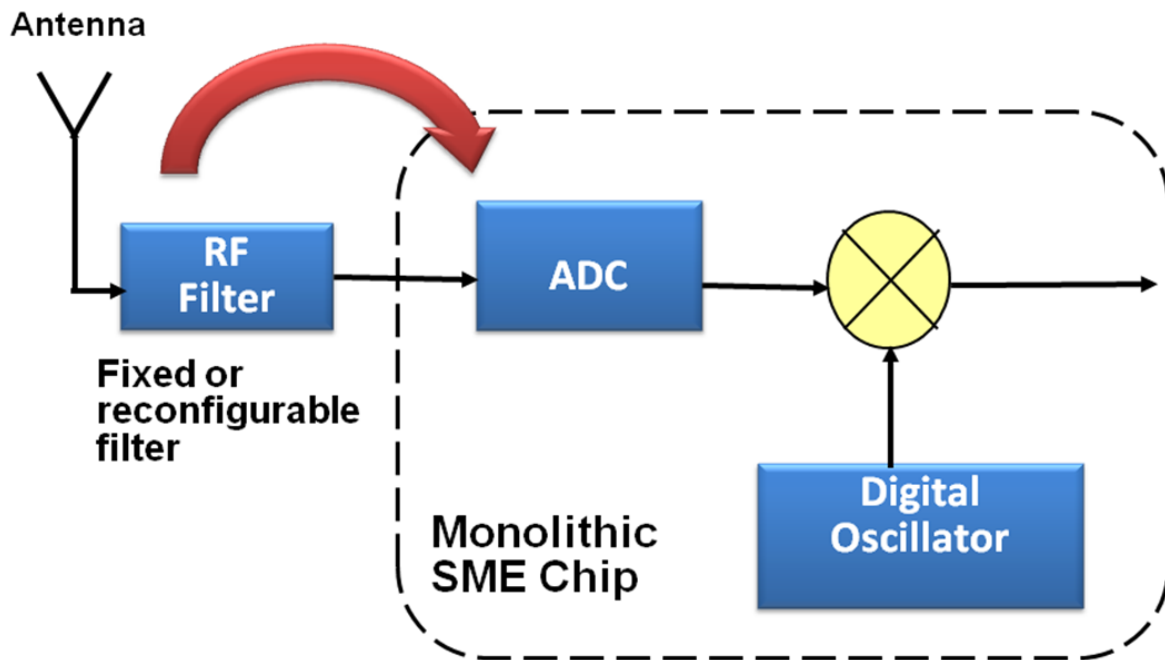


Fig. 1.1 Schematic block diagram of the SME digital receiver.

Combining the superconducting microwave filters with RF MEMS devices will allow for an RF reconfigurable system with unprecedented performance. It would have multi-band functionality for various wireless standards and applications, wide coverage of several frequency bands, tunability to compensate for variations inside the system, and adaptability for environmental effects such as temperature drift and aging. One of the main applications of tunable superconducting RF filters is integrating them with superconducting digital receivers, allowing for the realization of true software radios.

## 1.2 Objectives

The purpose of this research is to develop niobium-based low-temperature superconducting tunable devices such as switched capacitor banks, MEMS switches and varactors for integration with passive



low-temperature superconducting RF circuits. Namely, the main objectives of this research project are:

- Development of a post-processing technique as a complementary step to the SME fabrication process offered by Hypres that will enable the construction of tunable MEMS devices using this technology.
- Development of novel superconducting RF MEMS switches and variable capacitors capable of operating at extremely low temperatures (around 4K) for integration with superconductor digital receivers based on SME technology. The newly developed post-processing technique is employed for this integration.
- Development of an Nb-based fabrication process in the CIRFE lab at the University of Waterloo that is capable of integrating Nb-based RF devices with gold-based MEMS structures such as switches and varactors. The goal here is to make use of the low loss performance of the RF Nb-circuits while having the flexibility to optimize the thickness of the metal layers for the MEMS structure. Designers using the existing Hypres process do not have this flexibility.

### **1.3 Thesis Outline**

The motivation and the research objectives are outlined in this chapter. Chapter 2 discusses background information about RF MEMS switches and varactors in general, while focusing on superconducting RF MEMS devices in particular. Chapter 3 includes a study about the mechanical and RF performance of gold-based RF MEMS switches at cryogenic temperatures. Chapter 4 provides analyses of silicon and alumina substrates at cryogenic temperature and discuss RF testing issues at 4K. Chapter 5 introduces the superconducting niobium (Nb)-based fabrication process offered by Hypres. The newly proposed Nb-based RF MEMS devices, including switches, varactors, capacitor banks, tunable resonators and filters, are elaborated in this chapter. Chapter 6 introduces the novel 8-mask Nb-based fabrication process that integrates Nb-based RF circuits with gold-based RF MEMS devices in the CIRFE lab. Finally, a brief summary of the contributions of the thesis with an outline of proposed future research is given in Chapter 7.

# Chapter 2 Literature Survey

MEMS, which were initiated in the 1970s, are miniaturized devices ranging in size from one or two millimeters to a few micrometers. MEMS devices can be referred to as a two-port element that provides a link between a mechanical and an electrical system. The micro-fabrication techniques that are used to fabricate MEMS devices are similar to the Integrated Circuit (IC) fabrication methods. Many applications have been developed for MEMS devices, such as accelerometers, gyroscopes, pressure sensors, temperature sensors, and bio-sensors. The MEMS devices working at microwave frequency are called RF MEMS. Due to their outstanding performance, RF MEMS have immense potential for commercial and defense applications. The two main applications of RF MEMS devices are switches and varactors. RF MEMS switches use mechanical movement to achieve an open or short circuit in a Transmission Line (TL), while varactors are variable capacitors that function based on the mechanical movement of one of the plates in the capacitor.

## 2.1 RF MEMS Switches

RF MEMS switches come in two configurations: dc-contact and capacitive contact. Theoretically, a dc-contact series switch is 'off' when the beam is in the up-state position and no electrostatic force is applied to the MEMS structure. The switch is 'on' when the beam is in the down-state position and actuation voltage is applied to the beam, making the dc connect to the TL. Because these switches have a separate actuation electrode, it is possible for them to make direct dc contact to the TL. Ideally, dc-contact switches have infinite isolation and zero insertion loss. In reality, however, the metal-contact switches have a very low isolation of around 60 dB to 30 dB from 1 GHz to 20 GHz, and a very small insertion loss of around 0.1 dB. The operating frequency of these types of switches is in the range of 0.1 GHz to 40 GHz [6].

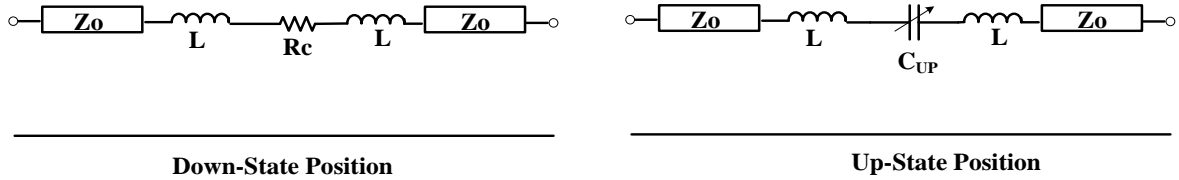


Figure 2.1 Circuit model of an ideal dc-contact series switch in the down-state and up-state positions [6].

Fig. 2.2 shows two dc-contact series switches developed by Analog Devices and Lincoln Laboratory, respectively. In the first switch, the cantilever beam was gold with a dimension of  $75\ \mu\text{m} \times 35\ \mu\text{m}$  and a thickness of about  $7\text{-}9\ \mu\text{m}$ . It was suspended on an Si substrate with an air gap of about  $0.6\text{-}1\ \mu\text{m}$  from the actuation electrode. The residual stress in the beam was very low and there was no release hole. The required actuation voltage was about  $60\text{-}80\ \text{V}$ . The switch had an isolation of approximately  $27\ \text{dB}$  and an insertion loss of about  $15\ \text{dB}$  at  $20\ \text{GHz}$ .

The Lincoln Laboratory switch had a tri-layer cantilever beam made of Oxide/Al/Oxide, with a total thickness of  $0.9\ \mu\text{m}$ . The beam's dimensions were  $55\ \mu\text{m} \times 50\ \mu\text{m}$ . The residual stress in the beam was very high, according to [6], and the required actuation voltage was between  $30\text{-}80\ \text{V}$ . The switch had an isolation of  $22\ \text{dB}$  and an insertion loss of  $0.15\ \text{dB}$  at  $30\ \text{GHz}$ .

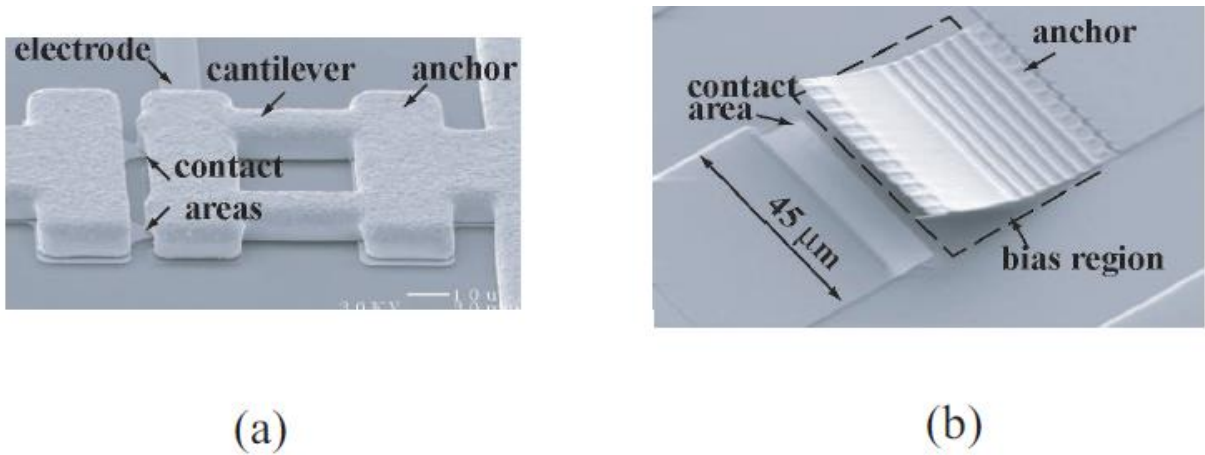


Fig. 2.2. (a) is a dc-contact series switch by Analog Devices and (b) is a dc-contact series switch by Lincoln Laboratory [6].

The capacitive-contact switches are placed in shunt between the TL and the ground plane. Ideally, the switch is on when the beam is in the up-state position, and off when the actuation voltage is applied and the beam is in the down-state position. Unlike the series switches, the actuation electrode of the shunt switches is not separate from the TL, which is the signal line itself. To create dc isolation, the

signal line underneath the beam is covered by a thin dielectric layer. Capacitive-contact switches are mainly employed in higher frequencies applications, compared to series switches, and their operating frequency is in the range of 5 GHz to 100 GHz. They should ideally have zero insertion loss and infinite isolation, but the switches usually have an insertion loss of about 0.1 dB and an isolation of 20 dB. Fig. 2.3 shows the circuit model of a capacitive-contact shunt switch in the down-state and up-state positions.

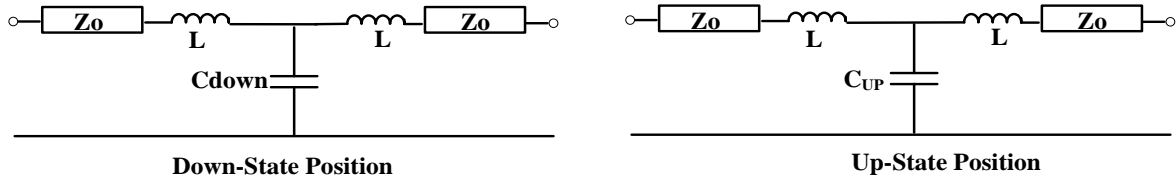


Fig. 2.3 Circuit model of an ideal capacitive-contact shunt switch in the down-state and up-state positions [6].

Fig. 2.4 shows a capacitive-contact switch developed by Raytheon. The switch membrane was aluminum, with a dimension of  $270\text{-}350\ \mu\text{m} \times 50\text{-}200\ \mu\text{m}$  and a thickness of  $0.5\ \mu\text{m}$ . The air gap between the bridge and the signal line was  $3\text{-}5\ \mu\text{m}$ , the residual stress in the beam was about 10-20 MPa, the required actuation voltage was 30 V to 50 V, and the capacitance ratio was 80 to 120. The operating frequency of the switch was between 10 GHz to 40 GHz, in which the device had an isolation of 20 dB and an insertion loss of 0.07 dB [6].

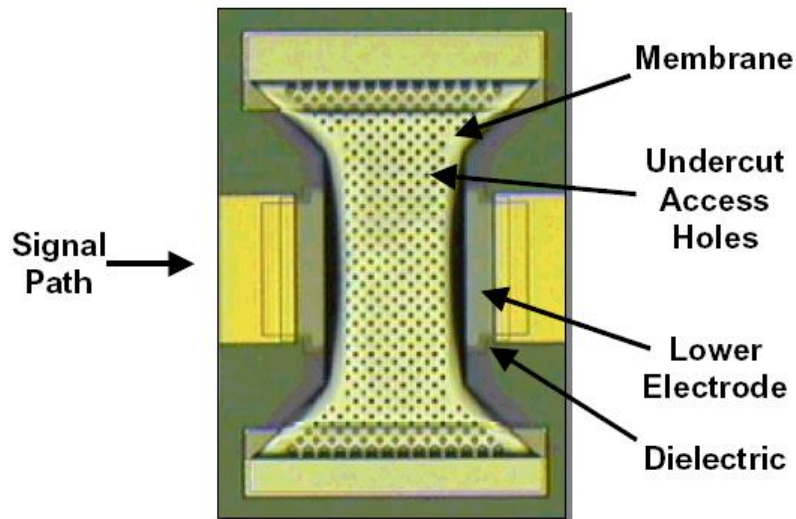


Fig. 2.4 Capacitive-contact shunt switch by Raytheon [6].

Fig. 2.5 shows a capacitive-contact shunt switch with a low actuation voltage, designed by the University of Michigan. As shown in the image, the switch has a low spring constant to reduce the actuation voltage, compared to the previous switch. The membrane was made of nickel, with a dimension of  $500\text{-}700\ \mu\text{m} \times 200\text{-}250\ \mu\text{m}$  and a thickness of about  $2\ \mu\text{m}$ . The bridge air gap was about  $4\ \mu\text{m}$ , the residual stress in the membrane was between 20 MPa to 100 MPa, and the required actuation voltage was between 6 V to 20 V, depending on the deflection of the beam. The switch isolation was about 25 dB and the insertion loss was 0.1 dB at 30 GHz.

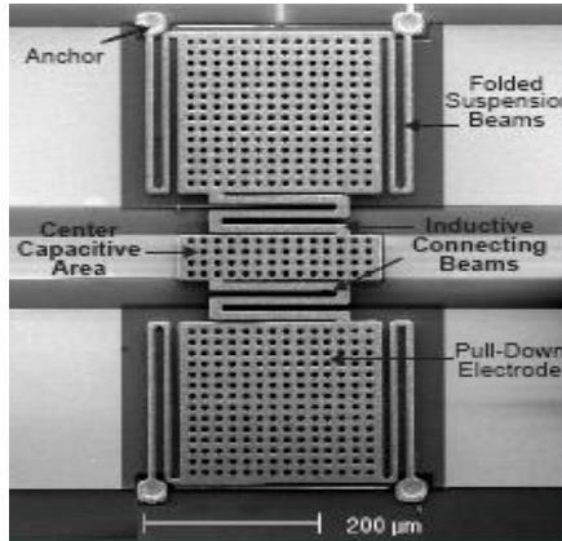


Fig. 2.5 Capacitive-contact shunt switch designed by the University of Michigan [6].

## 2.2 RF MEMS Varactors

A conventional MEMS variable capacitor is a parallel plate capacitor in which one of the plates is movable. Fig. 2.6 shows a schematic of a MEMS varactor. By applying a voltage between the two plates, the movable plate displaces toward the fixed plate. When the gap reaches two-thirds of the initial value, the top plate collapses. This is called pull-in status.

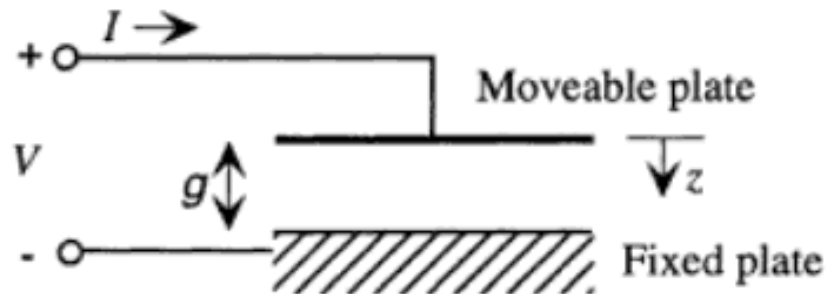


Figure 2.6 MEMS varactor [6].

The pull-in voltage ( $V_{PI}$ ) is calculated using Equation (2.1) [6]:

$$V_{PI} = \sqrt{\frac{8Kg_0^3}{27\epsilon_0 A}} \quad (2.1)$$

where  $g_0$  is the gap,  $A$  is the area of the plate,  $\epsilon_0$  is the permittivity of the vacuum and  $K$  is the spring constant of the switch, which depends on the type of support.

Considering a series model for the varactor, shown in Fig. 2.7, the quality factor is calculated by Equation (2.2) [6]:

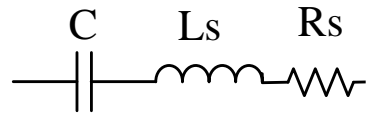


Fig. 2.7 Varactor series model.

$$Q = \frac{1}{\omega CR_s} \quad (2.2)$$

Fig. 2.8 shows the image of the very first MEMS varactor, which was designed and fabricated by the University of California, Berkeley. The plates were made of aluminum, with a dimension of  $200 \mu\text{m} \times 200 \mu\text{m}$  and a thickness of  $1 \mu\text{m}$ . The air gap between the two plates was about  $1.5 \mu\text{m}$ , the up-state capacitance value was measured  $0.51 \text{ pF}$ , and the varactor had a 15% variation in the capacitance value. The measured  $Q$  for four of these varactors connected in parallel was 60 at 1 GHz.

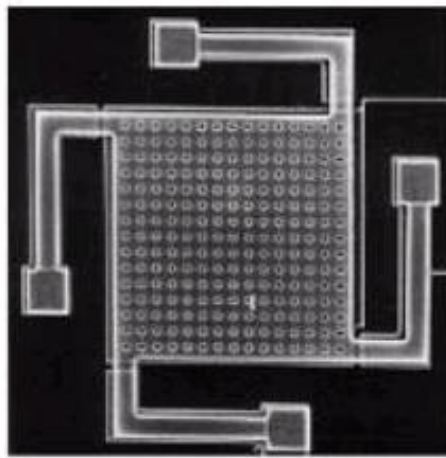


Fig. 2.8 First parallel plate varactor by UCLA, Berkeley [6].

A high-Q varactor was designed by the University of Michigan in 2002 [6]. Fig. 2.9 shows the SEM image of the device. The plates were gold and the dielectric layer was a PECVD (Plasma Enhanced Chemical Vapor Deposition) SiO<sub>2</sub>. The air gap exceeded 2.5 μm, the up-state capacitance value was 80 fF, and the tuning ratio obtained was about 1.90, with a control voltage of about 25 V. The measured quality factor for this varactor was 120 at 34 GHz.

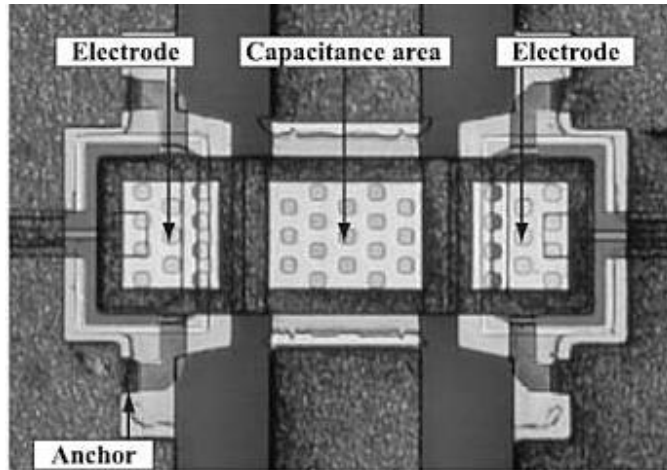


Fig. 2.9 SEM image of the University of Michigan high-Q varactor [6].

### 2.3 Superconductivity

In a superconducting metal, superconductivity occurs as the result of paired and unpaired electrons in the metal. The number of paired electrons suddenly increases as the temperature decreases below the critical temperature point, which is represented as  $T_c$  of the superconductor. The paired electrons travel, in the presence of an electric field, with no resistive loss. Due to the thermal energy present in the solid, a superconductor always contains unpaired electrons. Therefore, a superconductor's complex resistivity can be modeled as  $\sigma_1 - j\sigma_2$ , which can be interpreted as a parallel resistor and inductor, as shown in Fig. 2.10. [5].

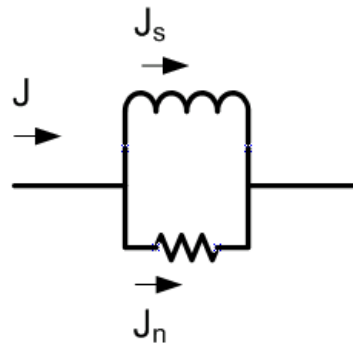


Fig. 2.10 Equivalent circuit of complex conductivity of a superconductor [5].

The propagation constant and intrinsic impedance of a superconductor are defined in a way that is very similar to a normal conductor:

$$\gamma = \sqrt{j\omega\mu(\sigma_1 - j\sigma_2)} \quad (2.3)$$

and

$$Z_s = \sqrt{\frac{j\omega\mu}{\sigma_1 - j\sigma_2}} \quad (2.4)$$

where  $\omega$  is the frequency and  $\mu$  is the permeability of free space. Considering  $\sigma_2 \gg \sigma_1$ , the above propagation constant and the intrinsic impedance of superconductor are simplified as:

$$\gamma \approx \sqrt{(\omega\mu\sigma_2) \left(1 + j \frac{\sigma_1}{2\sigma_2}\right)} \quad (2.5)$$

$$Z_s \approx \sqrt{\left(\frac{\omega\mu}{\sigma_2}\right) \left(\frac{\sigma_1}{2\sigma_2} + j\right)} \quad (2.6)$$

From the intrinsic impedance, one can derive the resistance and inductance values of a superconductor as:

$$R_s = \frac{\omega^2 \mu^2 \sigma_1 \lambda^3}{2} \text{ and } X_s = \omega\mu\lambda$$

where  $\lambda$  is the penetration depth of a superconductor. The penetration depth in a superconductor is similar to the skin depth of a normal conductor. It is the depth to which electromagnetic waves penetrate the superconductor and defines the extent of a region near the surface in which a current can be induced [5].

$$\lambda = \sqrt{\frac{1}{\omega\mu\sigma_2}} \quad (2.7)$$

As shown in the above equation, the resistivity of the superconductor is directly proportional to the frequency squared. Thus, at high frequencies, superconductors are more resistive than normal conductors. Fig. 2.11 depicts variations in the surface resistance of copper (Cu) as a normal conductor and two superconductors versus frequency at 4.2 K. The surface resistance of Nb is about  $10^3$  times less than Cu at 1 GHz, while they are equal at 1 THz [5].



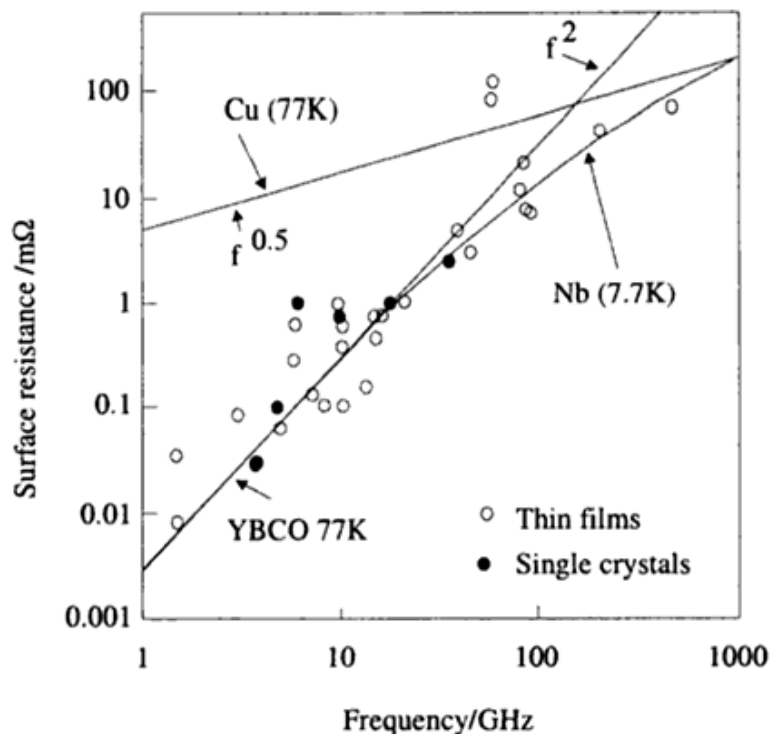


Fig. 2.11 Variation of surface resistance of copper as a normal conductor and different superconductors vs. frequency [5].

Even though the resistivity of superconductors increases by frequency, they can still be considered as lossless at RF. There are many advantages in using superconducting metals in RF devices. RF devices with a very low insertion loss and a very high-Q can be built employing superconducting metals. Since the loss is very small, designing miniaturized devices is feasible by utilizing lumped element components. To achieve such devices, low-temperature superconductors are more suited than high-temperature ones for the mass production and commercialization fabrication process. There are many complications in the fabrication process of High-Temperature Superconducting (HTS) materials. According to [7], the required condition for epitaxial growth and the anisotropic nature of an HTS material such as YBCO make HTS fabrication processes much more difficult than Nb-based fabrication processes.

## 2.4 Superconducting RF MEMS Switches

There are only a few reports in the literature regarding Nb-based superconductive RF MEMS devices. In 2003, M. Schickes et al. [8] designed and fabricated several air bridges with variations in the length, width and thickness for the top electrodes. They fabricated their devices on a quartz substrate, and the thickness of the bridges varied between 200 nm and 700 nm, while their width varied between

50  $\mu\text{m}$  and 300  $\mu\text{m}$ . The air gap was 5  $\mu\text{m}$ . They achieved an up-state capacitance value of 30-33 fF and a down-state capacitance value of 33-38 fF, which represents a 10%-15% capacitance variation. The actuation voltage of the bridge was 45 V. Fig. 2.12 illustrates the steps of the fabrication process used in [8]. After the dc sputtering of the first layer of Nb, the sacrificial layer was spin-coated. Photoresist (PR) AR-4000/8 (ALL RESIST GmbH) was used as the sacrificial layer, giving a resist thickness of 5  $\mu\text{m}$ . To obtain sufficiently smooth edges and to prevent the Nb film from breaking at the edges of the structures, the resist was baked for 30 min at 85  $^{\circ}\text{C}$  before exposure and an additional 4 h at 94  $^{\circ}\text{C}$  after development in a convection oven. Next, the top Nb layer was sputtered by a DC-magnetron at intervals of 9 s deposition and 5 min pause. The pauses were needed to reduce surface heating and thus deformation or polymerization of the resist layer. The air bridge was patterned by a PR AR 4000/8 and a Reactive Ion Etching (RIE). In the final step, the resist was washed away in 70  $^{\circ}\text{C}$  acetone. Fig. 2.13 shows the SEM image of the device.

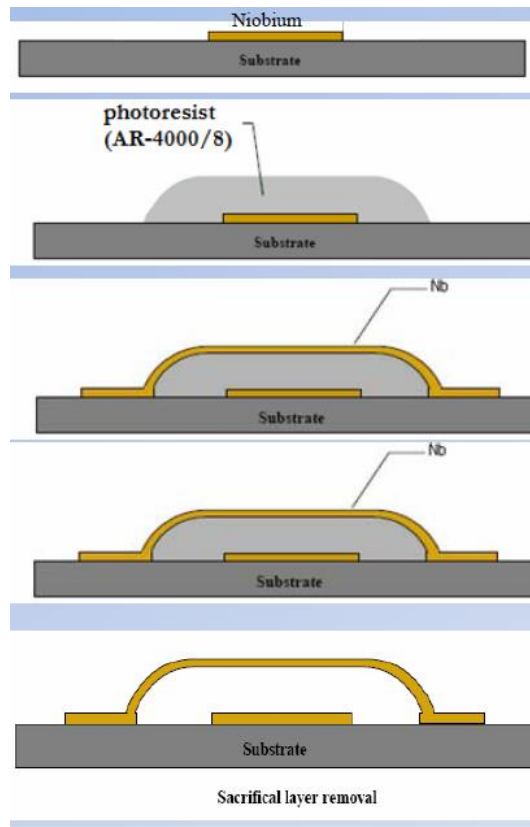


Fig. 2.12 Steps of the fabrication process of Nb air bridge [8].

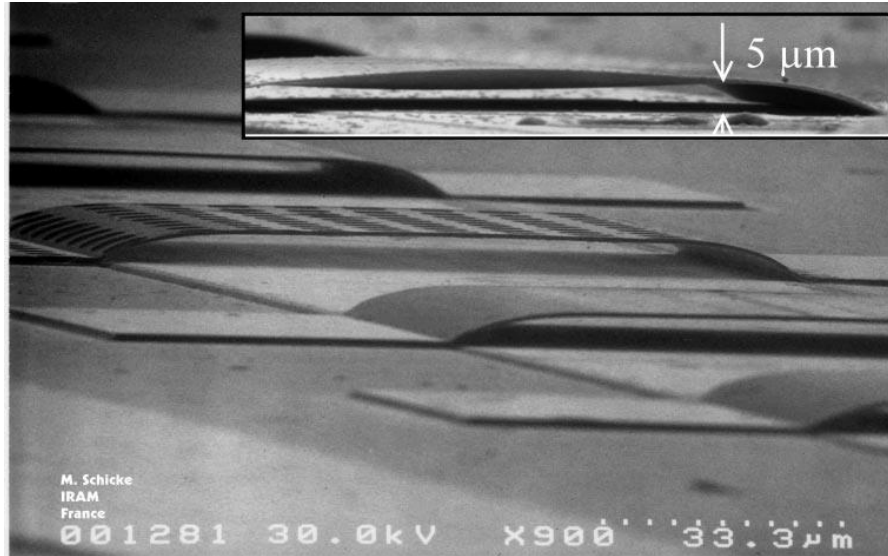


Fig. 2.13 SEM image of Nb-based air bridge by [8].

In 2008, M. Schickes et al. [9] designed and fabricated another RF MEMS air bridge. Fig. 2.14 shows the SEM image of the switch. The fabrication steps were similar to [8], in that they fabricated the device on a quartz substrate. The top electrode had a thickness of  $1.5\mu\text{m}$  and the air gap was  $2.6\mu\text{m}$ . Using a  $100\mu\text{m} \times 100\mu\text{m}$  plate, they achieved capacitance variations between 50 fF and just 70 fF using a voltage between 0 V and 50 V.

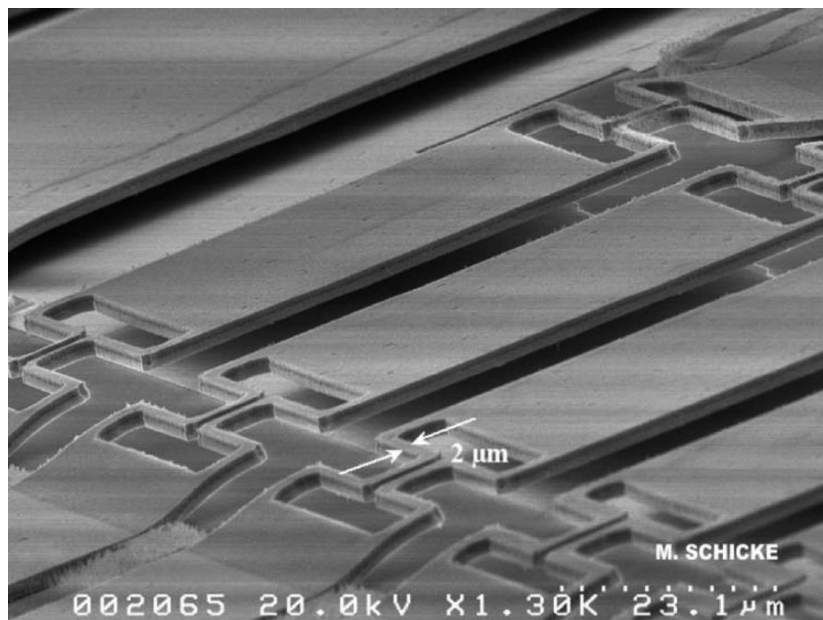


Fig. 2.14 SEM image of Nb-based air bridge by [9].

There is no data available on the superconducting behavior or mechanical characteristics at cryogenic temperatures for any of the above devices. There is also no data available on the RF performance of these devices. In addition, the fabrication process in [8] is not compatible with the process used for realization of direct digital receivers. The process in [8] includes two metal layers and only an air dielectric layer, resulting in a very small capacitance ratio.

# Chapter 3 Cryogenic Performance of Gold-Based RF MEMS Devices

The performance of RF MEMS switches at cryogenic temperatures is important, since they have the ability to be employed in the realization of high-Q superconducting reconfigurable circuits. Superconducting RF MEMS devices can lead to a very low insertion loss while maintaining excellent linearity performance.

There are not many data available in the literature regarding the characterization of RF MEMS switches at cryogenic temperature. J. Noel et al. [10] investigated the cryogenic pull-down voltage of a gold-based capacitive shunt switch. Their results indicated a more than 10-fold increase in the actuation voltage for temperature variations between 293K and 13K. C. Goldsmith et al. [11] fabricated an aluminum-based capacitive switch on a Pyrex glass substrate. Their investigation showed a 0.127 V/°C to 0.132 V/°C increase of the pull-in voltage.

All of the above switches have fixed-fixed supports, and there is no information regarding the initial displacement due to residual stress in the structures. Considering that there is no initial deformation in the membranes of these switches, a temperature decrease causes the beam and substrate to contract. Since the coefficient of thermal expansion (CTE) of the substrate is less than the CTE of the beam, the beam is under compression. The presence of compressive stress and the increase of the Young's modulus of the membrane results in an increase in the pull-in voltage as the temperature decreases.

This chapter investigates the effects of various types of supports and the initial deflection on the switch actuation voltage at different temperatures. More than 50 gold-based capacitive shunt RF MEMS switches are analytically characterized and tested at room and liquid nitrogen temperatures of 293K and 77K, respectively. While the results reported in the literature [10, 11] show that the actuation voltage increases at cryogenic temperatures, our experimental results show that the actuation voltage can either increase or decrease, depending on the switch structure. Our finding is also supported by simulation and analytical results that are in good agreement with the measured results [12].

### **3.1 Design and Fabrication**

Fig. 3.1 illustrates the steps of the fabrication process for the tested gold switches fabricated by R. Al Dahleh [13]. An alumina substrate is selected for the base substrate. The first step is the e-beam deposition and patterning of a 400 Å of chromium (Cr) and a 1200 Å of gold (Au). Next, a 1800 Å silicon nitride layer ( $\text{Si}_3\text{N}_4$ ) is PECVD deposited and patterned over the electrode area and bias lines. In Fig. 3.1(e), the sacrificial layer, which is a PR in this process, is spin-coated with a thickness of 2.6  $\mu\text{m}$ . The MEMS air bridge is then fabricated by the e-beam and electroplated up to 1.2  $\mu\text{m}$ .

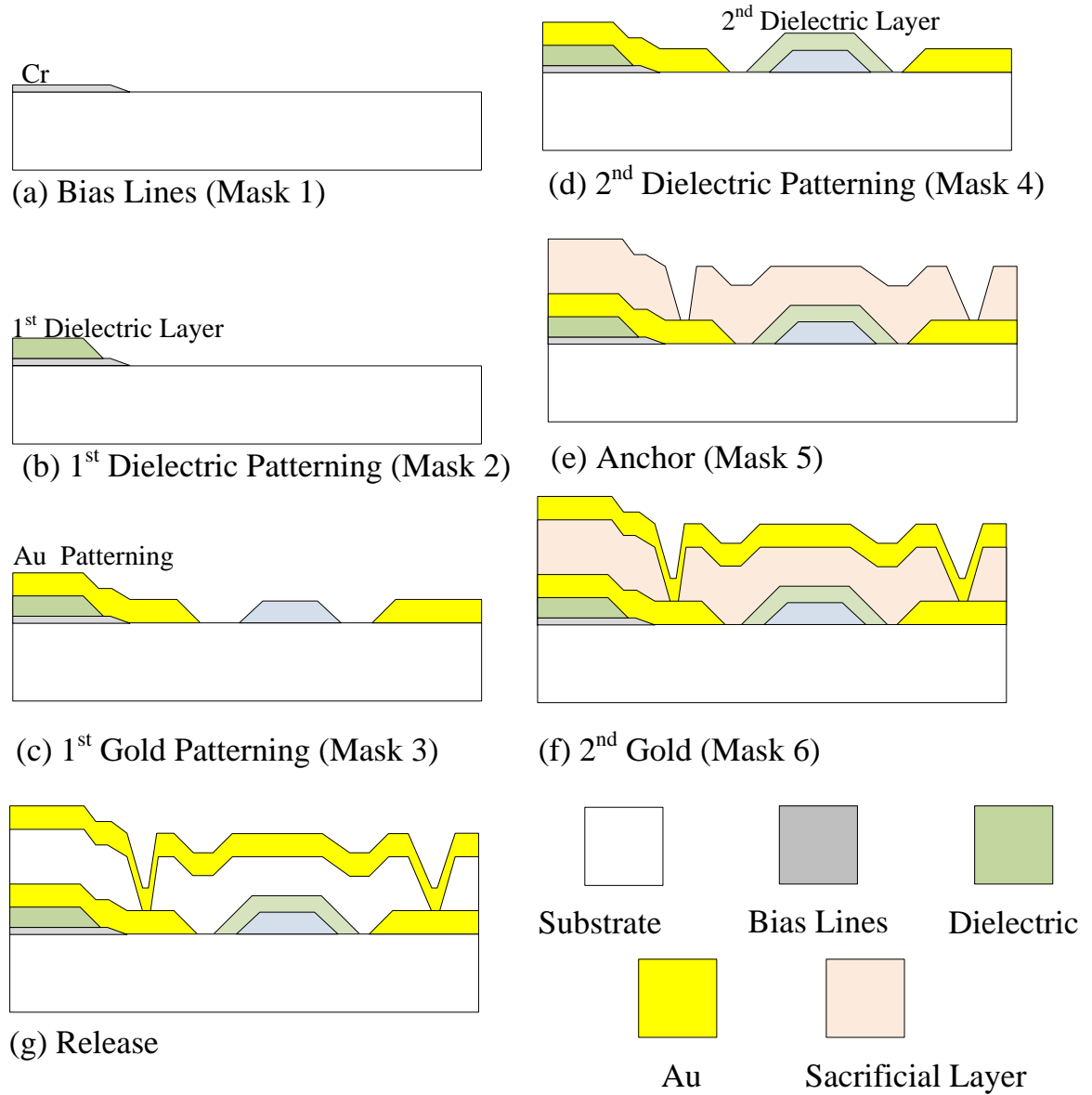


Fig. 3.17-mask fabrication process used to fabricate the tested gold-based RF MEMS switches [13].

The switches are mounted on a Coplanar Waveguide (CPW) TL. The dimensions and layout of the transmission line are illustrated in Fig. 3.2, while Fig. 3.3 and Fig. 3.4 depict the support structures used to attach to the plates of the switches.

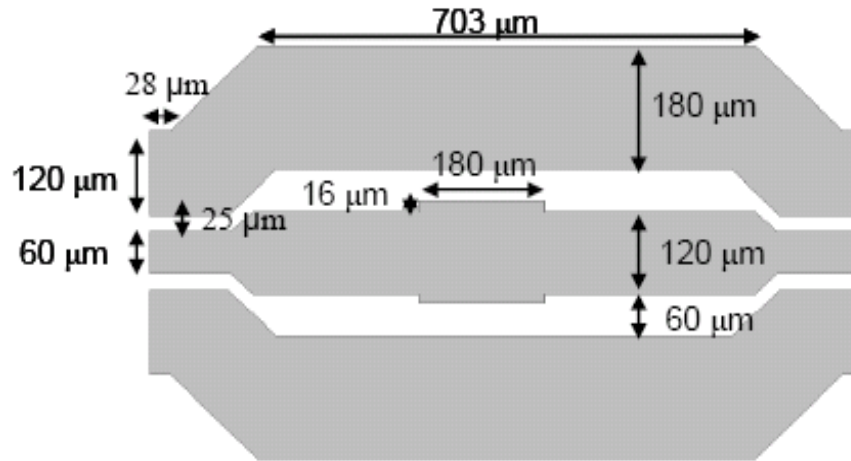


Fig. 3.2 Dimensions and layout of the CPW TL [13].

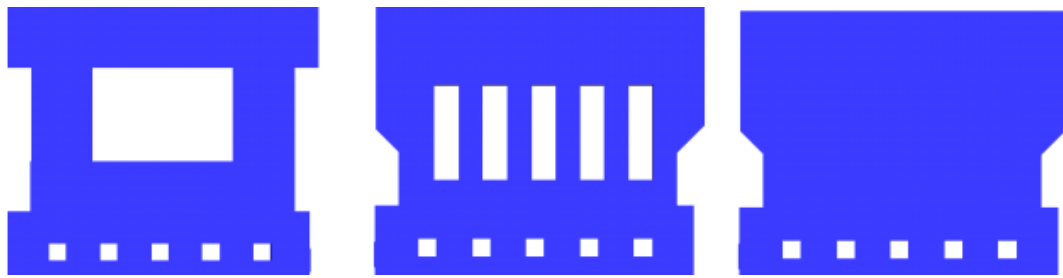


Fig. 3.3 Group I, fixed supports.

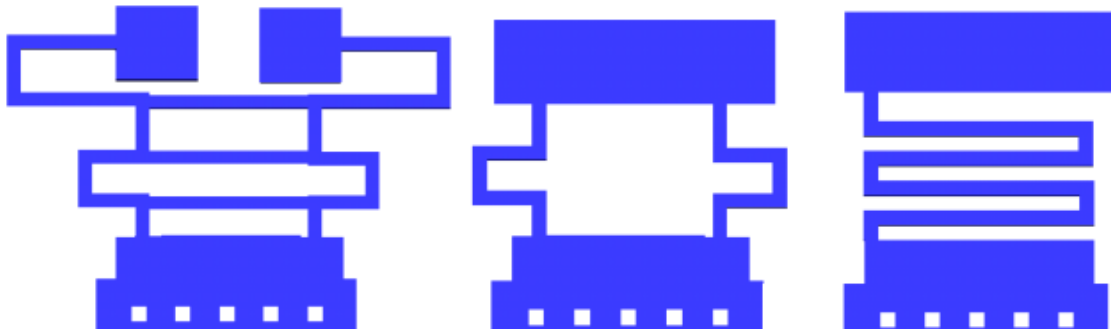


Fig. 3.4 Group II, flexible supports.

The switches are tested in a SUSS Micro Tech PMC-150 Cryoprober. The chuck temperature can be varied from 293K to 10 K. An Agilent 8722 Vector Network Analyzer is used to measure the RF response of the switches. The switches are actuated by applying a voltage to the dc pad, which is connected to the signal line through a Cr resistive line. The dc ground is connected to the RF ground.

The switches are first actuated at a typical room temperature of 293K. The actuation voltage is varied from 15 V to 60 V, depending on the support configuration. The switches are then tested at a typical



cryogenic temperature of 77K. The results significantly vary depending on the type of the supports and the initial displacement of the beam. In the switches with fixed supports (Group I), the actuation voltage decreases at cryogenic temperature, while for the switches with flexible supports (Group II), the actuation voltage increases at cryogenic temperature. To elaborate more on these variations, one switch in each category is analytically and numerically studied.

### 3.1.1 Switch I with Fixed Supports

Fig. 3.5 shows the optical profiler image of Switch I. The plate has a deflection of about  $5.3 \mu\text{m}$  in the centre, including a  $2.6 \mu\text{m}$  air gap. The initial deflection is due to the release of some residual stress in the thin film gold layer of the beam structure after the release process. The residual stress includes a tensile stress, which is due to the CTE difference between the gold layer and the sacrificial layer, and a gradient stress, which is due to some localized effects in the gold layer such as atomic diffusion through the thickness of the gold film to the film/substrate interface [14].

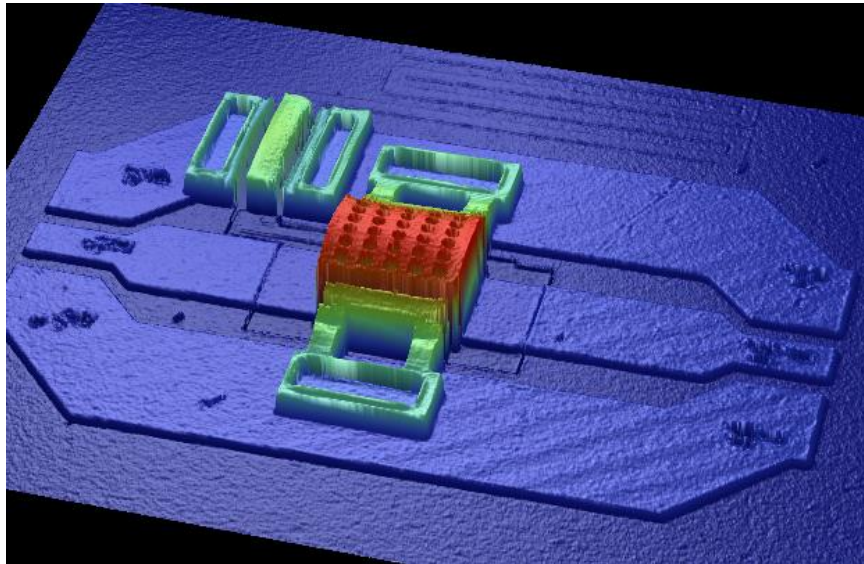


Fig. 3.5 3D optical profiler image of Switch I.

Fig. 3.6(a) shows the beam before the release process, which is perfectly straight, and Fig. 3.6(b) shows the buckling of the beam after removing the sacrificial layer. Fig. 3.6(c) shows the tensile stress distribution in section A-A'. By decreasing the temperature, both the alumina substrate and the gold beam are contracted. This adds a compressive stress to the beam, as shown in Fig. 3.7(a). The value of the compressive stress depends on the CTE difference between the substrate and the beam materials. The higher the CTE difference, the higher the compressive stress value will be. Depending on the value of the added compressive stress, the value and type of the initial residual stress varies. In this experiment, the value of the residual stress decreases but the type remains tensile, as shown in

Fig. 3.7(b). The simulation results in COMSOL [15] confirm the hypothesis. According to the results, by varying the temperature from 293K to 77K while the Young's modulus of the gold is increased from 57 GPa [16] to 82 GPa, the deflection is reduced from 5.3  $\mu\text{m}$  to 3  $\mu\text{m}$ . Fig. 3.8 shows the simulation results at room temperature.

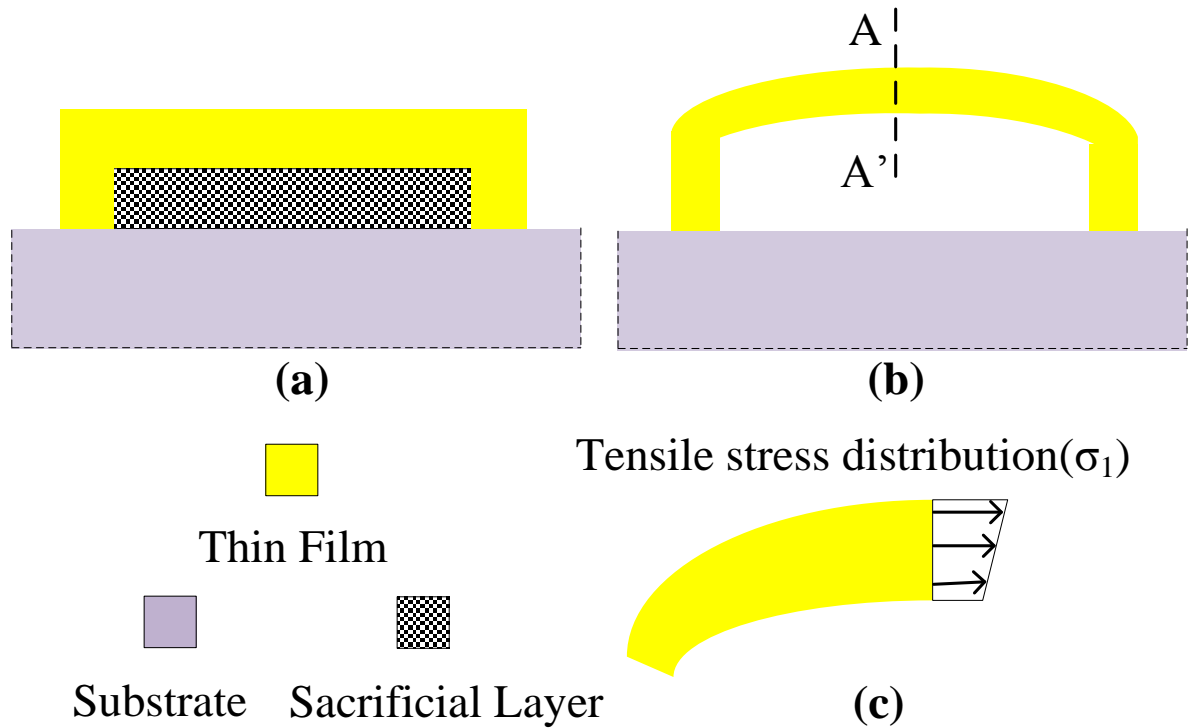


Fig. 3.6 The gold beam deformation before and after the release process. (a) Before removing the sacrificial layer, (b) Beam deformed after removing the sacrificial layer due to the tensile stress, (c) The tensile stress distribution in section A-A' after removing the sacrificial layer.

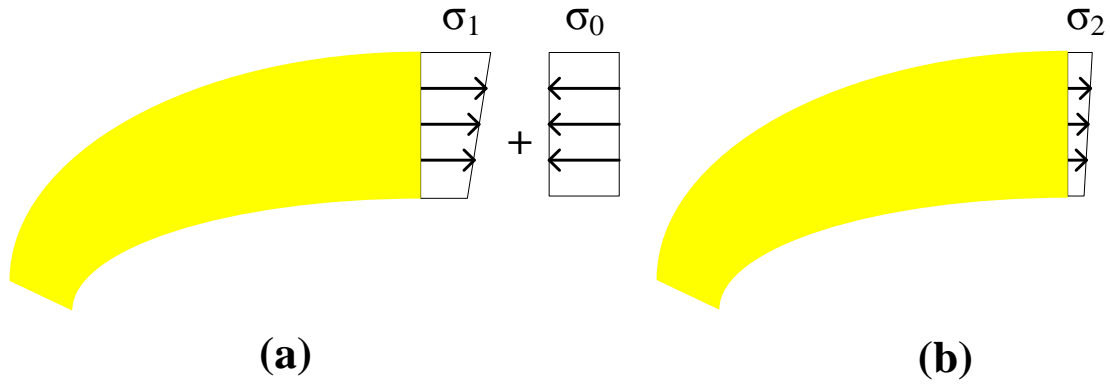


Fig. 3.7 The stress distribution in section A-A' of the beam after the temperature decrease. ( $\sigma_0$  is the applied compressive stress due to the temperature variations.  $\sigma_1$  is the stress due to localized effect in the gold layer.  $\sigma_2$  is the final residual stress.)

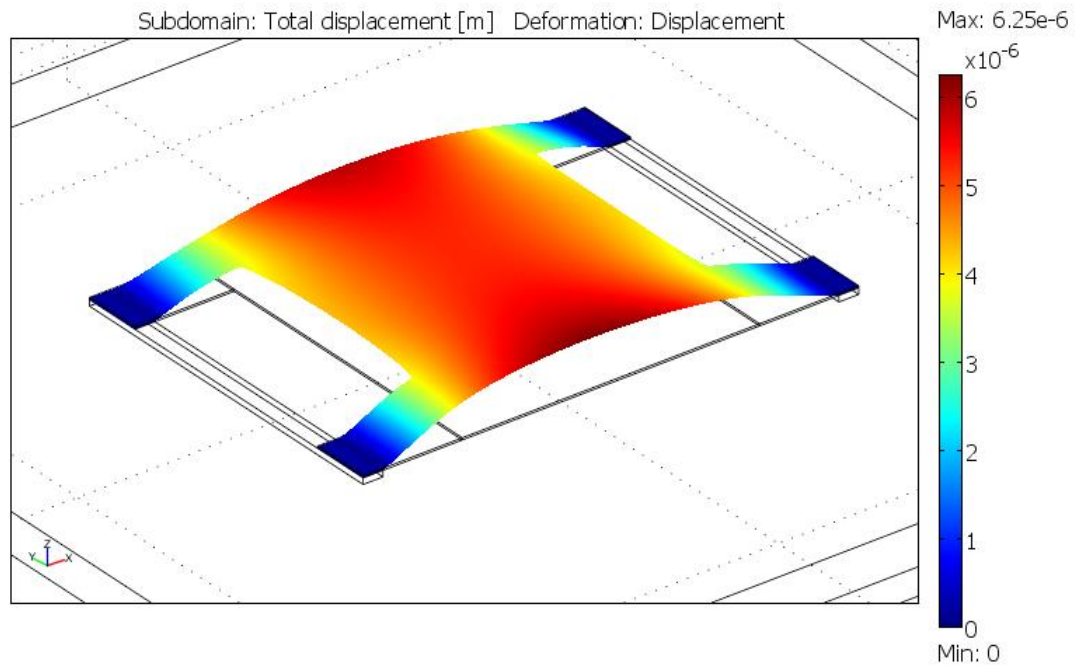


Fig. 3.8 COMSOL simulation of the initial displacement of Switch I at room temperature.

The pull-in voltage is modeled in CoventorWare, at both room and cryogenic temperatures, by applying the initial displacement obtained from COMSOL and the corresponding Young's modulus. The computed  $V_{PI}$  in CoventorWare at room temperature is 52.6 V. The simulation shows that  $V_{PI}$

decreases when the temperature decreases from 293K to 77 K. Table 3.1 shows the simulation and the measured results of Switch I. The measurement and the simulation are in good agreement.

Table 3.1. Simulation and measured results of  $V_{PI}$  for Switch I.

| Switch I    | Pull-In Voltage |            |
|-------------|-----------------|------------|
|             | Measured        | Simulation |
| Temperature |                 |            |
| 293K        | 53 V            | 52.6 V     |
| 77 K        | 30 V            | 36 V       |

The ratio of the pull-in voltage at room and cryogenic temperatures is:

$$\frac{V_{PICr}}{V_{PIr}} = \sqrt{\frac{E_{Cr}g_{0cr}^3}{E_r g_{or}^3}} \quad (3.1)$$

where  $V_{PIr}$  is the pull-in voltage at room temperature,  $V_{PICr}$  is the pull-in voltage at cryogenic temperature,  $E_r$  is the Young's modulus of the beam material at room temperature, and  $E_{Cr}$  is the Young's modulus at cryogenic temperature.

As shown in Equation (3.1),  $V_{PI}$  is expected to increase due to the increase in the Young's modulus of the gold at cryogenic temperature. Nonetheless, the variation effect of the air gap is cubical compared to the Young's modulus. Since the air gap decreases at cryogenic temperature, the actuation voltage decreases as well.

### 3.1.2 Switch II with Flexible Supports

Another switch from the second category is also tested. Fig. 3.9 shows the optical profiler image of the switch. The top capacitor plate has a concave shape after the release process, while the centre of the plate has no deflection. In this design, the flexible supports experience the most deformation. This design shows that, with flexible supports, the added compressive stress due to temperature decreases has no effect on the displacement of the plate. In fact, the flexible supports observe most of the applied compressive stress. In this type of structure, the most dominant factor on  $V_{PI}$  at different temperatures is the variation of the Young's modulus of the gold.

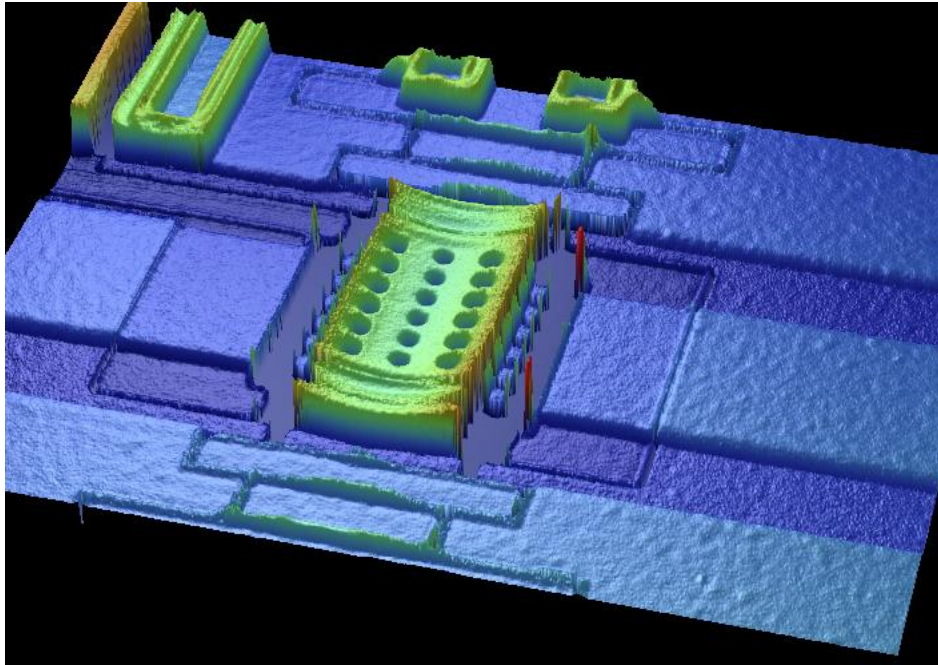


Fig. 3.9 3D optical profiler image of Switch II (The supports are not shown properly in the image due to the amount of the initial deflection.).

Similar to Switch I, the Thermo-Mechanical behavior of Switch II at room and cryogenic temperatures is simulated in COMSOL. The result indicates that the deflection at the centre of the plate is zero while the flexible supports show the highest amount of deformation. Fig. 3.10 shows the simulation results of the deformation of Switch II at room temperature after applying some residual stress similar to Switch I. The simulation results show that the plate is curled-in at the centre, similar to the profilometer image. When the temperature varies from room to cryogenic, only the deformation of the supports varies.

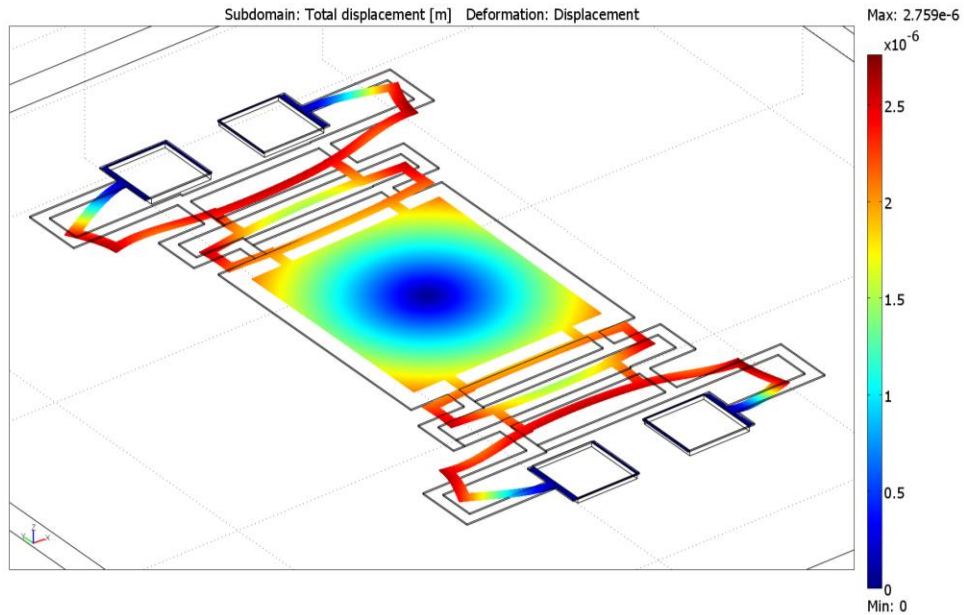


Fig. 3.10 COMSOL simulation of the initial displacement of Switch II at room temperature.

Table 3-2 shows the simulation and measured results. Since the deformation of the supports cannot be modeled in CoventorWare,  $V_{PI}$  is computed assuming no initial stress. This causes the deviation between the measurement and the simulation. The results confirm that the most dominant parameter in this design is the Young's modulus.

Table 3.2. Simulation and measured results of VPI for Switch II.

| Switch II   | Pull In Voltage |            |
|-------------|-----------------|------------|
|             | Measured        | Simulation |
| Temperature |                 |            |
| 293K        | 15V             | 4.8V       |
| 77K         | 20V             | 5.6V       |

In conclusion, the results indicate that variations in the pull-in voltage of the switch highly depend on the type of supports used in the design. This should clarify the claims made in the literature that the pull-in voltage of an RF switch increases when the temperature decreases. There are many factors that affect the mechanical performance of a switch in different environments, such as the mechanical design, residual stress, initial displacement, substrate material, and switch material. By choosing the appropriate values of these factors, one can increase, decrease, or fix the actuation voltage according to the application of the switch.

# Chapter 4 Analysis of Silicon and Alumina Substrates at Cryogenic Temperatures

Very limited data are available in the literature regarding the measurement of RF devices at cryogenic temperature (4K). Therefore, it is important to analyze the properties of the substrates and the superconducting metal layer both in a vacuum environment and at low temperatures. The two types of analyses performed in this investigation are thermal analysis and RF analysis.

## 4.1 Thermal Analysis

The cryogenic measurement for LTS-based devices is performed at the Lakeshore cryogenic probe-station [17]. As shown in Fig. 4.1, the probe-station has five temperature sensors at five different locations, namely, the radiation shield stage, the 4K shield stage, the sample stage, and one of the probe arms. The typical temperature for each stage is given in Fig. 4.1, but experiments show that these values can be reduced to 22K, 11K, 4.2K, 3K and 9K, respectively, with the use of an external pump.

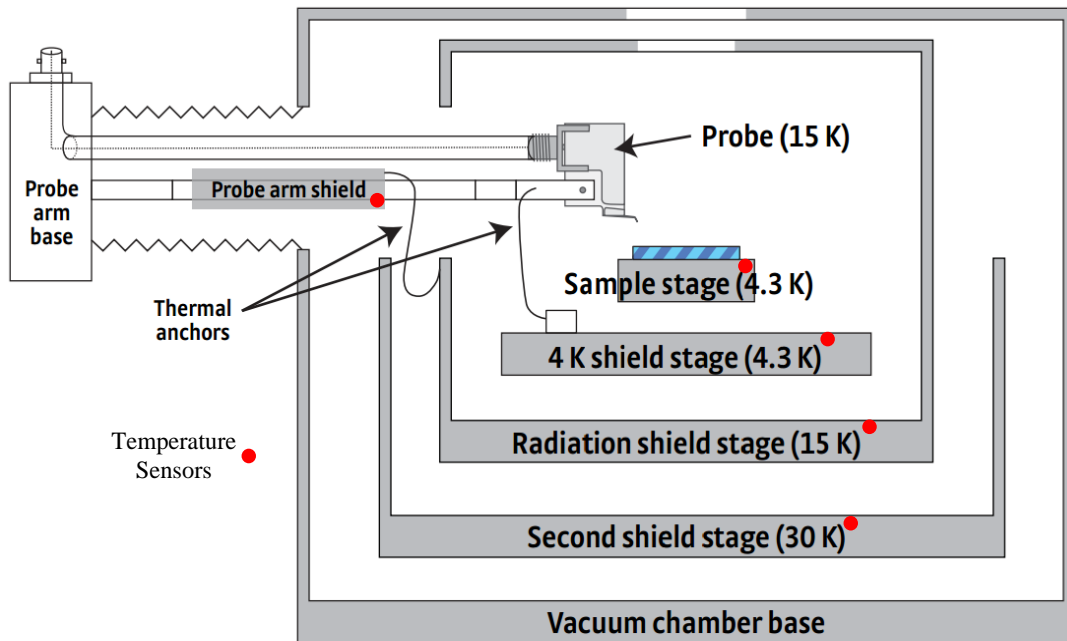


Fig. 4.1 Schematic of the four thermal shields of the Lakeshore cryogenic chamber and its typical temperature [17].

The chip is mounted on the chuck, as illustrated in Fig. 4.2. It is crucial to minimize the temperature variation between the sample stage and the mounted chip. Various types of mounting approaches are investigated, the first of which is Apiezon-N grease [18], a well-known type of adhesive typically used in a vacuum environment. The drawback of using this grease for low temperature measurement is that its thermal conductivity is only 0.005 W/mK. When working with superconductor materials, it is imperative that the superconductor be deep into its superconducting region, because even half a degree variation in temperature can affect the results. The measurement results of a 7-pole Nb-based bandpass filter (BPF) [19] show that, when using only Apiezon-N grease, the device is not sufficiently deep into the superconducting region.

A second possible approach proposed by Lakeshore cryogenics is to clamp the device on the chuck in order to apply a force to the chip, thereby increasing the thermal conductivity between the chip and the chuck. When using this device, the measurements show some improvement in the RF performance.

A third approach is using silver paint [20] to semi-permanently mount the chip on the chuck. The thermal conductivity of the silver paint is 429 W/mK, which is significantly greater than the thermal conductivity of the Apiezon-N grease. The BPF on two separate chips is measured in a cool-down run and similar calibration. One is mounted using a clamp and Apiezon-N grease, and the other is



mounted using only silver paint. The results show an approximate 1 dB of improvement in the insertion loss of the filter. Fig. 4.3 shows a comparison between the insertion loss of the 7-pole filter with a clamp and Apiezon-N grease, and with silver paint.

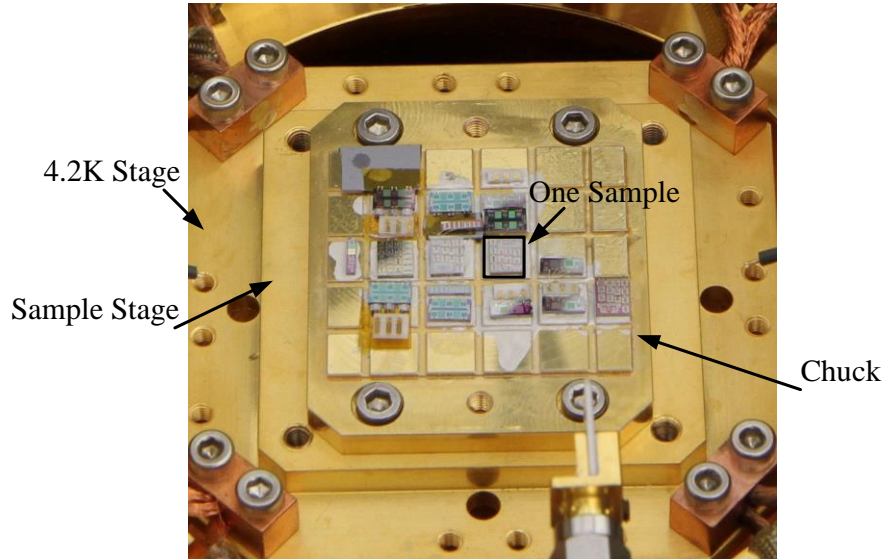


Fig. 4.2 Image of chips mounted on the chuck in the Lakeshore cryogenic probe-station.

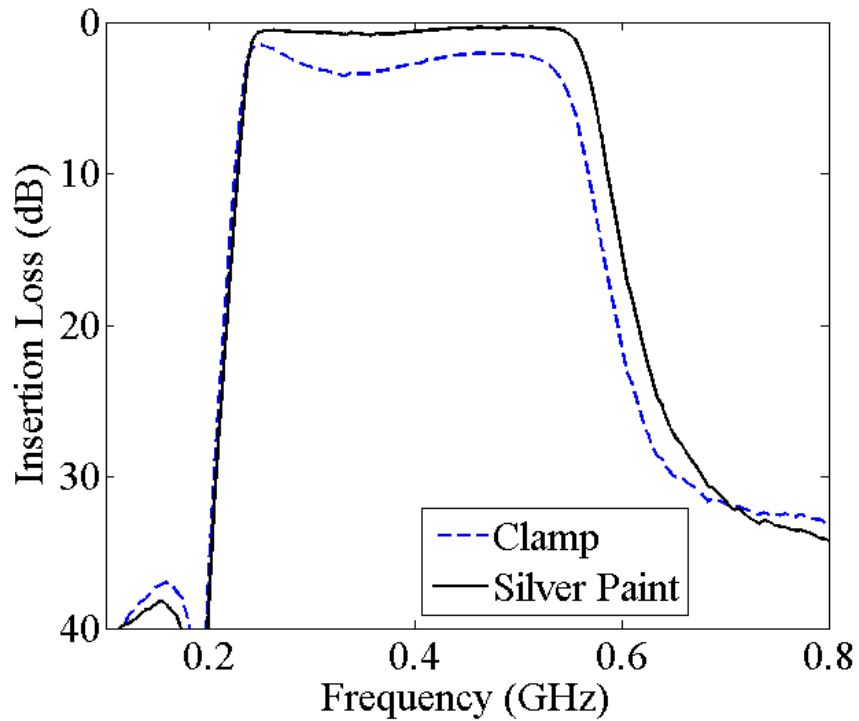


Fig. 4.3 Comparison between the insertion loss of two identical 7-pole BPFs at 4K. One is mounted on the chuck using a clamp and Apiezon-N grease, and the other is mounted on the chuck using only silver paint.

The simulation results of the temperature distribution across the device in COMSOL support the data. Fig 4.4 illustrates the model of the device for thermal analysis in COMSOL, showing a set of Nb-based CPW TL on a silicon (Si) substrate with a dimension of  $800\ \mu\text{m} \times 50\ \mu\text{m} \times 1\ \mu\text{m}$ . The substrate thickness is considered to be  $500\ \mu\text{m}$  and the thickness of the adhesive is considered to be  $300\ \mu\text{m}$ . RF probes are considered to be gold, with dimensions of  $30\ \mu\text{m} \times 5\ \mu\text{m} \times 1\ \mu\text{m}$ , according to the datasheet of Pico-probes [21]. The backside of the adhesive, mounted on the chuck, is considered to be 3K, and the probes' temperature is 9K. Fig. 4.5 (a) illustrates the simulation results of the model in COMSOL using Apiezon-N grease as an adhesive. It clearly shows that the substrate temperature is very close to 9K. Fig. 4.5 (b) illustrates similar simulation results but uses silver paint as the adhesive. The results indicate that most of the structure has a temperature very close to 3K, except for the parts located near the probes.

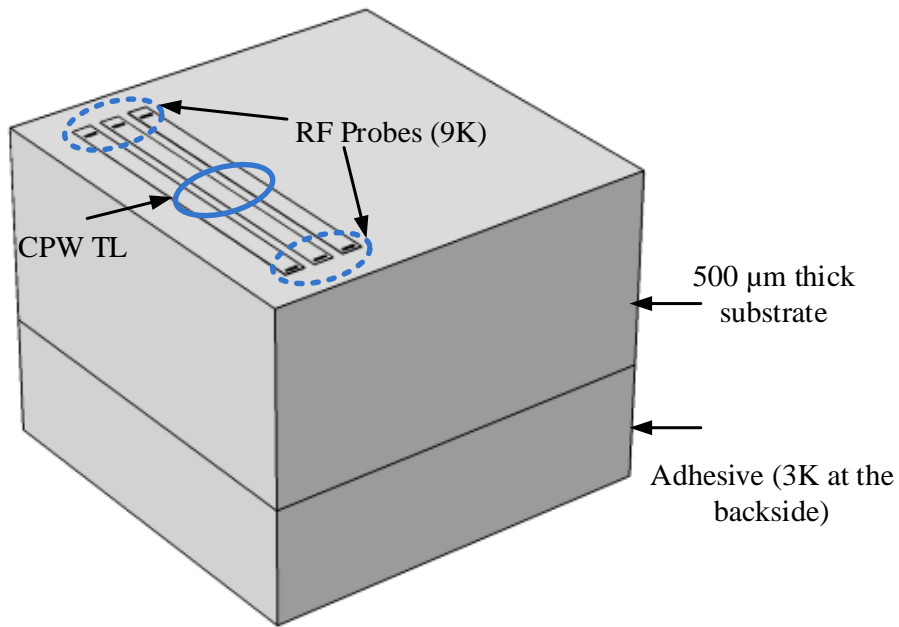


Fig. 4.4 A 3D model used to simulate temperature distribution across the device in COMSOL. It includes the adhesive material, the substrate, fabricated RF devices, and RF probes.

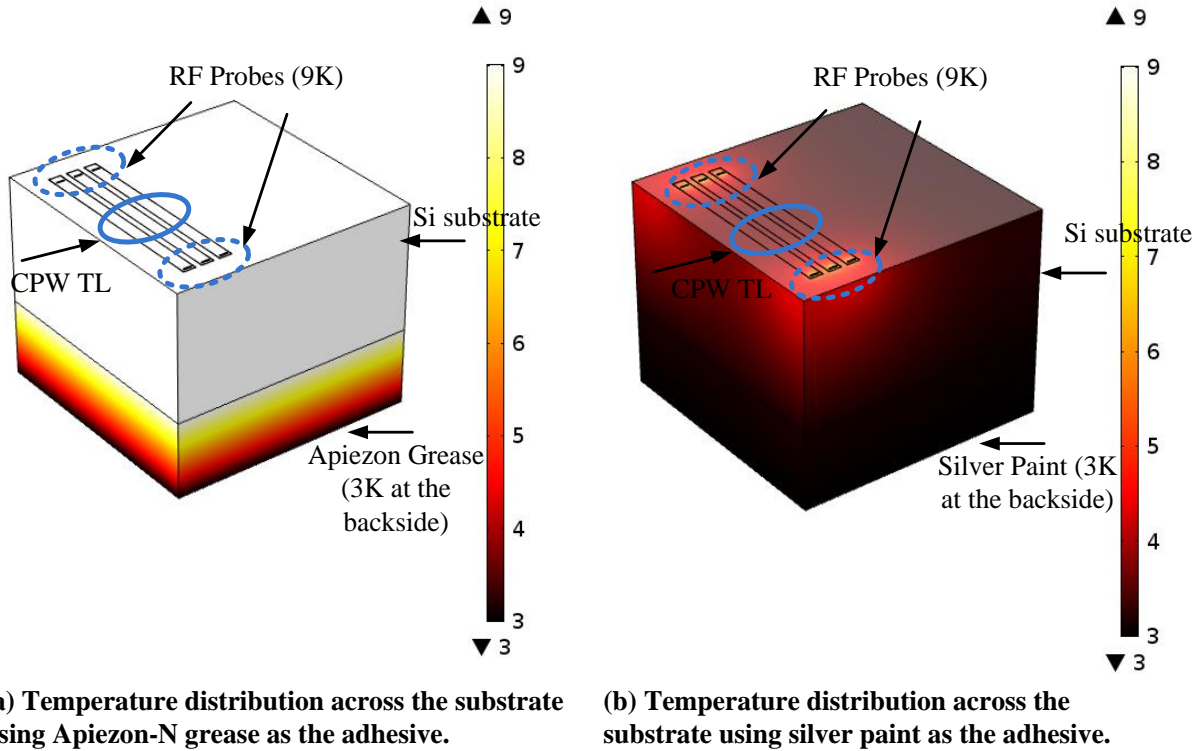


Fig. 4.5 Temperature distribution across the substrate and the fabricated RF devices using two types of adhesive: a) Apiezon-N grease, and b) silver paint.

Fig. 4.6 illustrates a comparison of the temperature distribution along the signal line for both types of adhesives. The figure shows that, for Apiezon-N grease, the temperature is very close to the temperature of the probes (9 K), which is due to the poor thermal conductivity of the grease. However, for silver paint, the temperature variations across the TL range from 3.7K to 5.5K. The effect of the probes can be reduced if they are touching a wafer that is thermally isolated from the actual device. Fig. 4.7 shows the thermal simulation in COMSOL for a similar model in which the main wafer is connected to the probes through a set of gold wirebonds and thermally lossy TLs. Titanium (Ti) is considered as the material for thermally lossy TLs. The thermal conductivity is 21.9 W/mK for Ti and 318 W/mK for gold. A comparison of the temperature distribution along the Nb-based and Ti-based TLs in Fig. 4.7 and Fig. 4.8 shows that the temperature of the Nb-based TL is very close to the temperature of the chuck. It should be mentioned that heat radiation from outside the chamber is not considered in this simulation, since only the effect of Ti-based TLs is under investigation.

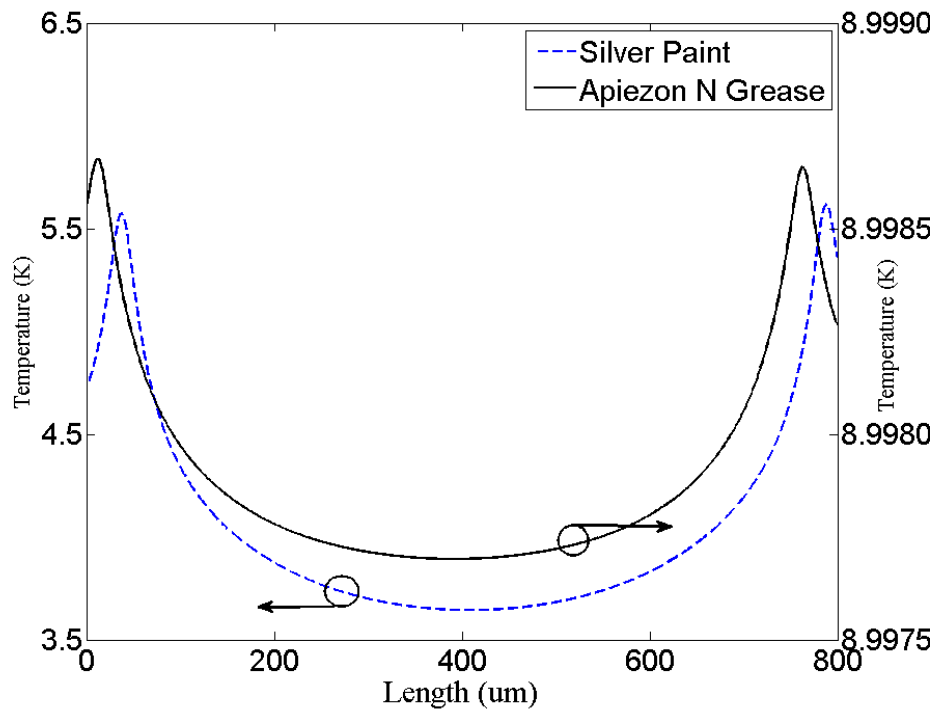


Fig. 4.6 COMSOL simulation results of the comparison of temperature distribution along the signal line for silver paint and Apiezon-N grease on silicon substrate.

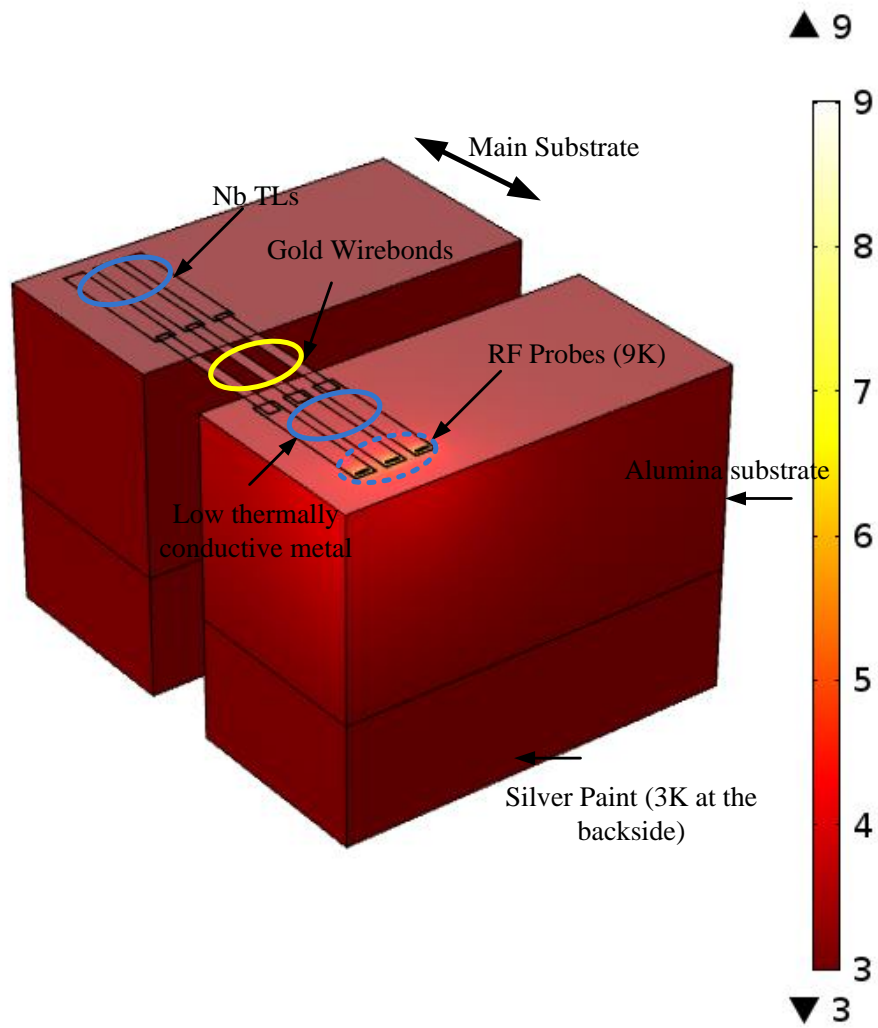


Fig. 4.7 Thermal simulation in COMSOL for a 3D model in which the Nb-based TLs are connected to the probes through a set of gold wirebonds and Ti-based TLs.

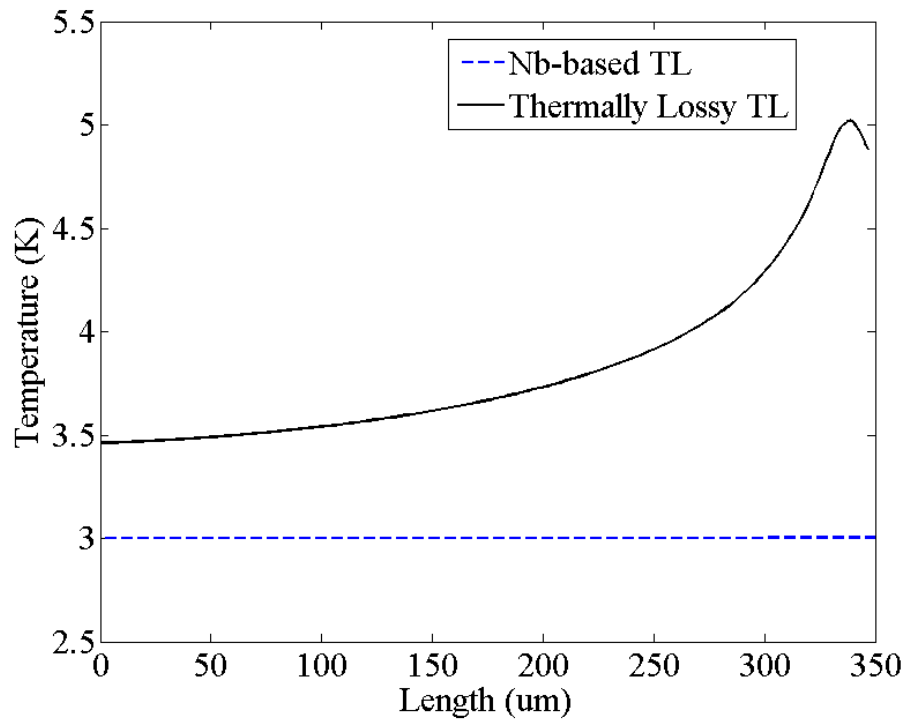


Fig. 4.8 A temperature comparison between the Ti-based TL and Nb-based TL, when the probes are touching the Ti-based TL.

In this research, superconducting devices are fabricated on two types of substrates: low resistive Si, and alumina. The thermal conductivity of Si and alumina are 130 W/mK and 35 W/mK, respectively. Since the thermal conductivity of Si is about 4 times greater than that of alumina, it is expected that the temperature of the superconducting device fabricated on Si would be lower than the temperature of the similar device fabricated on alumina. Fig 4.6 shows COMSOL simulation results of the temperature distribution across the signal line of a CPW TL (similar to Fig. 4.4) on Si and alumina substrates. The results indicate that although the minimum temperatures of the test structure on the two substrates are nearly the same, the area close to the probes has higher temperature values for alumina compared to Si.

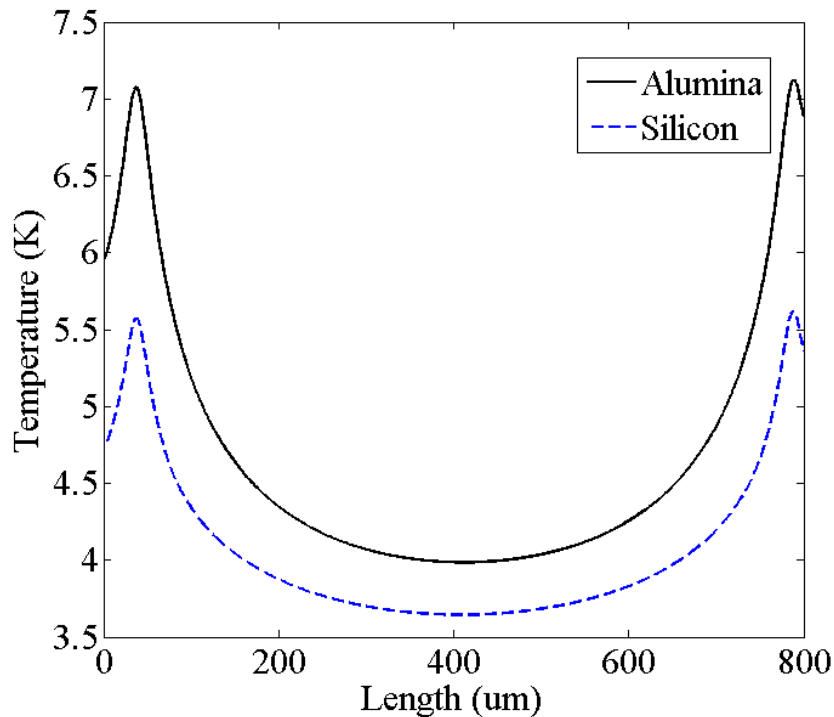


Fig. 4.9 COMSOL simulation results of temperature distribution across the signal line of a CPW TL on silicon and alumina substrates.

## 4.2 RF Analysis

According to [22], silicon acts as a dielectric at any temperature below 25K, due to the freeze-out of the free carriers. Because the silicon substrate provided by Hypres is a low-resistivity substrate, it is very critical to estimate the substrate loss at low temperature for the sake of RF design accuracy. To investigate the effect of a low-resistivity Si substrate on the capacitance value of a varactor, a set of Ground/Signal/Ground (G/S/G) pads are fabricated on the same substrate and measured at room and cryogenic temperatures. The extracted capacitance value of the G/S/G pads obtained from the measured results at room and at cryogenic temperatures is shown in Fig. 4.10. The result indicates that, at room temperature, an additional capacitance is added to the total capacitance value between the signal and the ground pads, which is more evident at a low frequency range. The added capacitance is the effect of the lossy silicon substrate and the native oxide on top of it. The extracted circuit is depicted in Fig. 4.11 and the fitted simulation at room temperature is shown in Fig. 4.10. The L and C values of the extracted circuit depends on the properties of silicon substrate and the thickness of the thermal oxide on top of it, which may vary in each fabrication run.

In Fig. 4.10, we can see that, at cryogenic, the extracted capacitance value is almost constant versus frequency, which indicates the elimination of the substrate loss. The capacitance value at room temperature converges to its value at cryogenic temperature at frequencies higher than 4 GHz, indicating that the effect of the added capacitor is less at higher frequencies.

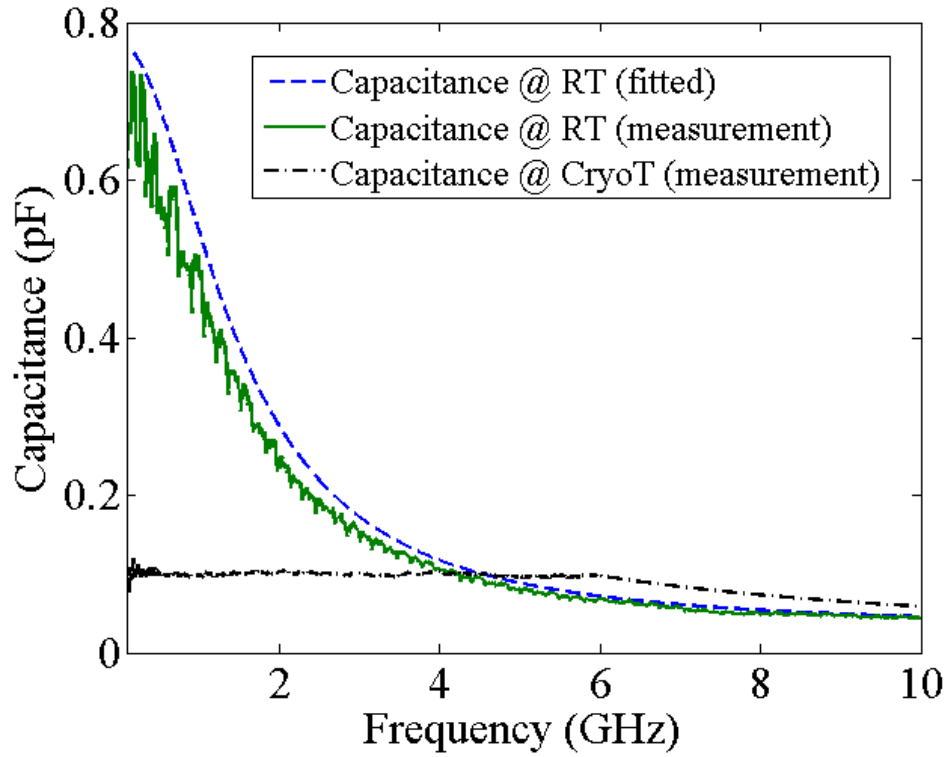


Fig. 4.10 The measured and fitted results of the capacitance variation of the G/S/G pads vs. frequency at room and cryogenic temperatures.



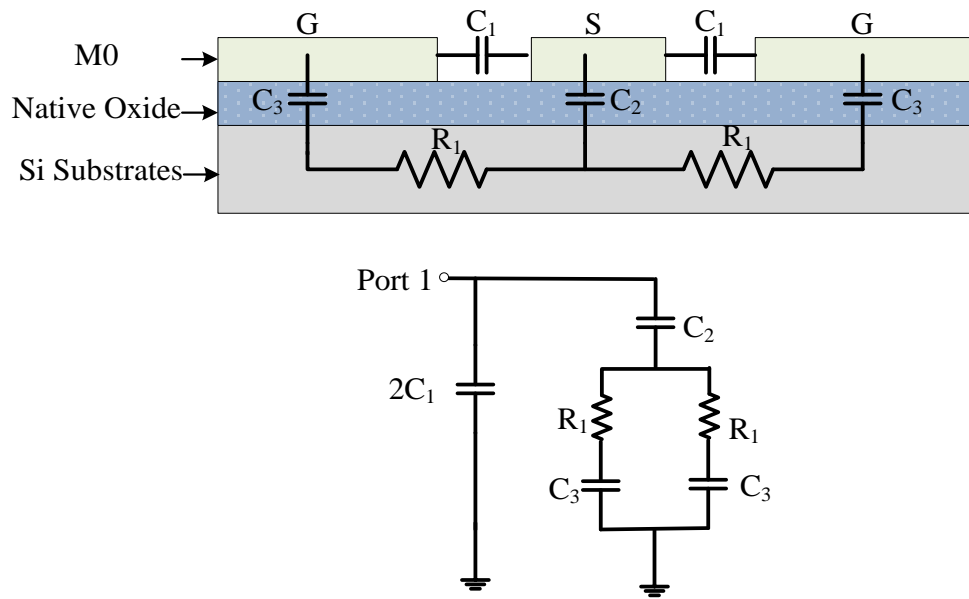


Fig. 4.11 Circuit model of the G/S/G pads at room temperature.

To further investigate silicon resistivity variation by temperature, a gold-based CPW transmission line is fabricated on the same silicon substrate as the niobium devices. Fig. 4.12 shows the measured and fitted simulation results of the transmission line at 293K and 4K. The improvement in the insertion loss of the transmission line is due to the elimination of the substrate loss at 4K and the improvement of gold conductivity.

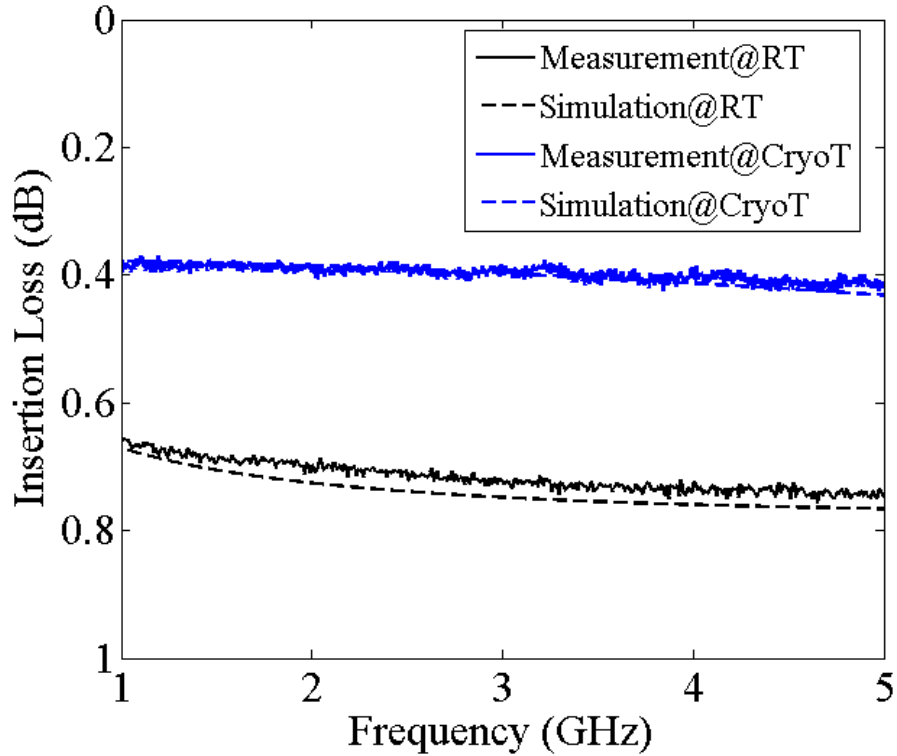


Fig. 4.12 The measured and fitted simulation results of the gold-based transmission line at 293K and 4K, to demonstrate the effect of the silicon substrate loss.

In conclusion, it is critical to choose the appropriate substrate according to the application of the superconducting devices. Substrates with higher thermal conductivity reduce thermal loss. The type of adhesive used is also critical, since a temperature variation of only 1 K can change the loss of the device and the superconducting behavior of the LTS material.

# Chapter 5 Development of RF MEMS Devices Using Nb-Based Multilayer Process

Nb is an element and shows superconducting properties, type II, when it is cooled below its critical temperature. The critical temperature of Nb is 9K, which can be reached using liquid helium. The main advantage of using an Nb-based fabrication process is to realize highly miniaturized multilayer low-loss RF devices. The process is also amenable to integration with MEMS devices, making it possible to realize highly miniature low-loss reconfigurable RF devices.

This chapter presents the Hypres fabrication technique and the post-processing steps that are applied for releasing the MEMS part of the SME chip. Fine-tuning of the post-processing steps is also discussed. Later in this chapter, simulation and measured results of different types of MEMS switches, varactors, tunable resonators and tunable filters are presented for implementing the Hypres fabrication procedure.

## 5.1 Hypres Fabrication Technique

To date, Hypres is one of the few companies in the world that produce and market digital superconducting electronic products. Some examples of these products include Superconductor-Insulator-Superconductor (SIS) mixers, all-digital receivers, and analog-to-digital and digital-to-analog converters [24].

A description of the Hypres process is given in Fig. 5.1 Three metal Nb layers, M0, M2 and M3, have a thickness of 100 nm, 300 nm and 600 nm, respectively, and three silicon dioxide ( $\text{SiO}_2$ ) layers, with thicknesses of 150 nm, 200 nm and 500 nm (from the bottom to the top layer) are used as the dielectric. There is also one resistive layer (R2), which is Molybdenum (Mo) or Ti (Titanium)/Au-Pd(Palladium)/Ti, depending on the required current density. M1 is an Nb/ $\text{AlSiO}_2$ /Nb tri-layer, and R3 is the gold layer, which is the top-most layer that covers the pads.

The main advantage of this process is the use of very thin dielectric layers that permit the realization of highly miniaturized parallel plate capacitance values and thus serve as miniaturized RF devices. Another advantage of this technology is its capability of realizing very fast, low-loss and noise-free active devices. The fabrication process is also amenable to the realization of RF MEMS devices, which is the only solution for integrating reconfigurable RF front-ends into an SME receiver chip and achieving a single-chip solution.

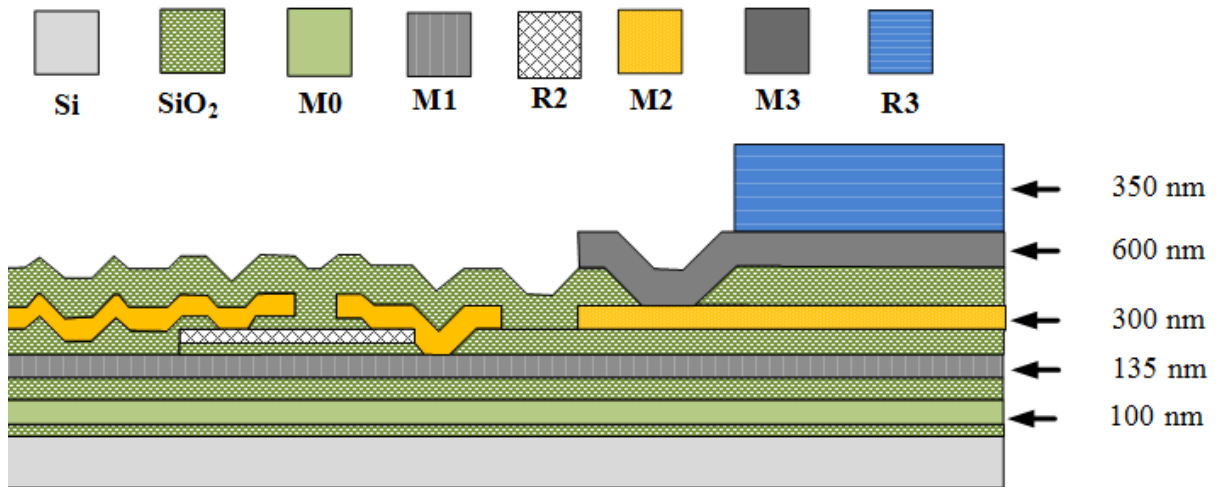


Fig. 5.1 Cross Section of the Hypres Process [4].

To fabricate MEMS devices using the Hypres foundry, several steps of post-processing are required. Through post-processing, the mechanical parts of the MEMS device are able to be released. Releasing a MEMS structure implies removing the sacrificial layer from underneath the movable part(s) of the device. The sacrificial layer can be selected to be one (or more) of the oxide layers or one of the metal layers.

### 5.1.1 Traditional Post-Processing Technique

The post-processing technique is based on selecting and removing one or two of the oxide layers as the sacrificial layer. It starts with a chip fabricated in the Hypres foundry. Fig. 5.2 shows the steps of the procedure. First, the protective PR layer is removed. The chip is immersed in pure Acetone for 19

min followed by 1 min of ultrasonic bath at minimum power and room temperature. Throughout this step, the chip is kept in pure acetone to remove the PR residue. This is followed by 2 min in water and 2 min in pure Isopropanol (IPA). PAD Etch 4 (Air Products and Chemical, Inc.) is used to remove the sacrificial layer, which is made of silicon dioxide. The etching time varies among different chips, depending on the minimum feature that needs to be released. Since both the sacrificial and dielectric layers use the same SiO<sub>2</sub> material, patterned metal layers are used to protect the dielectric layer from unwanted etching during the sacrificial layer removal step. The protective layer is extended to minimize the effect of under-etch, and release holes are introduced in the M3 layer to allow fast and isotropic etching of the SiO<sub>2</sub> sacrificial layer underneath it. Finally, the device is dried in a critical-point dryer system to prevent stiction after the wet etching step.

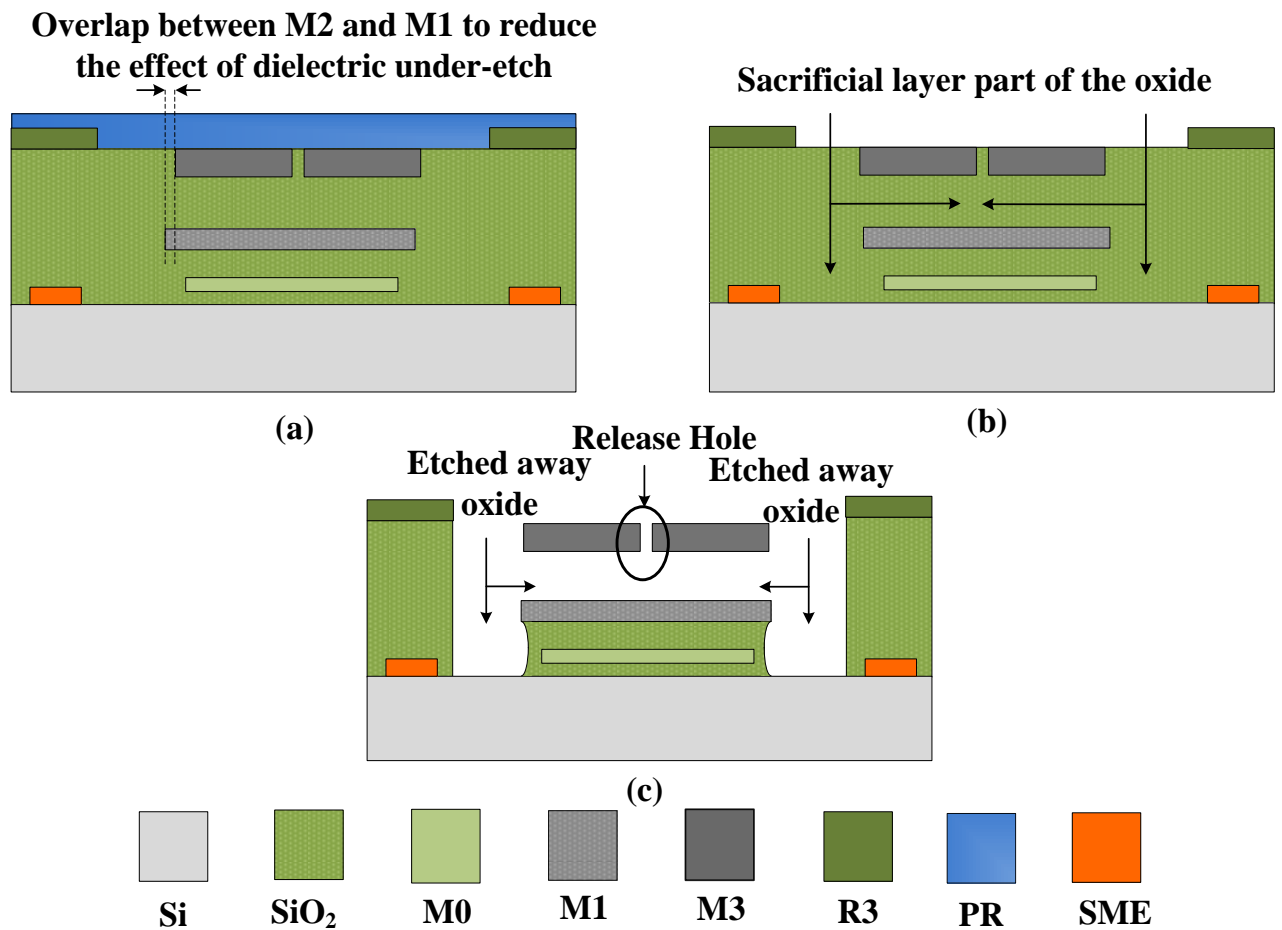


Fig. 5.2 The post-processing steps to release the MEMS structure [25].

The main advantage of this technique is being able to use the maximum air gap of  $0.7\ \mu\text{m}$ , which is between the M3 and M1 metal layers. This will achieve the maximum allowable tunability in varactors and isolation/insertion loss in the contact switches and capacitive switches. Furthermore, when the top plate snaps down onto the bottom plate, the thinnest dielectric layer (i.e., the one between M0 and M1) isolates the two plates. A high down-state capacitance value can be achieved for the varactors or the capacitive RF MEMS switches fabricated using this technique.

One of the main challenges of this technique is to optimize the release hole dimensions in order to achieve a reasonable release time while preventing any damage to the Nb itself by the wet etchant. As an initial step, the dimensions of the release holes are chosen similar to the minimum feature size of the M3 metal layer specified by the Hypres design rule, which is  $2\ \mu\text{m} \times 2\ \mu\text{m}$ . Experimentation shows that the release time required for such dimensions is about 15 min. The release hole dimensions and spacing are then varied and the release time is increased accordingly. Fig. 5.3 shows SEM images of several cantilever beam test structures with release hole dimensions varying in size from  $2\ \mu\text{m} \times 2\ \mu\text{m}$ , with spacing of  $2\ \mu\text{m}$  between each pair of holes, to  $6\ \mu\text{m} \times 6\ \mu\text{m}$ , with spacing of  $7\ \mu\text{m}$ . The release time varies from 13 min to 30 min. Results indicate that a minimum release time of 30 min is required to etch the test structure with the least number of release holes.

There is a tradeoff between the dimensions of the release holes and the release time. They should be selected such that there is no damage to the rest of the device. For example in the case of lumped element filters and resonators, the size of the inductors cannot tolerate a long etching time.

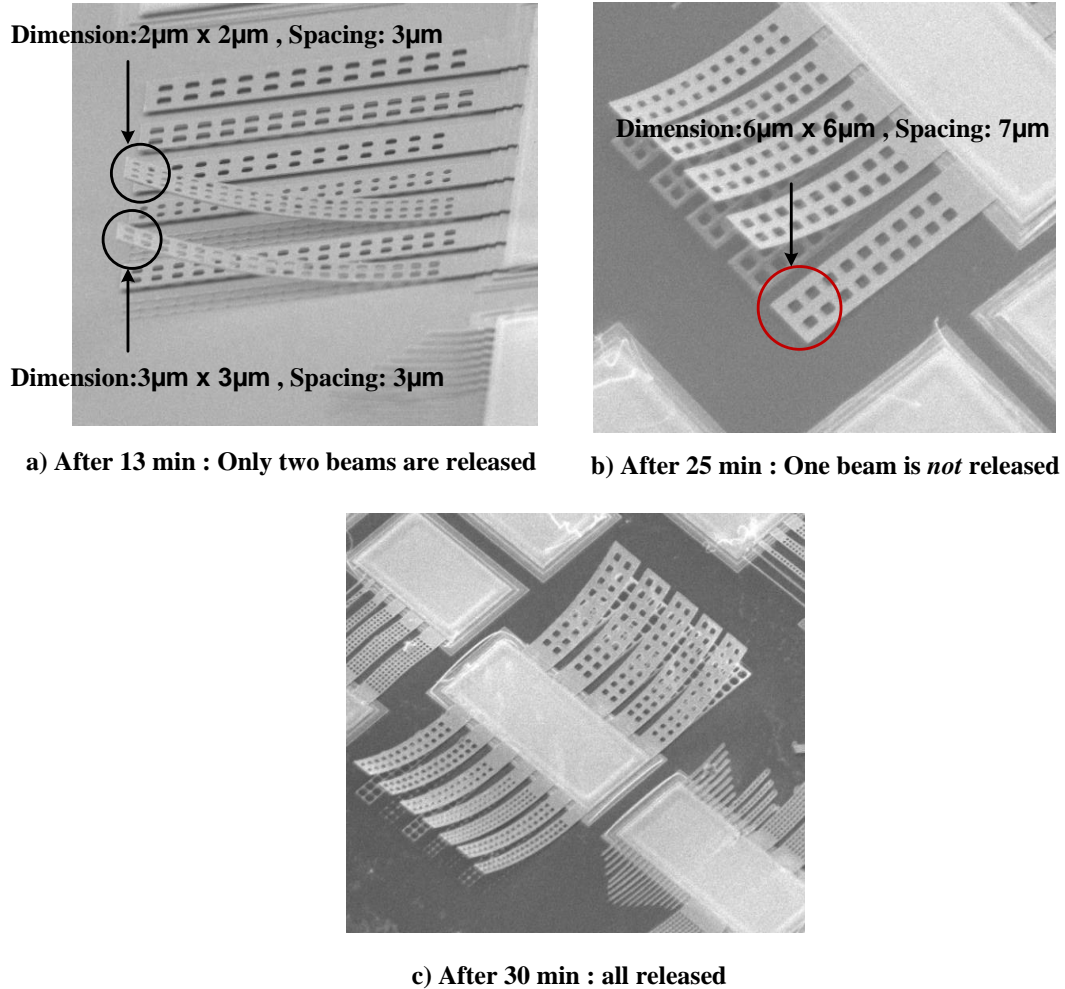


Fig. 5.3 SEM images of several cantilever beam test structures with release hole dimensions varying from  $2\mu\text{m} \times 2\mu\text{m}$  and spacing of  $2\mu\text{m}$  between each two holes, to  $6\mu\text{m} \times 6\mu\text{m}$  and spacing of  $7\mu\text{m}$ .

### 5.1.2 Stress Analyses

Generally, the residual stress induced to a thin film is caused by thermal mismatch in the metal layer itself ( $\sigma_1$ ), along with the difference in the Coefficient of the Thermal Expansion (CTE) between the metal layer ( $23.1 \times 10^{-6} \text{ 1/K}$ ) and the  $\text{SiO}_2$  sacrificial layer ( $0.5 \times 10^{-6} \text{ 1/K}$ ). The former causes beam out-of-plane deflection, while the latter causes beam axial deformation.

Accurate characterization of stress-induced deformation is crucial for the design and implementation of MEMS devices using the Hypres fabrication process. Residual stress values of the M3 metal layer are determined by conducting experiments on several cantilever beams and fixed-fixed beams.

Fig. 5.4 shows an SEM image of an array of released cantilever beams with lengths from  $30\mu\text{m}$  to  $50\mu\text{m}$ , used as test structures for stress analysis. The figure also illustrates that the beam's out-of-plane

deflection is dominant. [26] shows that the bending curvature of the cantilever beam is related to the residual stress value by (5.1).

$$\rho_x = \frac{EH}{2\sigma_1} \quad (5.1)$$

where  $E$  is the Young's modulus of the material, which is 105 GPa for Nb,  $H$  is the thickness of the beam (600 nm in this case), and  $\rho_x$  is the radius of curvature. The measured deflection profile of a  $40\ \mu\text{m} \times 7\ \mu\text{m}$  Nb-based beam using an optical interferometer WYKO is shown in Fig. 5.5. The stress gradient obtained from different cantilevers is averaged to be  $150 \pm 0.5$  MPa. As illustrated in Fig. 5.5, the measured deflection profile agrees with the simulation results using COMSOL.

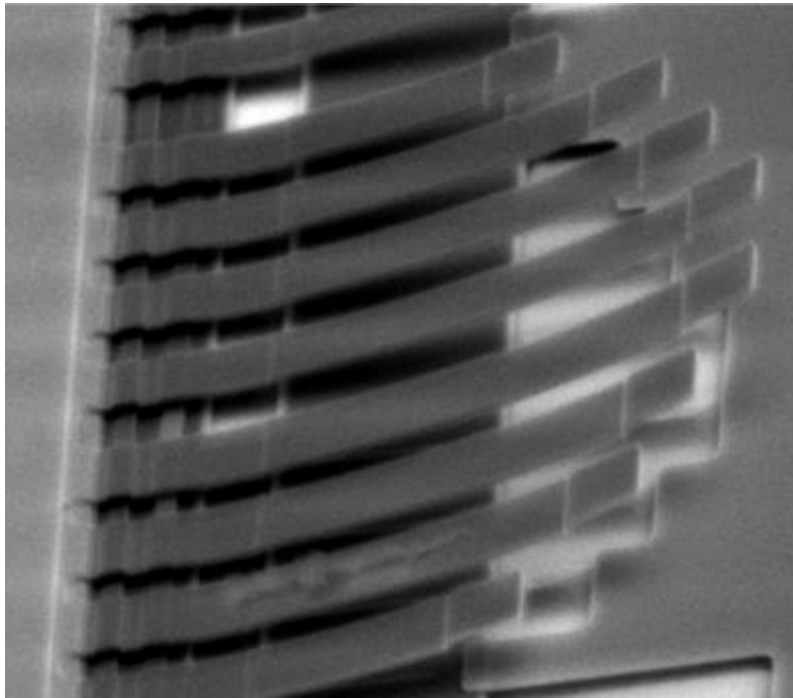


Fig. 5.4 The SEM image of an array of released cantilever beams.



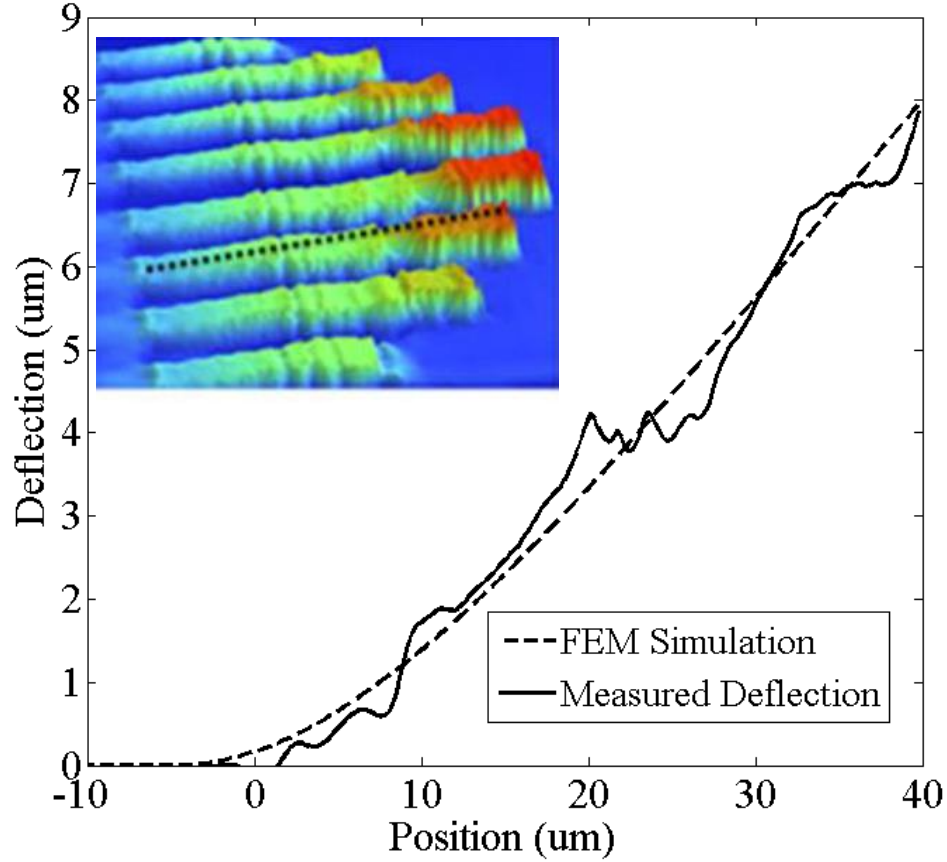


Fig. 5.5 Measured deflection results of the cantilever beam and FEM simulation results for  $150 \pm 0.5$  MPa gradient stress.

Residual stress values of the M3 metal layer are also determined by conducting experiments on several fixed-fixed beams. Fig. 5.6 shows the SEM image of an array of released beams. The beams have an equal length of  $80 \mu\text{m}$ , but the width varies from  $5 \mu\text{m}$  to  $22 \mu\text{m}$ .

If the total residual stress induces compressive load to a restrained beam, buckle-up occurs [26]. The first critical buckling mode is when a beam snaps from the straight position to the first critical buckling shape  $\psi_1(x)$ ,

$$\psi_1(x) = C_1(1 - \cos(\lambda_1 x)) \quad (5.2)$$

$$\lambda_1 = \frac{2\pi}{L} \quad (5.3)$$

where  $C_1$  is a constant,  $\lambda_1$  is the deflection of the beam at point  $x$ , and  $L$  is the length of the beam. The compressive force that causes the first buckling mode of the beam is obtained by [26].

$$P_{cr1} = \frac{\sigma_1 H}{\rho_x} \quad (5.4)$$

$$I = \frac{WH^3}{12} \quad (5.5)$$

where  $W$  is the width of the beam and  $I$  is the moment of inertia. Obtaining the beam deflection at point  $x$  by a profilometer, the compressive force induced to the beam is calculated by (5.6), where  $A = WH$ . [26]

$$P = \left( \frac{C_1^2 A}{4I} + 1 \right) P_{cr1} \quad (5.6)$$

The measured deflection profile of an  $80 \mu\text{m} \times 14 \mu\text{m}$  Nb-based beam using an optical interferometer WYKO is shown in Fig. 5.7. The stress gradient obtained from different beams is averaged to be 100 MPa. As illustrated in Fig. 5.7, the measured deflection profile agrees with the simulation results using COMSOL.

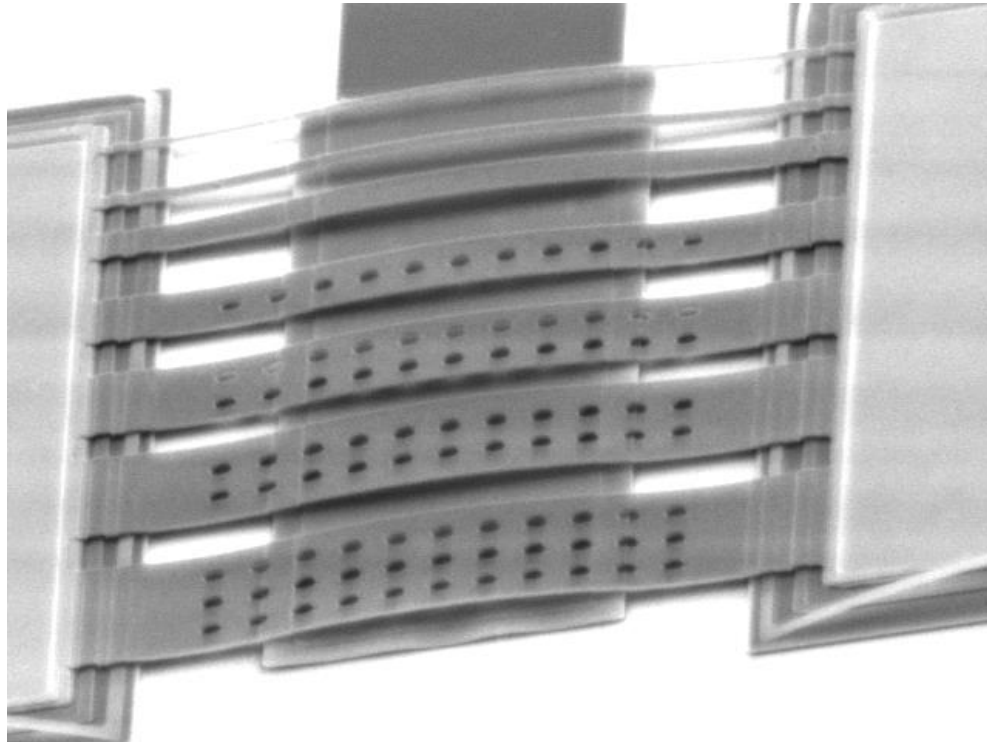


Fig. 5.6 The SEM image of an array of released restrained beams.

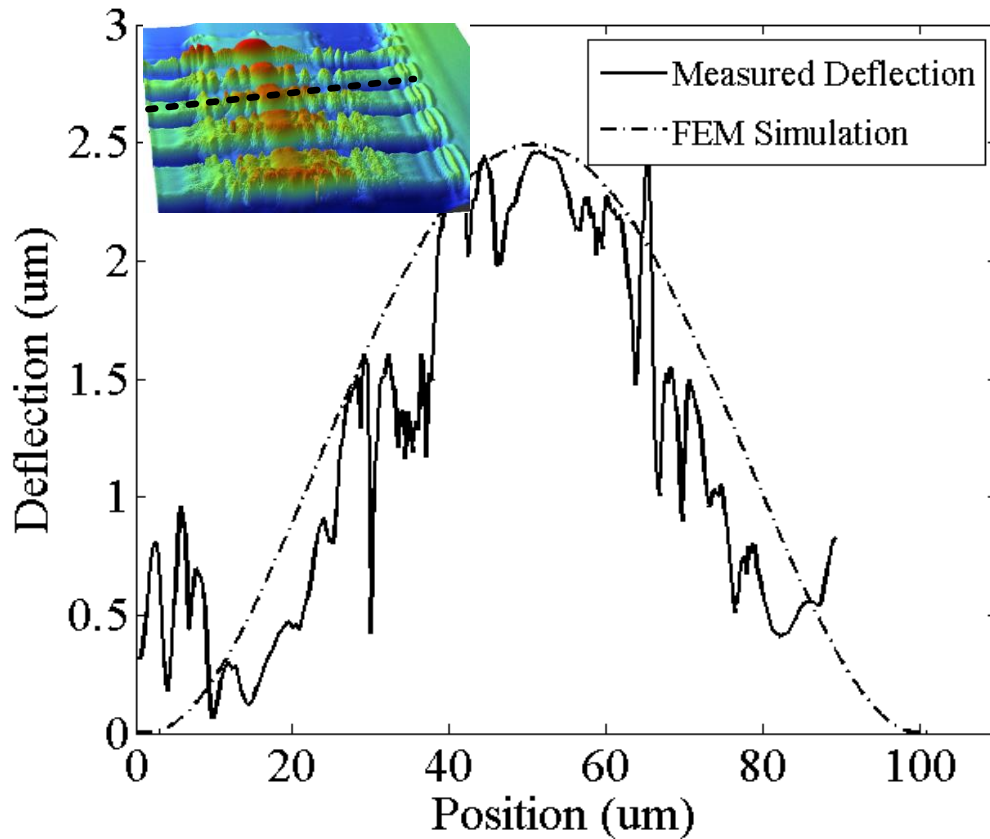
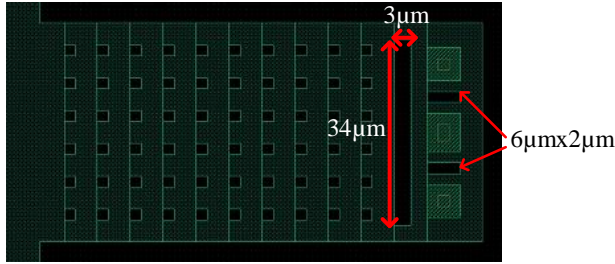


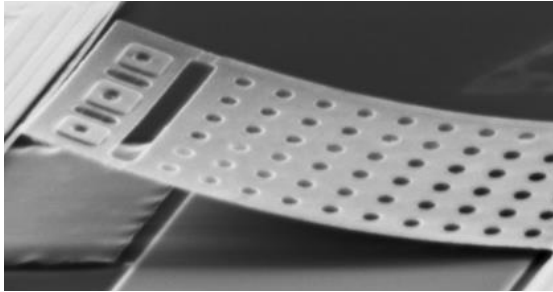
Fig. 5.7 Measured deflection results of the fixed-fixed beam and FEM simulation results for 100 MPa gradient stress.

### 5.1.3 Forming Dimples

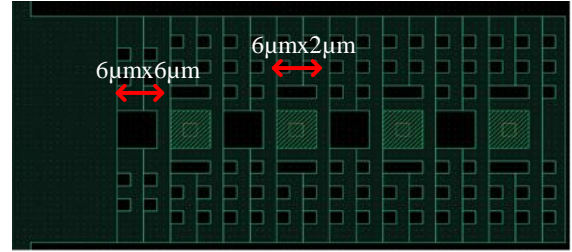
Since the Hypres fabrication process is not designed for MEMS devices, there is no fabrication step to create dimples. Many test structures are designed to form dimples using the available metal layers. Fig. 5.8 shows SEM images of several types of dimple designs that are formed by connecting two metal layers through vias. The challenge here is being able to remove the sacrificial layer underneath the dimples. Release times of 30 min and 35 min are used to investigate the effect of time on the release process as well as on the damages of the wet-etchant to Nb. After performing many experiments, the following structures are successfully released without damaging Nb metal layers.



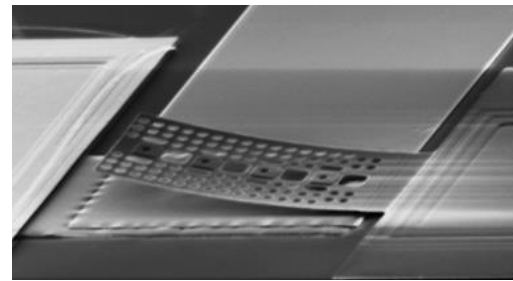
Other release holes are  $2\mu\text{m} \times 2\mu\text{m}$ , with the spacing of  $4\mu\text{m}$



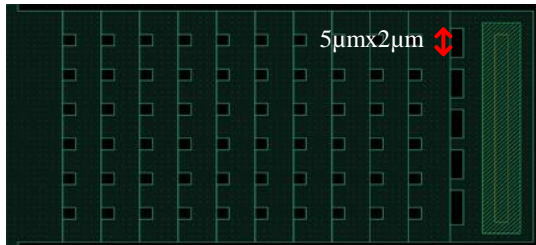
Release time = 30 min



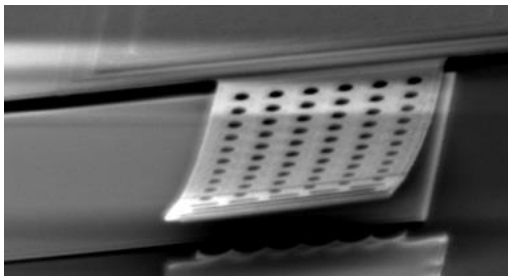
Other release holes are  $2\mu\text{m} \times 2\mu\text{m}$ , with the spacing of  $2\mu\text{m}$



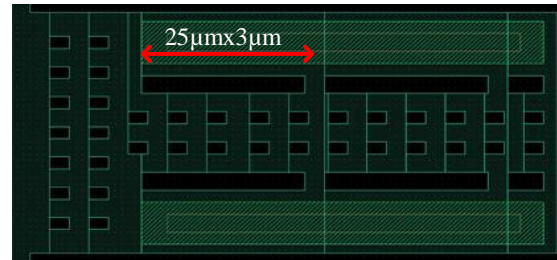
Release time = 30 min



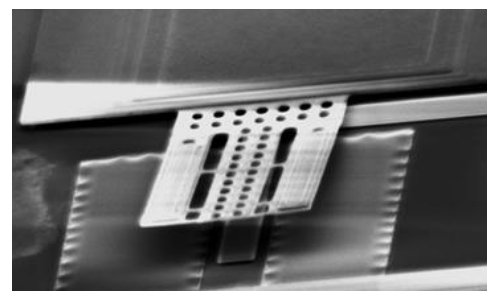
Other release holes are  $2\mu\text{m} \times 2\mu\text{m}$ , with the spacing of  $4\mu\text{m}$



Release time = 35 min



Other release holes are  $3\mu\text{m} \times 2\mu\text{m}$ , with the spacing of  $2\mu\text{m}$



Release time = 35 min

Fig. 5.8 SEM images of several designs to develop dimples using the fabrication process offered by Hypres.

## 5.2 Nb-Based RF MEMS Switches

Several MEMS switches can be designed, fabricated and characterized by employing the Hypres process. After receiving the chip from the foundry, the traditional MEMS post-processing technique is used to release the MEMS structures. While numerous papers have been published in the literature

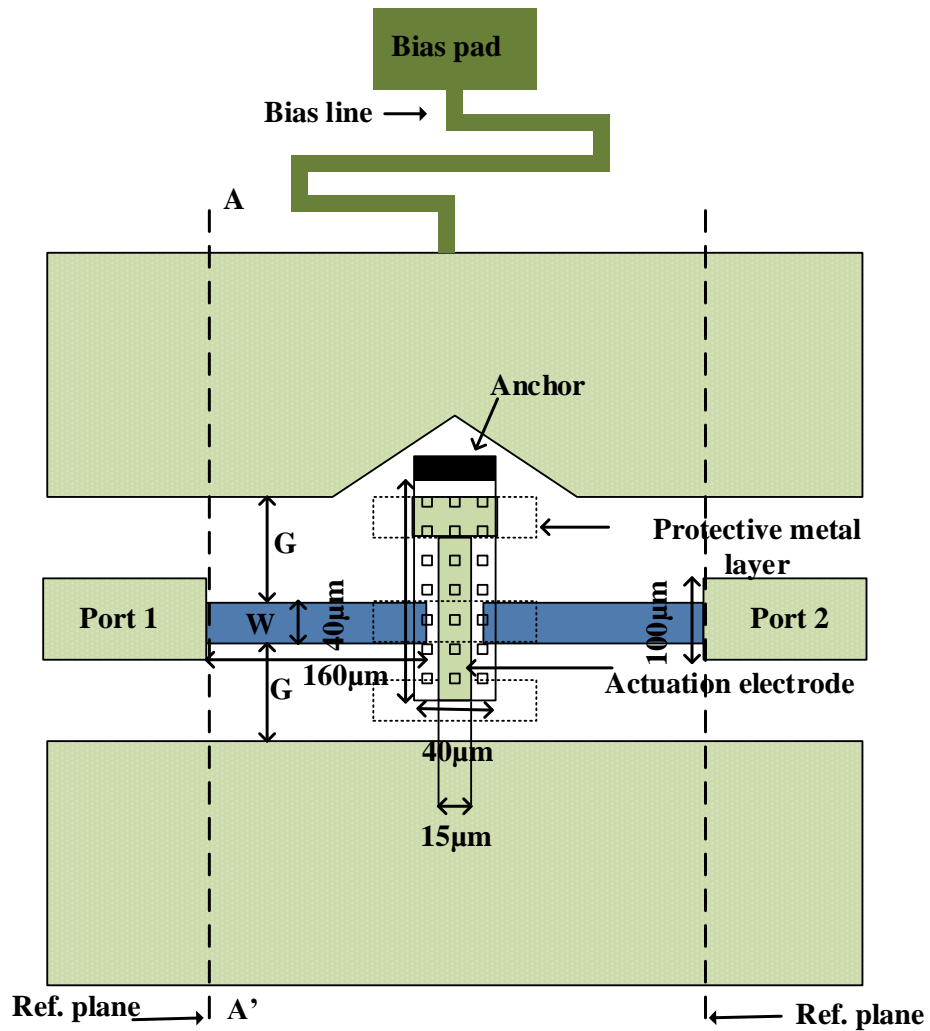
about conventional room temperature RF MEMS switches [29, 30], only a few publications have reported on RF MEMS switches operating at cryogenic temperatures [10] [31]-[33], and absolutely no measured results are available in the literature regarding niobium-based superconducting RF MEMS switches. In contrast to CMOS technology, the SME technology is not capable of realizing varactors or switches. RF MEMS switches and switched capacitors are the only solution to integrate reconfigurable RF front-ends into the SME receiver chip to achieve a single-chip solution.

### 5.2.1 DC-Contact RF MEMS Switch

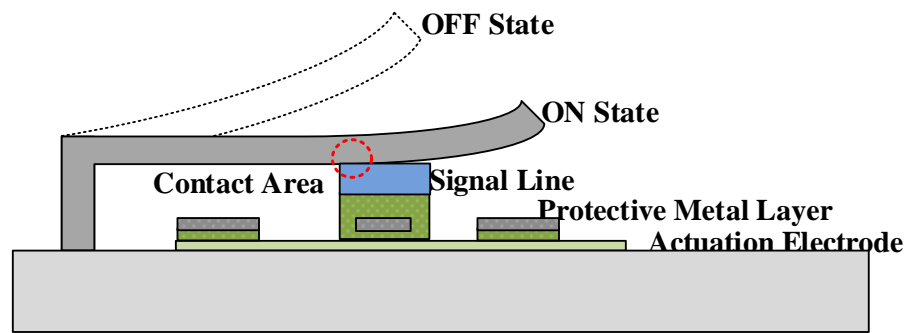
A dc-contact RF MEMS switch is realized by having metal-to-metal contact between a moving beam and an RF circuit. The switch is ‘off’ when the beam is in the up-state position and no dc-voltage is applied. The switch is ‘on’ when a dc-voltage is applied and forces the beam to be in its down-state position. Thus, the discounted signal line is connected through the switch.

#### Switch Design

Fig. 5.9 depicts the top view and cross-section view of the proposed switch. The switch consists of a coplanar waveguide (CPW) transmission line section and a warped plate anchored to the substrate and suspended over the centre conductor. The warped plate is on an M3 metal layer with a thickness of  $0.6\ \mu\text{m}$ , and the signal line is on M2 metal layers. The  $\text{SiO}_2$  layer between M3 and M2, with a thickness of  $0.5\ \mu\text{m}$ , is used as the sacrificial layer. The actuation electrode is on an M0 metal layer. To prevent any short between the beam and the actuation electrode, part of the dielectric layer is sandwiched between M0 and M1. The switch is designed such that the cantilever beam comes in contact with the two sides of the signal line where there is a discontinuity; this serves to connect the two sides prior to touching the actuation pad. However, the actual contact area is much smaller than this value, due to the surface roughness and the beam deflection [34]. To actuate the beam, a dc-bias voltage is applied between the beam and the actuation electrode, the latter which consists of two pads measuring  $80\ \mu\text{m} \times 15\ \mu\text{m}$  and  $40\ \mu\text{m} \times 20\ \mu\text{m}$ . The bias voltage is applied through the resistive metal layer (R2). To reduce the pull-in voltage, the actuation electrode is extended very close to the anchor, where the air gap between the cantilever beam on M3 and the M1 protective metal layer on top of the actuation electrode is as small as  $0.7\ \mu\text{m}$ .



(a) Top View



(b) Cross-sectional view (A-A')

Fig. 5.9 The top view (a) and the cross-section (b) of the superconducting RF MEMS switch in the 'off' and 'on' states.

The switch is mounted on a CPW transmission line with a dimension of  $60\ \mu\text{m} / 40\ \mu\text{m} / 60\ \mu\text{m}$ . The cantilever beam is  $100\ \mu\text{m} \times 40\ \mu\text{m}$ . Fig. 5.10 shows the circuit model of the switch in the ‘off’ and ‘on’ states. Due to the sandwich layer of  $\text{SiO}_2$  between M0 and M1, there is a capacitor in the dc-bias line path,  $C_b$ . The extracted up-state capacitance value of the switch is  $20\ \text{fF}$ . The contact resistance of the switch in the on-state is very close to zero due to its superconducting behavior at cryogenic temperature. Fig. 5.11 shows an SEM image of the released switch.

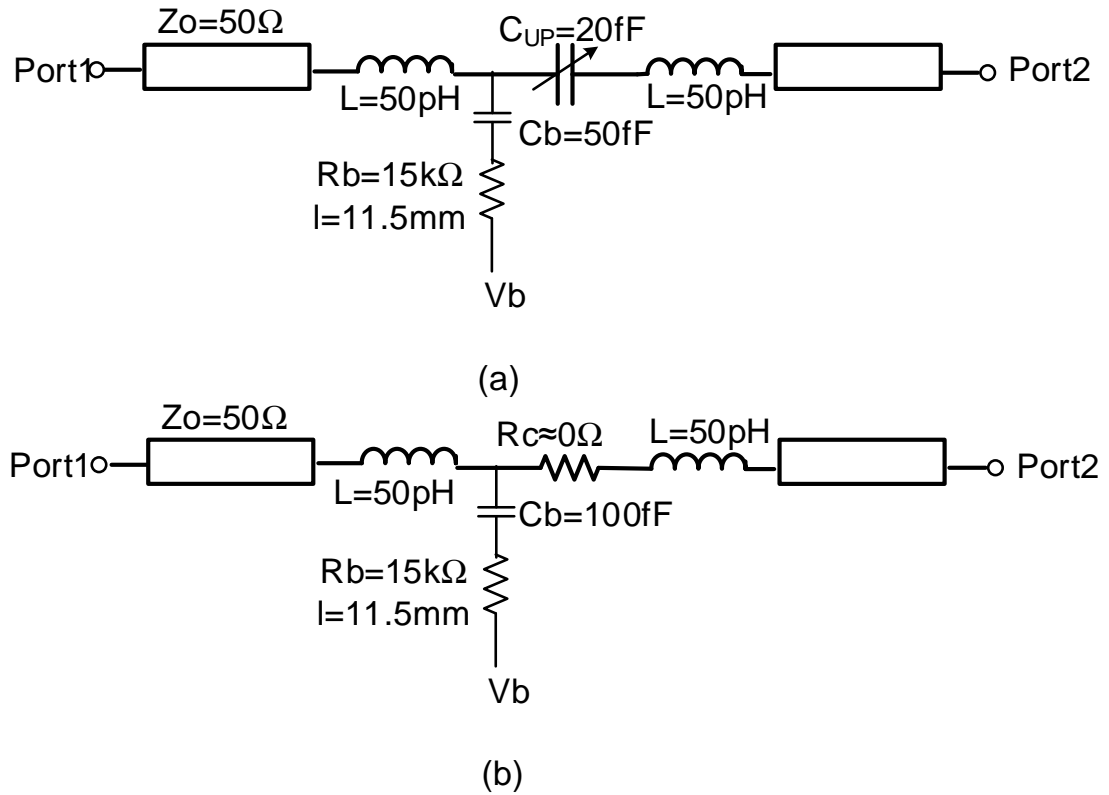


Fig. 5.10 Circuit model of the RF MEMS switch in the ‘off’ (a) and ‘on’ (b) states:  $R_b$  is the DC bias line resistivity and  $l$  is the length of the DC bias line.

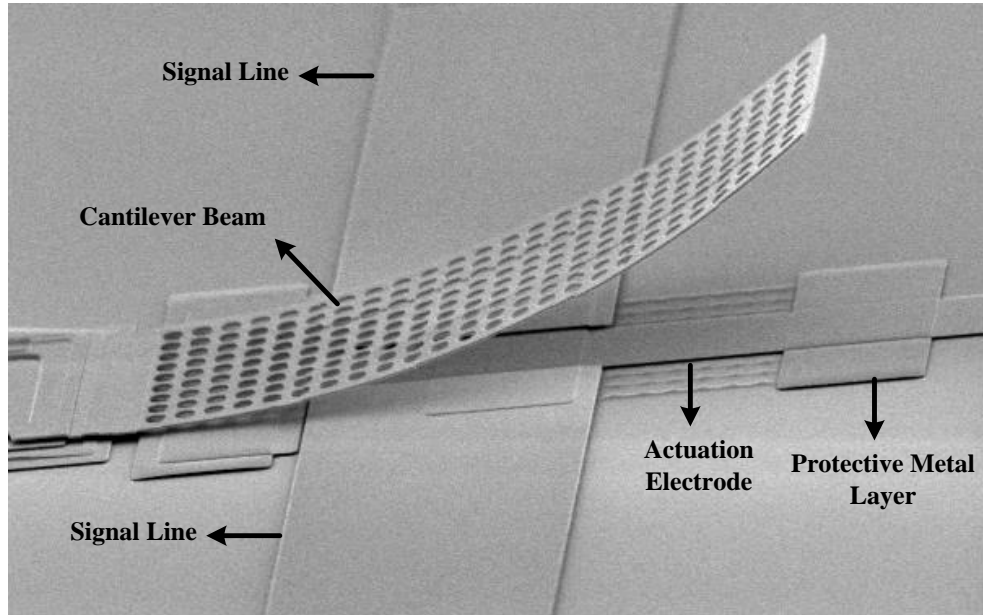


Fig. 5.11 The SEM image of the niobium superconducting RF MEMS switch after release.

### Simulation Results

Two types of simulation (mechanical and RF) are usually required for any RF MEMS switch. However, for this specific switch, thermal analysis is also required, since it works in a cryogenic environment.

Residual stresses present in the M3 metal layer cause warping of the cantilever beam of the proposed RF MEMS switch after removing the sacrificial layer. This property is advantageous, however, for improving the switch's isolation. To illustrate this concept, a finite-element analysis with COMSOL is performed to simulate the warpage of the cantilever beam. Using the same FEM simulator, the effect of temperature reduction on beam deformation is also investigated, and the RF performance of the switch is simulated using Ansoft High Frequency Structure Simulator (HFSS) software [35].

### Mechanical Simulation

Fig. 5.12 shows the final simulation result in COMSOL for the proposed superconducting MEMS switch deflection. An initial load is applied to the beam from the residual stress value obtained in section 5.1.2. The maximum simulated tip deflection of the warped plate is  $8.9 \mu\text{m}$ , which is very close to the measured value of about  $10 \mu\text{m}$ , as shown in the SEM image in Fig. 5.11.



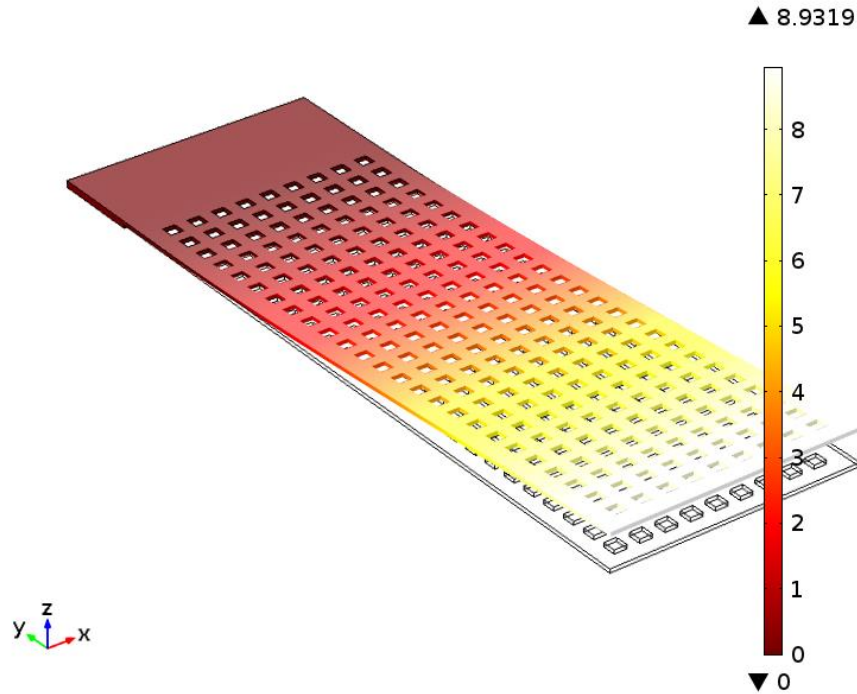


Fig. 5.12 FEM simulation results for the fabricated superconducting switch with warped plates using the determined residual stress value; the maximum beam deflection is 8.9  $\mu\text{m}$ .

To investigate the forces applied to the beam by the substrate due to temperature variation, the beam and the substrate are simulated in COMSOL. This is a crucial investigation that enables the prediction of beam deflection at cryogenic temperature [36]. The beam is considered flat, and the only load on both the beam and the substrate is the thermal load given by the temperature variation between 293K (room temperature) and 4K. The beam is  $100\ \mu\text{m} \times 40\ \mu\text{m}$ , with a thickness of  $0.6\ \mu\text{m}$ , and the substrate is  $2\ \text{mm} \times 2\ \text{mm}$ . The substrate thickness varies from  $500\ \mu\text{m}$  to  $50\ \mu\text{m}$  in the simulation to investigate its effect on beam deformation. The appropriate assigning of boundary conditions is very important, as they should take into account the effect of the forces applied to the beam by the substrate. The sole fixed boundary is at the bottom of the substrate. The surface area of the beam that is in contact with the relative surface of the substrate is identically meshed and the nodes are paired to enable transfer of the substrate movement due to thermal load to the beam. As shown in Fig 5.13, the substrate thickness causes the beam displacement to vary from an upward to a downward deflection.

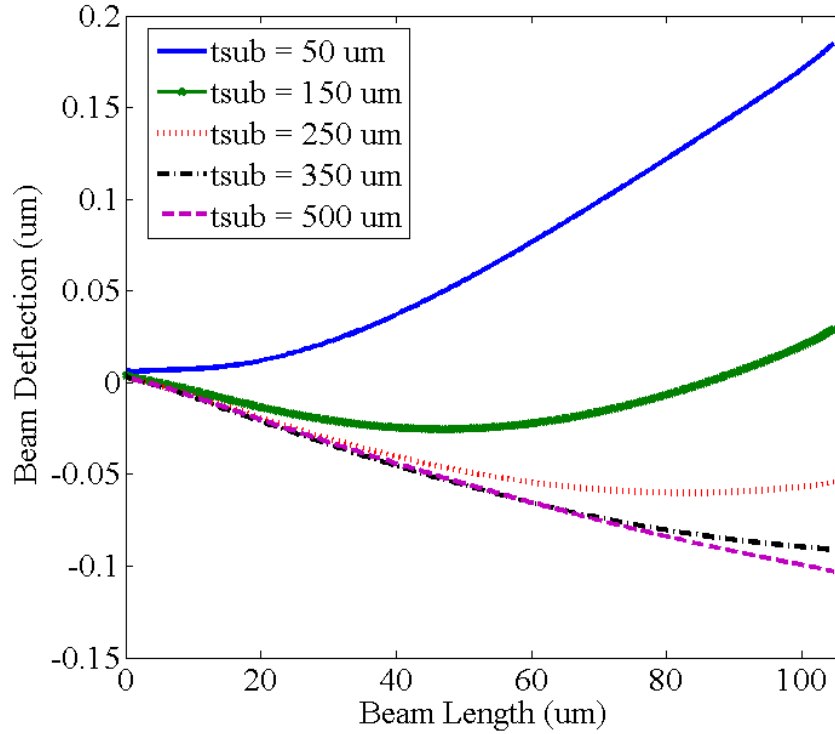


Fig. 5.13 Simulated results in COMSOL showing the effect of the substrate thickness on the beam deflection along the beam length when temperature changes from 293K to 4K.

Fig. 5.14 depicts the cross-section of the cantilever beam and the applied forces to the beam. There are two sources that apply force to the beam, one of which is the substrate contraction, which pulls the beam down as it contracts. This force and moment are shown by  $F_{\text{sub-to-beam}}$  and  $M_{\text{sub-to-beam}}$ , respectively. The other source of force is the result of the CTE difference between the beam and the substrate. The CTE of Si is considered  $3.2 \mu\text{/K}$  [15] and the CTE of Nb is considered  $7.2 \mu\text{/K}$  [27]. The force and moment induced in the beam due to the CTE difference are shown by  $F_{\text{CTE}}$  and  $M_{\text{CTE}}$ , which causes the beam to bend downward. The final direction of the beam displacement depends on the direction of the total force. Investigation shows that it is imperative to make the dimensions of the substrate, particularly its thickness, as close to reality as possible to ensure a better understanding of beam deformation at low temperature.

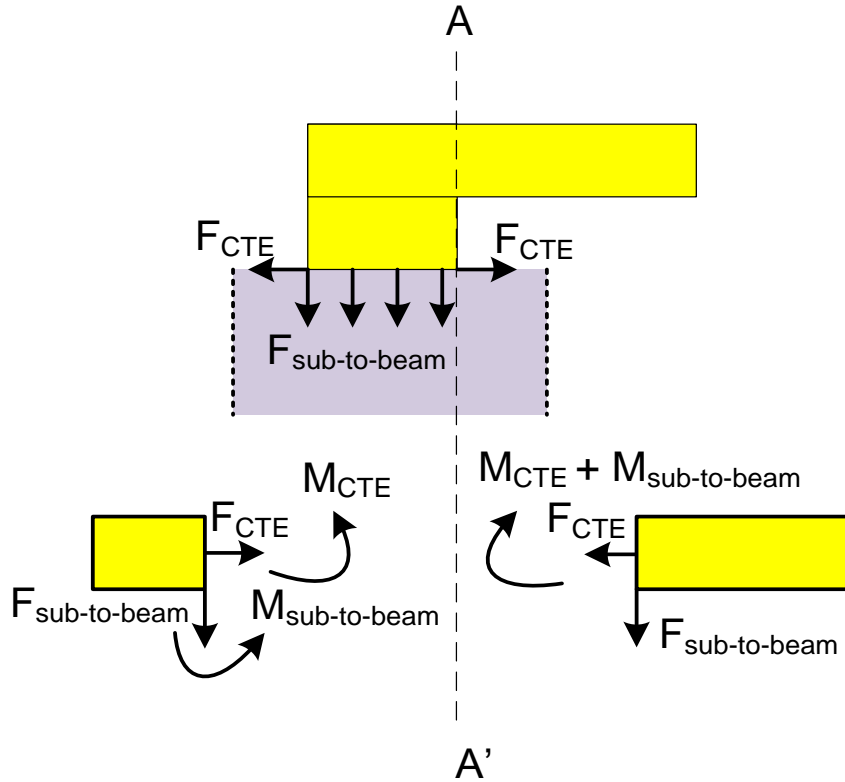


Fig. 5.14 Cross-section of the cantilever beam and the applied forces to the beam due to temperature variation.

Coupled-field electromechanical simulation is also performed with CoventorWare [37] to evaluate the actuation voltage of the switch. A dc voltage is applied between the actuation electrode and the cantilever beam. The simulated pull-in voltage is predicted to be 38 V, considering the 8.9  $\mu\text{m}$  initial warp-up of the beam.

### EM Analysis of Deformed Structure

EM simulations of the proposed switch are performed using Ansoft HFSS tools. Fig. 5.15 shows the simulated S-parameters of the switch from 10 MHz to 10 GHz for the up-state at 293K. The insertion loss is 3 dB at 10 GHz and the return loss is better than 15 dB up to 10 GHz. The 3 dB insertion loss represents niobium loss and Si substrate loss at room temperature. Niobium and silicon conductivities are considered to be 3.5 MS/m and 8 S/m, respectively, at 293K, which is within the range of the data provided by Hypres. Fig. 5.16 shows the simulated S-parameters of the switch at 4K. The switch demonstrates an insertion loss better than 0.2 dB at 4K, which is a significant improvement in the insertion loss compared to that obtained at 293K. The equivalent-circuit model parameters of the switch shown in Fig. 5.10 are extracted from the simulated S-parameters at cryogenic temperature.

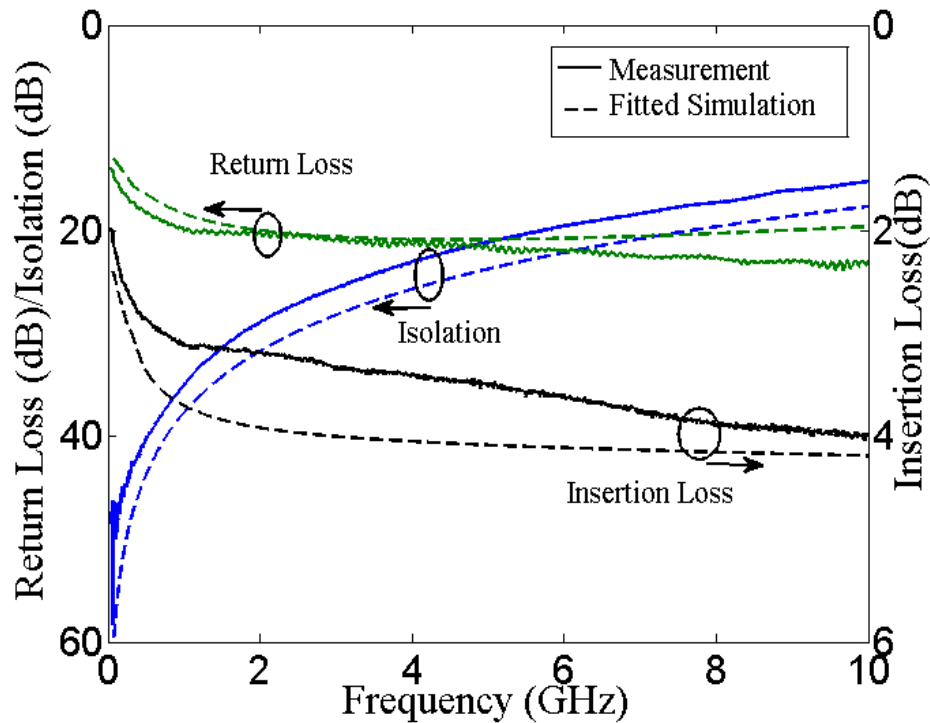


Fig. 5.15 The measured and simulated S-parameters of the superconducting RF MEMS switch at room temperature.

### Measurement Results

The RF performance of the switch is measured using two-port on-wafer measurements up to 10 GHz with a PNA-X N5241A Network Analyzer. The device is initially measured at 293K. The measured S-parameters of the switch for the up-state are presented in Fig. 5.15, along with the simulation results. The maximum insertion loss at 10 GHz is 4 dB and the return loss is better than 15 dB from 10 MHz up to 10 GHz. In order to measure the switch response in the superconducting state of niobium, the Lakeshore cryogenic probe station is used. To measure the device at cryogenic temperatures, the system is calibrated at 4K, using a calibration substrate. The RF probes mounted on the Lakeshore probe station are Pico probes. CS-5 calibration substrate is used for Short-Open-Load-Thru (SOLT) calibration. Several experimental and simulation results show that the room temperature standards for calibration are sufficiently accurate for cryogenic calibration as well.

The superconducting RF MEMS switch is measured in the cryogenic probe station, with the reference plane at the CPW pads. Fig. 5.16 shows the measured and simulated results of the proposed superconducting switch at 4K. The insertion loss is improved significantly from 4 dB to lower than 0.2 dB at 10 GHz. There are also improvements in the return loss and the switch's isolation. Table 5.1

compares the measured results of the proposed Nb-based RF MEMS switch with two commercial switches including Radant and Omron. The table shows that the superconducting switch has great insertion loss at 4K compare to the other two switches. The return loss of the Nb-based switch is also better than the other two switches. It should be mentioned that many of the commercially available MEMS switches could not survive the 4K temperature.

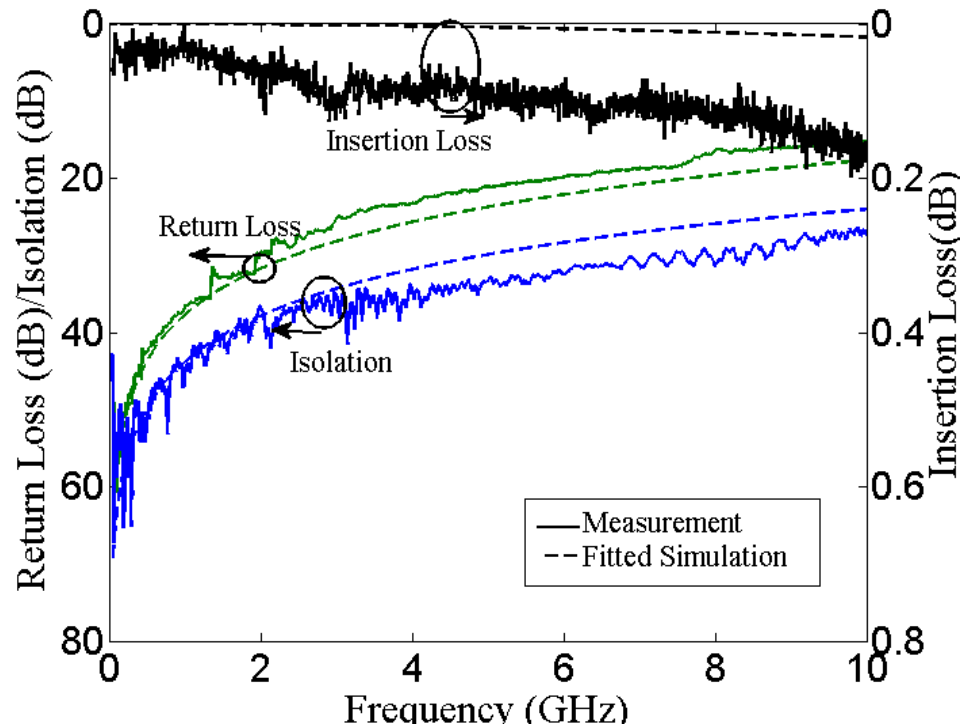


Fig. 5.16. The measured and simulated S-parameters of the superconducting RF MEMS switch performance at 4K.

Table 5.1. S-parameters and pull-in voltage comparison between two commercial RF MEMS switches and the Nb-based dc-contact RF MEMS switch.

| @ 5GHz            | Insertion Loss | Return Loss | Isolation | Pull-in Voltage |
|-------------------|----------------|-------------|-----------|-----------------|
| RMSW100HP<br>[52] | 0.3 dB         | 18.8 dB     | 17.7 dB   | 85 V            |
| 2SMES-01 [53]     | 0.8 dB         | 15 dB       | 33 dB     | 30 V            |
| Nb-Based          | 0.12 dB        | 23 dB       | 35 dB     | 46 V            |

The switch actuation voltage is also investigated. The required pull-in voltage is 39 V at 293K, which then increases to 46 V at 4K. The actuation voltage of the switch increases by 18% at cryogenic temperature compared to that of room temperature.

Young's modulus is obtained according to Equation (5.7).

$$E = \frac{\sigma}{\varepsilon} \quad (5.7)$$

where  $\sigma$  is tensile stress and  $\varepsilon$  is tensile strain. Both of these material properties are temperature-dependent, as their variation by temperature is obtained only by measurement. E is therefore temperature dependent. The Young's modulus of most metals increases as temperature decreases. According to [38], the Young's modulus of gold increases from 55 GPa at room temperature to 18.4 TPa at 14K.

To obtain similar variations for niobium, the mechanical simulation in CoventorWare is initially calibrated to the measured results obtained at both room and cryogenic temperatures. The beam is modeled considering an initial deflection of 8.9  $\mu\text{m}$  at its tip, while the Young's modulus of Nb is considered 105 GPa [27]. Such initial conditions give a pull-in voltage of 38 V in CoventorWare, which is very close to the room temperature measurement. To estimate the Young's modulus of Nb at 4K, the initial deflection of the beam is considered to be 8.8  $\mu\text{m}$  and the effect of the substrate on the beam at cryogenic temperature is also considered, as illustrated in Fig. 5.13. The only variable in the simulation is the Young's modulus of Nb. The value of Nb's Young's modulus is varied until the simulation results show a pull-in voltage of 46 V, which is when the Nb Young's modulus is considered to be 150 GPa.

Various switches are designed, fabricated, released and characterized both at room and cryogenic temperatures. Fig. 5.17 shows SEM images of some of the devices.

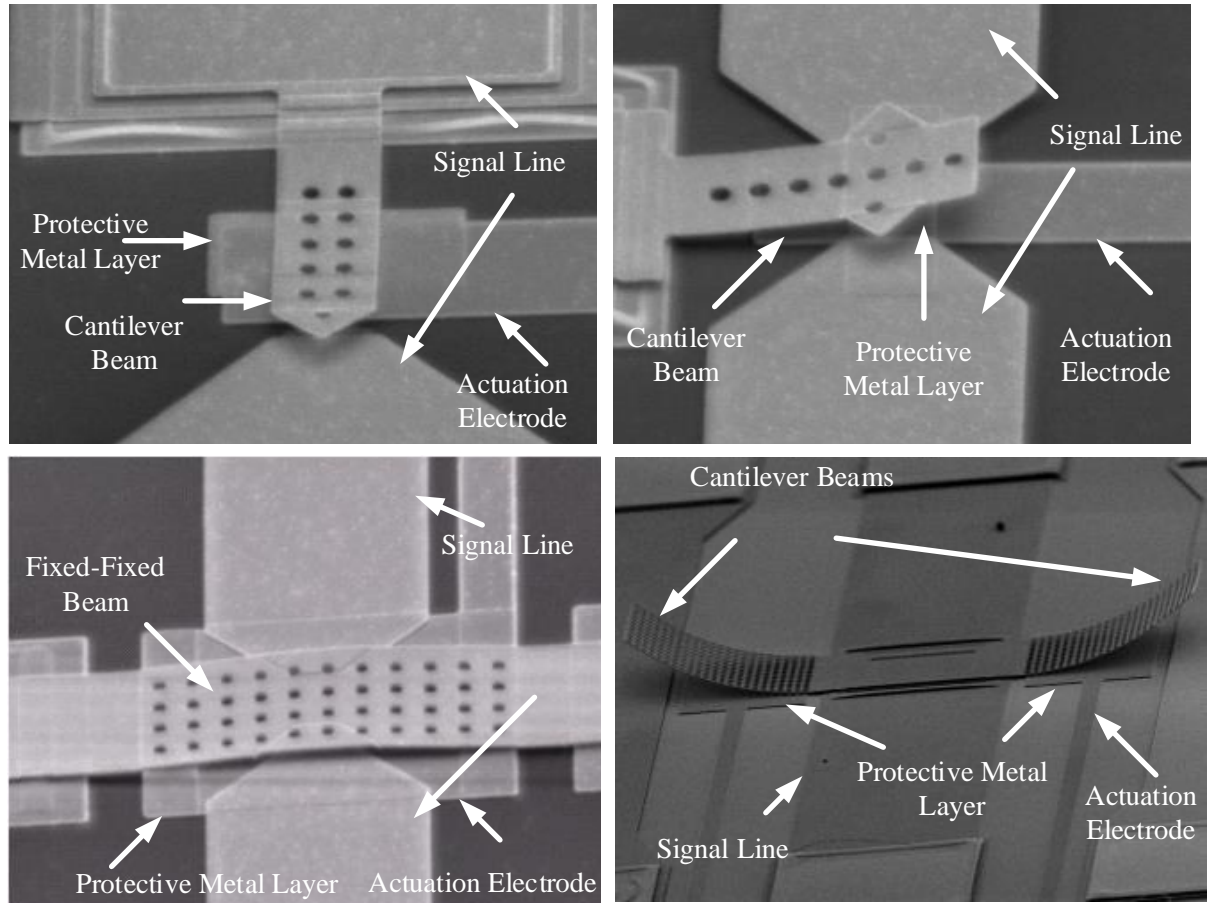


Fig. 5.17 SEM image of several designs of superconducting dc-contact RF MEMS switches fabricated using the Hypres foundry.

### 5.2.2 Capacitive-Contact RF MEMS Switches

Unlike dc-contact series switches, a capacitive-contact shunt switch is ‘on’ when there is no dc-voltage applied to the beam and the beam is in its up-state position. In this case, there is a small capacitance between the RF signal and the ground, which acts as an open circuit in high frequencies. When a dc-voltage is applied to the beam, it is actuated to its down-state position and the switch is ‘off’. There is a large capacitance between the RF signal and the ground, which acts as a short circuit at high frequencies.

#### Switch Design

Fig. 5.18 shows a cross-sectional view of a superconducting capacitive contact shunt RF MEMS switch. The suspended beam is on an M3 metal layer. The signal line is on M0, which is also the actuation pad. Part of the SiO<sub>2</sub> between M0 and M3 is protected from the wet etchant by M1. This is

required to protect any short circuit between M0 and M3 while actuating the suspended beam. In addition, the dielectric layer between M0 and M1 is the thinnest available dielectric layer, which allows for large down-state capacitance value and thus better isolation for the switch. When the switch is in the up-state position, the capacitance value between the ground plane and the signal line is very small, which acts as an open circuit at high frequency. After actuating the beam to its down-state position, the capacitance value between the ground plane and the signal line is much larger and acts as a short circuit. The dimensions of the plate and the TL are shown in Fig. 5.18. The size of each release hole is 2  $\mu\text{m}$ , with spacing of 2  $\mu\text{m}$ . The air gap should be 0.7  $\mu\text{m}$ ; however, it increases to 2  $\mu\text{m}$  due to the residual stress in the thin film. Fig. 5.19 shows the SEM image and the circuit model of the released device.



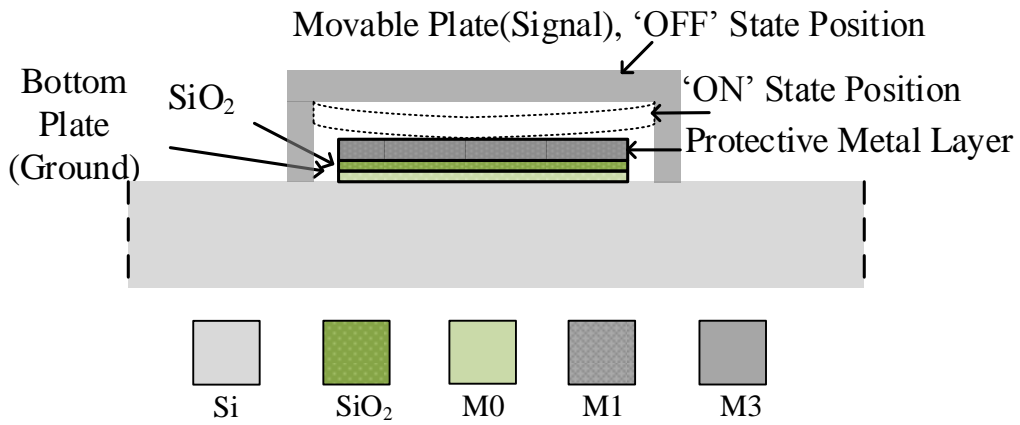
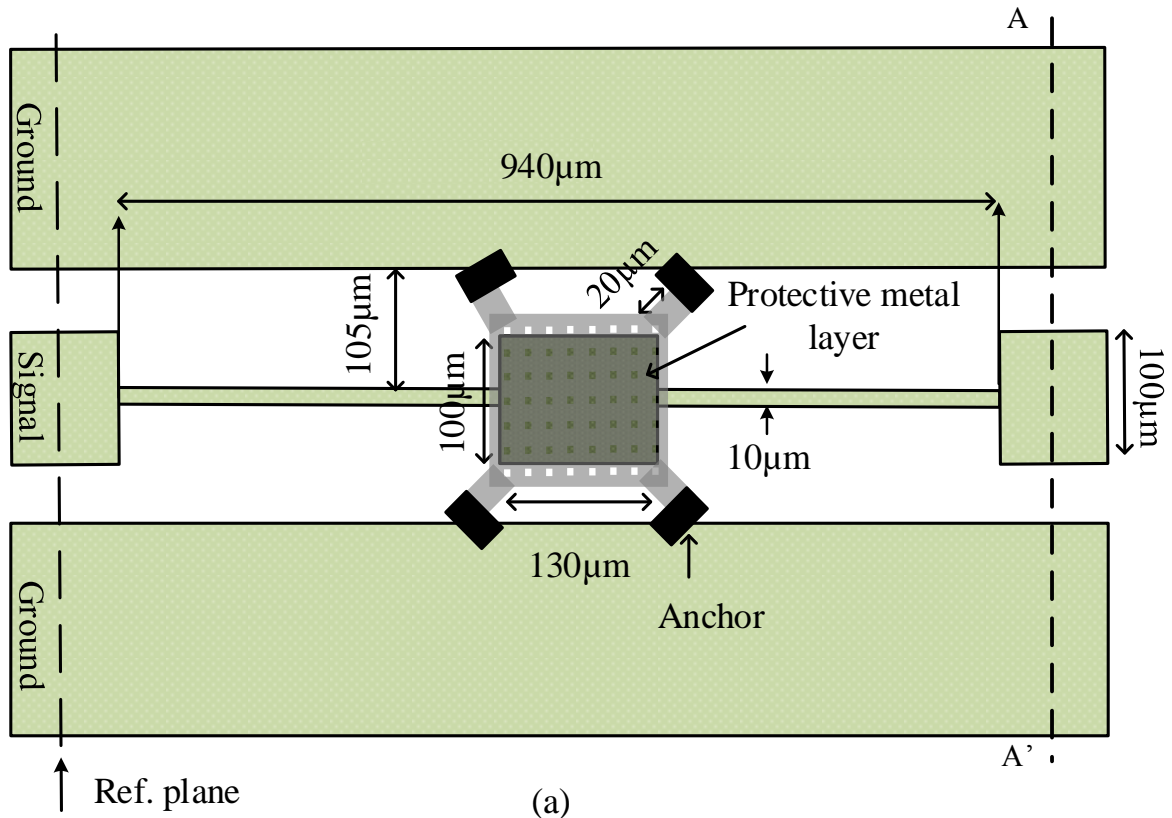


Fig. 5.18 The top view (a) and the cross-section (b) of the superconducting RF MEMS capacitive-contact switch.

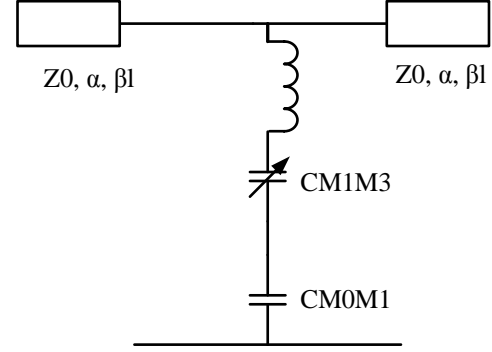
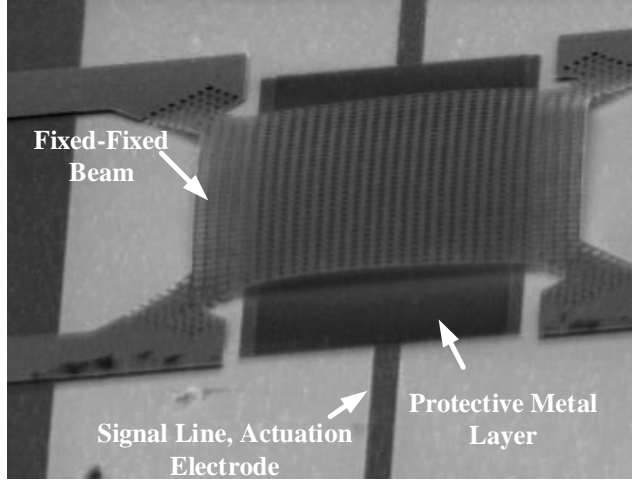


Fig. 5.19 The SEM image of the niobium superconducting RF MEMS capacitive-contact switch after release and its circuit model.

Assuming lossless metal layers, the up-state capacitance and down-state capacitance values are calculated as follows:

$$C_u^{-1} = C_{M0M1}^{-1} + C_{M1M3}^{-1} \quad (5.8)$$

$$C_{M1M3} = \frac{\epsilon_0 w W}{t_{d0}} \quad (5.9)$$

$$C_{M0M1} = \frac{\epsilon_0 \epsilon_r w W}{t_{d1}} \quad (5.10)$$

$$C_d = C_{M0M1} \quad (5.11)$$

where  $\epsilon_0$  is the vacuum permittivity,  $\epsilon_r$  is the permittivity of the  $\text{SiO}_2$  dielectric layer,  $W$  is the width of the signal line,  $w$  is the width of the beam,  $t_{d0}$  is the thickness of the oxide layer between M0 and M1, and  $t_{d1}$  is the thickness of the air gap. The capacitance ratio is an important factor in designing a capacitive switch. It is defined as:

$$CR = \frac{C_d}{C_u} \quad (5.12)$$

The higher the value of the capacitance ratio, the lower is the insertion loss and the higher the isolation of the device. Hence, in designing a capacitive switch, the focus is on increasing the down-state capacitance while decreasing the up-state capacitance value.

Fig. 5.20 shows the RF response of the switch at cryogenic temperature. The switch has good RF performance around 8 GHz, where both the isolation and return loss are 20 dB and the insertion loss is very close to zero. The switch actuation voltage is 26 V at cryogenic temperature.

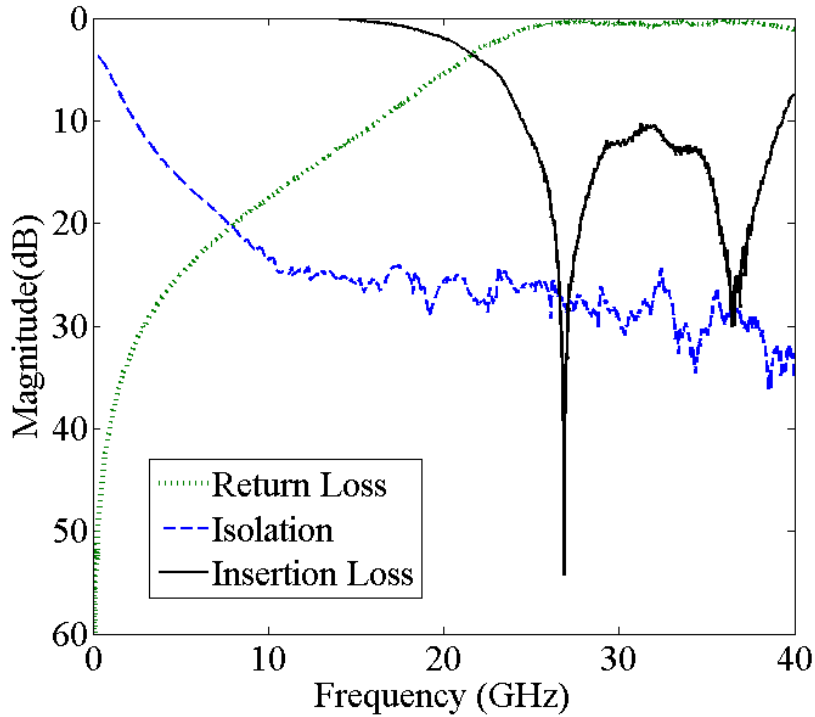
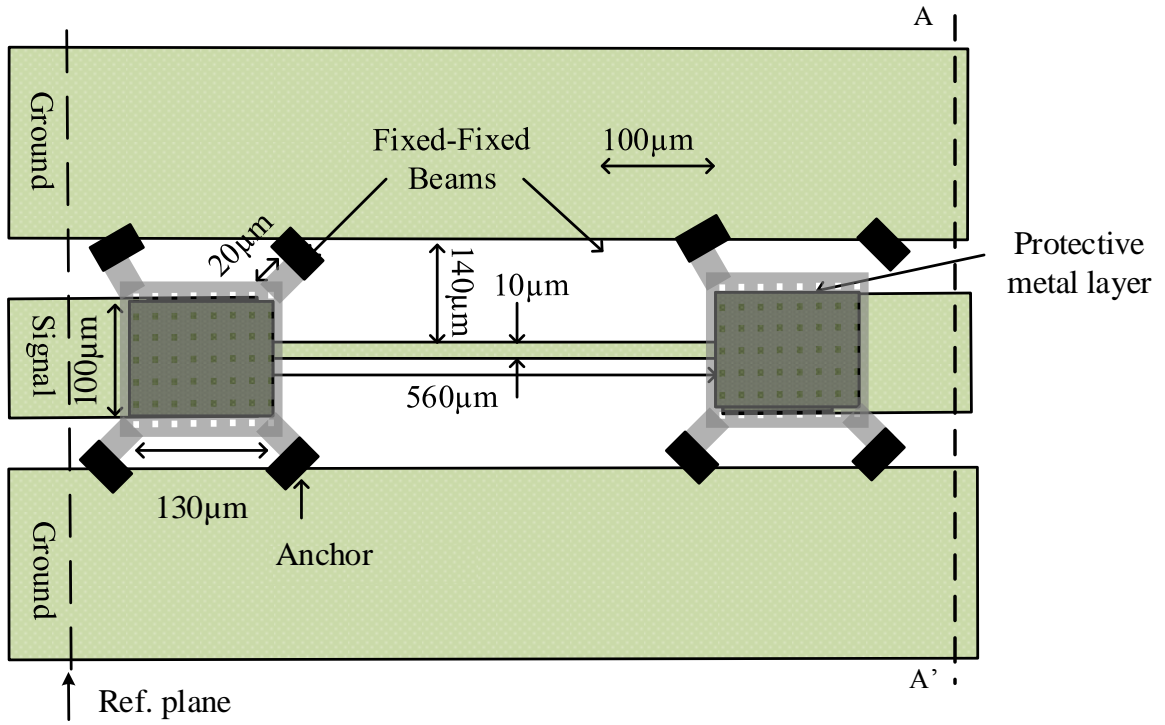


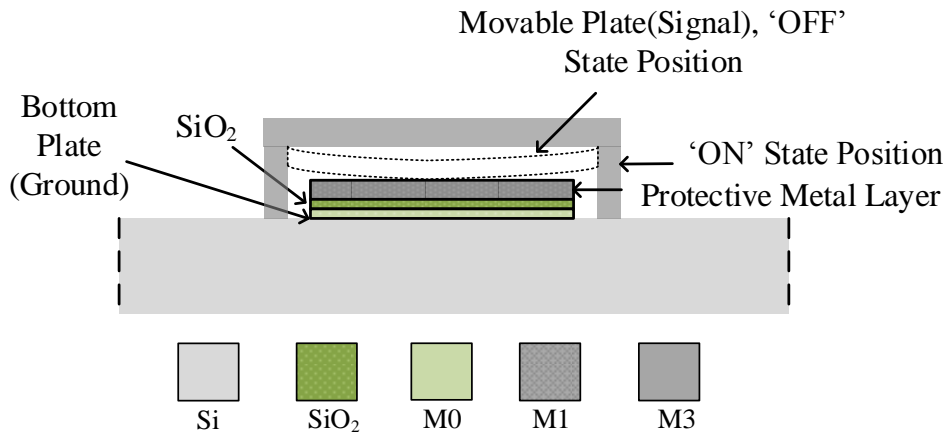
Fig. 5.20 The measured and simulated S-parameters of the superconducting RF MEMS capacitive-contact switch performance at cryogenic temperature.

Since all of the dielectric layers' thicknesses are fixed in the Hypres fabrication process, a high impedance line can be used between two capacitive shunt switches. This design is referred to as  $\pi$ -matching network in [6]

Fig. 5.21 illustrates the top and cross-section views of a  $\pi$ -match type capacitive-contact shunt switch. The dimensions of the high impedance line are designed to tune the RF performance of the switch from 5 GHz to 15 GHz. Fig. 5.22 shows the SEM image of the released device.



(a)



(b) Cross section view (A-A')

Fig. 5.21 The top view (a) and the cross-section (b) of the superconducting  $\pi$ -match type capacitive-contact switch.

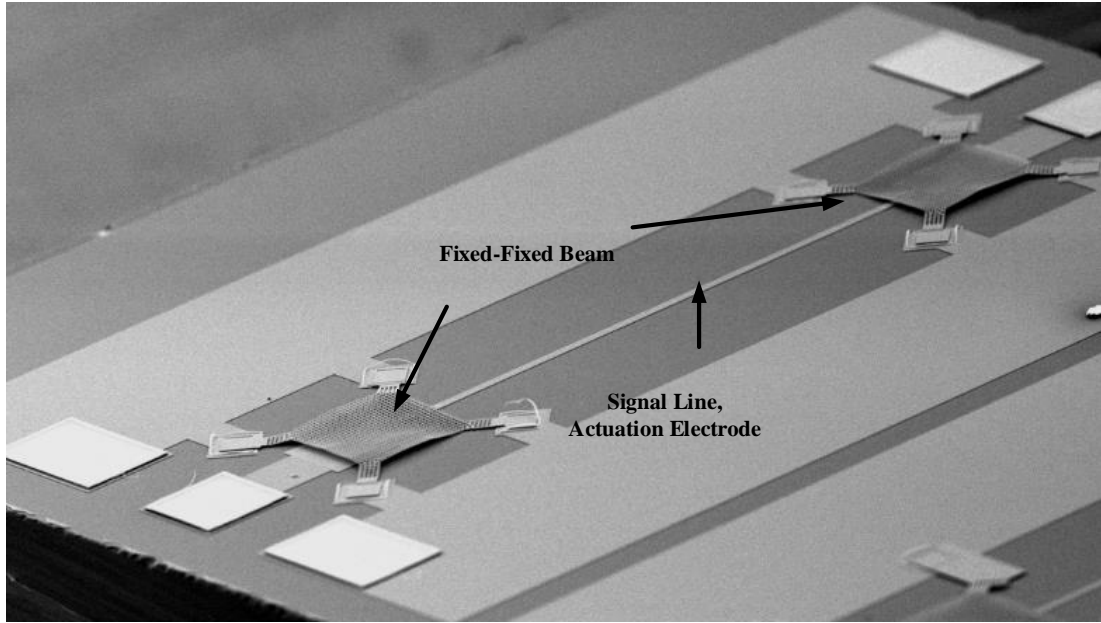


Fig. 5.22 The SEM image of the superconducting  $\pi$ -match type capacitive-contact switch.

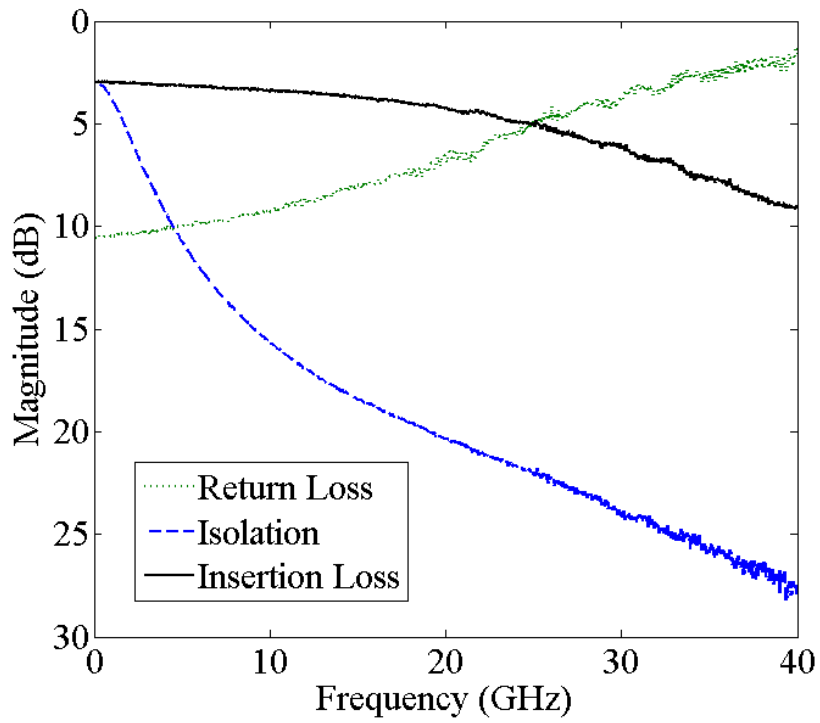


Fig. 5.23 Measured results of the RF performance of the superconducting  $\pi$ -match type capacitive-contact RF MEMS switch at room temperature.

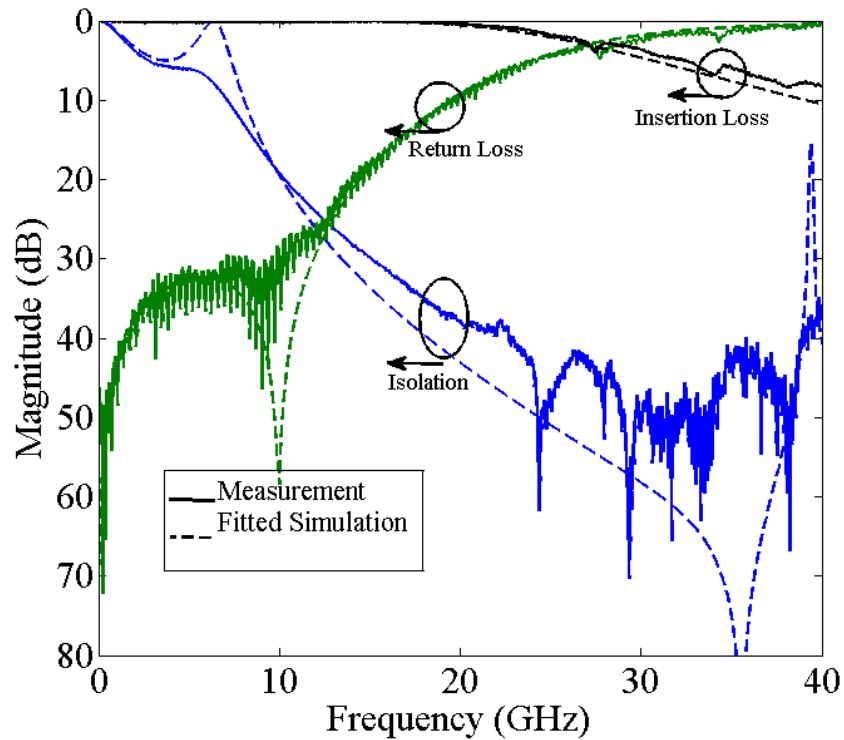


Fig. 5.24 Simulated and measured results of the RF performance of the superconducting  $\pi$ -match type capacitive-contact RF MEMS switch at cryogenic temperature.

Fig. 5.23 and Fig. 5.24 show the simulated and measured results of the RF performance of the switch at room and cryogenic temperatures, respectively. A comparison of the results shows that the insertion loss of the switch increases significantly at cryogenic temperature. The return loss and isolation have also improved. The switch RF performance at cryogenic temperature is very good from 10 GHz to 15 GHz. The return loss and isolation are both below 20 dB and the insertion loss is very close to zero in this frequency range. The actuation voltage is 42 V at cryogenic and 14 V at room temperature. Various designs are fabricated, released and characterized both at room and cryogenic temperatures. Fig. 5.25 shows SEM images of some of the devices.

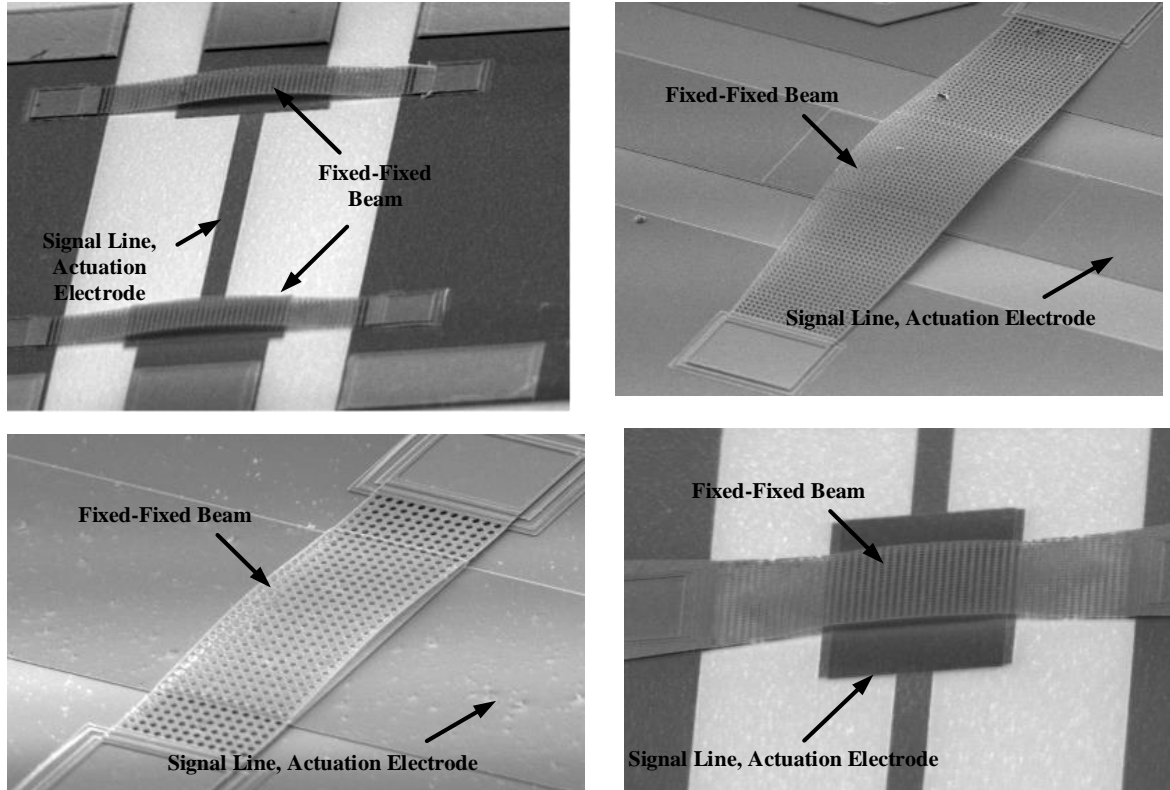


Fig. 5.25 SEM image of several designs of superconducting capacitive-contact RF MEMS switch fabricated using the Hypres foundry

### 5.3 Nb-Based RF MEMS Variable Capacitors

MEMS varactors have several advantages over their Si and GaAs counterparts. MEMS varactors are linear and offer a relatively high Q. The linearity property of MEMS varactors is, in particular, a huge advantage.

The RF MEMS varactor provides capacitance variations by changing the gap between the two plates of a parallel plate capacitor. Fig. 5.26 depicts the top and cross-section views of the proposed varactor, which is constructed of two capacitors that are connected in series, as shown in Fig. 5.26(b). The first capacitor, which is between M0 and M1, is a fixed capacitor. The second capacitor, which is between M1 and M3, is a variable capacitor. In this varactor, the fixed capacitor is designed as the protective metal layer. It also prevents the top plate, M3, from coming in contact with the bottom plate, M0, thereby avoiding a short circuit between the electrodes of the varactor. The first oxide layer is purposely trapped between M0 and M1 and is used as the dielectric layer of the fixed capacitor. Thus, when the sacrificial layer is being etched away, the dielectric layer remains intact. The second

and the third oxide layers are used as the MEMS sacrificial layers. Removing these sacrificial layers creates an air gap between the capacitor plates and allows the top plate to move toward the bottom plate. Each plate of the varactor has an area of  $100\ \mu\text{m} \times 100\ \mu\text{m}$ . The air gap is  $0.7\ \mu\text{m}$  and the thickness of the silicon dioxide dielectric layer between M0 and M1 is  $0.15\ \mu\text{m}$ . The structure is built on a low-resistivity Si substrate.

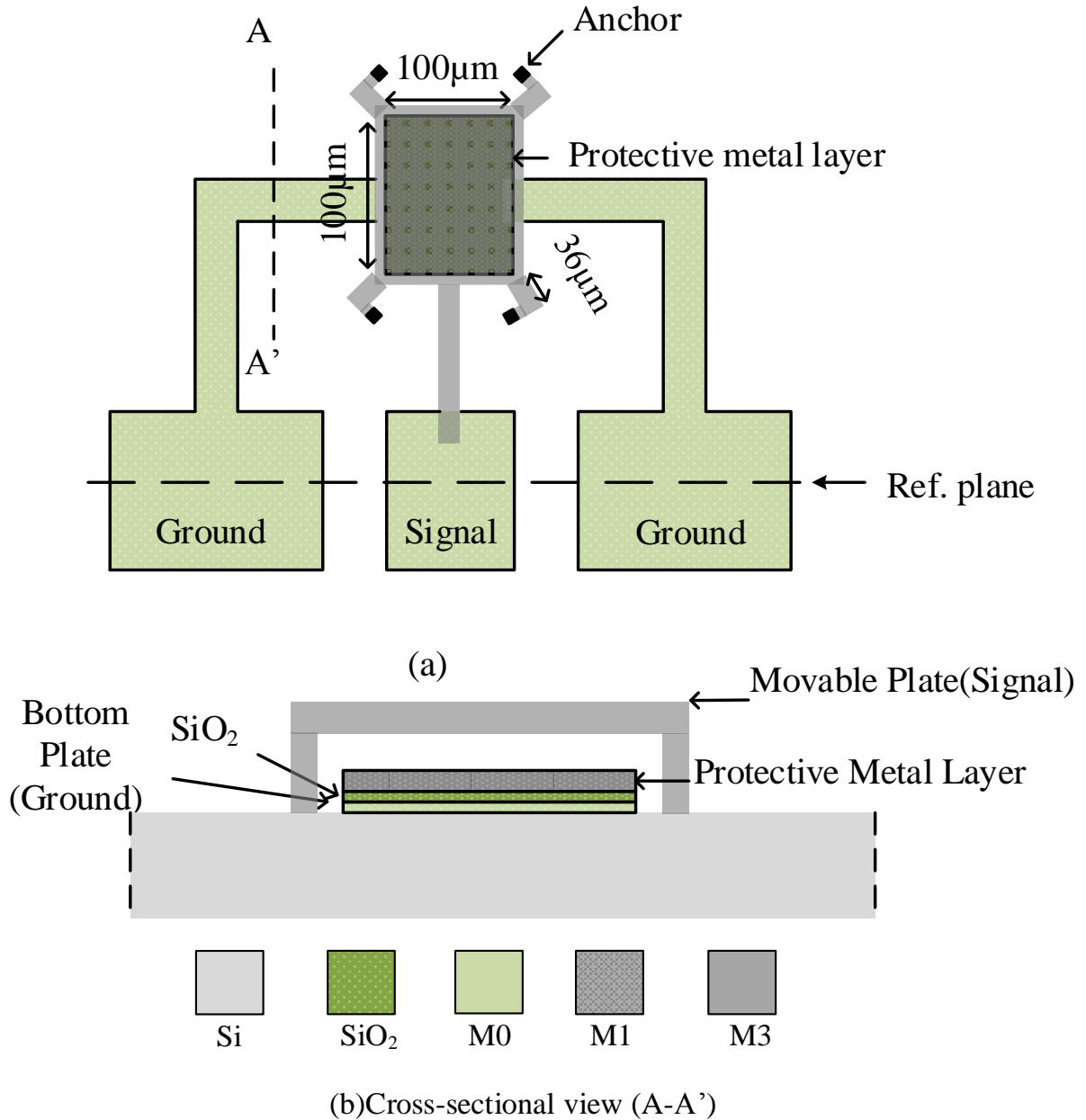


Fig.. 5.26. The top view (a) and the cross-section (b) of the superconducting RF MEMS varactor [39].



The coplanar waveguide (CPW) pads are introduced to facilitate the on-chip measurement of the device using an RF probe station. The top plate is connected to the signal pad and the bottom plate is connected to the ground pads. To actuate the varactor, a dc voltage is applied to the signal line through a bias-tee and the ground pads are connected to dc ground. Fig. 5.27 shows the SEM image of the released varactor.

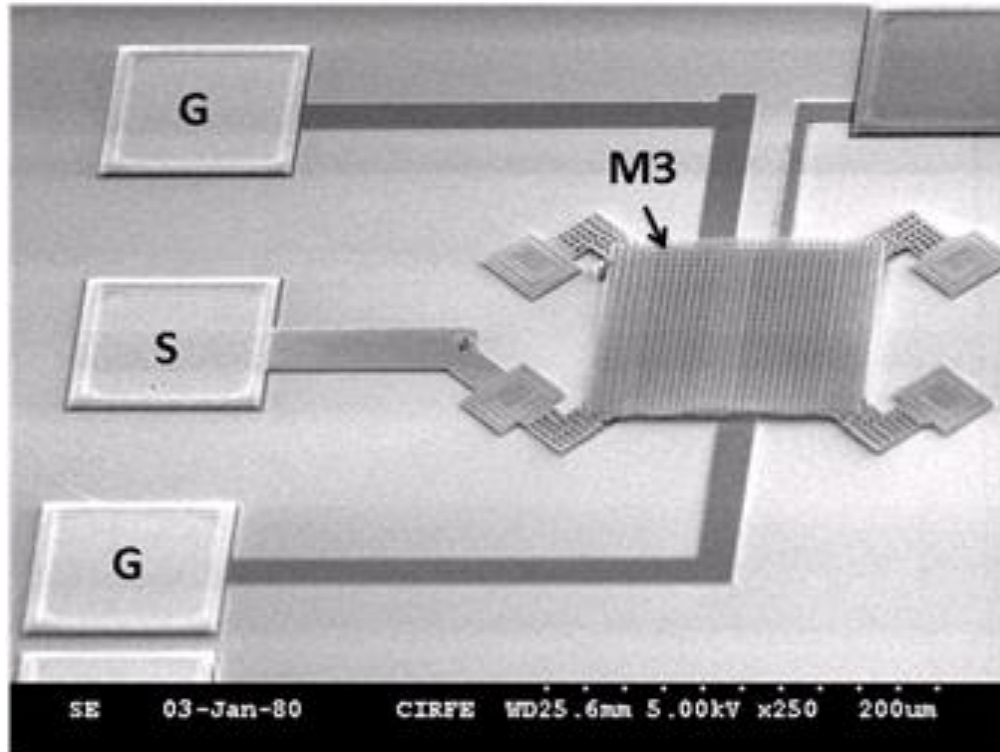


Fig. 5.27. The SEM image of the niobium superconducting RF MEMS varactor after release.

Residual stress present in the M3 metal layer causes buckle-up of the top plate of the proposed RF MEMS varactor after removing the sacrificial layer. This property, however, is an advantage to improve the down-state to up-state capacitance ratio of the varactor. Fig. 5.28 shows the final simulation results in COMSOL for the proposed superconducting MEMS varactor deflection. The maximum simulated buckle-up of the plate is  $5\ \mu\text{m}$ , which is very close to the measured value, as shown in the SEM image in Fig. 5.27. The simulated up-state capacitance value of the varactor at dc is 40 fF and the down-state capacitance value is 1.2 pF, considering an initial displacement of  $5\ \mu\text{m}$  for the movable plate of the device.

The RF performance of the varactor is measured using one port on wafer measurements with a PNA-X N5241A Network Analyzer. The device is initially measured at 293K. The varactor is actuated by applying the dc-voltage between the signal and the ground pads of the CPW port. Fig. 5.29 shows the

extracted capacitance variation at room temperature versus the applied voltage. The results show a more than 60% capacitance variation from 0.529 pF to 0.848 pF at 2 GHz before the pull-in of the movable plate at 30 V. The measured down-state capacitance value of the varactor is approximately 1.20 pF.

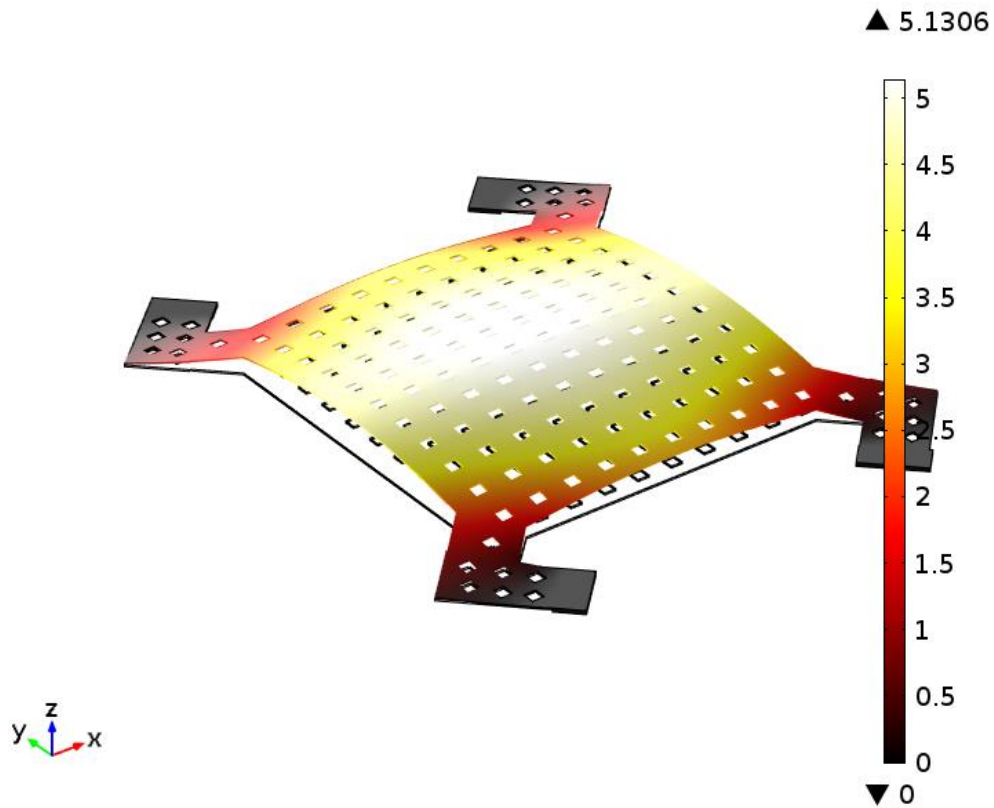


Fig. 5.28. FEM simulation results for the fabricated superconducting varactor with buckled plate. Using the determined residual stress value, the maximum plate deflection is 5  $\mu\text{m}$ .

The device is measured at the Lakeshore cryogenic probe station. Fig. 5.30 illustrates the capacitance variation of the varactor in a cryogenic environment, showing that the varactor's capacitance value changes from 0.04 pF to 0.46 pF and the actuation voltage varies from 0 V to 50 V. It is worth mentioning that the added capacitance due to silicon loss (discussed in section 4.2) at room temperature causes the discrepancy between capacitance variations at room temperature and those at cryogenic temperature. The main reason for the actuation voltage variation is an increase in the Young's modulus of niobium at cryogenic temperature [12].

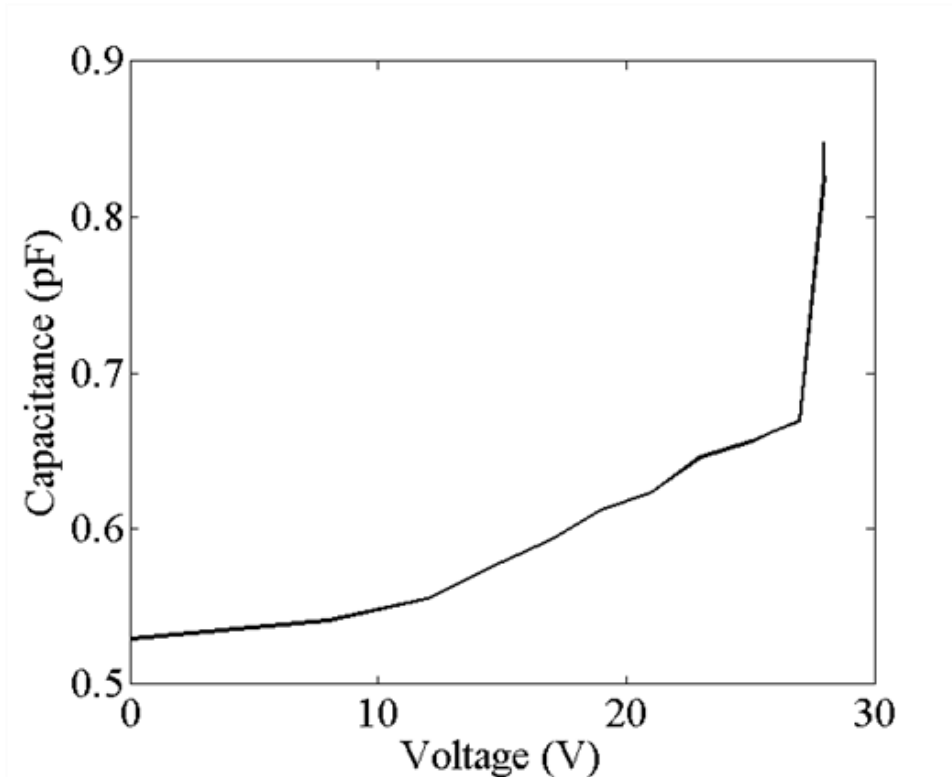


Fig. 5.29. Measured results of the extracted capacitance value variation versus the actuation voltage at room temperature at 2 GHz for the Nb-based varactor.

In order to compare the loss performance of niobium-based RF MEMS varactors with semiconductor varactors, a MA46H120-series GaAs varactor, having a relatively high Q value [40], is selected for the comparison. The measurement results show that the capacitance value of the GaAs varactor varies from 1 pF to 0.2 pF by applying a bias voltage up to 12 V. The Q of semiconductor and superconductor varactors is compared at room and cryogenic temperatures on a Smith chart, as shown in Fig. 5.31. The Nb-based varactor offers a very high Q value when Nb superconducts, whereas the quality factor of the semiconductor GaAs varactor only improves slightly at 4K. Various varactors are designed, fabricated, released and characterized both at room and cryogenic temperatures. Fig. 5.32 shows SEM images of some of the devices.

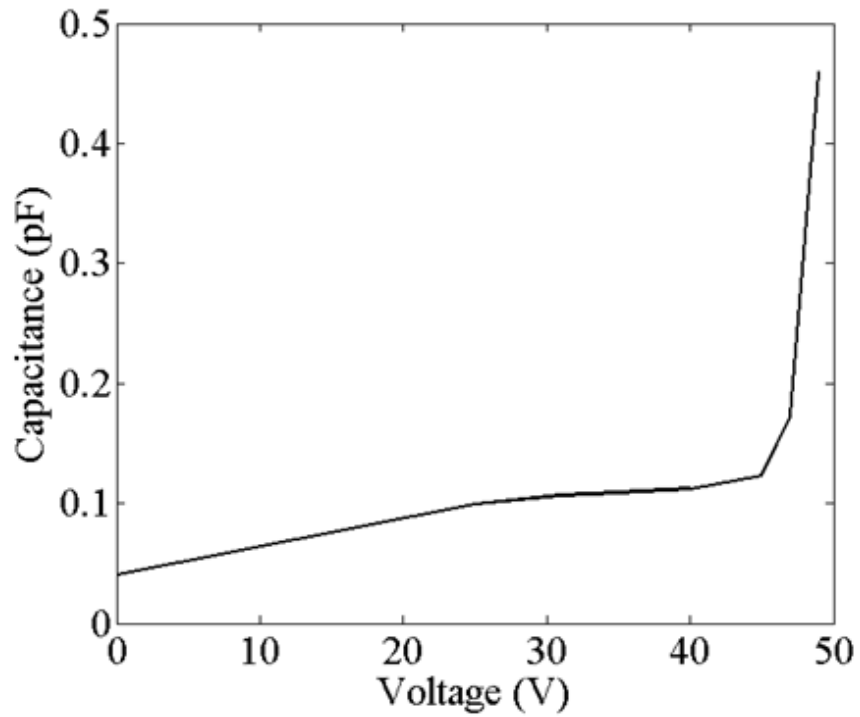


Fig. 5.30. Measured results of the extracted capacitance value variation versus the actuation voltage at cryogenic temperature, at 2 GHz for the Nb-based varactor.

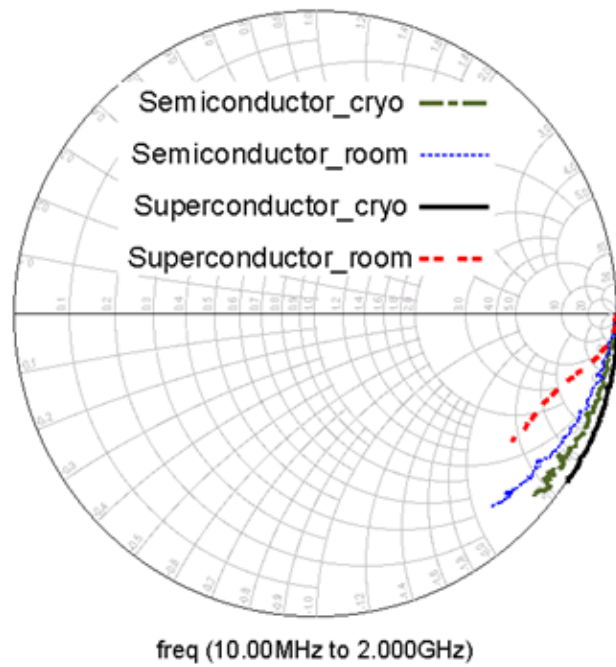


Fig. 5.31. Quality factor comparison of superconducting and semiconductor varactors at room and cryogenic temperatures.

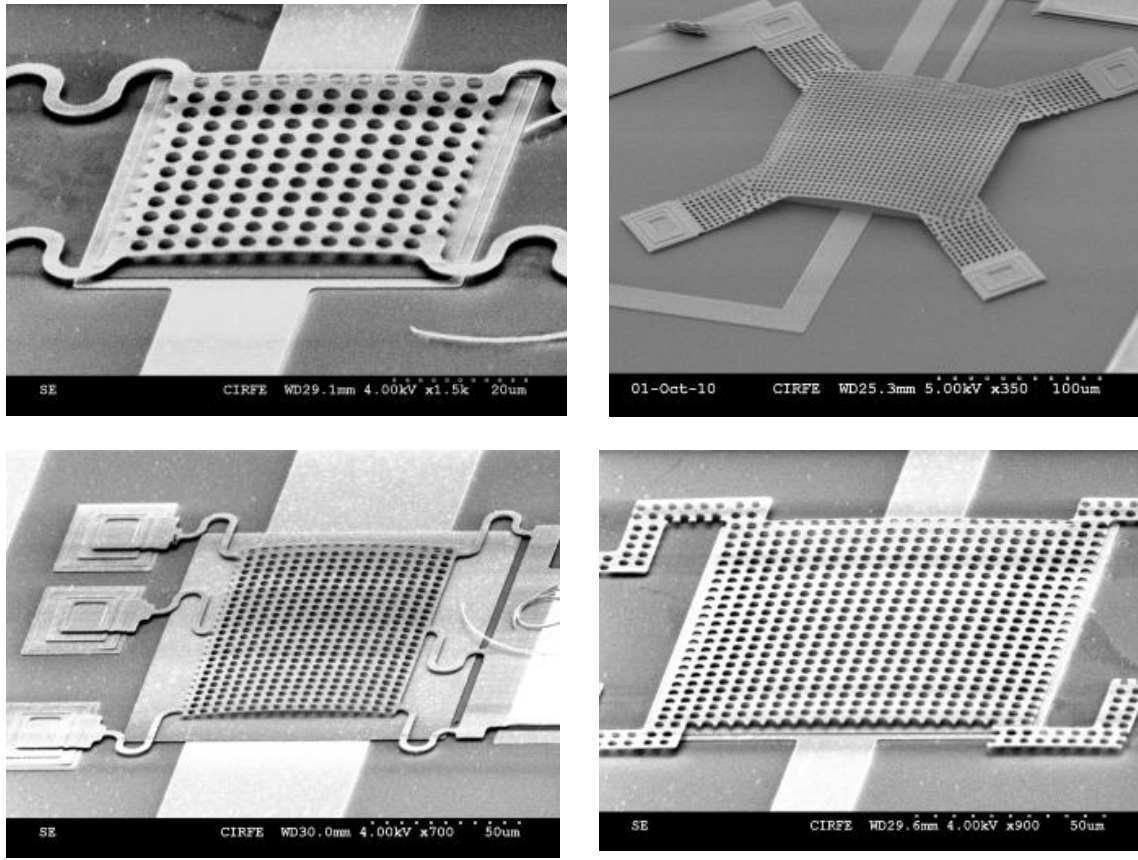


Fig. 5.32. SEM image of several designs of Nb-based varactors fabricated using the Hypres foundry.

## 5.4 Nb-Based RF MEMS Devices

In this part of the thesis, the previously elaborated dc-contact and capacitive-contact RF MEMS switches are employed to design more complex MEMS-based superconducting tunable RF devices, including Single-Pole-Double-Throw (SPDT) switches, capacitor banks, tunable resonators, and tunable filters.

### 5.4.1 Single-Port-Double-Throw RF MEMS Switch

A superconducting SPDT switch is designed employing two superconducting dc-contact RF MEMS switches. An SEM image of the device after the release process is illustrated in Fig. 5.33. The SPDT switch is measured at the Lakeshore cryogenic probe station at 4K. Fig. 5.34 depicts the measured S-parameters of the device in the two states, showing that the insertion loss is very close to zero for both states, and that the return loss is better than 18 dB at 2 GHz. The S-parameters from the input port to the output ports are not similar because the length of the TL from port 1 to port 3 is 20  $\mu\text{m}$  longer than from port 1 to port 2. This is just an initial prototype of a superconducting RF MEMS single-pole

multiple-throw switch, which then can be expanded to design switch matrices. The RF response can be enhanced significantly by optimizing the dimensions of the transmission line in each port [6].

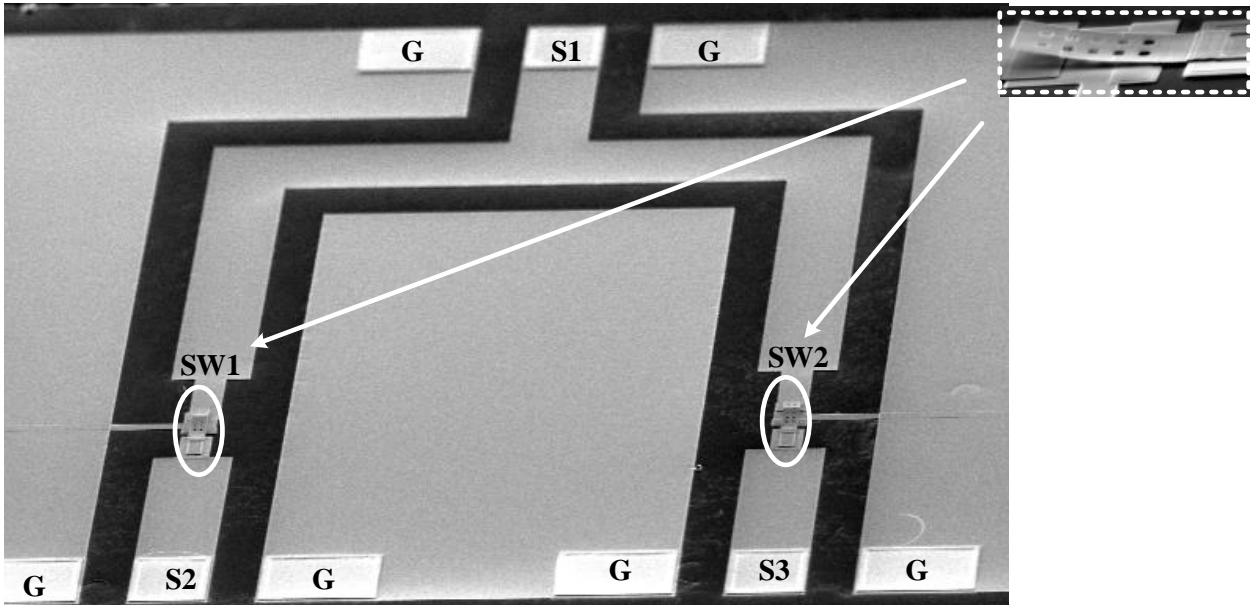


Fig. 5. 1. The SEM image of the niobium superconducting SPDT RF MEMS switch after release [41].

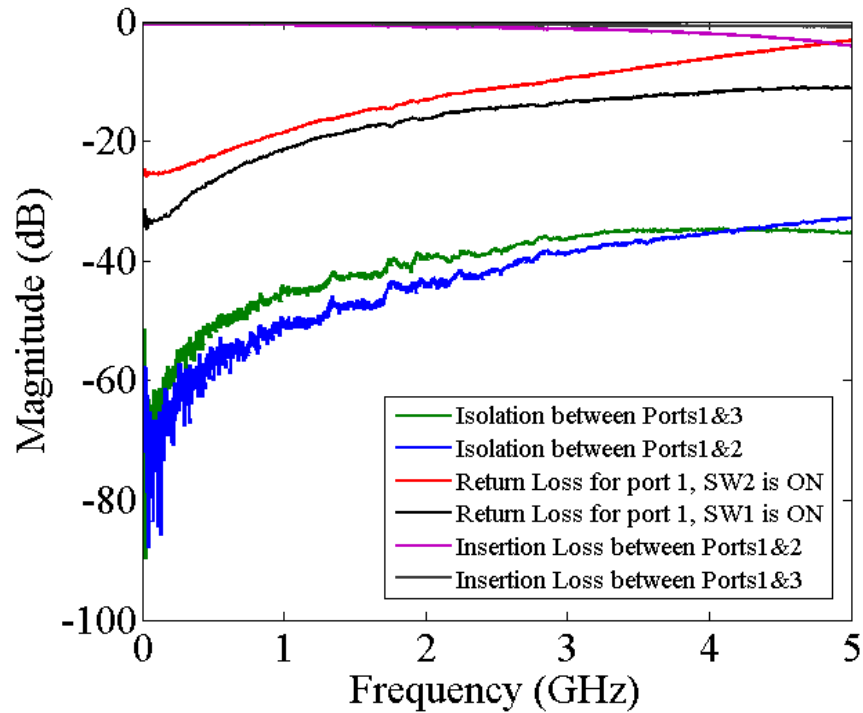


Fig. 5.33. The measured results of the superconducting SPDT RF MEMS switch S-parameter performance at cryogenic temperature.

#### 5.4.1 Capacitor Bank

Capacitor banks are major components for reconfigurable RF filters. Two novel capacitor banks are designed and fabricated using the Nb-based capacitive-contact RF MEMS switches and dc-contact switches proposed in sections 5.2.1 and 5.2.2.

##### Capacitor Bank Implementing DC-Contact RF MEMS Switches

In this design, there are four dc-contact RF MEMS switches that connect four fixed capacitors to the ground [41]. The value of each capacitor is about 0.45 pF at 2 GHz. Fig. 5.35 shows an SEM image of the device, along with a circuit model. The device is measured at the Lakeshore cryogenic probe-station at 4K. Fig. 5.36 shows the extracted capacitance values from the measured S-parameters. Only three states are presented here. The capacitance values are 0.2 pF, 0.61 pF, and 1 pF at 2 GHz, so that when all switches are ‘off’, SW1 is ‘on’ and SW2 is ‘on’, respectively.

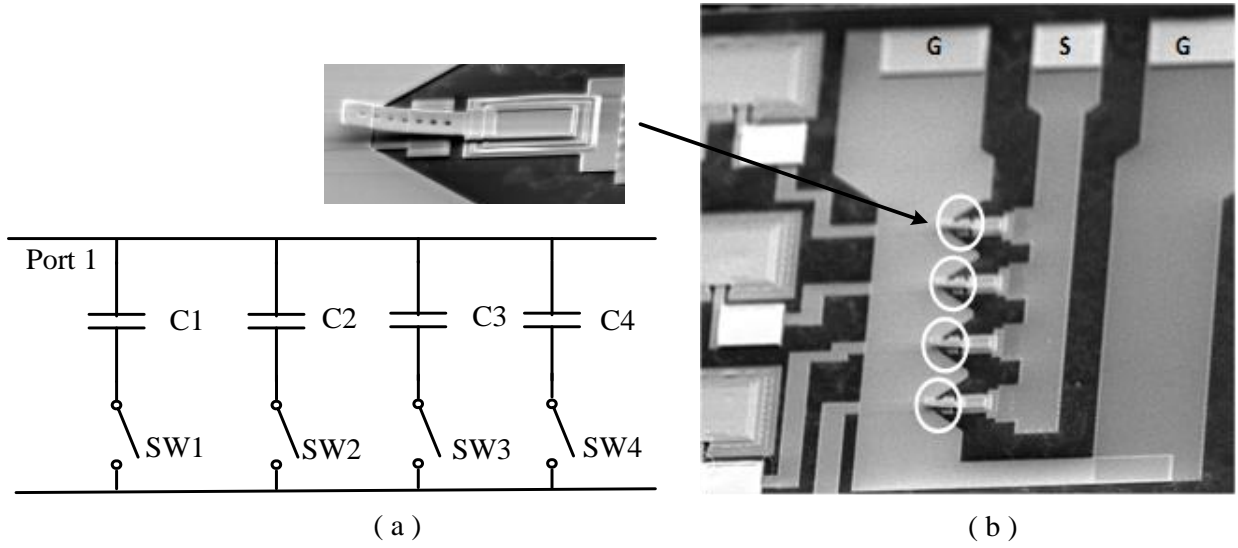


Fig. 5.34. (a) The circuit model and (b) the SEM image of the niobium superconducting capacitor bank implementing four DC contact RF MEMS switches

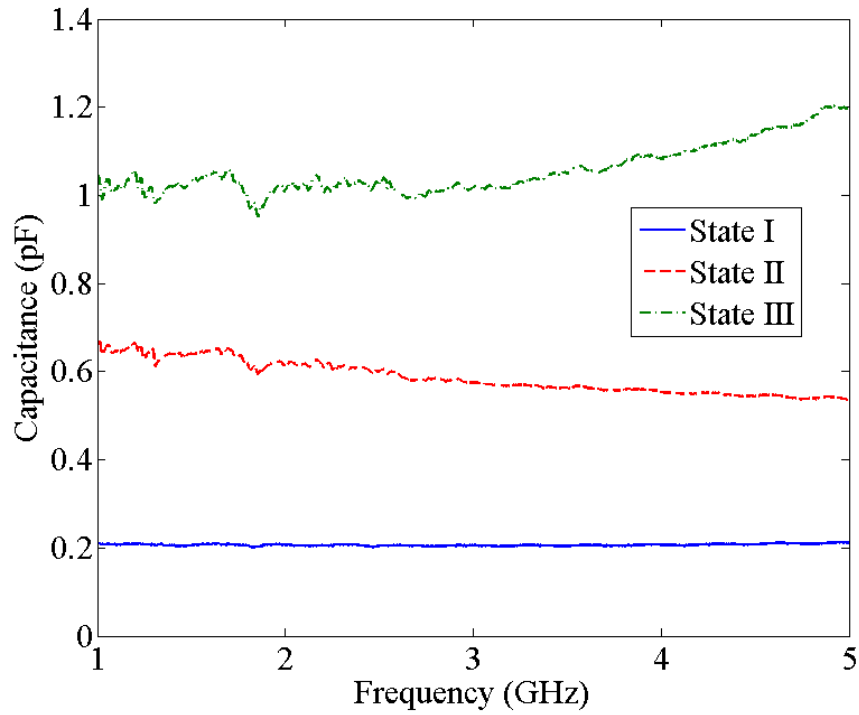


Fig. 5.35. The extracted capacitance value from the measured S-parameters of the superconducting RF MEMS capacitor bank implementing dc-contact RF MEMS switches at cryogenic temperature.



### Capacitor Bank Implementing Capacitive-Contact RF MEMS Switches

A capacitor bank is designed using capacitive-contact shunt RF MEMS switches [41]. Fig. 5.37 shows an SEM image and a circuit model of the device. It consists of three capacitive contact switches in shunt with the CPW transmission line. Three fixed capacitors are connected in series with the switches. At 2 GHz, the capacitance values for C1, C2 and C3 are 0.2 pF, 0.3pF and 0.7 pF, respectively. The up-state capacitance value of each capacitive switch is 0.1 pF and the down-state capacitance value is larger than 1 pF.

The device is measured at room temperature. Fig. 5.38 shows the extracted capacitance values from the measured S-parameters at room temperature. Four states are shown, including 0.4 pF, 0.45 pF, 0.55 pF and 0.94 pF at 2 GHz, with one capacitive switch being down each time. It should be mentioned that only one switch at a time could be actuated, since only two dc probes are available in the chamber – one for dc voltage, and the other for dc ground.

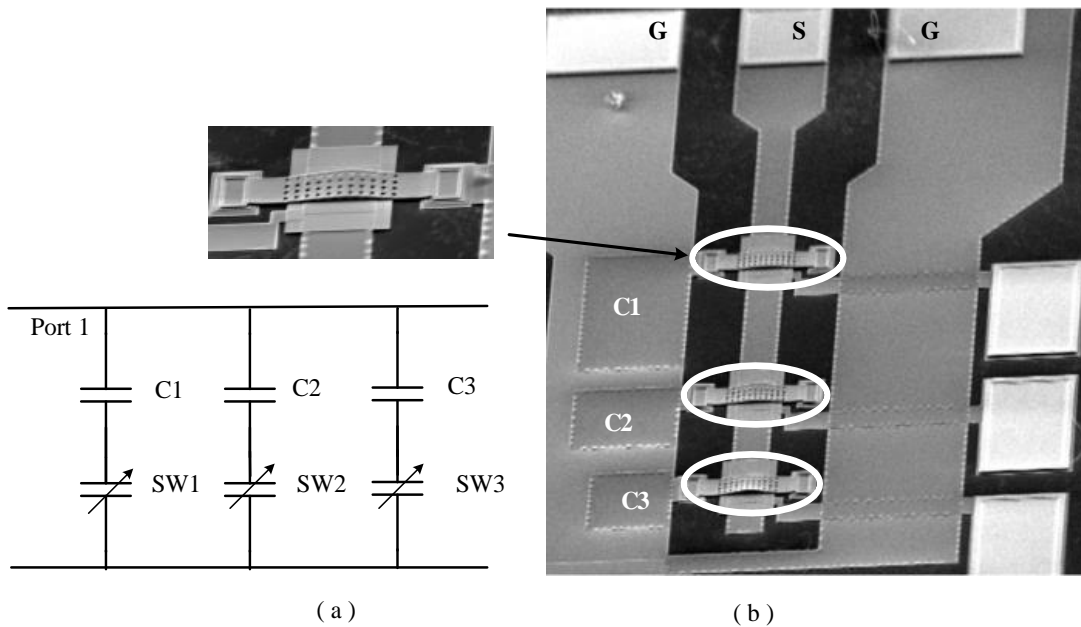


Fig. 5.36. (a) The circuit model and (b) the SEM image of the niobium superconducting capacitor bank implementing three capacitive contact RF MEMS switches.

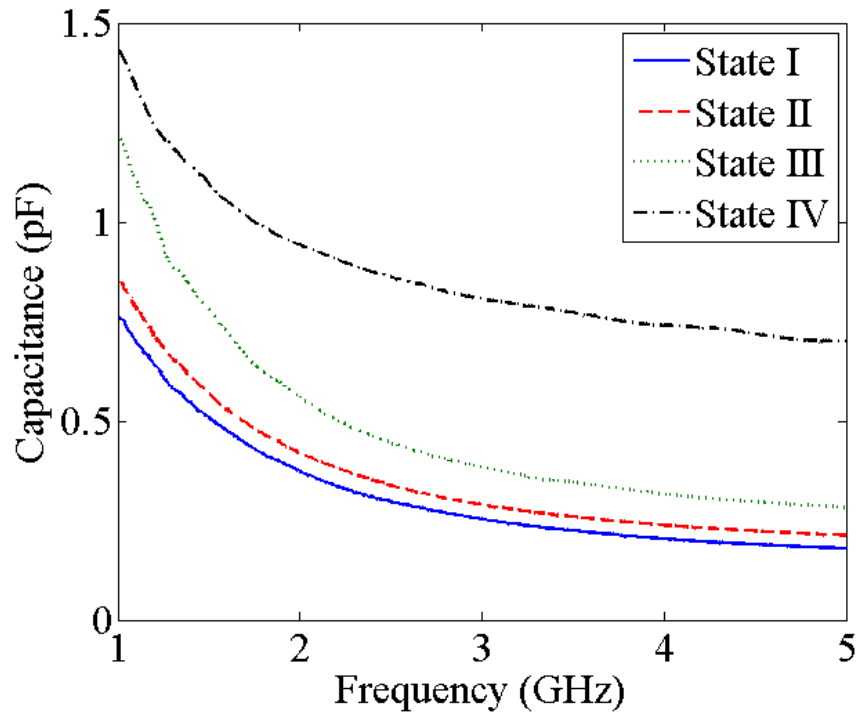


Fig. 5.37. The extracted capacitance value from the measured S-parameters of the superconducting RF MEMS capacitor bank implementing capacitive contact RF MEMS switches at room temperature.

#### 5.4.2 Tunable Resonator Using Switched Capacitor Bank

One of the main advantages of superconducting filters and resonators is miniaturization. Fig. 5.39 illustrates a picture of a 7-pole bandpass filter designed based on SME technology for the centre frequency of 400 MHz [19]. Fig. 5.40 is the measured RF response of the filter at 4K. The dimension of each resonator is 0.5mm, which is 1600 times smaller than the wavelength ( $\lambda$ ) while in the range of  $\lambda/2$  to  $\lambda/4$  for normal metals. Numerous studies have used RF MEMS switches and switched capacitor banks as tunable elements [42]-[45]. However, monolithically integrating a superconducting switched capacitor bank as the tuning element of a superconducting resonator is novel.

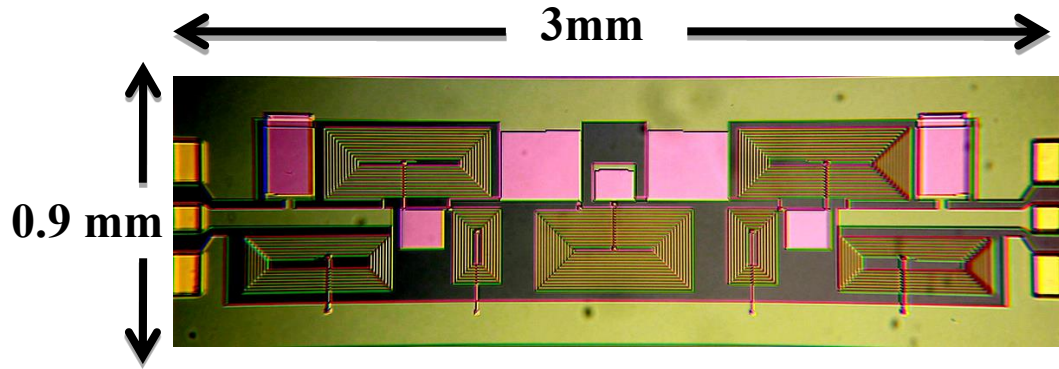


Fig. 5.38. Picture of the miniaturized superconducting 7-pole BPF [19].

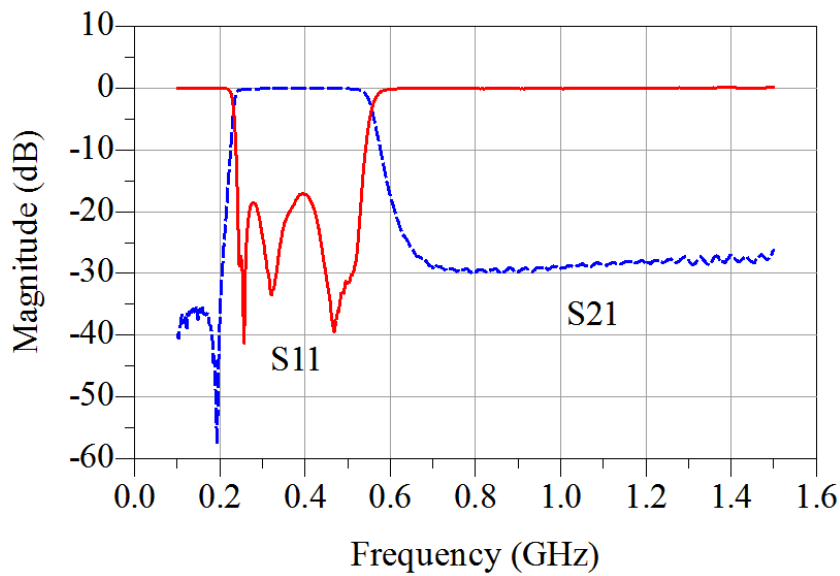


Fig. 5.39. Measured results of the RF response of the miniaturized superconducting 7-pole BPF at 4K [19].

The novel superconducting RF MEMS switch is implemented in a capacitor bank to realize different capacitance values, and the capacitor bank is monolithically integrated to a shunt bandstop resonator. Fig. 5.41 shows the circuit model of the tunable resonator. The resonator consists of a lumped element spiral inductor with a value of 50 nH, in series with a switched capacitor bank and at capacitance values in the range of fF. Fig. 5.42 illustrates a picture of the monolithically integrated bandstop resonator with the capacitor bank. The dimension of the device is 2.7 mm  $\times$  1.3 mm, which is extremely miniaturized for a high quality factor tunable resonator.

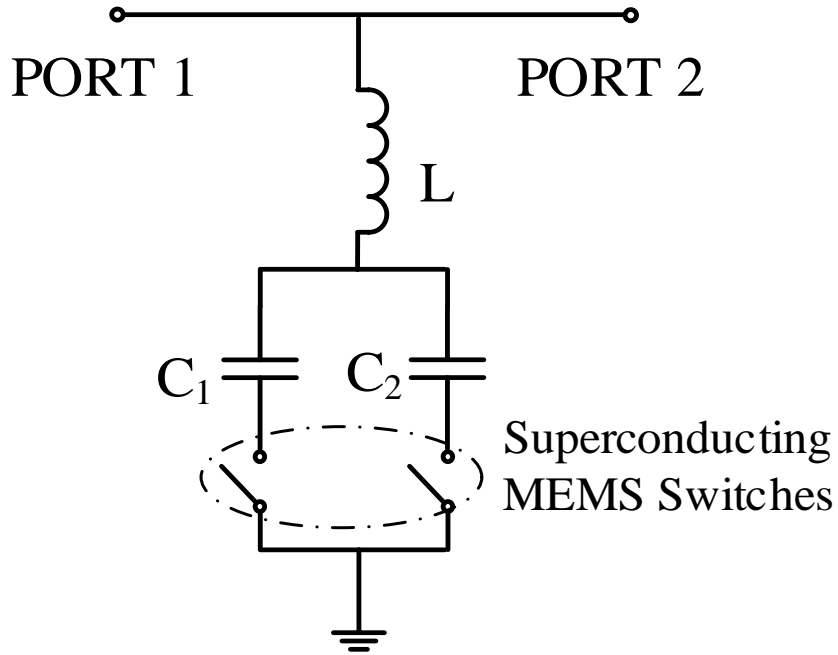


Fig. 5.40. The circuit model of the superconducting tunable bandstop resonator with switched capacitors.

The tunable resonator is measured at the Lakeshore cryogenic probe station using the same setup as the RF MEMS switch. The dc-bias voltage is applied through a 15 k $\Omega$  resistive bias line to the dc pad of each switch individually, and the ground is applied to the ground of the CPW transmission line. Fig. 5.41 shows the measured results of the three states of the tunable resonator at 4K. The resonance frequency is initially at 1.107 GHz when all of the switches are off (State I); it then shifts to 1.057 GHz and 1.025 GHz, respectively, when the first and second switches are on.

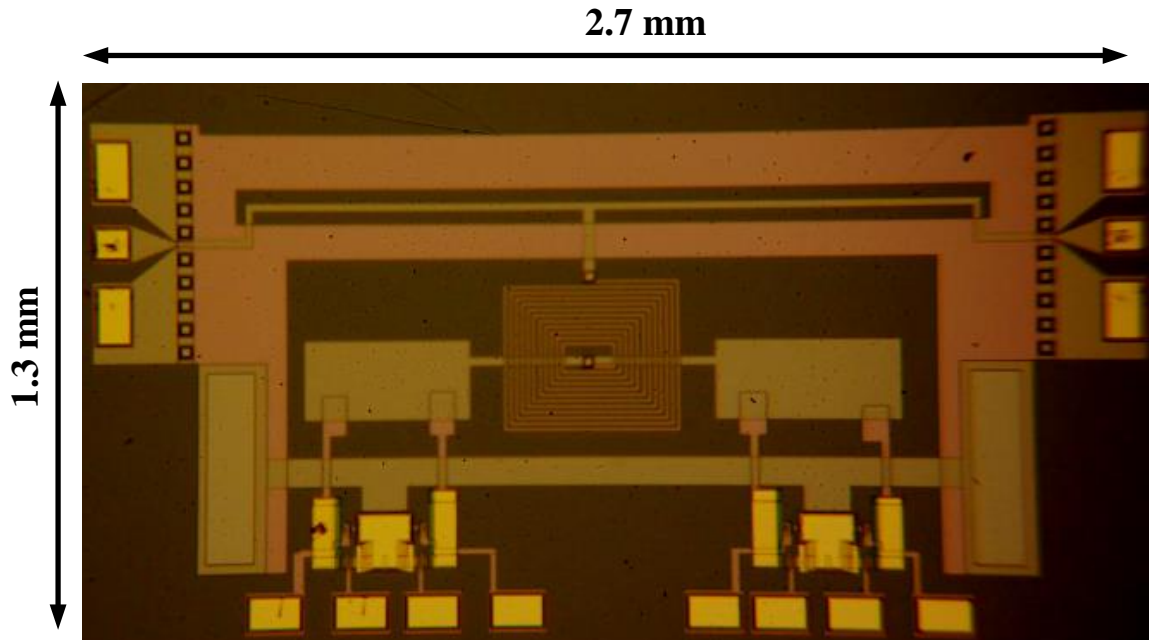


Fig. 5.41. Picture of the fabricated superconducting tunable resonator with monolithically integrated capacitor bank and superconducting MEMS switches.

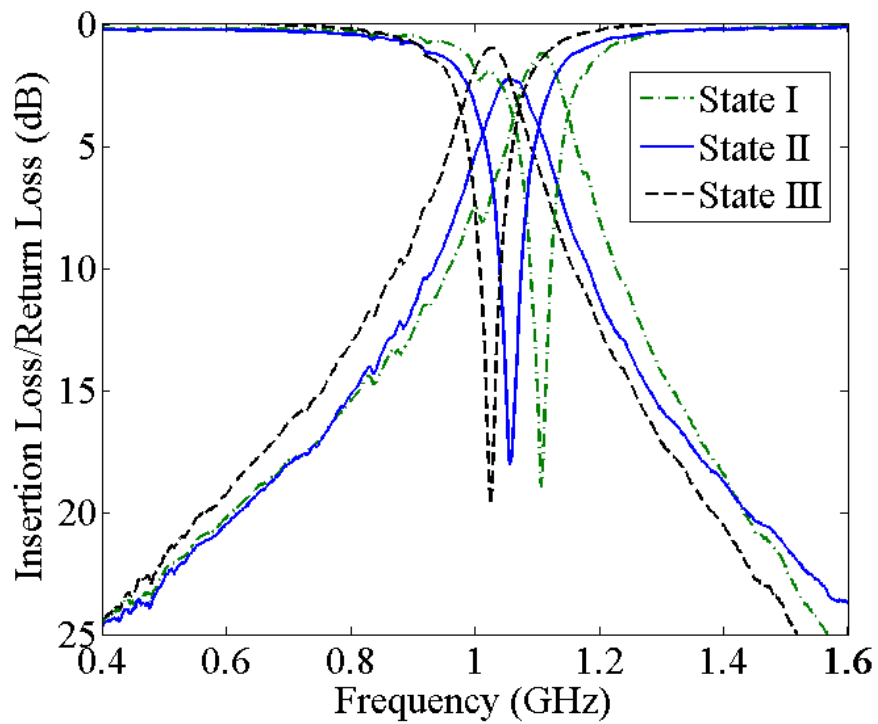


Fig. 5.42. Measured results of the three states of the superconducting tunable bandstop resonator when switches are off (State I), first switch is on (State II) and second switch is on (State III) at 4K.

### 5.4.3 Tunable Bandstop Resonator Using Varactor

The novel RF MEMS superconducting varactor is employed to realize a tunable lumped element bandstop resonator, with the varactor monolithically integrated with the resonator. Fig. 5.44 illustrates the SEM image and the circuit model of the integrated LTS MEMS tunable bandstop resonator. The shunt resonator consists of a spiral inductor with a value of 50 nH in series with an RF MEMS varactor and a fixed parallel plate capacitor. The CPW-to-microstrip transmission line transition is designed [19] at the input and output of the resonator to facilitate the measurement of the device. The size of the device is 1.38 mm  $\times$  0.9 mm, which is extremely miniaturized for a high quality factor tunable resonator.

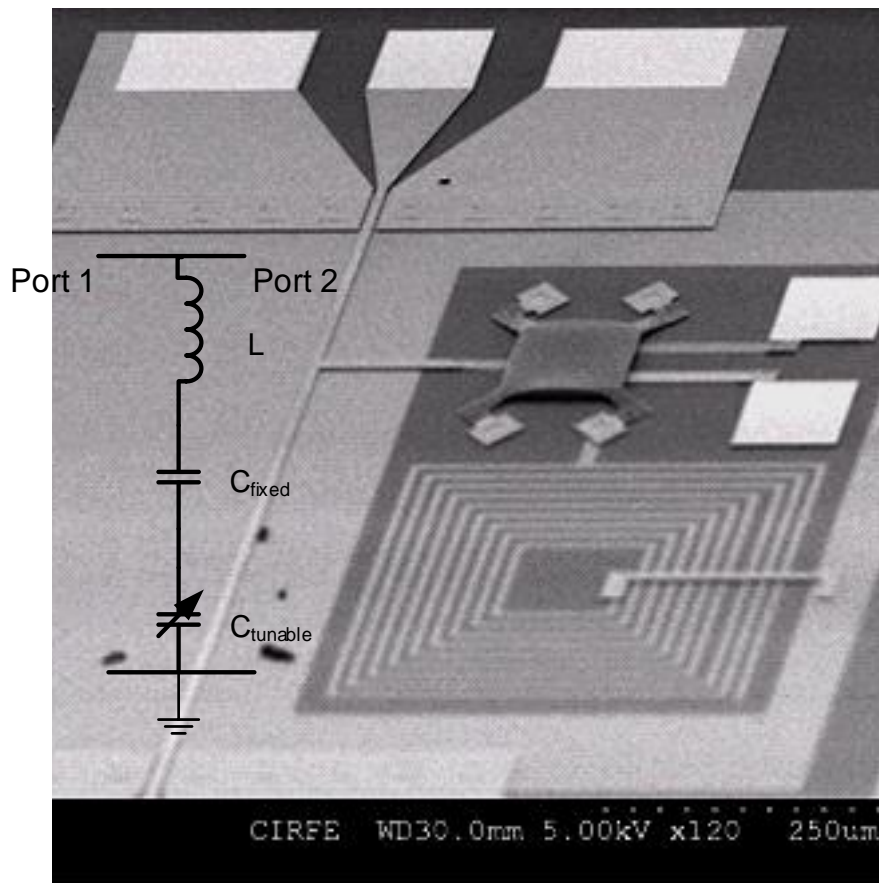


Fig. 5.43. SEM image of the integrated Nb-based MEMS tunable bandstop resonator. The varactor includes a fixed capacitor ( $C_{\text{fixed}}$ ) and a variable ( $C_{\text{tunable}}$ ) capacitor.

This resonator is measured by immersing the chip into liquid helium. The required voltage for the varactor tuning is applied across the signal line and the ground line of the CPW transmission line. Fig. 5.45 depicts the measured results of the tunable resonator at 4K. The results indicate a resonant frequency of 2.62 GHz when the capacitor plate is in its up-state position. The resonant frequency is

tuned by applying a sweep of actuation voltages to the varactor. The first variation in the resonant frequency is evident at 9 V. As the actuation voltage increases, the capacitance value increases, and the resonant frequency shifts to lower frequencies. By sweeping the actuation voltage up to 56 V, the centre frequency of the resonator sweeps down to 2.54 GHz. The varactor reaches its pull-in state at 58 V, which causes an abrupt frequency shift from 2.54 GHz to 1.95 GHz. This shows a continuous tuning range of 80 MHz and a discrete frequency variation of 670 MHz.

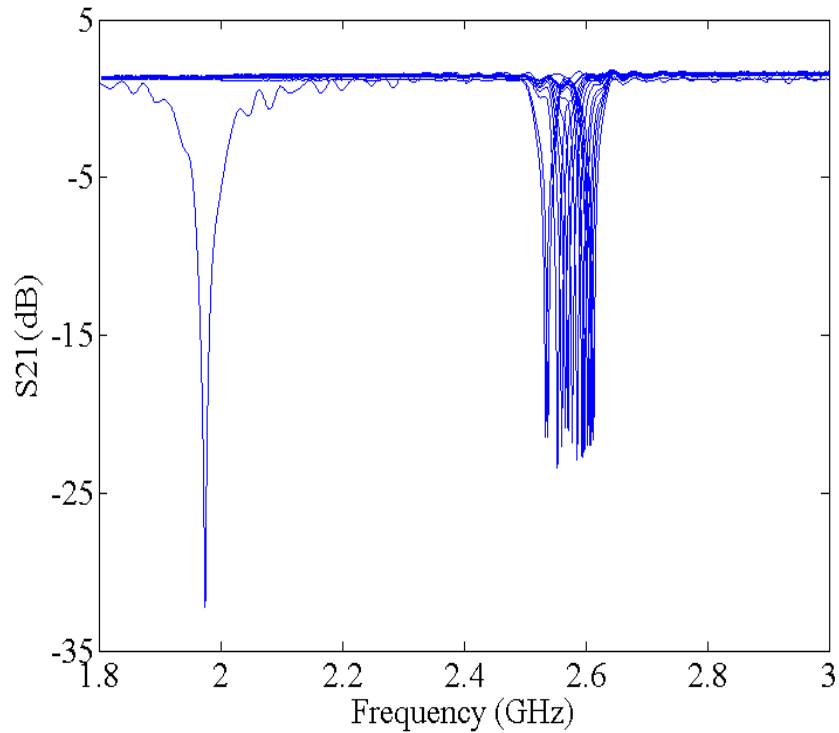


Fig. 5.44. Measured results for the tunable resonator implementing MEMS varactor at 4K.

Fig. 5.46 illustrates the variation of the resonant frequency versus the actuation voltage applied to the varactor. It shows that the resonant frequency decreases as the actuation voltage increases. There is a sudden variation of the centre frequency of the resonator just at the pull-in stage of the varactor.

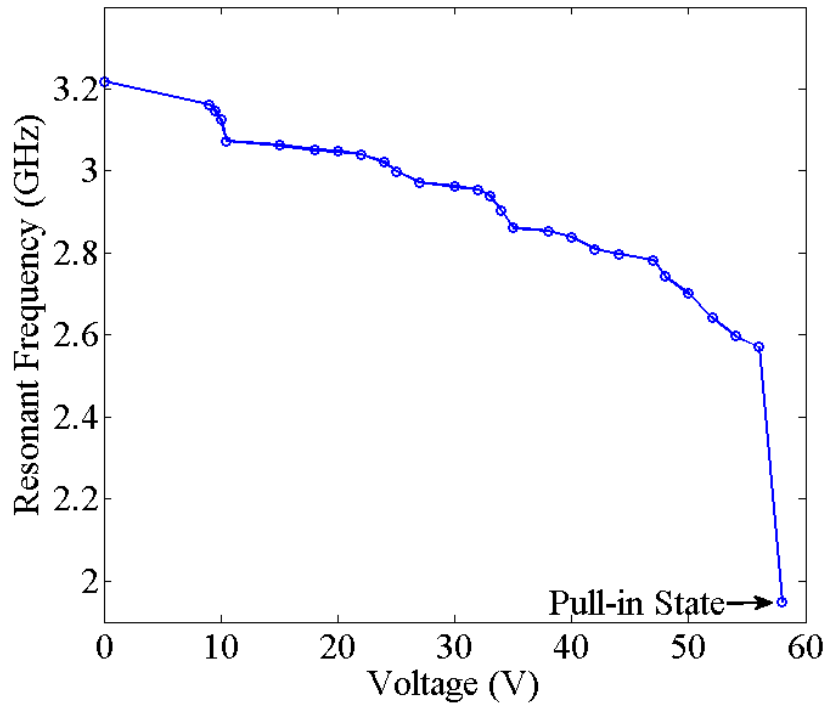


Fig. 5.45. Variation of the centre frequency of the resonator versus the actuation voltage applied to the varactor.

#### 5.4.4 Tunable Bandstop Filter Using Varactor

In order to achieve a filter with the highest possible tuning range using the MEMS varactor, a design approach is implemented employing an all-shunt-resonators topology. A fixed 3-pole BSF with all shunt resonators is designed for a centre frequency of 2 GHz and a percentage bandwidth of 5%. The schematic diagram of the filter is depicted in Fig. 5.47. The series resonator in the original shunt-series-shunt prototype is replaced with a shunt resonator and two  $90^\circ$  transmission lines with a characteristic impedance of  $50 \Omega$  as inverters.

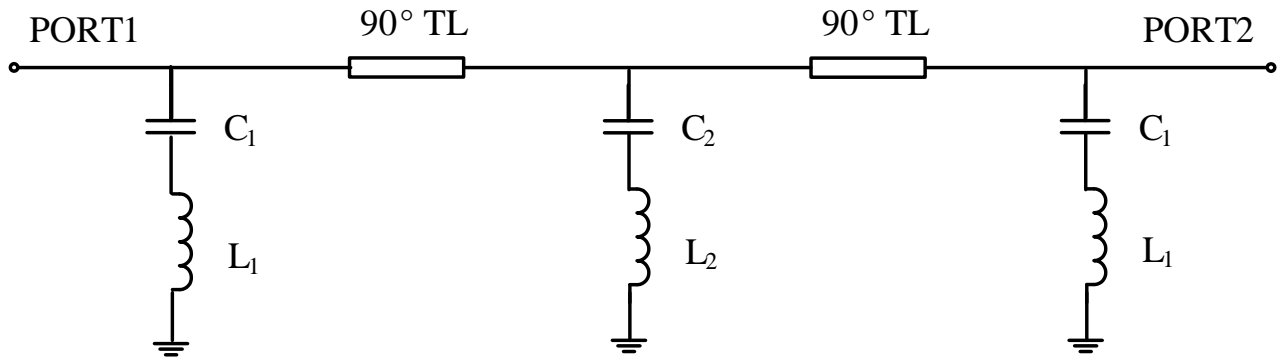


Fig. 5.46. Circuit model of the lumped element fixed BSF.



The multilayer aspect of the Hypres process allows for the realization of lumped element parallel plate capacitors and spiral inductors to design highly miniaturized lumped element filters while maintaining a high quality factor. Fig. 5.48 shows a picture of the fabricated fixed bandstop filter. The device measures only  $5 \text{ mm} \times 0.85 \text{ mm}$ , which is extremely miniaturized, considering that the wavelength at the centre frequency of the filter is  $150 \text{ mm}$ . The  $90^\circ$  TL between the resonators are microstrip lines that use the M0 metal layer as the ground plane and the M3 metal layer as the meander-shaped signal line [19]. The slots are introduced in the ground plane to reduce the characteristic impedance of the  $90^\circ$  TL to  $50 \Omega$ .

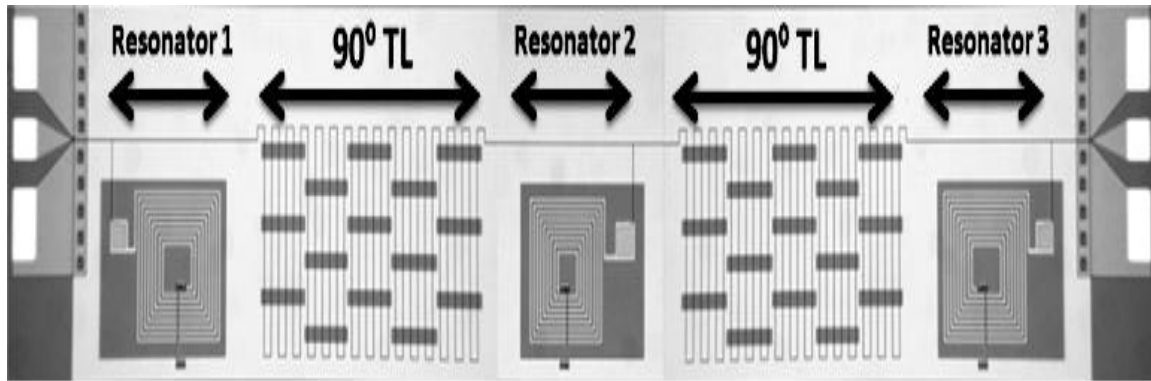


Fig. 5.47. Photograph of the fabricated fixed bandstop filter [19].

The fixed bandstop filter is measured using the Lakeshore probe station at  $4\text{K}$ . Fig. 5.49 shows the simulation and measured results of the fixed BSF. The small discrepancy of the filter's centre frequency is due to the difference in the simulated and measured dielectric permittivity, which is within the range of fabrication tolerances in the process. The difference in the simulated and measured  $S_{11}$  is also due to the fabrication tolerance on M3 metal layers, which affects the narrow TL between the resonators. This discrepancy can be minimized by changing the design of the TL to wide lines with trenches [19].

To achieve tunability, a MEMS varactor is added in series to the capacitor in each resonator. Fig. 5.50 illustrates the circuit model of the tunable filter. Each resonator includes a fixed capacitor, a tunable capacitor, and an inductor in series. The fixed capacitor in each resonator is constructed between M0 and M2, and the variable capacitor is between M2 and M3. The shunt resonators are coupled by  $90^\circ$  delay transmission lines.

Fig. 5.51 illustrates the measured results of the tunable filter at  $4\text{K}$ . The measured tuning range of the filter is narrow for several reasons. Since the buckling of the movable plates of the varactor after the release is not exactly the same, the filter response is initially detuned. Tuning each varactor

individually would achieve better results. However, since there are only 2 dc probes inside the cryogenic probe station, the only option is to apply the same voltage between the signal and ground of the filter using a bias-tee. For the same reason, the pull-in voltage of the varactor with less buckling is lower than that of the other varactors. Consequently, the maximum applied voltage is decided by the pull-in voltage of the varactor with the least amount of buckling. As a result, the tuning range for the filter is much less than that of the individual resonators.

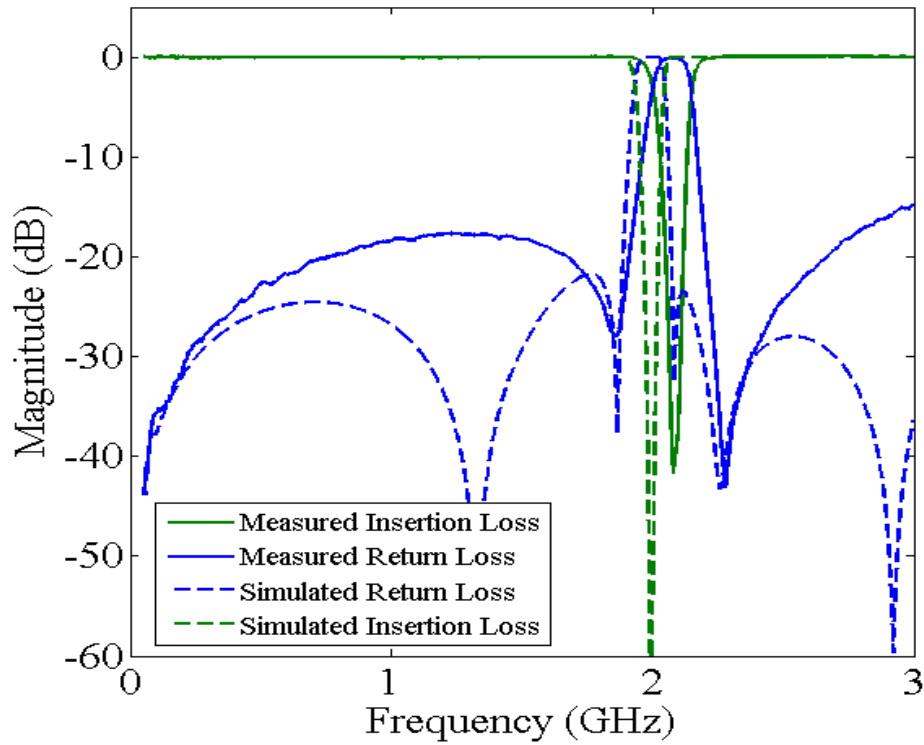


Fig. 5.48. Simulation and measured results of the superconducting BSF at cryogenic temperature.

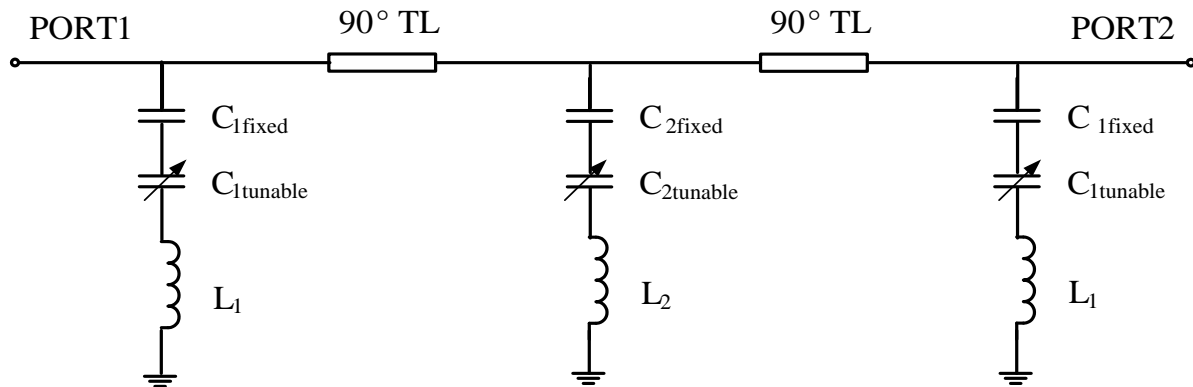


Fig. 5.49. Circuit model of the tunable lumped element BSF.

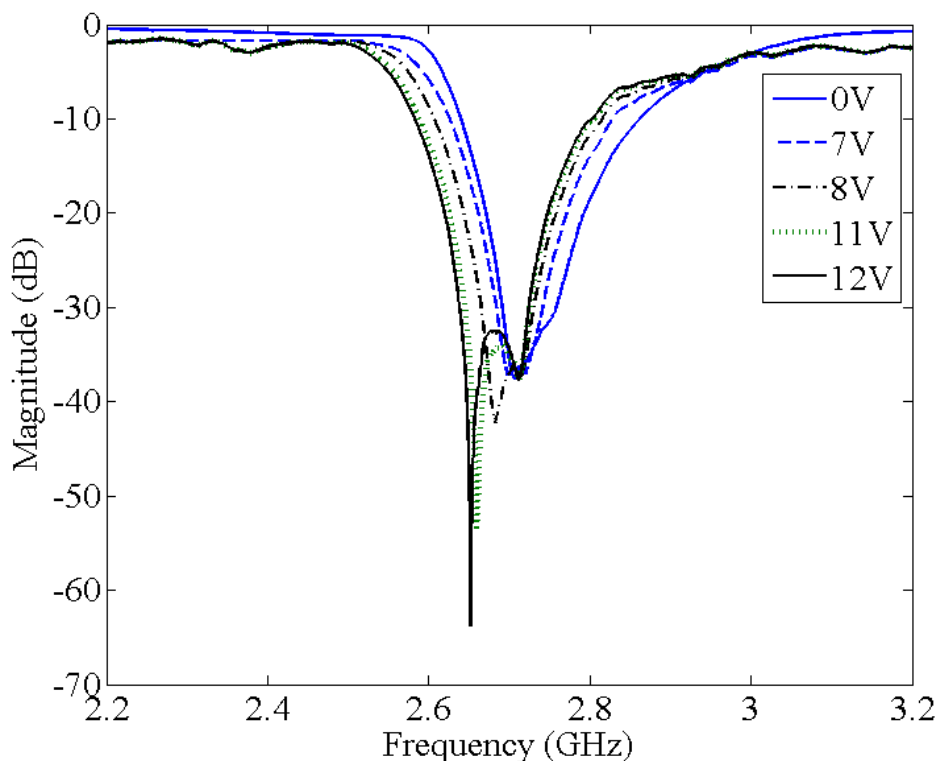


Fig. 5.50. Measured results of the insertion loss of the tunable BSA at 4K.

In this chapter, the post-processing steps that are applied as complementary steps to the Hypres fabrication process for releasing the MEMS devices were elaborated and various investigations for choosing optimum sizes of release holes were discussed. As well, dimples were successfully developed for dc-contact RF MEMS switches, despite the fact that there was no dimple mask on the Hypres micro-fabrication process.

Furthermore, dc-contact and capacitive-contact RF MEMS switches were fabricated using the same fabrication process employed in SME technology, making it possible to realize a high-speed receiver with a reconfigurable RF front-end integrated on the same chip. The RF performance of both switches indicated a significant improvement in the insertion loss of the switches when niobium superconducted. A superconducting RF MEMS varactor was also presented in this chapter. The measurement results of the varactor at 4K were provided, along with detailed mechanical and RF theoretical analyses.

All of the above devices were implemented in several tunable RF devices, including tunable resonators, tunable filters, capacitor banks, and SPDT switches. The RF performance of all devices was given both for room and cryogenic temperatures.

# Chapter 6 The Development of an Nb-Based Fabrication Technique

Although SME technology has the potential for realizing very low loss RF circuits, the pronounced nonlinearity of SME-based tuning elements hinders the applicability of the technology to implement high performance RF tunable circuits. The ability to integrate RF MEMS technology with SME technology will make it possible to realize low-loss and highly linear tunable RF devices for SME receiver applications. However, while Nb-based RF MEMS can be integrated within the Nb-layers of SME technology, designers often do not have the flexibility to select the thickness of the MEMS structural layers.

A novel Nb-based 8-mask fabrication process that integrates gold-based RF MEMS devices with Nb-based RF circuits is introduced in this section. The fabrication is carried out in the CIRFE laboratory at the University of Waterloo. Various types of superconducting MEMS-based devices are designed, fabricated and characterized, as elaborated in this section.

## 6.1 Nb Fabrication Process

A novel 8-mask process developed for the fabrication of Nb-based devices is illustrated in Fig. 6.1. It is a modified version of the UW-MEMS fabrication process introduced in [46] for superconducting RF devices.

After the RCA cleaning of the alumina substrate, 40 nm TiW is sputtered as the bias lines and actuation pads. Only non-magnetic metals can be used for the bias lines, since magnetic metals contaminate the dedicated chamber for Nb deposition. Mask 2 defines the opening in the silicon oxide (700 nm) layer deposited to passivate the bias lines.

Nb is deposited for the RF circuits. Initially, Nb is patterned prior to depositing the next layer. However, after Nb patterning, the adhesion of the second gold layer to Nb is very poor, which may be due either to a thin layer of Nb oxide being formed that prevents the adhesion of gold to Nb, or to some residue of photo-resist (PR) remaining on the Nb surface. To solve the problem, two methods are investigated. The first approach is to cover Nb with gold in-situ to prevent the formation of an Nb-oxide layer and promote the adhesion of gold to Nb. In this approach, Nb adhesion to gold is very good; the gold layer is patterned first, followed by the Nb layer. In the second approach, a bi-layer of Cr/Au is deposited on Nb prior to the patterning. The bi-layer is patterned first, after which the Nb is patterned. It should be mentioned that neither gold wet etchant (Transene gold etchant) nor Cr etchant attack Nb. Experiments show that both approaches are highly useful in promoting gold adhesion to Nb.

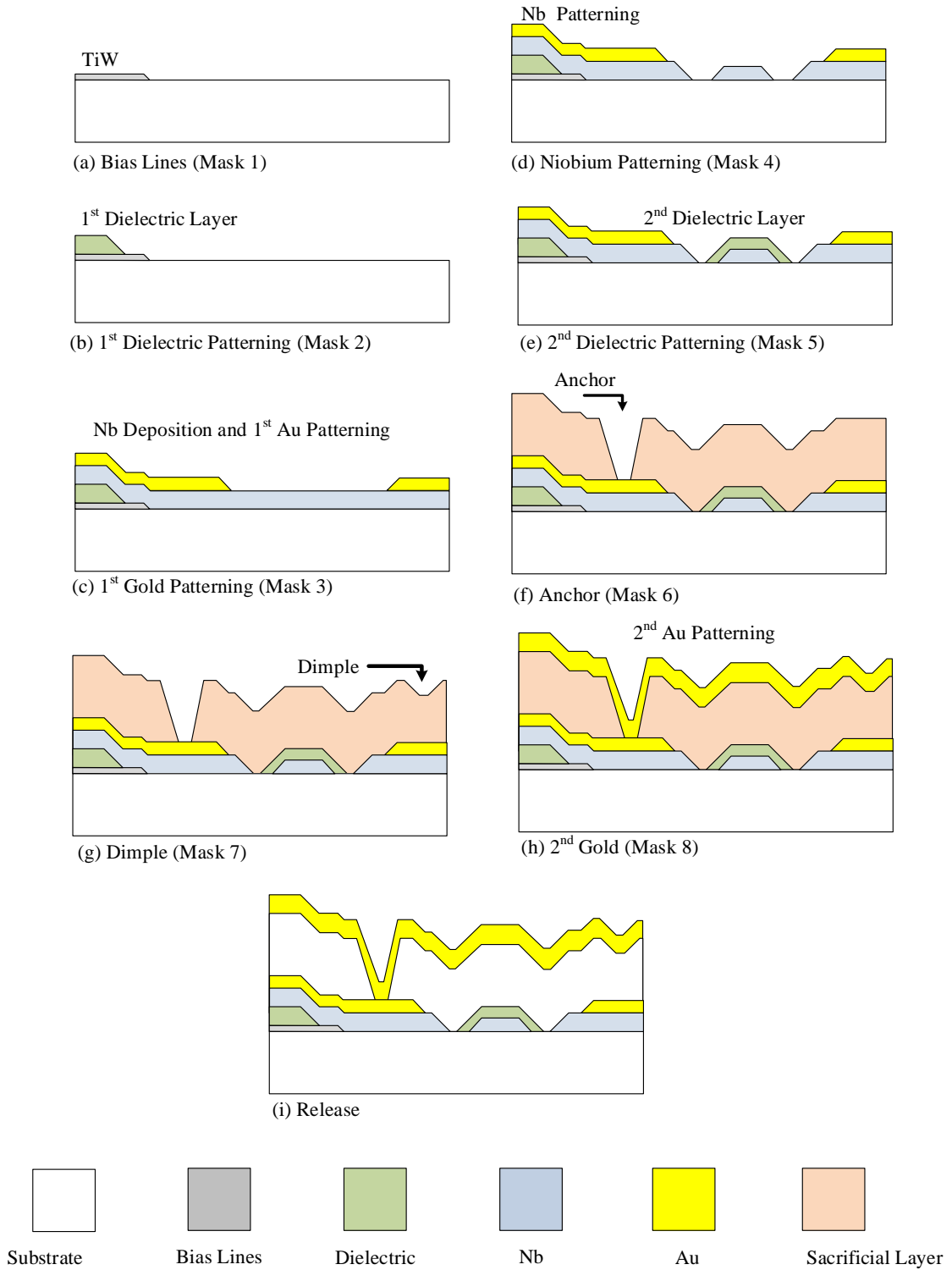


Fig. 6.1. The fabrication process steps to integrate Nb-based RF circuits with gold-based MEMS structures

Mask 3 defines the pattern of the first Au layer deposited on Nb, and then Nb is patterned using Mask 4. Dry-etch is used to etch Nb in an RIE system. Next, the second dielectric layer is deposited and patterned using Mask 5, and Polyimide (PI2562, HD Microsystems) is employed as the sacrificial layer. The speed and timing of the spin-coating is adjusted to produce a polyimide layer approximately 2  $\mu\text{m}$  thick that specifies the initial air gap of the devices. The high temperature annealing of PI is done on a hot-plate for 2 hours at 160°C. Normally, PI is cured in a furnace at temperatures of around 350°C; however, experiments show that curing PI in a furnace at such a high temperature oxidizes Nb.

Next, the polyimide is dry-etched in an RIE system to create the anchor and dimples using Mask 6 and Mask 7, respectively. Finally, the electroplating of the second gold layer (1.8  $\mu\text{m}$ ) completes the structure. The sacrificial layer is removed using wet-etching process and the samples are immersed in EKC 265 (DuPont Plasma Solve) and placed in a CPD.

Four locations are considered for the Nb deposition: the CIRFE lab and QNC (Quantum-to-Nano-Centre), both located at the University of Waterloo; Cornell University; and STAR Cryoelectronics. Table 6.1 shows the critical temperature ( $T_c$ ) of Nb in each centre provided to us by QNC. The  $T_c$  of Nb deposited in the CIRFE lab is low, since there are magnetic metals deposited in the same chamber, which contaminates Nb and significantly reduces its critical temperature. In fact, it would be advisable to allocate a chamber exclusively for Nb deposition, to prevent any contamination. For this thesis, the Nb deposited in QNC is used due to its good  $T_c$ , accessibility, and cost.

Table 6.1. Critical temperature of Nb deposited in the four available centres.

| Deposition Centre | CIRFE Lab | QNC  | Cornell | StarCryo |
|-------------------|-----------|------|---------|----------|
| $T_c$             | 2.8K      | 8.5K | 7.5K    | 9.1K     |

## 6.2 Single-layer Nb devices

The measurement started with a CPW TL with dimensions of 55  $\mu\text{m}$ / 110  $\mu\text{m}$ / 55  $\mu\text{m}$ . The first run of fabrication includes a single layer Nb, meaning the RF and dc probes are in direct contact with Nb. The results illustrate that there is no transmission at low frequencies. The conclusion is that there is a large coupling capacitance at the two ports of the device, which prevents the signal from being transmitted at low frequencies. At high frequencies, the large coupling capacitance acts as a short circuit. In addition, Nb resistivity is measured at room temperature and shows that the Nb layer is not conductive after going through the fabrication process steps. Various types of single-layer Nb filters and transmission lines are measured at both room and cryogenic temperatures, and these also show

similar behavior. The measurement of a low-pass filter (LPF) shows a performance similar to the TL. Furthermore, while there is no signal passing at low frequency, the filter response is closer to the simulated results at high frequency.

Our investigations show that a thin insulating layer forms on the surface of Nb after it goes through the lithography and patterning steps. This is the layer that forms the coupling capacitance between CPW probes and the input/output ports and can be penetrated by scratching the Nb surface by the tip of a dc probe. However, it still affects the RF measurement.

To eliminate the effect of the contaminated Nb surface, Au is deposited on Nb prior to patterning the Nb thin film. The Au layer is used where there is a need for a metal contact to the Nb layer, such as in the pads for RF and dc probing, the anchors, and the dimples. Two approaches are investigated. In the first approach, Au is deposited on Nb in-situ; in the second, a bi-layer of Cr/Au is deposited on Nb after it is exposed to air. A single-layer Nb-based 3-pole BPF is designed and simulated for a centre frequency of 9 GHz and a percentage bandwidth of 10%. Two versions of the BPF are fabricated: one with Au deposited in-situ, and the other with a bi-layer of Cr/Au. Fig. 6.2 presents a picture of the fabricated device. Both filters are measured in a cool-down run at the Lakeshore probe-station and similar calibration. Fig. 6.3 shows the measured results of the Nb-based BPF with gold pads at 4K. The results show no sign of the contaminated Nb and also confirm that the effect of Cr loss is negligible. The investigation regarding the loss of Cr is important in our case, since the in-situ deposition of Au on Nb is not possible in the CIRFE lab due to equipment limitations.

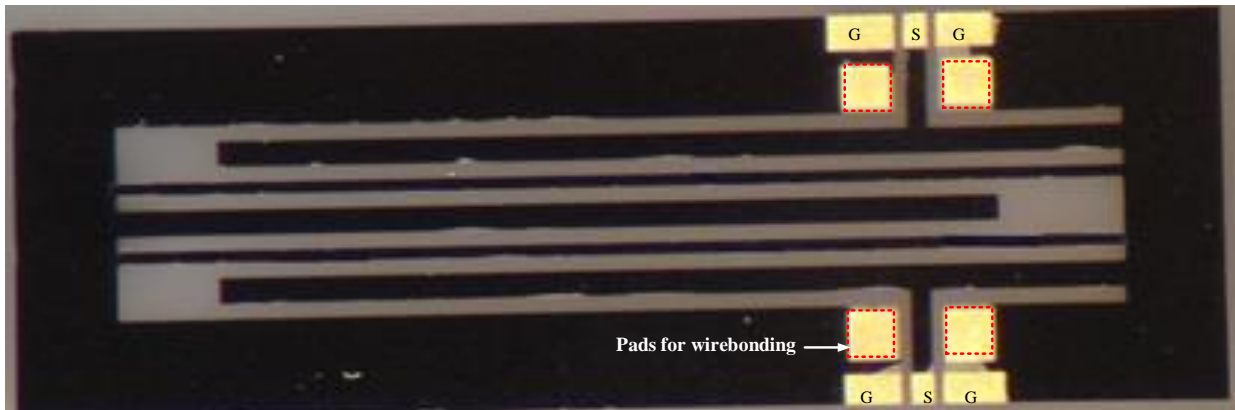


Fig. 6.2. Photograph of the Nb-based BPF with gold pads.



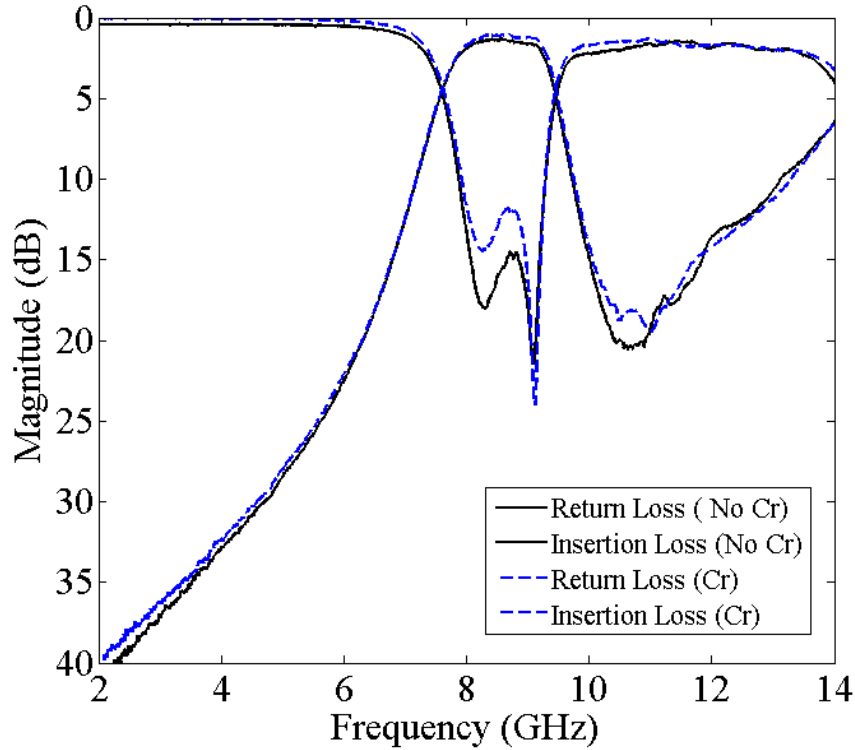


Fig. 6.3. The measured results of the RF response of Nb-based BPF at 4K with Au pads and Cr/Au pads.

### 6.3 Multi-layer Nb devices

As a first step, a TL with the dimensions of  $55\ \mu\text{m}/110\ \mu\text{m}/55\ \mu\text{m}$  is measured both at room and cryogenic temperatures. A simple TL is considered as the test structure to evaluate any variations in the critical temperature of the Nb layer after going through all 8-mask process steps. Fig. 6.4 shows the measured results of the TL. During the cryogenic measurement, the temperatures of the sample stage and RF probe arms are around 3K and 8K, respectively, at the Lakeshore probe-station. There is an improvement of more than 2 dB in the insertion loss of the TL at cryogenic temperature when compared to room temperature. The simulation results in Sonnet show that the Nb conductivity at room temperature is in the range of  $6 \times 10^6\ \text{S/m}$ .

Another test structure measured is the previously discussed LPF with gold pads added for probing at room and cryogenic temperatures. The effect of the contaminated Nb is eliminated by adding the Au layer for probing. Fig. 6.5 shows the RF performance of the LPF at 4K. The results show significant improvement in the insertion loss of the filter at cryogenic temperature compared to room temperature.

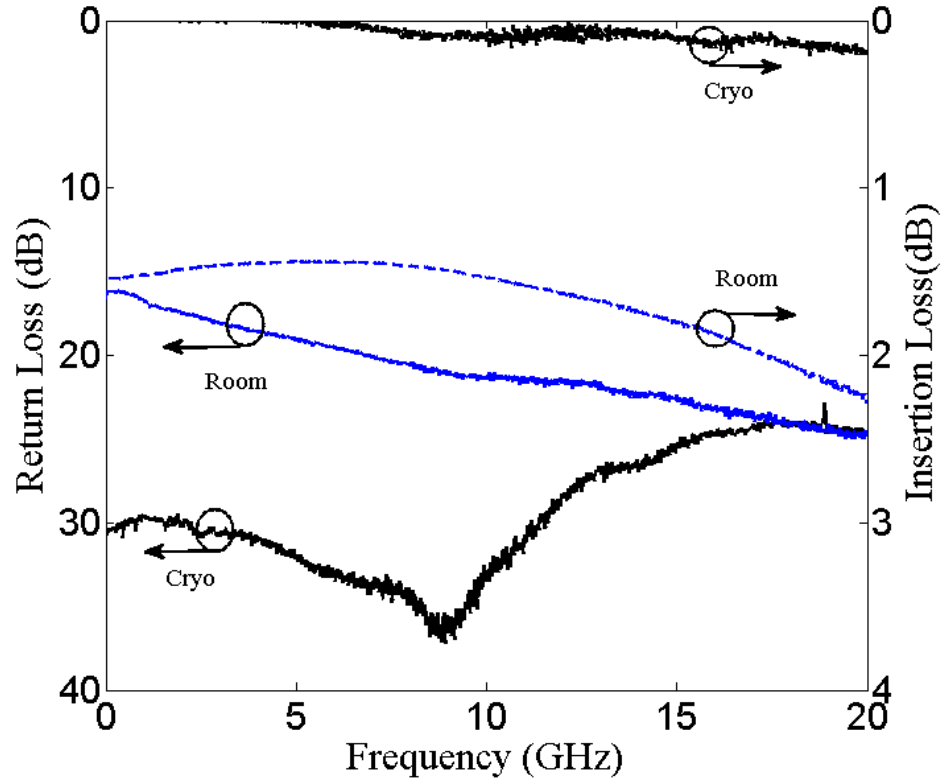


Fig. 6.4. The measured results of the RF response of Nb-based TL with gold pads at room temperature and 4K.

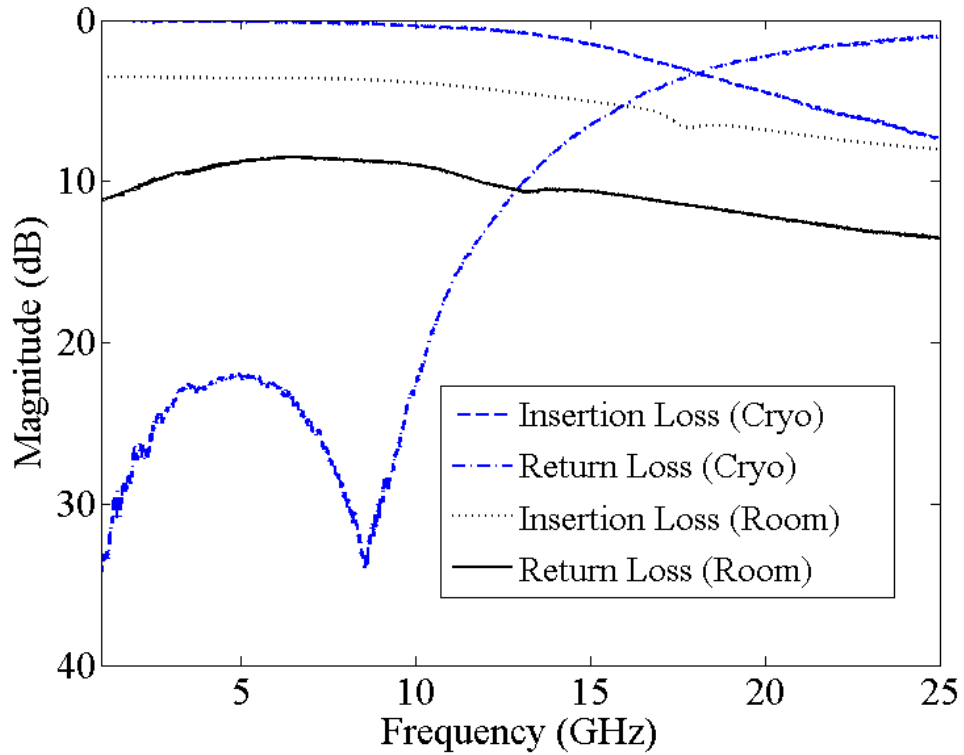


Fig. 6.5. The measured results of the RF response of Nb-based LPF with gold pads at room temperature and 4K.

### 6.3.1 DC-Contact RF MEMS Switch

Fig. 6.6 shows the top view of a dc-contact RF MEMS switch fabricated using the newly developed Nb-based process. The switch is ‘off’ when the cantilever beam is in the up-state position and ‘on’ when the beam is in the down-state position. Fig. 6.7 shows the SEM image of the switch, which is measured at room temperature. To actuate the device, dc voltage is applied to the bias pad and the signal line is grounded. Fig. 6.8 shows the measured and fitted simulation results of the ‘on’ and ‘off’ states of the switch at room temperature. The insertion loss of the switch is very high at room temperature due to the low conductivity of Nb at that temperature. The actuation voltage of the switch is 20 V at room temperature. Fig. 6.9 shows the measured and fitted simulation results of the switch RF performance at cryogenic temperature. The results show a significant improvement in the insertion loss and return loss of the switch at 4K, and the actuation voltage of the switch is 40 V at cryogenic temperature. The pull-in voltage of the switch changes at cryogenic temperature (compared to room temperature) from 20 V to 40 V, which, according to the discussion in Chapter 3, should be expected.

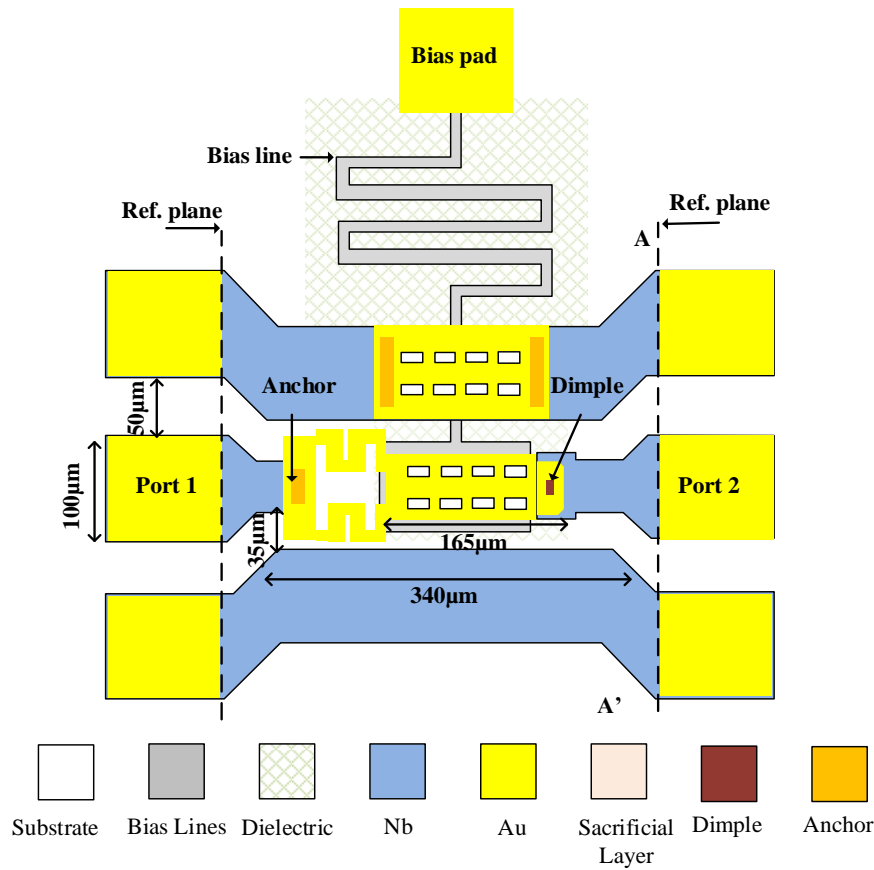


Fig. 6.6. The top view of the superconducting dc-contact RF MEMS switch fabricated using the 8-mask process in the CIRFE lab.

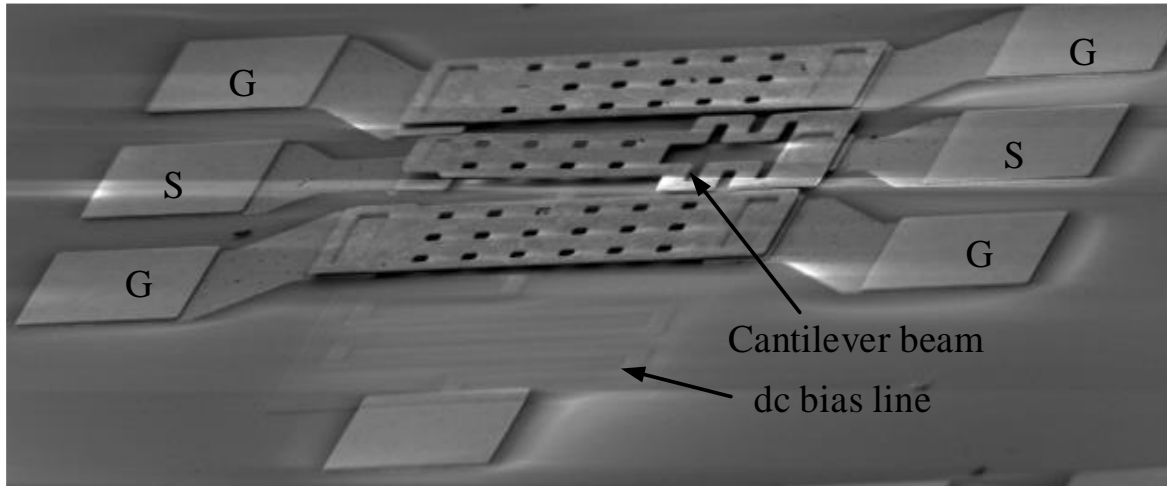


Fig. 6.7. SEM image of the superconducting dc-contact RF MEMS switch.

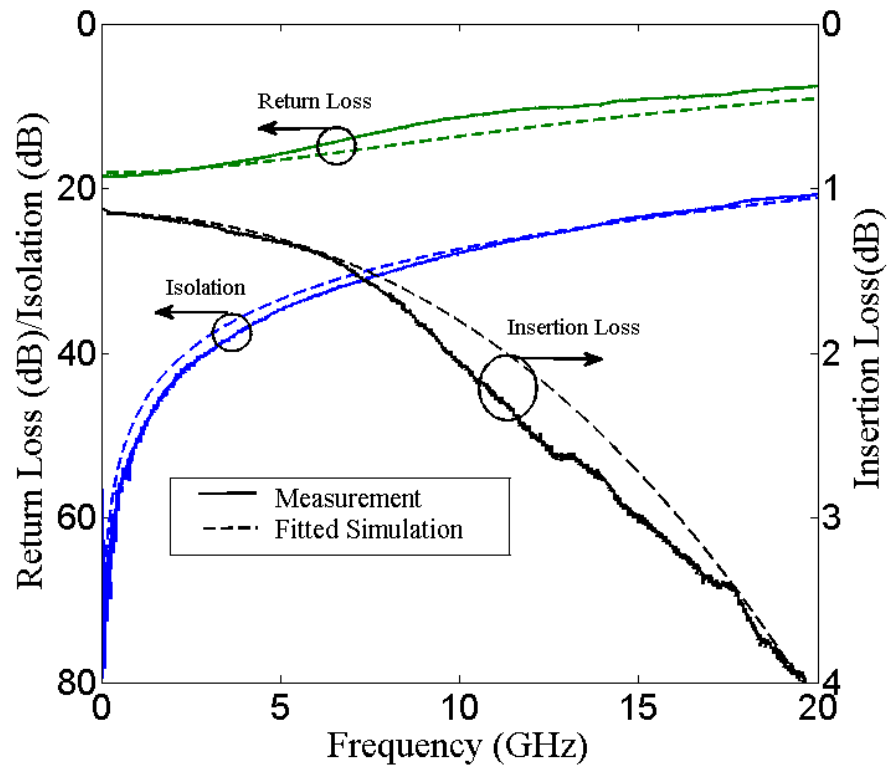


Fig. 6.8. The measured and simulated S-parameters of the superconducting dc-contact RF MEMS switch at room temperature.

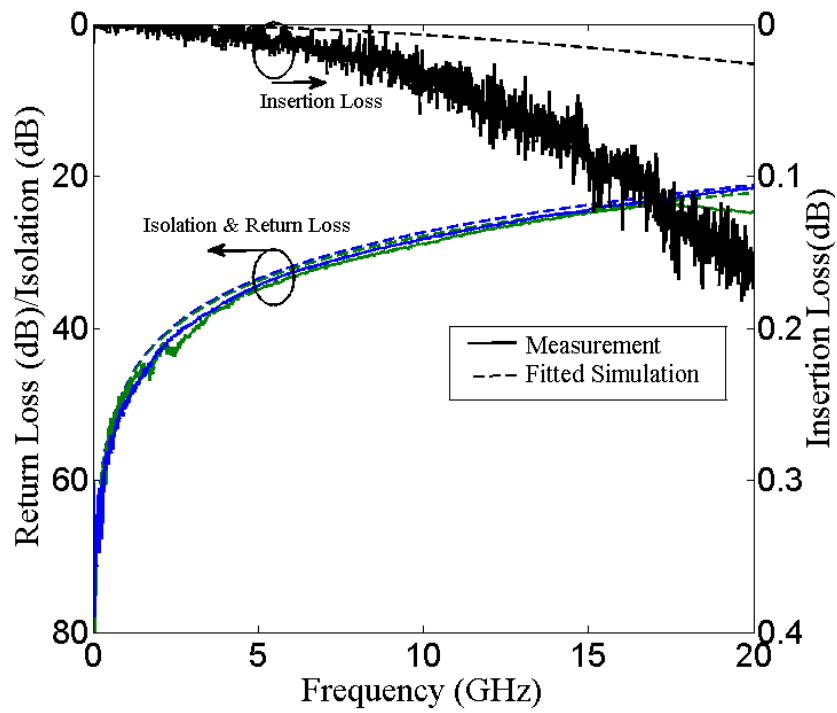


Fig. 6.9. The measured and simulated S-parameters of the superconducting dc-contact RF MEMS switch performance at cryogenic temperature.

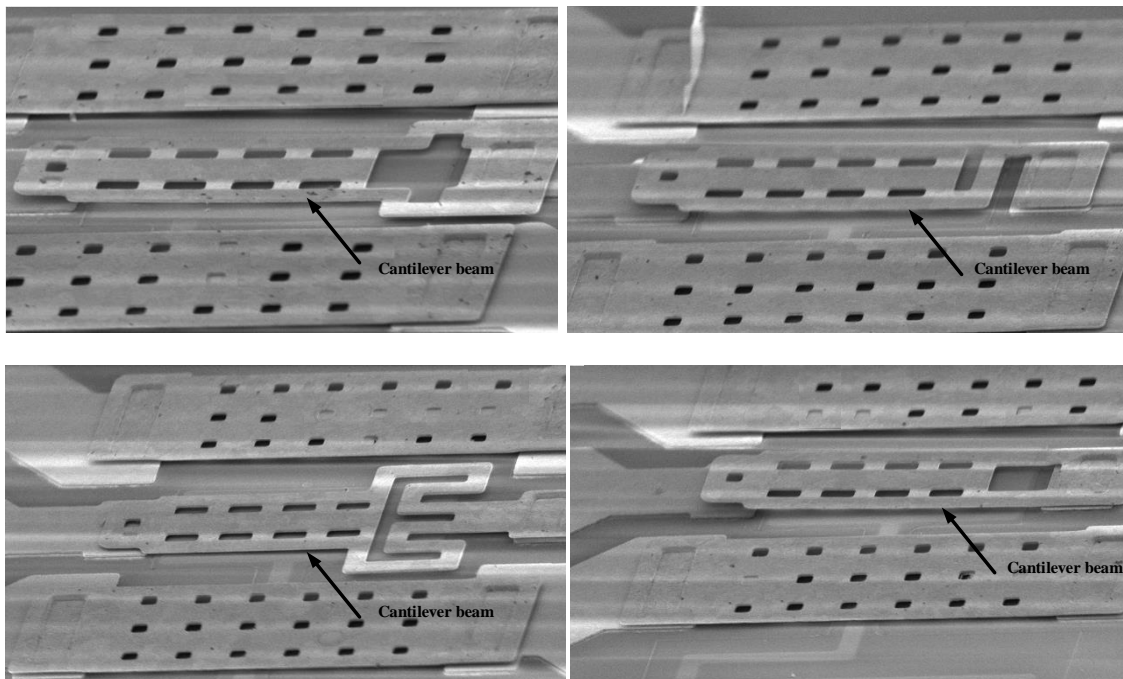


Fig. 6.10. SEM image of several designs of gold-based dc-contact RF MEMS switches monolithically integrated with Nb-based RF circuits.

Many dc-contact RF MEMS switches is fabricated and tested, each has different supports to estimate the actuation voltage and deflection of the switches at cryogenic temperature. Fig. 6.10 shows the SEM images of some of the fabricated switches.

### 6.3.2 Capacitive-Contact RF MEMS Switch

Fig. 6.11 shows the top view of a capacitive-contact RF MEMS switch fabricated using the newly developed Nb-based process. The switch is ‘on’ when the beam is in the up-state position and ‘off’ when the beam is in the down-state position. Fig. 6.12 shows the SEM image of the switch, which is measured at room temperature. To actuate the device, a dc voltage is applied between the signal line and the ground plane through a bias-tee. Fig. 6.13 shows the measured and fitted simulation results of the ‘on’ and ‘off’ states of the switch at room temperature. The insertion loss of the switch is about 3 dB at room temperature due to the low conductivity of Nb at that temperature. The actuation voltage of the switch is 16 V at room temperature.

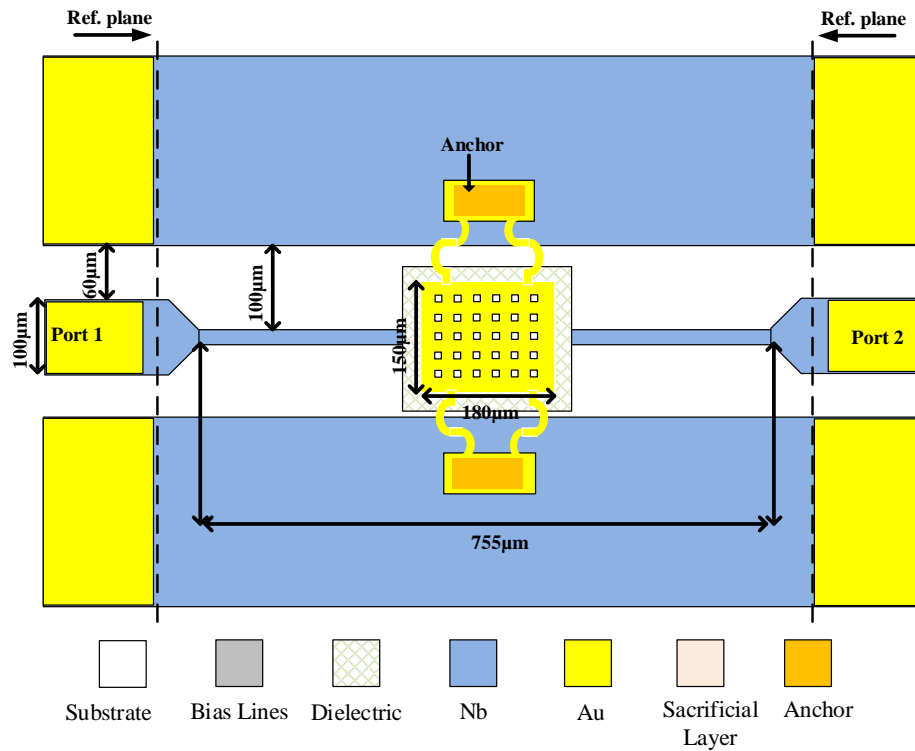


Fig. 6.11. The top view of the superconducting capacitive-contact RF MEMS switch fabricated using the 8-mask process in the CIRFE lab.

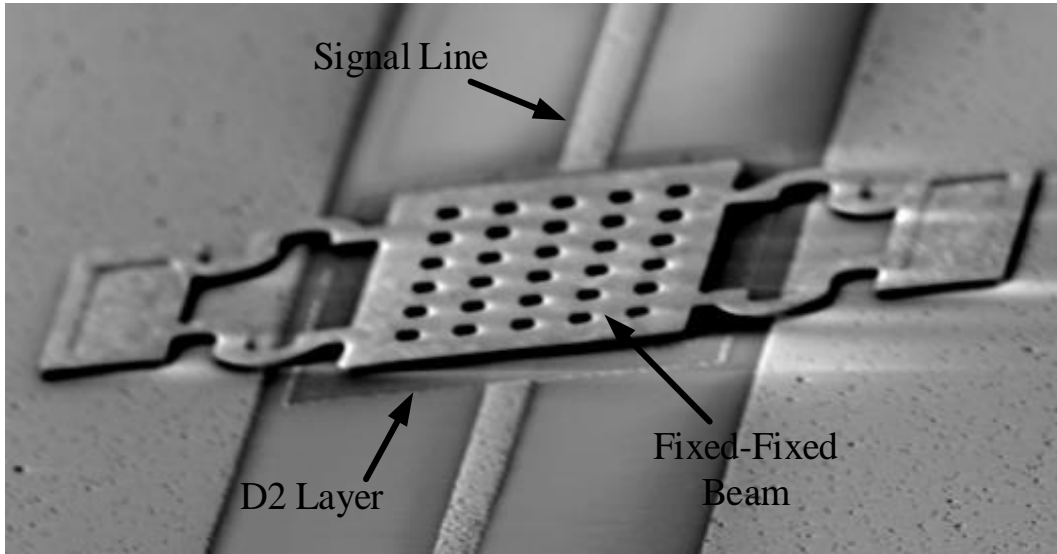


Fig. 6.12. SEM image of the superconducting capacitive-contact RF MEMS switch.

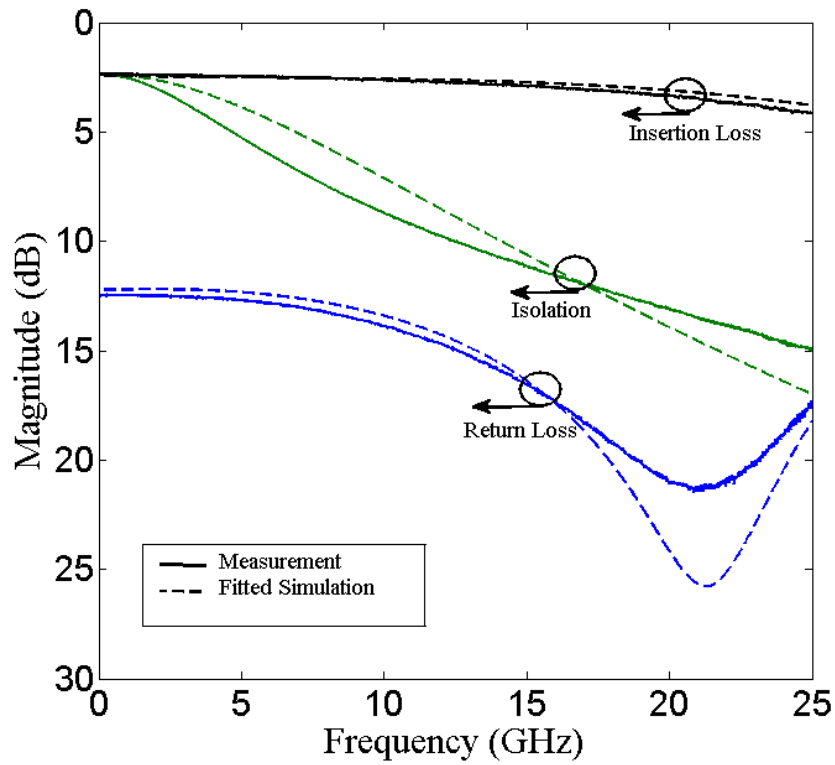


Fig. 6.13. The measured and simulated S-parameters of the superconducting capacitive-contact RF MEMS switch at room temperature.

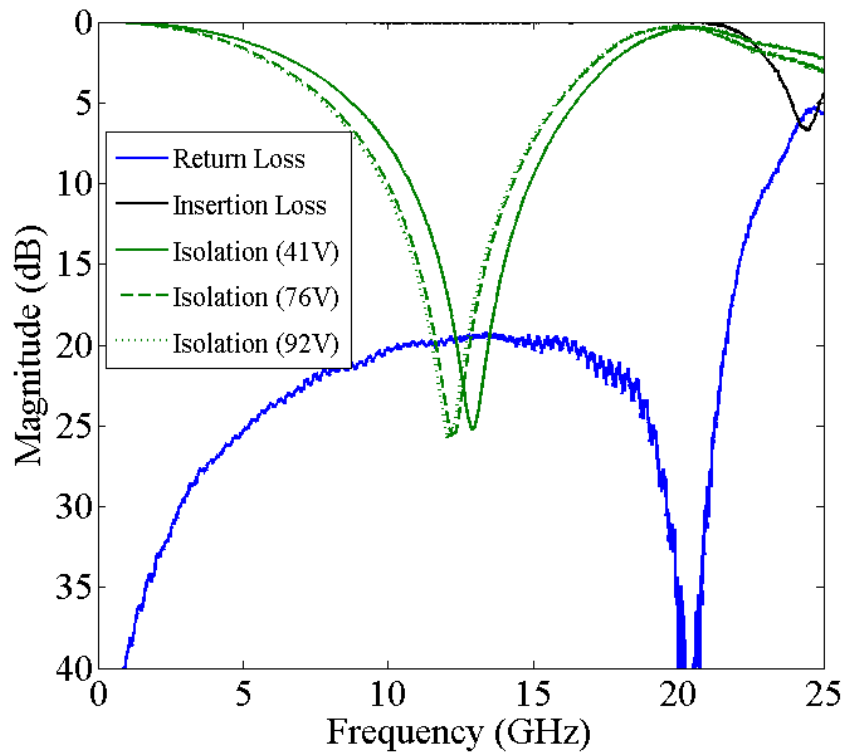


Fig. 6.14. The measured S-parameters of the superconducting capacitive-contact RF MEMS switch at cryogenic temperature for different actuation voltage values including: 0 V, 41 V, 76 V and 92 V.

Next, the switch is measured at cryogenic temperature. Fig. 6.14 shows the measured results at 4K for different actuation voltages, with the pull-in voltage at 41 V. By increasing the actuation voltage to higher values, the resonance frequency shifts to lower values, indicating that the plate is flattening on top of the dielectric layer. No additional changes are evident after 92 V. The isolation and return loss of the switch is about 20 dB between 11 GHz to 13 GHz and the insertion loss is close to zero. Many capacitive-contact RF MEMS switches are fabricated and tested, each with different supports to estimate the actuation voltage and deflection of the switches at cryogenic temperature. Fig. 6.15 shows the SEM images of some of these switches.



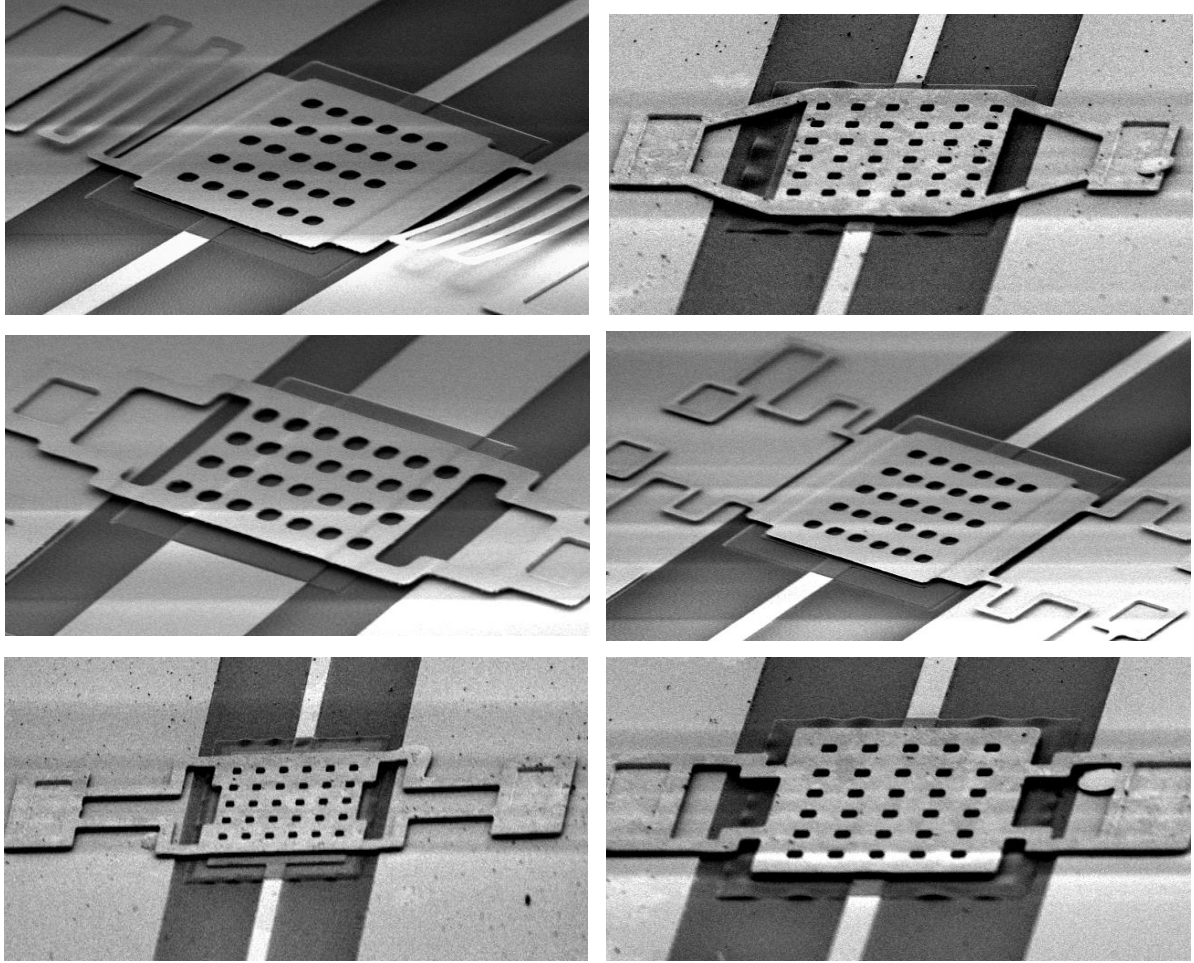


Fig. 6.15. SEM image of several designs of gold-based capacitive-contact RF MEMS switches monolithically integrated with Nb-based RF circuits.

### 6.3.3 Capacitor Bank

Fig. 6.16 shows the SEM image of a capacitor bank along with its circuit model. The RF MEMS switch is a dc-contact series type. There are four RF MEMS switches that connect four fixed capacitors to the ground, and the value of  $C$  is about 0.22 pF at 1 GHz. The device is measured in the Lakeshore cryogenic probe-station at 4K. Fig. 6.17 illustrates the increase of  $Q$  at 4K compared to room temperature for the smallest capacitance value, while Fig. 6.18 shows the extracted capacitance values from the measured S-parameters at cryogenic temperature. The capacitance value varies from 0.22 pF to 5.25 pF at 1 GHz, and the actuation voltage for each switch is around 50 V at cryogenic temperature.

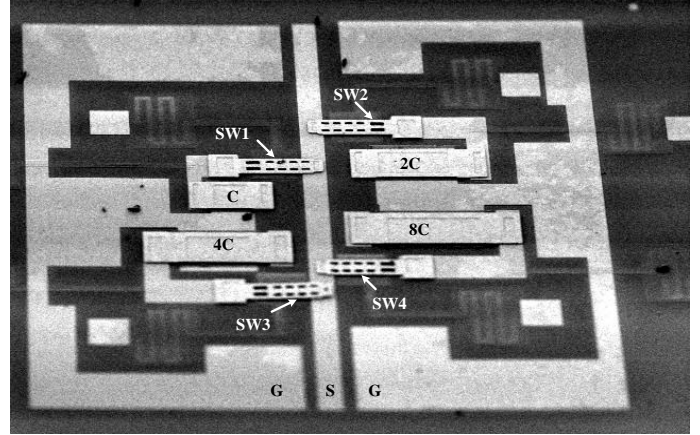
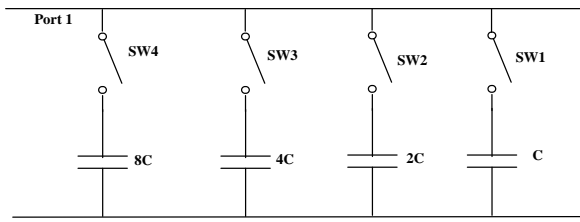


Fig. 6.16. The circuit model and the SEM image of the niobium superconducting capacitor bank implementing four dc-contact RF MEMS switches.

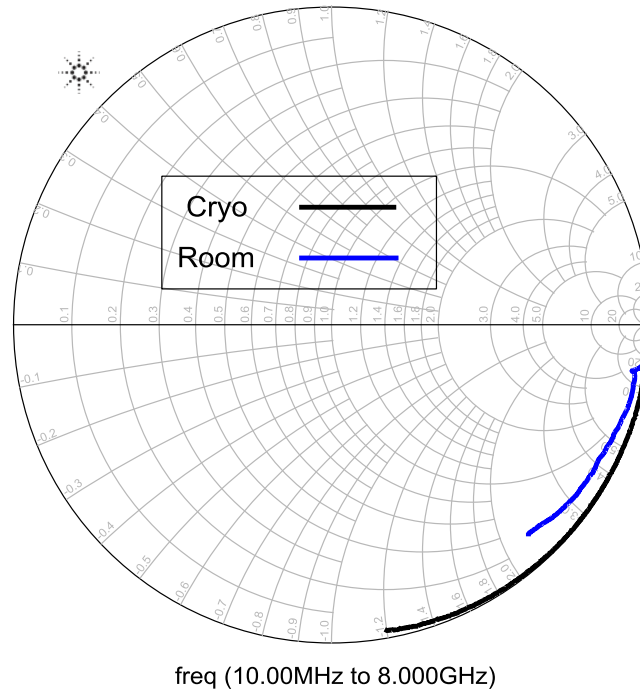


Fig. 6. 1. Q variation for the smallest capacitance value at 4K compare to room temperature.

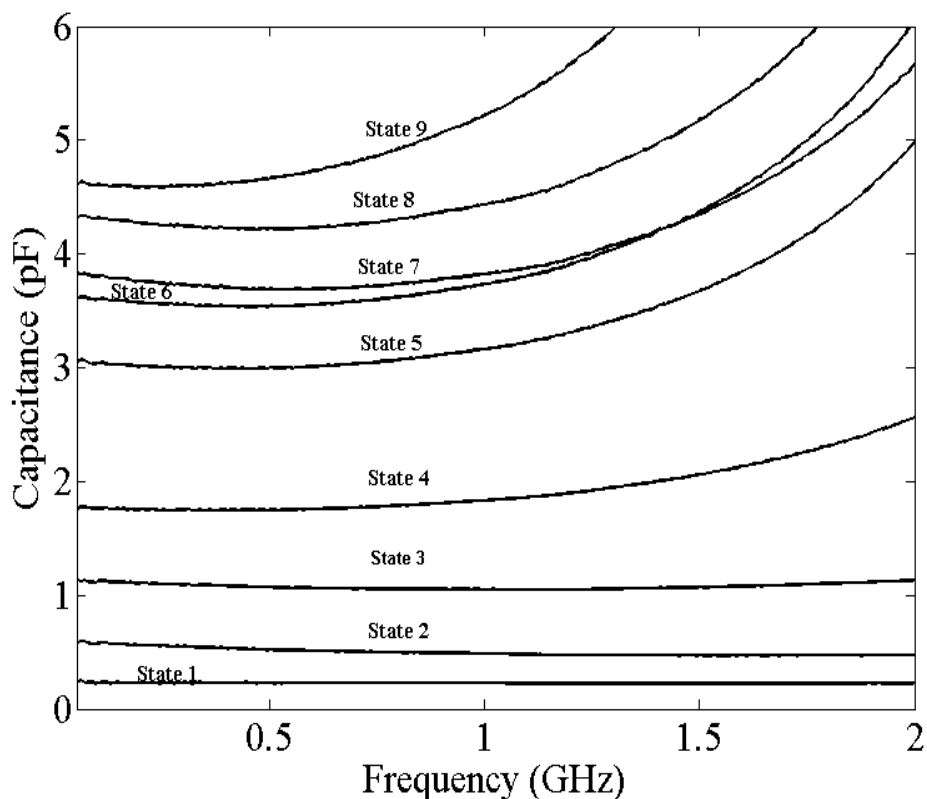


Fig. 6.17. The extracted capacitance value from the measured S-parameters of the superconducting RF MEMS capacitor bank implementing dc-contact RF MEMS switches at cryogenic temperature.

### 6.3.4 Tunable Bandpass Filter

The tunable filter designed, fabricated, and tested here is a 3-pole BPF with three distinct states of 8, 9 and 10 GHz, with each state having a 20 dB return loss channel bandwidth of 1 GHz over the passband [42]. Fig. 6.19 shows the layout of the filter. The RF MEMS switches are used to enable loading of the resonator while adjusting the coupling at the same time [42]. When the dc-contact RF MEMS switches are in the up-state position, the resonators and loading structures are weakly coupled. As soon as the RF MEMS switches are in the down-state position, the loading structures become part of the resonator and lower the resonant frequencies.

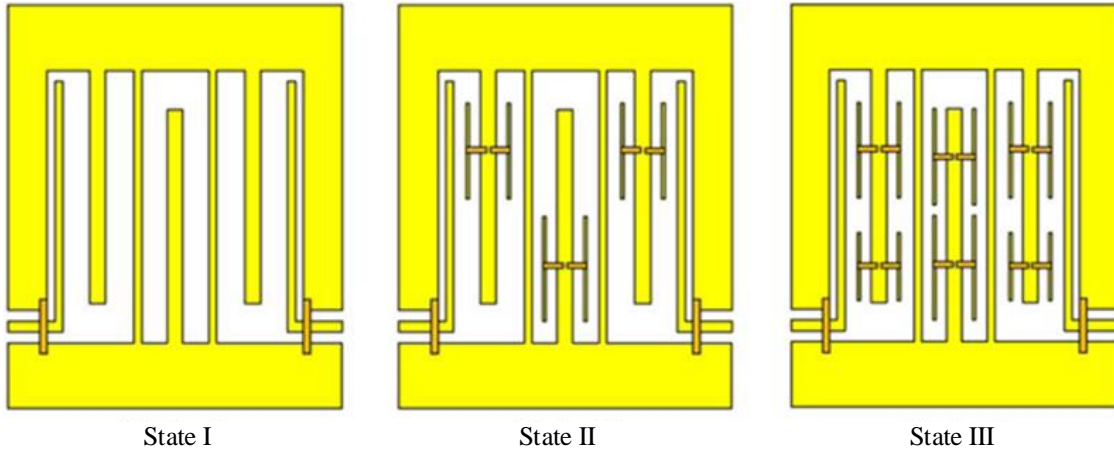


Fig. 6.18. Layout of the 3-pole BPF showing three different states of the filter for three different configurations of MEMS switches [42].

Fig. 6.20 and Fig. 6.21 show the simulation results along with the room temperature measured results of the insertion loss and return loss of the gold-based filter introduced in [42], respectively. The insertion loss in all three states is better than 3.5 dB, with the return loss better than 10 dB across the frequency band. According to [42], several factors can cause a discrepancy between the simulation and measured results, including radiation, substrate thickness, fabrication tolerances, and warp-up of the MEMS switches.

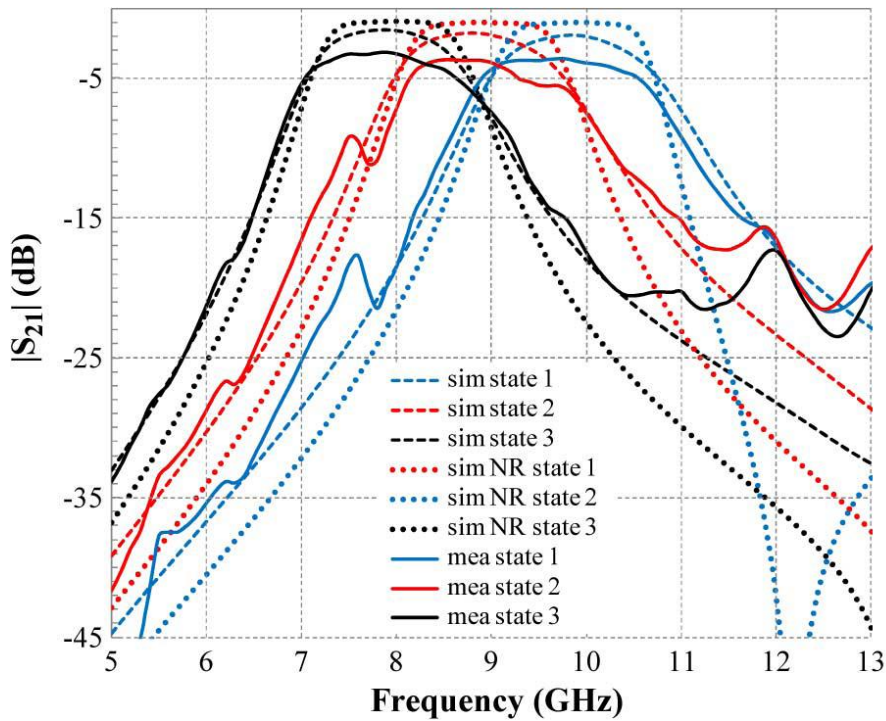


Fig. 6.19. The measured and simulated results of the insertion loss of the 3-pole gold-based BPF [42].

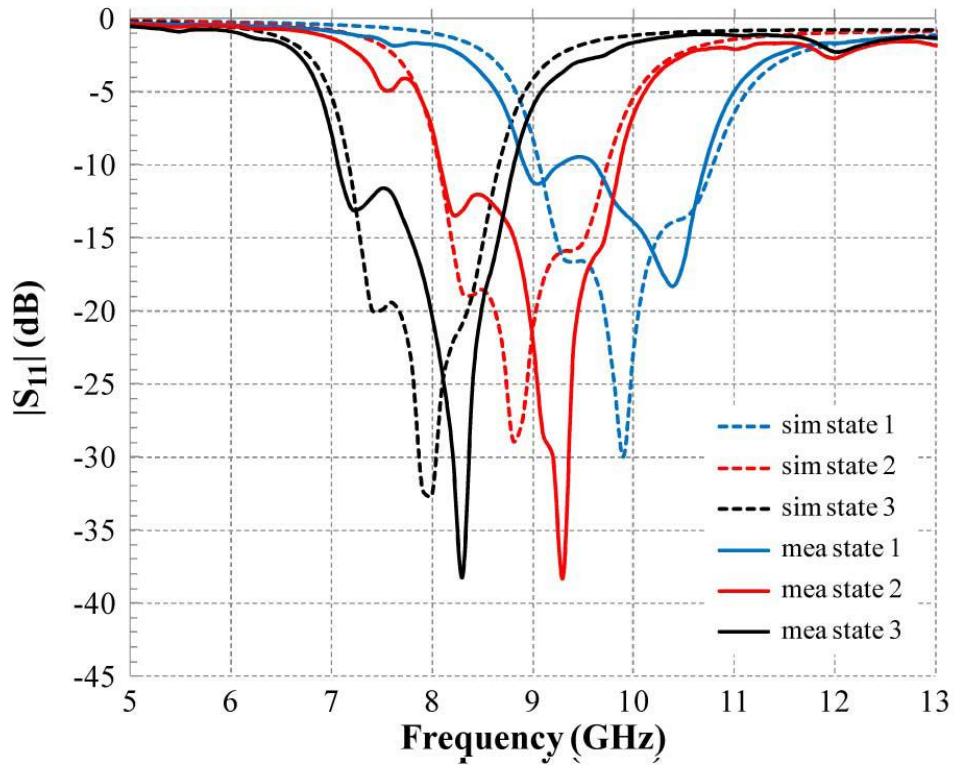


Fig. 6.20. The measured and simulated results of the return loss of the 3-pole gold-based BPF [42].

Fig. 6.22 shows an SEM image of the fabricated superconducting Nb-based filter integrated with gold-based dc-contact RF MEMS switches. Fig. 6.23 shows the measured results of only two states (State I and State II) of the filter at cryogenic temperature. The return loss of the filter is better than 10 dB. The insertion loss is very close to zero for State I and approximately 1.3 dB for State II. The improvement in the insertion loss of the superconducting-based BPF compared to the gold-based BPF is more than 3 dB for the first state and better than 2.2 dB for the second state. It should be mentioned that the filter is originally designed to be fabricated with gold and that this is not optimized to fully benefit from the superconducting behavior of Nb. A better RF performance would certainly have been obtained by taking into account factors such as radiation, fabrication tolerances, and warp-up of the MEMS switches and their dc bias lines. However, because our objective here is to demonstrate that Nb is not affected by our MEMS fabrication process, the focus is not on the filter itself.

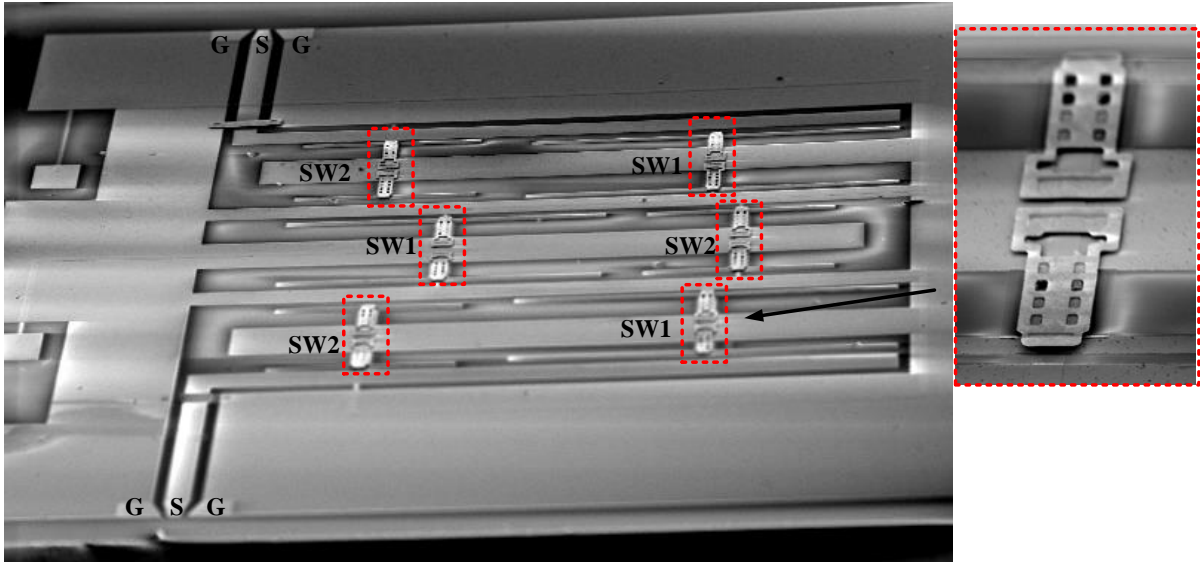


Fig. 6.21. SEM image of the fabricated Nb-based 3-pole tunable BPF.

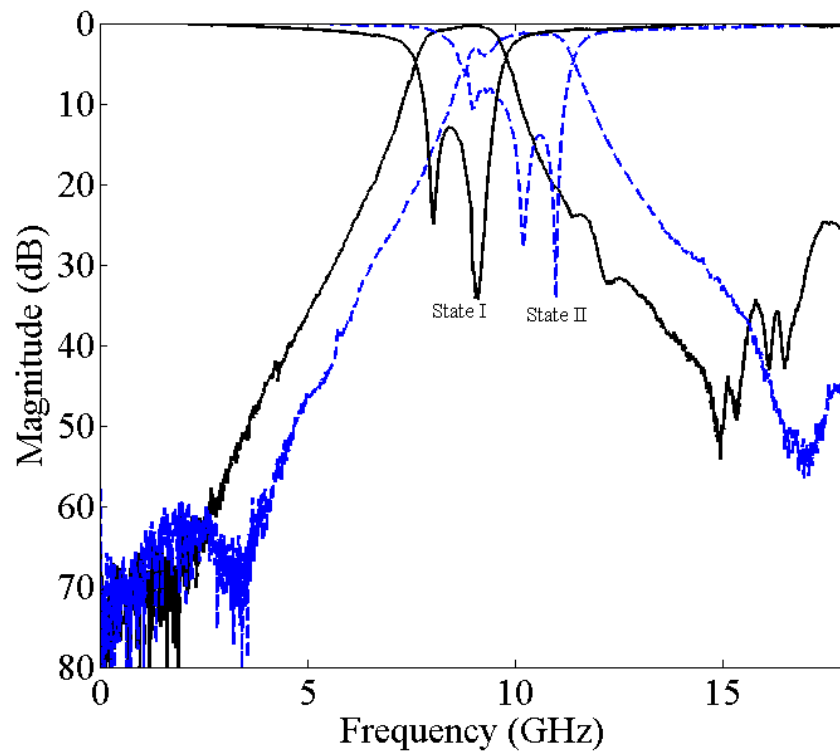


Fig. 6.22. Measured results of State I and State II of the Nb-based tunable BPF at cryogenic temperature.

Another tunable 3-pole planar BPF is designed by integrating dc-contact RF MEMS switches with the filter resonators. The centre frequency of the filter shifts down from 10 GHz to 9 GHz by changing the states of the RF MEMS switches.

Fig. 6.24 shows a 2D and 3D model of the filter, which is integrated with nine dc-contact RF MEMS switches. By changing the length of each resonator and the location where the shorted end of the resonator connects to the ground, both the resonant frequency and the coupling can be controlled for each resonator. To keep the absolute bandwidth constant at both states, the length of the transmission line and position of the input tap are controlled by the positions of the switch at the open end and the two switches at the shorted end of the resonator. The inter-resonator coupling can also be controlled in both states by moving the resonators laterally, as it is not possible to change the gap between the resonators for the two different states. The lateral change can be accomplished by appropriately adjusting the position of the two switches that connect the shorted end of the resonator to the ground. For the lower state to be ‘on’, the three switches near the open end of the resonators are in the down position, and the six switches near the shorted ends of the resonators are in the up position. The opposite is true (in terms of the states of the switches) for the higher state to be ‘on’ [47].

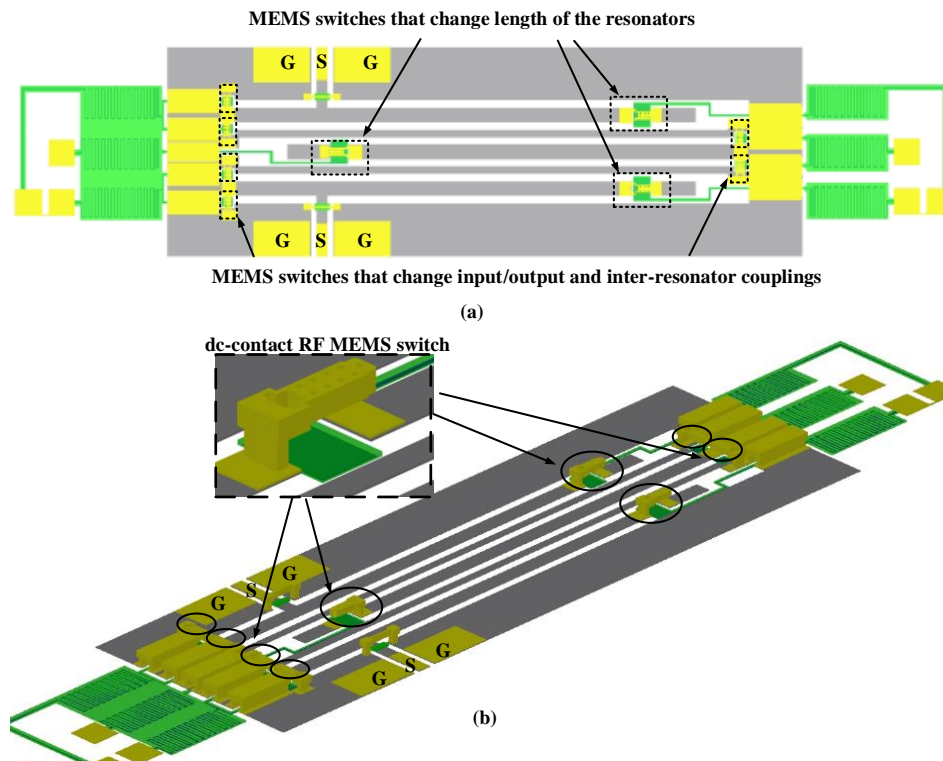


Fig. 6.23. 2D and 3D model of the tunable BPF, which is magnified 20 times in the Z direction: (a) specifies MEMS switches used for input/output and inter-resonator couplings; (b) shows locations of the MEMS switches.

The filter is simulated in Sonnet [48]. Fig. 6.25 shows the EM simulation results of the lossless filter in the ‘on’ and ‘off’ states of the switches. The simulation results show an insertion loss of almost zero and a return loss of better than 15 dB for both states. The first version of the tunable BPF is fabricated with gold only. Fig. 6.26 shows the SEM image of one of the gold-based dc-contact RF MEMS switches, and Fig. 6.27 illustrates the measured results of the gold-based tunable BPF. The insertion loss of the gold-based tunable filter is about 5.5 dB, while the actuation voltage of the RF MEMS switches at room temperature is around 32 V.

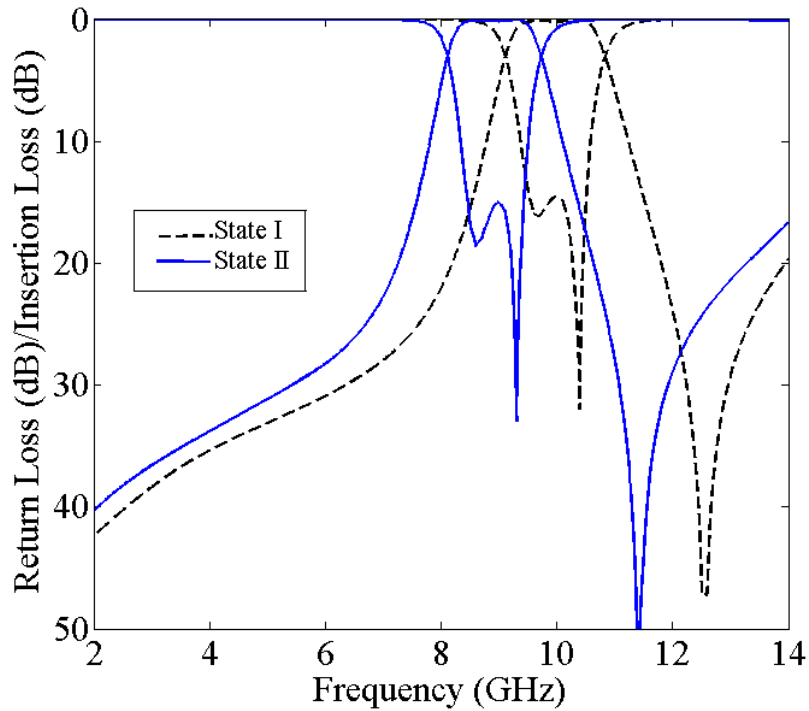


Fig. 6.24. Simulation results of the fabricated Nb-based 3-pole tunable BPF at cryogenic temperature.



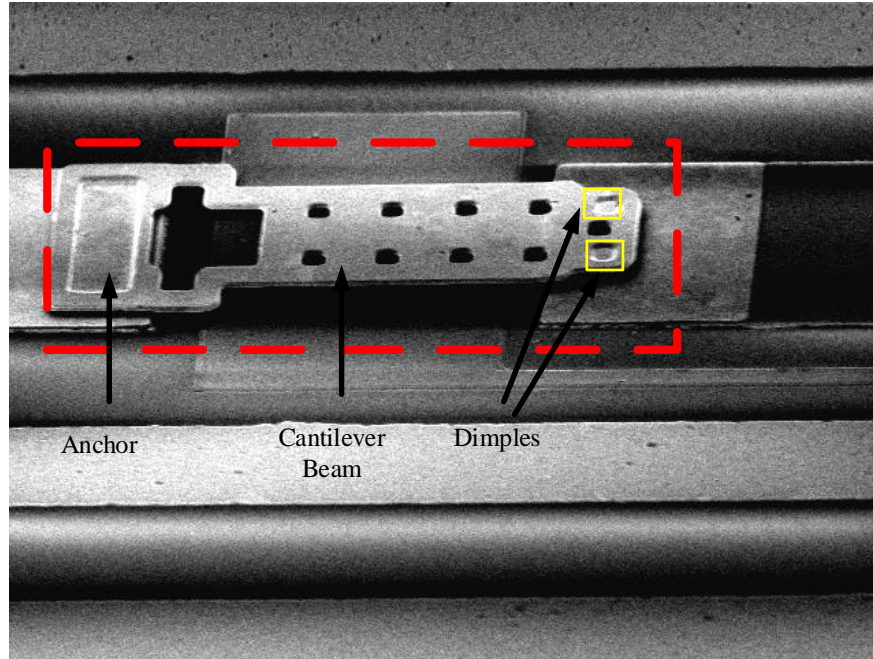


Fig. 6.25. SEM image of one of the dc-contact RF MEMS switches integrated with the BPF as a tunable element.

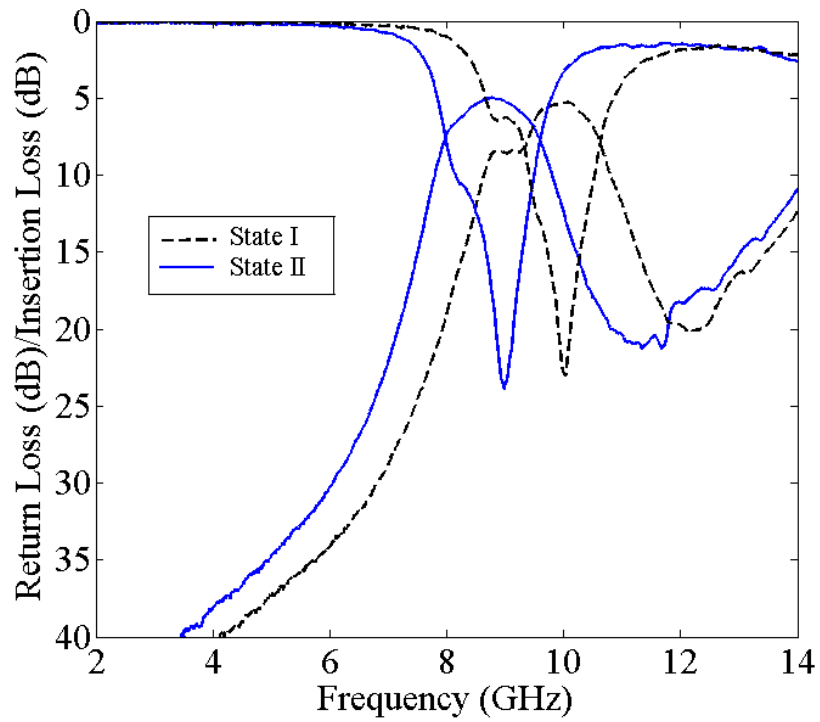


Fig. 6.26. Measurement results of the fabricated gold-based tunable BPF at room temperature.

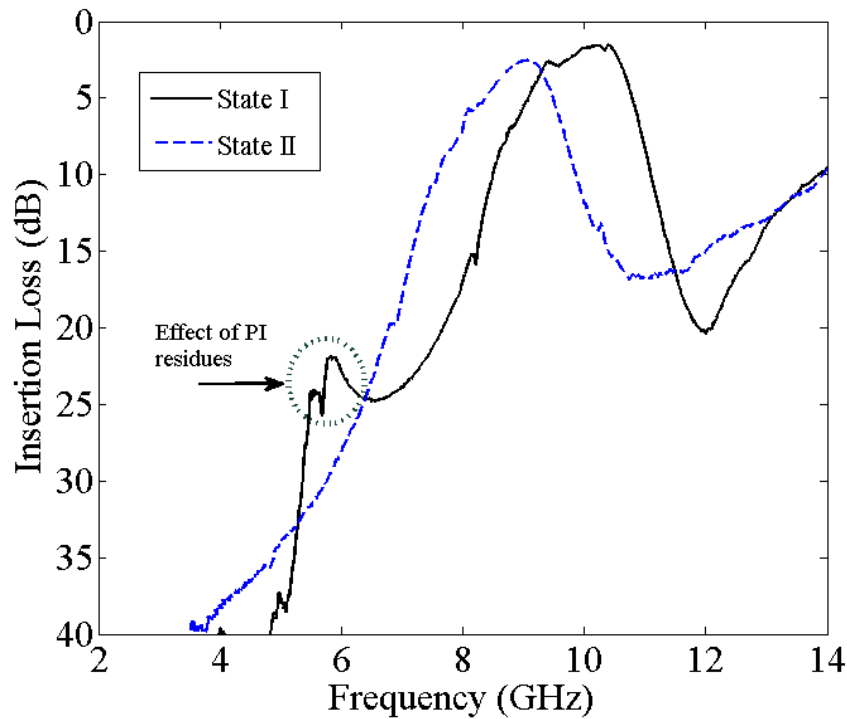


Fig. 6.27. Measurement results of the Nb-based tunable BPF at cryogenic temperature.

Fig. 6.28 shows the measurement results of the tunable version of the superconducting BPF at cryogenic temperatures. The insertion loss is improved more than 4 dB compared to the gold-based tunable version of the BPF.

The discrepancy between the simulation (Fig. 6.25) and measured results (Fig. 6.28) is due to the air bridges on the ground plane. Because no release hole is introduced into the bridges where the dc-bias lines are crossing, the PI underneath the bridge is not completely removed after the release process, and the remaining PI adds some capacitance to the circuit. A spike is evident in the isolation of State I around 6 GHz, which is also due to a lack of release holes on the bridges of the ground planes. Fig. 6.29 presents an SEM image of part of the tunable filter that shows the bridges without any release holes. Fig. 6.30 shows the simulation results of State I of the filter with and without the effect of the PI residues underneath the bridges, which proves the hypothesis. The actuation voltage of the switch is increased to 48 V at cryogenic temperature.

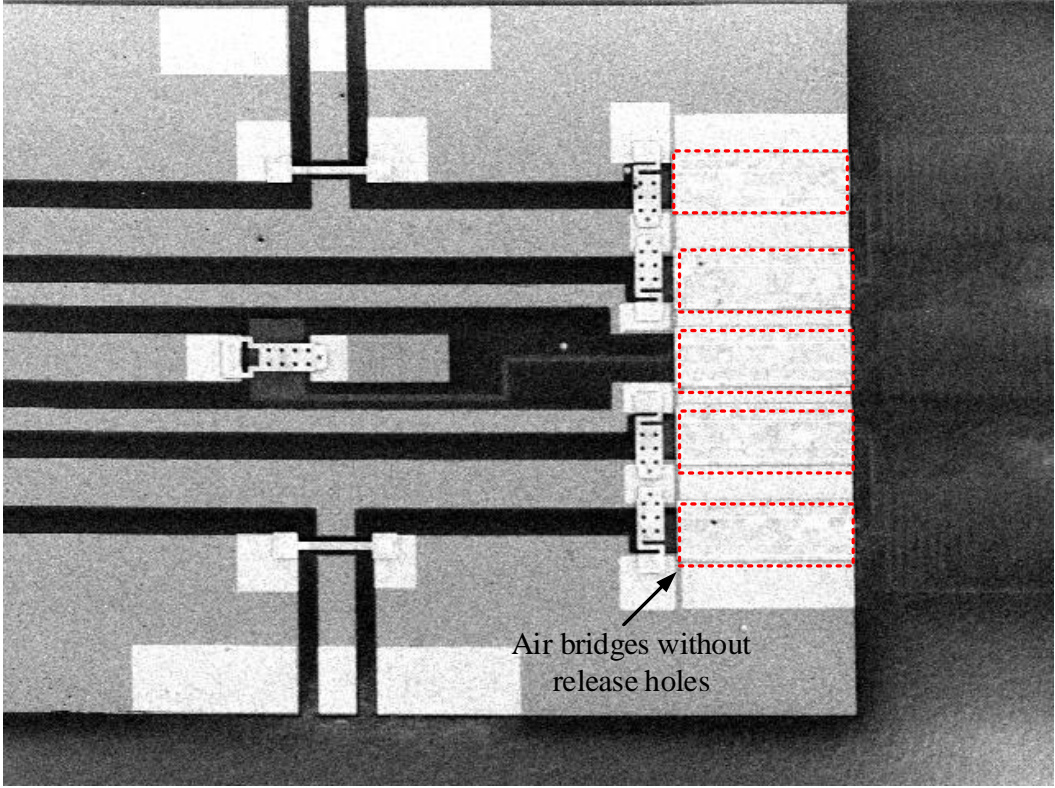


Fig. 6.28. SEM image of part of the Nb-based tunable BPF that shows the air bridges without release holes.

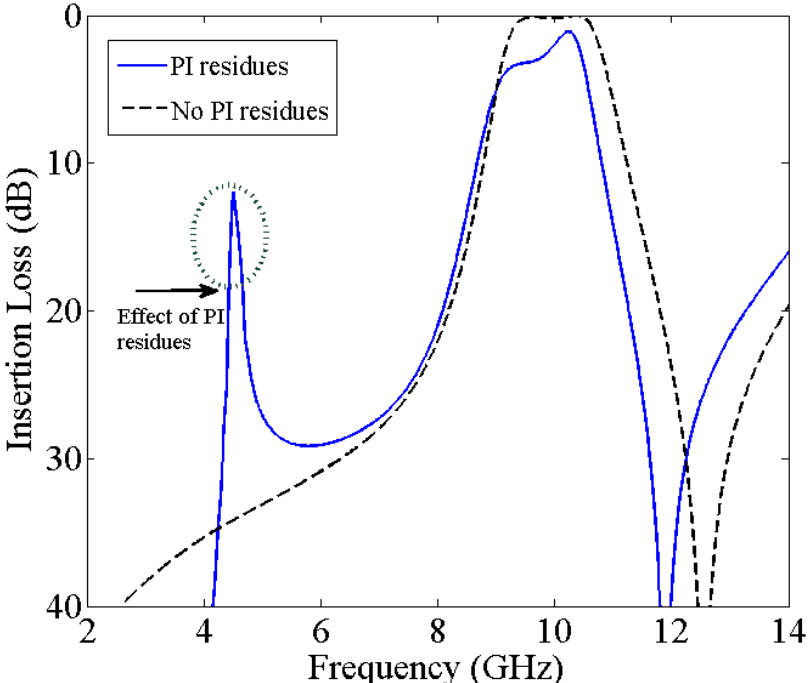


Fig. 6.29. Simulation results for State I of the Nb-based tunable BPF with and without PI residues under the bridges.

In summary, Chapter 6 presented an 8-mask niobium-based superconducting micro-fabrication process that enables the integration of gold-based RF MEMS devices with superconducting RF circuits. Several dc-contact and capacitive-contact RF MEMS switches were designed, fabricated and characterized, showing significant improvement in the insertion loss of the switch due to the superconducting RF circuit.

A capacitor bank was presented showing nine different states of capacitor values varying from 0.22 pF to 5.25 pF. A comparison between the loss of the capacitor at room and at cryogenic temperatures indicated significant improvement of the Q.

Two types of gold-based 3-pole tunable BPFs were also fabricated and measured at room and cryogenic temperatures using dc-contact RF MEMS devices as tunable elements. The RF performance was improved significantly in comparing the gold versions of the filters to the superconducting versions. Additional improvements in insertion loss can be achieved by operating the RF probe-station at lower temperatures.

It should be noted that the main objective of the 8-mask process is to demonstrate the feasibility of integrating gold-based MEMS with an Nb circuit while maintaining the superconducting characteristics of Nb. Better RF performance can be obtained through optimizing the filter design by considering radiation, bias lines coupling effects, and the kinetic inductance of Nb thin film.

# Chapter 7 Conclusions

The main focus of this thesis was on the development of low-temperature superconducting tunable RF devices using MEMS technology. A post-processing technique was developed for the integration of SME technology with MEMS technology that allows for the implementation of varactors and switches using commercially available standard SME fabrication technology offered by Hypres. An 8-mask micro-fabrication process was also developed in the CIRFE lab that integrates superconducting Nb-based RF circuits with gold-based MEMS technology. The major contributions of the research are summarized below. Some of the research problems and issues that can be addressed as future work are also listed in this chapter.

## 7.1 Contributions

The major contributions of this thesis are outlined as follows:

- Investigating the RF and mechanical performance of a MEMS device in a cryogenic environment is critical. The first part of this thesis was dedicated to the characterization of more than 50 gold-based RF MEMS capacitive switches, fabricated in the CIRFE lab at the University of Waterloo at liquid nitrogen temperature. Each of these switches had a different type of mechanical support. The analysis showed that the design of the mechanical supports had a significant impact on the pull-in voltage of the switch at cryogenic temperature. Specifically, the pull-in voltage for beams with rigid supports decreases at cryogenic temperature compared to room temperature, while it increases for beams with flexible supports. The characteristics of silicon and alumina substrates at cryogenic temperatures were investigated. A detailed analysis of the heat loads involved in testing RF devices at cryogenic probe stations was also carried out.
- The Hypres foundry offers a Nb-based multi-layer fabrication process. Hypres has successfully designed, fabricated and tested a complete RF digital receiver. A new SME-MEMS

processing and integration technique has been developed at the Centre for Integrated RF Engineering (CIRFE) at the University of Waterloo that allows, for the first time, the integration of tunable or reconfigurable RF MEMS devices with SME technology. The MEMS structures are formed out of the available metal layers and released by removing one or more dielectric layers as the sacrificial layers. The design and fabrication of several Nb-based RF MEMS switches and varactors were introduced in this thesis. By implementing the RF MEMS switches and varactors, several reconfigurable RF devices were designed and characterized, including tunable resonators, tunable filters, capacitor banks, and SPDT switches.

- A novel 8-mask micro-fabrication process was developed in the CIRFE lab for the fabrication of integrated niobium-based RF circuits with gold-based MEMS devices. The process benefits from the low-loss performance of the niobium RF circuits while having the flexibility to utilize well-known characteristics of gold-based MEMS structures. Some processing challenges and issues regarding the stiffness of MEMS structures at an extremely low temperature were addressed and circumvented, and several superconducting RF MEMS devices that are fabricated using the newly developed micro-fabrication process were demonstrated.

In summary, this thesis has demonstrated the world's first Nb-based superconducting RF MEMS switches and variable capacitors [12, 25, 33, 39, 41, 47]. By comparing the loss of superconducting RF MEMS switches with commercially available RF MEMS switches (e.g., Radant and Leti), we saw that almost all of the Radant switches failed at 4K but that some Leti switches survived at cryogenic temperature. However, the insertion loss of a Leti switch at 4K is 0.6 dB at 10 GHz, whereas it was better than 0.2 dB for the superconducting RF MEMS switch.

The Q of the superconducting varactors was very high, while the quality factor of the high-Q MACOM semiconductor-based varactor showed only slight improvement when the temperature changed from 293K to 4K. It should also be mentioned that many semiconductor varactors did not survive these low temperatures and failed at 4K.

## **7.2 Future Work**

This thesis has carried out extensive research and investigations into a wide range of topics, aiming to advance the development of superconducting RF MEMS devices and integration with SME technology. There are several related research problems in this area that could potentially be explored in the future. Below is a small sample of them.

- An investigation of the proposed SME-based RF MEMS devices is required in terms of switching time, life-time and reliability characterizations, all of which play an important role in the manufacturing and commercialization of the proposed processing and fabricated devices.
- The newly developed 6-metal-layer Hypres process can be used to build MEMS switches employing the available thick gold metal layer to increase the stiffness and life-time of the MEMS structures. Two types of contacts can be developed for a dc-contact RF MEMS switch using the Hypres process: Nb-to-Nb contact, and Nb-to-Au contact. These two contact types could be further investigated in terms of contact resistance and contact reliability, as well as for comparisons of switching time and total loss of the system.
- The preliminary steps of a new post-processing technique similar to [47] were developed and many MEMS test structures were successfully released. Nevertheless, more comprehensive research and experimentation is required to develop reliable MEMS structures based on SME technology using the new post-processing method.
- Future research and experimentation could also focus on the switching time and life-time of the MEMS devices fabricated employing the novel 8-mask Nb-based fabrication process at room and cryogenic temperatures. The contact resistance of the dc-contact RF MEMS switches could be monitored as the temperature decreases from room to 4K. As well, additional investigation is required into the mechanical characteristics of Nb and gold thin films at 4K.
- Ultimately, numerous types of devices can be designed and fabricated implementing the newly developed 8-mask superconducting fabrication process, including impedance matching networks, SPMT switches, and switch matrices. All of these devices show significant improvement in terms of insertion loss.

# Appendix A

## Post-Processing Technique 2

This section provides a description of the preliminary work done on the second post-processing technique to release MEMS structures that have been fabricated by employing the Hypres fabrication process.

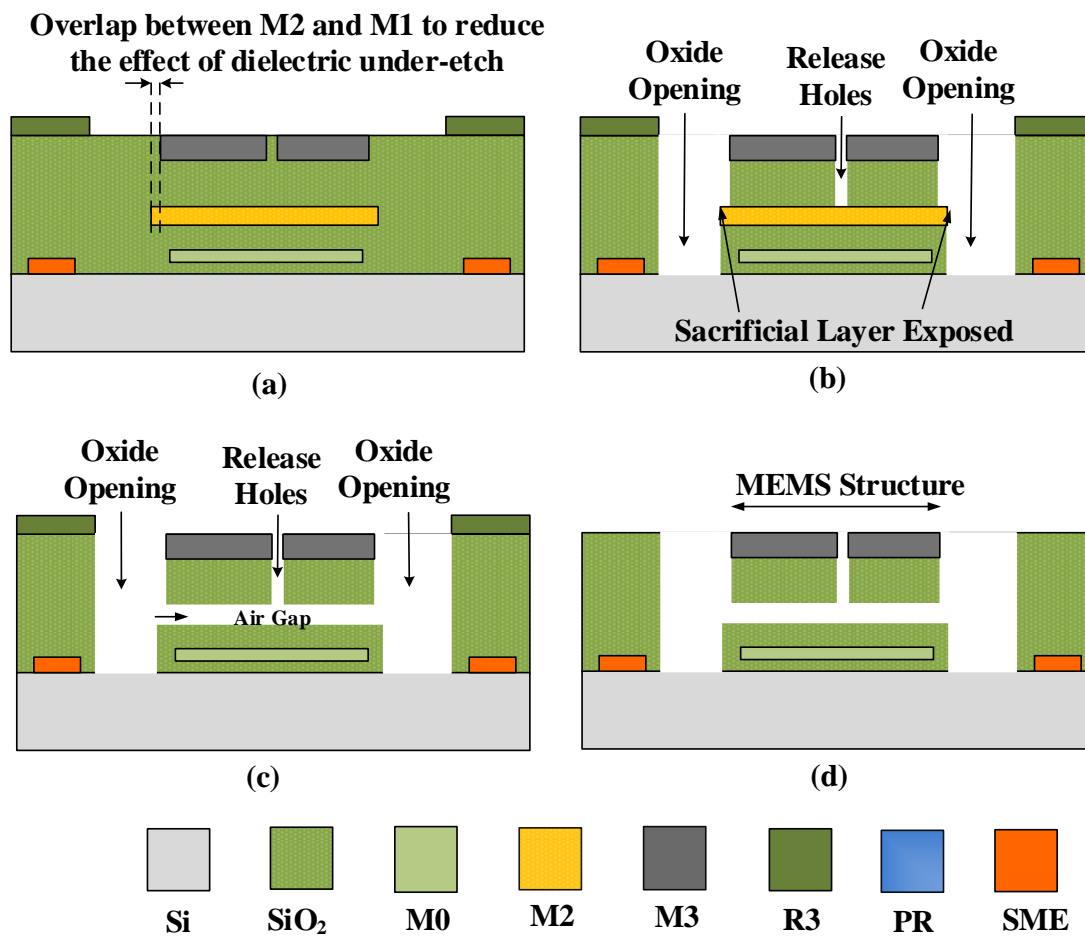


Fig. A. 1. Steps of the post-processing technique 2 to release MEMS devices fabricated using Hypres foundry.



Table A. 1. RIE recipe to etch SiO<sub>2</sub>.

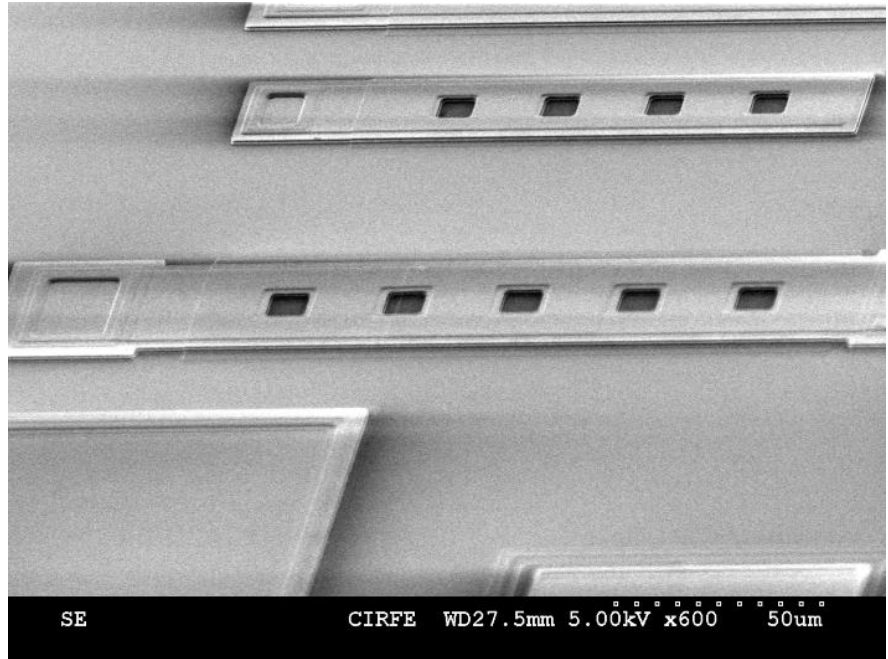
| <b>CHF<sub>3</sub></b> | <b>ICP (watts)</b> | <b>RIE (watts)</b> | <b>Pressure (mT)</b> |
|------------------------|--------------------|--------------------|----------------------|
| 50                     | 200                | 52                 | 20                   |

The second proposed post-processing technique is based on selecting and removing one of the metal layers as the sacrificial layer. A similar post-processing technique is implemented in CMOS technology in [50]. Fig. A.1 depicts the steps of the release procedure. The first step, after the removal of the top PR, is to etch the surrounding silicon dioxide layer around the MEMS device. R3 is used as the mask for the anisotropically reactive ion etching of the oxide, M3 is used for the movable plate, and M0 is used to build the RF circuit. Similar steps used in [50] are applied in this process. However, it should be mentioned here that a completely different process needs to be developed, since the metal layers in this case are Nb, while for CMOS they are aluminum.

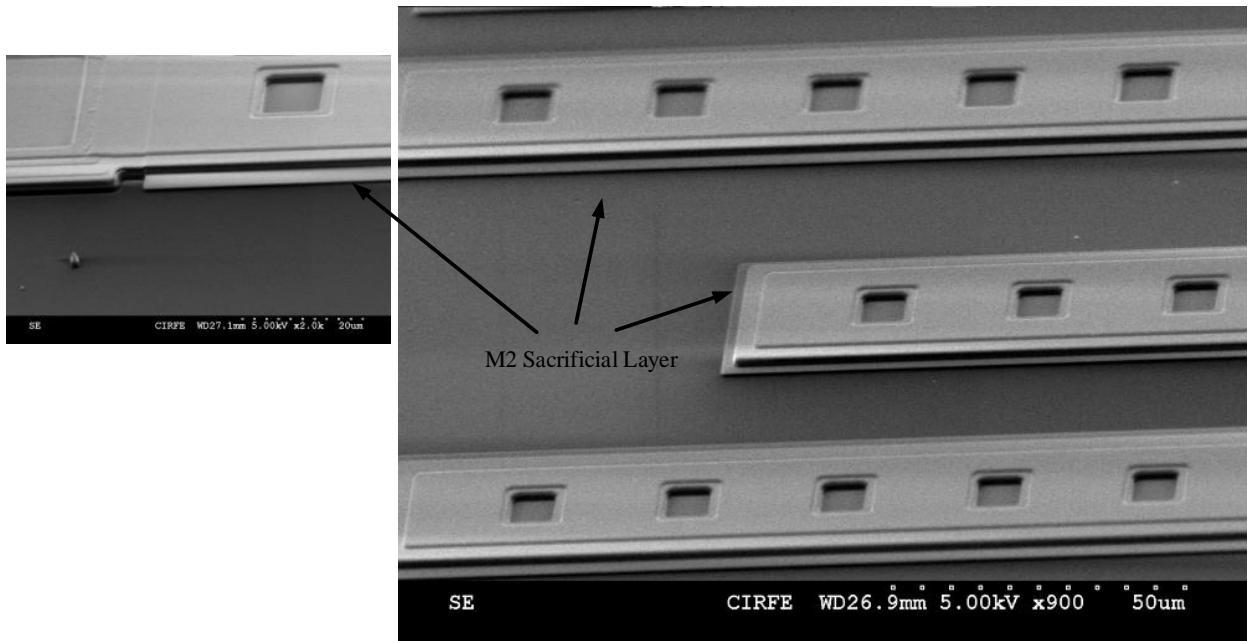
Table A.1 indicates the recipe to etch SiO<sub>2</sub>. Fig. A.2 shows the exposure of the M2 metal layer after 67 minutes of etching the oxide layer. The thickness of the oxide is approximately 0.85 μm. The etch rate of the SiO<sub>2</sub> using this recipe is about 0.209 A/sec.

The second step is to isotropically etch the M2 sacrificial layer. Potassium Hydroxide (KOH) can be used to isotropically etch the M2 Nb layer. To increase the etch rate of Nb by KOH, the wet etchant should be heated. Numerous experiments have been done regarding the temperature of the wet etchant and the release time. Fig. A.3 and Fig. A.4 show SEM images of a sample after 2 minutes in a 85°C KOH. M2 is completely removed in KOH after 25 minutes, at a temperature of 70 °C. Fig. A.4 shows a photograph of a few test structures that indicate the release of the MEMS structures.

There is no data available regarding the etch rate of Nb in warm KOH. Note that the sacrificial layer (M2) should be extended so that the wet etchant can attack this layer. After the wet release, the gold layer is also etched away. This step should be carried out with great precision, since the device is released. The final step is to dry the chip in the Critical Point Dryer system. Additional research and investigation are required to fine-tune all of the steps of the post-processing technique 2.

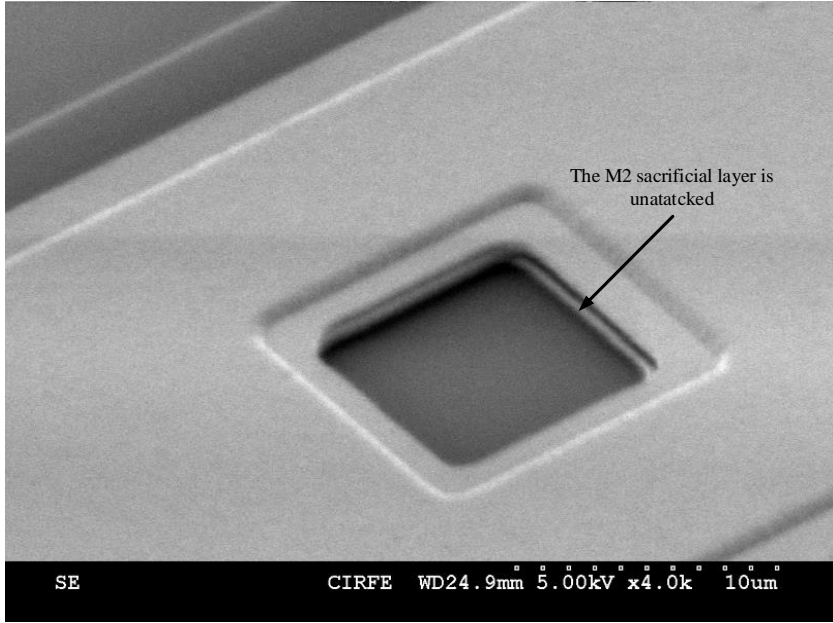


(a) Before etching SiO<sub>2</sub> layer and exposing the M2 sacrificial layer.

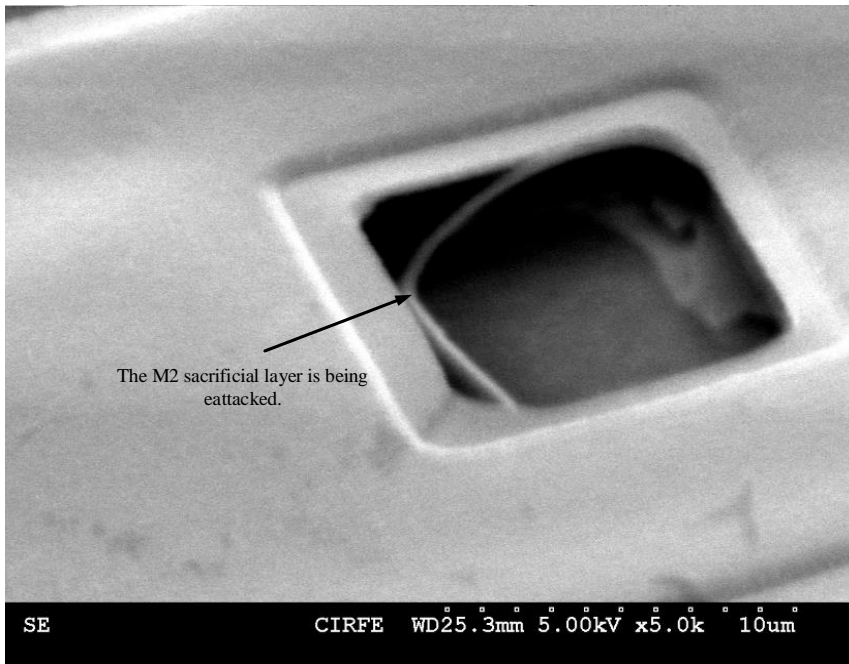


(b) After etching SiO<sub>2</sub> layer. M2 sacrificial layer is exposed.

Fig. A. 2. Exposure of the M2 metal layer after 67 minutes of etching the oxide layer.



(a) Prior to wet etching of the M2 sacrificial layer.



(b) After wet etching of the M2 sacrificial layer in KOH at 85°C for 2 min .

Fig. A. 3. An SEM image of a sample after 2 minutes in a 85°C KOH.

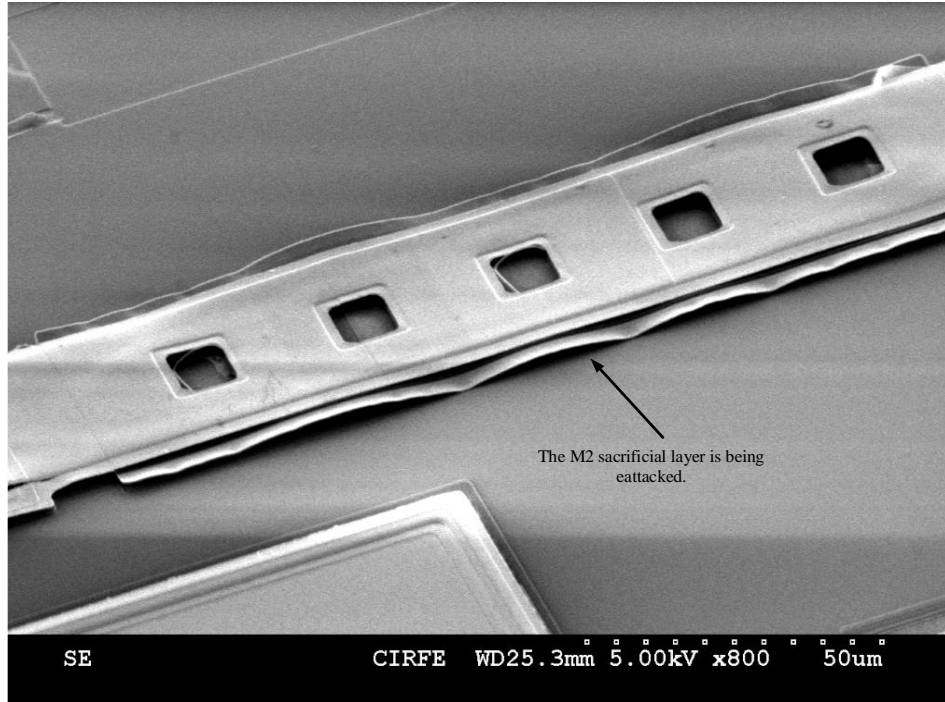
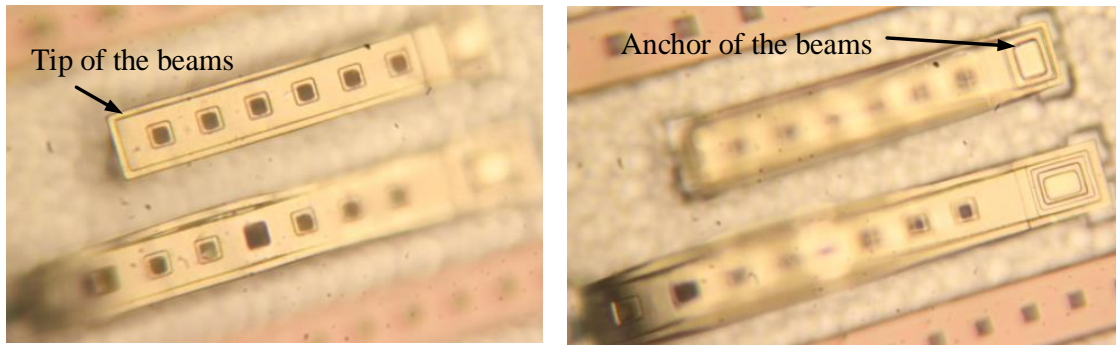


Fig. A. 4. Another SEM image of a sample after 2 minutes in a 85°C KOH.



(a) Focused to the tip of the beams.

(b) Focused to the anchor of the beams.

Fig. A. 5. Photograph of a few test structures indicating that the MEMS structures are released.

# Appendix B

## Nb-Based Fabrication Process

Step-by-step details of the fabrication process of the Nb-based RF circuit integrated with Au-based MEMS structures.

### 1. RCA clean process

- 600 ml DI water, 130 ml Ammonium Hydroxide (27%), 130 ml Hydrogen Peroxide at 70°C for 15 min
- Rinse in DI water
- Dehydration bake at 160°C for 4 min

### 2. Deposit 40 nm TiW for dc bias lines

- Sputter 40 nm TiW layer at 20Å/min

### 3. Pattern TiW layer (using SUSS MJB4 mask aligner)

- AZ3330 Positive Resist (Program S)
- Spin at 100rpm for 10 sec, 500 rpm for 10 sec and 3000 rpm for 30 sec
- Soft bake at 110°C for 60 sec
- Exposure for 4 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 55sec (AZ-MIF 300 developer)
- Hard bake 110 °C for 120 sec

### 4. Etch TiW layer

- Trion recipe – ICP=250 W, RF=100 W, P=250 mT, CF4=30 ccm
- Etch rate of recipe is about 0.4 nm/sec
- Estimated time of etch ~ 100 sec
- Remove PR in Kwik Strip at 65°C for 1 hr and 200 rpm

### 5. Deposit 750 nm PECVD SiO2

- Trion recipe – P=900 mT, RF=60 W, SiH<sub>4</sub>=5 ccm, N<sub>2</sub> = 118 ccm, N<sub>2</sub>O = 140 ccm, time = 400 sec

#### **6. Pattern PECVD SiO<sub>2</sub> layer**

- Adhesion promoter coating at 500 rpm for 15 sec and 4000 rpm for 45 sec
- Soft bake at 90 °C for 120 sec
- AZ3330 Positive Resist (Program S)
- Spin at 100rpm for 10 sec, 500 rpm for 10 sec and 3000 rpm for 30 sec
- Soft bake at 110°C for 60 sec
- Exposure for 4 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 55sec (AZ-MIF 300 developer)
- Hard bake 110 °C for 120 sec

#### **7. Etch PECVD SiO<sub>2</sub> layer**

- Buffered HF (BHF) 6:1 for 5 min and 20 sec without agitation
- Remove PR in Kwik Strip at 65°C for 1 hr and 200 rpm

#### **8. Deposit Nb layer**

- Sputter 300 nm Nb at 161 nm/min (Quantum-Nano-Centre, QNC)

#### **9. Deposit Cr/Au layer**

- E-beam 30 nm Cr layer and 50 nm Au layer

The adhesion of gold to niobium is only good prior to exposing niobium to air. Therefore, there is a need to deposit Cr as the adhesion layer. The in-situ deposition of gold on niobium is not accessible in this case.

#### **10. Pattern Cr/Au layer**

- NLOF2035 Negative Resist
- Spin at 100rpm for 10 sec, 500 rpm for 10 sec and 2500 rpm for 30 sec
- Soft bake at 110°C for 60 sec
- Exposure for 3 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 120 sec (AZ-MIF 300 developer)
- Hard bake 120 °C for 120 sec

### **11. Au electroplating**

- Au electroplating to achieve the thickness of more than 1  $\mu\text{m}$ . This layer of Au is only for probing and adhesion to the second Au layer.

### **12. Cr lift-off**

- E-beam 40 nm Cr layer
- Kwik Strip at 65°C for 40 min and 200 rpm

### **13. Au etch and Cr etch**

- Wet etching for 45 sec with Transene gold etchant
- Cr etching for 20 sec with 40% diluted etchant

### **14. Nb patterning**

- AZ3330 Positive Resist (Program S)
- Spin at 100 rpm for 10 sec, 500 rpm for 10 sec and 3000 rpm for 30 sec
- Soft bake at 110°C for 60 sec
- Exposure for 4 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 55 sec (AZ-MIF 300 developer)
- Hard bake 110 °C for 120 sec

### **15. Nb etch**

- Trion recipe – RF=50 W, P=50 mT, SF6=30 ccm
- Estimated time of etch ~ 550 sec
- Remove PR in Kwik Strip at 65°C for 1 hr and 200 rpm

Nb etch is temperature dependent. The sample has to be in the RIE for at least 200 sec so the above etch rate achieved. There is no sign of Nb etch if the sample is removed from the RIE with a period of less than 200 sec.

### **16. Deposit Cr**

- E-beam 40 nm Cr layer

The adhesion of SiO<sub>2</sub> to Nb is very good. Cr is used to cover Nb, since SiO<sub>2</sub> etching recipe also etches Nb with high etching rate.

### **17. Deposit 750 nm PECVD SiO<sub>2</sub>**

- Trion recipe – P=900 mT, RF=60 W, SiH4=5 ccm, N2 = 118 ccm, N2O = 140 ccm, time = 400 sec

### **18. Pattern PECVD SiO2 layer**

- Adhesion promoter coating at 500 rpm for 15 sec and 4000 rpm for 45 sec
- Soft bake at 90 °C for 120 sec
- AZ3330 Positive Resist (Program S)
- Spin at 100rpm for 10 sec, 500 rpm for 10 sec and 3000 rpm for 30 sec
- Soft bake at 110°C for 60 sec
- Exposure for 4 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 55sec (AZ-MIF 300 developer)
- Hard bake 110 °C for 120 sec

### **19. Etch PECVD SiO2 layer**

- Trion recipe – ICP=250 W, RF=100 W, P=250 mT, CF4=30 ccm
- Etch rate of recipe is about 1 nm/sec
- Estimated time of etch ~ 750 sec

### **20. Cr etch**

- Cr etching for 20 sec with 40% diluted etchant
- Remove PR in Kwik Strip at 65°C for 1 hr and 200 rpm

### **21. PI2562 (Sacrificial layer) spin-on**

- Spin at 100rpm for 10 sec, 500 rpm for 10 sec and 1300 rpm for 40 sec
- Soft bake at 90°C for 120 sec
- Hard bake at 150 °C for 120 sec
- Curing at 160 °C for 2 hrs

Curing PI in furnace at temperatures above 300 °C causes oxidization of Nb. Thus Nb is cured on the hot plate.

### **22. Deposit Aluminum metal mask**

- Sputter 200 nm of Aluminum at 180Å/min

### **23. Pattern Aluminum**



- AZ3330 Positive Resist (Program S)
- Spin at 100rpm for 10 sec, 500 rpm for 10 sec and 3000 rpm for 30 sec
- Soft bake at 110°C for 60 sec
- Exposure for 4 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 55sec (AZ-MIF 300 developer)
- Hard bake 110 °C for 120 sec

#### **24. Etch Aluminum layer for dimple opening**

- Warm up the PAN etch at 40 °C for 3 min

#### **25. Etch PI to create dimples**

- Trion recipe – ICP=50 W, RF=50 W, P=250 mT, O<sub>2</sub>=30 ccm, time=450 sec
- Wash PR with acetone and IPA
- Etch Aluminum in PAN etch

#### **26. Deposit Aluminum metal mask**

- Sputter 200 nm of Aluminum at 180Å/min

#### **27. Pattern Aluminum**

- AZ3330 Positive Resist (Program S)
- Spin at 100rpm for 10 sec, 500 rpm for 10 sec and 3000 rpm for 30 sec
- Soft bake at 110°C for 60 sec
- Exposure for 4 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 55sec (AZ-MIF 300 developer)
- Hard bake 110 °C for 120 sec

#### **28. Etch Aluminum layer for anchor opening**

- Warm up the PAN etch at 40 °C for 1 min

#### **29. Etch PI to create dimples**

- Trion recipe – ICP=100 W, RF=50 W, P=250 mT, O<sub>2</sub>=30 ccm, time=750 sec
- Wash PR with acetone and IPA
- Etch Aluminum in PAN etch

### **30. Deposit Au**

- E-beam 50 nm Au layer

### **31. Pattern Au layer**

- NLOF2035 Negative Resist
- Spin at 100rpm for 10 sec, 500 rpm for 10 sec and 2500 rpm for 30 sec
- Soft bake at 110°C for 60 sec
- Exposure for 3 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 120 sec (AZ-MIF 300 developer)
- Hard bake 120 °C for 120 sec

### **32. Au electroplating**

- Au electroplating to achieve the thickness of about 1.8  $\mu\text{m}$ .

### **33. Cr lift-off**

- E-beam 40 nm Cr layer
- Kwik Strip at 65°C for 40 min and 200 rpm

### **34. Au etch and Cr etch**

- Wet etching for 45 sec with Transene gold etchant
- Cr etching for 20 sec with 40% diluted etchant

### **35. Wet release**

- Wet release in EKC 265 at 60 °C for 15 min
- CPD system to dry the samples

# References

- [1] R. Rafique, T. Ohki, P. Linner, and A.Y. Herr, “Niobium tunable microwave filter,” *IEEE Trans. Microw. Theory Techn.*, vol. 57, No. 5, pp. 1173-1179, May 2009.
- [2] A. Kirichenko, D. Gupta, and S. Sarwana, “RSFQ Asynchronous Switch Matrix,” *IEEE Trans. Appl. Supercond.*, vol. 17, No. 2, pp. 505-508, Jun. 2007.
- [3] D. Gupta, D. E. Kirichenko, V. V. Dotsenko, R. Miller, S. Sarwana, A. Talalaevskii, J. Delmas, R. J. Webber, S. Govorkov, A. F. Kirichenko, I. V. Vernik, and J. Tang, “Modular Multi-function Digital-RF Receiver Systems,” *IEEE Trans. Appl. Supercond.*, vol. 21, No. 3, pp. 883-890, Jun. 2011.
- [4] [www.hypres.com](http://www.hypres.com)
- [5] M. J. Lancaster, *Passive Microwave Device Applications of High Temperature Superconductors*; Cambridge University Press, 1997.
- [6] G. M. Rebeiz, *RF MEMS: Theory, design and technology*, Wiley, 2003.
- [7] D. A. Cardwell, D. S. Ginley, *Handbook of Superconducting Materials, Volume 2*, IOP Publishing Ltd., 2003.
- [8] M. Schickes, K. F. Schuster, “Integrated of Niobium Thin Film Air Bridges as Variable Capacitors for Superconducting GHz Electronic Circuits,” *IEEE Trans. Appl. Supercond.*, vol. 13, No. 2, pp. 135-137, Jun. 2003.
- [9] M. Schickes, A. Navarrini, “Niobium SupraMEMS for reconfigurable millimeter wave filters,” *IEEE Trans. Appl. Supercond.*, vol. 17, No. 2, pp. 910-913, Jun. 2007.
- [10] J. Noel, A. Bogozi, Y. Vlasov, G. Larkins, “Cryogenic pull-down voltage of microelectromechanical switches,” *Journal of Microelectromechanical Systems*, vol. 17, No. 2, pp. 351-355, 2008.
- [11] C. Goldsmith, D. Forehand, “Temperature variation of actuation voltage in capacitive MEMS switches,” *IEEE Microwave and Wireless Component Letters*, vol. 15, No. 10, pp.718-720, 2005.
- [12] S. S. Attar, S. Setoodeh, R. Al-Dahleh, and R. R. Mansour, “Cryogenic performance of gold-based and niobium-based RF MEMS devices,” *Microwave Integrated Circuits Conference (EuMIC), 2011 European*, pp. 672-675, Oct. 2011.

- [13]. R. Al Dahleh, *Integrated MEMS Based Phase Shifters*, PhD Dissertation, University of Waterloo, 2008.
- [14] W. Fang, J. A. Wickert, “Determining mean and gradient residual stresses in thin films using micromachined cantilevers,” *Journal of Micromech. Microeng*, vol. 6, pp. 301-309, 1996.
- [15] [www.comsol.com](http://www.comsol.com)
- [16] A. M. Collard, *High temperature elastic constant of gold single crystals*, PhD Dissertation, Rice University, 1991.
- [17] [www.lakeshore.com](http://www.lakeshore.com)
- [18] [www.cmr-direct.com](http://www.cmr-direct.com)
- [19] S. Setoodeh, *Superconducting Microwave Filters*, MSc Thesis, University of Waterloo, 2011.
- [20] [www.2spi.com](http://www.2spi.com)
- [21] [www.ggb.com](http://www.ggb.com)
- [22] J. Krupka, J. Breeze, A. Centeno, N. Alford, T. Claussen, and L. Jensen, “Measurements of permittivity, dielectric loss tangent, and resistivity of float-zone silicon at microwave frequencies,” *IEEE Trans. Microw. Theory Techn.*, vol. 54, No. 11, pp. 3995-4001, Nov. 2006.
- [23] [www.home.agilent.com](http://www.home.agilent.com)
- [24] J. Rosa, D. Gupta, W. Littlefield, “SATCOM on the Move (SOTM) using superconductor microelectronics – a quantum leap in performance,” *IEEE/Sranoff Symposium on Advances in Wired and Wireless Communication*, pp.95-98, 2004.
- [25] S. S. Attar, S. Setoodeh, R. R. Mansour, D. Gupta, “Low Temperature Superconducting DC-Contact RF MEMS Switch for Cryogenic Reconfigurable RF Front-Ends”, *IEEE Trans. Microw. Theory Techn.*, vol. 62, No. 7, pp. 1437-1447, Jul. 2014
- [26] S. D. Senturia, *Microsystem Design*, Springer, 2000.
- [27] C. K. Gupta, A.K. Suri, *Extractive Metallurgy of Niobium*, CRC Press, 1993.
- [29] K. U. Chan, M. Daneshmand, R. R. Mansour, and R. Ramer, “Scalable RF MEMS switch matrices: methodology and design,” *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 6, pp. 1612-1621, Jun. 2009.
- [30] G. M. Rebiez, and J. B. Muldavin, “RF MEMS switches and switch circuits,” *IEEE Microwave Magazine*, pp. 59-71, Dec. 2001.

- [31] C. Goldsmith, D. Forehand, "Temperature variation of actuation voltage in capacitive MEMS switches," *IEEE Microwave and Wireless Component Letters*, vol 15, No. 10, pp.718-720, Oct. 2005.
- [32] G. Songbin, T. Reck and N. S. Barker, "A temperature insensitive DC-contact RF-MEMS switch," *Microwave Integrated Circuits Conference (EuMIC), 2010 European*, pp.1114-1117, Sep. 2010.
- [33] S. S. Attar, S. Setoodeh, R. R. Manosur, and D. Gupta, "Low temperature superconducting DC-contact RF MEMS switch for superconducting tunable resonators," *IEEE MTTs Int. Microwave Symp.* Jun. 2012.
- [34] A. Broune, J. Dhennin, P. Charvet, P. Pons, N. B. Jemma, P. Heeb, F. Coccetti, and R. Plana, "Multi-physical characterization of micro-contact material for MEMS switches," *56<sup>th</sup> IEEE Holm Conference on Electrical Contacts*, pp.1-10, Oct. 2010
- [35] [www.ansys.com](http://www.ansys.com)
- [36] S. Gong, H. Shen, and N. S. Barker, "Study of broadband cryogenic DC-contact RF MEMS switches," *2009 IEEE Trans. Microw. Theory Techn.*, vol 57, pp. 3442-3449, Dec. 2009.
- [37] [www.coventor.com](http://www.coventor.com)
- [38] A. Bogozi, A. V. Datye, M. Brzhezinskaya, Y. S. Hijazi, J. Martinez, J. Noel, K. H. Wu, Y. A. Vlasov, and G. L. Larkins, Jr. "Elastic modulus study of gold thin film for use as an actuated membrane in a superconducting RF MEMS switch," *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 980-983, Jun. 2005.
- [39] S. S. Attar, S. Setoodeh, P. Laforge, M. Bakri-Kassem, R. R. Mansour, "Low Temperature Superconducting Tunable Bandstop Resonator and Filter", *IEEE Trans. Appl. Supercond.*, vol. 24, No. 4, Aug. 2014..
- [40] [www.macomtech.com](http://www.macomtech.com)
- [41] S. S. Attar, R. R. Mansour, "Low Temperature Superconducting RF MEMS Devices", *IEEE Trans. Appl. Supercond.*, vol. 23, no.3, Jun. 2013.
- [42] K. Y. Chan, S. Fouladi, R. Ramer, and R. R. Mansour, "RF MEMS switchable interdigital bandpass filter," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 1, pp.44-46, Jan. 2012.

- [43] N. Zahirovic, S. Fouladi, R. R. Mansour, and Ming Yu, "Tunable suspended substrate stripline filters with constant bandwidth," *2011 IEEE MTT-S Int. Microwave Symp.*, pp. 1-4, Jun. 2011.
- [44] K. Entesari, K. Obeidat, A. R. Brown, and G. M. Rebeiz, "A 25-75 MHz RF MEMS tunable filter," *IEEE Trans. Microw. Theory Techn.*, vol. 55, No. 11, pp. 2399-2405, Nov. 2007.
- [45] E. M. Prophet, J. Musolf, F. Betty, and S. Jimenez, "Highly-selective electronically-tunable cryogenic filter using monolithic, discretely-switchable MEMS capacitor arrays," *IEEE Trans. Appl. Supercond.*, pp. 956-959, Jun. 2005.
- [46] UW MEMS Handbook. Waterloo, ON, Canada: Centre for Integr. RF Eng. (CIRFE), Univ. Waterloo, 2010. [Online]. Available: <http://cirfe.uwaterloo.ca/>
- [47] S. S. Attar, P. Laforge and R. R. Mansour, "A Novel Micro-Fabrication Process for Integration of Superconductor Niobium-Based RF Circuits with Gold-Based RF MEMS Devices", *44<sup>th</sup> European Microwave Conference (EuMW)*, 2014, *submitted*.
- [48] S. S. Attar and R. R. Mansour, "Integration of Niobium Low Temperature Superconducting RF Circuits with Gold-Based RF MEMS Switches", *IEEE Trans. Appl. Supercond.*, *submitted*.
- [49]. [www.sonnetsoftware.com](http://www.sonnetsoftware.com)
- [50] S. Fouladi, *Reconfigurable Impedance Matching Networks based on RF-MEMS and CMOS-MEMS Technologies*, PhD dissertation, University of Waterloo, 2010.
- [51] S. S. Attar, S. Setoodeh, R. R. Mansour, "Low Temperature Superconductive Bandreject Resonator and Filters", *2010 IEEE MTT-S Int. Microwave Symp.*, 2010, pp.1376-1379.
- [52] [www.radantmems.com](http://www.radantmems.com)
- [53] [www.components.omron.com](http://www.components.omron.com)