Heterojunction Photovoltaic Devices With Rapid Thermally Annealed Crystalline Thin Films

by

Christopher Baldus-Jeursen

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

Abstract

Rapid thermal annealing (RTA) is a low thermal budget high throughput method of crystallizing hydrogenated amorphous (a-Si:H) silicon films. This thesis had three principal goals: 1) to fabricate heterojunction solar cells by PECVD deposition of n-type a-Si:H without using an intrinsic a-Si:H buffer layer, 2) to use low thermal budget RTA to form highly crystalline emitters with sufficient lateral conductivity to eliminate the transparent conducting oxide, and 3) to investigate alternative heterojunction interface passivation layers such as silicon nitride which are suitable for high temperature processing. Thin a-Si:H films deposited on silicon wafer substrates were annealed by RTA at temperatures from 500^oC to 1000^oC. The crystalline emitter layers were characterized by transmission electron microscopy, Raman, UV-reflectance, ellipsometry, and scanning electron microscopy. Electrical characterization was performed by Hall Effect and temperature dependent current-voltage measurements. The RTA crystallization process was epitaxial, but the resulting films had a large enough defect density that their UV-reflectance and ellipsometry dielectric function curves were very similar to those of nanocrystalline silicon. However, as the RTA temperature was increased the quality of the epitaxial films greatly improved approaching that of bulk crystalline silicon. Preliminary simulations were performed approximating the epitaxial films as nanocrystalline material, and comparison was made with defect-free epitaxial and a-Si:H /c-Si heterojunction cells. Basic solar cells were fabricated on polished silicon wafers. Cells were analyzed by dark current-voltage, external and internal quantum efficiency, solar simulator, and spreading resistance profiling. Phosphorous diffusion at RTA temperatures above 750^oC reduced cell photocurrent. A cell efficiency of 15.1 % on a 1 cm^2 sample was achieved for RTA at 750^oC for 5 minutes. The principal factor limiting the open-circuit voltage of the cells was recombination in the quasi-neutral region of the silicon wafer. Experimental results showed that the recombination velocity at the heterojunction interface was low (between 10 cm/s to 100 cm/s). Advanced simulations focused on quantifying the defect density at the heterojunction interface by capacitance spectroscopy and electroluminescence. Advanced cell architectures were also studied, and several additional processing steps were implemented. Wafers were thinned to reduce recombination losses in the absorber, and pyramid textured to decrease reflectance. A thin passivating layer of silicon nitride was introduced between the emitter and the substrate. A nanocrystalline p$^+$ layer was deposited on the back side to reduce back surface recombination. Although the wide band gap of silicon nitride appeared to hinder charge carrier transport, a preliminary cell efficiency of 11.5% was achieved at an annealing time of 20 minutes at 1000^oC.

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III. List of Acronyms

a-Si:H	Amorphous silicon diluted with hydrogen
EQE	External quantum efficiency [%]
FTIR	Fourier transform infrared spectroscopy
HIT	Heterojunction with intrinsic thin layer
IQE	Internal quantum efficiency [%]
MTCE	Multi-tunneling capture and emission
OPE-A	Organic peracetic acid etch (recipe A)
PECVD	Plasma enhanced chemical vapour deposition
RNG	Random nucleation and grain growth
RTA	Rapid thermal annealing
SEM	Scanning electron microscopy
SPE	Solid phase epitaxy
TCO	Transparent conducting oxide
TEM	Transmission electron microscopy
UV	Ultraviolet
XRD	X-ray diffraction

IV.   List of Symbols

A	Device area [cm^2]
A_a	Absorptivity
b	Distance between front and back contacts [cm]
C_D	Depletion capacitance [F]
C_{DF}	Diffusion capacitance [F]
C_{LFP}	Low frequency plateau capacitance [F]
c_n	Electron capture cross section [cm^{-2}]
C_n	Capacitance on the n-side [F]
c_p	Hole capture cross section [cm^{-2}]
C_p	Capacitance on the p-side [F]
C_s	Dopant surface concentration [cm^{-2}]
D	Diffusion coefficient for phosphorus [cm^2/s]
D_{it}	Density of defect states at the heterojunction interface [cm^{-3}]
D_n	Electron diffusion coefficient [cm^2/s]
D_p	Hole diffusion coefficient [cm^2/s]
E	Energetic distribution of states throughout the bandgap [eV]
E_a	Potential barrier height due to grain boundary [eV]
E_A	Activation energy [eV]
E_{ACPG}	Acceptor Gaussian peak energy [eV]
E_C	Conduction band energy [eV]
E_{DA}	Switchover energy [eV]
E_{DONG}	Donor Gaussian peak energy [eV]
E_e	Demarcation energy [eV]
E_f	Fermi level [eV]
E_{Fn}	Quasi-Fermi level of conduction band electrons [eV]
E_{Fp}	Quasi-Fermi level of valence band holes [eV]
E_g	Semiconductor bandgap [eV]
E_{inc}	Random nucleation and grain growth nucleation activation energy [eV]
E_{na}	Trap activation energy [eV]
E_o	Activation energy between amorphous and crystalline state [eV]
E_T	Arbitrary deep level impurity in the bad gap [eV]
E_{TA}	Trap activation energy [eV]
E_V	Valence band energy [eV]
f_a	Model fit parameter for volume fraction of material component "*a*"
f_b	Model fit parameter for volume fraction of material component "*b*"
FF	Fill factor [%]
G	Conductance [S]
G_L	Charge carrier optical generation rate [cm^{-3}]
G_{MGA}	Density of acceptor-like states [cm^{-3}eV^{-1}]
G_{MGD}	Density of donor-like states [cm^{-3}eV^{-1}]
G_1	Coefficient for quasi-neutral zone recombination in the emitter
G_2	Coefficient for quasi-neutral zone recombination in the base
h	Electrode length [mm]

I	External current [A]
I_B	Base component of quasi-neutral zone recombination [A]
I_d	Diffusion current [A]
I_E	Emitter component of quasi-neutral zone recombination [A]
I_g	Generation recombination current [A]
I_{MP}	Cell current at maximum power point [A]
I_{ph}	Generated photocurrent [A]
I_o	Pre-exponential factor accounting for number of nucleation sites [s^{-1}]
I_s	Saturation current [A]
I_{sc}	Short-circuit current or light generated current [A]
I_{SCA}	Short-circuit current contribution from the absorber [A]
I_{SCD}	Short-circuit current contribution from the depletion region [A]
I_{SCE}	Short-circuit current contribution from the emitter [A]
I_{sh}	Current passing through shunt resistance [A]
I_1	Dark saturation current due to recombination in the quasi-neutral regions [A]
I_2	Dark saturation current due to recombination in the space charge regions [A]
J_{INT}	Interface recombination current [A/cm^2]
J_{MP}	Current density at the maximum power point [A/cm^2]
J_n	Electron current density [A/cm^2]
J_p	Hole current density [A/cm^2]
J_{QNR}	Quasi-neutral zone recombination current [mA/cm^2]
k	Boltzmann constant [J/K, eV/K]
L	Distance between electrodes [mm]
L_B	Bulk diffusion length [μm]
L_{eff}	Effective diffusion length [μm]
L_f	Effective depletion length [nm]
L_n	Electron diffusion length [cm]
L_p	Hole diffusion length [cm]
n	Electron concentration [cm^{-3}]
n_o	Thermal equilibrium electron concentration [cm^{-3}]
N_A	Acceptor dopant concentration [cm^{-3}]
N_C	Effective density of states in the conduction band [cm^{-3}]
N_D	Donor dopant concentration [cm^{-3}]
N_{DB}	Total bulk density of states per unit volume [cm^{-3}]
n_i	Intrinsic carrier concentration [cm^{-3}]
N_S	Electron sheet density [cm^{-2}]
N_T	Net charge of all traps located in the bandgap [cm^{-3}]
n_t	Interface trapped charge per unit area [cm^{-2}]
N_V	Effective density of states in the valence band [cm^{-3}]
n_1	Diode ideality factor for the quasi-neutral regions
n_2	Diode ideality factor for the space charge regions
N_1	Net free carrier concentration in material 1 [cm^{-3}]
N_2	Net free carrier concentration in material 2 [cm^{-3}]
p	Hole concentration [cm^{-3}]
p_o	Thermal equilibrium hole concentration [cm^{-3}]
P_{gen}	Generated power at the maximum power point [W]
P_{in}	Incident power [W]

P_{loss}	Total power loss [W]
q	Electron charge [C]
R_c	Contact resistance [Ω]
R_n	Electron recombination rate [cm^{-3}]
R_p	Hole recombination rate [cm^{-3}]
R_{pr}	Probe resistance [Ω]
R_s	Series resistance [Ω]
R_{sp}	Spreading resistance [Ω]
R_{sh}	Parallel/ shunt resistance [Ω]
s	Spacing between adjacent contact fingers [cm]
s_b	Back surface recombination velocity [cm/s]
s_{it}	Interface recombination velocity [cm/s]
t	Annealing time [seconds]
T	Device temperature [K]
t_c	Characteristic time of crystallization [s]
t_g	Grain growth time [s]
t_o	Amorphous incubation time (time before crystallization occurs) [s]
T_o	Turn-on temperature [K]
v	Solid phase epitaxy growth velocity [cm/s]
v_o	Solid phase epitaxy film dependent pre-factor [cm/s]
V_{th}	Thermal voltage at room temperature [V]
V	Voltage [V]
V_{bi}	Built-in potential [V]
V_D	Diffusion potential [V]
V_{int}	Intercept voltage [V]
V_{MP}	Cell voltage at maximum power point [V]
v_n	Attempt to escape frequency [Hz]
V_{oc}	Open-circuit voltage [V]
$V_{oc\ INT}$	Limiting open-circuit voltage for interface dominant recombination current [V]
$V_{oc\ QNR}$	Limiting open-circuit voltage for quasi-neutral zone dominant recombination current [V]
$V_{oc\ SCR}$	Limiting open-circuit voltage for space charge region recombination current [V]
W	Depletion region width [nm]
W_D	Bias dependent depletion region width [cm]
W_{DG}	Standard deviation of the donor and acceptor Gaussians [eV]
W_N	Emitter thickness [cm]
W_P	Absorber thickness [cm]
X	Crystal fraction [%]
x_n	Depletion region width in the emitter [cm]
x_o	Defective layer thickness [nm]
x_p	Depletion region width in the absorber [cm]
Y	Complex admittance [S]
Y'	Susceptance [S]
β	Temperature dependent exponent [V^{-1}]
δQ	Differential change in stored charge [C]
δV	Differential change in voltage [V]

δ_1	Energy difference between Fermi level and valence band in material 1 [eV]
δ_2	Energy difference between Fermi level and conduction band in material 2 [eV]
ΔE_C	Conduction band offset [eV]
ΔE_V	Valence band offset [eV]
Δn	Excess minority carrier electron concentration [cm^{-3}]
ε	Dielectric function (dielectric permittivity)
ε_a	Dielectric function of material component "a"
ε_b	Dielectric function of material component "b"
ε_f	Effective dielectric function for the Bruggeman effective medium approximation
ε_i	Imaginary component of the dielectric function
ε_n	Dielectric constant on the n-side
ε_p	Dielectric constant on the p-side
ε_r	Real component of the dielectric function
η	Solar cell efficiency [%]
λ	Wavelength of light [nm]
μ_n	Electron mobility [cm^2/Vs]
ρ	Complex reflectance
ρ_s	Resistivity [Ω cm]
$\rho_\square$	Sheet resistivity [$\Omega/\square$]
σ_n	Root-mean-square thermal velocity of free electrons [cm/s]
σ_{na}	Trap cross section [cm^{-2}]
τ	Characteristic time of microscopic interaction [s]
τ_D	Effective lifetime in the depletion region [s]
τ_R	Dielectric relaxation time [s]
ϕ_b	Effective barrier height [eV]
χ^2	Ellipsometry goodness-of-fit parameter
ψ_n	N-side electrostatic potential difference between intrinsic level and Fermi level [V]
ψ_p	P-side electrostatic potential difference between intrinsic level and Fermi level [V]
ω	Frequency [Hz]

1 Literature Review

1.1   Physics and Applications of Photovoltaic Cells

The first modern photovoltaic solar cell, converting sunlight to electricity with an efficiency of 6%, was produced in 1954 at Bell Labs where it was discovered that a p-n junction generated a voltage in response to illumination. [1] Over the decades, photovoltaic cell efficiency has increased, cost has decreased, and cell fabrication has diversified beyond silicon wafer devices exploring thin film alternatives made, for example, from hydrogenated amorphous silicon (a-Si:H), polycrystalline silicon, CdTe, and $CuInGaSe_2$. Multi-junction concentrator based photovoltaics are also being developed using III-V compound semiconductors such as GaInP, GaAs, GaAsP, and AlGaAs. Beyond the inorganic semiconductors, dye sensitized solar cells as well as polymeric conjugated semiconductor materials are being explored. As photovoltaic technologies have become more mature, the price has been reduced due to economies of scale and improvements in manufacturing methods. Between 1998 and 2008, the market for photovoltaic modules increased by a factor of 20. Although the cost of a module depends on many factors such as geographic location, cost of electricity, and support mechanisms such as feed-in-tariffs, module costs are approaching 1 US $/W and have been reduced by more than a factor of 10 since the 1970s. [2] Photovoltaics first found application in remote off-grid areas and in replacing batteries in satellites. Since then, its application has expanded to large scale power generation in many countries.

The photovoltaic effect occurs when a semiconductor absorbs light. Photons with energy greater than the semiconductor bandgap, E_g, transfer their energy to electrons in the valence band elevating them to the conduction band. If the semiconductor has a small bandgap, then a large wavelength range of photons will be able to create electron hole pairs, producing a large photocurrent but a small voltage. If the bandgap is large, the photovoltage will be high but the current low. In an isolated semiconductor, an excited electron will eventually recombine with a hole either through the emission of a photon or phonon. In order to extract useful electrical energy, excited charge carriers must be collected before they recombine, typically by using the charge separating junction of a p-n diode. The passage of minority carriers (holes in the n-type region, electrons in the p-type region) prevents electron-hole recombination. Minority carrier electrons produced in the p-type region will have a limited lifetime in the presence of majority carrier holes, but after having passed across the junction into the n-type side they become majority carriers with an essentially unlimited lifetime. A similar process occurs for minority carrier holes produced in the n-type region. For crystalline silicon the p-n junction is formed, for example, by furnace diffusion of dopant impurities or ion implantation creating two layers of different conductivity type. Diffusion of charge carriers across the junction occurs until equilibrium is established by an internal electric field. This built-in electric field acts as the charge separation mechanism and is critical for solar cell operation. Minority carrier electrons produced in the p-type region migrate to the junction and are swept across to the n-type side by the internal electric field. Similarly, minority carrier holes produced in the n-type region are swept by the field into the p-type region. In this way, light energy is absorbed and transferred to charge carriers from which energy is extracted as they travel through an external circuit.

A typical p-n junction solar cell consists of a front ohmic contact, bus bar and fingers, and a back ohmic contact (Figure 1.1). The junction depth is typically around 250 nm. Any photon energy above E_g is wasted as heat. Important recombination mechanisms in a solar cell include recombination through traps in the bandgap (Shockley-Read-Hall), radiative (band-to-band) recombination, and Auger recombination. Interface recombination may also be significant at the interface between two dissimilar semiconductors (heterojunction), and at metal-semiconductor contacts at the front or back of the cell. [3] As determined by Shockley and Queisser, a single bandgap silicon solar cell reaches a theoretical thermodynamic efficiency limit under 1 sun of 29%. [4] This limit is
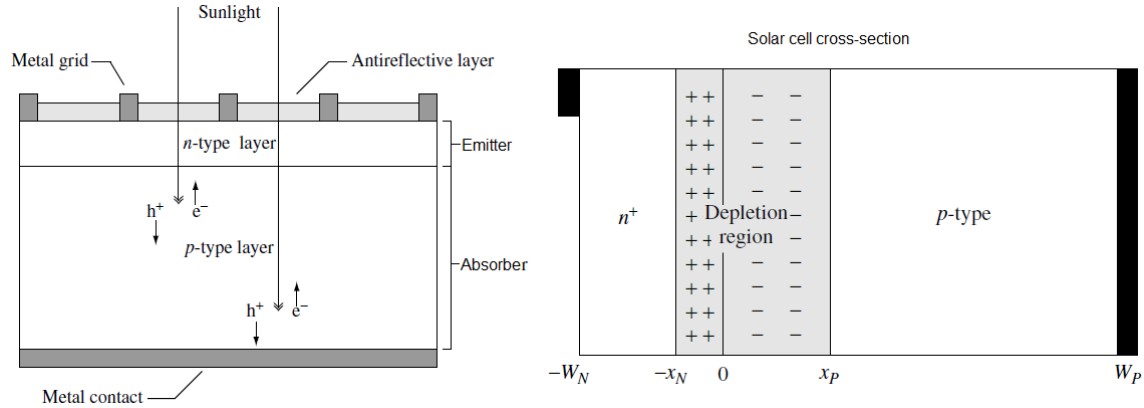
Figure 1.1: Schematic of a photovoltaic cell showing light-induced creation of electron hole pairs in the emitter and absorber.

due largely to the inefficient use of photons with energy above or below the bandgap. Photons with energy greater than the bandgap produce an electron hole pair whose excess energy is dissipated by thermalization (phonon vibrations producing heat within the crystal lattice). Thermalization is a spectrum blue loss involving photons of blue and ultraviolet wavelength. At the other end of the spectrum there is red loss: infrared photons whose energy is too low to bridge the bandgap to produce an electron hole pair. The ideal current-voltage behavior of a cell under illumination is given by equation 1.1:

$$I = I_{sc} - I_1\left(e^{qV/kT} - 1\right) - I_2\left(e^{qV/2kT} - 1\right) \tag{1.1}$$

The external current is I and V is the voltage, T is the device temperature, k is the Boltzmann constant, and I_{sc} is short-circuit current or light-generated current. [5] The short-circuit current is the sum of contributions from the n-type emitter, I_{SCE}, the depletion region, I_{SCD}, and the p-type absorber, I_{SCA}. The dark saturation current due to recombination in the quasi-neutral regions is I_1 which is the sum of contributions from the emitter (assumed n-type), I_E, and base (assumed p-type), I_B, according to equation 1.2.

$$I_1 = I_E + I_B \tag{1.2}$$

The magnitude of I_E and I_B is given by equation 1.3 and equation 1.4 and depends on the intrinsic carrier concentration, n_i, the dopant concentration in the n-type and p-type regions, $N_{D/A}$, the minority carrier diffusion coefficient and diffusion lengths for electrons and holes, $D_{p/n}$ $L_{p/n}$, and the thicknesses of the depletion regions in the n-type and p-type layers (as shown in Figure 1.1).

$$I_E = qA \frac{n_i^2}{N_D} \frac{D_p}{L_p} \left(\frac{D_p/L_p \sinh\left[(W_N - x_N)/L_p\right] + S_F \cosh\left[(W_N - x_N)/L_p\right]}{D_p/L_p \cosh\left[(W_N - x_N)/L_p\right] + S_F \sinh\left[(W_N - x_N)/L_p\right]} \right) \tag{1.3}$$

$$I_B = qA \frac{n_i^2}{N_A} \frac{D_n}{L_n} \left(\frac{D_n/L_n \sinh\left[(W_P - x_P)/L_n\right] + S_{BSF} \cosh\left[(W_P - x_P)/L_n\right]}{D_n/L_n \cosh\left[(W_P - x_P)/L_n\right] + S_{BSF} \sinh\left[(W_P - x_P)/L_n\right]} \right) \tag{1.4}$$

The component of the dark saturation current due to recombination in the depletion region is given by equation 1.5 (where W_D is the bias-dependent depletion width, A is the device area, τ_D is the effective lifetime in the depletion region). [6]

$$I_2 = qA \frac{W_D n_i}{\tau_D} \tag{1.5}$$

The equivalent-circuit of a solar cell consists of a constant current source in parallel with two diodes and a load resistance. The solar cell figures of merit are the efficiency, η, Fill Factor, FF, open-circuit voltage, V_{oc}, and short-circuit current, I_{sc}, for a given incident power, P_{in}.

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_{sc}}{I_1}\right) \tag{1.6}$$

$$\eta = \frac{FF \cdot I_{sc} V_{oc}}{P_{in}} \tag{1.7}$$

The fill factor is the power produced at the maximum power point divided by the maximum power rectangle as given by $FF = I_{MP} V_{MP}/I_{sc} V_{oc}$ and shown in Figure 1.2a). One of the factors that affect cell efficiency is series resistance of the front contacts (series resistance should be as close to zero as possible). Series resistance depends on the impurity concentrations of the n-type and p-type regions and the geometric arrangement of the front contact fingers and bus bars. Total series resistance is typically around 0.7 Ω or less for n⁺p cells, and around 0.4 Ω for p⁺n cells due to the lower resistivity of n-type substrates. [3]

a)

Maximum power point (V_{MP}, I_{MP})

Parameter	Value
I_{SC}	3.67 A
V_{OC}	0.604 V
I_{MP}	3.50 A
V_{MP}	0.525 V

b)
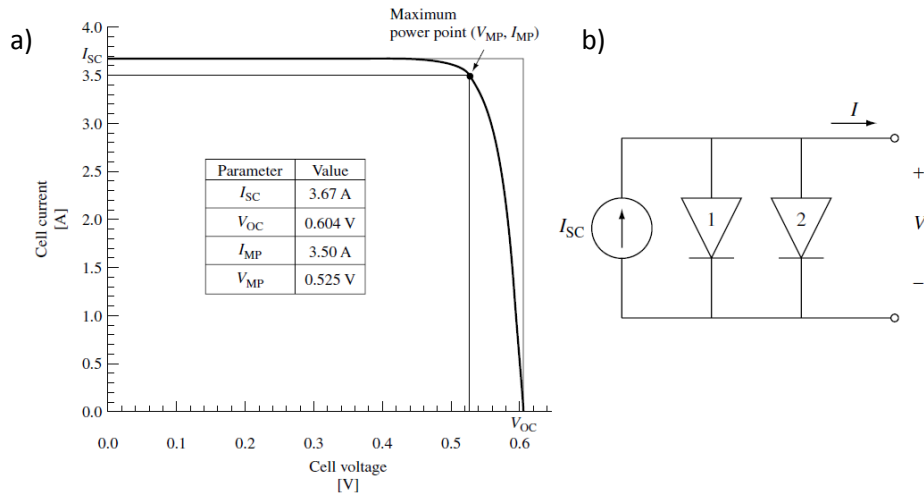
Figure 1.2: a) Current-voltage characteristic for a 100 cm² solar cell, b) corresponding double diode equivalent circuit. [6]

1.2   Heterojunction Solar Cell State-of-the-Art

Silicon wafer heterojunction solar cells can be divided into two types: those with or without an intrinsic layer. The heterojunction solar cell is a bulk device because nearly all of the photocurrent is produced in the silicon substrate. However, the thin emitter layer and the heterojunction interface (both only a few nanometers thick) strongly affect charge transport, defect density, conductivity, and recombination. [7] In both homo and heterojunction solar cells, electrons and holes are produced throughout the bulk of the device and move in a direction dictated by diffusion/drift. In the bulk c-Si wafer the transport of charges is almost exclusively by diffusion. In an ideal solar cell, diffusion is the dominant transport mechanism, but since carriers are transported across the depletion region by the electric field there is also a drift (voltage-dependent) component. Both the homojunction and the heterojunction solar cell have recombination at the front and back contacts, and recombination within the depletion region and quasi-neutral regions. However, defects at the heterojunction interface and charge carrier trapping create a new recombination pathway not present in homojunction cells. For traditional solar cells, the series and shunt resistances (R_s and R_{sh}) are extracted from the slope of the current-voltage curve close to short-circuit and open-circuit, but in a heterojunction solar cell interface recombination can sometimes influence these slopes making reliable extraction of R_s and R_{sh} problematic. [7] [8]

The classic example of the heterojunction solar cell is Panasonic's (formerly Sanyo) heterojunction with intrinsic thin layer (HIT). The approximate structure of the cell is shown in Figure 1.3. State-of-the-art efficiency for a laboratory HIT cell was recently reported at 24.7%, ($V_{oc} = 750$ mV)

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for a cell area of 101.8 cm^2. [9] The HIT cell is a bifacial device consisting of an n-type wafer, PECVD deposited a-Si:H layers forming a p-i structure on the light-absorbing side, and a n-i structure for back surface field. The n-type wafer is favoured over the p-type wafer due to a reduced sensitivity to interface defects. [10] Because of the high sheet resistance of the a-Si:H layer, a transparent conducting oxide (TCO) is needed to minimize resistive losses from current flowing to the metal contacts. A TCO on both sides allows lateral charge collection and functions as anti-reflection and surface passivation. Finger electrode spacing is around 2mm (less than that of conventional diffused junction cells) to compensate for poor sheet resistance of the TCO. The HIT cell has a lower dark reverse current (by 2 orders of magnitude) than a standard cell. Notable HIT cell advantages are:

1) Due to the high open-circuit voltage, the temperature coefficient is better than conventional solar cells with higher output power at high temperatures.
2) The a-Si:H intrinsic layer passivates dangling bonds and surface defects on the c-Si substrate.
3) The entire cell is fabricated at temperatures below 200°C which provides two benefits: i) reduced mechanical stress allowing use of thinner wafers, ii) improved minority carrier lifetime because lifetime is sensitive to wafer thermal history (particularly for cheaper substrates with increased impurity concentration). [11]
4) The thinness of the amorphous silicon layers used in the device means the Staebler-Wronski effect is negligible.

The deposition conditions of the a-Si:H layers are very important and must be "soft" (low power, low substrate temperature) to prevent excessive ion damage to the wafer. Wafer cleaning methods are equally important to minimize interface recombination. In order to increase the cell open-circuit voltage it is important to reduce the interface recombination at the a-Si:H / c-Si interface to suppress the backward saturation current. That can be done by the deposition of high quality a-Si:H layers with low surface damage and by optimizing the band offset between the various materials. In addition, continual improvements in other technologies such as TCO, and screen printing of
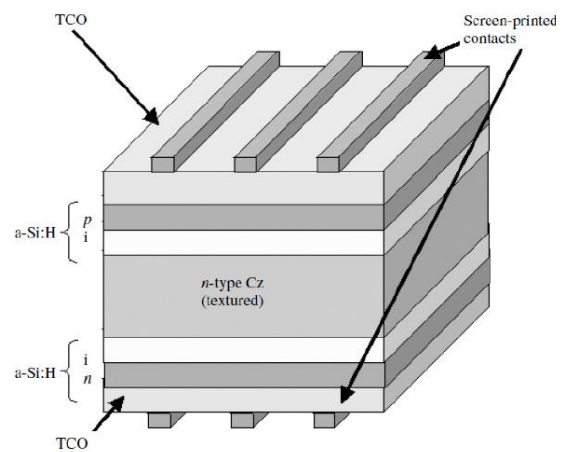
Figure 1.3: Panasonic HIT solar cell. The thickness of doped a-Si:H is around 10-20 nm, and the intrinsic a-Si:H passivation layers are around 5nm.

highly conductive metallic pastes also translate into further HIT cell performance advances. Other areas of improvement include optimization of the back surface field (improving spectral response in the high wavelength region and increasing short-circuit current) and development of large bandgap window layers like a-SiC. [12] Also, enhanced chemical cleaning steps before layer deposition, combined with hydrogen plasma annealing to passivate remaining dangling bonds can further increase efficiency. The drawback of heterojunctions is the possibility of a new recombination pathway through defects at the interface. [8] Interface defects can refer to impurities but also unsaturated dangling bonds in c-Si and dangling bonds in a-Si:H which are within the tunneling distance of minority charge carriers coming from c-Si. [13] [14] [15]. There are very few details on the wafer cleaning and surface preparation steps and PECVD deposition conditions. Only a few authors provide this information. [15] Table 1.1 summarizes some of the research groups investigating heterojunction cells based on amorphous and crystalline silicon emitters.

Heterojunction with intrinsic layer	Base material			Solar Cell Figures of Merit					Ref
	Wafer	Texture	Doping (Ωcm)	Area (cm^2)	V_{oc} (mv)	I_{sc} (mA/cm^2)	FF (%)	Eff (%)	
n+ a-Si:H/i a-Si:H/ n c-Si/i a-Si:H/p+ a-Si:H	Cz (n)	Yes	1	101.8	750	39.5	83.2	24.7	[16]
n+ a-Si:H/i a-Si:H/ n c-Si/i a-Si:H/p+ a-Si:H	Cz (n)	No	1-10	Not Reported	631	36.3	76.1	17.4	[17]
p+ epi/i epi/n c-Si	Cz (n)	No	1	1	558	32	73	13.1	[15]
p+ a-Si:H/i epi/n c-Si	Cz (n)	No	1	1	608	29	72	12.8	[15]
p+ μc-Si/i a-Si:H/n c-Si	Cz (n)	No	1	1	638	28.1	76	13.7	[15]
n+ a-Si:H/i a-Si:H/p c-Si	Cz (p)	Yes, Al BSF	1	2.3	600	37.1	76.3	17.0	[18]
n+ a-Si:H/i a-Si:H/ n c-Si/i a-Si:H/p+ a-Si:H	Cz (n)	Yes	0.5-5	1	678	34	73.7	17.0	[19]
Heterojunction without intrinsic layer	Base material			Solar Cell Figures of Merit					Ref
	Wafer	Texture	Doping (Ωcm)	Area (cm^2)	V_{oc} (mv)	I_{sc} (mA/cm^2)	FF (%)	Eff (%)	
n+ a-Si:H/p c-Si	FZ (p)	No	1×10^{16} cm^{-3}	7.9	654.5	26.65	88	14.1	[8]
n+ a-Si:H/p c-Si/p+ a-Si:H	FZ (p)	Yes	1-2	1	629	34.9	79	17.4	[13]
p+ a-Si:H/n c-Si/n+ a-Si:H	FZ (n)	Yes	1-2	1	639.4	39.3	78.9	19.8	[13]
p+ a-Si:H/n c-Si/n+ a-Si:H	FZ (n)	Yes	1-2	1	612	35.3	74.3	17.1	[20]
n+ a-Si:H/p-cSi/p+ a-Si:H	FZ (p)	Yes	1-2	1	631	37.25	79	17.6	[20]
n+ a-Si:H/p c-Si	Cz (p)	No	0.5-5	1	568	31.3	71	12.6	[19]
n+ a-Si:H/p c-Si/p+ a-Si:H	Cz (p)	No	0.5-5	1	634	30.3	81	15.5	[19]
p+ a-Si:H/n c-Si/n+ a-Si:H	Cz (p)	Yes	0.5-5	1	641	36.5	78.2	18.3	[19]
p+ a-Si:H/n c-Si	Cz (n)	No	1-10	0.76	530	31	54	13.5	[14]
p+ μc-Si/n c-Si	Cz (n)	No	1-10	0.76	500	38	71.1	8.9	[14]

Table 1.1: Summary of heterojunction solar cell efficiencies from different research groups. All semiconductor film deposition was performed by PECVD with the exception of reference [14] where radio frequency magnetron sputtering was used.

1.3 Rapid Thermal Annealing for Heterojunction Solar Cells

The classic heterojunction using amorphous silicon with thin intrinsic layers requires very careful deposition conditions for intrinsic a-Si:H because the layer is usually around 5 nm thick. The process window for depositing an ultrathin intrinsic a-Si:H is narrow because a high deposition temperature (> 130°C) leads to partial epitaxial growth and a high dark saturation current due to interface defects. [21] The optimized deposition conditions are not widely available as illustrated by differences in HIT cell efficiencies in Table 1.1.

The goal of this thesis is to reduce the processing constraints for a heterojunction cell by: 1) deposition of n-type a-Si:H without using an intrinsic a-Si:H buffer layer and 2) using rapid thermal annealing (RTA) with a low thermal budget to create a highly crystalline emitter with sufficient lateral conductivity to eliminate the transparent conducting oxide, and 3) to investigate alternative heterojunction interface passivation layers such as silicon nitride which is suitable for high temperature processing. RTA is attractive for photovoltaics because it is rapid and can be scaled on an industrial level.

Creation of thin crystalline films can be done by many methods. Very high frequency PECVD has uniformity issues for deposition over large areas due to the formation of standing waves in the plasma. Crystallization by laser (for example, excimer) is expensive. [22] Annealing of spin on dopants by RTA can introduce contaminants into the chamber. By contrast, RTA of a-Si:H films minimizes the contamination issue (compared to spin on dopants) while still maintaining a small thermal budget. Furnace crystallization by regular furnace has a high thermal budget with long ramp-up and ramp-down times of several hours. The definition of thermal budget is the product of heating temperature and time (including ramp-up and ramp-down cycles). Phosphorous diffusion in a batch furnace occurs by bubbling nitrogen carrier gas through liquid POCl$_3$ or by using solid diffusion sources. A representative processing condition for a solar cell phosphorous diffusion is an annealing temperature around 900°C for 30 minutes with a ramp-up rate of 50°C per minute and a cool-down rate of 20°C per minute. [6] By contrast, a typical RTA cycle sufficient to produce a highly crystalline n-type emitter is a 750°C anneal for 1 minute with a ramp-up rate of 10°C/s. In addition, the conventional furnace diffused junction solar cell requires steps of phosphorous silicate glass removal and edge isolation by laser grooving neither of which are required for RTA processed cells. Using a crystalline instead of an a-Si:H emitter also reduces parasitic absorption losses. The bandgap of n-type amorphous silicon is approximately 1.7-1.8 eV whereas the bandgap of nanocrystalline silicon is in the range of 1.1-1.5 eV. [23] Although a-Si:H has a higher bandgap than nanocrystalline silicon, a-Si:H is a direct bandgap semiconductor and thus has a

larger absorption coefficient. However, when an intrinsic a-Si:H layer is no longer used, consideration of the dopant concentration in the emitter becomes more important. The higher the dopant concentration, the greater the dangling bond density in the doped a-Si:H and the greater the recombination rate via gap states. A highly doped emitter will increase V_{oc} because of greater band bending. But as the dopant density increases beyond a certain concentration, enhanced recombination negates any further V_{oc} increase. The closer the Fermi level is to the conduction band the higher the V_{oc}. But the highest doping concentration does not necessarily give the best efficiency. [20] The optimum doping for a heterojunction without intrinsic layer is obtained for a Fermi level which is as close to the conduction band as possible while still keeping the interface defect concentration relatively low. There Is a trade-off: increasing the dopant concentration in the emitter increases band bending but also raises the defect density at the interface and increases the number of gap states in the emitter. [20] For heterojunctions without a passivation layer, hydrogen dilution is also critical. A lower hydrogen dilution worsens the passivation ability of the emitter. [15] For example, Rizolli et al. note that that for epitaxial and microcrystalline emitter heterojunctions, a drop in hydrogen dilution from 99% to 96% can cause a decrease in V_{oc} of up to 300 mV. [15]

1.4   Solid Phase Crystallization by Epitaxy

Methods for producing thin crystalline films can be divided into four families: 1) Liquid phase crystallization by laser, electron beam, or ion beam, 2) Solid phase crystallization by rapid thermal annealing or conventional furnace annealing, 3) direct deposition by VHF PECVD or LPCVD, and 4) solid phase crystallization by metal-induced crystallization. This review examines solid phase crystallization by RTA and conventional furnace. Although the photon spectra of RTA and conventional furnace are different, the underlying kinetics of crystallization are similar because they are both thermally activated. [24] Solid phase crystallization can be divided into two types: silicon epitaxy from a single crystal silicon substrate, and random nucleation and grain growth.

Solid phase crystallization of a-Si:H occurs because a-SiH has a higher free energy than c-Si. There is a driving force towards crystallization to lower free energy. Crystalline silicon and a-Si:H both have strong covalent bonds and tetrahedral bonding arrangements, but in a-Si:H there is no long range order beyond approximately two interatomic distances. During crystallization, thermal agitation

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produces small clusters of ordered silicon atoms with low free energy. The bulk free energy of an ordered cluster is lowered, compared to the amorphous phase, because of a reduction in bond distortions. However, the free energy of atoms at the cluster surface may increase due to the distortion of bonds caused by the interface between a-Si:H and c-Si. [25] Solid phase epitaxy (SPE) occurs by the movement of the single crystal interface from the wafer plane to the film surface which gradually consumes a-Si:H (Figure 1.4). Epitaxy is first noticed at temperatures at and above 500°C. The SPE rate is critically dependent on concentration of impurities, crystal orientation, and the annealing temperature. [26] The epitaxy process shows a thermally activated behaviour with a crystallization rate that follows an Arrhenius behaviour given by equation 1.8:

$$v = v_o exp(- E_A / kT) \hspace{4cm} (1.8)$$

where v is the SPE growth velocity, v_o is a film dependent property, and E_A is the activation energy. The extracted value of the activation energy is more accurate the larger the temperature range over which the measurements are made. [25] [26]

Influence of substrate orientation: The epitaxy rate is dependent on substrate orientation. Epitaxy is fastest on (100) crystals and 2 and 20 times slower on (110) and (111) orientations respectively. Many other factors also influence epitaxy such as crystallization temperature, film thickness, type and concentration of impurities, and the presence of capping layers. The best quality epitaxial films are obtained on (100) orientation silicon wafers with film thickness between 20-500 nm. [26] By contrast, epitaxy on (100) silicon is best for devices because it has fewer defects compared other orientations and can be performed on thicker films (20-500 nm), over a wider range of temperatures 500-1000°C. Epitaxy dislocation density is around $10^2 - 10^3$ cm^{-2}, and is suggested to be due to imperfections from the substrate. The annealing temperature greatly determines whether or not the dominant crystallization mechanism will be epitaxy or random nucleation and grain growth. As the annealing temperature rises the competition between the two mechanisms increases. For example, investigation by Zotov et al. for epitaxy of vacuum deposited a-Si:H on Si wafers showed complete epitaxy throughout the film thickness at an annealing temperature of 600°C. However, Zotov states that for films thicker than 80 nm at an annealing temperature of 900°C, a thin polycrystalline layer formed at the surface which blocked epitaxy. [26]

Influence of non-dopant impurities: Epitaxial growth on silicon requires a very clean interface and minimal contamination during growth. Deposited a-Si:H contains micro-voids which can further act as absorption centers for impurities. Low substrate temperature during a-Si:H deposition can increase impurity adhesion. Even exposure to clean room air can contaminate the a-Si:H layer which can absorb carbon, oxygen, and nitrogen up to a depth of 100 nm. [27] A high density of non-dopant impurities hinders the epitaxial growth front, causing epitaxy to proceed from isolated areas in a columnar growth pattern followed by lateral epitaxy. Film contamination will reduce the epitaxy growth rate, create high defect density, and may cause the dominant crystallization mode to switch to random nucleation and grain growth. The cleanliness of the interface is critical: For example, Zotov et al. have shown that as the atomic oxygen concentration on the surface decreases from 10^{15} cm^{-2} to 10^{13} cm^{-2}, the crystallization changes from random crystallization to SPE. Ideally, both deposition and epitaxial growth should be performed under ultra-high vacuum conditions of around $(0.4 - 1) \times 10^{-7}$ Pa. Under worse vacuum conditions SPE is slowed. For example at 5×10^{-7} Pa the SPE growth rate is slower by a factor of 2. [26] Alternatively, capping layers may also be used to protect the a-Si:H from exposure to impurities. Layers such as SiN$_x$ can cause hydrogen passivation of defects. PECVD deposited SiN$_x$ has a high concentration of hydrogen which is ejected into the crystallizing film during annealing. [25]

Influence of boron and phosphorous: dopant impurities added to an a-Si:H film will induce competition between random nucleation and grain growth and SPE. Dopant concentration also has a large influence on the epitaxy rate. Oxygen, nitrogen and carbon decrease the epitaxy growth rate, whereas dopants from groups III and V of the periodic table present in amounts greater than 0.1 atomic % can enhance or hinder depending on the concentration. Olson and Roth have shown that for intrinsic and lightly doped films there is a single activation energy, around 2.7 eV, over the temperature range from 470 °C to 1350°C which is characteristic of epitaxy and independent of the method by which the a-Si:H film was deposited (whether PECVD, e-beam, sputtering, ion implantation). The fixed activation energy suggests that the interfacial process of bond breaking and
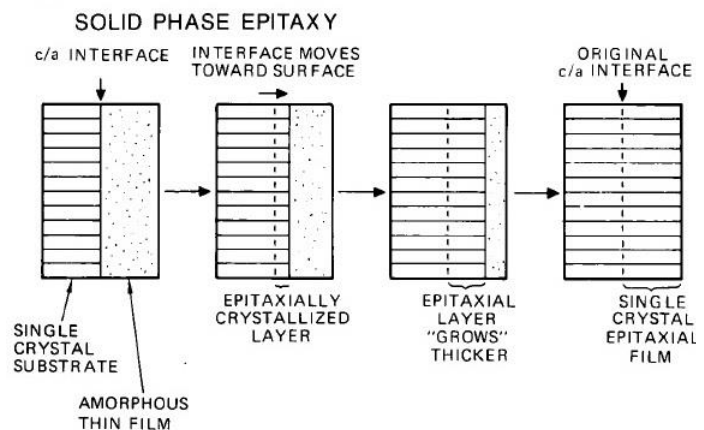
Figure 1.4: Illustration of solid phase epitaxy from c-Si substrate. [25]

rearrangement is the same regardless of the microstructure of the precursor material. However, the pre-exponential factor, v_o , in equation 1.8 will be different for films deposited in different ways which indicates a difference in the number of interface sites available for atomic rearrangement. [25] As the dopant concentration of phosphorous or boron is increased, the epitaxy growth rate increases until a limiting concentration is reached beyond which the dopant concentration decreases. The decrease in epitaxy growth rate is due to faulting and dopant segregation. Phosphorous and boron act differently in the epitaxy process. For phosphorous dopant concentrations beyond 3×10^{20} cm^{-3}, for example, Zotov noted that phosphorous both speeds up the rate of lateral epitaxy, and slows down and suppresses random nucleation and grain growth. Having a high phosphorous dopant concentration (for example, 1.7×10^{20} cm^{-3}) can increase the growth rate up to a factor of between 6 to 8. [28] However, for comparable boron concentrations there is enhanced lateral epitaxy but no suppression of random nucleation. [26] Boron is shown to enhance SPE over a broad range of temperatures and annealing times, and so it is representative of a "simple" rate enhancement with other competing effects (random nucleation and growth, precipitate formation and segregation) being negligible. For boron, the SPE rate increases until boron concentration reaches 2×10^{20} cm^{-3}. Dopant concentrations from groups III and V above 10^{19} cm^{-3} generally enhance the SPE rate, while non-dopant impurities generally slow SPE. The SPE rate enhancement is less for phosphorous doped films than for boron doped films. However, when boron and phosphorous are present in a-Si:H in equal concentrations there is no additive effect SPE and the epitaxy rate is driven back to that for intrinsic material. Epitaxy rate as a function of temperature for a given boron or phosphorous concentration shows Arrhenius behaviour with typical activation energies around 2.52 eV (B), 2.68 eV (P). In spite of the high dopant concentration, all of these activation energies fall very close to the activation energy of intrinsic epitaxially grown films (2.7 eV). [26] Most of the group V dopants when present in high enough concentration cause temperature dependent interaction between random nucleation and grain growth and dopant diffusion. [25] As the Fermi level moves towards either band edge there is an enhancement in SPE rate. One exception is at high temperatures. At high temperatures, the thermally excited carrier concentration overwhelms the ionized dopant carrier concentration making the semiconductor intrinsic and returning the Fermi level to midgap. However, under these conditions there is surprisingly no drop in SPE rate. [25]

Theoretical models: There are several models to predict the epitaxy rate while taking into account key crystallization factors such as the a-Si:H/c-Si interface, orientation of crystal substrate, and concentration of dopant-induced growth centers. However, the growth rate is also affected in complicated ways by the structure of the a-Si:H precursor which may contain micro-voids and crystal

defects. Currently, there is no complete theory of epitaxy which takes into account all of the factors that can affect crystallization. There are several models that try to predict the characteristic activation energy. [29] Ohdomari proposed a model for activation energy that is the sum of the energy required to break the bond and the energy associated with bond disorder. Germain proposed a model based on the movement and diffusion of charged dangling bonds in a-Si:H towards the c-Si / a-Si:H interface where they are collected/captured by atoms which then become incorporated into the crystal lattice. [30] Williams and Elliman built on these models and added an additional complexity by taking into account the affect of dopants on the SPE process. The premise of the Williams model is that the SPE rate is dependent on the density of charged nucleation sites at the interface, and that the density of these sites increases with increasing dopant concentration. [31] [32] Although it is clear that rate enhancement of SPE is affected by electronic changes at the c-Si / a-Si interface, the exact atomistic interpretation of rate enhancement is still unclear and a subject of active research. [26] [25]

1.5 Solid Phase Crystallization by Random Nucleation and Grain Growth

Crystallization of a-Si:H to polycrystalline silicon by random nucleation and grain growth (RNG) is influenced by film defect density and microstructure and hydrogen content of deposited films. The amorphous incubation time, t_o , is defined as the time before any crystallization occurs. During the incubation period there is nucleation of crystallization sites which act as centers of grain growth. The nucleation rate has an exponential dependence given by Lee et al. in equation 1.9. [33]

$$I = I_o exp(-E_{inc}/kT) \tag{1.9}$$

The pre-exponential factor, I_o, accounts for the number of nucleation sites, and E_{inc} is the nucleation activation energy. Films with a large nucleation rate have a small final grain size. [33] The nucleation sites may be located at a material interface between the a-Si:H and the substrate (heterogeneous nucleation) or may be uniformly distributed throughout the film (homogeneous nucleation). Often, the nucleation in the film may be a combination of heterogeneous and homogeneous nucleation. The grain growth phase is defined by the crystal growth time, t_g, which occurs after the incubation period. The characteristic time of crystallization, t_c, is the sum of the incubation time and crystal growth time according to equation 1.10.

$$t_c = t_o + t_g = \tau \, exp(E_o/kT) \tag{1.10}$$

The activation energy between the metastable amorphous state and the stable crystalline state is E_o, the characteristic time of microscopic interaction between neighbouring atoms is τ (approximately

10^{-14} seconds). The transformation of the film from amorphous to polycrystalline takes place by a displacement of silicon atoms from amorphous metastable sites by overcoming a potential barrier and reaching stable (crystalline) lower energy sites. [34] The time dependence of the crystalline fraction is given by equation 1.11. [33]

$$X(t) = 1 - exp[-(t - t_o)^3/t_c^3] \tag{1.11}$$

For conventional furnace annealing, the total crystallization time by homogeneous RNG is not affected by the thickness of the film. As the annealing temperature increases, the crystal grain size decreases. The activation energy of the film differs greatly depending whether it was formed by RNG or SPE. Epitaxy has an activation energy around 2.7 eV whereas random grain growth films are around 4 eV. In general, epitaxy dominates at low temperatures whereas RNG dominates at temperatures above 1000°C. However, in reality the presence of defects and impurities cause RNG to become significant compared to epitaxy at temperatures below 1000°C. [25]
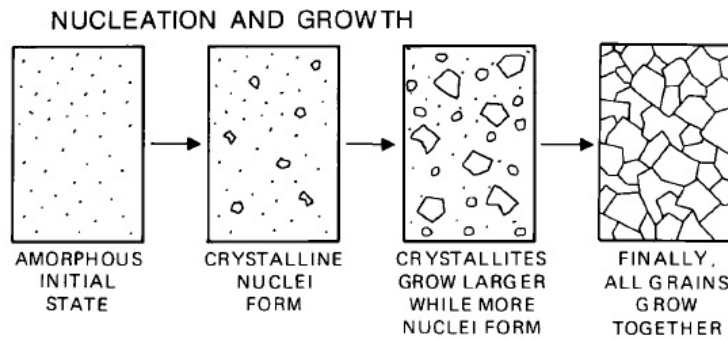
Figure 1.5: Illustration of random nucleation and grain growth in amorphous silicon. [25]

Influence of non-dopant impurities: Films exposed to air showed a much slower crystallization time (5 to 10 times slower) than films crystallized in a vacuum. Studies have shown that it is not the grain growth rate that is affected by exposure but rather the nucleation rate (an oxide forms which makes nucleation sites at the surface unavailable). Under these conditions, crystallization proceeds by homogeneous nucleation rather than nucleation at the surface. [25]

Influence of Hydrogen: The key point proposed by Mahan is that the crystallization depends not on the disorder in the film due to hydrogen evolution, but rather on the spatial distribution of the hydrogen. [35] The ratio of isolated (unclustered) to clustered hydrogen in the film is particularly important. The density of clustered and isolated hydrogen was calculated and found to be an order of

magnitude smaller for hot-wire CVD of a-Si:H films compared to PECVD films. Mahan proved that PECVD deposited films have a much larger ratio of clustered to isolated hydrogen. Crystallization kinetics depend on a critical crystallite size which requires a minimum number of silicon atoms. Mahan has shown that the hydrogen-deficient regions in PECVD films are smaller than the critical crystal size and thus have great difficulty to crystallize whereas hot-wire CVD has hydrogen-deficient regions which are sufficiently large that crystallization is relatively fast. This explains the much longer incubation time of PECVD films compared to hot-wire CVD films. The films that nucleate the fastest also have the smallest grain size. More recent work by Mahan [35] has provided further evidence for the influence of the critical crystal size. The regions with higher order (due to hydrogen deficiency resulting in isolated rather than clustered hydrogen) are the sites which act as nucleation centers (Figure 1.6). It seems that nucleation in thermally annealed a-Si:H depends critically on the hydrogen distribution (in isolated form or as clusters) and nucleation proceeds from the most well ordered parts of the film which are hydrogen-deficient and without clustered hydrogen. [36] [33] [37] It is hypothesized that the out-gassing of weakly bound hydrogen (1.4-1.6 eV activation energy) inhibits crystallization, but once the more tightly bound hydrogen (2.2 eV activation energy) leaves the film it creates defects (such as dangling bonds) that allow crystallization to proceed. [36] [38]
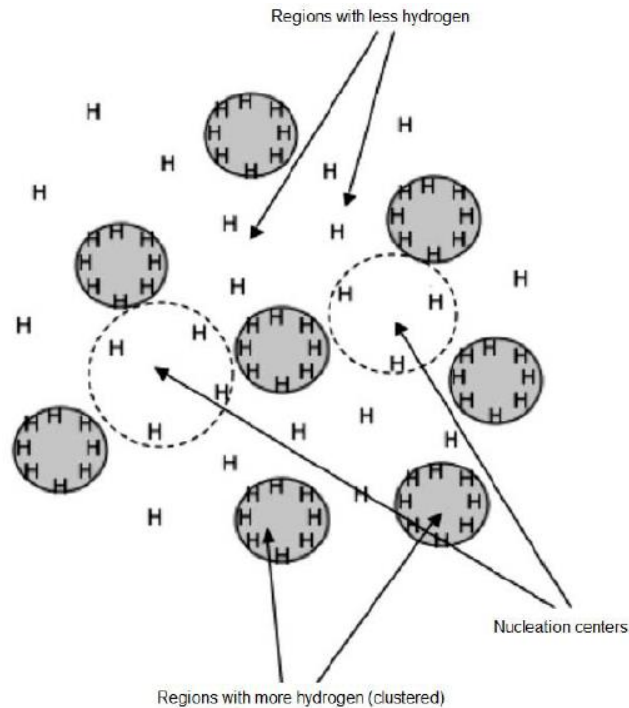
Figure 1.6: Illustration of clustered and isolated hydrogen. The dashed circles show regions of better ordered silicon network (isolated hydrogen) that act as nucleation centers for crystal growth. The shaded circles show areas of worse silicon atomic order due to clustered hydrogen. [35]

Crystallization Comparison between RTA and conventional furnace: RTA has a faster growth time and faster crystallization time at a given temperature compared to conventional furnace. For both RTA and furnace, higher annealing temperatures yield smaller grain size. Due to longer crystallization time, conventional furnace gives larger grain size than RTA. The RTA spectrum contains highly energetic photons that create carriers that recombine. This can break weak or strained bonds in a-Si:H resulting in localized heating and rapid nucleation and grain growth. [22] [39] Compared to RTA, conventional furnace generally has a larger concentration of inter-grain defects such as micro-twins. The defect density inside the grains for conventional furnace annealing was estimated at 2×10^{11} cm^{-2}, whereas RTA annealed films had a defect density of around at 3×10^{10} cm^{-2}. Micro-twins are electrically inactive, but when they terminate inside a grain and act as scattering centers they lower the effective grain size. For example, a 300 nm grain with micro-twins of 30 nm size is equivalent to a 50 nm grain free of micro-twins. More than conventional furnace, RTA has the capability of improving polysilicon film characteristics by reducing the density of dangling bonds and in-grain micro-twins. [40] Doping concentration does not affect the grain size significantly for conventional furnace annealed films. But, higher doping concentration in RTA has a large influence by reducing the crystallization temperature and

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increasing grain size significantly. Such behaviour for doped RTA films has been explained by transformation of a silicon dangling bond from a neutral state to a charged state. [41] [38]

1.6   Measurement Techniques

Optical Techniques (crystallinity of thin Si films): There are many techniques that can be used to assess the crystallinity of silicon films. X-ray Diffraction (XRD), UV-reflectance, Raman [33] [42], and ellipsometry are non-destructive, whereas transmission electron microscopy (TEM), Rutherford backscattering and ion channeling are more time-consuming and expensive. [36] [26] Additional techniques include low energy electron diffraction and electron backscattering diffractometry. For ellipsometry, the spectral dependence of the imaginary part of the dielectric constant distinguishes between the amorphous and crystalline silicon phase. The dielectric constant is given by real and imaginary components. [43] Ultraviolet and infrared reflectance is also suitable. Ultraviolet photons have a high absorption coefficient in silicon, less than 50 nm, which give information on surface crystallinity of the film. [44] Infrared reflectance gives information on bulk film crystallization and can distinguish between epitaxy and random nucleation and grain growth. [43] [37] [38] The refractive index of a-Si:H exceeds that of c-Si in the visible part of the spectrum which causes a change in reflectivity both at the surface and at the c-Si / a-Si:H interface [25]. XRD provides an average grain size estimate. Instrumental broadening has to be taken into account using standards for polycrystalline powder. Two sources of XRD line broadening are defect density and film stress. [36] [42] The final grain size is determined using the Scherrer formula, and the (111) diffraction peak full width at half maximum. [45]

Electrical Techniques (heterojunction interface defect density): There are many methods that can be used to extract information about the defect density. Defects can be indirectly measured by μ-PCD and modulated photoluminescence. Other techniques can involve simulation studies to extract bulk device parameters. The best qualitative measurement techniques for assessing the interface are also the most common: external and internal quantum efficiency and current-voltage. It is not always clear how to interpret these results to derive information about the heterojunction interface because it can be difficult to separate interface states from bulk states and surface states. [7] Illuminated current-voltage gives information on the recombination and trapping when performed at low temperatures and low illumination levels. Capacitance measurements are also sensitive to interface defects. Gudovskikh and Unold outline two methods of capacitance analysis: one at low temperature in the dark, and the other

with the device under illumination and forward bias. [3] [46] Several authors have noted that a large step-like increase in capacitance occurs for a defect density threshold greater than 10^{12} cm^{-2}. [47]

2   Experimental Studies on Crystallization of Thin Amorphous Silicon Films

The effect of rapid thermal annealing on thin n-type a-Si:H films deposited on Si wafers was studied by optical and electrical methods. Deposition of a-Si:H films by PECVD was optimized for high deposition rate and good film uniformity. Optical characterization was by transmission electron microscopy (TEM), Raman, ellipsometry, UV-reflectance, and defect etching followed by examination by scanning electron microscopy (SEM). Electrical characterization was by Hall Effect to examine carrier mobility, and dark current-voltage to clarify transport properties.

2.1   Optimization of Thin Doped Amorphous Silicon Films by PECVD

The conductivity, mobility, and uniformity of rapid thermally annealed amorphous silicon depends on establishing a recipe for high rate deposition of n-type a-Si:H. Optimization studies for this film were completed using Trion PECVD (13.56 MHz). The structure of the PECVD reactor is the parallel plate electrode with radial gas flow and pump for gas extraction. One electrode is grounded while the other electrode has an applied RF voltage. The system setup is shown in Figure 2.1. The grounded electrode is

heated by resistance heater. Plasma discharge occurs between the electrodes, and the deposition results depend on many variables including: temperature, pressure, gas flow rate, electrode power, and the flow rate ratio between different gases. All deposited films were doped n-type using phosphine (PH_3) diluted to 1% concentration in hydrogen (PH_3/H_2). The pressure inside the reactor determined the mean free path of gas molecules, and whether reactions occurred in the plasma or at the surface of the growing film. The gas flow rate determines the residence time of gases, and ions from the plasma may cause defect formation in the film. [48] In general, the film hydrogen content decreases with increasing substrate temperature. Defect density in the film was lowest at low RF power, low temperature (200-300°C), and high silane concentration. High silane dilution and high RF power generally produced poor films. Silane dissociates by many different reaction paths producing neutral radicals or ions (depending on the supplied RF power). Due to the small mean free path of gas molecules (10^{-3}-10^{-2} cm) there are many collisions and larger particles (mainly Si_2H_6, Si_3H_8) can be formed which has been shown to hinder film growth. [49] The concentration of radicals in the plasma is greatly affected by secondary reactions (which depend on silane concentration, radical reactivity, and concentration gradient). Highly reactive gases have a short lifetime and will likely not reach the growing surface before reacting with silane. However, one particular radical, SiH_3, does not react with silane and is very long lived. [49]
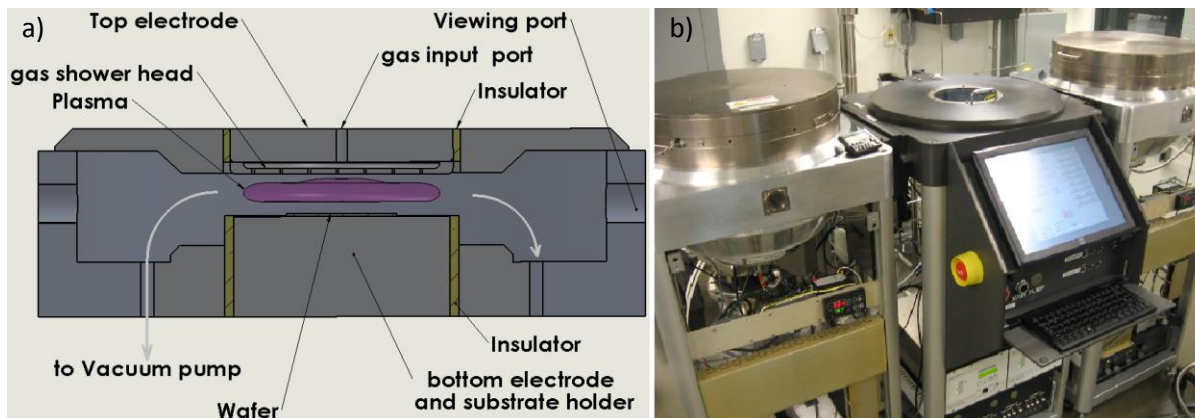
Figure 2.1: a) Cross section of PECVD Trion chamber, b) Trion system showing left side chamber for PECVD, and right side chamber for inductively coupled plasma.

For conductivity measurement, n-type a-Si:H films were deposited on glass followed by 800 nm thick aluminum contacts deposited by electron-beam evaporation using a shadow mask. Film thickness measurements to determine uniformity across the wafer were done by reactive ion etching and Dektak profiling. Before film deposition, the chamber was cleaned, walls exposed to a hydrogen plasma, and a passivating layer of a-Si:H was deposited. The cleaning recipe used was: CF_4/O_2 flow rate of 100 sccm,

pressure 300 mTorr, top electrode power 200 W, bottom electrode power 15 W, and temperature 180°C. After varying flow rates of SiH4, PH3/H2, and H2 it was determined that the best combination of high uniformity, conductivity and deposition rate for n-type a-Si:H was achieved under the following conditions: SiH4 flow rate 20 sccm, PH3/H2 flow rate 40 sccm, temperature 180°C, pressure 200 mTorr, electrode power of 5 W, deposition rate of approximately 8 nm/minute, and conductivity of 1.67×10^{-2} S/cm. Unless otherwise stated, these were the deposition conditions used for all n-type films in this work.

2.2   Sample Preparation and Thermal Profiles

For sample preparation, single side polished silicon wafers of thickness 500 µm and resistivity 0.5-0.75 Ω-cm were RCA-1 and RCA-2 cleaned, and dipped in 2% hydrofluoric acid to remove the native oxide. Wafers were immediately placed into the Trion chamber and n-type a-Si:H was deposited by PECVD. Rapid thermal annealing was performed using a ramp-up rate of 10°C/s, and plateau temperatures of 600°C, 700°C, 800°C, 900°C, and 1000°C each at three different hold times of 1, 2.5, and 5 minutes. RTA consists of three phases: ramp-up, a plateau period at fixed temperature, and cool-down. Control factors in the software were used to adjust the rate at which lamp intensity increased and control how accurately the wafer temperature followed the programmed profile. During annealing, wafer temperature was within ±1°C of the programmed thermal profile with the exception of the cool-down phase. During the cool-down, cooling rate was limited by radiation and convection and was around 150°C/minute for a nitrogen gas flow rate of 20 SLPM. A removable quartz tray with three quartz support pins was used to insert the wafer into the furnace. Temperature was measured by a thermocouple in contact with the underside of the wafer as shown in Figure 2.2 a). The interior of the RTA chamber consists of two banks of tungsten halogen lamps which uniformly illuminate the wafer from both sides (Figure 2.2 c)). The tungsten filaments radiate as a black body with a spectrum dependent on filament temperature. For temperatures between 600°C to 1100°C, the spectrum is infrared, visible, and ultraviolet and under typical processing conditions the emitted photons have a wavelength of less than 1 µm. As the filament is operated at higher temperatures, the ultraviolet portion of the spectrum will increase. During RTA, nitrogen gas was set to 20 SLPM for 2 minutes before turning on the lamps in order to purge air from the chamber. After, nitrogen flow was reduced to 3 SLPM for the remainder of the process.
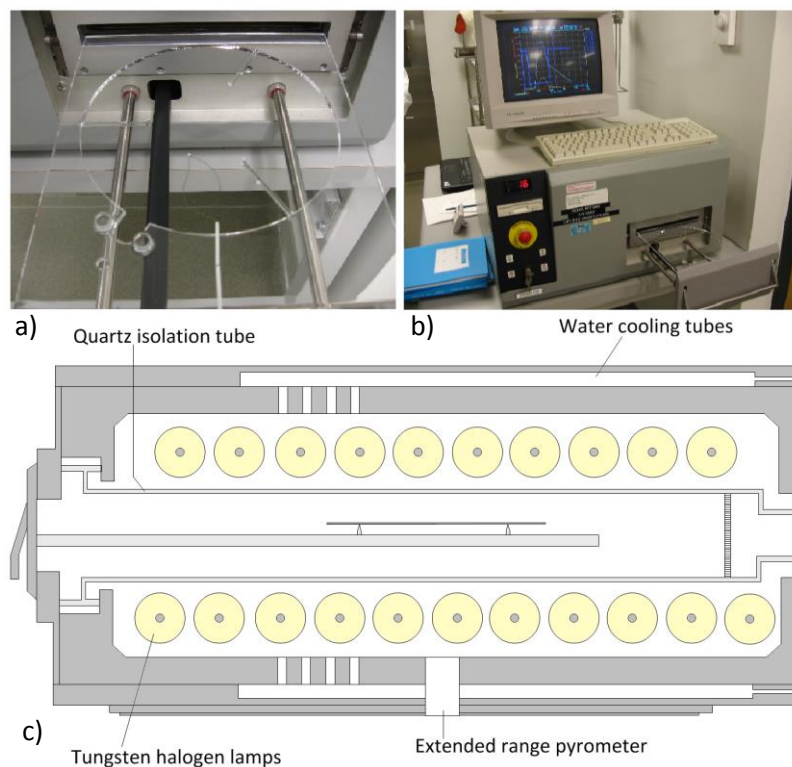
Figure 2.2: a) Quartz tray for inserting wafer into RTA chamber, b) RTP 600S system, c) cross-section of RTA chamber with quartz tray and silicon wafer.

It is typical for a-Si:H films deposited at 200°C to have a hydrogen content as high as 17 atomic %. [50] A critical problem that was encountered during RTA was the ejection of hydrogen gas from the film. Rapid thermal cycles under certain conditions caused fast and destructive out-gassing of hydrogen as the temperature of the wafer was ramped up. Hydrogen bubbles formed at the a-Si:H/c-Si interface and explosively ejected outwards through the emitter layer causing pin-hole formation which act as shunt paths in the solar cell. Numerous a-Si:H films were deposited on Si wafers in order to experiment with different RTA profiles to eliminate the pin-hole problem. In several samples the pin-holes were not immediately obvious but became evident only after the samples were processed into solar cells which exhibited very low shunt resistance. Although not solving the problem, initially it was assumed that dopant diffusion along crystal grains in the emitter was producing shunt paths and several experiments were performed to lower the phosphine flow rate to decrease the dopant concentration in the n-type layer. The next method to address pin-holes was to raise the deposition temperature for PECVD a-Si:H to reduce the hydrogen content before RTA. Films were deposited at 200°C, 250°C, 300°C, and 350°C and RTA processed using a ramp rate of 100°C/s followed by a hold at 900°C for 5 minutes. All of the films were visibly pin-holed (Figure 2.3) even when the annealing time was reduced from 5 minutes to
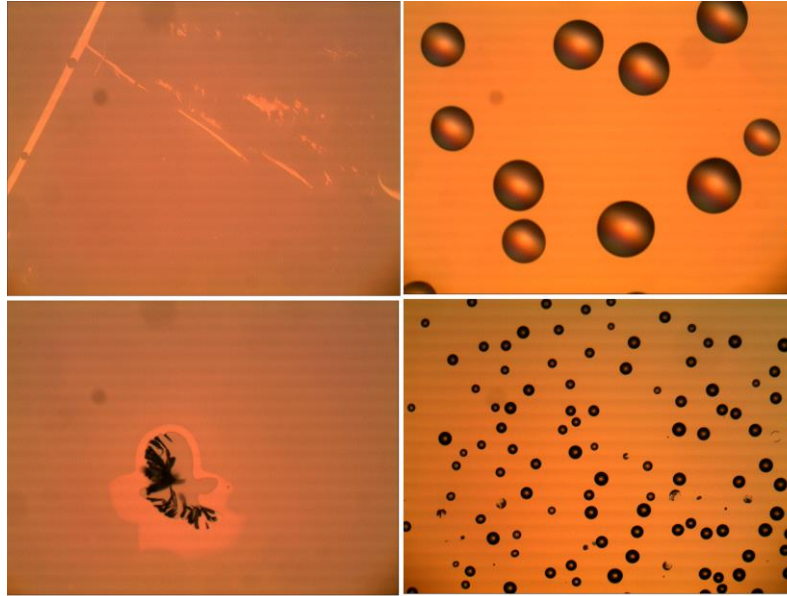
Figure 2.3: Microscope images of pin-holes and cracked RTA processed films on Si wafer using 2.5 x 10 and 10 x 10 magnification. Surface feature size is on the order of 100 μm.

30 seconds. Next, the ramp rate was maintained at 100°C/s with a 30 second annealing time but the plateau temperature was reduced from 900°C to 500°C. All films were still pin-holed. Thus, it was determined that most of the hydrogen out-gassing was happening during the ramp-up phase within the first minutes of RTA. Next, depositing a-Si:H at 200°C, four different ramp rates were used. The results are summarized in Table 2.1.

	Ramp rate			
RTA plateau	100°C/s	50°C/s	25°C/s	10°C/s
500°C	○	○	○	●
600°C	○	○	○	●
700°C	○	○	○	●
800°C	○	○	○	●
900°C	○	○	○	●
1000°C	○	○	○	●

Table 2.1: Summary of RTA thermal profiles. "○" denotes films that were pin-holed and cracked, "●" denotes films that were uniform.

Films that were RTA processed using a ramp rate of 10°C/s had pin-hole free surfaces regardless of the RTA plateau temperature. Thus, for all future RTA processes the ramp rate was fixed at 10°C/s. The hydrogen content in a-Si:H can be measured by Fourier Transform Infrared Spectroscopy (FTIR). In the infrared, a-Si:H has three absorption modes: a wagging mode centered at 640 cm^{-1}, a doublet mode at 840-890 cm^{-1} due to a dihydride bending or scissor mode, and two stretching modes at 2000-2100 cm^{-1} due to clustered monohydrides and polyhydrides. The FTIR procedure to determine the hydrogen

content in a-Si:H follows the procedure of Brodsky, Cardona, and Cuomo where hydrogen concentration, N_H, is related to the integrated absorbance of the film, I , by equation 2.1:

$$N_H = I(A/N_{si})$$

where A is a calibration constant which correlates the hydrogen content with the infrared absorption due to Si-H vibration, and $N_{si} = 5 \times 10^{22}$ cm^{-3} is the atomic density of pure silicon. [51] [52] Although FTIR measurements were made for a-Si:H and RTA processed films, the results for hydrogen percentage were ambiguous due to the extremely low film thickness of 50 nm, and light scattering from the roughened wafer back-side which reduced the transmittance signal strength. Nevertheless, based on results from literature, it can be assumed that the hydrogen content in the films after RTA was less than 1 atomic %. [53]

2.3   Transmission Electron Microscopy

In TEM, electrons are accelerated to high voltages and are focused on to the sample by condenser lenses. A diffraction pattern is formed by transmitted and forward scattered electrons and is then projected onto a fluorescent screen. The three imaging modes are bright-field, dark-field, and high resolution. In high resolution mode, several diffracted beams are combined to produce an interference image which can display features on an atomic scale.

In order to gain insight into the crystallization mechanism for RTA annealed a-Si:H, a sample that had been annealed at 750ºC for 5 minutes was thinned for TEM analysis by focused ion beam milling. Figure 2.4 shows the high resolution TEM displaying the c-Si wafer substrate and the 50 nm thick RTA processed film. The interface between the wafer and the substrate was visible as a thin region around 3-7 nm thick. The micrograph clearly showed that RTA has crystallized the a-Si:H into an epitaxial film. The crystalline atomic order of the emitter extended throughout the entire film thickness with white dots representing columns of silicon atoms. There appeared to be no random nucleation and grain growth. Epitaxy was the dominant crystallization mechanism. Although defects and the high dopant concentration in the a-Si:H film can interfere with epitaxy and promote random nucleation of crystals, the film was so thin that random grain growth was an unlikely crystallization mechanism. If the film were thicker, the gradual accumulation of defects during epitaxy might eventually lead to random grain growth. For the film studied here, RTA did not seem to affect epitaxy by causing random grain growth. Highly energetic ultraviolet photons absorbed very close to the surface of the emitter did not seem to
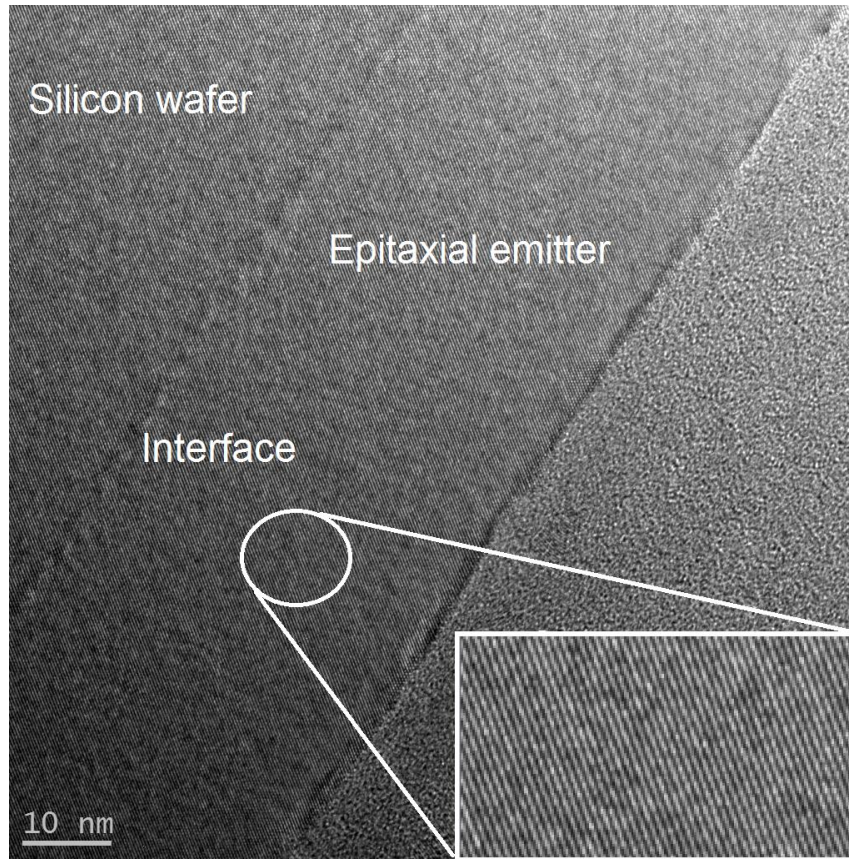
Figure 2.4: TEM showing silicon wafer and 50 nm emitter. The amorphous material deposited on top of the emitter is a carbon coating.

form nucleation sites. Although it has not been proven by further TEM studies, the result for the 750°C RTA film implied that the a-Si:H films annealed at the other temperatures in this study (600°C, 700°C, 800°C, 900°C, and 1000°C) were also epitaxial. As noted by Olsen and Roth [54], epitaxy is the dominant crystallization mechanism for films annealed in a conventional furnace at temperatures at or below 1000°C. Also, as noted by Zotov [55], the thinner the film the greater the probability that epitaxy will occur and all the films annealed in this study were only a few tens of nanometers thick. Since the ramp rate was 10°C/s, for annealing temperatures of 800°C, 900°C, and 1000°C, it was highly likely that the a-Si:H emitter had already completely crystallized by epitaxy before the plateau temperature was reached. Results for Hall Effect, UV-reflectance, and ellipsometry all showed that as the annealing temperature increased, the RTA processed films more closely approached the optical and electrical characteristics of bulk silicon. This was further evidence that epitaxy was likely maintained at higher RTA temperatures.

The micrograph in Figure 2.5 shows a closer view of the junction interface. Although the native oxide on the Si wafer was removed by a 2% hydrofluoric acid dip before PECVD, there was inevitably a

small amount of contaminant particles from the air or from the interior of the Trion chamber that may have adhered to the surface of the wafer and created trap states at the junction interface. One way to decrease interface contamination would be to remove the native oxide during PECVD. Hydrogen plasma cleaning is considered an effective way to remove native oxide and hydrocarbon contaminants on a Si surface at low temperature. [56] Removing the oxide by a hydrofluoric dip exposed the wafer to clean-room air, and the quality of the interface also depended on the purity of the etchant solution and the cleanliness of the beaker that contained it.
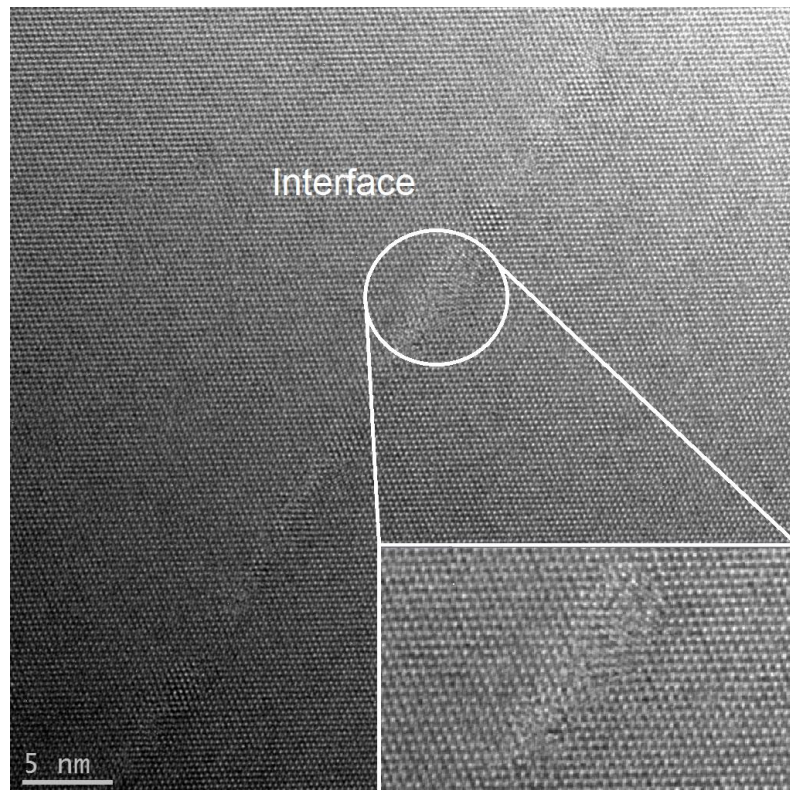
Figure 2.5: Closer examination of the heterojunction interface between p-type c-Si wafer and epitaxial RTA emitter.

2.4 Raman Spectroscopy

Many techniques can be used to assess the crystallinity of silicon films. For example, X-Ray Diffraction, UV-reflectance, Raman, and ellipsometry, are fast and non-destructive, whereas TEM, Rutherford backscattering, and ion channelling are more time consuming and expensive. [53] [55] Additional techniques include low energy electron diffraction and electron backscattering diffractometry. In Raman spectroscopy, a small fraction of incident photons (a few parts per million)

interact with the atomic lattice imparting energy by the creation of optical phonons. Such scattered photons have a down-shifted frequency referred to as Stokes shifted scattering which is detected by the photo-detector. The optical phonon energy for the crystalline silicon lattice is 0.067 eV which corresponds to a sharp Stokes spectrum (Gaussian shaped) with a peak centered around $1/\lambda = 520$ cm^{-1}. The Stokes spectrum shifts, broadens, and becomes asymmetric for grain sizes less than about 10 nm then becomes very broad for amorphous silicon which exhibits a Stokes spectrum peak around $1/\lambda = 480$ cm^{-1}. [57] Because the Stokes spectra for amorphous silicon and single crystal silicon are so different, deconvolution of the spectrum into two Gaussian curves determines the crystal volume fraction. [58] While Raman is very effective in estimating volume fraction for crystalline films of several micrometers, it was necessary to determine if it was suitable for the thin emitter layers of 50 nm or less which were required for solar cells in this research. The suitability of Raman for thin silicon films depends on the absorption depth of laser light and on the material of the substrate. Experiments were carried out comparing three different films: 600 nm a-Si:H, 50 nm a-Si:H, and 50 nm a-Si:H which had been crystallized by RTA at 800°C for 5 minutes.
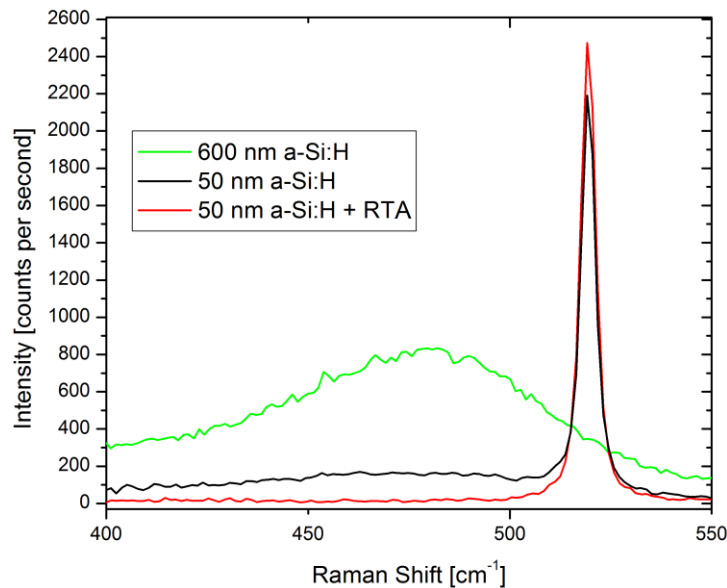
Figure 2.6: Raman spectra for three films on Si substrates. The laser intensity on the substrate was reduced to 10% of its maximum value to approximately 0.27 mW to avoid melting and crystallization of the silicon films. The beam spot size was approximately 100 μm².

All films were deposited by PECVD on the polished surface of (100) orientation Si wafers. Experiments were done using a Renishaw Mirco-Raman 1000 Spectrometer. The laser source was 488

nm Argon-Ion which was chosen over the 633 nm Helium-Neon excitation source due to smaller absorption depth. Figure 2.6 shows the Raman spectra for these three samples.

The Raman spectrum for the 600 nm a-Si:H film showed the expected broad peak at 480 cm^{-1} and no peak at 520 cm^{-1} which indicated that there was no interference from the silicon wafer. However, for the 50 nm a-Si:H there was interference from the substrate. Although there was a low intensity shoulder around 480 cm^{-1} there was also a strong peak at 520 cm^{-1} caused by photons that had passed through the amorphous layer and interacted with the silicon wafer beneath. The spectrum for the RTA crystallized film showed the disappearance of the amorphous shoulder which implied that a-Si:H had been consumed. There was a sharp peak at 520 cm^{-1} which was due both to the crystallized silicon film and the single crystal wafer beneath. It was impossible to separate these two contributions to the peak, and so calculation of the crystal volume fraction was inaccurate. The absorption depth for photons of wavelength of 488 nm in a-Si:H is approximately 61 nm, and for crystalline silicon is approximately 790 nm. [59] Thus, with 50 nm thick films, very little laser light was absorbed in the either the amorphous or the RTA crystallized layers and so Raman was therefore not a reliable method of characterization. Using thicker films was not an option because of the reduction in solar cell short-circuit current. A good alternative to Raman is UV-reflectance which operates between 200-400 nm.

2.5   UV-Reflectance

Ultraviolet reflectance is an ideal method to characterize the crystallinity of thin silicon films. The spot size is relatively large ($\approx$1 cm^2) compared to Raman ($\approx$100 um^2) and provides an area averaged indication of film crystallinity. A photo-spectrometer with integrating sphere was used to determine the total hemispherical reflectance between 200-400 nm for wafers processed by RTA at 1, 2.5, and 5 minutes annealing times at 500°C, 600°C, 700°C, 800°C, 900°C, and 1000°C. Reflectance on polished crystalline silicon shows two characteristic peaks at 365 nm and 276 nm. The peaks are a measure of the crystal quality and are related to direct optical transitions. [60] Defects and disorder associated with amorphous silicon, grain boundaries, or crystalline defects cause a broadening and a reduction in peak intensity. The absorption depth, d, for $\lambda = 400$ nm in crystalline silicon is approximately 100 nm. At 365 nm the absorption depth is $d = 11$ nm, and at 276 nm $d = 4.2$ nm. [61] Thus, for the crystalline films in this study, it was reasonable to assume that between 200-400 nm almost none of the incident light was reflected from the Si substrate. The interference from the crystalline substrate in the Raman analysis

was negligible in UV-reflectance measurements because the wavelength was lower and the deposited film was sufficiently thick.

The UV-reflectance results for all RTA samples are shown in Figure 2.7. For the samples annealed at 500°C for 1, 2.5, and 5 minutes, the reflectance data were nearly identical and so the three spectra were plotted as a single curve for clarity. At 500°C, there were no peaks at 365 nm and 276 nm which confirmed that the film was still amorphous. At 600°C and 700°C, clear peaks formed indicating a transition from amorphous to crystalline silicon, and the reflectance for 700°C was higher than for 600°C indicating a better optical quality. However, there was no discernible difference between films annealed for 1, 2.5, or 5 minutes at 600°C or 700°C.
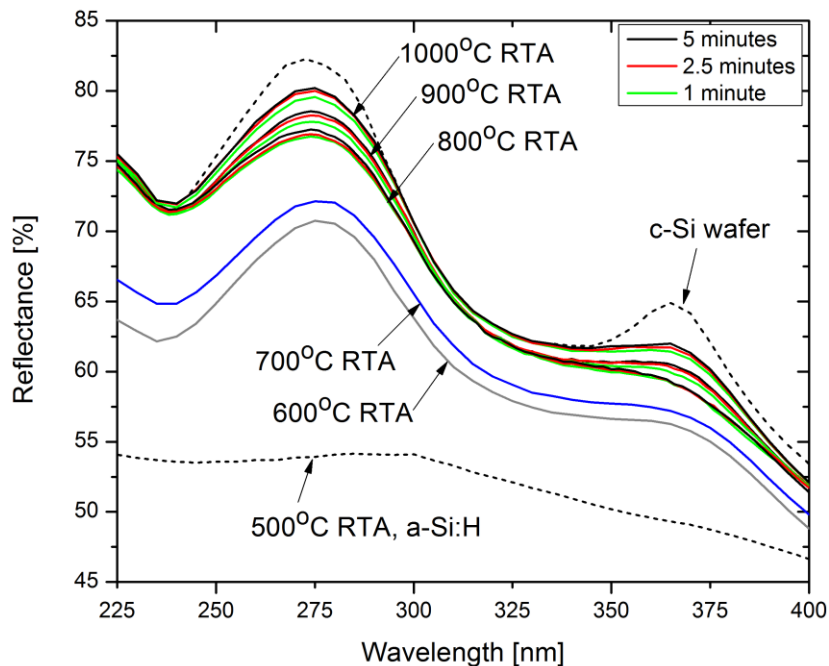
Figure 2.7: UV-reflectance for wafers with a-Si:H thin film with RTA for 1, 2.5, and 5 minute annealing times from 500°C to 1000°C.

For the a-Si:H films annealed at 800°C, 900°C, and 1000°C, there was again an increase in reflectance across the entire wavelength range, and the peak heights approached that of defect free crystalline Si. A reflectance dependence on annealing time became evident with the reflectance peak height at 800°C, 900°C, and 1000°C, increasing by approximately 2% as the annealing time was increased from 1 to 2.5 to 5 minutes. This was due to the fact that at high temperatures, RTA has the ability to anneal away crystalline defects. [62] The crystallinity of the films was qualitatively determined by comparison of the twin peak height to that of the c-Si reference. The samples annealed at 1000°C for 5

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minutes showed the best optical properties that were most similar to c-Si. Although all of the films annealed from 600°C to 1000°C were likely epitaxial, the reflectance peak heights were still clearly below those of a c-Si wafer which can be explained by the fact that the epitaxially crystallized films contained a high density of crystalline defects which caused a reduction and broadening in the peaks.

The UV reflectance spectra of thin films are not only influenced by crystallinity but also by surface roughness, particle contamination, and surface layers such as SiO$_x$. Surface roughness is believed to cause a wavelength-dependent reduction in reflectance, whereas contamination produces a uniform reduction in reflectance over the entire wavelength range [63].

2.6 Ellipsometry

Ellipsometry was used to determine the optical parameters and layer composition of the samples that had been processed by RTA. The annealing conditions are shown in Figure 2.9. Ellipsometry measures the change in polarization state of reflected light. If polarized light is reflected at the interface between two materials, the polarization state will be linear, circular, or elliptical depending on the properties of the sample. Elliptical polarization of reflected light is the most common. When plane-polarized light is incident on an absorbing material, or undergoes multiple reflections within a thin layer between the air and the substrate, both the amplitude and the phase will be altered. The phase shift creates a component that is polarized 90° to the incident beam which transforms the light from plane-polarized to elliptically-polarized. The property of light exploited by ellipsometry is the change from plane-polarized to elliptically-polarized light upon reflection. The principal variables used in ellipsometry measurements are the ellipsometric angles Ψ ($0^o \leq \Psi \leq 90^o$), and Δ ($0^o \leq \Delta \leq 360^o$) which are mathematically related to the amplitude and phase of the reflected and incident electric field of the electromagnetic wave. The variables Ψ and Δ are a measure of the differential changes in phase and amplitude that occur when incident light interacts with a surface. The optical properties of the film are determined according to the complex reflectance, $\rho = tan\Psi e^{i\Delta}$. To perform an ellipsometric measurement, the sample properties such as layer thickness and refractive index are approximated using models such as reference library materials data or dispersion formulae which allow the optical properties of the film to be calculated at each wavelength and angle of incidence. Based on the modeling, the Ψ and Δ values can be calculated from theory and then compared to the experimentally measured Ψ and Δ spectra. Next, the parameters of the model (such as film thickness, volume fractions,

or the variables in the dispersion formulae) are varied using optimization algorithms in order to minimize the difference between the measured and calculated values of Ψ and Δ. The better the agreement between theory and measurement the more accurately the model describes the layers of the actual sample. The goodness-of-fit is described by χ^2 which is a measure of the discrepancy between the experiment data and the best fit results calculated from theory. There is no clear definition of what is a "low" or "high" value for χ^2 because it is dependent on the type of film, the layer model, and the fitting conditions. As references, over the range of 1.5-5 eV, 2 nm of SiO_2 on Si gives $\chi^2 < 0.2$, 200 nm of SiO_2 on Si gives $\chi^2 < 2$, and 550 nm TiO_2 on Si gives $\chi^2 < 15$.[67] The thicker the film the greater χ^2 because the spectra have more features.

Ellipsometric measurements were performed on samples using a Horiba Joben Yvon UVSEL ellipsometer. The angle of incidence was 75°, and the wavelength range was from 250 nm to 830 nm (1.5 to 5 eV). The fitting algorithm used was the Marquardt routine, and integration time was 300 ms. Step size was 0.03 eV which was small enough to resolve spectral features (117 data points) while at the same time minimizing the collection time. Data were collected in units of electron volt. The spot size was approximately 1 x 4 mm². Before measurement, all samples were dipped in 2% hydrofluoric acid to remove any SiO_2 layer that had formed during RTA. Although the RTA chamber was purged with nitrogen before the start of annealing, there was some remaining oxygen which caused formation of SiO_2 during heating and was determined by ellipsometry to be between 4 nm to 7 nm thick. RTA formation of SiO_2 in nitrogen ambient has also been noted by Mohadjeri. [64] After RTA, a thin SiO_2 layer did form due to exposure to air but this layer was less than 2 nm thick and had little impact on optical characterizations. Although the compositions of the RTA crystallized films were assumed to be epitaxial at RTA temperatures of 600°C and above, UV-reflectance analysis has shown that these films are defective. Several different models were used incorporating grain boundaries, amorphous silicon, and nanocrystalline silicon to approximate the defective states in the epitaxial emitter. The four models are shown in Figure 2.8. Model a) assumed defect-free solid phase epitaxy from the c-Si substrate. Model b) consisted of fine grained nanocrystalline silicon (nc-Si). Model c) assumed a two layer structure consisting of a-Si:H and c-Si in the bottom layer, and a-Si, c-Si, and voids in the top layer which was a surface roughness layer. The a-Si:H c-Si mixture is a common method of modeling nanocrystalline silicon for ellipsometry. Model d) was identical to model c) except the a-Si:H in both layers was replaced by nc-Si. For the surface roughness layer, it was assumed that the feature size was less than the wavelength of light so that it was possible to define an average refractive index. All of the optical property data for the film components were taken from reference library data (crystalline silicon from [65], amorphous silicon

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from [66], and nanocrystalline silicon from [61]). No dispersion formulae were required. In the fitting routine, the software was set to vary both the film thicknesses and percentage composition of a-Si:H, c-Si, nc-Si, and voids. The substrate was assumed to be infinitely thick, and because it was back-side roughened reflections from the back were neglected.
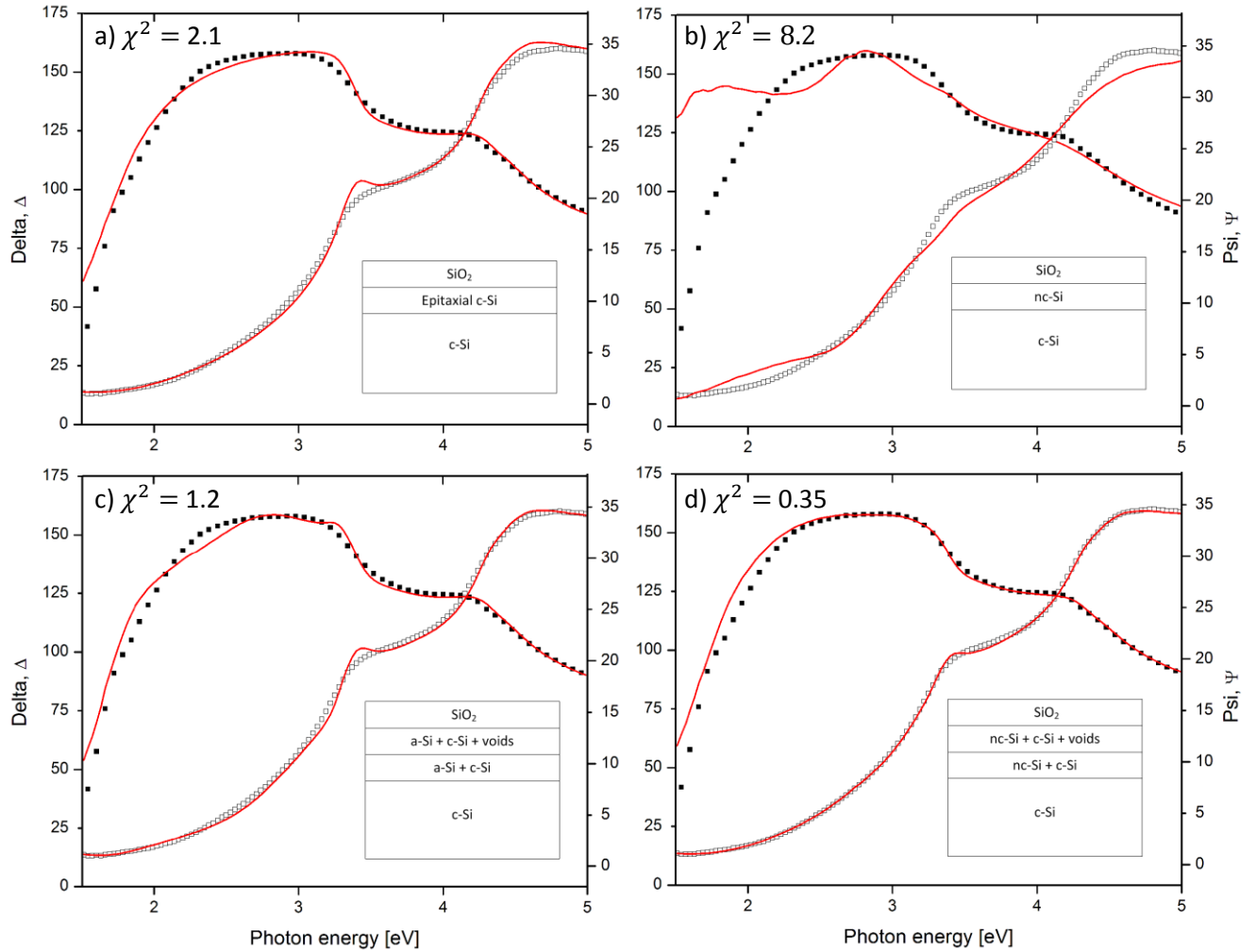
Figure 2.8: □ denotes Psi, ■ denotes Delta, — denotes theoretically calculated values of Delta and Psi based on the layer material assumptions shown in the inset of each graph. This model comparison is for an RTA sample annealed at 900°C for 5 minutes. However, for all of the other samples annealed above 500°C, model d) consistently gave the lowest χ^2.

For layers consisting of several materials, the Bruggeman effective-medium-approximation was used to calculate the dielectric function. The approximation assumes a homogeneous distribution and combines the independent dielectric functions of the host materials with corresponding volume fractions. The layer is macroscopically homogeneous but microscopically heterogeneous on a length

scale between 1 nm to 1 μm. [67] In Figure 2.8, the model which gave the best fit to the data for RTA films processed at or above 600°C was the model consisting of a combination of nc-Si, c-Si, and a surface roughness layer containing voids. For samples annealed at 500°C, model d) gave a very poor fit to the data because these films were still highly amorphous. In this case, a model consisting of the silicon substrate, an a-Si:H layer, and a capping layer of SiO₂ gave the best fit with $\chi^2 = 0.57$ to $\chi^2 = 0.63$ for annealing times of 1, 2.5, and 5 minutes.

A measure of crystallinity is provided by the square of the refractive index which is the dielectric function $\varepsilon = \varepsilon_r + i\varepsilon_i$ composed of real and imaginary parts. The dielectric function is dependent on electronic band structure. The imaginary component, ε_i , is directly related to the joint density of electronic states by two critical point peaks at 3.5 eV and 4.2 eV which are dependent on changes in crystalline atomic order. [68] Figure 2.9 shows the real and imaginary components of the dielectric function for n-type a-Si:H films RTA processed from temperatures of 500°C to 1000°C for annealing times of 1, 2.5, and 5 minutes. Ellipsometer sensitivities to changes in dielectric function in silicon can be as low as 10⁻³. However, the difference in dielectric function between amorphous, nanocrystalline, and single crystal silicon shown in Figure 2.9 was very large. The sensitivity in ε_i was particularly high around the critical point energy peak at 4.2 eV where the difference was greater than 10. The dielectric function is related to the properties of the crystalline film by effective medium theory. The effective medium theory assumes that the film is composed of a homogeneous mixture of phases that are large enough to retain their bulk properties but smaller than the wavelength of ellipsometric light thus avoiding scattering. For a mixture of two materials consisting of dielectric functions ε_a and ε_b a generalized form of the effective medium theory, the Bruggeman effective-medium-approximation, is used to calculate the effective dielectric function, ε_f, which is given by equation 2.2.

$$0 = f_a \frac{\varepsilon_a - \varepsilon_f}{\varepsilon_a + 2\varepsilon_f} + f_b \frac{\varepsilon_b - \varepsilon_f}{\varepsilon_b + 2\varepsilon_f} \tag{2.2}$$

The model fit parameters are the volume fractions of the two materials, f_a and f_b, where ε_a and ε_b are known and ε is calculated by altering f_a and f_b. For wavelengths greater than 3 eV, light did not penetrate the emitter film, and so the dielectric function was representative of the emitter layer modified only slightly by surface layers such as roughness and native oxide. The crystallinity of the measured films was defined by the "position" of the real and imaginary components of the dielectric function between the upper and lower limits of crystalline silicon and amorphous silicon. In the visible
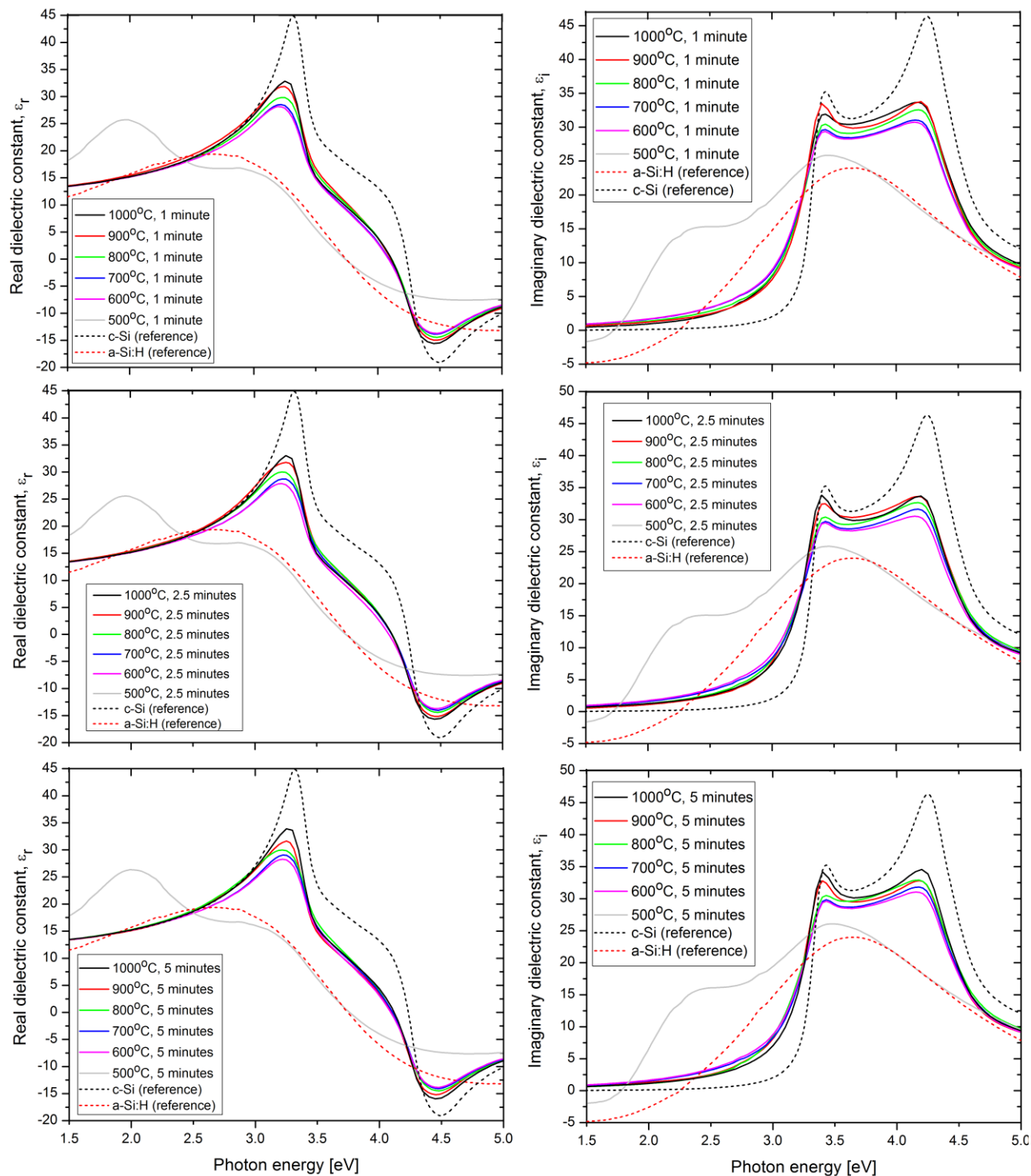
Figure 2.9: Ellipsometry results for RTA annealed a-Si:H films for annealing periods of 1, 2.5, and 5 minutes. RTA annealing temperatures were from 500°C to 1000°C. The dotted lines indicate reference optical parameters for c-Si and a-Si:H taken from the Horiba Jobin Yvon materials properties library.

Annealing temperature	Layer 1: (nc-Si + c-Si)	Layer 2: Surface roughness (c-Si + nc-Si + voids)	Layer 3: Surface oxide, SiO$_2$
600°C, 1 min $\chi^2 = 1.16$	Thickness: 27.4 ± 2.7 nm c-Si: 85.2 ± 4.5 % nc-Si: 14.8 %	Thickness: 10.4 ± 1.0 nm c-Si: 48.0 ± 3.7 % nc-Si: 47.5 ± 3.5 % Voids: 4.5 %	Thickness: 1.7 ± 0.1 nm
700°C, 1 min $\chi^2 = 0.97$	Thickness: 27.0 ± 2.3 nm c-Si: 84.0 ± 4.2 % nc-Si: 16.0 %	Thickness: 10.7 ± 1.0 nm c-Si: 50.1 ± 3.2 % nc-Si: 45.9 ± 3.2 % Voids: 4 %	Thickness: 1.7 ± 0.1 nm
800°C, 1 min $\chi^2 = 1.2$	Thickness: 27.9 ± 3.5 nm c-Si: 88.1 ± 4.8 % nc-Si: 11.9 %	Thickness: 10.8 ± 1.2 nm c-Si: 54.9 ± 3.7 % nc-Si: 42.1 ± 3.6 % Voids: 3 %	Thickness: 1.5 ± 0.1 nm
900°C, 1 min $\chi^2 = 0.7$	Thickness: 24.6 ± 2.7 nm c-Si: 89.1 ± 2.8 % nc-Si: 10.9 %	Thickness: 10.8 ± 0.8 nm c-Si: 45.8 ± 3.0 % nc-Si: 51.2 ± 2.1 % Voids: 3 %	Thickness: 1.6 ± 0.1 nm
1000°C, 1 min $\chi^2 = 0.58$	Thickness: 34.5 ± 5.4 nm c-Si: 94.4 ± 3.2 % nc-Si: 5.6 %	Thickness: 9.3 ± 0.8 nm c-Si: 62.0 ± 2.8 % nc-Si: 36 ± 0.5 % Voids: 2%	Thickness: 2.0 ± 0.5 nm
Annealing temperature	Layer 1: (nc-Si + c-Si)	Layer 2: Surface roughness (c-Si + nc-Si + voids)	Layer 3: Surface oxide, SiO$_2$
600°C 2.5 min $\chi^2 = 0.9$	Thickness: 26.3 ± 2.2 nm c-Si: 83.9 ± 4.1 % nc-Si: 16.1 %	Thickness: 11.2 ± 1.0 nm c-Si: 49.6 ± 3.1 % nc-Si: 46.3 ± 3.1 % Voids: 4.1 %	Thickness: 1.8 ± 0.1 nm
700°C 2.5 min $\chi^2 = 0.9$	Thickness: 25.5 ± 2.0 nm c-Si: 83.1 ± 4 % nc-Si: 16.9 %	Thickness: 11.8 ± 1.1 nm c-Si: 52.2 ± 3.0 % nc-Si: 44.0 ± 3.1 % Voids: 3.8 %	Thickness: 1.6 ± 0.1 nm
800°C 2.5 min $\chi^2 = 1.2$	Thickness: 28.5 ± 3.6 nm c-Si: 88.9 ± 4.7 % nc-Si: 11.1 %	Thickness: 10.5 ± 1.0 nm c-Si: 52.6 ± 3.6 % nc-Si: 44.7 ± 3.6 % Voids: 2.7 %	Thickness: 1.5 ± 0.1 nm
900°C 2.5 min $\chi^2 = 0.43$	Thickness: 33.3 ± 8.9 nm c-Si: 96.2 ± 3.7 % nc-Si: 3.8 %	Thickness: 8.2 ± 0.9 nm c-Si: 63.6 ± 4.2 % nc-Si: 34.6 ± 3.8 % Voids: 1.8 %	Thickness: 2.1 ± 0.1 nm
1000°C 2.5 min $\chi^2 = 0.56$	Thickness: 34.5 ± 5.4 nm c-Si: 94.4 ± 3.1 nm nc-Si: 5.6 %	Thickness: 9.3 ± 0.8 nm c-Si: 62.0 ± 2.8 % nc-Si: 36 ± 2.1 % Voids: 2.0 %	Thickness: 1.6 ± 0.1 nm
Annealing temperature	Layer 1: (nc-Si + c-Si)	Layer 2: Surface roughness (c-Si + nc-Si + voids)	Layer 3: Surface oxide, SiO$_2$
600°C 5 min $\chi^2 = 0.81$	Thickness: 25.4 ± 1.9 nm c-Si: 82.8 ± 3.7 % nc-Si: 17.2 %	Thickness: 11.7 ± 1.0 nm c-Si: 50.0 ± 2.8 % nc-Si: 46.2 ± 2.8 % Voids: 3.8 %	Thickness: 1.7 ± 0.1 nm
700°C 5 min $\chi^2 = 0.91$	Thickness: 26.0 ± 2.0 nm c-Si: 82.7 ± 4 % nc-Si: 17.3 %	Thickness: 11.4 ± 1.1 nm c-Si: 52.1 ± 3.1 % nc-Si: 44.2 ± 3.1 % Voids: 3.7 %	Thickness: 1.5 ± 0.1 nm
800°C 5 min $\chi^2 = 0.99$	Thickness: 29.1 ± 5.1 nm c-Si: 92.7 ± 4.4 % nc-Si: 7.3	Thickness: 11.0 ± 0.8 nm c-Si: 51.5 ± 3.2 % nc-Si: 46.7 ±3.2 % Voids: 1.8 %	Thickness: 1.5 ± 0.1 nm
900°C 5 min $\chi^2 = 0.35$	Thickness: 25.2 ± 4.5 % c-Si: 89.5 ± 3.2 % nc-Si: 10.5 %	Thickness: 10.1 ± 1.5 % c-Si: 63.4 ± 3.0 % nc-Si: 35.9 ± 2.9 % Voids: 0.7 %	Thickness: 1.9 ± 0.1 nm
1000°C 5 min $\chi^2 = 0.56$	Thickness: 34.5 ± 5.4 nm c-Si: 94.4 ± 3.1 % nc-Si: 5.6 %	Thickness: 9.3 ± 0.8 nm c-Si: 62.0 ± 2.8 % nc-Si: 36.0 ± 3.0 % Voids: 2.0 %	Thickness: 1.6 ± 0.1 nm

Table 2.2: Summary of RTA film characteristics for 1, 2.5, and 5 minute RTA.

and ultraviolet part of the spectrum, the main influence on the dielectric function is the electric polarizability which is due to the bonding configuration, short-range and long-range atomic order, and density. [69] Figure 2.9 shows the imaginary dielectric function for a-Si:H, which had no long-range order, and only a single peak around 3.5 eV. By contrast, crystalline silicon had perfect long-range order and exhibited peaks in ε_i at 3.4 eV (E_1 transition) and 4.2 eV (E_2 transition). Both amorphous and crystalline silicon are homogeneous on a length scale of 1nm – 1 µm. However, nanocrystalline silicon is inhomogeneous in this scale. The ε_r and ε_i spectra for the films annealed between 600°C, and 1000°C were very similar to the nc-Si dielectric spectra reported in literature. Thus, although the RTA processed films were epitaxial, their dielectric spectra similarity to nanocrystalline silicon implied that the epitaxial films were defective. Figure 2.9 showed that as the RTA temperature was increased, ε_r and ε_i became closer to that of single crystal silicon. However, there was a significant difference between 500°C and 600°C film. The dielectric transition from amorphous to epitaxial phases occurred quite suddenly.

Using model c) consisting of a-Si:H, c-Si, and voids to describe defective epitaxial Si did not result in a good fit at the E_1 and E_2 transition points for ε_i. The inadequacy of model c) to simulate the defective emitter may be due to difficulty the software encounters when trying to use amorphous silicon to account for the presence of crystalline defects. Model d) gave the best fit because the defective sites in the epitaxial layers were better modeled by the grain boundaries present in nanocrystalline silicon. The dielectric peaks at 3.4 eV for both ε_r and ε_i in the epitaxial films were believed to be due to direct optical transitions [70] and an interaction between heavy doping effects and the influence of crystal grain size on the density of states. [71] [59] The percentage composition of the two layers using the nc-Si + c-Si + voids model is given in Table 2.2 for all annealing temperatures.

Taking an average of the percentage compositions for nc-Si and c-Si for the three different annealing times at each RTA temperature, the average crystallinity was plotted in Figure 2.10. As the annealing temperature was increased, the percentage of c-Si in both Layer 1 and Layer 2 increased while the percentage of nc-Si decreased. This implied that at higher annealing temperature there was an annealing away of crystalline defects (in agreement with the results from UV-reflectance). The percentage composition results were consistent with the trends in dielectric constant towards increasing crystallinity as the RTA temperature increased (Figure 2.9). Another feature was that the c-Si content in Layer 1 was much larger than the c-Si content in Layer 2. There was a thickness-dependent increase in nc-Si percentage. This provided insight into the growth mechanism. It implied that epitaxial crystallization had a relatively low defect density near the c-Si interface (where the nc-Si volume fraction

was smallest) and epitaxy became progressively more defective further away from the interface (where the nc-Si volume fraction was larger).
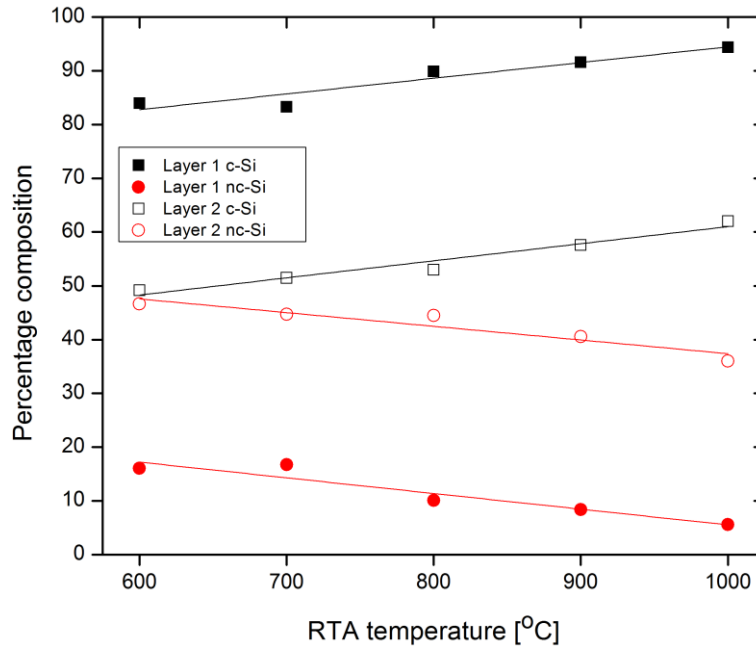
Figure 2.10: Average crystallinity for RTA films processed at plateau annealing times of 1, 2.5, and 5 minutes.

2.7 Defect Etching and Scanning Electron Microscopy

Defect etches are typically used to reveal the size, type and density of defects on a semiconductor surface. By an etch-pitting process, the defect etch will make defects visible by creating a variety of etch patterns as a result of surface features such as dislocations or stacking faults. All defect etches have a common chemistry consisting of an oxidizing agent, a fluoride to dissolve silicon dioxide, and a dilution component such as acetic acid or water. Common oxidizing agents are nitric acid, hydrogen peroxide, and particularly chromium compounds like CrO_3, and $K_2(Cr_2O_7)$.

The Secco etch is often used to reveal grain boundaries and defects in polycrystalline silicon in order to determine crystal grain size. Secco etch is based on a dilute solution of HF and $K_2(Cr_2O_7)$. [72] Other defect etching solutions introduced in the sixties and seventies such as Schimmel [73], Wright [74], Yang [75], Seiter [76], MEMC [77], and Dash [78] etch are also used. However, while the above recipes are well adapted to defect etches on Si wafers they are very difficult to apply to thin Si films only a few tens of nanometers thick. For this work, the Dash and Secco etch were attempted but difficulties

were encountered with non-uniform etch removal, and in some cases complete etching away of the film. Due to the relatively high etching rates of μm/min, exposure times of only a few seconds were necessary which made the etching procedure unreliable. In order to overcome these difficulties, an organic peracid etch recently introduced by Kolbesen and Possner [79] was used called OPE-A. The mixture consists of acetic acid (100%, 143 ml), hydrofluoric acid (50%, 14.5 ml), and hydrogen peroxide (30%, 43 ml). The reaction proceeds with acetic acid and hydrogen peroxide forming peracetic acid according to equation 2.3.

$$CH_3COOH + H_2O_2 \Longrightarrow CH_3COOOH + H_2O \qquad (2.3)$$
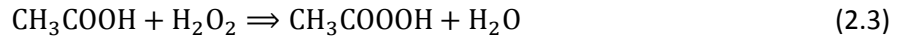
Peracetic acid is the active species and oxidizes silicon according to equation 2.4. After oxidation, silicon dioxide is dissolved by hydrofluoric acid according to equation 2.5.

$$Si + 2CH_3COOOH \Longrightarrow SiO_2 + 2CH_3COOH \qquad (2.4)$$

$$SiO_2 + 6HF \Longrightarrow H_2SiF_6 + 2H_2O \qquad (2.5)$$
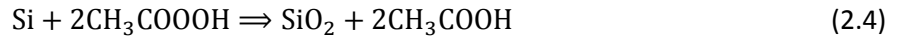
The etch rate of OPE-A is determined by the concentration of hydrogen peroxide and peracetic acid whereas the concentration of hydrofluoric acid will affect the diameter of the etch pits. The advantage of the OPE-A recipe is its homogeneous etching and low removal rate of 0.6 nm/min at 25°C. [79] For comparison, a diluted Secco etch has a removal rate a factor of 100 greater than OPE-A. In addition, OPE-A is found to be 10-20 times more sensitive to defects than Secco. For this work, OPE-A was prepared according to the above recipe, but was only used after a period of 24 hours in order to give enough time for the formation of a sufficient quantity of peracetic acid (3 mol/L). Samples with an n-type 50 nm thick a-Si:H film that had been RTA processed at 750°C were dipped in OPE-A for 40 minutes in order to etch approximately half way through the film. Etching was performed at room temperature without physical agitation. Before OPE-A, samples were etched in 2% hydrofluoric acid to remove surface oxide. Samples were analyzed by SEM and the results are shown in Figure 2.11.

Etch pit formation is governed by many factors including strain fields in the film, the presence of impurities such as metals, and crystal defects which occur within crystal grains and grain boundaries. OPE-A has been shown to have very high etching selectivity between defect-free and defective regions of the crystal lattice. [80] As OPE-A etched through the films, regions containing crystallographic defects and impurities were etched faster than relatively low defect concentration areas. The SEM analysis was complicated by the fact that the film contained voids. Nevertheless, at higher magnifications of 75,000 and 150,000, surface features became visible. As was shown earlier, at 750°C the film emitter was
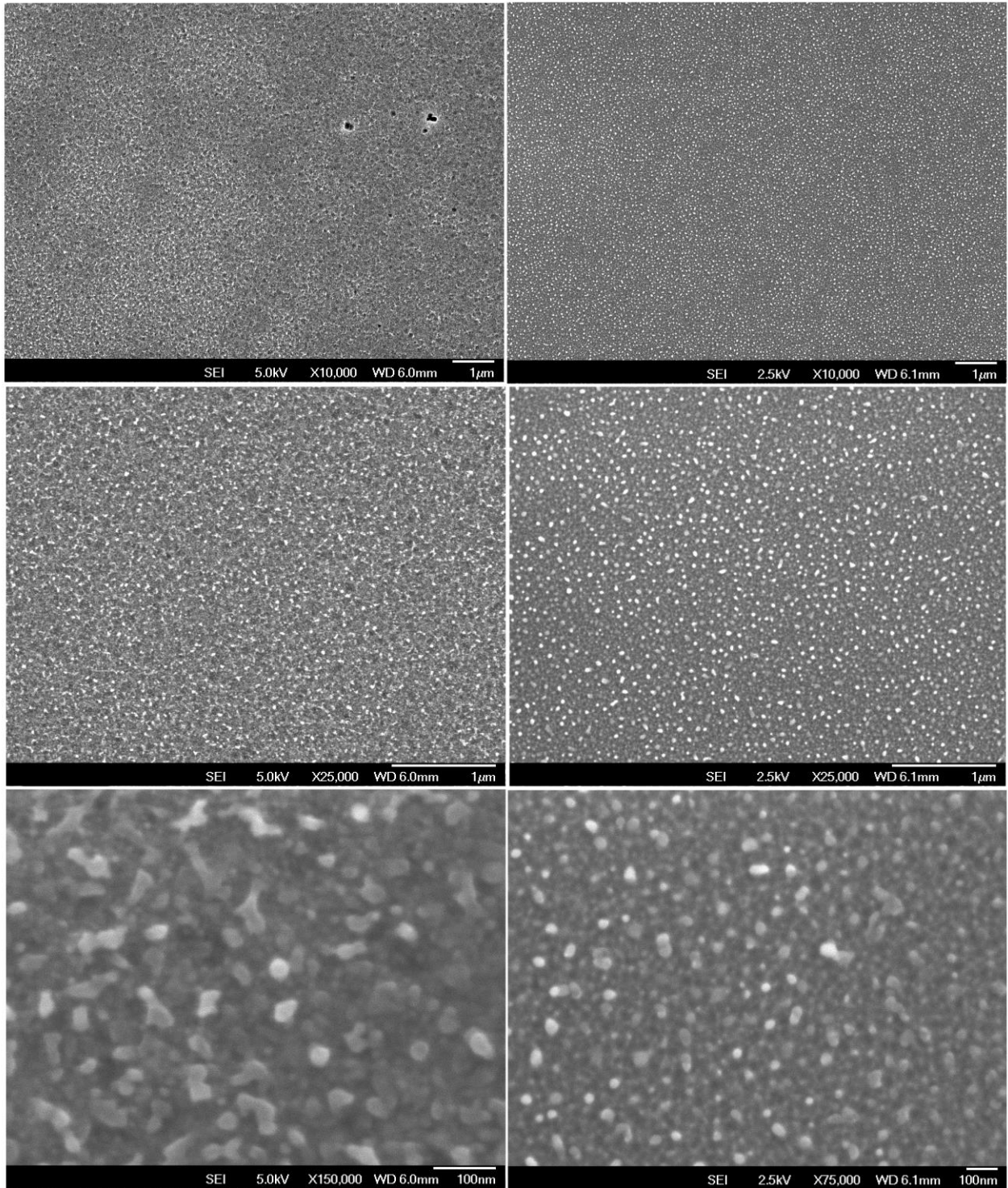
Figure 2.11: OPE-A of RTA processed sample. N-type a-Si:H annealed at 750ºC for 5 minutes. OPE-A etch was 40 minutes.

epitaxial. However, the OPE-A etched film surface was highly pitted and irregular which indicated that there was a high density of defect centers where the etch rate was increased relative to less defective crystalline areas. Some areas of the film appeared to be relatively smooth and defect free and these regions could be seen at the highest magnifications of 75,000 and 150,000. The SEM images reinforced the results of TEM, UV-reflectance, and ellipsometry which indicated that the crystalline emitters were epitaxial but also defective.

2.8 Hall Effect

Hall Effect measurements were performed using an Ecopia 3000 HMS system at room temperature. The Hall Effect applies a magnetic field perpendicular to the direction of current flow. The magnetic field exerts a Lorentz force causing a deflection and accumulation of mobile charge carriers resulting in a downward electric field which balances the Lorentz force (the Hall Field). For a known magnetic field, film thickness, current flow, and Hall voltage, the resistivity, carrier density, and Hall mobility are calculated. Wafers processed by RTA at 1, 2.5, and 5 minute annealing times at 500°C, 600°C, 700°C, 800°C, 900°C, and 1000°C were diced into 1.5 x 1.5 cm^2 squares and aluminum contacts were deposited by e-beam evaporation at the corners of each sample using a shadow mask. The contact area of each of the four pads was approximately 0.75 mm^2. The magnetic field strength was 0.54 T. A magnetic field reversal was made in order to cancel any unbalanced voltage due to the contacts not being exactly opposite to one another. Readings were averaged (100 measurements at each field direction).

The results for Hall mobility and resistivity for each RTA condition is shown in Figure 2.12. The software required the film thickness which was input from earlier ellipsometry measurements. There was a sharp increase in mobility from 500°C to 600°C, which was in agreement with the optical analysis showing that at 500°C the film was still amorphous whereas at 600°C it was crystalline. At 600°C and 800°C, mobility gradually increased with annealing time. While the results at 700°C did not show a clear dependence on annealing time, the overall trend of increasing mobility at higher temperatures was clear. Particularly at temperatures of 900°C and 1000°C, increased mobility was evident as the annealing time was increased. The highest mobility was achieved at 1000°C for 5 minutes with $\mu_n = 67.2 \pm 0.6$ cm^2/Vs. The phosphorous dopant concentration for these devices was approximately 10^{20} cm^{-3}. At room temperature, mobility was likely limited by a combination of impurity scatter, lattice scatter, and

scattering at defects. For single crystal silicon with an identical doping concentration at 300 K, the mobility is approximately 90 cm^2/Vs which is the upper limit that the RTA mobility cannot surpass. [81] As the RTA plateau temperature increased, increasing mobility was likely due to the annealing away of defects in the epitaxial layer. Micro-twins are a commonly observed defect and can act as scattering centres. Micro-twin defects are unstable, and it has been shown that their density can be drastically reduced with RTA annealing temperatures at or above 750°C. [62]
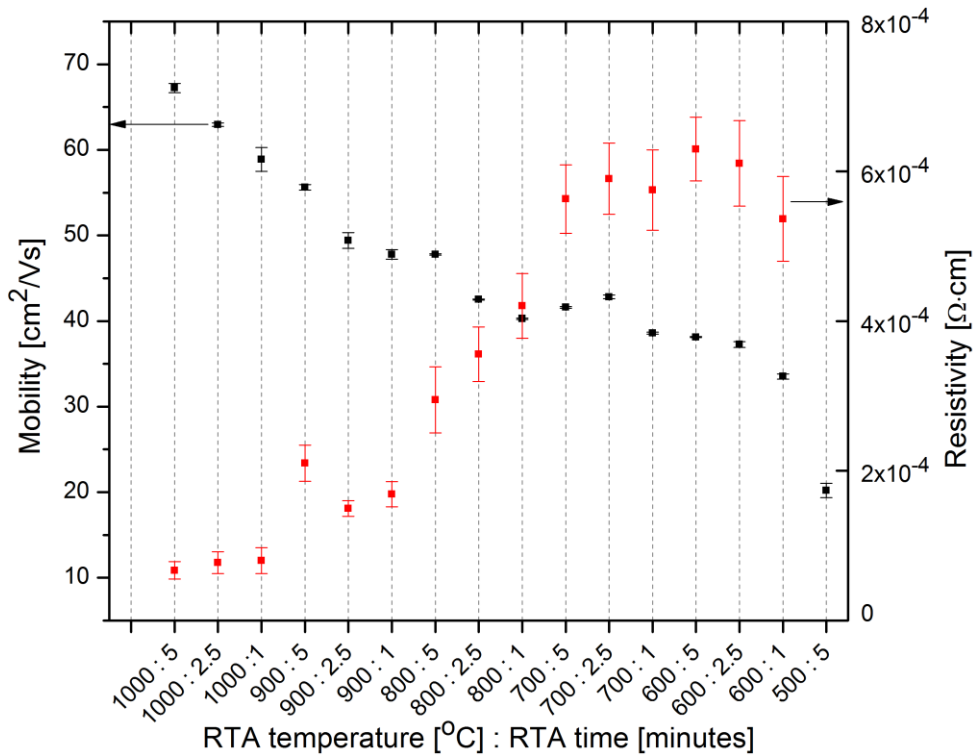
Figure 2.12: Hall Effect measurement for RTA processed samples.

Not all of the samples followed the trend of increasing mobility with higher annealing temperatures and this was due to measurement uncertainties and variability between samples. For thin films on substrates of opposite conductivity type, the active film thickness was not necessarily the same as the total film thickness due to depletion effects caused by surface charges and band bending at the interface with the substrate. This affected the Hall coefficient. It was also assumed that the doping concentration, and thus the mobility and resistivity, were uniform throughout the film thickness which was not exactly the case as is shown by spreading resistance profiling in Chapter 4. Lastly it was assumed that the samples satisfy the van der Pauw conditions: symmetrical point contacts located at the

periphery, and no pinholes in the film. In this way, device parameters could be determined without knowing the current pattern.

2.9   Diode Transport Properties: Dark Current-Voltage Characteristics

Diodes were made on 4 inch diameter p-type silicon wafers (7-10 Ω cm). Wafers were RCA-1 and RCA-2 cleaned, followed by deposition of an n-type a-Si:H film on the polished surface by Trion PECVD. The thickness of the deposited films was approximately 50 nm. Samples were RTA processed at 600°C, 700°C and 800°C for 5 minutes. Front and back contacts were deposited by electron-beam evaporation of aluminum. Photolithography followed by lift-off was used to define square contacts of four different areas: 0.25 x 0.25 mm², 0.5 x 0.5 mm², 2 x 2 mm² and 1 x 1 cm². Mesa etching was performed using Trion Phantom reactive ion etcher to electrically isolate all diodes by removing the emitter using gases O_2 and SF_6. Etching conditions were: DC power 40 W, O_2 flow rate of 3 sccm, SF_6 flow rate of 22 sccm, pressure of 50 mTorr, and etching time of 60 seconds. A Dektak surface profiler was used to measure the step height which indicated that approximately 450 nm of silicon had been etched.

The transport of charge carriers across the heterojunction is fundamental to understanding device operation. Dark I-V measurement as a function of temperature is a well established method to examine transport characteristics. Compared to transport in p-n homojunctions, transport in heterojunctions is complicated by: conduction and valence band offsets which act as charge transport barriers, trap states at the heterojunction interface, dipole layers, and discontinuous material properties. Anderson first described heterojunction transport paths in Ge-GaAs [82], and since then a wide variety of transport mechanisms have been identified. Despite several groups presenting analytical expressions for device currents [83], there is currently no universal analytical model that accounts for all transport paths. Several paths may be present simultaneously. The two most common transport mechanisms in a typical diode are diffusion-limited transport in the neutral bulk, and recombination occurring in the space charge region. Recombination or diffusion may be present particularly in the low forward bias region ($V_a < 0.4$ V) where an exponential relationship exists between current and applied voltage as given by equation 2.6:

$$I = I_s(exp[\beta V] - 1) \tag{2.6}$$

where I_s is the saturation current, and recombination or diffusion within the depletion region are identified by the temperature dependent exponent, β, according to equation 2.7.

$$\beta = q/nkT \tag{2.7}$$

The ideality factor, n, indicates whether the dominant transport mechanism is diffusion or recombination. If the diffusion of carriers across the junction is the dominant transport mechanism then the ideality factor is near $n = 1$. If transport is controlled by recombination in the depletion region then $n = 2$. Two other important transport mechanisms in heterojunctions are thermionic currents and tunneling. Thermionic currents occur when charge carriers have sufficient energy to be transported over a band offset spike. Under low forward bias, tunneling current may exceed diffusion or thermionic emission currents by several orders of magnitude. To account for tunneling currents, models of Multi-tunneling Capture Emission (MTCE) are used to account for numerous defect states in the band gap. Charge carriers can tunnel into the band gap via defect states, and even migrate between valence and conduction bands. To summarize these various transport mechanisms, Schulze's depiction of transport pathways in a typical p-n heterojunction is reproduced in Figure 2.13. [84]
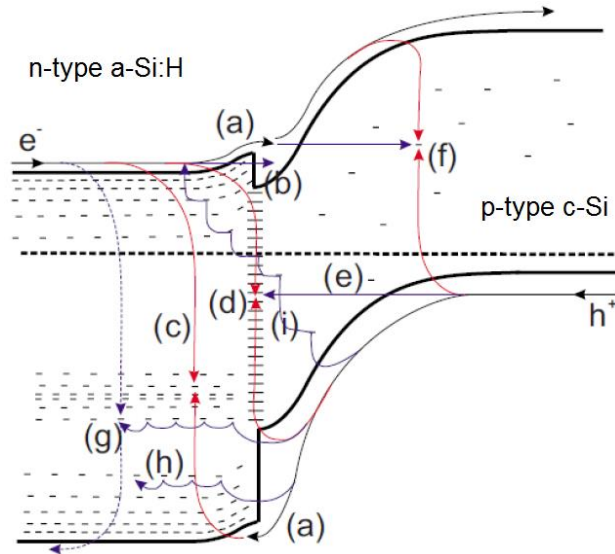
Figure 2.13: Depiction of various transport mechanisms in a n⁺p a-Si:H / c-Si solar cell. The heterojunction is at thermal equilibrium. Transport pathways shown are: a) emission of carriers across a band spike created by the conduction band offset, b) tunneling through a band spike, c) recombination of an electron and a hole at an a-Si:H energy state in the forbidden gap, d) recombination occurring via states at the amorphous/crystalline interface, e) tunneling into interface states followed by hopping to higher energy interface states, f) recombination via deep defects in the crystalline substrate, g) multi-tunneling through successive capture and re-emission, h) tunneling followed by hopping to various defect states in the band tail of amorphous silicon, i) band-to-band multi-tunneling process.

Dark I-V measurements, shown in Figure 2.14, were made at 30°C, 60°C, 90°C, and 120°C using a Cascade Microtech probe station with thermally controlled Temptronic 3000 chuck with an accuracy of ±1°C. The voltage bias range was divided into three regions: reverse bias, low forward bias $(V_a < 0.6$ V), and high forward bias $(V_a > 0.6$ V). In the reverse bias regime, all samples showed an increase in reverse

saturation current with temperature which was due to thermally induced generation (drift) current with the number of thermally generated electron hole pairs increasing with device temperature.

Figure 2.15 shows the ideality factors for diodes from the three annealed wafers. There was a clear temperature dependence for all of the ideality factors meaning that tunneling was not the dominant transport mechanism (tunneling has a temperature independent ideality factor). For all three annealed wafers, the ideality factors increased with decreasing temperature, remaining within bounds of approximately $1 < \eta < 2$. At the highest temperatures (90°C, 120°C) the ideality factors approached unity demonstrating that the high temperature zone was limited by diffusion current. In contrast to diffusion dominated current, at a temperature of 60°C, current was controlled by a mixture of both diffusion and recombination, as given by the ideality factors around 1.5. In the lower temperature zone,
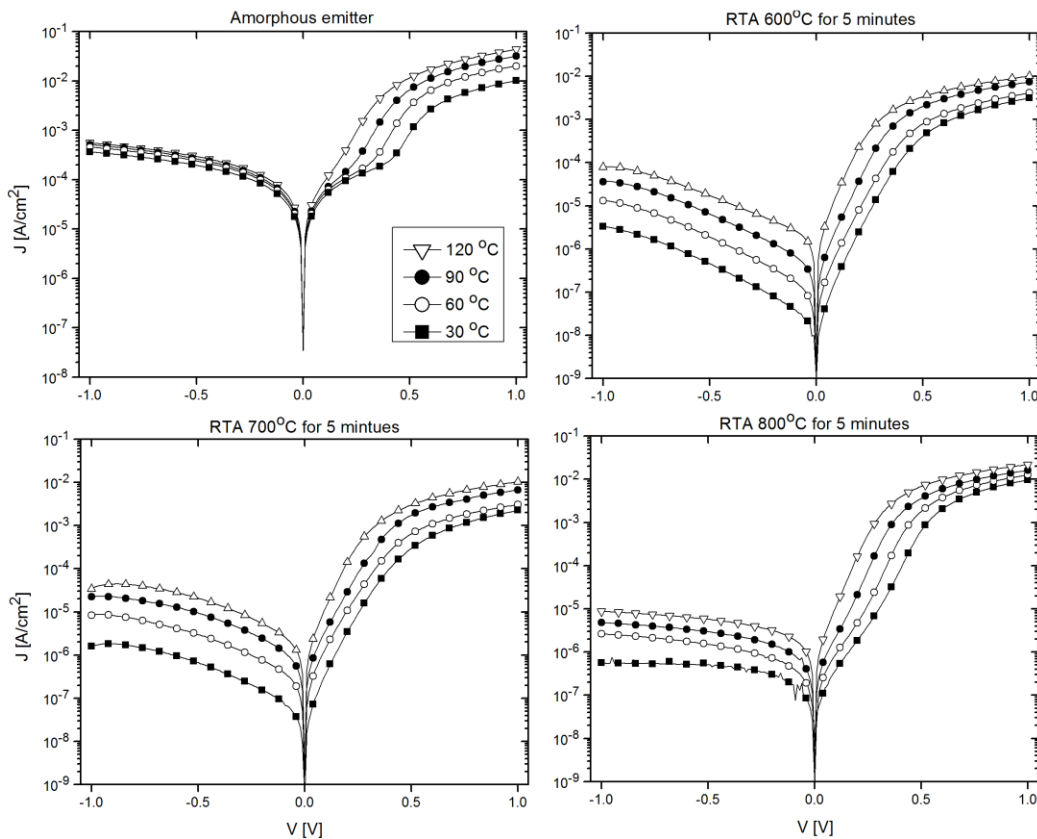
Figure 2.14: Dark current-voltage curves for four diode types with reverse bias sweep.

30°C, recombination current became the dominant transport mechanism as the ideality factors approached $\eta = 2$. The temperature-dependence of the ideality factor also meant that thermionic current transport may be present, but more experiments are required to determine whether it is comparable to the diffusion/recombination current.
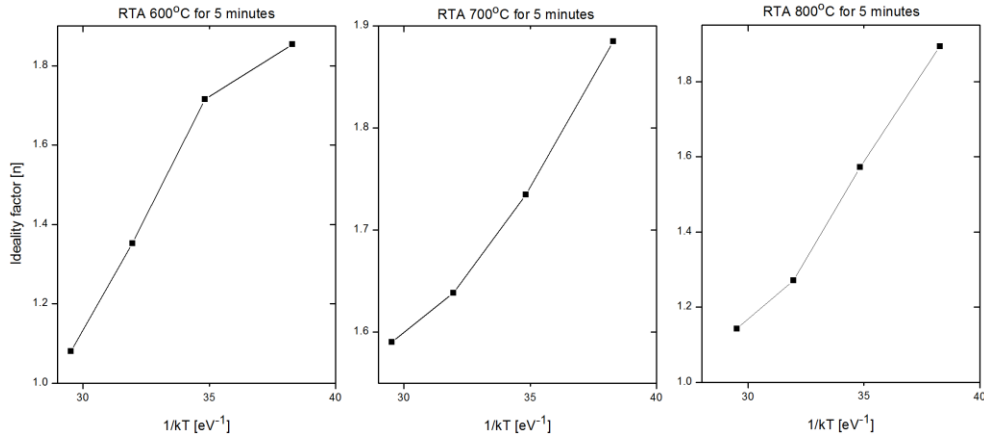
Figure 2.15: Temperature dependence of ideality factor for RTA annealed films at measurement temperatures of 30°C, 60°C, 90°C, and 120°C.

2.10 Conclusions

Optical and electrical characterization of RTA processed films showed good agreement. Films annealed at 500°C were amorphous, whereas films annealed between 600°C to 1000°C appeared epitaxial but defective as indicated by UV-reflectance, ellipsometry, and Hall Effect. Due to the defect density of the epitaxial layers, they were best modeled by ellipsometry not as a perfect crystalline film but as a homogeneous distribution of crystalline and nanocrystalline silicon. The RTA epitaxial films had a large enough defect concentration that their UV-reflectance and ellipsometry dielectric function curves were very similar to those of nanocrystalline silicon seen in literature. [63] [68] Hall Effect measurements confirmed that RTA films with good optical quality (near to that of c-Si) were also of good electrical quality. As RTA temperature increased, mobility of RTA films approached that of bulk silicon. Analysis of heterojunction transport mechanisms showed that carrier tunneling was not significant.

3 Simulations of Heterojunction Photovoltaic Cells with Crystalline and Amorphous Thin Films

In chapter 2, it was shown that solid phase crystallization of amorphous silicon on c-Si produced epitaxial but highly defective crystalline films. Ellipsometry results indicated that the epitaxial films were best modeled as a mixture of crystalline and nanocrystalline silicon. Because nanocrystalline silicon has defective grains and grain boundaries, it was used in this chapter to simulate the defective epitaxial emitter. This was a reasonable approximation particularly because RTA epitaxial films had a large enough defect density that their UV-reflectance and ellipsometry dielectric function curves were very similar to those of nanocrystalline silicon seen in literature. [85] [86] In order to better understand solar cell performance, simulations were performed to compare cells with three types of emitters: defect-free epitaxial silicon (epi-Si), nanocrystalline silicon (nc-Si), and a-Si:H (on Si wafer). The cell structures are shown in the inset of Figure 3.2. A model was established for the defect distribution at the heterojunction interface. Simulation was used to examine the optical and electrical properties of different emitter layers, and the influence of interface defects on solar cell open-circuit voltage.

3.1   Simulation Settings and Solar Cell Thermal Equilibrium Band Structure

All simulations were performed using heterojunction simulation software AFORS-HET version 2.4.1 from Helmholtz-Zentrum Berlin. AFORS-HET is capable of simulating heterostructures with ultra-thin layers of several nanometers on top of thick c-Si wafers (300 μm). An arbitrary number of layers can be simulated with user-specified distributions of defects within the bandgaps. Different models for the

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transport of charge across interfaces such as drift-diffusion or thermionic emission are available. The software models the steady-state of the heterostructures by solving three one-dimensional coupled nonlinear partial differential equations: Poisson`s equation (equation 3.1) and hole and electron continuity equations (equations 3.2 and 3.3):

$$\nabla \cdot \varepsilon \vec{E} = q(p - n + N_D - N_A + N_T) \tag{3.1}$$

$$\nabla \cdot \vec{J_p} = q(G_L - R_p) \tag{3.2}$$

$$\nabla \cdot \vec{J_n} = q(R_n - G_L) \tag{3.3}$$

where n and p are the electron and hole concentrations, J_n and J_p are the electron and hole current densities, G_L is the optical generation rate, R_n and R_p are the electron and hole recombination rates, N_T is the net charge of all the traps located in the bandgap, N_A and N_D are the acceptor and donor concentrations, and ε is the electric permittivity of the semiconductor. Recombination is modeled by Auger, direct band-to-band, and Shockley-Read-Hall recombination. Finite difference methods are used to discretize the equations on user-defined grid points. Using the appropriate boundary conditions, the semiconductor equations are iteratively solved to obtain carrier concentrations and electric potential at each grid point from which other device parameters can be computed.

For the simulation of the silicon wafer, the parameters are well established. In AFORS-HET, the dopant concentration and defect density of the wafer was required and the rest of the parameters were determined by various models as can be found in other solar cell simulation software such as PC1D. The impurities present in the wafer (mainly oxygen, carbon and transition metals) were modelled as
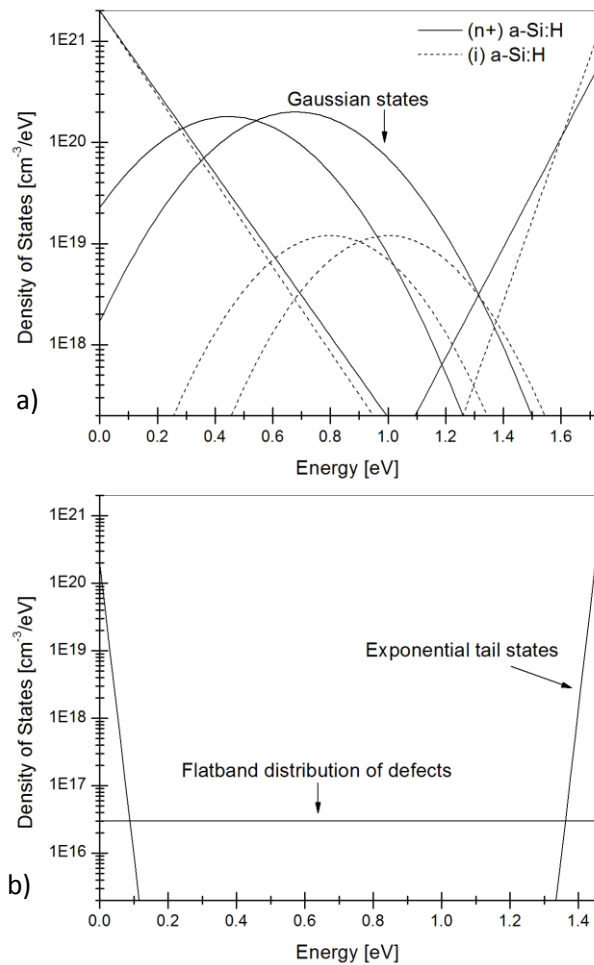
Figure 3.1: a) Density of states for a-Si:H, b) density of states for nc-Si.

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a single Shockley-Read-Hall defect state in the bandgap with temperature and doping dependent recombination. Models were implemented for bandgap narrowing, and charge carrier mobility. Auger recombination was calculated according to the model of Kerr and Cuevas [87]. More complicated was the simulation of amorphous and nanocrystalline silicon. As shown in Figure 3.1, for a-Si:H the defect states within the band gap were described by exponential tail states and Gaussian dangling bond states. For nc-Si, the exponential tail states had a steeper slope, and the Gaussian dangling bond states were replaced by a linear (constant) distribution of mid-gap states divided into donor-like states and acceptor-like states characterized by a switch-over energy half way through the bandgap. [88] Table 3.1 shows the electrical properties of each emitter type. For the nanocrystalline emitter, Table 3.1 also shows electrical characteristics for grain boundaries between crystal grains. Properties for the defective layer at the heterojunction interface (further discussed in section 3.2) are shown as well.

Figure 3.2 shows the equilibrium band diagrams for each of the three cell types as well as the cell structure. Because of the thin emitter layer, all three cells had an 80 nm thick ZnO layer to enhance lateral conductivity. The
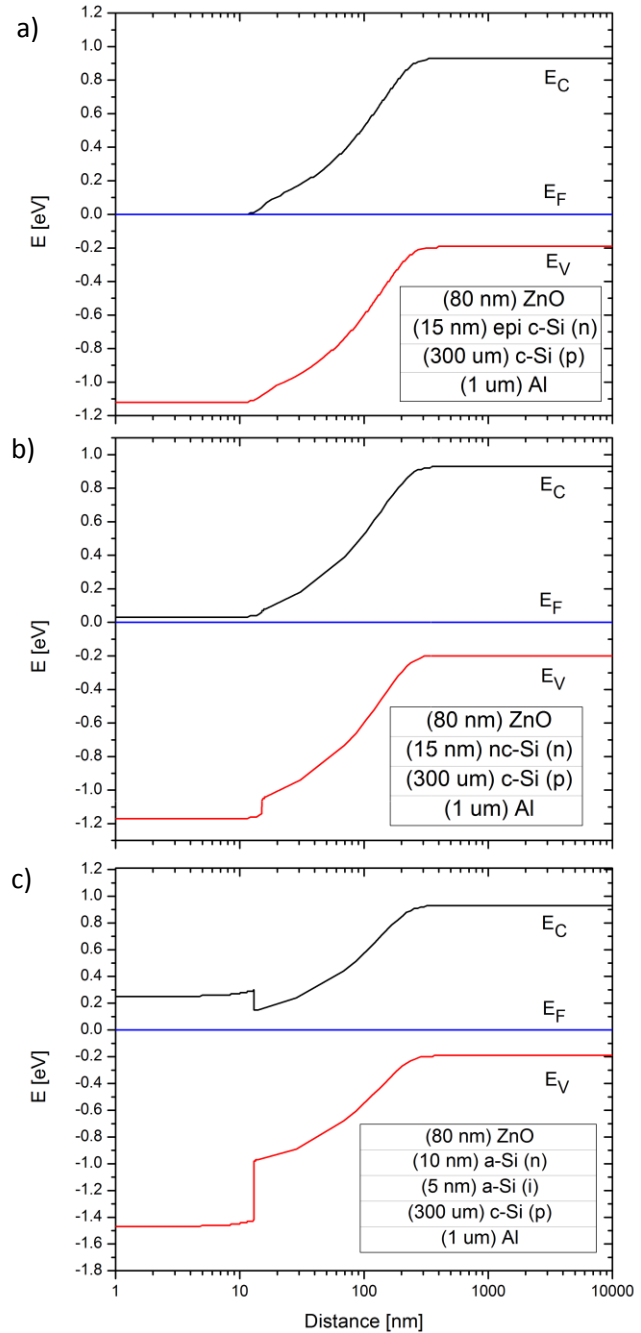
Figure 3.2: Band diagrams under thermal equilibrium for solar cells consisting of the following three emitters: a) epitaxial, b) nanocrystalline, and c) amorphous silicon. The various device layers are shown in the inset.

Fermi energy was set to zero. At the front and back cell contacts, a flat-band condition was specified with a high surface recombination velocity (10^7 cm/s). The cell surface was flat and the reflectance was assumed to be 20% which was typical for non-textured wafers. [88]

Parameters and units (e and h for electrons and holes respectively)	Epi-Si (n) (Epitaxial)	nc-Si (n) (Nanocrystalline)	a-Si:H (n) (Amorphous)	Polycrystalline grain boundary	Defective interface layer
General electrical properties					
Dielectric constant [--]	11.9	11.9	11.9	11.9	11.9
Electron affinity [eV]	4.11	4.05	3.9	4.05	4.05
Band gap [eV]	1.12	1.2	1.72	1.12	1.12
Effective density of states in the CB [cm^{-3}]	9.2×10^{18}	3×10^{19}	1×10^{20}	2.8×10^{19}	2.8×10^{19}
Effective density of states in the VB [cm^{-3}]	8.7×10^{18}	2×10^{19}	1×10^{20}	1.04×10^{19}	2.7×10^{19}
Electron mobility [cm^{2}V^{-1}s^{-1}]	123.6	40	20	1	1041
Hole mobility [cm^{2}V^{-1}s^{-1}]	160.4	4	5	1	413
Ionized acceptor concentration [cm^{-3}]	0	0	0	0	1.5×10^{16}
Ionized donor concentration [cm^{-3}]	9×10^{18}	9×10^{18}	7.32×10^{19}	9×10^{18}	0
Thermal velocity of holes [cm/s]	1×10^7	1×10^7	1×10^7	1×10^7	1×10^7
Thermal velocity of electrons [cm/s]	1×10^7	1×10^7	1×10^7	1×10^7	1×10^7
Layer density [g cm^{-3}]	2.33	2.33	2.33	2.33	2.33
Effective minority carrier diffusion length [nm]	4000	20	5	----	----
Band tail parameters					
Valence band tail donor-like states [cm^{-3}eV^{-1}]	----	2×10^{20}	2×10^{21}	1×10^{21}	----
Valence band tail capture cross section, e [cm^{-2}]	----	1×10^{-15}	7×10^{-16}	1×10^{-15}	----
Valence band tail capture cross section, h [cm^{-2}]	----	1×10^{-17}	7×10^{-16}	1×10^{-17}	----
Valence band tail Urbach energy [eV]	----	0.01	0.094	0.049	----
Conduction band tail acceptor-like states [cm^{-3}eV^{-1}]	----	2×10^{20}	2×10^{21}	1×10^{21}	----
Conduction band tail capture cross section, e, [cm^{-2}]	----	1×10^{-17}	7×10^{-16}	1×10^{-17}	----
Conduction band tail capture cross section, h, [cm^{-2}]	----	1×10^{-15}	7×10^{-16}	1×10^{-15}	----
Conduction band tail Urbach energy [eV]	----	0.01	0.068	0.021	----
Gaussian distribution parameters					
Gaussian acceptor-like states [cm^{-3}eV^{-1}]	----	----	1.3×10^{20}	5×10^{16}	----
Maximum energy of acceptor Gaussian [eV]	----	----	0.6	0.49	----
Width of acceptor Gaussian [eV]	----	----	0.21	0.18	----
Acceptor-like capture cross section, e, [cm^{-2}]	----	----	3×10^{-15}	1×10^{-15}	----
Acceptor-like capture cross section, h, [cm^{-2}]	----	----	3×10^{-14}	1×10^{-14}	----
Gaussian donor-like states [cm^{-3}eV^{-1}]	----	----	1.3×10^{20}	5×10^{16}	----
Maximum energy of donor Gaussian [eV]	----	----	0.5	0.63	----
Width of donor Gaussian [eV]	----	----	0.21	0.18	----
Donor-like capture cross section, e [cm^{-2}]	----	----	3×10^{-14}	1×10^{-14}	----
Donor-like capture cross section, h [cm^{-2}]	----	----	3×10^{-15}	1×10^{-15}	----
Flat band distribution parameters					
Density of donor-like midgap states [cm^{-3}eV^{-1}]	----	3×10^{16}	----	----	8.9×10^{16}-8.9×10^{22}
Donor-like capture cross section, e [cm^{-2}]	----	1×10^{-14}	----	----	1×10^{-14}
Donor-like capture cross section, h [cm^{-2}]	----	1×10^{-15}	----	----	1×10^{-14}
Density of acceptor-like midgap states [cm^{-3}eV^{-1}]	----	3×10^{16}	----	----	8.9×10^{16}-8.9×10^{22}
Acceptor-like capture cross section, e, [cm^{-2}]	----	1×10^{-15}	----	----	1×10^{-14}
Acceptor-like capture cross section, h, [cm^{-2}]	----	1×10^{-14}	----	----	1×10^{-14}
Switch over energy [eV]	----	0.6	----	----	0.56

Table 3.1: List of layer parameters used in solar cell simulation with AFORS-HET. Effective minority carrier diffusion lengths were from R. Stangl [88]. Nanocrystalline materials properties were from AMPS 1-D materials library. [89] All other materials properties were from the AFORS-HET materials library.

There was a band gap offset exhibited at the junction interface for the nc-Si and a-Si:H heterojunctions while the epi-Si structure showed no offset. Because the bandgap of nc-Si was so close to that of crystalline silicon, the offset was small compared to the a-Si:H heterojunction. For any heterojunction solar cell, the bandgap of the emitter will affect the band gap offset, recombination, and

built-in potential [90]. Large bandgap offsets can be used to selectively control the transport of carriers across the junction. The bandgap of the emitter material is important for minimizing recombination losses in the emitter to improve the cell efficiency. Figure 3.3 shows the band diagram of an n$^+$p heterojunction with wide band gap (n$^+$) a-Si:H emitter.
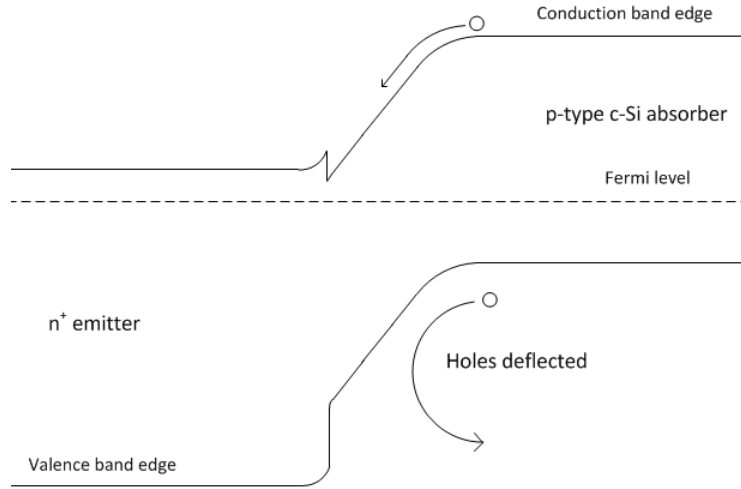
Figure 3.3: Heterojunction solar cell band diagram at thermal equilibrium.

Light-induced minority carriers produced in the absorber are swept by the junction into the opposite region where they become majority carriers and are collected at the contacts. Majority carriers that are injected into the opposite region become minority carriers and a source of recombination which reduces cell efficiency. For a wide bandgap heterojunction solar cell, as shown in Figure 3.3, the large barrier to majority carrier holes travelling towards the emitter reduces the number of holes that enter the emitter and recombine. [91] Ideally, the entire band offset between the two layers is entirely in the valence band. However, real heterojunctions will have offsets in both valence and conductions bands. The band spike in the conduction band will hinder the collection of electrons, but if the spike is small the charge carriers will pass through by tunneling, trap assisted tunneling, or thermionic emission. The improvement in cell efficiency for a wide bandgap emitter layer can also be seen in equation 3.4 which is the emitter component of the dark saturation current.

$$I_E = qA\frac{n_i^2}{N_D}\frac{D_P}{L_P}\left[\frac{D_P/L_P sinh[(W_N-x_N)/L_P]+S_{F,eff}cosh[(W_N-x_N)/L_P]}{D_P/L_P cosh[(W_N-x_N)/L_P]+S_{F,eff}sinh[(W_N-x_N)/L_P]}\right] \tag{3.4}$$

$$n_i = \sqrt{N_C N_V}e^{-E_G/2kT} \tag{3.5}$$

From equation, 3.5, a wide bandgap emitter has a significantly smaller intrinsic carrier concentration which will reduce the emitter component of the dark saturation current, and thus reduce the net

recombination in the emitter. The bandgap of the emitter is also important in order to act as a window layer. Photons with energy less than the bandgap will pass through the emitter and be absorbed in the Si wafer rather than near the front surface where recombination in a homojunction cell would be high.

3.2   The Effect of Heterojunction Interface States on Solar Cell Performance

The efficiency of a heterojunction solar cell depends critically on the defect density at the junction interface. Interface defects can consist of dangling bonds, or molecules that have been adsorbed onto the surface after the wafer cleaning procedure or during film deposition. Transport across the heterojunction interface is modeled by creating a thin defective layer between the p-type and n-type semiconductors. The modelling of the interface is complicated and many assumptions are required. For example, the thickness of the defective layer is not precisely known (although estimations in the nanometer range are common). [92] The trap cross-section area for electrons and holes within the defective layer is difficult to measure but was estimated to be 10^{-14} cm^{-2}. [93] The defective layer is likely present both on the emitter side and within the crystalline silicon absorber. However, such a scenario is difficult to implement in the simulation. It was

Figure 3.4: Density of states for 3 nm thick defective interface layer with a defect density concentration of 1 x 10^{10} cm^{-3}eV^{-1}.

assumed here that the defective layer was entirely on the side of the crystalline silicon and had a band gap of 1.12 eV with a doping density identical to that of the wafer substrate. The interface defect density was divided into two regions (Figure 3.4). The donor-like dangling bond states were in the lower half of the c-Si bandgap and the acceptor-like states were in the upper half, separated by a switchover energy, E_{DA}, approximately half way through the band gap. The total density of states per unit area at the interface was D_{it}. The interface states were modeled according to equation 3.6, where x_o was the thickness of the defective layer and G_{MGD} and G_{MGA} were the constant donor-like and acceptor-like states per unit volume per unit energy, respectively.

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$$D_{it} = [G_{MGD}(E_{DA} - E_V) + G_{MGA}(E_C - E_{DA})]x_o \tag{3.6}$$

Assuming the density of donor-like and acceptor-like states were equal, equation 3.6 simplified to equation 3.7:

$$D_{it} = G_{MGD}(E_C - E_V)x_o = G_{MGD} \cdot E_G \cdot x_o \tag{3.7}$$

where E_g is the bandgap of the defective layer. In order to study the effect of D_{it} on cell performance, D_{it} was varied between 10^{10} to 10^{16} cm^{-2} for all three emitter types. The results are shown in Figure 3.5.
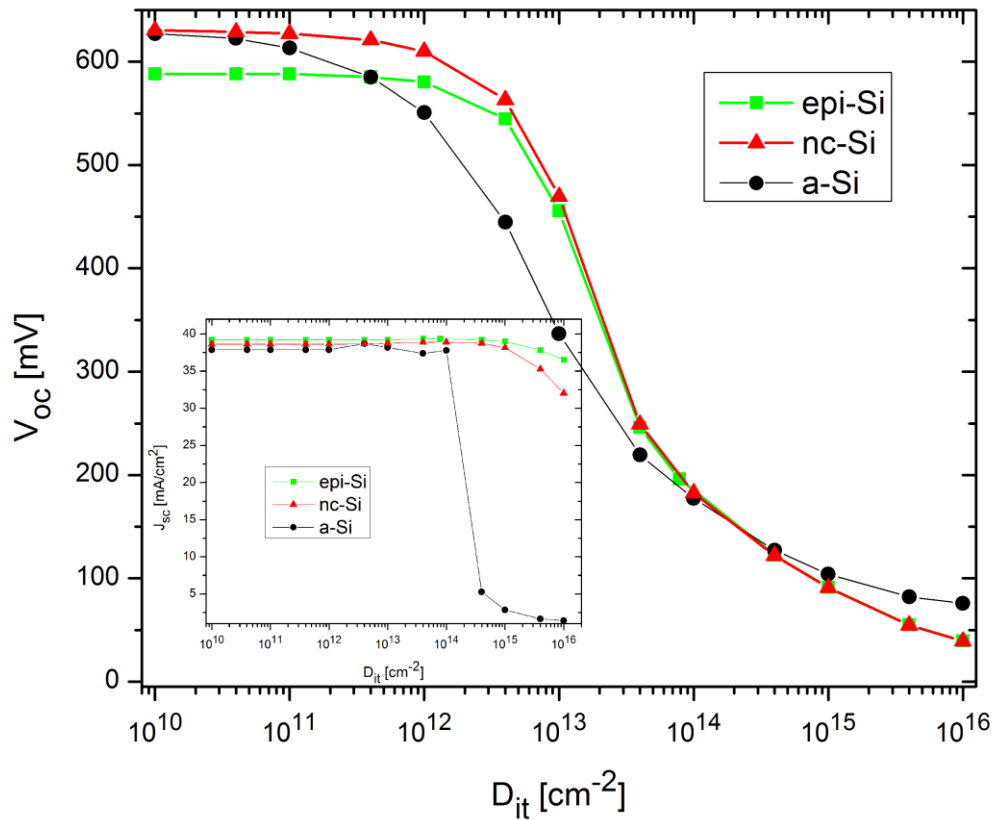
Figure 3.5: Dependence of open-circuit voltage, V_{oc}, on defect density at the heterojunction interface. Short-circuit current, J_{sc}, versus D_{it} is shown in the inset. The defective interface layer was assumed to be 3 nm thick and entirely on the c-Si side.

From Figure 3.5, solar cell V_{oc} was extremely sensitive to interface defects for defect densities greater than a threshold of around 10^{12} cm^{-2}. The D_{it} threshold was approximately the same for epitaxial, nanocrystalline, or amorphous emitter layers. By contrast, solar cell J_{sc} (shown in the inset graph) was relatively insensitive to D_{it}, and remained nearly constant even for very large defect densities up to 10^{14}

cm^{-2}. All three emitter types exhibited the same dependence between J_{sc} and D_{it} for the defect density concentrations typical of high efficiency heterojunction solar cells (where D_{it} does not exceed 10^{12} cm^{-2}).

3.3   Influence of the Emitter: Light Absorption and Density of States

Because a-Si:H is a direct band gap semiconductor, whereas epitaxial and nanocrystalline silicon are indirect, an a-Si:H emitter has a significantly higher absorption coefficient than nc-Si or epi-Si over a wavelength range of approximately 350-800 nm. Figure 3.6 a) shows the absorption coefficients of a-Si:H, nc-Si, and epi-Si as a function of wavelength. Thus, a-Si:H absorbed more light than nc-Si or epi-Si in spite of its larger band gap. Comparing the defect densities within the three emitter layers, the epi-Si emitter has significantly fewer defects. From literature, the defect density for highly doped n-type a-Si:H, nc-Si, and epi-Si was approximately 10^{18} cm^{-3}, 10^{17} cm^{-3} and 10^{13} cm^{-3} respectively. [88] The maximum hole minority carrier diffusion length in epi-Si was around 4000 nm. Charge carriers produced in the epi-Si emitter (for example by the absorption of ultraviolet light) will be able to reach the electrodes and contribute to the photocurrent. For nc-Si, the minority carrier diffusion length was substantially lower (20 nm) but minority carriers produced in the emitter should be able to reach the contacts if the emitter is less than 20 nm thick. The a-Si:H emitter was highly defective so the minority carrier diffusion length was only 5 nm. Thus, charge carriers generated in a-Si:H will not contribute to the photocurrent. The minority carrier diffusion lengths were calculated by AFORS-HET based on the electrical parameters and distribution of states in the gap. The values were approximate because they did not take into account the energetic location of defects within the gap (for example defects located at the midgap tend to be more effective as recombination centres than defects located close to the band edges). However, if an intrinsic buffer layer of a-Si:H or nc-Si is added between n-type and p-type materials, charge carriers produced in the buffer will contribute to the total current and be collected by the built-in electric field of the n-i-p structure. Furthermore, the activation energy of the dark conductivity of a-Si:H (defined as the energetic difference between $E_C - E_F$) is limited to values greater than 200 meV. However, the activation energies for nc-Si and epi-Si junctions (as shown in the band diagrams of Figure 3.3) approached zero. This meant that the band bending and built-in potential could be greater in nc-Si and epi-Si than a-Si:H heterojunctions.

The optical and electrical quality of the three emitters was also examined by Internal Quantum Efficiency (IQE). The IQE is defined as the number of collected electrons per number of absorbed photons in the solar cell. The influence of reflection is eliminated. The IQE for the three emitters (Figure

3.6 b)) showed an increasing amount of parasitic absorption loss as the emitters became more defective and their minority carrier diffusion length decreased. The IQE response was highest for epi-Si, and lowest for the a-Si heterojunction, with the nc-Si IQE lying between these two limits. The illuminated cell efficiencies are shown in Figure 3.6 c), and confirm the results from IQE. The optical quality of the emitter can be gauged by the short-circuit current. The more defective the emitter, the greater was the parasitic absorption and the lower the current. The cell efficiencies ranged between 14.9 -15.9 %. When high efficiency features were added (pyramid textured surface with reflectance loss less than 3%, and back surface field), cell efficiency exceeded 20%.

One of the main goals of this thesis was to examine heterojunction cells without a thin passivating intrinsic layer. When the intrinsic layer was removed, the highly doped and defective emitter was in direct contact with the c-Si absorber and did not provide as good surface passivation to c-Si compared to an intrinsic buffer layer. Removing the intrinsic layer will increase D_{it} and place more stringent requirements on the electrical quality of the doped emitter in terms of its dopant concentration and bulk defect density (which are interrelated). While it was assumed that the epitaxial emitter cell was a perfect crystal, the a-Si:H and nc-Si emitters had a significant
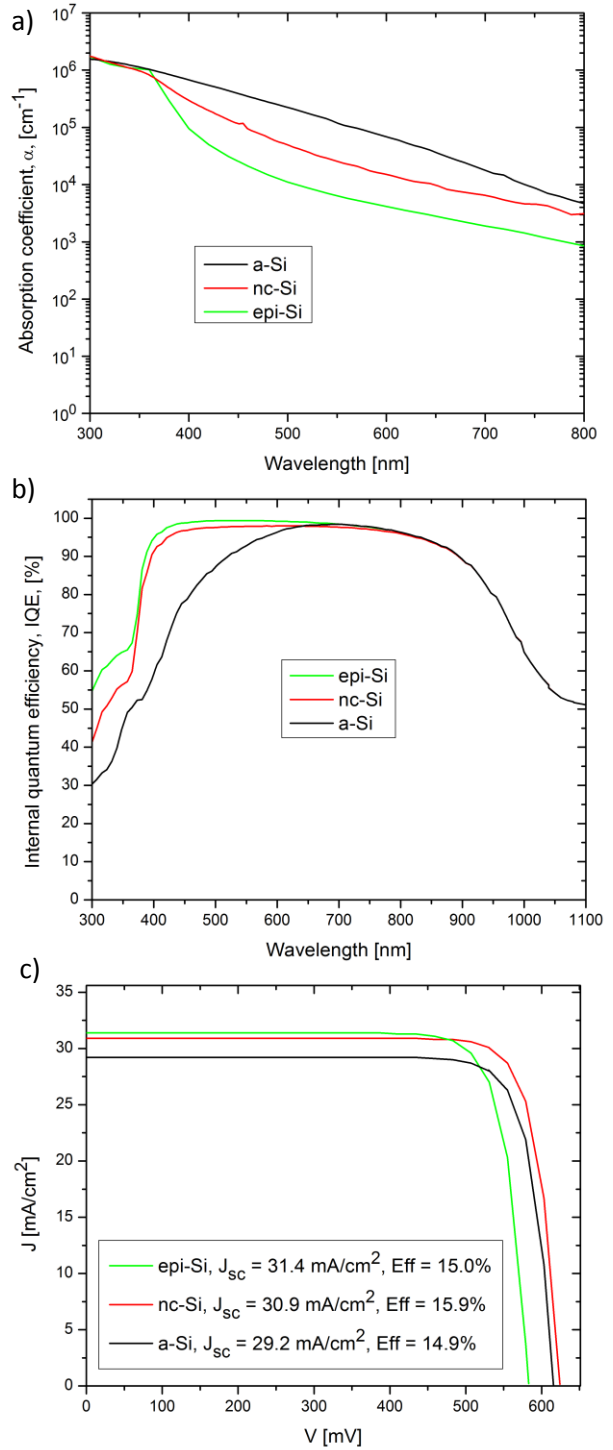
Figure 3.6: Comparison of optical and electrical properties of epi-Si, nc-Si, and a-Si:H on c-Si. a) absorption coefficients. b) internal quantum efficiency. c) Illuminated I-V using Air Mass 1.5 at 25°C.

distribution of band gap defects which could be influenced by growth conditions. In a-Si:H, the total bulk density of states per unit volume was given by N_{DB}. For intrinsic a-Si:H, N_{DB} varies from 1×10^{16} to 1×10^{18} cm^{-3}. For doped a-Si, it varies from 1×10^{18} to 2×10^{20} cm^{-3}. [94] However, in the AFORS-HET software there was no option to vary N_{DB} directly. N_{DB} is related to the acceptor-like and donor-like Gaussian density of states which are assumed to be equal and are defined as N_{tr}. N_{DB} is related to N_{tr} according to equation 3.8, where E represents the energetic distribution of defects throughout the bandgap, E_{DONG} is the donor Gaussian peak energy measured positive from E_C, E_{ACPG} is the acceptor Gaussian peak energy measured positive from E_V, and W_{DG} is the standard deviation of the donor and acceptor Gaussians which are assumed to be equal.

$$N_{DB}(E) = N_{\text{tr}} \int_0^{E_g} \left\{ exp\left[-\frac{1}{2} \frac{(E - E_g + E_{DONG})^2}{W_{DG}^2} \right] + exp\left[-\frac{1}{2} \frac{(E - E_{ACPG})^2}{W_{DG}^2} \right] \right\} dE \qquad (3.8)$$

N_{tr} was varied in the software, and equation 3.8 was simplified by integration from zero to E_g which gave:

$$N_{DB} = 1.14381 \cdot N_{tr} \qquad (3.9)$$

Figure 3.7 shows a comparison of simulations for a-Si:H and nc-Si heterojunctions. The Gaussian density of states for a-Si:H and nc-Si was varied from $N_{tr} = 1 \times 10^{18}$ to 2×10^{20} cm^{-3} for the a-Si:H /c-Si heterojunction, and from 1.8×10^{16} to 2×10^{19} cm^{-3} for the nc-Si / c-Si heterojunction. Information on the expected N_{tr} range for thermally annealed nc-Si was not available in the literature, and so the N_{tr} range was increased from the baseline value until strong negative effects on cell efficiencies were achieved. In Figure 3.7, the red lines in the density of states distributions indicated the normal reference Gaussian and flat-band defect densities for a-Si:H and nc-Si that were taken from literature. The density of state distributions were then increased as indicated by the dashed lines by increasing N_{tr}. At the same time, the interface defect density, D_{it}, was varied for each fixed N_{tr}, and the gradual drop in cell efficiency was plotted (Figure 3.7, bottom). For a-Si:H and nc-Si cells, as the interface defect density was increased the efficiency dropped off sharply which was to be expected. The defective interface layer was assumed to be 1 nm thick. For the reference (lowest) value of N_{tr}, the a-Si:H cell was slightly less sensitive to interface defects than the nc-Si cell. The efficiency started to drop off at $D_{it} = 10^{13}$ cm^{-2} for a-Si:H and at $D_{it} = 10^{12}$ cm^{-2} for nc-Si. This might be because a-Si:H provided better surface passivation than nc-Si. As N_{tr} was increased above the baseline values for both emitter types, the cell efficiency dropped off more rapidly and the heterojunction became increasingly sensitive to interface defects with the efficiency drop off point occurring at lower values of D_{it}. For example, for a-Si:H, as N_{tr} was

increased from 10^{19} cm^{-3} to 10^{20} cm^{-3}, the value of D_{it} at which the efficiency started to reduce was lowered from 10^{13} cm^{-2} to 10^{12} cm^{-2}. Similarly, as nc-Si value of N_{tr} was increased from 10^{17} cm^{-3} to 10^{18} cm^{-3}, the defect density at which the efficiency started to drop was lowered from 10^{12} cm^{-2} to 10^{11} cm^{-2}.
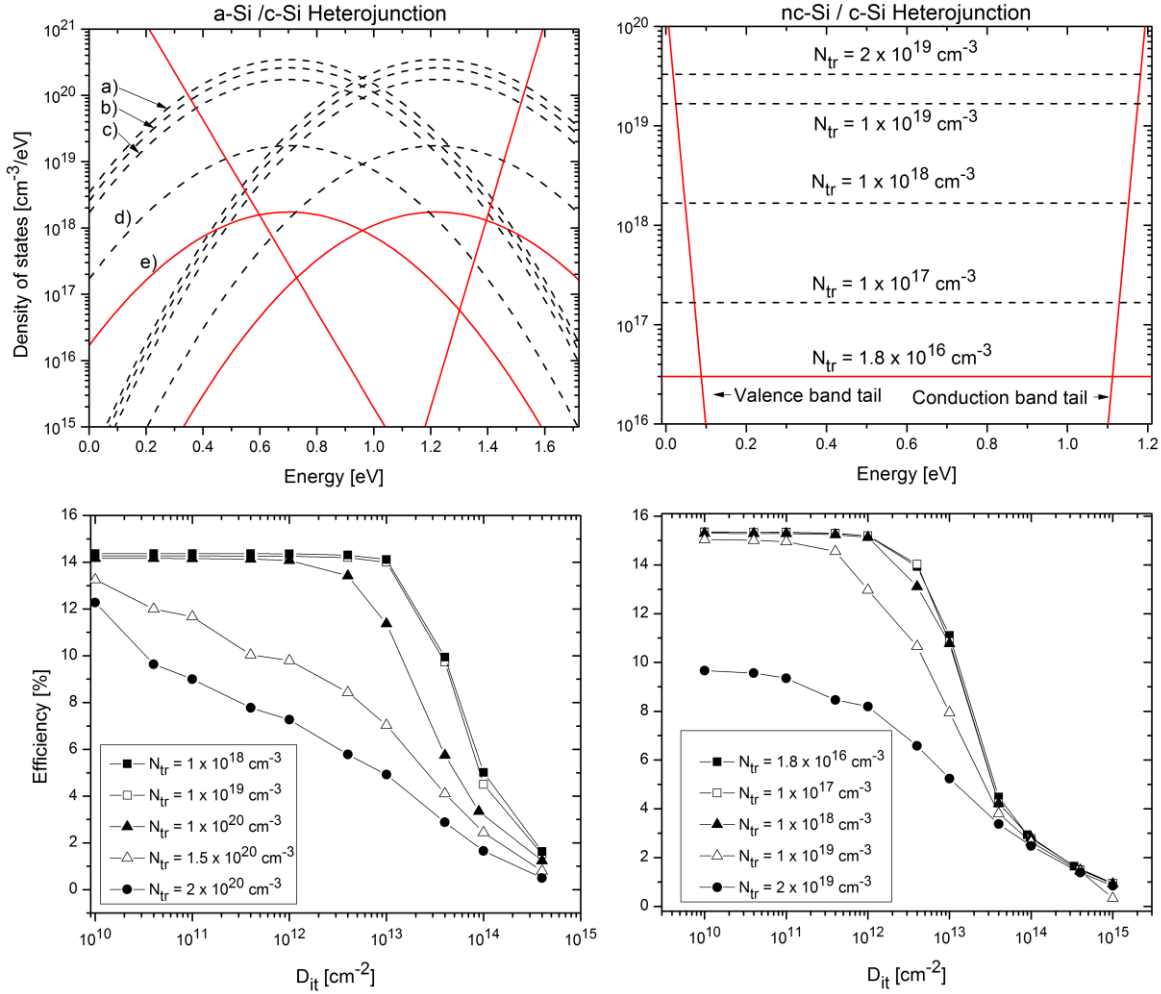
Figure 3.7: (Left, top): Density of states for (n) a-Si:H [89] by increasing the total density of Gaussian donor-like and acceptor-like defect densities, N_{tr} , where a) $N_{tr} = 2 \times 10^{20}$ cm^{-3}, b) $N_{tr} = 1.5 \times 10^{20}$ cm^{-3}, c) $N_{tr} = 1 \times 10^{20}$ cm^{-3}, d) $N_{tr} = 1 \times 10^{19}$ cm^{-3}, and e) $N_{tr} = 1 \times 10^{18}$ cm^{-3} . (Left, bottom): Cell efficiency versus interface defect density for an a-Si:H / c-Si heterojunction with five variations of N_{tr}. (Right, top): Density of states for (n) nc-Si by increasing the total density of flat-band donor-like and acceptor-like defect densities. (Right, bottom): Cell efficiency versus interface defect density for an nc-Si / c-Si heterojunction with five variations of N_{tr}.

Thus, simulations showed that the defective bulk of the emitter influenced interface recombination. For cells without a thin intrinsic passivating layer, as the emitter became increasingly defective the cell was less tolerant of interface defects.

3.4 Examination of Grain Boundaries in Nanocrystalline Silicon

As was shown in chapter 2, although RTA crystallized emitters were epitaxial, nanocrystalline silicon was needed to account for defects in the epitaxial film. Because nanocrystalline silicon has defective grains and grain boundaries, it was used to approximate the defective epitaxial film. Charge trapping in defect states within grain boundaries and particularly within band tails has been shown to create potential barriers to charge transport, which can be modeled by thermionic emission. [95] [96] The number of grain boundaries through which a charge carrier must pass before reaching the contacts depends on the direction of travel. For charge carriers travelling vertically (perpendicular to the substrate), the number of grain boundaries will be relatively small and have a negligible effect on device performance. However, if no transparent conducting oxide is used, charge carriers must travel horizontally (parallel to the substrate) to reach the front contact electrodes and will encounter far more grain boundaries compared to the case of vertical conduction. The difference between current conduction in the vertical and horizontal directions will depend on the grain size, the defect density within grains and at the grain boundaries, the height of the potential barrier at the grain boundary, and the spacing between the front electrodes if no transparent conducting oxide is used. A diagram showing the two paths for current conduction and the potential distribution in a polycrystalline film is shown in

Figure 3.8. There is an anisotropic resistivity: high resistivity for transport parallel to the substrate, and comparably low resistivity for transport perpendicular to the substrate. The same anisotropic resistivity might be expected for the highly defective epitaxial layers produced by RTA. AFORS-HET was used to create a simplified one-dimensional simulation of charge transport through an emitter which had a varying number of grain boundaries. The material properties for the grain boundaries are given in Table 3.1. The movement of charge carriers across the grain boundary potential barrier was modeled by thermionic emission. Charge build-up in defect states creates a space-charge layer and a potential
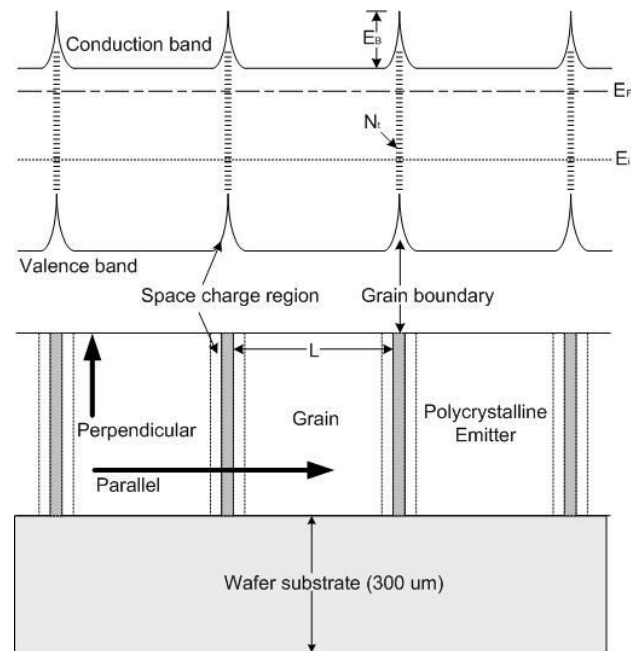
Figure 3.8: Illustration of grain boundaries in a nc-Si film on a wafer substrate and two directions of current transport. Corresponding band diagram shows energetic barrier, E_a, and defect states in the gap for grain boundaries.

barrier. The height of the potential barrier was the limiting factor for current transport in the emitter. The situation was modeled as shown in Figure 3.8 where ordered nanocrystalline grains defined by the specified film thickness were separated by highly disordered grain boundaries. The number of grain boundaries was altered between zero (defect-free epitaxial Si) and 250 (highly defective epitaxial Si). The height of the potential barriers [97] is given by equation 3.10:

$$E_a = e^2 n_t^2 / (8 \, \varepsilon \, N_H) \tag{3.10}$$

where e is the electron charge, n_t is the interface trapped charge per unit area, ε is the dielectric permittivity of silicon, and N_H is the doping level. In the AFORS-HET simulation, a layer stack consisting of uniform grains of width 25 nm separated by grain boundaries 1 nm thick was implemented. The results of dark current-voltage for the diode are shown in Figure 3.9.
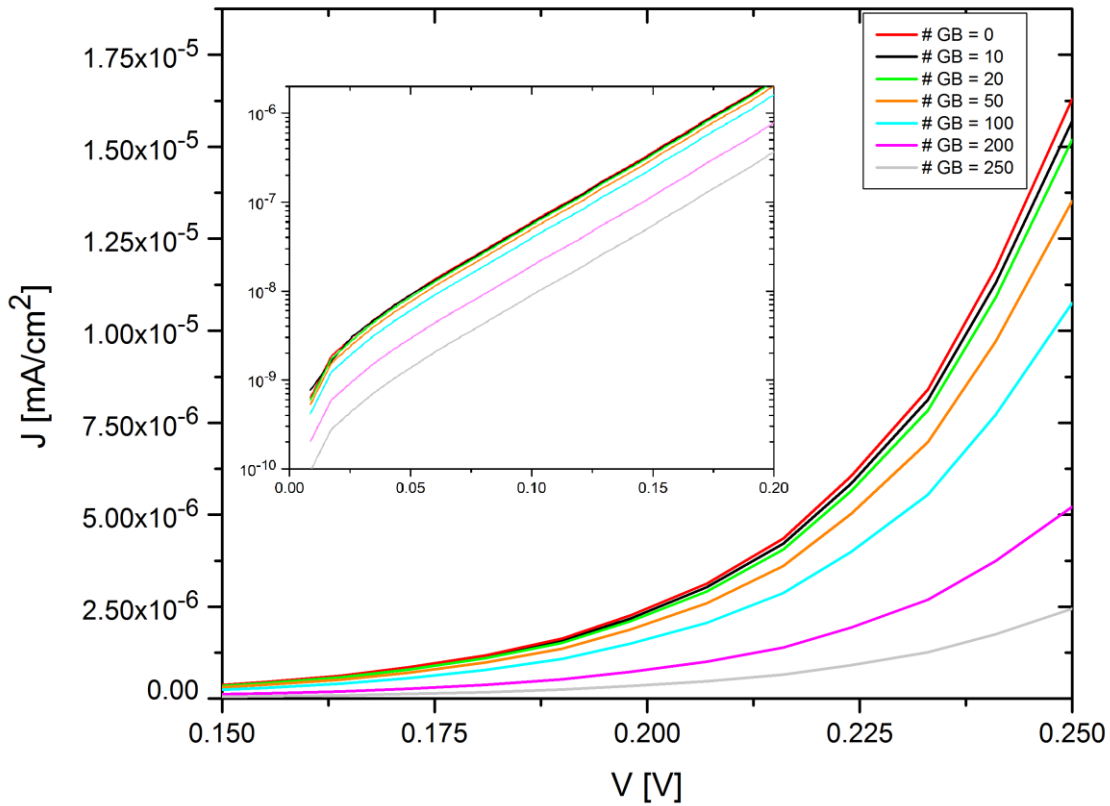
Figure 3.9: Dark current-voltage characteristics of layer stack consisting of 25 nm grains separated by 1 nm grain boundaries on (p-type) c-Si. The inset graph axes have the same units as the main graph.

The uppermost curve (red) approximated the case where the current conduction occurred in the vertical direction for an epitaxial emitter that was defect-free. To approximate a defective epitaxial layer, the number of grain boundaries was increased to 250. The dark forward current was severely reduced due

to the grain boundary barriers, and the distance the current traveled in the emitter reached 6.5 μm. The potential barrier used in simulation was 80 mV, and the trapped charge density was chosen to be 10^{12} (from literature). [98] Much is not known about the exact nature of the defects in the epitaxial emitters: their precise density of states distribution, their behaviour under high temperature annealing, or their ability to act as shunts.

3.5   The Effect of Band Gap Offsets and the Presence of an Inversion Layer

The thermal equilibrium band diagrams for epi-si, nc-Si, and a-Si:H heterojunctions (Figure 3.2), all had band offsets. The offset between epi-Si and c-Si was negligible and was only due to band gap narrowing caused by heavy doping. The offset for nc-Si was larger, approximately 0.1 eV, and was assumed to be entirely in the valence band. The a-Si:H heterojunction had by far the largest offset which was present in the valence band and conduction band. Band offsets are important in solar cell devices not only due to their ability to reduce recombination, but also for their effect on capacitance-voltage (C-V) measurements. C-V methods are important for determining dopant concentrations and built-in voltage as well as for measuring band offsets. However, it was recently shown that a strong inversion layer in a-Si:H / c-Si heterojunctions exists due to band offsets which introduce significant uncertainty into these measurements. [93] [99] In an n^+p heterojunction, the inversion layer is a thin electron layer located in p-type crystalline silicon very close to the interface, and manifests itself as an additional conductivity path as shown in Figure 3.10.
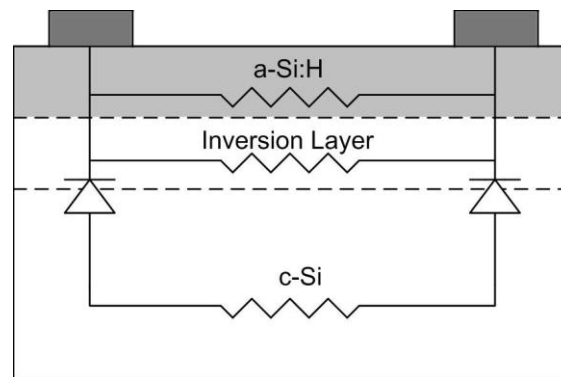
Figure 3.10: Inversion layer in a-Si /c-Si heterojunction. Planar conductance measurements consist of three components: conductance from a-Si:H, from the inversion layer, and a conductance component from the c-Si wafer. The conductance of the p-type wafer is much higher than that of the a-Si:H, but the two layers are electrically isolated because of different conductivity types. The space charge region normally confines current flow to the emitter.

Although epi-Si / c-Si band offsets were too small to cause an inversion layer, was one to be expected in nc-Si heterojunctions? In order to assess whether or not an inversion layer was present in nc-Si / c-Si, AFORS-HET was used to examine the electron concentration, $n(x)$, and to calculate the electron sheet density, N_S, and conductance, G. The electron sheet density is given by equation 3.11, where $n(x)$ is the electron concentration as a function of position in the junction and is integrated across a device layer.

$$N_S = \int_0^{d_{c-Si}} n(x)dx \qquad (3.11)$$

The conductance is given by equation 3.12, where q is the electronic charge, μ_n is the electron mobility in the given layer, h is the length of the electrodes, and L is the distance between them.

$$G = q\mu_n N_S\, h/L \qquad (3.12)$$

For each device, the n$^+$ emitter layer was defined to be 100 nm thick on a lightly doped p-type Si wafer. The temperature dependent mobility for lightly doped c-Si is given by the power law $\mu_n(T) = \mu_{300}(T/300)^{-\alpha}$ where $\alpha = 2.4$. [100] Figure 3.11 shows the result for simulation of $n(x)$ at 300K in the dark. The a-Si / c-Si junction showed a clear spike at the interface on the c-Si side of the junction while no spike in electron concentration was visible for nc-Si and epi-Si junctions.
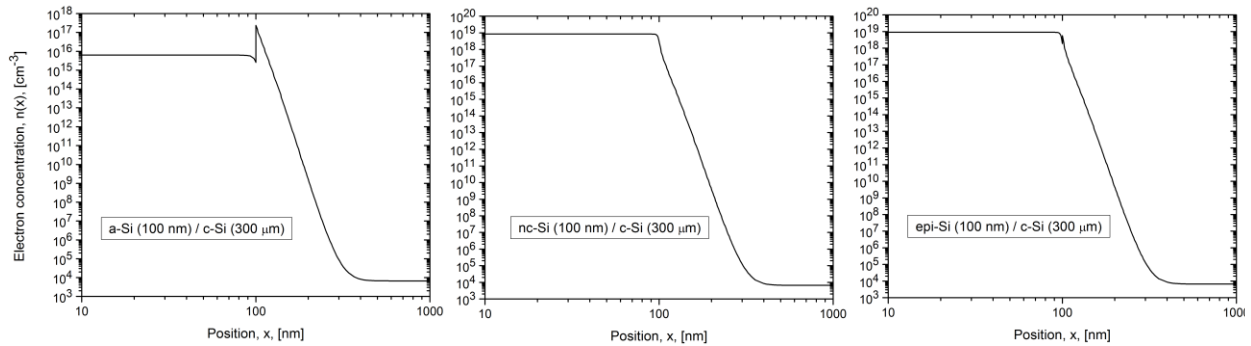
Figure 3.11: Electron concentration as a function of position in the three heterojunctions.

The conductance as a function of temperature from 100 K to 400 K was simulated by integrating the electron sheet density. Conductance was compared between two scenarios for a-Si:H, nc-Si, and epi-Si: 1) films on glass, and 2) films on c-Si. For films on c-Si, if an inversion layer was present then the component of electron conductance from the c-Si would be relatively large as implied by Figure 3.11. For films on glass, N_S was calculated at each temperature by integrating across the thickness of the semiconductor. For films on c-Si, N_S was calculated at each temperature by integrating only across the

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thickness of c-Si and ignoring the emitter layer. The data for N_S was then used to calculate the conductance according to equation 3.12. The results are shown in Figure 3.12. For nc-Si and epi-Si, the electron conductance of the films on glass was orders of magnitude greater than the corresponding electron conductance from the minority electrons in the c-Si wafer. However, for a-Si:H, the component of electron conductance from the c-Si wafer was larger than the conductance of the a-Si:H layer on glass. This was proof of the inversion layer in a-Si:H / c-Si structures. For the band offsets used here, it appeared that an inversion layer in nc-Si / c-Si was not possible.

The presence of an inversion layer and the calculation of the band offsets are interlinked. There are several methods to calculate band offsets including current transport techniques, photocurrent spectroscopic characteristics, and capacitance-voltage. A relatively simple and reliable method is capacitance-voltage intercept. To use this technique, the capacitance of the heterojunction is measured. It is assumed that the heterojunction is abrupt, and that the doping concentrations are uniform throughout all layers. The depletion capacitance, C_D, associated with the space charge region is modeled as a series contribution of capacitances on both sides of the heterojunction. [101]
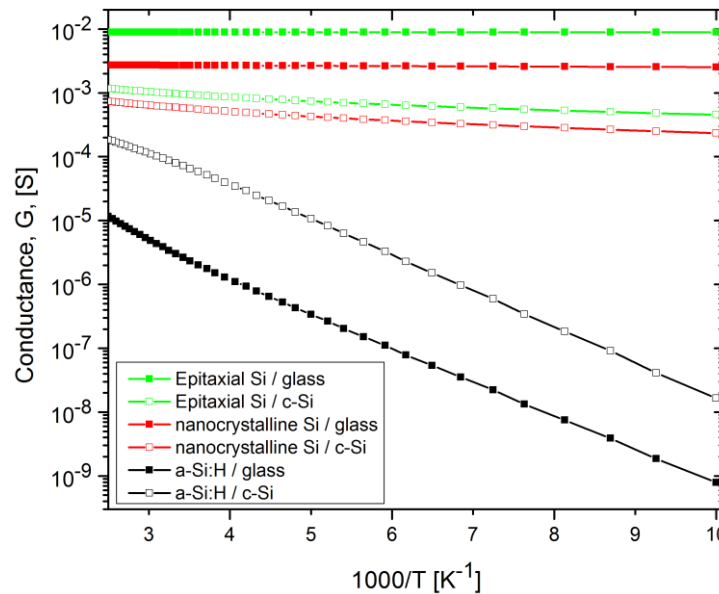
Figure 3.12: Planar conductance comparison between films on glass and c-Si for three film types: a-Si:H, nc-Si, and epi-Si.

The total capacitance per unit area is given by equation 3.13 (where N_1 and N_2 are the net free carrier concentrations in materials 1 and 2):

$$C_D^2 = \frac{qN_1N_2\varepsilon_1\varepsilon_2}{2(\varepsilon_1N_1+\varepsilon_2N_2)(V_D-V)} \qquad (3.13)$$

A graph of $1/C_D^2$ versus V gives the free carrier concentration, and an intercept with the voltage axis gives the diffusion potential, V_D. Once the diffusion potential is known, it is possible to calculate the conduction band offset for any p-n heterojunction [101] according to equation 3.14:

$$\Delta E_C = qV_D - E_{g1} + \delta_1 + \delta_2 \qquad (3.14)$$

where δ_1 is the difference in energy between the Fermi level and the valence band maximum in material 1 (p-type), and δ_2 is the difference in energy between the Fermi level and the conduction band maximum in material 2 (n-type). The conduction band offset, ΔE_C, has a linear dependence on V_D which must be measured as accurately as possible. If the bandgaps of both layers are know then the difference in bandgap energies between materials 1 and 2 is given by equation 3.15:

$$\Delta E_g = |E_{g2} - E_{g1}| = \Delta E_c + \Delta E_v \qquad (3.15)$$

It was recently discovered by Kleider et al. that the inversion layer evident for a-Si:H / c-Si heterojunctions makes the C-V intercept method inaccurate for band offset calculation. [99] However, equations 3.13, 3.14, 3.15 would apply for nc-Si / c-Si and epi-Si / c-Si devices because simulation showed there was no inversion layer.

3.6   Conclusions

When a defective layer was introduced at the heterojunction interface, the approximate defect density threshold beyond which solar cell performance significantly started to reduce was around $D_{it} = 10^{12}$ cm^{-2} for epi-Si, nc-Si, and a-Si:H heterojunctions. However, these results were also dependent on the specified thickness of the defective interface layer. It was likely that a-Si:H heterojunctions were somewhat more tolerant of interface defects because a-Si:H was an excellent passivation layer. Regarding parasitic absorption in the emitter layer, epi-Si and nc-Si heterojunctions provided slightly higher short-circuit currents and better quantum efficiency in the blue and ultraviolet parts of the spectrum compared to a-Si:H heterojunctions. For nc-Si heterojunctions, the grain size and defective nature of the grain boundaries was a critical limiting factor for cell performance particularly when there was no transparent conducting oxide to reduce lateral current conduction. The relatively large bandgap of a-Si:H produced an inversion layer which affects the accuracy of capacitance-voltage measurements

of built-in potential, dopant concentration, and valence band and conduction band offsets. Simulation results showed that nc-Si did not have an inversion layer and so measurements of band offsets would be much more reliable for these heterojunctions compared to a-Si:H / c-Si.

4 Design, Fabrication, and Characterization of Basic Photovoltaic Cells with Crystallized Thin Films

Solar cell structures were fabricated and characterized consisting of n-type a-Si:H deposited on non-textured silicon wafers by PECVD followed by rapid thermal annealing. Annealing recipes established in Chapter 2 were used to minimize mechanical stress in the film in order to avoid peeling, cracking, and pinhole formation. The influence of the annealing temperature on cell performance was examined with an emphasis on establishing what regions of the device were limiting the device open-circuit voltage and short-circuit current: the emitter, the bulk (silicon wafer absorber), or the heterojunction interface.

4.1 Solar Cell Processing: Design and Fabrication

Thin n-type a-Si:H films of approximately 50 nm thickness were deposited onto the polished surface of (100) orientated p-type (1-2 Ω cm) Czochralski Si substrates. Prior to deposition, wafers were RCA-1 and RCA-2 cleaned and dipped in 2% hydrofluoric acid for one minute to remove the native oxide. N-type a-Si:H was deposited according to the optimized recipe in Chapter 2. The deposition conditions were: SiH$_4$ flow rate 20 sccm, PH$_3$ (diluted in 99% H$_2$) flow rate 40 sccm, pressure at 200 mTorr, deposition time 5 minutes, substrate temperature 200°C, and RF power 10 W. The a- Si:H films were RTA processed at temperatures of 600°C, 650°C, 700°C, 750°C, 800°C, 900°C, and 1000°C for annealing periods of 5 minutes. The temperature ramp rate was approximately 10°C/s. The annealing period of 5

minutes at 800°C, 900°C, and 1000°C, although longer than necessary to completely crystallize the film, was chosen based on earlier results which showed that RTA a-Si:H films became progressively more crystalline with better optical and electrical properties as annealing time was increased. From 600°C to 750°C, the annealing time of 5 minutes was sufficient to completely crystallize the a-Si:H films. For example, Kingi et al. have demonstrated that intrinsic a-Si:H PECVD deposited 100 nm thick films can be completely crystallized with annealing times that are several minutes shorter than what was used for the devices in this thesis. [102] After the wafers were annealed, a silicon nitride SiN_x antireflection coating approximately 80 nm thick was deposited by PECVD using SiH_4 (5 sccm) and NH_3 (100 sccm), pressure 600 mTorr, a deposition time of 156 seconds, substrate temperature 350°C, and RF power 15 W. The SiN_x was patterned by photolithography to define the front contacts. Wafers were heated at 110°C for two minutes to remove any moisture, then negative photoresist (AZ nlof 2035) was spin coated at approximately 3000 RPM for 70 seconds, producing a film thickness of approximately 3 μm. The photoresist was soft baked at 110°C for one minute then allowed to cool. The wafer was placed in the mask aligner and aligned to the mask along the major flat in the (100) direction for ease of dicing. UV lamp exposure was at 350 nm for 2 minutes with an approximate energy density dose of 200 mJ/cm^2 to cause polymerization of the photoresist. A post-exposure hard-bake was performed at 110°C for two minutes and then the sample was dipped into AZ300 MIF Photoresist developer in order to strip away the non-polymerized areas of photoresist. The sample was washed in deionized water, dried in N_2, and inspected under the microscope to ensure the quality of the pattern transfer and sufficient undercut of the photoresist. Next, the wafer was dipped in buffered hydrofluoric acid for between 30-60 seconds until the SiN_x was etched away revealing the emitter beneath. Samples were then immediately loaded into e-beam for deposition of the front and back contact. Metallization was performed using Intlvac electron beam evaporation of titanium (50 nm to promote adhesion) followed by silver (1 μm) for the front contact, and aluminum (1 μm) for the back contact. Lift-off was performed by immersing the samples in acetone for 10-30 minutes to define the front contacts. Solar cells were diced using a DAD-2H/6TM Disco dicing saw into 1 cm^2 squares. Finally, several samples were annealed in forming gas in order to improve the electrical quality of the contacts.

For comparison purposes, solar cell devices were also fabricated using PECVD low temperature epitaxial deposition of a 50 nm thick n-type emitter on p-type (1-2 Ω cm) Czochralski Si substrates. The PECVD optimization of the recipe for n-type epitaxial silicon will not be discussed in detail here as it was already the subject of a Ph.D. thesis in this research group. Deposition conditions were: RF power 15 W, 200 mTorr, SiH_4 flow rate 10 sccm, H_2 flow rate 250 sccm, PH_3 flow rate 80 sccm, and substrate

temperature of 300°C (no RTA processing). The cell processing for patterning, lift-off, SiNₓ and metallic contact depositions were identical to those for the RTA processed cells.

The sheet resistivity of the thin highly doped emitter of the p-n junction is an important characteristic of a solar cell. Four point probe sheet resistivity measurements gave a sheet resistivity for all RTA and epitaxial samples of between $\rho_\square = 90 - 120 \; \Omega/\square$. The sheet resistivity of a typical diffused junction solar cell is 40-100 $\Omega/\square$. [103] The sheet resistance is an important figure of merit for the design of the front contacts, in particular the finger width and finger spacing. On the one hand, the finger design should minimize series resistance losses from lateral current flow and so the fingers should be sufficiently wide and close together. At the same time the finger area should minimize shading loss which reduces photocurrent. The fractional power loss due to series resistance in a cell is given by equation 4.1.

$$\frac{P_{loss}}{P_{gen}} = \frac{\rho_\square s^2 J_{MP}}{12 V_{MP}} \tag{4.1}$$

The maximum power point current density is J_{MP}, the maximum power point voltage is V_{MP}, the spacing between adjacent fingers is s, the total power loss is P_{loss}, and the generated power at the maximum power point is P_{gen}. [104] Assuming typical solar cell operating parameters of $J_{MP} = 30$ mA/cm², $V_{MP} = 450$ mV, and a lateral power resistance loss of $P_{loss}/P_{gen} < 1\%$, and a target sheet resistance $\rho_\square = 200 \; \Omega/\square$, the resultant finger spacing should be $s \leq 1$ mm. A certain safety margin must be provided to account for different annealing conditions and small variations in film thickness
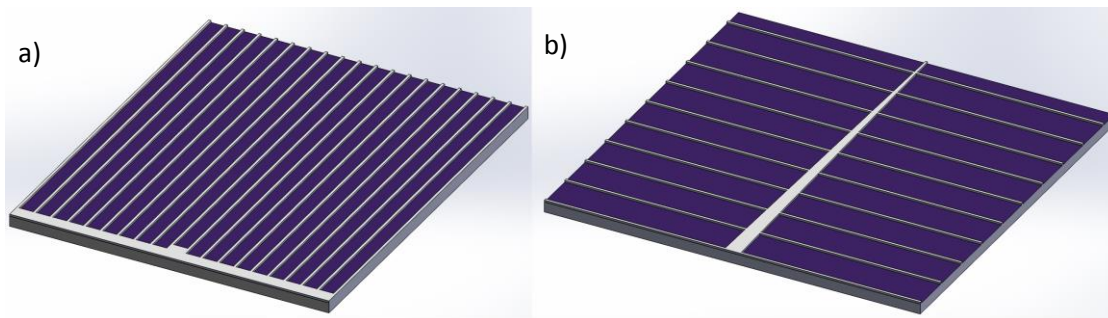
Figure 4.1: a) Front electrode design for solar cells processed by RTA. Spacing between fingers was 350 µm. Mask surface area covered 7.8 % of a 1 cm² area cell. Both masks had the same finger width of 20 µm. b) Electrode design for solar cell with PECVD deposited epitaxial emitter. Spacing between fingers was 1 mm. Mask surface area covered 4.1 % of a 1 cm² area cell.

which might produce a sheet resistivity larger than the targeted 100 $\Omega/\square$. For the solar cells with the low temperature epitaxial n-type layer, the sheet resistance was repeatable (around 100 $\Omega/\square$) and was on

average lower than that of the RTA processed films. Thus two different photo-mask designs were implemented as shown in Figure 4.1. A narrow finger spacing was used for RTA processed cells and wider finger spacing for the low temperature epitaxial emitter cells.

4.2 Dark Current-Voltage

The dark I-V characteristics at 25°C for seven RTA processed cells were made using an Agilent 4155C parameter analyzer. The current-voltage characteristics of a solar cell can be predicted with a single diode with ideality factor $n_1 = 1$ that describes electronic conduction in the quasi-neutral region of the junction (diffusion and recombination). However, a double diode model is more accurate because it accounts for both the diffusion current in the quasi-neutral regions and the recombination current via traps in the space-charge region where the ideality factor of the second diode is $n_2 = 2$. The dark current characteristic of a solar cell is given by equation 4.2 and 4.3:

$$I = I_g + I_d + I_{sh} \tag{4.2}$$

$$I_g = I_1 \cdot \left[exp\left(\frac{V-IR_s}{n_1 \cdot V_{th}}\right) - 1\right], I_d = I_2 \cdot \left[exp\left(\frac{V-IR_s}{n_2 \cdot V_{th}}\right) - 1\right], I_{sh} = \frac{V-IR_s}{R_{sh}} \tag{4.3}$$

where I_g is the voltage-dependent generation-recombination current, I_d is the voltage-dependent diffusion current, I_{sh} is the current passing through shunt resistance R_{sh}, R_s is the series resistance, I_1 is the dark saturation current from recombination in the quasi-neutral regions, I_2 is the dark saturation current due to recombination in the space charge region, and V_{th} is the thermal voltage at room temperature (25.6 mV).

Using the methods of Sigmund [105] and Kaminski [106], all six diode parameters (n_1, I_1, n_2, I_2, R_s, R_{sh}) were derived directly from empirical data without the need for numerical simulations. The extracted diode parameters are shown in Figure 4.2, Figure 4.3, Figure 4.4, and Figure 4.5 which show the forward bias dark I-V characteristics for each cell. Substituting the diode parameters back into equation 4.2, the theoretically predicted dark I-V behaviour was compared to the empirical data. There was good agreement between measurement and theory. As an additional check to make sure the diode parameters extracted from the dark I-V data were accurate, the parameters were used to predict the solar cell open-circuit voltage, V_{oc}, and short-circuit current I_{sc}, under varying illumination intensities. Under illumination, a photocurrent is generated and must be added to equation 4.2. Under open-circuit conditions, equation 4.2 becomes equation 4.4:

$$0 = I_{ph} - I_1 \cdot \left[exp\left(\frac{V_{oc}}{n_1 \cdot V_{th}}\right) - 1 \right] - I_2 \cdot \left[exp\left(\frac{V_{oc}}{n_2 \cdot V_{th}}\right) - 1 \right] - \frac{V_{oc}}{R_{sh}} \qquad (4.4)$$

And under short-circuit current conditions the result is equation 4.5:

$$I_{sc} = I_{ph} - I_1 \cdot \left[exp\left(\frac{I_{sc} \cdot R_S}{n_1 \cdot V_{th}}\right) - 1 \right] - I_2 \cdot \left[exp\left(\frac{I_{sc} \cdot R_S}{n_2 \cdot V_{th}}\right) - 1 \right] - \frac{I_{sc} \cdot R_S}{R_{sh}} \qquad (4.5)$$

In the inset graphs of Figure 4.2, Figure 4.3, and Figure 4.4 , equations 4.4 and 4.5 were used to calculate the theoretical relation between I_{sc} and V_{oc} under varying illumination, and this result was compared to the measured solar cell I_{sc} and V_{oc} obtained by using three different lamp intensities. There was a good agreement between theory and measurement both for dark and illuminated I-V measurements which confirmed the validity of the extracted diode parameters.
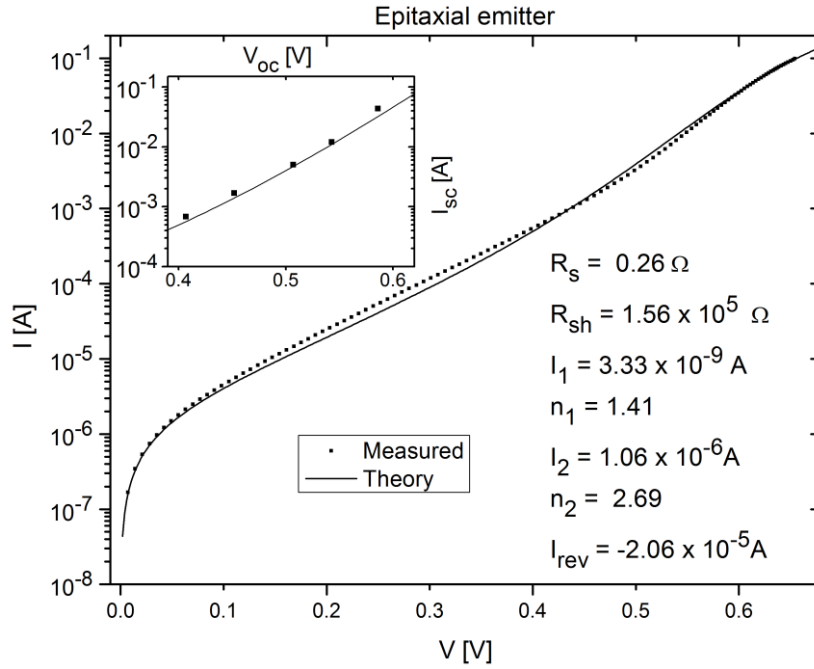
Figure 4.2: Low temperature PECVD deposited epitaxial solar cell dark I-V results. The inset graphs show the theoretical short-circuit current versus open-circuit voltage compared to experimentally measured data obtained by varying light intensity.

Both dark and illuminated measurements were made using a four probe (Kelvin) arrangement. The Kelvin measurement was superior to the two probe arrangement especially under illumination where there was a substantial current increase causing significant parasitic voltage drops due to contact resistance between the probes and the contact pads. By the Kelvin arrangement, the voltage was measured with two additional contacts and the current flowing through this voltage path was negligibly small due to the high impedance of the voltmeter. [107] Several trends were evident from the diode parameters. The diode reverse current, I_{rev}, decreased with increasing RTA temperature (In Figure 4.2, Figure 4.3, Figure 4.4, and Figure 4.5, reverse current was measured at a bias of -0.7 V). The shunt resistance seemed to increase slightly with RTA temperature, although shunt resistance was also influenced by
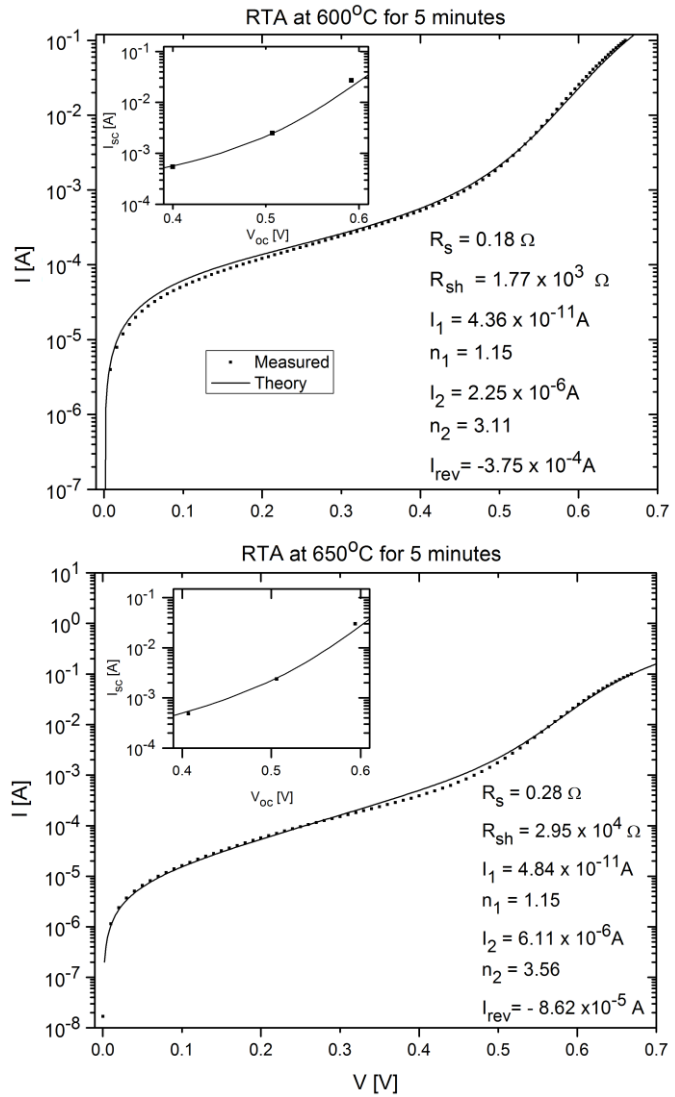
Figure 4.3: Dark I-V results for RTA processed samples at 600°C and 650°C.

fabrication defects which provided alternate current paths for light-generated charge carriers. The shunt resistance was on the order of 10^4 Ω for the devices annealed at 600°C and 650°C, and was approximately 10^5 Ω for the devices annealed at 700°C up to 1000°C and the low temperature epitaxial cell. The highest shunt resistance, $R_{sh} = 3.49 \times 10^5$ Ω, occurred at 1000°C RTA. The series resistance for all devices was less than 0.3 Ω. A typical n⁺p solar cell usually has a series resistance of 0.7 Ω or less, dependent on the junction depth, the impurity concentration in the n-type and p-type layers, and the geometry of front-side metal contacts. The space-charge region saturation current, I_2, was on the order of 10⁻⁶ for annealing temperatures of 600°C and 650°C, and decreased by approximately an order of magnitude to 10⁻⁷ for annealing temperatures above 700°C. Also, the shape of the forward bias curve

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changed. The RTA annealed film at 600°C had two distinct diodes/slopes (one at low forward bias and the other at high forward bias), whereas the difference in these two slopes for devices annealed at 700°C to 1000°C seemed to be reduced. This effect was attributed to the decrease in space-charge saturation current, I_2, that occurred as the annealing temperature was raised. Also, the second diode ideality factor, n_2, was between 2.5-2.7 for the epitaxial cell and the cells at annealed at 700°C to 1000°C, but n_2 became greater than 3 for cells annealed at 600°C and 650°C.

The key device parameter affecting the efficiency of any heterojunction solar cell is the electrical quality of the junction interface. In the crystallization of amorphous silicon films by RTA or furnace, micro-twins are a commonly observed inter-grain defect.

Figure 4.4: Dark I-V results for RTA samples at 700°C and 750°C.

Micro-twins may terminate inside a grain and act as scattering centres. Micro-twin defects are unstable, and it has been shown that their density can be drastically reduced with RTA annealing temperatures at or above 750°C. [108] In the literature, the electron spin resonance technique has been used to measure the spin density which is correlated to the density of dangling bonds at grain boundaries, and defects within the grain. It has been shown that high temperature RTA reduces the spin density/dangling bond density (compared to regular furnace annealing) resulting in polysilicon films of good electrical quality (as confirmed by Hall mobility measurements). [108] Thus, RTA has the capability of greatly improving crystallized Si film characteristics by reducing the density of dangling bonds and in-grain micro-twins. For

the RTA annealed films, it is postulated that a high density of defect states such as micro-twins and grain boundaries may act as shunt paths which could explain the low shunt resistance at $600^{\circ}C$ compared to the much higher shunt resistances at temperatures above $700^{\circ}C$ where the concentration of unstable micro-twins may be reduced by RTA. These trends would seem to suggest that higher annealing temperatures improved the electrical quality of the heterojunction interface by annealing away defects. In summary, the devices annealed at $600^{\circ}C$ and $650^{\circ}C$ had larger reverse current loss by approximately a factor of 5 to 10, and had lower shunt resistance and larger second diode ideality factor compared to the low temperature epitaxial cell and $700^{\circ}C$ to $1000^{\circ}C$ annealed cells.

4.3   Quantum Efficiency

External quantum efficiency (EQE) is defined as the number of electrons collected by the solar cell per incident photon. EQE will always be less than 100% due to a combination of optical (reflection and parasitic absorption) and recombination losses. In a monochromator based system, chopped monochromatic light illuminates a reference cell (for calibration), and then the sample for measurement. The current output is converted to a voltage which is amplified by a lock-in amplifier triggered by a chopper wheel. The illumination area was
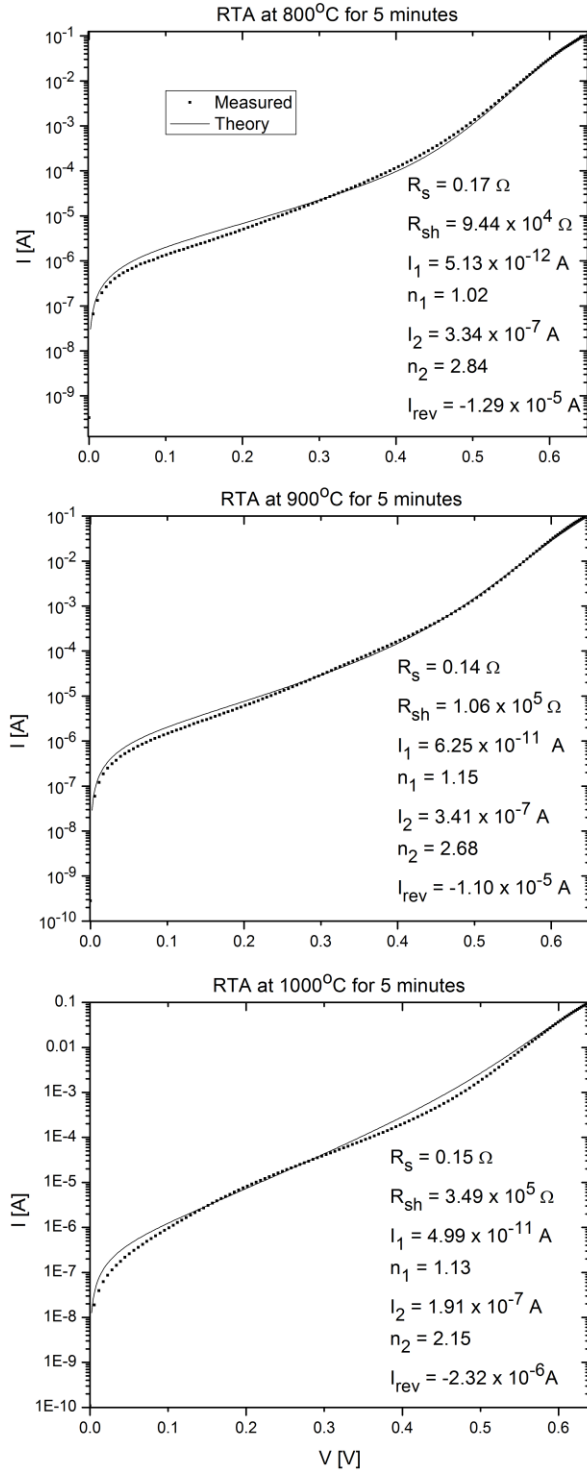
Figure 4.5: Dark I-V results for RTA samples at $800^{\circ}C$, $900^{\circ}C$, and $1000^{\circ}C$.

approximately 1 mm x 5 mm which was substantially smaller than the fabricated cells. The EQE was thus a local property, which varied slightly with location on the cell surface due to reflection from the finger contacts and bus bar. The internal quantum efficiency (IQE) is the number of electrons collected per incident photon absorbed in the solar cell and is related to EQE and reflectance, R, by $IQE(\lambda) = EQE(\lambda)/(1 - R(\lambda))$. Reflectance measurements were made using a Perkin Elmer Lambda 950 spectrometer with 150 mm InGaAs integrating sphere over the wavelength range from 300-1100 nm. From the combined EQE and reflectance, IQE was calculated. External quantum efficiency (EQE) measurements were performed using Model QEX7 Solar Cell Spectral Response system (PV Measurements Inc.) with a two probe configuration and a chopping frequency of 100 Hz.

Low temperature annealing is a common method of lowering resistance between metal layers and silicon. A forming-gas annealing at 350°C for ten minutes in an ambient of N_2 and H_2 was performed in order to promote ohmic contacts. It was an important step for creating ohmic contacts, especially for the back contact where the metal was contacting lightly doped p-type Si. A thin layer (30-50 nm) of titanium was used to minimize junction spiking and to improve the adhesion of silver to prevent peeling off the metallization layer during lift-off and dicing. However, it was possible that pinholes or film-stress cracks existed in the titanium layer and that silver was in direct contact with silicon in some small regions. Wherever it contacted silicon, silicon dissolved into silver during annealing. The amount of silicon dissolved depended on the annealing temperature, annealing time, solubility, and the volume of silver to be saturated with silicon. From a process of trial and error, it was determined that best solar cell results were achieved with a forming gas anneal of 10 minutes. Longer annealing increased the probability of junction spiking while shorter annealing times were sometimes insufficient to realize ohmic contacts.

The EQE, IQE and reflectance for the RTA and low temperature epitaxial samples were measured before and after forming gas annealing. Comparing the EQE results of Figure 4.6 and Figure 4.7, the forming gas anneal caused a significant improvement in cell short-circuit current for all samples, and also reduced the standard deviation of the measurements substantially as can be seen in the reduction of the error bar magnitude. The short-circuit current increased with rising RTA temperature from 600°C to 750°C and reached a peak of $J_{sc} = 31.1 \pm 0.2$ mA/cm². For annealing temperatures of 800°C, 900°C, and 1000°C, short-circuit current decreased with increasing RTA temperature reaching a minimum of $J_{sc} = 26.4 \pm 0.1$ mA/cm².
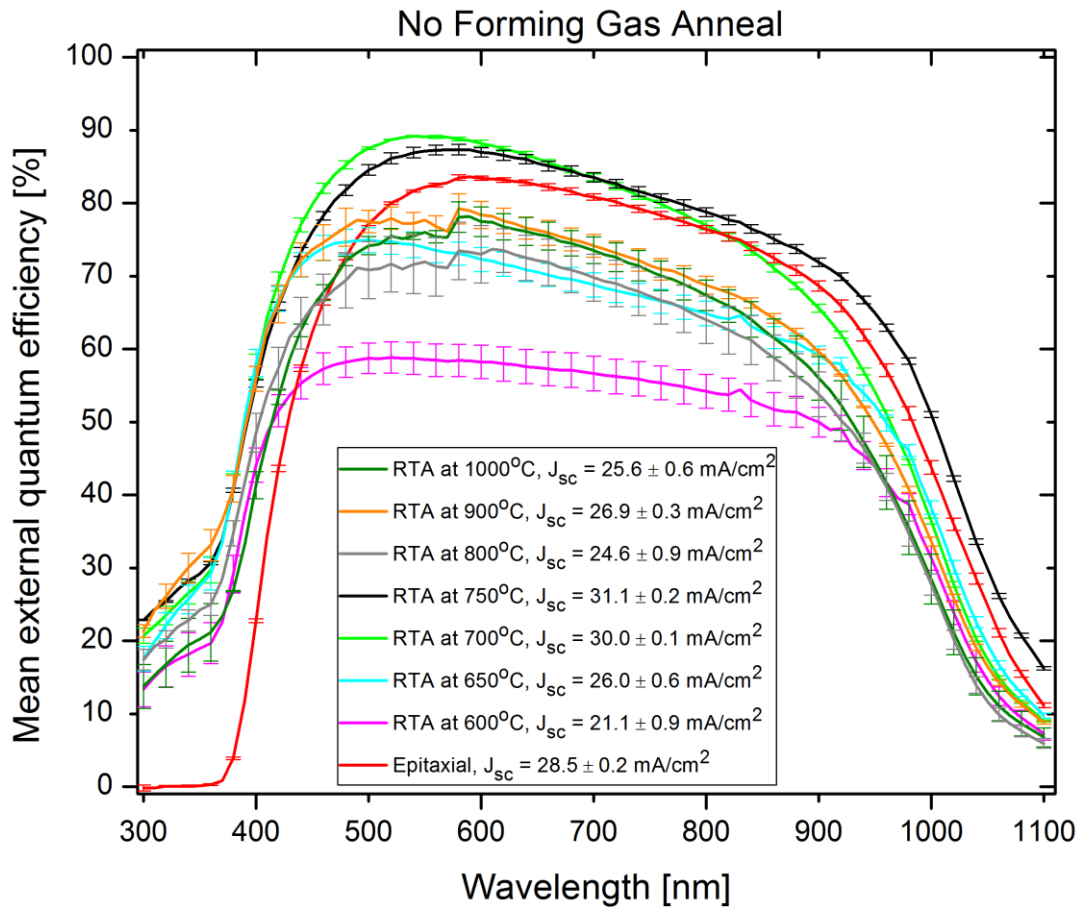
Figure 4.6: External quantum efficiency results for low temperature PECVD epitaxial, and RTA processed solar cells.

In Figure 4.7, the EQE of around 20% at 300 nm was substantially lower than the comparable EQE (60%) of typical diffused junction solar cells [113]. This indicated that although the n-type layer was crystalline it was defective. There was little difference in EQE results in the 300-400 nm range as RTA temperature was changed.

The results of IQE after forming gas anneal are shown in Figure 4.8. For high energy photons of approximately $\lambda < 650$ nm, IQE spectrum losses were mainly due to recombination in the emitter, at the heterojunction interface, and within the bulk of the silicon wafer near the interface. Optical losses were also incurred due to parasitic absorption in the SiN_x anti-reflection coating. For low energy photons of approximately $\lambda > 800$ nm recombination of charge carriers produced by the red part of the spectrum were due to the limited minority carrier diffusion length in the silicon bulk (absorber losses).

Examining the high energy photon losses, Figure 4.8 a) showed a steadily increasing IQE suggesting that
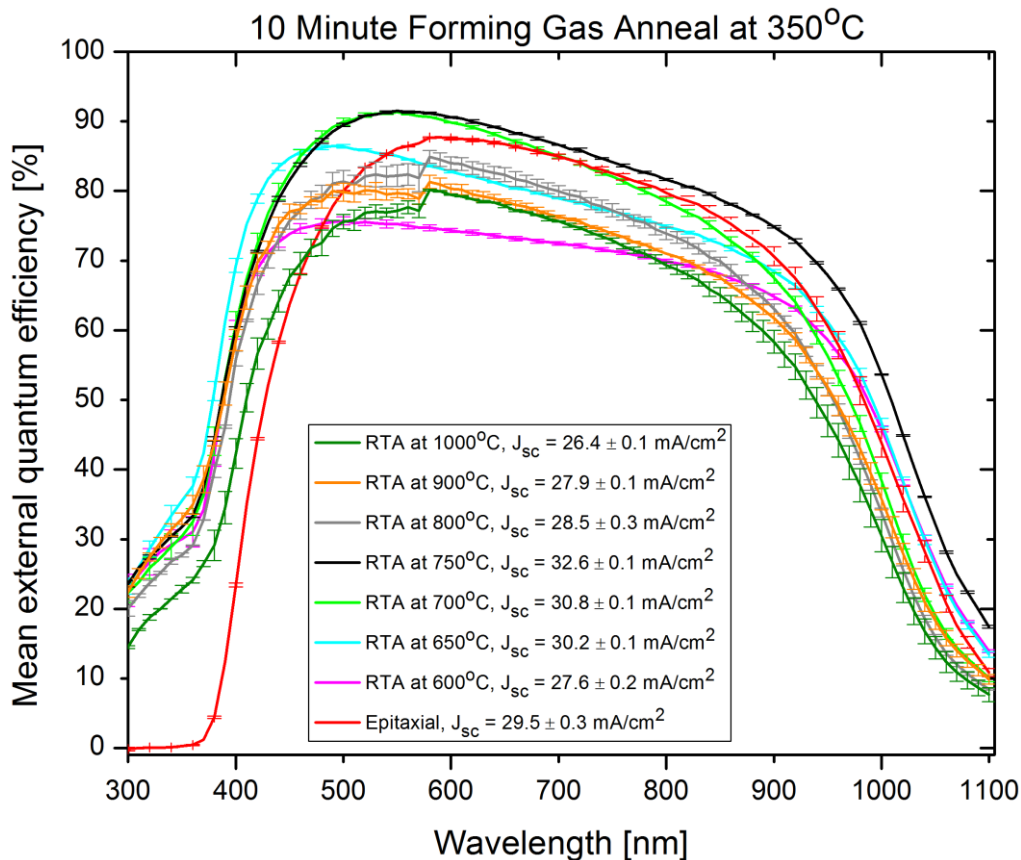
Figure 4.7: External quantum efficiency results for low temperature PECVD epitaxial and RTA processed cells after forming gas anneal.
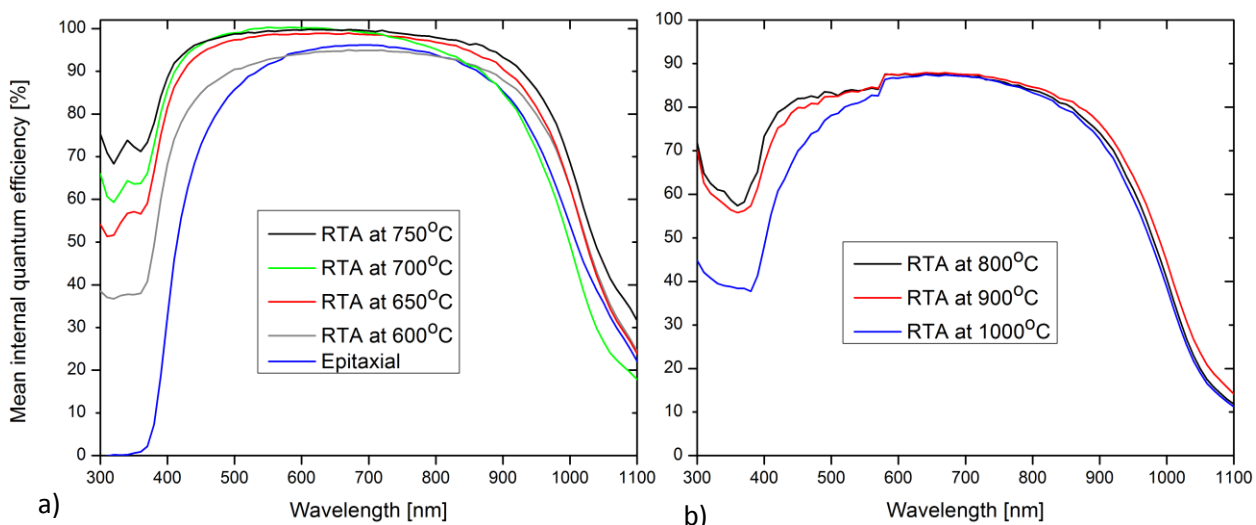
Figure 4.8: Mean internal quantum efficiency versus wavelength for low temperature PECVD epitaxial, and RTA processed cells.

the electrical quality of the emitter was improved with higher RTA temperatures. Figure 4.8 b) showed a worse IQE with increasing annealing temperature above 800°C. From chapter 2, it was clear that higher annealing temperatures gave better electrical and optical quality emitters. Thus, the losses for $\lambda <$ 650 nm were attributed to greater recombination at the heterojunction interface and within the Si wafer close to the p-n junction. In addition, while Figure 4.8 a) had an IQE of 20-30% at 1100 nm, Figure 4.8 b) had a corresponding IQE of only 10-15 %. This loss could be attributed to enhanced recombination in the silicon absorber bulk, perhaps due to a reduced minority carrier diffusion length as a result of prolonged high temperature processing. The IQE response of the low temperature epitaxial cells between 300-400 nm was nearly zero which was due to a combination of high dopant concentration and defects in the emitter.

4.4   Solar Simulator

Solar simulator measurements were performed using an Abet Technologies 2000 solar simulator. Cells were measured under standard test conditions at 25°C, and Air Mass 1.5G spectrum approximated by a Tungsten halogen and Xenon lamp. Load resistance was varied to sweep the voltage. Samples were contacted using a four probe arrangement. The cell results for the RTA processed and low temperature epitaxial devices before and after forming-gas anneal are shown in Figure 4.9 and Figure 4.10.

In addition to increasing the short-circuit current, the forming gas also significantly increased the cell open-circuit voltage by as much as 20 mV to 100 mV. Although the forming gas anneal reduced the contact resistance of the front and back contacts, such a large increase in V_{oc} also revealed a defect passivation occurring within the emitter and at the heterojunction interface. Hydrogen was likely diffusing into the junction and passivating dangling bonds. The S-shaped illuminated I-V characteristics clearly seen in Figure 4.10 have been attributed to heterojunctions with defective interfaces by several research groups. [109]
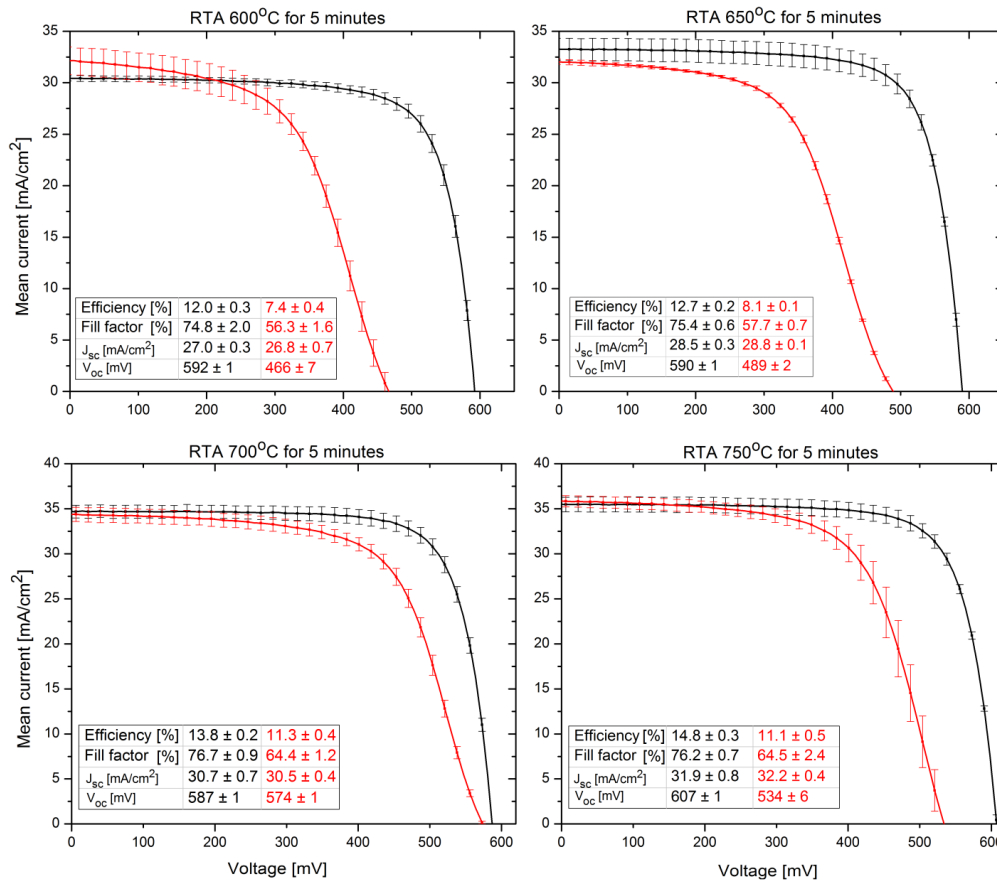
Figure 4.9: Solar simulator results comparison before and after forming gas anneal for cells processed by RTA from 600°C to 750°C. Results shown in red are before forming gas anneal and results shown in black are after forming gas anneal.

The variation in open-circuit voltage among forming gas annealed samples did not seem to be influenced by annealing temperature. As was confirmed by EQE, the cell short-circuit current showed a clear correlation to annealing temperature reaching a peak for RTA at 750°C and decreasing for temperatures above and below this inflection point. The correlation between device efficiency and J_{sc} after forming gas anneal is shown in Figure 4.11.

RTA 800°C for 5 minutes

Efficiency [%]	13.4 ± 0.1	5.0 ± 1.2
Fill factor [%]	80.6 ± 0.2	39.0 ±12.1
J_{sc} [mA/cm^2]	28.1 ± 0.2	27.1 ± 0.5
V_{oc} [mV]	590 ± 1	478 ± 47

RTA 900°C for 5 minutes

Efficiency [%]	12.8 ± 0.	7.5 ± 0.2
Fill factor [%]	79. ± 0.1	57.1 ± 0.5
J_{sc} [mA/cm^2]	27.3 ± 0.	27.0 ± 0.2
V_{oc} [mV]	589 ± 1	488 ± 1

RTA 1000°C for 5 minutes

Efficiency [%]	11.9 ± 0.1	5.9 ± 0.4
Fill factor [%]	79.4 ± 0.4	47.1 ± 1.0
J_{sc} [mA/cm^2]	25.8 ± 0.3	25.5 ± 0.4
V_{oc} [mV]	580 ± 2	491 ± 14

Epitaxial emitter

Efficiency [%]	11.7 ± 0.4	8.3 ± 1.4
Fill factor [%]	73.9 ± 1.0	55.6 ± 8.4
J_{sc} [mA/cm^2]	27.6 ± 0.5	27.0 ± 0.9
V_{oc} [mV]	572.2 ± 3.8	548.5 ± 3.1

Figure 4.10: Solar simulator results comparison before and after forming gas anneal for low temperature epitaxial emitter and RTA processed cells at temperatures from 800ºC to 1000ºC. Results shown in red are before forming gas anneal and results shown in black are after forming gas anneal.
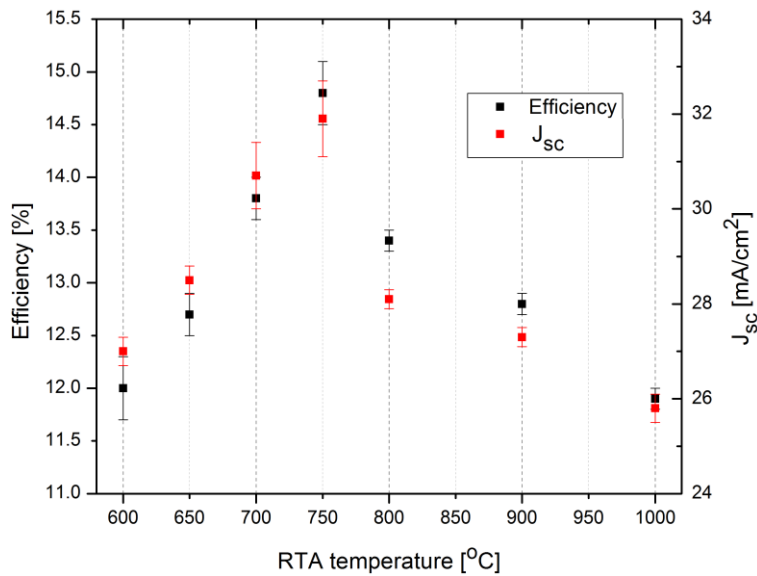
Figure 4.11: Cell efficiency with corresponding short-circuit current for all RTA processed cells after forming gas anneal.

4.5 Spreading Resistance Profiling

Spreading resistance profiling is used to obtain resistivity and dopant density depth profiles. The sample is lapped using a diamond paste or other polishing compound, and a bevel angle is formed across which two carefully spaced probes are stepped. Figure 4.12 shows a beveled sample and probe setup. A current, I, flows from the probe and spreads out from the tip. The resistance between the probes consists of the probe resistance, R_{pr}, contact resistance, R_c, and spreading resistance, R_{sp}, as given by $R = 2R_{pr} + 2R_c + 2R_{sp}$. The measured spreading resistance is converted into silicon resistivity by calibration curves using reference samples of known resistivity. The resistivity profile is then converted to a carrier profile using mobility data. [107] It is assumed that the carrier profile of the beveled surface is identical to that of the vertical profile, and also that the carrier profile is identical to the dopant profile. For shallow junctions, for example n⁺p, there is some redistribution of mobile carriers (carrier spilling) when electrons in the highly doped n-type region migrate to the lightly doped p-type substrate. [110]
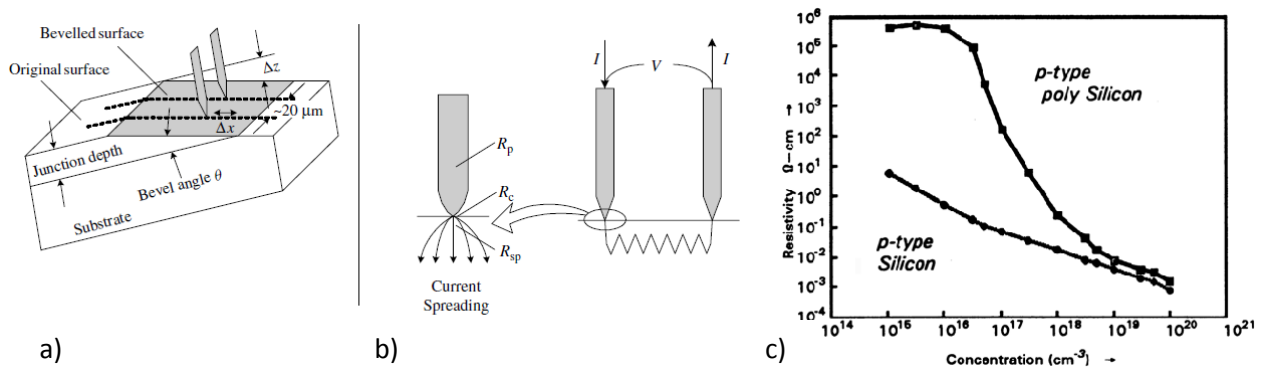
Figure 4.12: a) Principle of spreading resistance profiling. b) Two point probe showing contact resistance, probe resistance, and current spreading. [107] c) Resistivity versus dopant concentration for p-type single crystal silicon compared to polysilicon. [111]

During rapid thermal annealing, the high temperatures caused phosphorous from the n⁺ layer to diffuse into the lightly doped p-type wafer. In order to assess to what extent phosphorous diffusion was occurring during annealing, samples were analyzed consisting of 50 nm n-type a-Si:H crystallized by RTA for a period of 5 minutes at the following temperatures: 600°C, 650°C, 700°C, 750°C, 800°C, 900°C, and 1000°C. As was shown in Chapter 2, at these temperatures the films appeared to be defective, epitaxial, and best modeled as a combination of crystalline and nanocrystalline silicon. Spreading resistance profiling applied to nanocrystalline silicon requires approximations because single crystal calibration samples of known resistivity are used to convert spreading resistance profiles, and then resistivity is

converted to carrier concentration using mobility data for single crystal silicon. However, when nanocrystalline silicon is highly doped, the uncertainties associated with calibration and mobility are significantly reduced. For conversion from spreading resistance to resistivity, the calibration charts for doped silicon of different crystal orientations differ by very little at the low resistivity end, and so nanocrystalline silicon can safely be considered as an average of the two curves. Furthermore, Figure 4.12c shows resistivity versus concentration data for polycrystalline and single crystal silicon. At doping concentrations greater than 10^{19} cm^{-3}, the differences in resistivity are greatly reduced. [111]

The results of spreading resistance profiling for the samples annealed at 600°C, 650°C, 700°C, and 750°C are shown in Figure 4.13. Spreading resistance measurements confirmed that the thickness of the n-type layer was around 50 nm. Moving away from the metallurgical junction, the phosphorous concentration increased abruptly by more than two orders of magnitude within a distance of approximately 4 nm, and continued to increase more gradually reaching a peak concentration at the emitter surface with $N_D \approx 2 \times 10^{20}$ cm^{-3}.
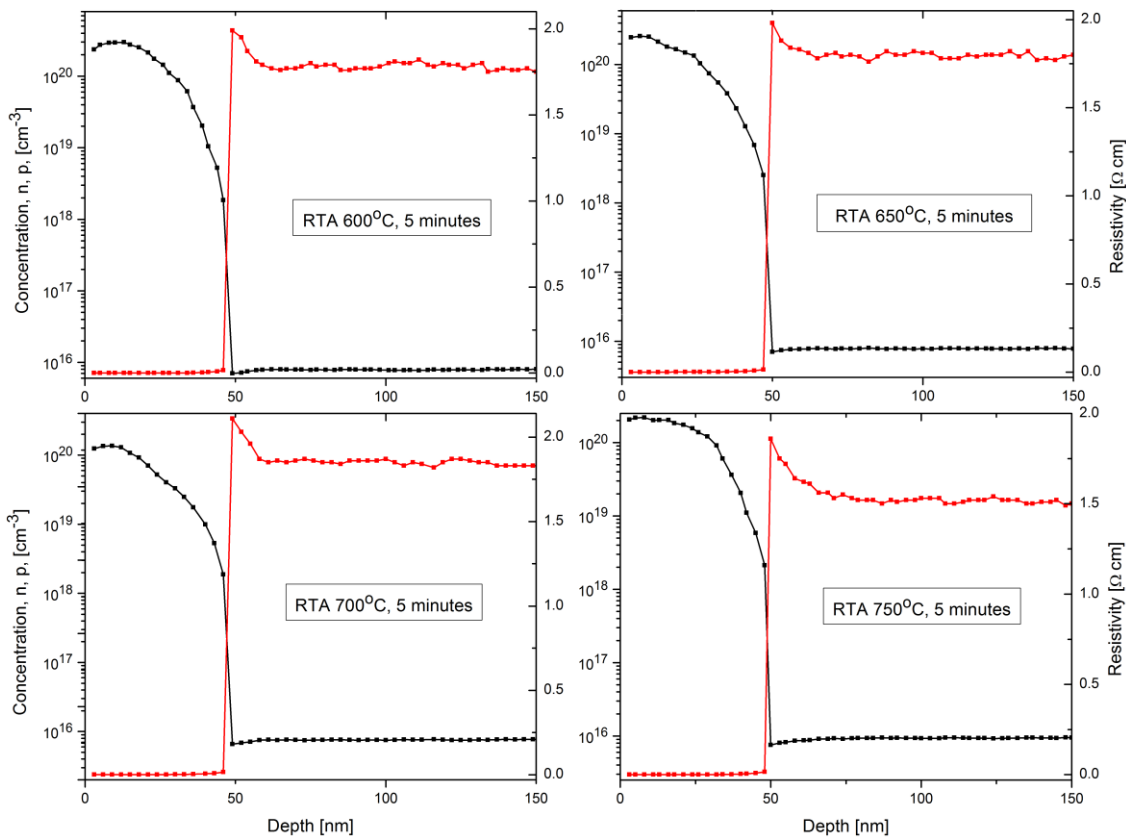
Figure 4.13: Spreading resistance profiling for RTA for 5 minutes at temperatures from 600°C to 750°C. The uncertainty in depth scale is $\pm 3\%$ and the uncertainty in carrier concentration and resistivity near the junction is $\pm 30\%$ and $\pm 15\%$ respectively. These limits are regarded as typical for such measurements.

The results of spreading resistance profiling for the samples annealed at 800°C, 900°C, and 1000°C are shown in Figure 4.14. For these samples, there was increasing amount of dopant diffusion from the emitter into the silicon wafer as the temperature increased. Instead of being abrupt, the junctions became slightly diffused and the wafer surface was compensated. The n-type depth substantially increased from approximately 50 nm where dopant diffusion was negligible ($T \leq 750$°C) up to 400 nm ($T = 1000$°C). The diffused doping in the wafer will reduce the electric field strength at the heterojunction interface. Also, there will be a greater amount of recombination for high energy photons absorbed close to the cell surface which reduces the photocurrent. This explains why the blue part of the spectral response was poor at high RTA temperatures. In addition to dopant diffusion, high annealing temperatures may also cause electrical activation and diffusion of impurities. Impurities may be located at the heterojunction interface dependent on the chemical cleaning process, may have been incorporated into the amorphous film during PECVD deposition, or were introduced in the RTA nitrogen ambient gas or quartz annealing tube.
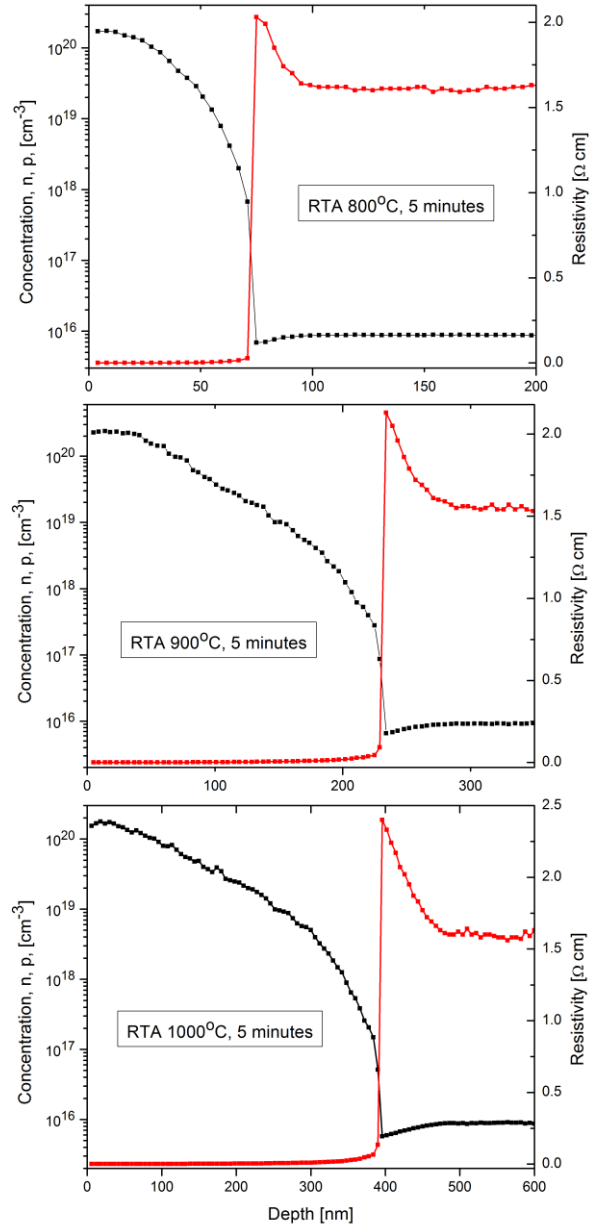
Figure 4.14: Spreading resistance profiling for samples annealed at 800°C, 900°C, and 1000°C for 5 minutes.

Dopant diffusion during RTA was influenced by temperature but also by the spectrum emitted by the tungsten halogen lamps. For regular furnace annealing, when a host atom acquires enough vibration energy to leave its lattice site it creates a vacancy into which a phosphorous atom can diffuse. Phosphorous dopant migration can also occur due to interstitial diffusion. Typical diffusion of phosphorous by furnace requires temperatures between 900-950°C for at least 15 minutes. [112] In an

idealized case, the solution of the diffusion equation for a constant surface concentration and the appropriate boundary conditions is the complimentary error function: $(x, t) = C_s erfc(x/2\sqrt{Dt})$. Where C_s is the surface concentration, D is the diffusion coefficient for phosphorous, and t is the annealing time. [113] Figure 4.15 compares the measured dopant density to the theoretical dopant density assuming a phosphorous diffusion coefficient at 1000°C of $D = 5 \times 10^{-14}$ cm²/s, an average surface concentration in the emitter of $N_D = 1.5 \times 10^{20}$ cm⁻³, and an annealing time of $t = 300$ s. Clearly, the theoretical diffusion profile underestimates the dopant concentration.
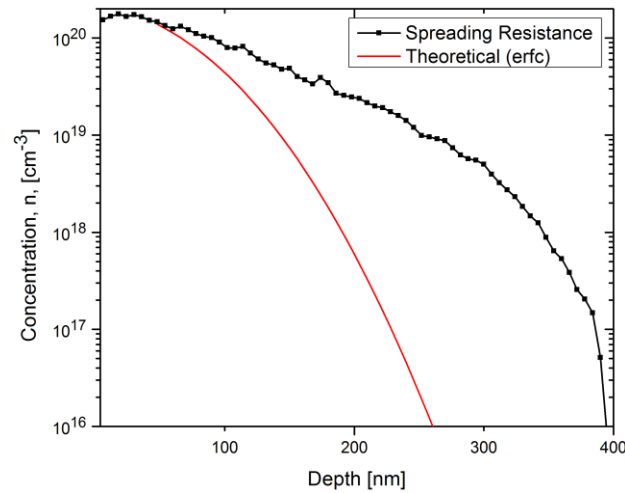
Figure 4.15: Comparison between theoretical and measured impurity profile for RTA processed sample at 1000°C.

The discrepancy can be examined from a thermal and spectral perspective. From a thermal perspective, the diffusion was either intrinsic or extrinsic depending on the dopant concentration and whether or not it was lower than the intrinsic carrier concentration. For example, at 1000°C, silicon has an intrinsic carrier concentration of 5×10^{18} cm⁻³. Under high doping conditions the standard solution to the diffusion equation no longer applies, and the diffusivity becomes concentration dependent. From the spectral side, dopant diffusion in silicon has been shown to be enhanced by high energy photons particularly in the ultraviolet leading to increased diffusion coefficients for phosphorous compared to regular furnace diffusion. [114] The question of what fundamental mechanism is causing the enhancement remains under debate. Ultraviolet photons are absorbed within the emitter, or very close to the silicon wafer surface, and may cause photochemical effects such bond breaking and layer densification. Rapid thermal annealing is characterized by a relatively fast ramp-up and cool-down rate. It has been suggested that transient effects due to temperature or interface equilibration between the phosphorous source and the silicon wafer during RTA can play a larger role in diffusion compared to

regular furnace annealing. Mathiot et al. have noted that ultraviolet light greatly increases phosphorous injection in silicon, creating an excess of phosphorous interstitials that are highly mobile compared to substitutional phosphorous. The interstitial phosphorous will dissociate with a time constant that, if comparable to the rapid thermal annealing time, will cause a significant enhancement in diffusion. [115]

4.6   Recombination Mechanisms Limiting Open-Circuit Voltage

It is assumed that the solar cell open circuit-voltage was limited by three main recombination mechanisms: recombination in the quasi-neutral regions, the space charge region, and at the heterojunction interface. Beginning with the recombination in the quasi-neutral regions, the total dark saturation current, J_0, due to recombination of minority carriers is the sum of the dark saturation current in the quasi-neutral region in n$^+$ emitter, J_E, and the p-type base, J_B, as given by equation 4.6.

$$J_{QNR} = J_E + J_B = q \frac{n_i^2}{N_D} \frac{D_p}{L_p} G_1 + q \frac{n_i^2}{N_A} \frac{D_n}{L_n} G_2 \qquad (4.6)$$

Where D_n and D_p are the diffusion coefficients of the minority electrons and holes with associated diffusion lengths L_n and L_p. The terms G_1 and G_2 are coefficients for the emitter and base which depend on front and back surface recombination velocity, emitter and base thickness, as well as minority carrier diffusion coefficient and diffusion length. The emitter was extremely thin and has a high probability for minority carrier recombination compared to the base, due to its large density of dopants and crystalline defects. The cell surface was well passivated due to the SiN$_x$ anti-reflection coating, and the effective surface recombination velocity should be low. Thus, the emitter component of the saturation current, J_E, was ignored since it was the silicon wafer absorber in which most of the photocurrent was produced. The electrical quality of the silicon wafer is critical to device performance. For the base component, J_B, assuming that the diffusion length in the base is much less than the base thickness, and that carriers created deeper than one diffusion length are unlikely to be collected (the long-base approximation), equation 4.6 simplifies to equation 4.7.

$$J_{QNR} = q \frac{n_i^2}{N_A} \frac{D_n}{L_n} \qquad (4.7)$$

For diffusion and recombination of minority carriers in the quasi-neutral zone, the diode ideality factor is assumed to be $n \approx 1$. The limiting V_{oc} for quasi-neutral zone recombination is given by equation 4.8: [116]

$$V_{oc\ QNR} = \frac{kT}{q} ln \left(\frac{J_{sc}}{J_{QNR}} \right) = \frac{E_g}{q} - \frac{kT}{q} ln \left(\frac{qDN_C N_V}{N_A J_{sc} L_{eff}} \right) \tag{4.8}$$

where the bandgap of the absorber is E_g, N_A is the dopant concentration in the absorber, J_{sc} is the cell short-circuit current, and the effective diffusion length, L_{eff}, has been substituted for the bulk diffusion length for electrons, L_n. The effective diffusion length, L_{eff}, for minority charge carriers generated in silicon wafer solar cells is often determined by inverse internal quantum efficiency, IQE^{-1}. Once the external quantum efficiency, EQE, and reflectance, R, are measured the internal quantum efficiency is obtained for each wavelength by $IQE = EQE/(1 - R)$. The plot of IQE^{-1} versus absorption coefficient, α^{-1}, between the wavelengths of 800 to 1120 nm shows two linear regimes (Figure 4.16). [116] [117]
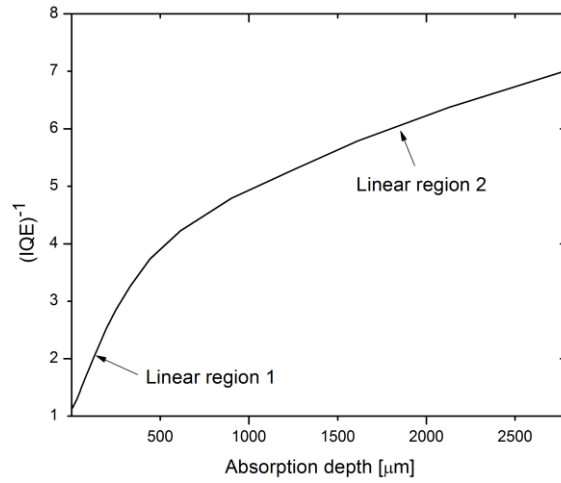
Figure 4.16: Inverse internal quantum efficiency versus absorption depth in crystalline silicon from wavelengths from 800-1100 nm for a solar cell processed by RTA at 900°C for 5 minutes and forming gas

In the first linear regime, photons are of wavelength 800-1000 nm and so absorption and recombination in the emitter is ignored. Also, photons are assumed not to reach the back surface if the wafer is sufficiently thick. It is the first linear region that is analysed here, where the relation between IQE^{-1} and L_{eff} is given by equation 4.9.

$$IQE^{-1} = 1 + \frac{cos\theta}{\alpha \cdot L_{eff}} = 1 + \frac{1}{\alpha \cdot L_{eff}} \tag{4.9}$$

The angle, θ, is zero for refracted light entering a non-textured cell. The effective diffusion length is given by equation 4.10. [116]

$$L_{eff} = L_B \frac{S_b L_n sinh(W/L_n) + D_n cosh(W/L_n)}{S_b L_n cosh(W/L_n) + D_n\ sinh(W/L_n)} \tag{4.10}$$

The effective diffusion length depends on the bulk diffusion length, L_n, the wafer thickness, W, the diffusion constant, D_n, and the back surface recombination velocity, S_b. For a sufficiently thick cell, where $W > 2L_n$, the effective diffusion length is approximately equal to the bulk diffusion length within an accuracy of 4% (within 1% if $W > 3L_n$). [116] Since the cells analysed in this chapter were 500 μm thick, the injected minority carriers in the neutral bulk were likely to recombine before reaching the back surface, and the back surface recombination velocity had little contribution to the dark saturation current. [118] For each of the RTA processed cells from 650°C to 1000°C, reflectance and EQE was used to calculate IQE, and L_{eff} was calculated from equation 4.9. The absorption coefficients for crystalline silicon over the relevant wavelength range were taken from literature. [119] The effective diffusion length at each annealing temperature was determined from the slope of the line and the results are show in Figure 4.17.
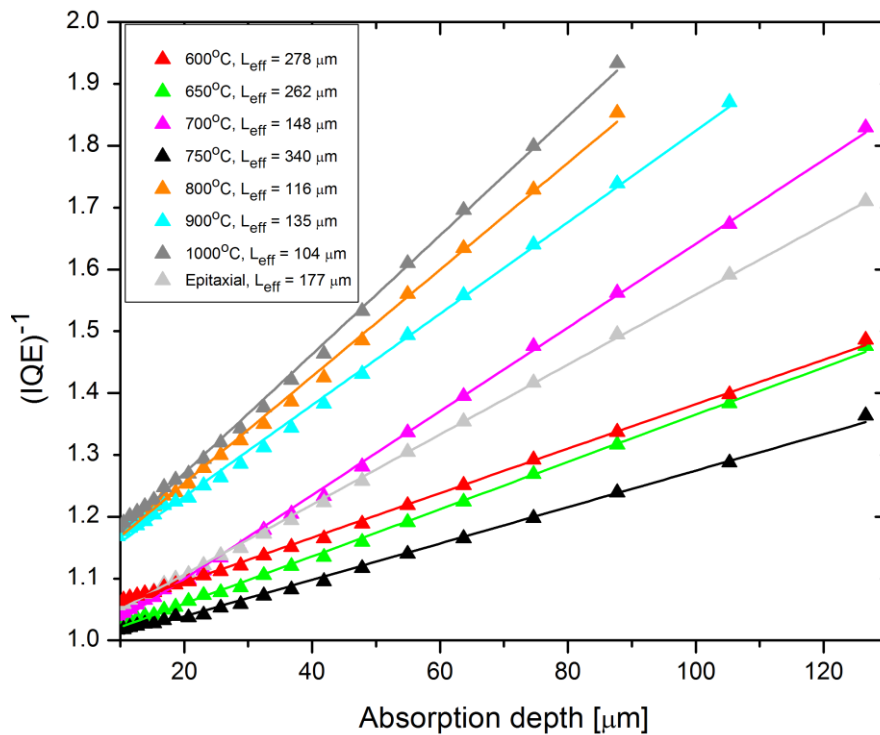
Figure 4.17: Inverse internal quantum efficiency versus absorption depth for solar cell heterojunctions prepared by RTA. Also included for comparison is the low temperature epitaxial emitter cell.

The results for L_{eff} for the various RTA temperatures and for the low temperature processed epitaxial cell are typical of Czochralski silicon wafers.

In addition to recombination in the quasi-neutral regions there is also recombination in the space-charge region. If space-charge region recombination is the dominant recombination mechanism then open-circuit voltage is given by equation 4.11:

$$V_{oc\,SCR} = \frac{2kT}{q} ln\frac{J_{sc}}{J_{SCR}} = \frac{E_g}{q} - \frac{2kT}{q} ln\left(\frac{DkT\pi\sqrt{N_CN_V}}{J_{sc}L_{eff}^2F_{max}}\right) \qquad (4.11)$$

where $F_{max} = 2qN_AV_{bi}/\varepsilon$ is the electric field which is dependent on the built-in potential, V_{bi}. The diode ideality factor is assumed to be $n \approx 2$. The built-in potential is determined by measuring the capacitance, C, as a function of voltage. For an abrupt junction, there is a linear relationship between $1/C^2$ versus V which gives V_{bi} from the intercept with the voltage axis, V_{int}, and dopant concentration in the base from the slope. This analysis applied to homojunctions can also be applied to heterojunctions if the influence of interface states on capacitance is negligible. [120] [121] Furthermore, the value of the intercept voltage may be slightly shifted from the real built-in potential, but the technique can nevertheless provide an approximate value for V_{bi}. [122] In order to measure the built-in potential, capacitance measurements were made at room temperature in the dark using a four terminal pair configuration and an Agilent 4200 SCS parameter analyzer. The signal was 100 kHz applied from the high current terminal, and measured by the ammeter at the low current terminal, while the voltage across the device was measured by the high potential and low potential terminals. Figure 4.18 shows a typical C-V result measured on a finished cell.
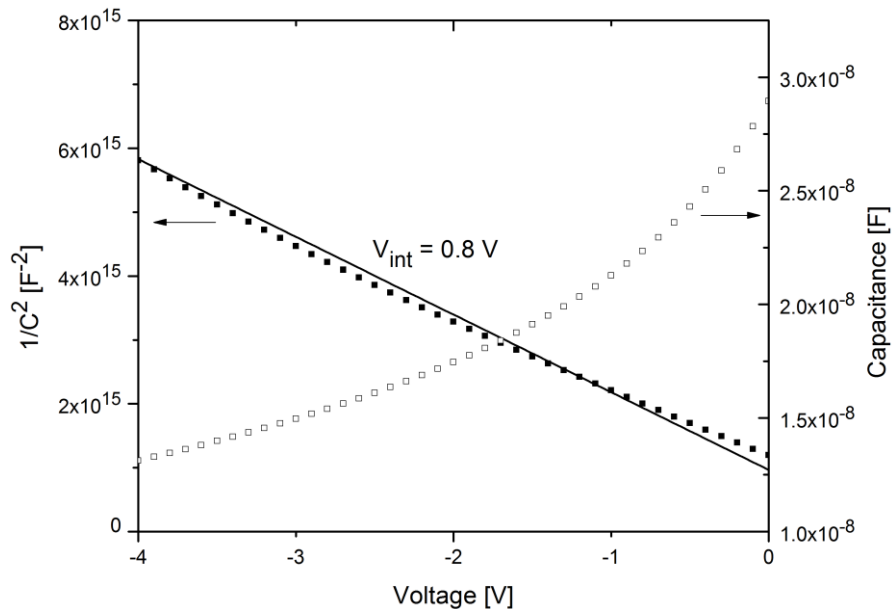
Figure 4.18: Graph of 1/C² versus V for an RTA processed cell at 750°C for 5 minutes. The built-in voltage was 0.8 V.

With V_{bi} measured by C-V, the dopant concentration independently determined by spreading resistance profiling, and the short-circuit current determined by EQE, all the data were complete to calculate the $V_{oc,QNR}$ and $V_{oc,SCR}$ as a function of L_{eff} according to equations 4.8 and 4.11. The limiting voltages for both cases are shown in the inset of Figure 4.19. At low effective diffusion lengths ($L_{eff} < 2$ µm), open-circuit voltage was limited by recombination in the space-charge region. For $L_{eff} > 2$ µm, open-circuit voltage was limited by recombination in the quasi-neutral region of the absorber. The cross-over point between the two recombination mechanisms was $L_{eff} \approx 2$ µm. For each of the seven RTA processing conditions, an average minority carrier diffusion length and open-circuit voltage was experimentally determined as discussed earlier. The V_{oc} and L_{eff} pair corresponding to each RTA condition was plotted in the inset graph and shown in the expanded view of Figure 4.19. For all RTA processed samples, irrespective of annealing temperature, the open-circuit voltage was very close to the upper limit specified by the quasi-neutral zone recombination. The average V_{oc} for each of the seven annealing conditions was within 5% of the maximum V_{oc}.
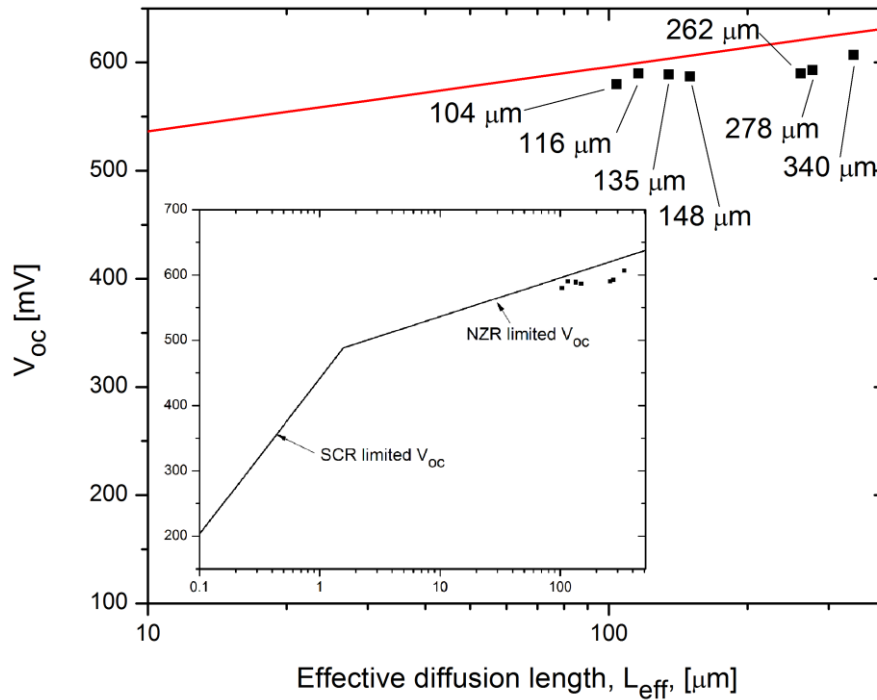
Figure 4.19: Space-charge and quasi-neutral zone recombination limited open-circuit voltage versus effective diffusion length. The red line indicates the quasi-neutral zone recombination limited voltage from theory.

The measured effective diffusion lengths were obviously far greater than the transition diffusion length, and so recombination in the space charge region of the devices was not a limiting factor. Since the device V_{oc} was limited by the electrical quality of the quasi-neutral region in the absorber, the most

immediate avenue to improve cell efficiency was to increase the dopant concentration in the p-type wafer, increase the effective diffusion length, and avoid a reduction in minority carrier lifetime. In order to achieve L_{eff} substantially higher than 300 μm, higher purity Czochralski wafers must be used and the dopant concentration optimized. Alternatively, devices could be fabricated on float-zone silicon which has a significantly lower concentration of impurities due to the absence of a crucible to contain the melt. Another approach which has been proven to give higher V_{oc} in a-Si:H / c-Si heterojunctions and may be applicable to RTA processed cells is to use a p⁺n structure where the absorber is lightly doped n-type and the emitter is highly doped p-type.

Once the neutral zone recombination current becomes sufficiently small, the V_{oc} will now be limited by recombination at the heterojunction interface as characterized by the interface defect density, D_{it}. The saturation current density dominated by interface recombination is given by equation 4.12 where the interface recombination velocity is S_{it}, ϕ_b is the effective barrier height for recombination of charge carriers in the absorber at the p-n interface, $N_V = 1.04 \times 10^{19}$ cm⁻³ is the effective density of states in the valence band, and the diode ideality factor is assumed $n \approx 1$. The corresponding V_{oc} limit due to interface recombination is given by equation 4.13.

$$J_{INT} = qS_{it}N_V e^{-\frac{\phi_b}{kT}} \tag{4.12}$$

$$V_{oc\,INT} = \frac{kT}{q} ln\left(\frac{J_{sc}}{J_{o,INT}}\right) = \frac{\phi_b}{q} - \frac{nkT}{q} ln\left(\frac{qN_V S_{it}}{J_{sc}}\right) \tag{4.13}$$

From equation 4.12, the effective barrier height (shown in Figure 4.20) should be as large as possible to ensure a large V_{oc} and to minimize interface recombination current.
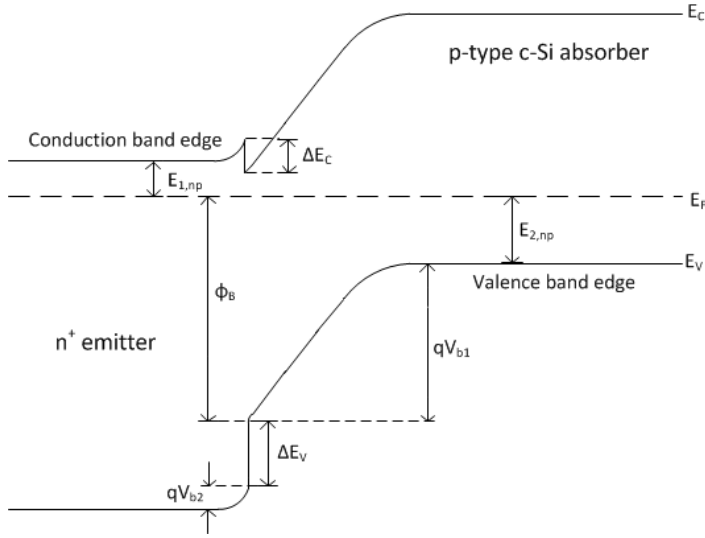
Figure 4.20: Band diagram of a nc-Si / c-Si heterojunction. The valence band and conduction band offsets, ΔE_V and ΔE_c, are exaggerated for clarity.

Combining equations 4.8 and 4.12 to take into account both quasi-neutral zone recombination and interface recombination, open-circuit voltage is given by equation 4.14.

$$V_{oc} = \frac{kT}{q} \ln \left(\frac{J_{sc}}{J_{NZR} + J_{INT}} \right)$$
(4.14)

Using equation 4.14, the limiting V_{oc} as a function of L_{eff} was plotted for several different interface recombination velocities as shown in Figure 4.21.

The effective barrier height, as determined by C-V measurement, was assumed to be $\phi_b = 0.8$ V. The dopant concentration in the wafer was determined by spreading resistance profiling and was approximately 7.9×10^{15} cm^{-3}. For $S_{it} = 10$ cm/s, the interface recombination current only caused a noticeable reduction in V_{oc} for effective diffusion lengths larger than 40 μm. As the surface recombination velocity decreased below $S_{it} = 10$ cm/s, interface recombination current became negligible compared to the neutral-zone recombination current. But, as S_{it} increased, the reduction in V_{oc} became severe as the interface recombination current far exceeded neutral-zone recombination current. The averaged data point for pairs of V_{oc} and L_{eff} for each of the seven RTA temperatures are shown in Figure 4.21. These seven data points were between interface recombination velocity lines of $S_{it} = 10$ cm/s and $S_{it} = 100$ cm/s which was thus an estimate of the quality of the heterojunction interface for these cells. Values of S_{it} within this range are common for amorphous silicon heterojunctions as reported, for example, by Wang et al. [123] and Jensen et al. [124] In a hypothetical best-case scenario, Figure 4.21 showed that the neutral-zone recombination limited V_{oc} for a float-zone

wafer device of dopant density 4.5×10^{16} cm^{-3} could approach 700 mV once $L_{eff} > 400$ μm (assuming negligible interface recombination current).
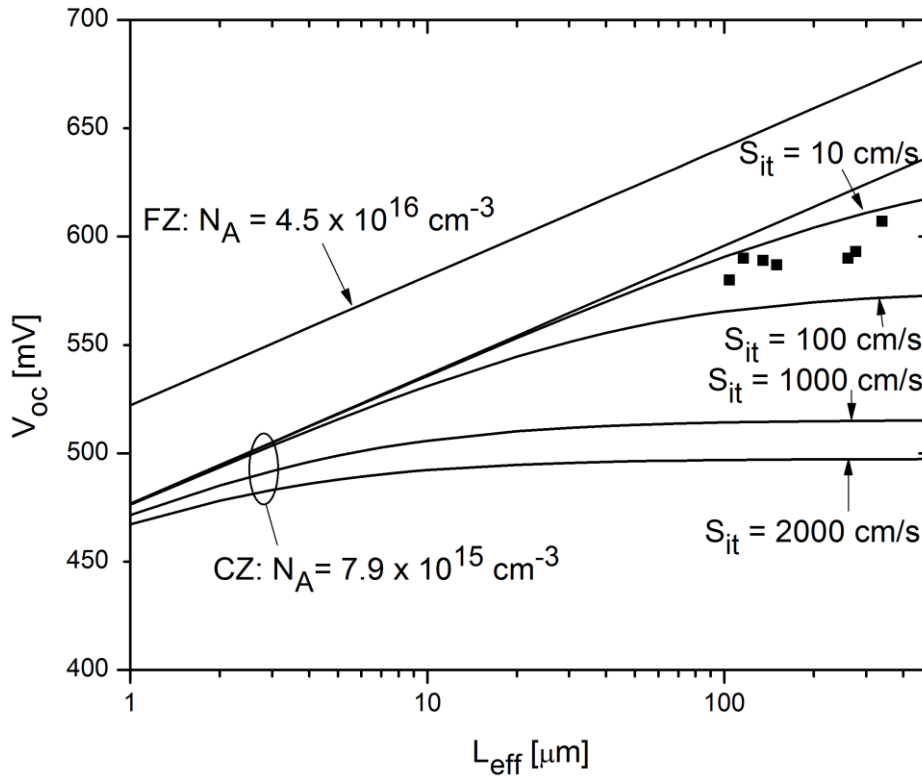
Figure 4.21: Limiting cell V_{oc} is shown as a function of neutral zone recombination in the absorber, and interface recombination velocity, S_{it}.

4.7   Conclusions

Rapid thermal annealing was used to crystallize 50 nm thick n-type a-Si:H films deposited by PECVD on Si substrates. The RTA processing conditions between 600°C to 1000°C indicated a clear peak in solar cell efficiency of 15.1% at 750°C with cell efficiencies decreasing at temperatures above and below this point. Although the best optical and electrical properties for the emitter layers were achieved at RTA temperatures above 750°C, improved quality came at the cost of dopant and impurity diffusion from the emitter into the substrate reducing short-circuit current. Limiting factors for cell open-circuit voltage were divided into three recombination mechanisms: the heterojunction interface, the space-charge region, and the quasi-neutral zones in the emitter and the absorber. Analysis of minority carrier

effective diffusion lengths for RTA processed devices indicated that V_{oc} was limited predominantly by minority carrier recombination in the absorber. Thus, the most direct pathway to improve cell V_{oc} was to optimize the doping concentration in the absorber and increase the minority carrier lifetime by careful choice of annealing temperature and time.

5 Advanced Simulations for Studying the Effect of Heterojunction Interface Defects

Heterojunction solar cells have recombination of photo-generated carriers at the junction interface which can severely limit cell efficiency. The ability to characterize the defect density at the interface is a key step in fabricating high efficiency devices. In this chapter, AFORS-HET was used to simulate the effect of junction interface defects on cell performance by methods of capacitance spectroscopy and electroluminescence. Capacitance spectroscopy refers to capacitance measurements made over a range of frequencies or temperatures at a given voltage bias. There are two types of capacitance spectroscopy used to quantify the defect density at the interface that are applicable to solar cell structures: 1) capacitance measured in the dark as a function of temperature and frequency (C-T-f spectroscopy), and 2) capacitance as a function of frequency (C-f spectroscopy) at room temperature and under forward bias and illumination. These methods are applicable not only to a-Si:H / c-Si heterojunctions but to other device structures including polymorphous silicon and compound semiconductor materials. Basic p-n junction theory is discussed to provide a basis for capacitance spectroscopy analysis.

5.1 Theory of the p-n Junction and Bandgap Defects

The p-n junction is formed by contacting two oppositely doped semiconductors by diffusion, layer growth, or ion implantation. Before thermal equilibrium, a large carrier concentration gradient

exists as the p-type material has a large concentration of holes, and the n-type material has a large concentration of electrons. By diffusion, electrons migrate from the n-side to the p-side exposing positively charged donor ions, N_D^+, and holes migrate from the p-side to the n-side exposing negatively charged acceptor ions N_A^-. The ionized dopant atoms on either side of the junction cause the creation of a built-in electric field directed from n-type to p-type side. The electric field creates a drift current for electrons and holes which exactly counter the diffusion current. Hence, under equilibrium conditions, the net current flowing in the p-n junction is zero and the equations defining the intrinsic carrier concentration, n_i, and the position of the Fermi level, E_F, are given in equations 5.1, 5.2, and 5.3 respectively.

$$n_i^2 = p_o n_o = N_C N_V exp\left(-\frac{E_g}{kT}\right)$$ (5.1)

$$E_C - E_F = kT \, ln\left(\frac{N_C}{n_o}\right)$$ (5.2)

$$E_F - E_V = kT \, ln\left(\frac{N_V}{p_o}\right)$$ (5.3)

The equilibrium electron and hole concentrations are n_o and p_o respectively, the effective density of states in the conduction band is N_C, and the effective density of states in the valence band is N_V. The device temperature is T, and k is the Boltzmann constant. The total electrostatic potential difference, V_{bi}, between the n-side and p-side neutral regions (at thermal equilibrium) is given by equation 5.4: [125]

$$V_{bi} = \psi_n - \psi_p = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right)$$ (5.4)

where ψ_n is the electrostatic potential difference between the intrinsic energy level and the Fermi level on the n-side, and ψ_p is the electrostatic potential difference between the intrinsic energy level and the Fermi level on the p-side (as shown in Figure 5.1). The depletion region width is given by equation 5.5:

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A+N_D}{N_A N_D}\right) V_{bi}}$$ (5.5)

For an abrupt junction ($N_D \gg N_A$) equation 5.5 can be simplified to equation 5.6.

$$W \cong x_{\mathrm{p}} = \sqrt{\frac{2\varepsilon_s V_{bi}}{q N_\mathrm{A}}}$$ (5.6)

For a p-n heterojunction consisting of two different layers, with dielectric constants ε_p and ε_n, the depletion region width on the p-type side, x_p, and the n-type side, x_n, is given by equations 5.7 and 5.8 respectively. The total capacitance is the series addition of the capacitances in each of the two

semiconductors according to equation 5.9. An applied ac bias will cause variations in the space charge density at the depletion region edges.

$$x_p^2 = \frac{2}{q} \frac{N_D \varepsilon_p \varepsilon_n (V_d - V_a)}{N_A (\varepsilon_p N_A + \varepsilon_n N_D)} \tag{5.7}$$

$$x_n^2 = \frac{2}{q} \frac{N_A \varepsilon_p \varepsilon_n (V_d - V_a)}{N_D (\varepsilon_p N_A + \varepsilon_n N_D)} \tag{5.8}$$

$$\frac{1}{C} = \frac{1}{C_n} + \frac{1}{C_p} \tag{5.9}$$

Figure 5.1 shows the thermal equilibrium characteristics of an abrupt p-n junction. [125]
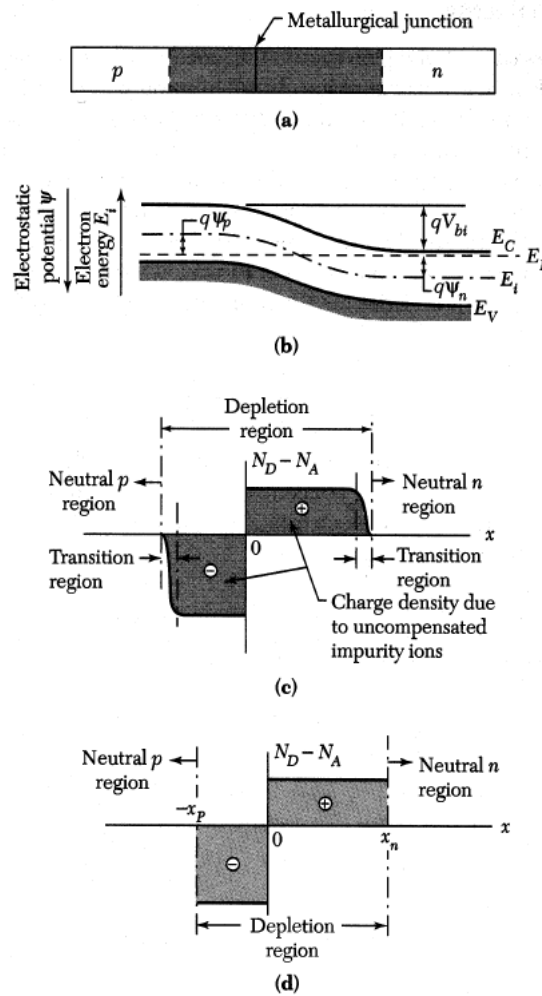
Figure 5.1: a) p-n junction with abrupt dopant change at the metallurgical junction, b) energy band diagram at thermal equilibrium, c) space charge distribution, d) rectangle approximation of space charge distribution made by ignoring transition regions. [125]

In contrast to the perfect band diagram illustrated in Figure 5.1, real semiconductors have defect energy levels within the bandgap. Impurities such as dopants create shallow level impurities which are energy levels near the conduction or valence band edges. Deep level impurities are at or near the middle of the bandgap and can act either as generation-recombination centers or traps. Unintentional impurities may include foreign interstitials (such as oxygen), foreign substitutionals, vacancies, precipitates, or crystal defects such as edge dislocations. The energy level band diagram of a real semiconductor is shown in Figure 5.2. There is an arbitrary deep level impurity at E_T which may be involved in four possible processes: a) capture an electron from the conduction band characterized by capture cross section c_n, b) emit a captured electron back to the conduction band, c) capture a hole from the valence band characterized by capture cross section, c_p, d) emit a hole back to the valence band. Generation occurs when the carrier concentration is below equilibrium. A recombination event is the capture of an electron from the conduction band followed by the capture of a hole from the valence band. Recombination occurs when there are excess carriers. Generation occurs when a trap emits an electron into the conduction band and then emits a hole into the valence band. Trapping refers to when a carrier is captured and then subsequently emitted back to the band from which it came. What determines whether an impurity acts as a trap or a generation-recombination center is the energy level within the band gap, the location of the Fermi level, temperature, and trap capture cross-section. Shallow energy levels tend to act as traps, whereas deep impurity energy levels tend to act as generation/recombination centers. [126]
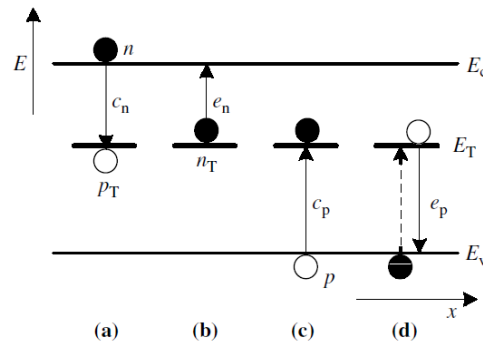
Figure 5.2: Recombination and trapping at defect states within the bandgap. [126]

If the device is cooled and reverse biased, the traps in the p-n junction are filled with majority carriers, and if the device is forward biased or exposed to optical injection then the traps are filled with minority carriers. [126]

5.2 Theory of Admittance Spectroscopy

Admittance spectroscopy is a very useful tool to analyze the bulk and interface states in buried layers in diode-like devices such as solar cells. Electronic states associated with impurities can be divided into shallow states and deep states. Capacitance spectroscopy detects non-radiative transitions from deep states. Deep states often act as recombination centers, and can reduce minority carrier lifetime. The small signal capacitance is sensitive to the capture and release of charge carriers from traps. By definition, the small signal capacitance is the charge response, δQ to a small change in voltage, δV, where $C = \delta Q / \delta V$. Charge may not vary linearly with applied voltage, but with the small signal approximation ($V_a < kT/q = 25\ mV$) it is assumed that $\delta Q \propto \delta V$. [127] [128] Admittance Spectroscopy uses an ac bias and ramps either the temperature and or frequency in order to obtain a response from deep states across a spectrum of activation energies. When a small ac voltage of frequency, ω, is applied there is a linear current response which can consist of two components: one in phase with the applied voltage and another 90° out of phase. For an ideal resistor and capacitor in parallel, the total measured current has a real and imaginary component that is represented by a phasor in the complex plane according to: $I = V(R^{-1} + j\omega C)$. For a diode device such as a solar cell, a parallel circuit model with series resistance, R_s, is assumed as shown in Figure 5.3.
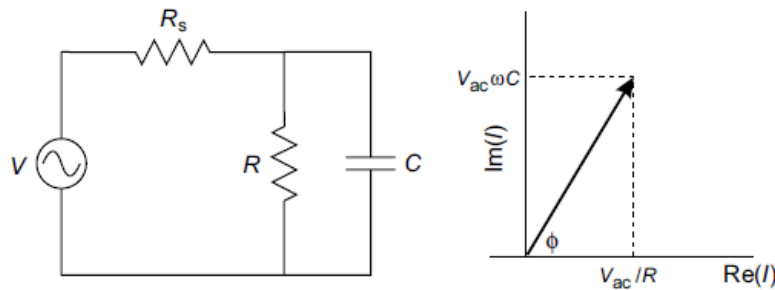
Figure 5.3: Parallel circuit model with series resistance, and phasor diagram for circuit model ignoring R_S. [130]

The small signal response of the sample is defined by the complex admittance, $Y = G + jY'$, where G is the conductance, and Y' is the susceptance. From the parallel circuit model of Figure 5.3, $C = Y'/\omega$. For the parallel circuit model to be valid, $R_S \ll R$, and $\omega R_S C \ll 1$. Too high a series resistance can be caused by series resistance in the device contacts or spreading resistance from a large area sample size. Frequencies above 1 MHz can cause stray inductance. [129] In order to measure the admittance, the ac current response to an applied ac voltage signal is measured. The ac current consists of two components: one which is in phase and a second which is 90° out of phase.

For capacitance-voltage profiling, the depletion approximation is used which states that the depletion region is precisely defined, abrupt, and completely depleted of free carriers. The capacitance response originates from the edges of the depletion region. However, error is introduced for semiconductor films that have a large density of deep states in the band gap. For admittance measurements, the depletion approximation is no longer true, and charge capture and release from deep states has to be taken into account. The activation of a deep trap, causing a transition from one charged state to another, is a thermally activated process which depends on the trap's apparent (measured) cross section, σ_{na}, and activation energy, E_{na}. The thermally activated electron emission from a deep trap is given by equation 5.10.

$$e_n = \gamma \sigma_{na} T^2 exp\left(\frac{-E_{na}}{kT}\right) \tag{5.10}$$

It is assumed that deep traps do not interact with one another and obey the law of superposition (whereby each trap contributes a set of energy levels to the band gap which, added together, form the density of states). When a small signal voltage perturbation is applied, there is a band bending which causes a change in trap state occupation at a given location in the band gap. The occupancy of deep traps is related to the energetic location of the trap with respect to the Fermi level by a Fermi-Dirac distribution. [130] Traps will contribute to capacitance in two ways: i) modifying the space charge density in the depletion region and changing the depletion region width, ii) altering their charge state to dynamically follow the ac voltage contributing to $\delta Q/\delta V$.

The aim of admittance spectroscopy is to alter the sample temperature or frequency so as to cross the transition threshold where traps start to respond. If the sample is too cold, or the modulation frequency is too high, trap states in the bulk cannot respond to the applied voltage to move in and out of the depletion region edge. This is the freeze out zone. Under the freeze out condition, the capacitance will be that of the bulk dielectric given by $C = \varepsilon \varepsilon_o A/b$, where A is the device area, and b is the distance between the front and back contacts. Beyond the freeze-out regime, when the temperature is increased or the frequency lowered, a capacitance step forms increasing from $C = \varepsilon \varepsilon_o A/b$ to $C = \varepsilon \varepsilon_o A/W$ where W is the depletion region width. This first capacitance step is due to the thermal activation of free carriers. As the temperature is further increased or the frequency decreased, the deep trap states can now start to respond. The demarcation energy determines the cut-off energy at which traps will respond to the signal. Demarcation energy is given by equation 5.11, where σ_{na} is the trap cross-section area and ω is the frequency.

$$E_e = kT ln\left(\frac{\gamma \sigma_{na} T^2}{\omega}\right) \tag{5.11}$$

When the trap's apparent activation energy is less than or equal to the demarcation energy, the trap will respond to the ac voltage and contribute to the capacitance by changing its charge state. As the demarcation energy is increased, successively deeper trap states can respond to the signal.

5.3 Capacitance Spectroscopy: C-T-f Method

C-T-f spectroscopy measures the steady state capacitance as a function of temperature, and capacitance steps (or current peaks) are observed as traps emit their carriers by thermal activation. The capacitance is obtained by superimposing a small ac voltage typically in the range of 20 mV, with a frequency between 100 Hz to 1 MHz (although other frequencies and voltages are possible). C-T-f spectroscopy was applied to heterojunction solar cells (a-Si:H on crystalline silicon wafers) by several research groups to analyze the effect of interface defects. Kleider et al. used C-T-f to examine heterojunction cells with different surface treatments such as hydrofluoric acid dip or a layer of tunnel oxide. [131] Unold et al. used C-T-f spectroscopy on heterojunction devices with and without a thin intrinsic a-Si:H layer between the n-type a-Si:H and the substrate. [132] Vischetti et al. used C-T-f spectroscopy to analyze the interface quality of heterojunctions using amorphous and polymorphous emitter layers on p-type wafers. [133] C-T-f spectroscopy is performed in the dark and at zero bias or small reverse bias (up to -0.2 V is common to decrease leakage current). Under these conditions depletion capacitance must be considered. The depletion capacitance of a p-n junction per unit area is given by equation 5.12:

$$\frac{C}{A} = \frac{dQ}{dV} = \frac{\varepsilon_s}{W} \tag{5.12}$$

where W is the depletion region width. For an incremental change in the applied voltage, dV, there is an incremental change in the depletion layer charge per unit area, dQ. Considering a voltage, V, applied to the n-side of a p-n junction, if the voltage is increased by an amount, dV, then charge and field distributions will expand as the depletion region widens. [125] The depletion capacitance is a weak function of applied bias, and dominates under reverse bias. A p-n junction has a space charge region which contains stored charge given by $Q = qN_A N_D W$, where N_A and N_D are the concentrations of ionized acceptors and donors respectively. It is assumed in equation 5.12 that N_A and N_D are constant and do not vary with distance. When an alternating voltage is applied to the junction, gap states due both to the emitter and traps at the heterojunction interface will respond to the modulation. However,

because the voltage drop on the emitter side of the interface is small, and the depletion zone extends much further into the more lightly doped side, the response of gap states in the emitter can often be ignored. A capacitance step will form when the temperature is increased, or the frequency is decreased. The position of the step will depend on the trap capture cross section for electrons and holes, and the magnitude of the step will depend on trap density per area at the heterojunction interface.

Figure 5.4 shows the AFORS-HET simulation for C-T-f spectroscopy of an amorphous silicon heterojunction for the capacitance density as a function of temperature at frequencies of 100 Hz, 1 kHz, 10 kHz, and 100 kHz. Figure 5.5 and Figure 5.6 show C-T-f simulations for a nanocrystalline emitter and epitaxial emitter on a c-Si substrate respectively. In order to simplify simulation, all device structures had a 1 nm thick defective interface layer which was assumed to be entirely within the crystalline wafer. The device layers are listed beneath each figure. For all frequencies, an ac signal of 20 mV was used. Regarding the magnitude of the capacitance density, Figure 5.4, Figure 5.5, and Figure 5.6 all showed a similar trend: for a given interface defect density concentration, D_{it} , the capacitance increased with temperature. The reason for the rise was that, as temperature increased, the built-in potential became smaller and thus the depletion region width decreased. Capacitance increased because of the inverse dependence on depletion region width (equation 5.12).
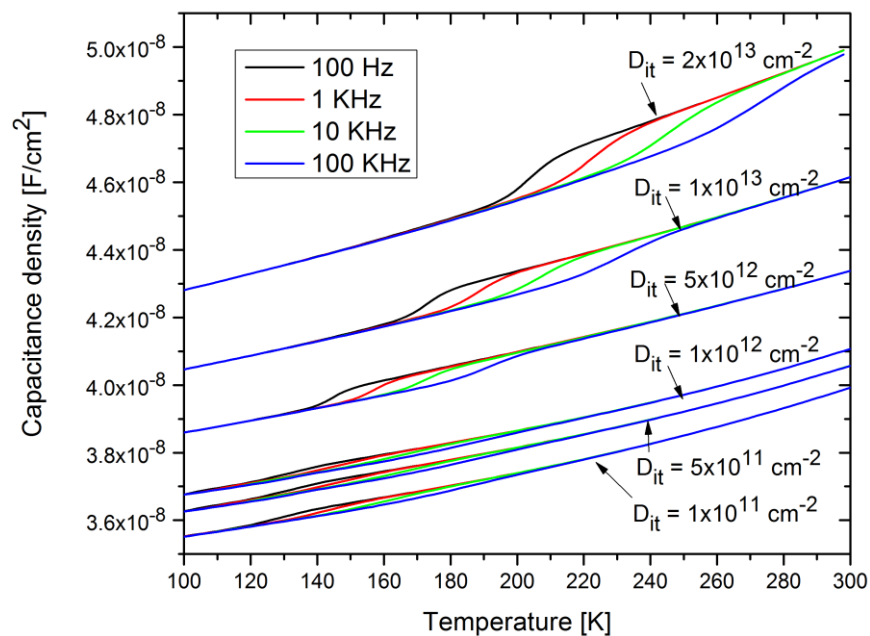
Figure 5.4: C-T-f spectroscopy simulation for a-Si:H/c-Si heterojunction with intrinsic a-Si:H layer. Device was: TCO (80 nm) / (n) a-Si:H (10 nm) / (i) a-Si:H (5nm) / (p) c-Si (1 nm) / (p) c-Si (300 μm) / Al (1 μm).
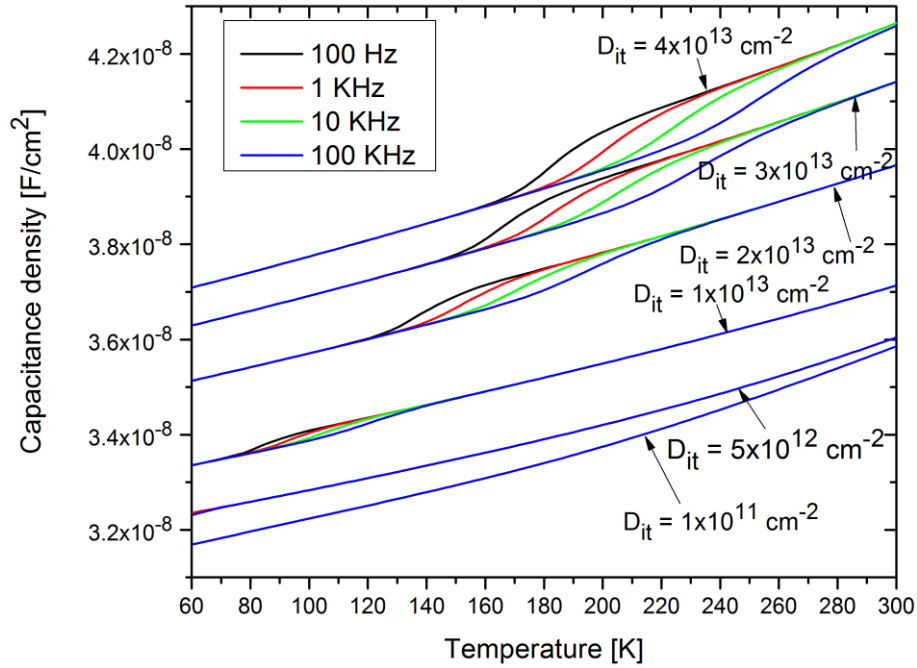
Figure 5.5: C-T-f spectroscopy simulation for nc-Si:H/c-Si heterojunction. Device was: TCO (80 nm) / (n) nc-Si (15 nm) / (p) c-Si (1 nm) / (p) c-Si (300 μm) / Al (1 μm).
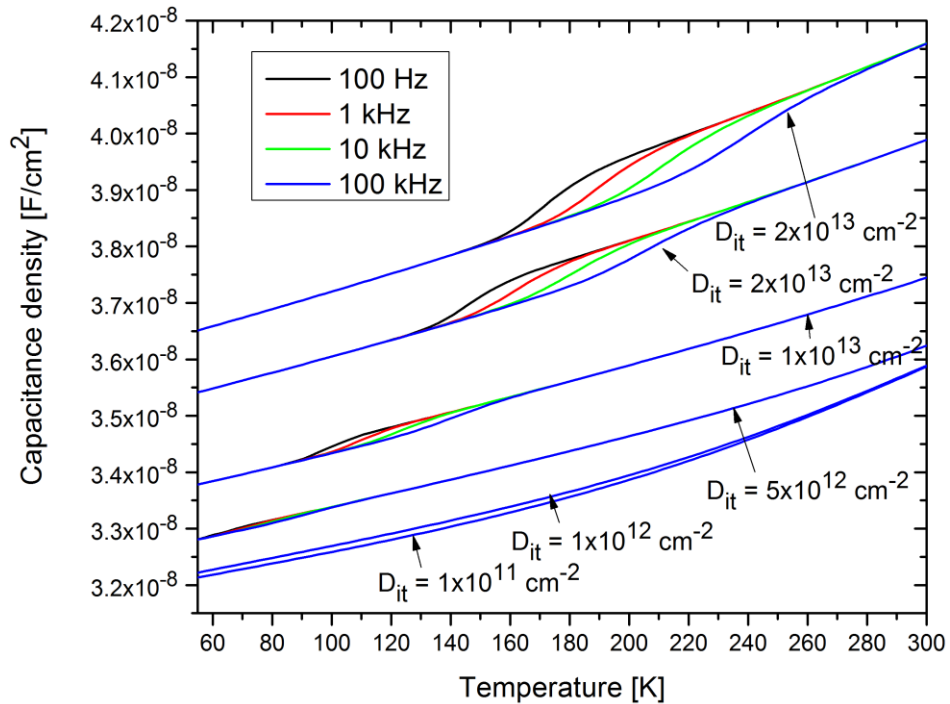
Figure 5.6: C-T-f spectroscopy simulation for epi-Si / c-Si heterojunction. Device was: TCO (80 nm) / (n) epi-Si (15 nm) / (p) c-Si (1 nm) / (p) c-Si (300 μm) / Al (1 μm).

The C-T-f results for all three cell structures were divided into two regions: low interface defect density (typical of high efficiency cells) where $D_{it} < 5 \times 10^{12}$ cm^{-2}, and high interface defect density where $D_{it} > 5 \times 10^{12}$ cm^{-2}.

For the low defect density region, for the nanocrystalline and epitaxial emitters (Figure 5.5, and Figure 5.6) there was a very small capacitance step at temperatures less than 100 K. At all frequencies, for very low defect densities the capacitance values were essentially the same and overlapped forming a single line. The a-Si:H emitter cell in Figure 5.4 showed at all frequencies three small low temperature capacitance steps around 140 K, and the location and magnitude of the steps remained independent of temperature as long as $D_{it} < 10^{12}$ cm^{-2}. The capacitance steps in a-Si:H may have been due to amorphous silicon having a greater density of band gap defects (Gaussian defects and band tails) compared to nanocrystalline and epitaxial silicon. Some of the gap states in amorphous silicon at the heterojunction interface may have responded to modulation frequencies and acted as trap-and-release centers for charge carriers contributing to the junction capacitance. A more general explanation for the low temperature step increase in capacitance for a-Si:H, nc-Si, and epi-Si was the thermal activation of conductivity. For extremely low temperatures, there was a freeze-out regime where there was insufficient thermal energy to ionize dopants and the semiconductor was essentially intrinsic. The dielectric relaxation time is given by $\tau_R = \rho_s \varepsilon \varepsilon_o$ where the resistivity, ρ_s, depends on the bulk conductivity which is thermally activated. [130] Once the temperature was increased beyond the freeze-out zone, the carrier concentration increased and the semiconductor became extrinsic. Carriers in the bulk undepleted material could now respond to the applied ac voltage and shift in and out of the depletion region edges.

In the high interface defect density zone, where $D_{it} > 5 \times 10^{12}$ cm^{-2} there was a much larger increase in capacitance density which could not be explained only by conductivity activation or depletion capacitance. All three cell types showed similar behaviour: there was a large non-linear increase in capacitance which had clear temperature dependence. As the interface defect density was increased, the capacitance step at all frequencies shifted to higher temperatures. Also, the magnitude of the step increased. Below the capacitance step at very low temperature, the capacitance per unit area was dependent on the sum of the depletion region width in the c-Si base, x_p, and the emitter, x_n, according to $\frac{C}{A} = \varepsilon / (x_n + x_p)$. At the onset of the step, the capacitance density changed and was now larger than what could be attributed to the depletion capacitance alone. An additional capacitance was being added in series to the depletion layer capacitance which was the interface capacitance due to the

capture and release of charge carriers at interface traps. According to Kleider and Gudovskikh, the step increase in capacitance for non-negligible interface defect densities can be explained by the concept of the effective depletion length, L_f. The effective depletion length is a kind of Debye length that is a function of the density of gap states which cause a change in capacitance. [131] The smaller the effective depletion length is the larger the defect density at the heterojunction interface. Above the capacitance step, capacitance is now inversely proportional to the sum of the depletion region width in the base (c-Si), and the effective depletion length, L_f, in the emitter according to $\frac{C}{A} = \varepsilon / (l_f + x_p)$. [131]

In the literature, the effective depletion length has been applied to explain the C-T-f spectroscopy of a-Si:H / c-Si heterojunctions, but it can also be applied to C-T-f spectroscopy of junctions with nanocrystalline or epitaxial emitters (Figure 5.5 and Figure 5.6) which showed very similar capacitance steps when the interface defect density was sufficiently high. In all three cases, the rise in capacitance was due to the thermal activation of defects at the

Figure 5.7: a) a-Si:H emitter, b) nc-si emitter, c) epi-Si emitter. The normalized conductance peaks shift to higher temperature as the defect density is increased.

heterojunction interface. The interface capacitance was due to a combination of factors such as: trapping and release of electrons between the n-type emitter and the interface layer, and trapping and release of holes between the interface states and the crystalline wafer. The C-T-f simulations also provided a related parameter, the conductance, which when divided by frequency (normalized) and plotted as a function of temperature showed characteristic peaks. The temperatures at which the normalized conductance peaks occurred corresponded to the locations of capacitance step increase. The conductance results for a frequency of 100 Hz were normalized and plotted as a function of defect

density and temperature as shown in Figure 5.7 for the three emitter types of a-Si:H, nc-Si, and epi-Si. Figure 5.7 showed clear peaks in the conductance at specific temperatures. The temperatures at which these peaks occurred corresponded to the onset of the interface defect induced capacitance steps shown in Figure 5.4, Figure 5.5, and Figure 5.6. For low defect densities, less than approximately $D_{it} = 10^{13}$ cm^{-2}, the conductance peaks were either non-existent (in the case of nc-Si and epi-Si), or for the case of a-Si showed no peak shifting to higher temperature as defect density increased. However, the conductance peaks showed a clear shift to higher temperatures as the defect density was increased beyond approximately $D_{it} > 10^{13}$ cm^{-2}. Taken together, the C-T-f and normalized conductance versus temperature results seemed to indicate a similar response to interface defects regardless of whether the emitter was amorphous silicon or crystalline. When the interface defect density was between $10^{12} - 10^{13}$ cm^{-2} or larger, strong changes were seen in the C-T-f and normalized conductance graphs in the form of temperature dependent shifts of capacitance steps and conductance peaks.

a)

b)

c)
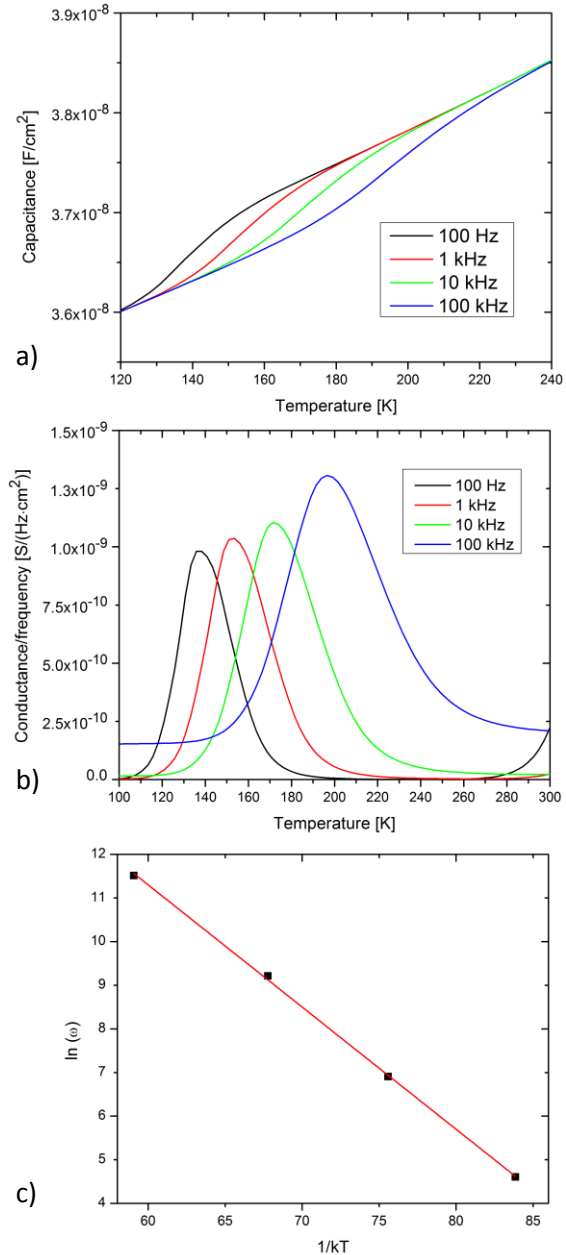
Figure 5.8: nc-Si emitter, a) C-T-f diagram for an interface defect density of 2x10^{13} cm^{-2}, b) corresponding normalized conductance, G/ω, showing characteristic peaks, c) Arrhenius plot yielding activation energy.

A plot of the normalized conductance peaks for a fixed interface defect density can provide information about the defect states themselves. Figure 5.8 a) shows the C-T-f diagram for a nc-Si emitter for an interface defect density of 2×10^{13} cm^{-2}. In Figure 5.8 b), the corresponding graph of normalized conductance showed that the characteristic peaks tracked the onset of activation of the defect states at

the interface. The location of each normalized conductance peak corresponded to a given measurement frequency and turn-on temperature, T_o. At a given measurement frequency, ω, there is a corresponding turn-on temperature at which trap states can begin to respond to the ac voltage signal by changing their charge state by the capture and release of charge carriers. The turn-on temperature is related to the frequency by equation 5.13,

$$\omega = 2\nu_n exp\left(\frac{-E_{TA}}{k_B T_o}\right) \tag{5.13}$$

where E_{TA} is the trap activation energy, and $\nu_n = \sigma_n v_{th} N_c$ is the attempt-to-escape frequency which is the product of the trap cross-section area, σ_n, the root-mean-square thermal velocity of free electrons, v_{th}, and the effective density of states in the conduction band, N_c. Figure 5.8 c) shows the Arrhenius plot frequency versus turn-on temperature. From the slope of the line, the activation energy was $E_a = 0.28$ eV. If the thermal velocity is known, the intercept with the vertical axis provides the trap cross-section area.

5.4   Capacitance Spectroscopy: C-f Method

One drawback of C-T-f spectroscopy is that it is limited in its detection sensitivity of defect density and cannot detect $D_{it} < 10^{12}$ cm^{-2}. However, most high efficiency heterojunction solar cells already have $D_{it} < 10^{12}$ cm^{-2}. In this case, a useful alternative is C-f spectroscopy which has better sensitivity than C-T-f and has been used to analyze the interface defect density in a-Si:H / c-Si heterojunction solar cells by several research groups such as Unold and Gudovskikh. [134] [132] [135]. In addition to providing information about the interface, C-f spectroscopy can also be used to examine the effect of the front and back surface recombination velocity on low frequency capacitance. [132] [134]

Solar cell C-f spectroscopy is performed at Air Mass 1.5 illumination under a forward bias equal to the cell open-circuit voltage. Under open-circuit, no current flows through the device which minimizes the problem of series resistance. [135] C-f spectroscopy is based on diffusion capacitance. Capacitance refers to the stored charge in a device, as illustrated by the parallel plate capacitor where the capacitance is $C = \varepsilon A/d$, where two plates of area, A, are separated a distance, d, by a dielectric insulator with permittivity, ε. The differential capacitance per unit area is the ratio of incremental charge variation, dQ, over voltage variation, dV. Under forward bias, electrons are injected from the n-type to the p-type region where they become minority carriers and recombine with majority carriers in an

exponential decay with distance. Current flow occurs due to the minority carrier distribution gradient leading to charge storage in the p-n junction. By integrating the excess minority carrier hole concentration, $p_n - p_{no}$, across the neutral n-region one can calculate the charge of injected minority carrier holes according to equation 5.14. [125]

$$Q_p = q \int_{x_n}^{\infty}(p_n - p_{no})dx = \tau_p J_p(x_n) \tag{5.14}$$

A similar equation can be derived for the stored electrons in the neutral p-region. Thus, the total stored charge is written in terms of the injected current, J_p. Under forward bias, the diffusion capacitance in the n-type neutral region of a p$^+$n junction, C_{DF}, is due to the rearrangement of stored charges in the neutral region and is given by equation 5.15. [125] L_p is the diffusion length of minority carrier holes in the n-type region. Diffusion capacitance is dominant under forward bias conditions, whereas depletion capacitance has little dependence on the applied voltage and dominates mostly under reverse bias.

$$C_{DF} = \frac{Aq^2 L_p p_{no}}{kT} e^{qV/kT} \tag{5.15}$$

Figure 5.9 and Figure 5.10 a) show the simulation results for capacitance versus frequency for interface defect density concentrations from $D_{it} = 5 \times 10^9$ cm^{-2} to $D_{it} = 1 \times 10^{13}$ cm^{-2} for the three different structures of a-Si:H, nc-Si, and epi-Si heterojunctions. Device structures were identical to those used in the C-T-f simulations and are shown in the inset of each graph. The defective layer was assumed to be entirely within the p-type Si wafer and had a thickness of 1 nm. For all three structures, at low frequencies (10^2-10^4 Hz), a capacitance plateau was present, but as the frequency increased beyond approximately 10^4 Hz the capacitance dropped and approached zero. Furthermore, as the interface defect density increased, the capacitance density, C_{LFP}, at which the low frequency plateau occurred decreased. This was the opposite of C-T-f spectroscopy where capacitance increased with increasing defect density.
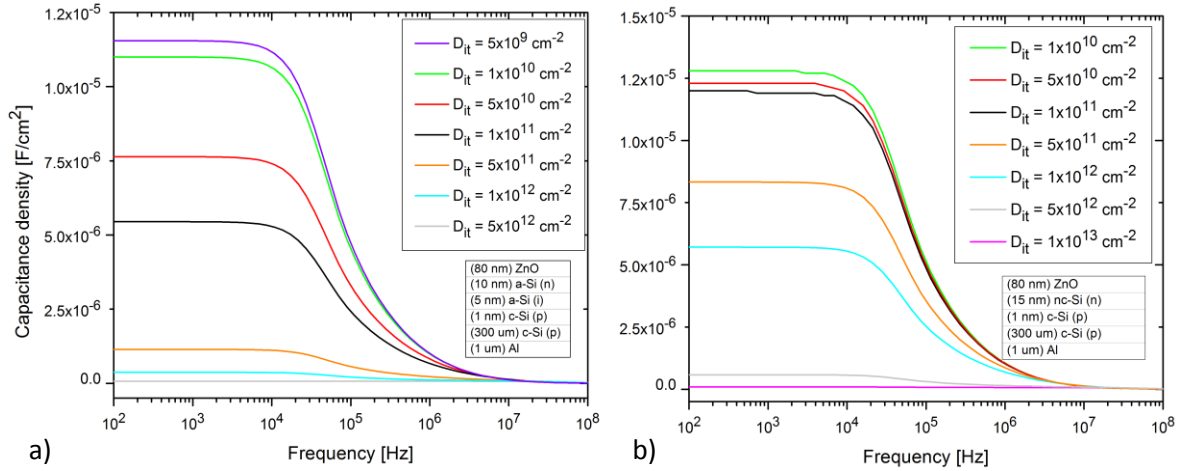
Figure 5.9: a) Capacitance versus frequency for a-Si / c-Si heterojunction. b) Capacitance versus frequency for nc-Si / c-Si heterojunction.

The reason the low frequency capacitance of a forward biased heterojunction decreases with increasing interface defect density is due to the diffusion capacitance. The diffusion capacitance is given by $d\Delta Q/dV_a$ (where ΔQ is the charge due to the minority (electron) concentration in the p-type silicon wafer, and V_a is the applied voltage). The diffusion capacitance depends on the minority carrier charge which is obtained by integrating the excess minority carrier electron density over the quasi-neutral region of the base (in this case the p-type Si wafer). In the simulations, as the interface defect density was increased to non-negligible values (around $D_{it} > 10^9$ cm^{-2}), interface recombination reduced the concentration of excess minority carriers, $\Delta n \equiv n_p(x) - n_{po}$, close to the interface (as shown in Figure 5.10 b). Increasing the interface defect density concentration caused a rearrangement in the minority carrier concentration which reduced the diffusion capacitance causing a reduction in low frequency capacitance, C_{LFP}. The defect density in the emitter layer should not cause an increase in C_{LFP}. The voltage drop across the emitter is relatively small and so the oscillating applied voltage should only change the occupation of defects by no more than a few percent. In addition, the minority carrier concentration is also affected by band offsets and the electrical quality of the back contact which depends on whether or not a back surface field is present.

For solar cells whose thickness, w, is less than the minority carrier diffusion length, L, a back surface field is important to reduce back surface contact recombination. The minority carrier back surface recombination velocity, s_n, is reduced if a back surface field is present (which can be formed, for example, by screen printed annealed aluminum or by forming a high-low heterojunction with a wider band gap material). The back surface field keeps minority carriers away from the back contact and increases their chances of collection. Figure 5.11 shows that as s_n is increased, the excess minority carrier electron concentration, Δn, was shifted down. For higher recombination velocities, Δn decreased not only at the back contact, but also at the heterojunction interface which affected the diffusion capacitance and lowered the absolute value of the low frequency capacitance, C_{LFP}. Thus, C-f spectroscopy was a measure not only of the defect density at the heterojunction interface, but also of the electrical quality of the back contact through

Figure 5.10: a) Capacitance versus frequency for epi-Si / c-Si heterojunction. b) Excess minority carrier concentration as a function of interface defect density for nc-Si / c-Si heterojunction. Conditions were: flat-band ohmic contact, AM 1.5 illumination, and forward bias equal to open-circuit voltage.

the back surface minority carrier recombination velocity. The front surface contact recombination velocity had a negligible impact on C_{LFP} due to the relatively large amount of recombination in the highly doped and defective emitter.
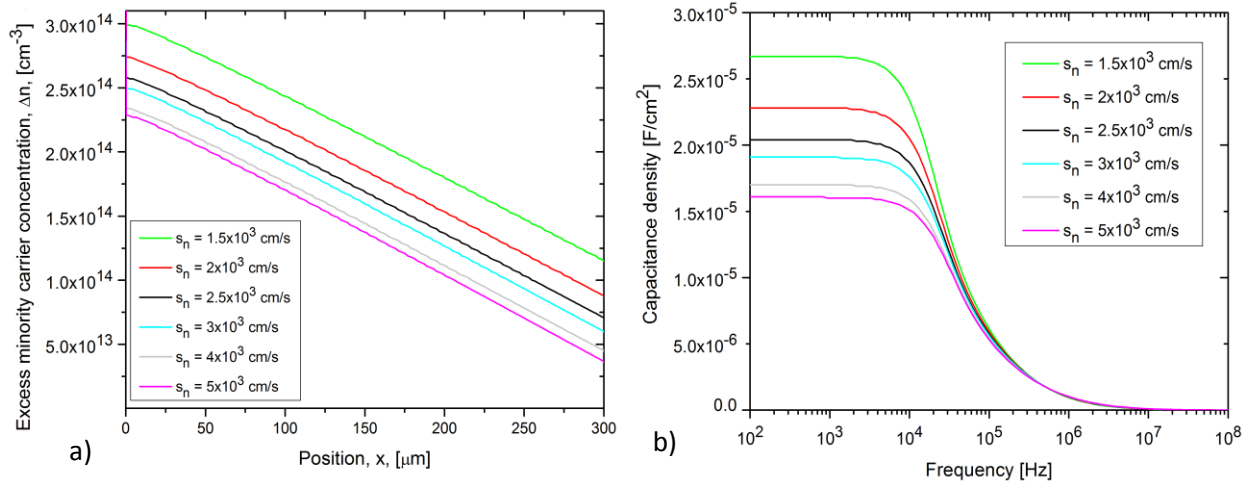
Figure 5.11: a) Variation of Δn in c-Si as a function of position within the junction for six different back surface minority carrier recombination velocities, s_n. b) Reduction in low frequency capacitance, C_{LFP}, as s_n increases.

Another factor that affected C_{LFP} was the conduction band offset. As the conduction band offset was decreased, there was decreased band bending in the c-Si wafer at the heterojunction interface which resulted in reduced electric field strength. The reduced field strength in turn caused an increase in excess minority carrier electron recombination, $\Delta n(x)$, near the junction in c-Si which reduced the diffusion capacitance and the magnitude of C_{LFP}. Figure 5.12 a) shows $\Delta n(x)$ as a function of junction position for five different conduction band offsets for a nc-Si heterojunction. As ΔE_C was decreased, $\Delta n(x)$ decreased as well which was reflected in the reduction of C_{LFP} shown in Figure 5.12 b). Thus, the difficulty with C-f spectroscopy from an experimental standpoint is that the magnitude of C_{LFP} depends not only on D_{it}, but also on the band offset and the back surface recombination velocity (quantities that may not be well known). It is difficult to separate these three influences, although the situation is simplified if a back surface field is used to provide a low surface recombination velocity. If the interface defect density was extremely low ($D_{it} < 10^{10}$ cm^{-2}) then C-f spectroscopy could be used to analyze the back surface electrical contact quality.
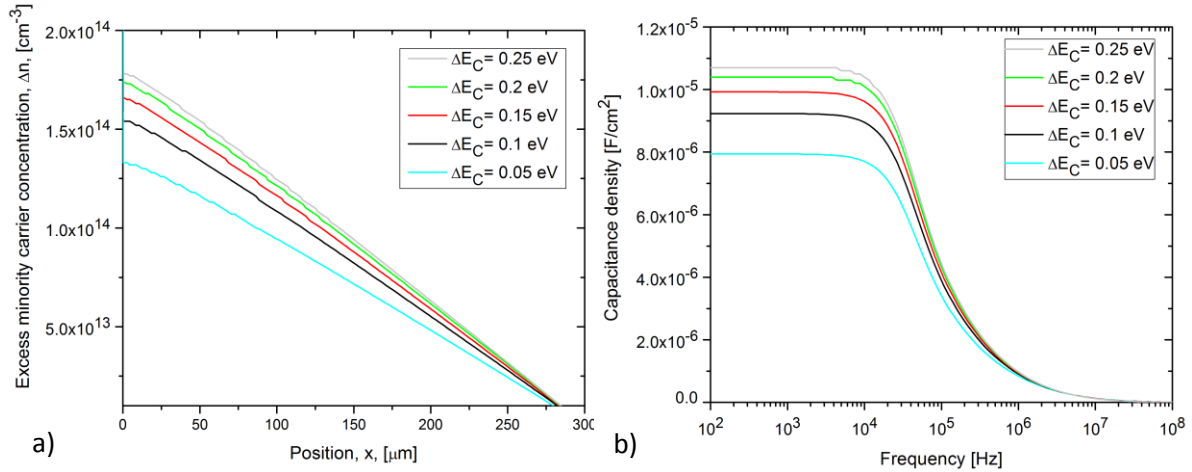
Figure 5.12: a) Effect of conduction band offset on $\Delta n(x)$ for interface defect density of $D_{it} = 1 \times 10^{13}$ cm^{-2}. The device structure was nanocrystalline silicon emitter (n) on p-type wafer, and b) effect of conduction band offset on C_{LFP} as a function of frequency. AC amplitude was 20 mV.

5.5 Electroluminescence

In addition to the methods of C-T-f and C-f spectroscopy, electroluminescence is also an important method for quantifying the interface defect density in heterojunction solar cells. In this section, AFORS-HET was used to simulate the electroluminescence of a cell in the dark under forward bias. The interface defect density between p-type and n-type materials was assumed to be 1 nm thick, and was varied for a nc-Si / c-Si heterojunction. Cell structure was identical to that used in capacitance spectroscopy simulations. Electroluminescence probes excess carrier concentrations in crystalline silicon, and requires electrical contacts in order to forward bias the junction. The emitted spectral radiation provides information on quasi-Fermi level splitting. [136] The quasi-Fermi level splitting and excess carrier density are sensitive to the life time in the bulk, to the surface recombination, or (if the device is well passivated) to the interface recombination. For a silicon wafer passivated with, for example, a-Si:H or nc-Si, electroluminescence will reveal the effect of interface recombination between the wafer and the emitter. Of course, even a moderate interface defect density will reduce the cell open-circuit voltage. As the forward bias is increased, the amount of injected carriers increases which creates increasing recombination (and radiative recombination) which boosts the luminescence signal and causes the solar cell to operate as a light emitting diode. The more efficient the solar cell, the greater the amount of radiative recombination relative to other recombination pathways such as interface recombination. [137] In AFORS-HET, the electroluminescence spectra were calculated using a

generalized Planck's Law that takes into account quasi-Fermi level splitting and the optical absorption properties of the device layers.

The emitted photon flux density from the sample with a given thickness was calculated by accounting for the quasi-Fermi level splitting, $E_{Fn} - E_{Fp}$, and the absorptivity, A_a, according to equation 5.16.

$$dj_\gamma(\hbar\omega) = \frac{(\hbar\omega)^2}{4\pi^2\hbar^3c^2} A_a(\hbar\omega) exp\left(-\frac{\hbar\omega}{kT}\right) exp\left(\frac{E_{Fn}-E_{Fp}}{kT}\right) d(\hbar\omega) \qquad (5.16)$$

The quasi-Fermi levels of the conduction band electrons, E_{Fn}, and valence band holes, E_{Fp}, are defined by $n = N_C exp\left(-\frac{E_C-E_{Fn}}{kT}\right)$ and $p = N_V exp\left(-\frac{E_{Fp}-E_V}{kT}\right)$. Figure 5.13 a) shows the sensitivity of the electroluminescence signal to the interface defect density concentration for the nc-Si / c-Si heterojunction. The larger the defect densities, the smaller the charge carrier concentrations became under forward bias conditions and the smaller the signal. Recombination at interface defects reduced the amount of radiative band-to-band recombination. The maximum luminescence intensity occurred at a wavelength of around 1130 nm which corresponded to band-to-band radiative recombination in c-Si. For high defect densities, $D_{it} > 10^{13}$ cm^{-2}, the luminescence signal became extremely weak, and would be very difficult to measure. The integrated spectral photon flux from 900-1200 nm for two different values of D_{it} is shown in Figure 5.13 b). There was an exponential increase in integrated flux with applied voltage. The cell with low interface defect density, $D_{it} = 1 \times 10^{10}$ cm^{-2}, was a more efficient light emitting diode than the cell with $D_{it} = 1 \times 10^{13}$ cm^{-2}.
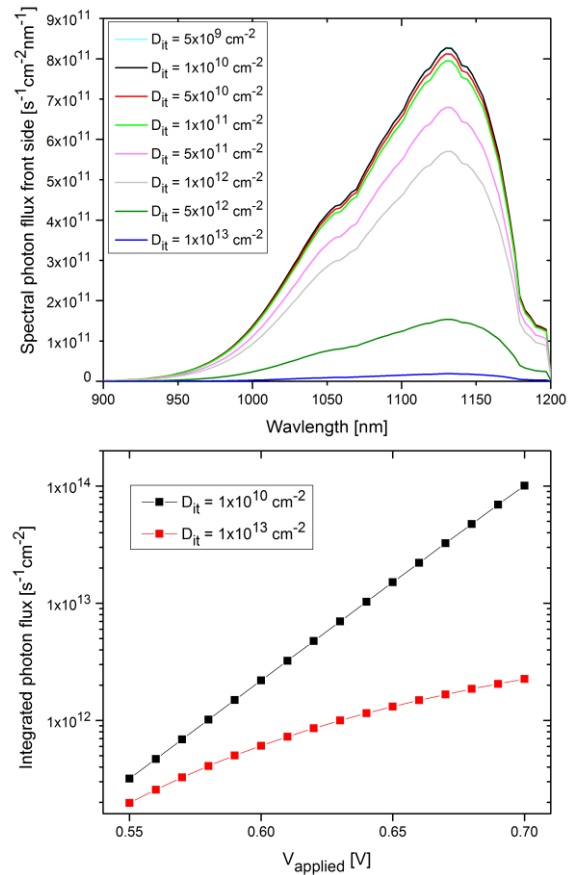
Figure 5.13: a) Electroluminescence simulation for a nc-Si /c-Si heterojunction at room temperature under forward bias of 0.7 V, b) Integrated photon flux as a function of applied forward bias.

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5.6 Conclusions

C-T-f spectroscopy and C-f spectroscopy are fundamentally different in terms of how the capacitance depends on interface defects. For C-T-f, the capacitance was determined by the capture and emission of charges at the interface. However, for C-f, the capacitance was dependent on the recombination of minority charge carriers in the crystalline wafer near the junction interface. Recombination of excess carriers depended on the magnitude of D_{it}, but was also dependent on the conduction band offset, ΔE_c (which determined the band bending in c-Si), and on the back surface recombination velocity. [135] It was clear that interface defects had a very different effect on the measured capacitance depending on whether the measurement was in the dark at zero or slight reverse bias (C-T-f), or at forward bias equal to open-circuit voltage under illumination (C-f). The former method showed an increase in capacitance with increasing interface defect density. The latter method showed a decrease in the absolute value of the plateau capacitance with increasing defect density. A limitation of C-T-f is that capacitance can only be distinguished from the crystalline silicon space charge capacitance when the defect density at the interface is higher than approximately 1×10^{12} cm^{-2}, and this is not sufficient sensitivity for the optimization of high efficiency solar cells. However, C-f spectroscopy and electroluminescence are much more sensitive down to at least $D_{it} = 10^{10}$ cm^{-2}. For the three cell emitter types simulated consisting of epi-Si, nc-Si, and a-Si;H, there was no clear advantage between them in terms of tolerance to interface defects. In the literature, C-T-f and C-f studies have been applied to a-Si:H. This thesis extended these methods to nc-Si and epi-Si heterojunctions.

6 Design, Fabrication, and Characterization of Advanced Photovoltaic Cell Architecture

To improve solar cell efficiencies achieved for the simple cell structure outlined in Chapter 4, several additional processing steps were implemented. Wafers were thinned to reduce recombination losses in the absorber and textured to decrease reflectance. A thin passivating layer of silicon nitride was introduced between the emitter and the substrate. A nanocrystalline p^+ layer was deposited on the back side to form a back surface field and reduce back surface recombination.

6.1 Interface Passivation Layer

Intrinsic a-Si:H is the most common interface passivation material for heterojunction solar cells. But for RTA processed devices, spreading resistance profiling in Chapter 4 showed significant diffusion of dopants into the c-Si wafer at temperatures above 800°C which resulted in a reduced photocurrent. In order to have the benefit of a high mobility low defect density emitter, high RTA temperatures are required. A thin passivating layer of SiN_x can act as a diffusion barrier to impurities and dopants from the emitter, maintain an abrupt junction even at high RTA temperatures, and reduce the density of defects at the junction interface by passivating dangling bonds. However, large band-gap materials like SiN_x or SiO_2 have been noted to block charge carrier transport due to their high barrier potential which results in an S-shaped I-V curve. The band offsets between the passivation layer and the c-Si wafer create substantial barriers to transport of photo-generated carriers across the junction. [138] The band gap of SiN_x is approximately 5 eV, and for SiO_2 can be as large as 9 eV. A thicker buffer layer provides better surface passivation but is also a much greater barrier to charge carrier tunnelling. Lee et al. have used

rapid thermal oxides as passivation for HIT solar cells and have shown that the optimum passivation layer thickness is around 1 nm to 3 nm. [139] Chowdhury et al. have reported a native oxide surface passivation method with a thickness of 1 nm that yields a low surface recombination velocity of 8 cm/s. [140]

6.2   Fabrication on Polished Silicon Substrates

Polished 400 µm thick silicon wafers were thinned using a solution of 30% potassium hydroxide (weight by volume in pellet form in deionized water). Before immersion, wafers were RCA-1 cleaned. Wafers were thinned individually by immersing the Teflon carrier into the thinning solution covered by a glass slide to prevent excessive evaporation. During etching, the temperature of the thinning solution was maintained at 80°C. The etch rate was approximately 2.6 µm/min. Wafers were thinned for 60 minutes until wafer thickness was around 250 µm. Then, the wafers were placed immediately in deionized water for 10 minutes. Wafers were cleaned in a solution of 10 % HCL for five minutes followed by 10% HF for five minutes at room temperature, and then RCA-1 and RCA-2 cleaned again before deposition of device layers. A passivating layer of SiN_x approximately 3 nm thick was deposited by PECVD under the following conditions: power 40 W, 200 mTorr, SiH_4 flow rate 5 sccm, N_2 flow rate 105 sccm, NH_3 flow rate 20 sccm, temperature 350°C, for 10 seconds. Without breaking vacuum, a 40 nm thick layer of n-type a-Si:H was deposited on top of the passivation layer. Next, the sample was flipped and a p^+ nc-Si layer was deposited to form the back surface field. The deposition conditions for the p^+ layer were: power 10 W, 600 mtorr, SiH_4 flow rate 2 sccm, H_2 flow rate 180 sccm, B_2H_6 flow rate 20 sccm, and temperature 280°C for 20 minutes.

After the PECVD depositions were completed, the wafer was annealed by RTA. However, even using the slow ramp rate of 10°C/s that had earlier been established for damage-free annealing, the films were severely pin-holed after temperatures as low as 500°C for 30 seconds. The pin-holing was so extensive (Figure 6.1) that it was impossible to fabricate devices on these wafers. Lower RTA hold temperatures of 400°C, 300°C, and 200°C were used with a ramp rate of 10°C/s, 5°C/s, and 1°C/s but all devices were still pin-holed and cracked. Next, annealing at 200°C in a regular furnace with nitrogen ambient was performed using a very slow ramp rate of 6 hours but this did not solve the pin-hole problem. Because annealing at such low temperatures and ramp rates cannot cause explosive out-gassing of hydrogen from a-Si:H or SiN_x, it was assumed that the reason for the pin-hole formation was the mismatch in thermal expansion coefficients. The coefficient for SiN_x is around 3.3×10^{-6} ^{o}C^{-1}
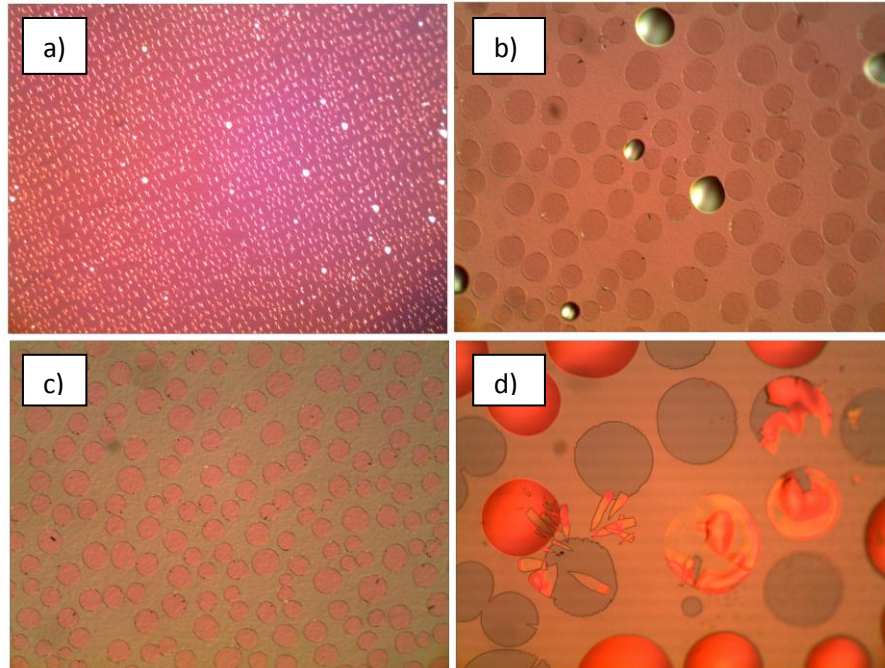
Figure 6.1: Optical microscope view of pinholes after annealing of thin film stack consisting of SiN_x passivating layer and 40 nm thick emitter on Si wafer. a) 2.5 x 10, b) 10 x 10, c) 10 x 10, d) 20 x 10 magnification. Image b) shows pin holes that pass entirely through the emitter and the SiN_x revealing the Si substrate.

whereas for a-Si:H it is 2.3×10^{-6} °C^{-1}. [141] The thermal expansion mismatch in combination with a poor adhesion of a-Si:H to the SiN_x resulted in delamination of the emitter even at low temperatures. A significant amount of time and effort was required to thin a single wafer and deposit all of the PECVD layers, but only one thermal profile could be tested on each sample. Dicing the wafers into five squares of 2.5×2.5 cm allowed multiple thermal profiles to be tested from a single wafer but the quartz tray in the RTA system was only designed to handle whole wafers. Thus, each square had to be mounted on a silicon carrier wafer. But, during the rapid heating cycles, a thin cushion of expanding air formed under the sample during ramp-up. The air cushion caused many samples to float off the carrier wafer and fall onto the bottom of the quartz tube. In order to prevent the samples from sliding during RTA, a silicon sample holder with a square hole was fabricated by laser micromachining (Figure 6.2). The depth of the counter-sunk border was approximately 250 µm. Because the samples were small and thin they were not heavy enough to form reliable contact with the thermocouple and so the holder was designed so that the sample was in the center with the thermocouple touching the periphery of the holder. Although the thermocouple measured the temperature of the holder rather than the sample itself, because both the sample and holder were in direct contact they quickly reached thermal equilibrium. The temperature of the sample and the holder was maybe a few degrees different during ramp-up but

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reached equilibrium during the several minutes during the annealing plateau.
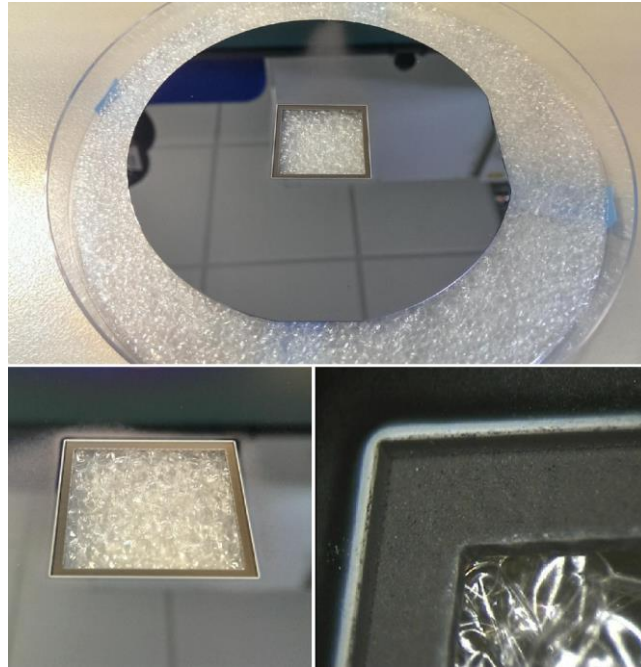
Figure 6.2: Laser machined Si wafer with square opening and detail of counter-sunk border. Laser cutting debris was removed followed by RCA-1 and RCA-2 cleaning.

6.3   Fabrication on Textured Silicon Substrates

Adhesion of a thin film to a substrate can be improved when the substrate is roughened. In order to solve the adhesion problem between the a-Si:H emitter and the SiN_x passivation layer, the PECVD process was performed on thinned and textured Si wafers instead of polished wafers. Wafers were thinned as described earlier, and textured by anisotropic pyramid formation by etching in a solution of potassium hydroxide and 2-propanol. The purity of the potassium hydroxide greatly affected the uniformity of the pyramid coverage as well as the pyramid size. Texturing was initially performed using potassium hydroxide pellets but the pyramid coverage was non-uniform. Therefore, Sigma Aldrich potassium hydroxide solution (semiconductor grade, 45% in deionized water) was used with impurity of potassium carbonate less than 0.3%. The total volume of texturing solution was 1.5 L (67 ml potassium hydroxide and 105 ml 2-propanol in deionized water). The solution was stirred for one minute, covered with a glass slide and heated. Wafers were textured individually submerged in a Teflon carrier. By adjusting the temperature of the hot plate, the solution was maintained at 80°C. Etching time was 70 minutes. After texturing, wafers were placed in an overflowing water bath for 10 minutes. In order to

remove potassium contamination, wafers were cleaned in a solution of 10 % hydrochloric acid for five minutes followed by 10% hydrofluoric acid for five minutes at room temperature, and then RCA-1 and RCA-2 cleaned before deposition of PECVD layers.

Reflectance measurements for three textured wafers are shown in Figure 6.3. The beam spot was located at the center of each wafer and had an area of approximately 1 cm^2. Due to spatial constraints within the loading port, it was not possible to measure reflectance at locations along the wafer periphery. The reflectance at 950 nm was used to compare the reflectance spectra taken from different samples. The average reflectance (without antireflection coating) at 950 nm was 9.68 ± 0.08 %. The low standard deviation indicates that the texturing recipe gave repeatable results for different wafers. The reflectance values agree with those of textured wafers from literature.[142][143][144]
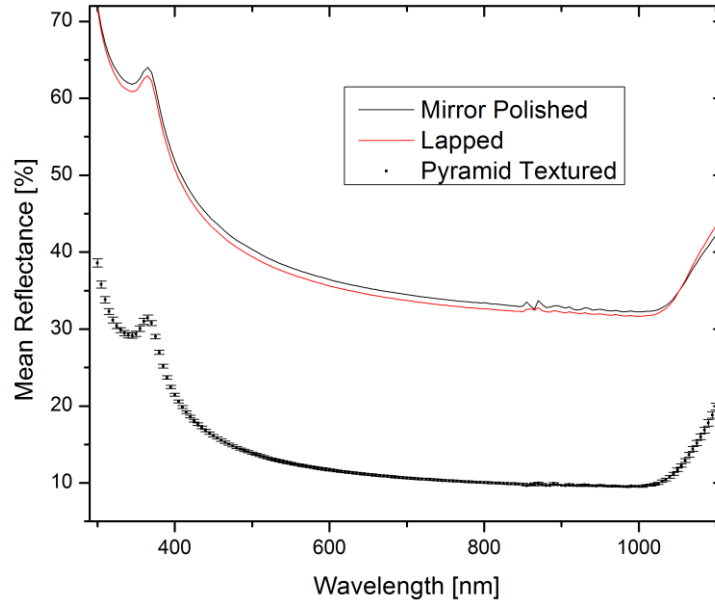
Figure 6.3: Averaged reflectance for three pyramid textured wafers, with the standard deviation given by the error bars. For comparison, the reflectance of a mirror polished and back side roughened Si wafer was also measured.

The textured wafers were examined by SEM and the results are shown in Figure 6.4. The pyramid height was estimated to be between 5-10 µm. After RTA processing, the textured samples showed no pin-hole formation. It is suspected that the pyramid texture improved the adhesion of the emitter to the passivation layer.
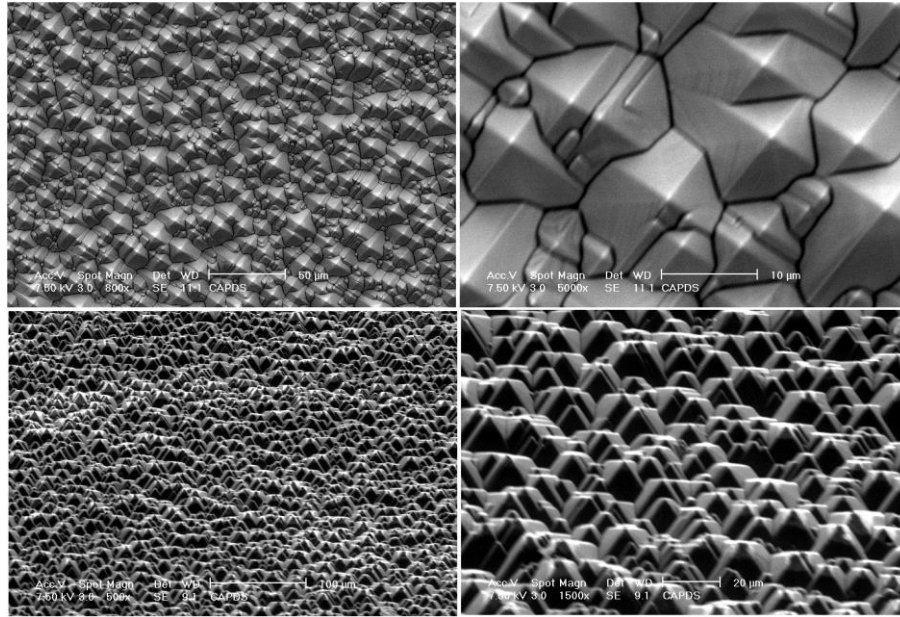
Figure 6.4: SEM results for anisotropically etched Si wafer with 3 nm layer SiN_x and 40 nm n-type emitter.

6.4   Solar Cell Processing and Performance

After RTA processing, an 80 nm thick layer of SiN_x was deposited as anti-reflection coating. Negative photoresist AZ nlof 2035 was used for patterning, but with the standard recipe of 3000 RPM for 70 seconds the resist layer was too thin (3.5 μm) and did not uniformly cover the pyramids. During the lift-off process it was evident that tips of some of the pyramids protruded through the photoresist preventing removal of metal layers needed to form the front contact fingers and bus bar. A modified recipe of 1000 RPM was used for a photoresist thickness of 6 μm. Although coverage of the pyramids with this thicker film was improved, lift-off was unsuccessful. Next, a 10 μm thick photoresist was achieved using 500 RPM for 60 seconds which resulted in excellent pyramid coverage and successful lift-off as shown in Figure 6.5. Pre-bake was for 3 minutes at 110°C, and UV-exposure was 3 minutes (dose of 300 mJ/cm^2). Post-bake was 1 minute at 110°C followed by a 90 second immersion in AZ300 MIF photoresist developer. Before e-beam metal deposition, samples were dipped in buffered hydrofluoric acid for between 30-60 seconds to remove the SiN_x anti-reflection coating. Front contacts were 30 nm titanium and 1 μm silver, and back contact was 1 μm aluminum.
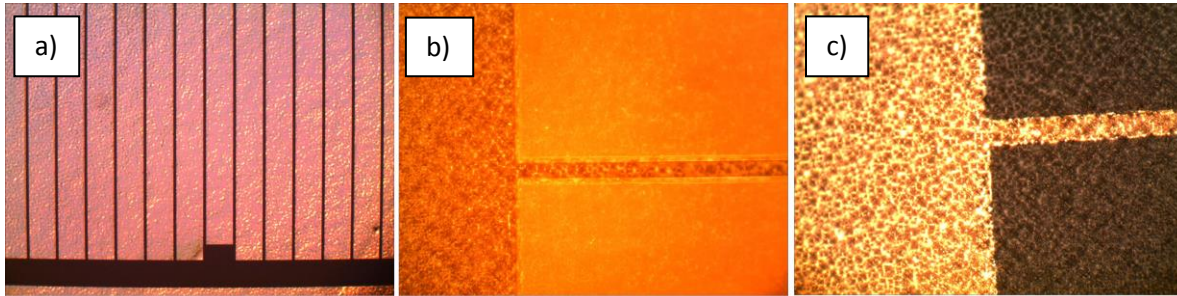
Figure 6.5: Photoresist coverage at 500 RPM for textured samples. a) 2.5 x 10 magnification after UV-exposure, post-bake, and developer, b) 20 x 10 magnification showing photoresist and under-cut necessary for lift-off, c) 20 x 10 magnification showing metallization after successful lift-off.
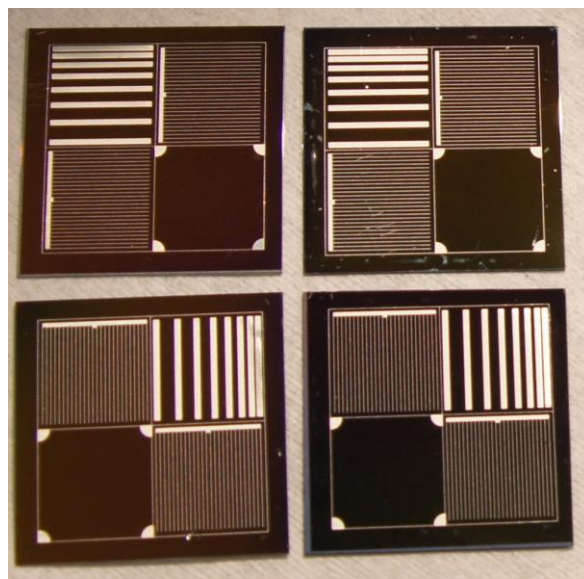
Figure 6.6: Finished devices before dicing. There are two solar cells per square with addition patterns for planar conductance and Hall Effect measurement.

Solar cell efficiency was measured under standard test conditions at AM 1.5. The results are shown in Figure 6.7. Efficiency was below 1% for annealing temperatures less than 900°C. At 1000°C, efficiency started to show a significant improvement as the annealing time was increased. At 1000°C for 1 minute cell efficiency was 1.7% which increased to 6.2 % at 2.5 minutes annealing time. At 1000°C for 10 minutes, 20 minutes, and 30 minutes annealing the cell efficiency remained nearly unchanged at around 10.6 % to 11.5 %. From literature, it is known that the n-type a-Si:H film is completely crystallized at temperatures as low as 600°C for 1 minute.[145] Due to the SiN$_x$ passivation, epitaxy was not possible and the crystallization proceeded by random nucleation and grain growth forming a polycrystalline emitter. The reason for the low efficiency at RTA temperatures less than 1000°C may in small part be due to a higher density of defects in the polycrystalline compared to epitaxial silicon. However, a much

more important reason for the low efficiency was likely the large band gap of SiN$_x$ which hindered minority charge carrier transport. It may be that the large increase in efficiency at RTA temperatures of 1000°C was due to diffusion of phosphorous into the passivation layer which increased its conductivity and lowered the potential barrier for minority carrier electrons allowing them to more easily tunnel through the SiN$_x$ band spike.
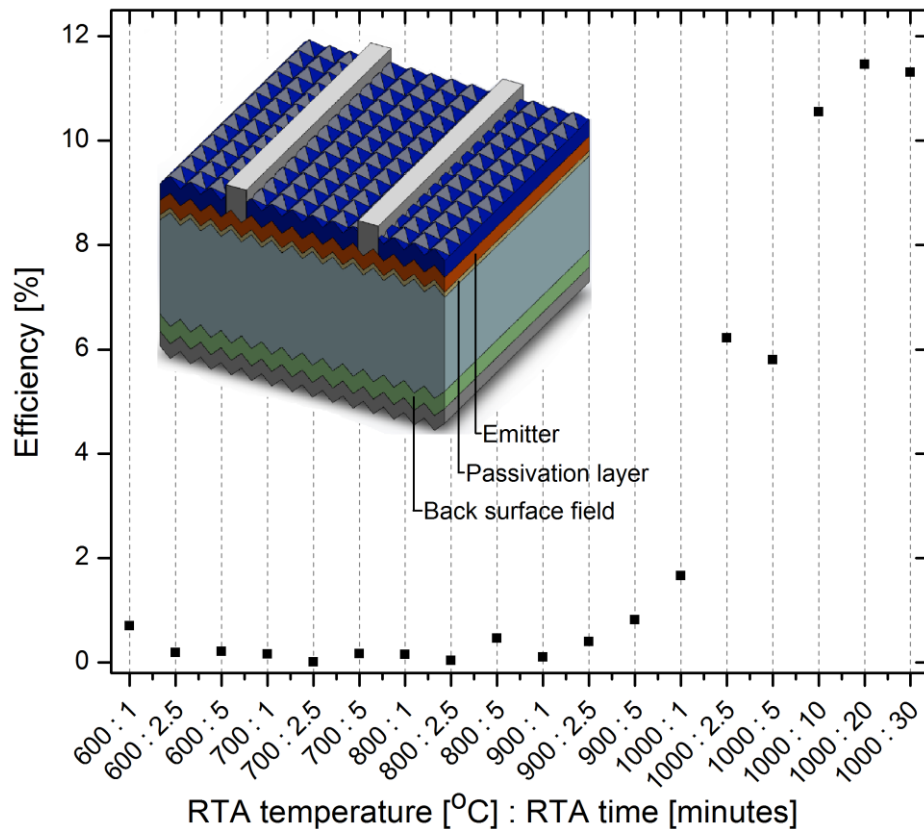
Figure 6.7: Summary of textured cell efficiencies versus RTA plateau temperature and time. Better cell efficiencies were achieved for annealing temperatures of 1000°C for 10 minutes or longer.

Another explanation for the low efficiency may be that the SiN$_x$ layer was too thick. If the thickness were reduced from 3 nm to 1 nm then charge carrier tunneling through the band spike would be greatly increased.

6.5 Conclusions

Although SiN$_x$ is potentially an attractive passivation layer for RTA processed cells, more data are required to assess the defect density at the heterojunction interface to compare with the solar cells in

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Chapter 4 which were without passivation layer. A preliminary cell efficiency of 11.5% was achieved at an annealing temperature of 1000°C for 20 minutes. Further cell improvement could be achieved by reducing the thickness of the passivation layer and minimizing the thermal budget to increase minority carrier lifetime in the Si substrate. Additional investigations could be performed into optimized SiN_x recipes with a reduced band gap. Also, increasing the hydrogen content in the SiN_x layer could be beneficial. The hydrogen would be out-gassed into the crystalline emitter during RTA which would passivate emitter defects such as dangling bonds.

7   Conclusions and Summary of Research

Rapid thermal annealing of thin a-Si:H films was studied for use in photovoltaic cells. The objective of the research was to use RTA to crystallize thin a-Si:H emitters on silicon wafers while simplifying the manufacturing process by avoiding the use of a thin intrinsic silicon passivation layer and transparent conducting oxide. Electrical and optical characterization of the RTA crystallized films showed them to be epitaxial but slightly defective. The most suitable ellipsometric model for the defective epitaxial material was a homogeneous mixture of nanocrystalline and crystalline silicon. However, as the RTA temperature was increased the quality of the epitaxial films greatly improved approaching that of bulk crystalline silicon. Electrical and optical properties of 50 nm thick RTA crystallized n-type silicon films for solar cell applications are relatively unstudied compared to more common techniques of crystalline film formation such as conventional furnace annealing or direct deposition of nanocrystalline silicon by PECVD. The combination of optical and electrical characterization methods in this research provided insight into the epitaxial crystallization process by RTA. Within the context of the larger scientific field and body of knowledge in solid-phase crystallization and photovoltaics, this research provided quantitative information in the areas of epitaxial crystallization, defect density analysis, and photovoltaic cell recombination mechanisms and performance. The defect density type, magnitude, and vertical defect distribution within the crystallized emitter was elucidated by SEM, UV-reflectance, and ellipsometry measurements respectively. The epitaxial crystallization mechanism was clearly illustrated by TEM. Carrier mobility as a function of annealing temperature was provided by Hall Effect, and transport mechanisms of the heterojunctions were studied by dark current-voltage measurements at elevated temperature. Basic solar cells were fabricated on polished silicon wafers, and a **cell efficiency of 15.1%** was achieved for a 1 cm^2 device for RTA at 750°C for 5 minutes. The principal factor limiting the open-circuit voltage of the cells was recombination in the quasi-neutral region of the silicon wafer. Experimental results showed that the recombination velocity at the heterojunction interface was quite low (between 10 cm/s to 100 cm/s). Simulations were performed by approximating the epitaxial films as nanocrystalline material, and comparison was made with defect-free epitaxial and a-Si:H / c-Si heterojunctions. Simulations also focused on quantifying the defect density at the heterojunction interface by capacitance spectroscopy and electroluminescence. While capacitance spectroscopy simulations for a-Si:H / c-Si heterojunctions have been performed by several groups, this research extended the capacitance simulations to nc-Si / c-Si and epi-Si / c-Si devices. For further research for the basic RTA solar cell devices it is important to reduce the thermal budget. The annealing temperature of

750°C provided the highest cell efficiencies compared to the other RTA temperatures. The 750°C annealing for 5 minutes was longer than necessary to completely crystallize the a-Si:H emitter. Exploration to reduce the annealing time should be carried out. It is highly likely that lower annealing times of less than 3 minutes could be sufficient to cause complete crystallization. Very high temperature treatments can cause minority carrier lifetime degradation in Czochralski silicon wafers. A reduced annealing time would have a benefit of a lower thermal budget, reduced film stress, and most importantly would improve the minority carrier diffusion length in the absorber leading to higher cell efficiencies. Additional areas of further research for the standard RTA solar cell structure would be to implement surface texturing and to use thinner wafers.

As a secondary research objective, advanced cell architecture was implemented. Wafers were thinned to reduce recombination losses in the absorber, and pyramid textured to decrease reflectance. A thin passivating layer of silicon nitride was introduced between the emitter and the substrate and a nanocrystalline p^+ layer was deposited on the back side to reduce back surface recombination. Successful fabrication of these devices with efficiency reaching 11.5% (at an annealing time of 20 minutes at 1000°C) showed that silicon nitride as an interface passivation layer was feasible. Further improvements that could be investigated for the advanced cell architecture include reducing the bandgap of the passivation layer to improve charge carrier transport, reducing the layer thickness below 5 nm, and deposition of hydrogen rich SiN_x films. During RTA, hydrogen ejection from the SiN_x layer would passivate interface defects and dangling bonds.

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