High Frequency Receiver Front-End Module for Active Antenna Applications

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

This research is based on the analysis and development of an integrated receiver front-end module for high gain active antenna systems at the K-band ($20\,GHz$). In the design of conventional satellite receivers (such as reflector antennas), the system is usually specified by the gain/directivity, gain-to-temperature ratio (G/T) and radiation pattern requirements. The challenge in high gain active antenna systems development, in addition to beam-forming/beam-steering requirements, is to develop transmit/receive modules which will meet the power, noise and radiation pattern requirements of the conventional antenna. In order to guarantee an optimal design, it is important to be able to translate the specifications from the system level to the transistor level. The focus is on the development of a single-channel CMOS-based integrated receiver module.

The G/T requirement is analysed to derive the noise figure and gain specifications for the low noise amplifier(LNA). An LNA design in $65nm$ CMOS is demonstrated to achieve a $2.6\,dB$ noise figure and uses only $7\,mW$ of DC power. The digital phased shifter specifications are studied. The generation of "quantization lobes" is analysed and used to estimate the number of bits based on side-lobe level requirements. The design of a 5-bit digital phase shifter based on quadrature signal modulation and a unique digital control logic is presented and tested at $20\,GHz$. The phase shifter is shown to achieve $< 5.5^\circ$ rms phase error and $> 10\,dB$ input and output return loss between $16 - 21\,GHz$. The effect of pattern tapering on the side-lobe level is investigated and used to specify the minimum dynamic range for a variable gain amplifier (VGA). A VGA design is demonstrated to meet this dynamic range with low phase-frequency variation.

A schematic level design of the proposed single-channel array is studied featuring a hybrid coupler and switch for polarisation requirements, as well as a low-voltage bandgap reference circuit. Simulations results verify that the receiver can be used to generate two hands of polarisation (right and left) with $< 1.1\,dB$ axial ratio.

Acknowledgements

I would like to thank my supervisor, Professor Safavi Naeini, for giving me the opportunity and encouragement to undergo this research study at the University of Waterloo. His knowledge and expertise in electromagnetic and antenna theory, microwave engineering and wireless communication has been a source of inspiration and direction in my graduate studies and research. I am grateful to have had the chance to complete my dissertation under his guidance.

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I would like to thank my fellow professors who offered valuable advice and courses that have led to my broad understanding of the topics of microwave systems and integrated circuits. In particular, Professor Slim Boumaiza, who offered the course on microwave systems and non-linear circuits and taught me many practical design techniques. Also Professor David Nairn, who taught me Analog Integrated Circuits and offered me advice on Raising and ESD. And also Professor John Long, who gave excellent tips on RFIC layout. Thanks to Hamed Holisaz for seeing my potential and presenting the proposal for this project along with Professor Nabavi, and thanks to all the members of the Centre for Intelligent Antenna and Radio Systems group (CIARS) at the University of Waterloo, for all their support and encouragement throughout my degree.

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Chapter 1

Introduction

1.1 Satellite Communication Link

The basic satellite system consists of two segments, the space segment and the ground segment[1]. The space segment consists of the satellites (Figure 1.1) and their corresponding control station (also known as the Telemetry, Tracking and Command, TT&C, station) which is responsible for monitoring the satellite in orbit. The station may also provide local data services such as backup and security. The ground segment consists of all the earth stations which communicate with the satellite. These could range from large scale base-stations with very high gain satellite antennas, to residential/mobile station with very small aperture antennas (VSAT).
To enable a large number of earth stations to share the satellite communication resources, various multiple access schemes are employed which include:

- Time Division Multiple Access (TDMA)
- Frequency Division Multiple Access (FDMA)
- Code Division Multiple Access (CDMA)

or a combination of two or more of the above.

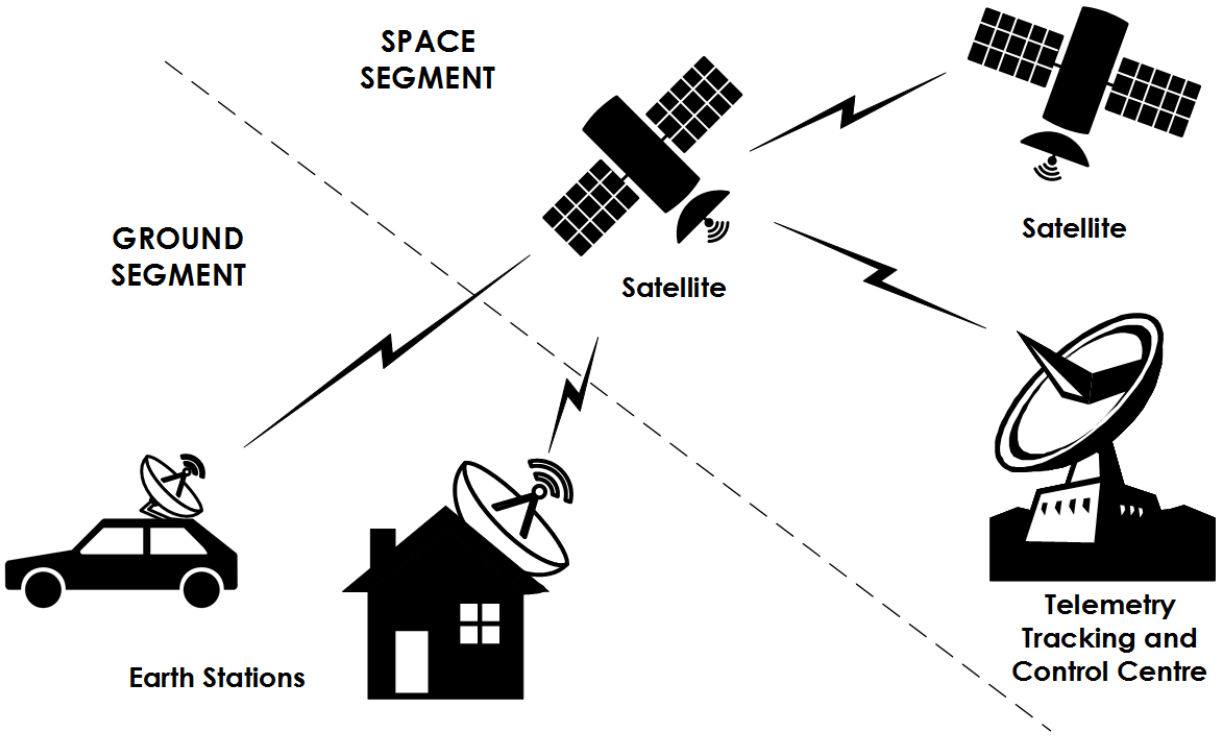


Figure 1.1: Satellite communication system

1.2 Satellite Communication Services

1.2.1 Classification of Satellite Services

Satellite services are provided through the use of spectrum and orbital resources. As these two may cause interference with each other and other systems, a regulatory body is necessary. Satellite communication resources are managed and regulated by the International Telecommunication Union (ITU). Three important satellite services listed in the ITU Radio Regulation(ITU-RR) are the[2]

- Fixed Satellite Service (FSS)
- Mobile Satellite Service (MSS)
- Broadcast Satellite Service (BSS)

Radio bands are allocated to one or more of the above services and differ with geometric regions. Under the ITU Radio Regulation the world is divided into three ITU Regions:

- Region 1 covers Europe, Africa, Persian Gulf, former Soviet Union and Mongolia

- Region 2 covers Americas, Greenland and eastern Pacific Islands
- Region 3 covers Asia, Iran and it's eastern borders.

Figure 1.2 shows the Ka/Ku band spectrum allocation for Canada (Region 2). This dis-

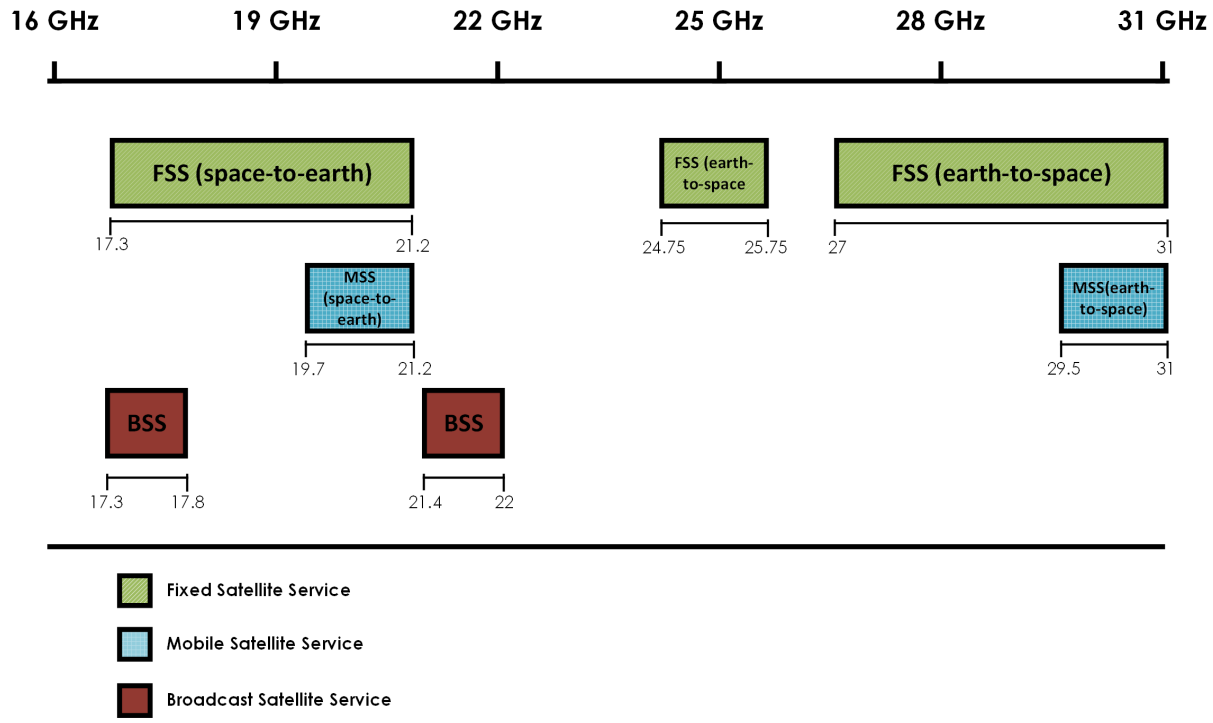


Figure 1.2: Ka/Ku band spectrum allocation for satellite services in canada

sertation is focused on a fixed satellite service(FSS) system.

1.2.2 Fixed Satellite Service

The ITU Radio Regulations defines fixed satellite services in a broad manner as[1]

> 'A radiocommunications service between earth stations at specified fixed points when one or more satellites are used; in some cases this service includes satellite-to-satellite links, which may be effected in the inter-satellite service; the fixed satellite service may also include feeder links for other space radio communication'

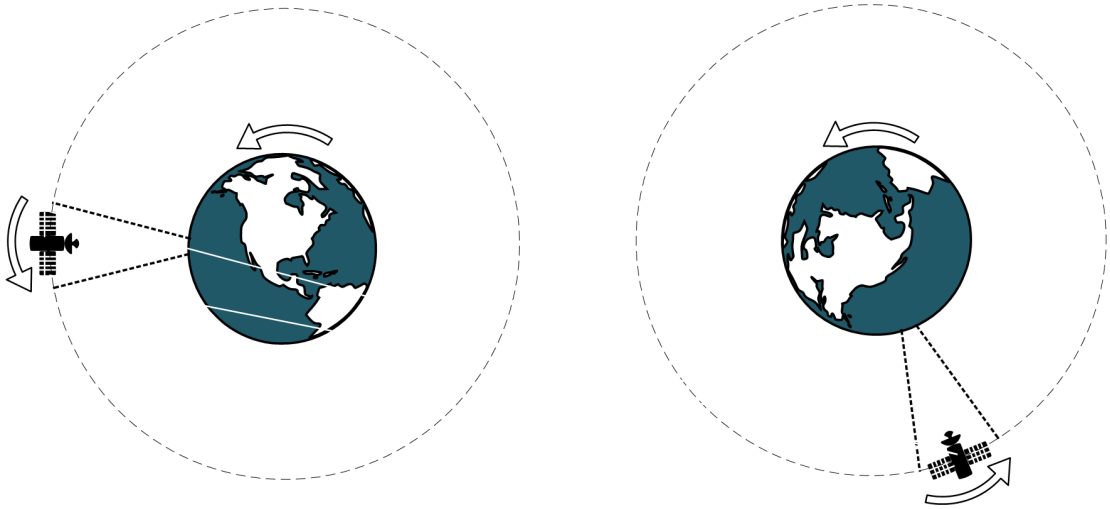


Figure 1.3: Geostationary-earth-orbit (GEO) satellites

Fixed Satellite Services links are provided through Geostationary-Earth Orbit(GEO) satellites (Figure 1.3). These satellites keep pace with the rotating Earth, such that, to an observer on Earth, the satellite in orbit appears stationary[3]. In such a system, the earth stations do not need to track the satellite's spot beam and can be built pointing in a stationary direction at all times. Services provided by FSS include:

- Video Services: Television, Video Distribution, Conferencing...
- Telecom Services: Private Networks, Broadcast, Backhaul...
- Data Services: Data Security, Backup & Restoration...

Earth Stations making use of the FSS service have antenna(s) which could vary between a few meters to tens of meters in diameter. The former group are referred to as Very Small Aperture Terminal (VSAT) antennas and have been in a state of rapid development in commercial satellite communication systems. The size and specification of the antenna is determined from link budget analysis of the communication link.

1.3 Antennas for VSAT Communications

1.3.1 Link Budget Specification

Link budget analysis is used to estimate the minimum specifications for individual components to guarantee a certain quality of service(QoS) in a communication link. Given the

received signal power (P_R), antenna gain (G_R) and transmitter effective isotropic radiated power ($EIRP$), the received signal and noise power at the receiving antenna (see Appendix A) is given as:

$$P_R[dBW] = G_R[dB] + EIRP[dBW] - 20log_{10}\left(\frac{4\pi d}{\lambda}\right) \tag{1.1}$$

$$P_N = kT_sB \;\; W \tag{1.2}$$

From (1.1) and (1.2), the signal-to-noise ratio (SNR) in dB is:

$$\frac{S}{N} = EIRP[dBW] + G_R[dB] - L[dB] - 10log_{10}(kT_sB) \tag{1.3}$$

A term often used to characterize the receiver system is the gain-to-temperature ratio(G/T) in dB/K [4]. Replacing G_R and T_s gives the expression:

$$\frac{S}{N} = EIRP[dBW] + \left(\frac{G}{T}\right)[dB/K] - L[dB] - 10log_{10}(kB) \tag{1.4}$$

(1.4) is the signal-to-noise ratio at the receiver given the system specification, which in turn determines the bit error rate (BER)or QoS. (1.4) is the system link budget for communication in free-space.

Uplink Budget

In *uplink* (see Appendix A), where the transmitter is a VSAT earth station and the receiver is a satellite. The SNR at the satellite is given as:

$$\frac{S}{N} = EIRP_{VSAT} + \left(\frac{G}{T}\right)_{sat} - L - 10log_{10}(kB) \tag{1.5}$$

The satellite G/T is fixed and is usually low due to having a relatively large spot beam. The path loss is determined from the link distance, and fading conditions (rain, multipath,...). Table 1.1 shows the VSAT link budget specification for Satellite Uplink at the Ka-band.

Downlink Budget

In the *downlink* model (Appendix A), the transmitter is the satellite and the receiver is a VSAT earth station. The link budget equation is given as:

$$\frac{S}{N} = EIRP_{sat} + \left(\frac{G}{T}\right)_{VSAT} - L - 10log_{10}(kB) \tag{1.6}$$

The EIRP of the satellite is fixed, and the performance of the earth station is characterised by the G/T value. Table 1.2 shows the receiver specifications for the K-band VSAT satellite receiver. The axial ratio and cross-polarisation discrimination (XPD) are for polarisation requirements, while the side-lobe level (SLL) is required to meet noise and interference specifications.

Table 1.1: Ka-band uplink specification

Specification		**Value**	**Unit**
Modulation	Frequency Range	29.5-30	GHz
	Bandwidth	100	MHz
	Modulation Type	M-PSK	
Tranmitter Specification	EIRP	48	dBW
	Transmit Power	3	W
Antenna Specification	Gain	40	dBi
	Polarisation	RHCP/LHCP	

1.3.2 High Gain Reflector Antennas

VSAT earth station antennas are commonly associated with medium to high antenna gain $(20 - 60\,dBi)$. Generating radiation patterns with such a high directivity is where the reflector antenna has found its most use. The reflector antenna has been used in radio astronomy, medical application and remote sensing after being demonstrated by Heinrich Hertz[5] for radio band communication.
The reflector antenna is designed from a low gain *feed antenna*, which radiates on to

Table 1.2: K-band downlink specification

Specification		Value	Unit
Modulation	Frequency Range	19.7-20.2	GHz
	Bandwidth	100	MHz
	Modulation Type	M-PSK	
Receiver Specification	G/T	12	dB
Pattern Specification	Gain	40	dBi
	Polarisation	RHCP/LHCP	
	Axial Ratio	< 1.3 ($> 20\,dB$ XPD)	
	XPD	> 20	dB
	1^{st} Sidelobe Level	> 20	dB
	n^{th} Sidelobe Level	> 30	dB

a reflector that focuses the beam to the receiver. The most common type of reflector antenna is the parabolic reflector, named for shape of the reflector. A reflector antenna used for residential VSAT communication and multimedia is shown in Figure 1.4.

The parabolic reflector can be designed to meet various antenna specifications. Consider the simplified illustration in Figure 1.5. Given a feed antenna with a normalised gain pattern, $G_f(\theta', \phi')$, the directivity of the parabolic antennas is given as[6]:

$$D_0 = \left(\frac{\pi d}{\lambda}\right)^2 \left\{ cot^2\left(\frac{\theta}{2}\right) \left| \int_0^{\theta_0} \sqrt{G_f(\theta', \phi')} tan\left(\frac{\theta'}{2}\right) d\theta' \right|^2 \right\} \tag{1.7}$$

The term in the braces is known as the antenna *aperture efficiency*, and is less than 1:

$$\epsilon_{ap} = cot^2\left(\frac{\theta}{2}\right) \left| \int_0^{\theta_0} \sqrt{G_f(\theta', \phi')} tan\left(\frac{\theta'}{2}\right) d\theta' \right|^2 \tag{1.8}$$

So, the maximum directivity is given as:

$$D_{0,max} = \left(\frac{\pi d}{\lambda}\right)^2 = A_{ph} \frac{4\pi}{\lambda^2} \tag{1.9}$$

Figure 1.4: Reflector VSAT antenna (Courtesy of iNetVu®)

where A_{ph} is the physical area of the antenna. For example, to generate $> 40\,dBi$ gain at $20\,GHz$, the diameter of the antenna needs to be at least $0.5\,m$. The polarisation, side-lobe levels and bandwidth are determined from the radiation pattern of the feed antenna which also sets the aperture efficiency as shown in (1.8).

1.3.3 Antenna Arrays

Antenna arrays have been a subject of study and design for more than a century. The development of antenna arrays and array theory dates back to early works by Friis[7], Schelkunoff[8], Hansen and Woodyard[9], and many other contributors. Fundamental array theory shows that when N isotropic antenna elements are placed with a spacing, d_x from each other(Figure 1.6), and fed uniformly, the overall pattern has a maximum directivity[6]:

$$D_0 = 2N\frac{d_x}{\lambda} \tag{1.10}$$

This shows that, radiation patterns with high directivity can be realized by using antenna arrays with large number of elements. In terms of the physical size of the antenna, it can

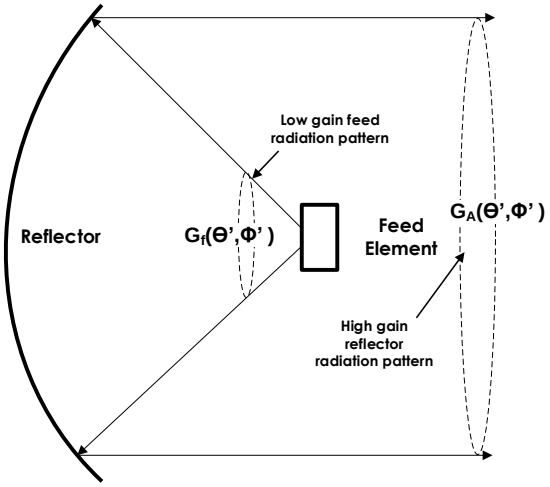


Figure 1.5: Parabolic reflector radiation pattern

be shown that for a 2-dimensional array with N^2 elements, where the length of one side is:

$$L = (N-1)d_x \tag{1.11}$$

the directivity is the product of two linear directivity factors from (1.10):

$$D_0 \approx D_{0x}D_{0y} = \left(2\frac{L}{\lambda}\right)^2 = A_{ph}\frac{4}{\lambda^2} \tag{1.12}$$

Comparing (1.9) and (1.12), a large rectangular array can be used as an alternative to attain high gain radiation patterns. Other pattern characteristics are synthesized by varying the characteristics of the antenna elements, such as:

- spacing
- excitation phase and amplitude
- radiation pattern
- polarisation

Another added advantage of the array antenna is the ability to beam-steer[10]. By adding a progressive phase variation between elements, the direction of the main lobe can be steered electronically. This is especially useful for tracking received signals in time varying environments.

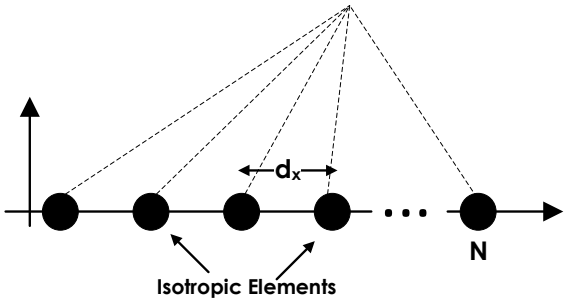


Figure 1.6: Linear array of isotropic antenna elements

1.4 Thesis Objective

Antenna array systems with electronic beam-steering and beam-forming provide a means of optimizing the satellite communication link margin in situations where physical movement of the antenna module either does not provide enough resolution, or is impractical. When used in a feedback control loop, these *smart antennas* are capable of adaptively beam-forming to maximize the received signal and minimize interferences[6]. Smart antennas for automotive radar and communication has been the topic of research and development for over a decade, [11, 12, 13], but a number factors have made the design of such antenna systems very challenging:

- complex transceiver circuits and systems
- power consumption / low efficiency of circuits
- Size
- computation complexity (for adaptive beam-forming)

The first three bullet points relate to the circuits required for gain and phase variation. At microwave frequencies, low noise amplifiers, variable gain amplifiers/attenuators with low phase distortion and high resolution phase shifters are challenging to design. These circuits increase cost and power consumption, which would scale in applications where hundreds to thousands of these components are required. As a result, over-specifying components becomes unaffordable in low-cost antenna development. However, specifications for smart antennas are adapted from the specifications for conventional antennas[4]. These usually relate to properties of the radiation pattern as shown in Table 1.1 and 1.2, which have to be translated to the performance requirements of various sub-systems and components of the smart antenna.

The objective of this dissertation is to investigate the design of an integrated circuit front-end receiver module in CMOS, capable of variable gain and phase control. The intent is to use this front-end module in a low cost VSAT active antenna. When used in a large array, the receiver modules will be able to meet the downlink requirements listed on Table 1.2, as well as provide beam-forming capabilities (Figure 1.7).

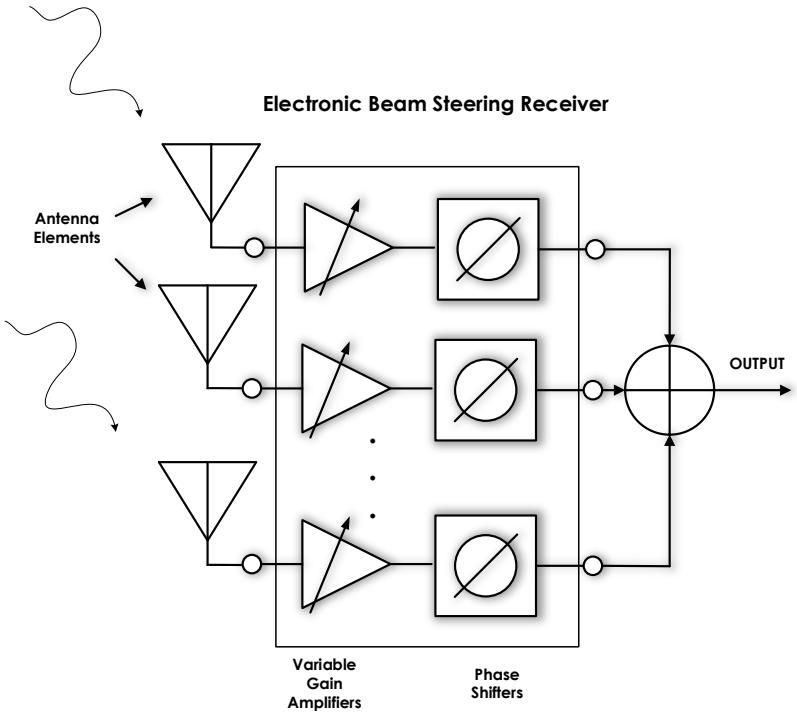


Figure 1.7: Electronic beam-steering receiver

The dissertation will cover the system and circuit level specifications, then present a design of major circuit components. Each chapter will introduce the system level requirements and design implication of each device, then translate them to transistor level specifications. A potential design will be presented based on these requirements accompanied by simulations and/or measurement results. The final chapter will then present a system level simulation of a single receiver channel and it's implications on the radiation pattern.

Chapter 2

Low Noise Amplifiers

2.1 System Noise Considerations

In the introductory chapter, the gain-to-temperature ratio (G/T) of the receiving antenna was introduced as a critical element in specifying the downlink budget. The G/T of a receiver is given as:

$$G/T = \frac{G_A}{T_{sys}} \tag{2.1}$$

where G_A is the antenna gain and T_{sys} is the equivalent noise temperature of the system which consists of the antenna temperature (T_a) and the noise temperature of the feed-network (T_f) due to losses. In active antenna applications, the active and passive beam-forming components also contribute to the overall system temperature.
Consider the antenna array system model in Figure 2.1. Each antenna element has a gain, G_a, with an equivalent antenna temperature, T_a. It is connected to a low noise amplifier(LNA) having a gain, G_{LNA}, through a *feednetwork* with loss, L_f. The beam-forming network contains the phase shifting element for beam-steering, and gain adjustment circuits for tapering. Grouping all the components besides the antenna gain as G_{act}, the overall Gain on the n-th channel, G_n, is:

$$G_n = G_a G_{act,n} \tag{2.2}$$

To include the effect of tapering, the individual active channel gains, $G_{act,n}$, can be normalised to a nominal element gain G_{act} such that:

$$G_{act,n} = G_{act}\frac{1}{L_n} \tag{2.3}$$

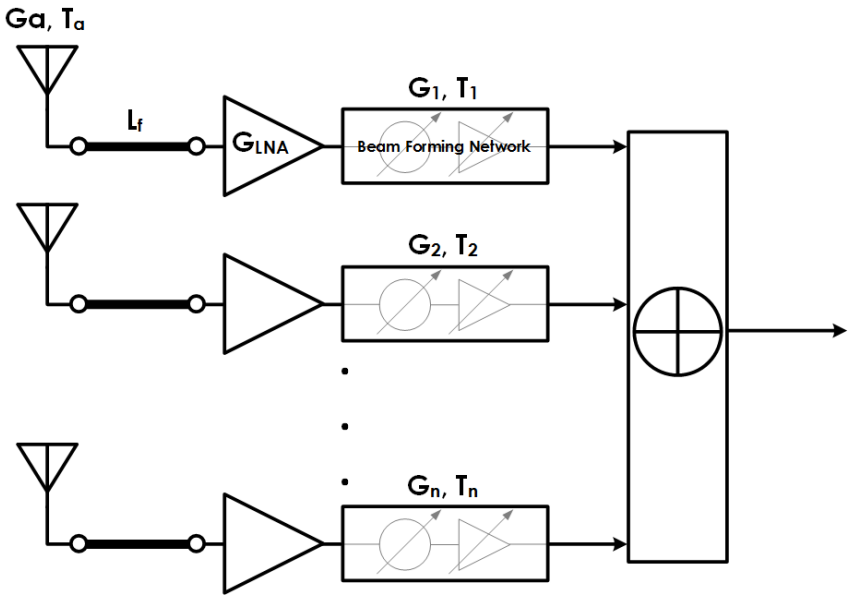


Figure 2.1: Active antenna model for noise consideration

where L_n represents the tapering factor on channel n. If U_i is the received signal amplitude per element, the total power gain at the output is given as:

$$G = \frac{U_o}{U_i} = G_a G_{act} \left(\sum_{n=1}^{N} e^{j\phi_n} \sqrt{\frac{1}{L_n}} \right)^2 \tag{2.4}$$

For the overall noise, let T_n be the average equivalent noise temperature for each channel:

$$\begin{aligned} T_n &= T_i + T_o[F-1] \\ &= T_i + T_o \left[L_f + L_f(F_{LNA} - 1) + \frac{L_f}{G_{LNA}}(F_{BFN,n} - 1) - 1 \right] \end{aligned} \tag{2.5}$$

if the following assumptions are made

1. the LNA is the only "gain element",
2. the beam-forming network is the only source of tapering in the channel,

it is shown in [14] that the G/T of the antenna array is given as:

$$\frac{G}{T} = \frac{NG_a\eta_{ap}}{T_i + T_o\left[L_f F_{LNA} + \frac{L_f L_{BFN}}{G_{LNA}} \frac{N}{\sum_{n=1}^{N}(1/L_n)} - \frac{L_f}{G_{LNA}} - 1\right]} \tag{2.6}$$

where η_{ap} is the *aperture efficiency* given as[15]:

$$\eta_{ap} = \frac{\left(\sum_{n=1}^{N} e^{j\phi_n}\sqrt{\frac{1}{L_n}}\right)^2}{N\sum_{n=1}^{N}\left(\frac{1}{L_n}\right)} \tag{2.7}$$

To highlight the importance of Equation (2.6), consider a case where the low noise amplifier is absent. In (2.6), $G_{LNA} = 1$ and $F_{LNA} = 1$, thus the G/T is:

$$\left(\frac{G}{T}\right)_{\text{no LNA}} = \frac{NG_a\eta_{ap}}{T_i + T_o\left[L_f L_{BFN} \frac{N}{\sum_{n=1}^{N}(1/L_n)} - 1\right]} \tag{2.8}$$

This shows that the G/T of the receiver is not only affected by the loss in the beam-forming network, but is also reduced by the effect of tapering (note that: $\sum_{n=1}^{N}(1/L_n) \leq N$). Now, consider the case where the LNA gain is much higher than the loss of the feed-network and tapering, then the G/T becomes:

$$\left(\frac{G}{T}\right)_{HighG_{LNA}} \approx \frac{NG_a\eta_{ap}}{T_i + T_o\left[L_f F_{LNA} - 1\right]} \tag{2.9}$$

So, to desensitize the system noise performance from the effect of tapering and loss of the beam-forming network, a sufficiently large LNA gain is required. In this case, the G/T is *becomes independent of the LNA gain*, but can still be increased by:

1. Increasing the number of elements and/or the aperture efficiency
2. Increasing the gain of each antenna element
3. Minimizing the feed loss
4. Minimizing the LNA noise figure

To illustrate this, the system under consideration has 4000 antenna elements, each with an antenna gain of $6\,dB$. Assuming an antenna temperature of $290K$, a feed loss of $2.1dB$ and the LNA has a fixed noise figure of $3dB$, the system G/T is plotted in (2.2) for different Beam-Forming Network losses (which incorporate tapering effect). To achieve a G/T of $12\,dB$ and desensitize the effect of the beam forming network, an LNA gain greater than $27dB$ is required.

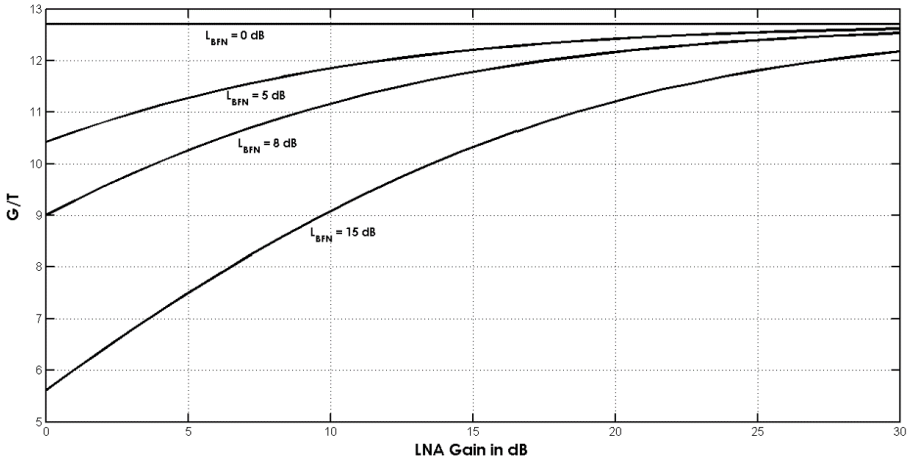


Figure 2.2: Effect of the LNA gain on the system's G/T

2.2 High Frequency Cascode CMOS Amplifiers

CMOS transistors are employed in the design of low frequency circuits, the most common being the operational amplifier [16, 17]. These circuits are built from transistors operating at frequencies ranging from DC to a few megahertz. Op-Amps are characterized by high voltage/current gain ($> 60\,dB$), wideband characteristics, and typically consists of numerous transistor stages. In contrast, high frequency circuits employ transistors operating closer to their unity gain frequency, f_T. They are characterized by low to moderate voltage/current gain ($< 40dB$), narrower bandwidth and increased power consumption. The moderate transistor gain necessitates impedance matching to maximize the power transferred between circuit stages. Figure 2.3 shows the current gain of a $65nm$ transistor, identifying the low frequency and high frequency regions. The $20\,GHz$ operating region is just a decade below the transistor's f_T.

2.2.1 Cascode Amplifier Analysis

Due to the feedback capacitor, C_{gd}, it can be shown that the common-source amplifier exhibits negative resistance for inductive loads at lower frequencies(see Appendix B), which is a typical bias termination in high frequency amplifier. The cascode(Figure 2.4a) on the other hand is shown to be a more stable alternative as an amplifier.

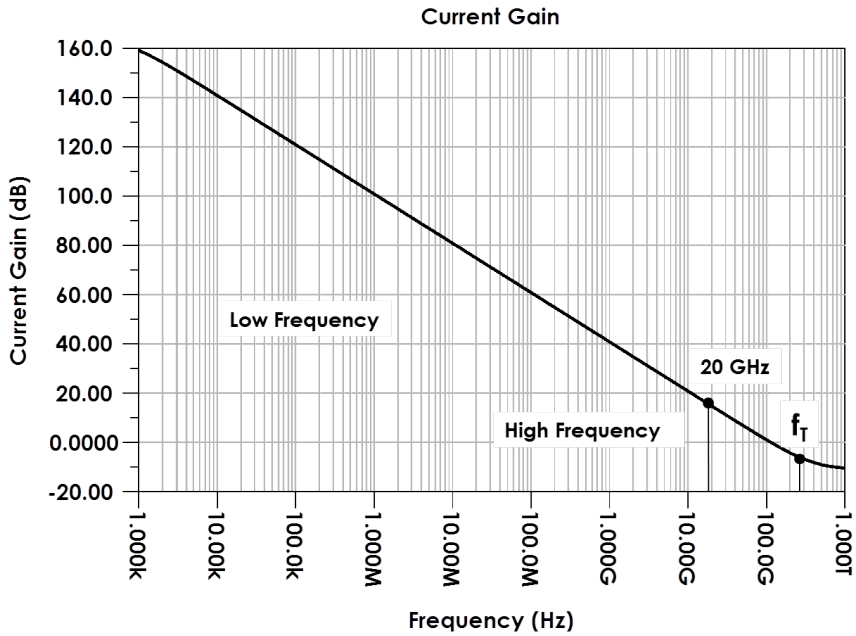


Figure 2.3: Current gain ($\frac{i_d}{i_g}$) of NMOS transistor in $65nm$ technology ($f_T \approx 290\,GHz$)

Gain Performance

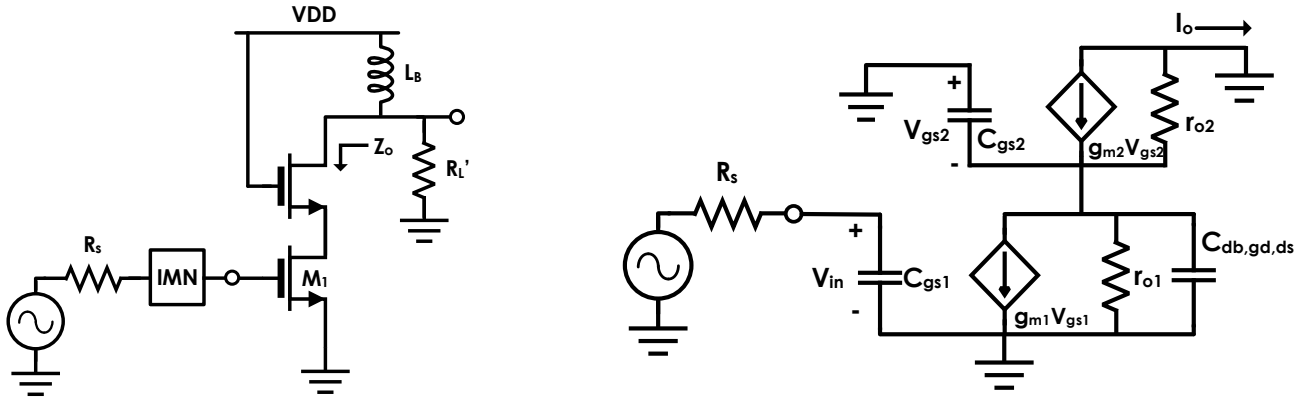
The power gain for a general amplifier is given as:

$$G_{max} = |H_{21}|^2 \frac{R_o}{4R_s} \tag{2.10}$$

where H_{21} is the current gain of device, R_s is the resistance of the source generator and R_o is the output resistance of the device. The common-gate transistor increases the output impedance of the cascode by a factor, $(g_{m2}r_{o2} + 1)$ higher than the the common-source amplifier (Figure 2.5a). The transconductance of the common-source transistor(M_1) is given as:

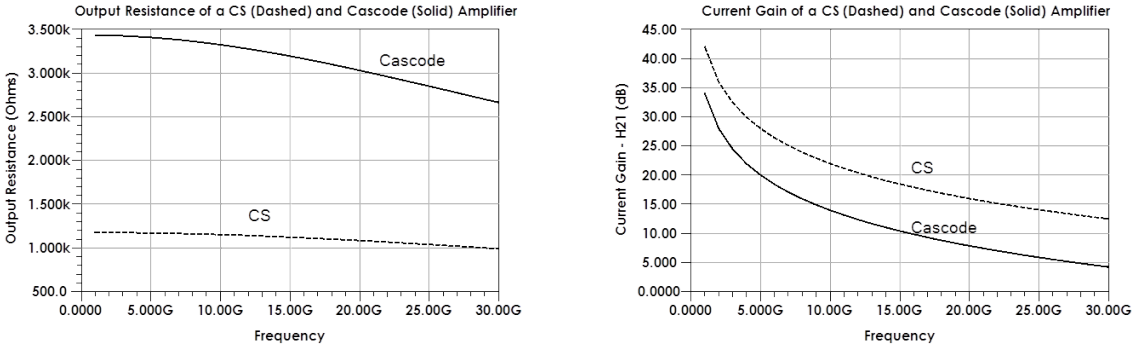
$$g_{m1} \approx \begin{cases} \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D[1 + \lambda(V_{DS} - (V_{gs} - V_t))]} & (V_{gs} - V_t) << E_{sat}L \\ \frac{\mu_n C_{ox}}{2} W E_{sat}[1 + \lambda(V_{DS} - V_{DS,sat})] & E_{sat}L << (V_{gs} - V_t). \end{cases} \tag{2.11}$$

In velocity saturation, the transconductance scales linearly with V_{DS}, and is almost independent of the drain current. In the cascode configuration, the diode connected transistor, M_2, will add a significant voltage drop, leading to a lower V_{DS} in M_1, and resulting in a



(a) Schematic (b) Small Signal

Figure 2.4: Cascode LNA Configuration and small-signal model



(a) Output Resistance (b) Current Gain

Figure 2.5: Current gain and output resistance of a common-source and cascode amplifier

lower transconductance compared to the common-source configuration.

The effective transconductance of the cascode is given as[18]:

$$g_{m,casc} = g_{m1}\left(1 - \frac{1}{(g_{m2}ro_1 + \frac{ro_1}{ro_2})(\frac{1}{1+j\omega C_{gs2}ro_1})}\right) \tag{2.12}$$

and $g_{m,casc} \leq g_{m1}$. The frequency term in the denominator of (2.12) causes a first-order roll-off at $f > \frac{1}{2\pi C_{gs1}ro_1}$, which affects designs at frequencies close to the transistor's f_T. Inductive elements placed in shunt/series at the drain-source terminal create higher order responses leading to "g_m-boosted" amplifiers at high frequencies[19]. To maximize the gain, the common-gate device must be size large enough to minimize the drain-source voltage drop and as well maximize the small signal output resistance.

Noise Performance

The common-gate transistor has a significant impact on the noise figure of the cascode. Consider the noise equivalent circuit of the cascode configuration in Figure 2.6.

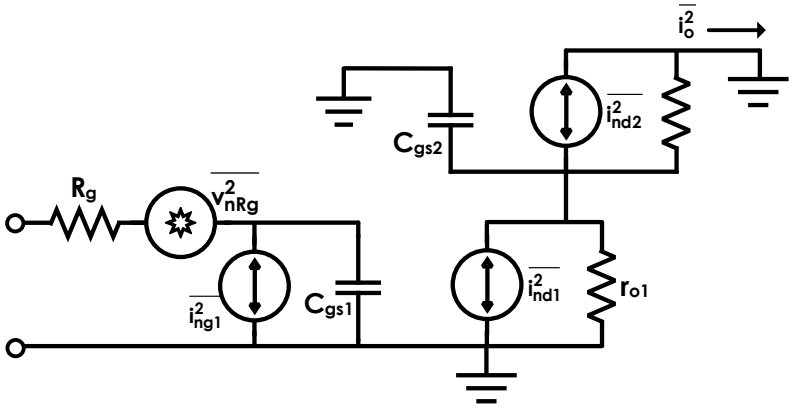


Figure 2.6: Small signal model of a cascode amplifier with channel noise sources

Since the channel noise sources are uncorrelated, the equivalent input voltage source is the *rms*-sum of the two noise sources. Referring the output noise current from $\overline{i_{nd1}^2}$ back

to the input, the equivalent input voltage noise is given as:

$$\overline{v_{nd1}^2} = \frac{\overline{i_{nd1}^2}}{|g_{m,casc}^2|}\left(\frac{ro_1}{ro_1 + ro_2}\right)^2 \tag{2.13}$$

Referring $\overline{i_{nd2}^2}$ back to the input:

$$\overline{v_{nd2}^2} = \frac{\overline{i_{nd2}^2}}{|g_{m,casc}^2|} \tag{2.14}$$

Where $g_{m,casc}$ is the effective transconductance of the cascode configuration (2.12). The overall voltage noise is:

$$\overline{v_{ni}^2} = \frac{4kT}{|g_{m1}K_{casc}|^2}\left(\gamma_1 g_{d0,1}\left(\frac{ro_1}{ro_1 + ro_2}\right)^2 + \gamma_2 g_{d0,2}\right) \tag{2.15}$$

where $K_{casc} = \left(1 - \frac{1}{(g_{m2}ro_1 + \frac{ro_1}{ro_2})(\frac{1}{1+j\omega C_{gs2}ro_1})}\right)$, is the g_m which is less than 1 and g_{d0} is the common-source transconductance at $V_{DS} = 0$ [20]. It is guaranteed that the common-gate transistor adds to the overall noise figure of the cascode compared to a common-source amplifier. As previously mentioned, the common-gate transistor create a large voltage drop and severely lowers the V_{DS} of the common-source transistor. The effect of V_{DS} on g_m is very pronounced in sub-micron transistors which in-turn impacts the noise performance. If the size of M_2 is increased, then $V_{GS,2}$ becomes smaller and g_{m1} increases, decreasing the overall noise figure. However, if M_2 is too large, then ro_2 decreases and the noise contribution of the first term in the parentheses starts to dominate.
The minimum noise figure is plotted against the width of M_2 at $20\,GHz$ in Figure 2.7. For this amplifier, the lowest noise figure is obtained when the common-gate device is $55\,um$.

Input Matching and Matching Network

It is required that the amplifier is impedance or noise matched to an off-chip Antenna element. Neglecting the parasitic resistances at the gate (from poly-silicon and contacts), the input admittance of the common-source transistor is given as (see Appendix B):

$$\begin{aligned} G_{in} &= \omega^2 C_{gd}^2 R_L\left(1 - Q_L\frac{g_m}{\omega C_{gd}}\right) \\ B_{in} &= \omega C_{gs} + \omega C_{gd}(1 + g_m R_L + \omega C_{gd} X_L) \end{aligned} \tag{2.16}$$

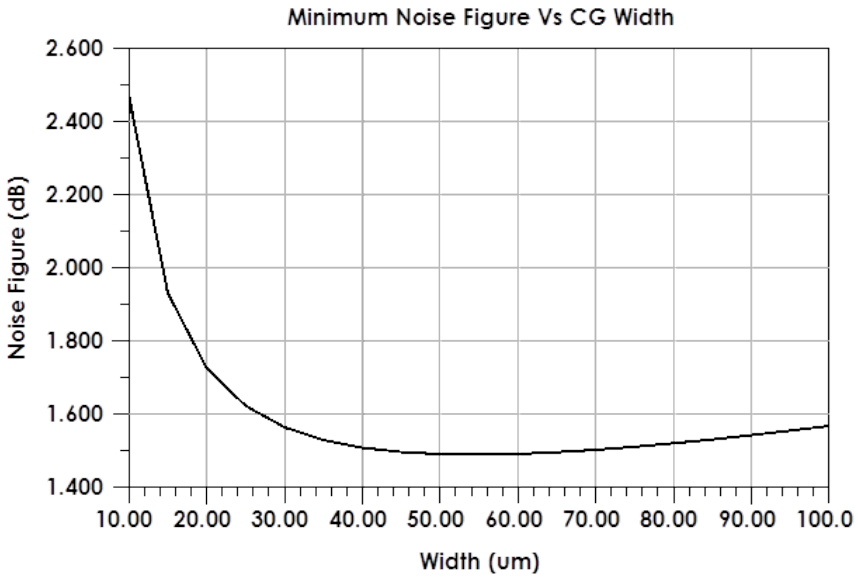


Figure 2.7: Minimum noise figure variation with the width of the common-gate device

where Q_L is the quality factor of the load. Note that the "load" in this equation is the impedance looking into the source of the common-gate stage. The quality factor of the input is expressed in admittance terms as:

$$Q_{in,p} = \frac{B_{in}}{G_{in}} = \frac{C_{gs} + C_{gd}(1 + g_m R_L + \omega C_{gd} X_L)}{\omega C_{gd}^2 R_L \left(1 - Q_L \frac{g_m}{\omega C_{gd}}\right)} \tag{2.17}$$

The quality factor approaches infinity at low frequencies and, from the term in the denominator, monotonically decreases as the frequency increases (Figure 2.8).

The series resistance in most cases is much less than 50Ω and needs to be transformed to higher impedances by a matching network. Two basic matching networks capable of this transformation are shown in Figure 2.9. The noise figure of the *shunt element* contributes to the equivalent *input current noise* (open circuit input), while the *series element* contributes to the equivalent *input voltage noise*. The equations for the equivalent input voltage and current noise is:

$$\begin{aligned} \overline{v_{i,n}}^2 &= 4kTR_{Ms} \\ \overline{i_{i,n}}^2 &= \frac{4kT}{R_{Mp}} \end{aligned} \tag{2.18}$$

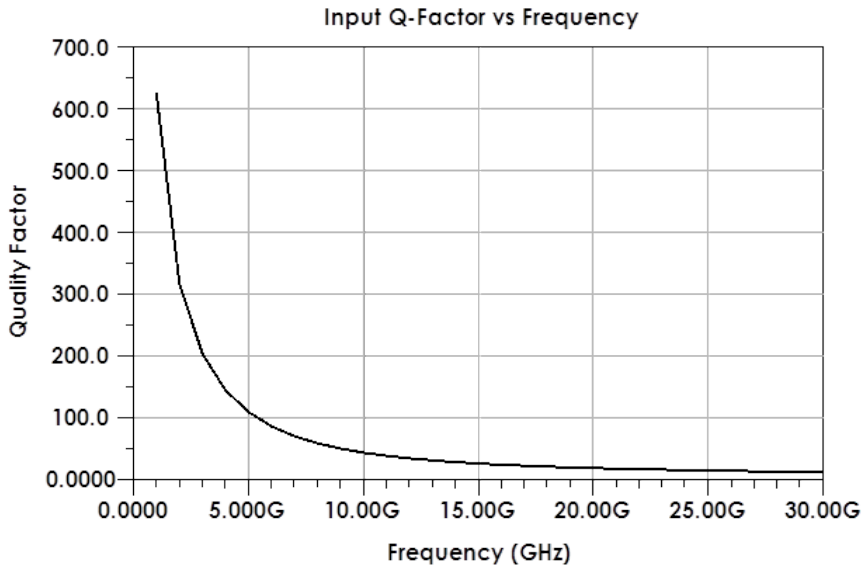


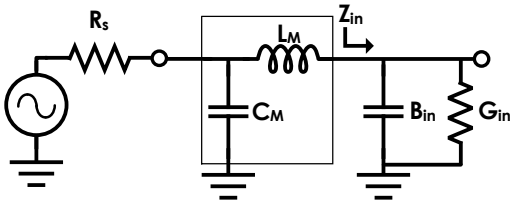
Figure 2.8: Quality factor of the cascode transistor

R_{Ms} and R_{Mp} are the series and parallel equivalent losses of the series and shunt element respectively. The choice of what element to place in shunt or series is strongly dependent on the quality factor of the components at the required frequency. Below the millimeter wave frequency ($30GHz$), capacitors will have a higher parallel quality factor than inductors (large R_{Mp})[21], and Figure 2.9a is shown to be a more suitable choice for matching. At the millimeter wave bands, the quality factor of inductors become comparable (or even higher) than capacitors[22], making Figure 2.9b a more suitable choice in some configurations[23].

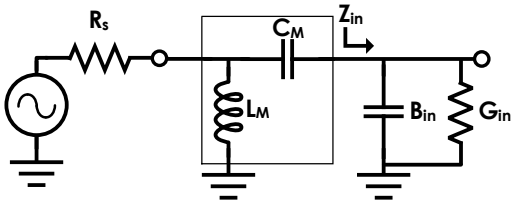
Transistor Sizing for Input and Noise Matching

The series input impedance and quality factor of the cascode amplifier is plotted against the current density for a *fixed drain current* and varying width in Figure 2.10.

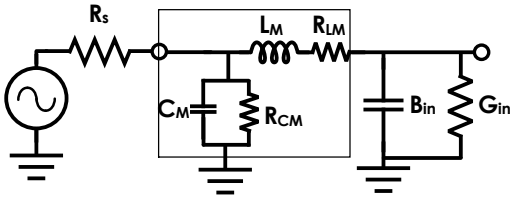
The plot shows that the quality factor decreases with decreasing drain current, but below $100\,uA$, there is a sharp increase in the noise figure. The transistor's f_T also decreases sharply around this region. One advantage of a low Q input impedance is that it leads to a wider bandwidth. However, it will be shown that the Q of the input also has an effect on the circuit's noise performance. Gonzalez[24] had shown that for impedance matching, the quality factor of the driven impedance looking into the load, must be equal to the quality factor looking towards the source terminal. Consider the matching network in Figure 2.11, ignoring the C_m term, for $Q_s = Q_{in}$, the required inductance is, $L_m \approx \frac{RsQ_{in}}{\omega}$. Thus, the



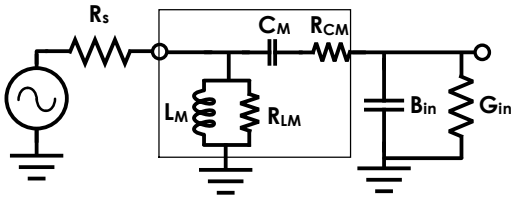
(a) C parallel, L series



(b) L parallel, C series

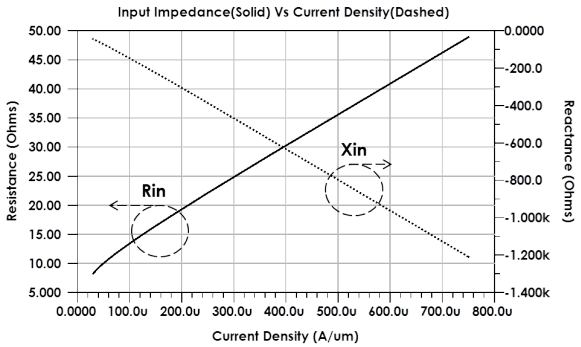


(c) C parallel, L series

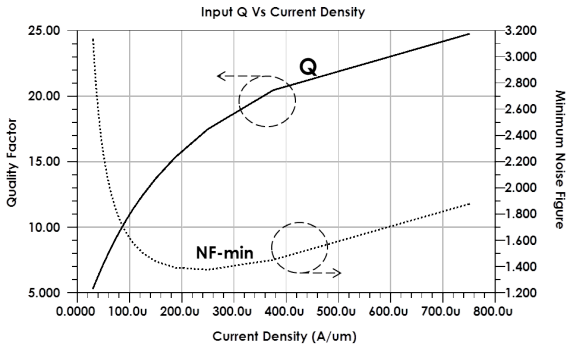


(d) L parallel, C series

Figure 2.9: Impedance tranformation networks for $Re(Z_{in}) < R_S$



(a) Input resistance and reactance



(b) Input Quality Factor and NF-min

Figure 2.10: Transistor parameters vs current density (constant current, varying width)

inductance is proportional to the input quality factor.

On chip passive components are very lossy (low Q). At $20\,GHz$, the inductors have a

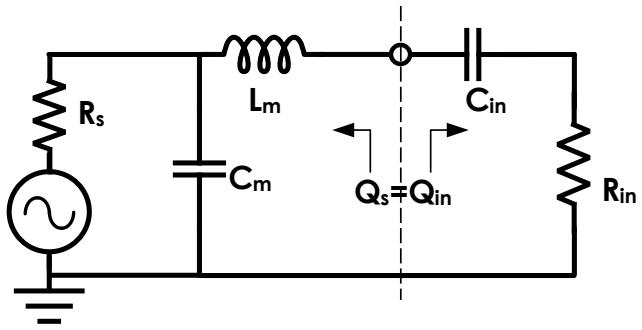


Figure 2.11: The unloaded-Q of a conjugately matched network

quality factor ranging from 8-20, depending on the size of the inductor. A high-Q matching network requires a large series inductor at the gate, L_G, which will contribute noise from it's winding resistance. One way to lower the quality factor of the common-source stage while minimizing the noise degradation is to apply a source inductor, L_S. The approximate input impedance (ignoring C_{gs}) is given as[25]:

$$Z_{in} \approx \omega_T L_S - j\Big(\frac{1}{\omega C_{gs}} - \omega L_S\Big) \tag{2.19}$$

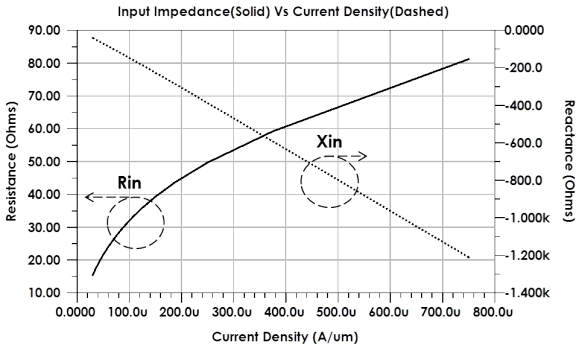
where the input is predominantly capacitive ($\frac{1}{\omega C_{gs}} >> \omega L_S$). The input quality factor is:

$$Q_{in} = \frac{\frac{1}{\omega C_{gs}} - \omega L_S}{\omega_T L_S} \tag{2.20}$$

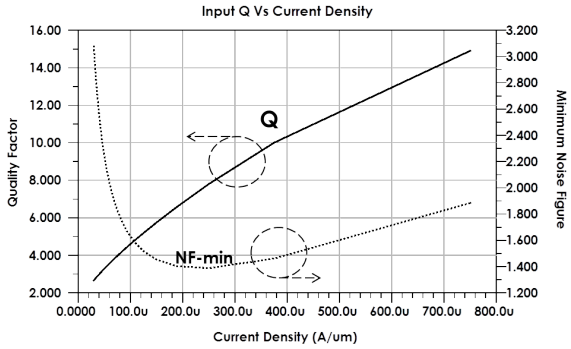
which decreases as L_S and C_{gs} increases. However, the effective transconductance of the cascode:

$$g'_{m,casc} \approx \frac{g_{m,casc}}{1 + j\omega L s g_{m,casc}} \tag{2.21}$$

decreases as L_S increases, increasing the input referred noise. The source inductance should be chosen carefully along with the transistor size to minimize the quality factor with little gain degradation. Figure 2.12 is a plot of the input quality factor at $20GHz$, when a $80\,pH$ source inductor is added, cutting the Q by half.



(a) Input resistance and reactance



(b) Input quality factor and NF-min

Figure 2.12: Transistor parameters vs current density (constant current, varying width) with inductive degeneration [$L_S = 80\,pH$]

2.3 20GHz Low Noise Amplifier Design in 65nm CMOS

2.3.1 Overview of the Architecture

In this section, a low noise amplifier design is presented to meet the active antenna G/T requirements. In the system noise study, it was stated that for a $2.1\,dB$ feed-loss, an LNA with $3\,dB$ Noise Figure requires a gain $> 27\,dB$ to desensitize the effect of tapering. From the $f_T/f_{max}/NF_{min}$ plots in Figure 2.13, a $160GHz$ f_{max} is achievable. At $20\,GHz$, the Maximum Available Gain in dB is given as:

$$\begin{aligned} G_{max} &\approx 20log\Big(\frac{f_{max}}{f}\Big) \\ &= 18\,dB \end{aligned} \tag{2.22}$$

This leaves a lot of room for a 2-stage design. The first stage is biased for low noise and wide bandwidth, while the second stage is biased for high gain and linearity. The overall noise figure for the two stages is given from Friis' Formula:

$$F_{LNA} = F_{stg1} + \frac{F_{stg2} - 1}{G_{stg1}} \tag{2.23}$$

Depending on the noise figure obtained in the first stage, the noise requirements of the second stage can be relaxed by the gain of the first stage. The block diagram illustration of the two-stage LNA is shown in Figure 2.14. The transistors in the first stage will be sized for low-Q input matching, lowering the loss (and added noise) of the input matching network.

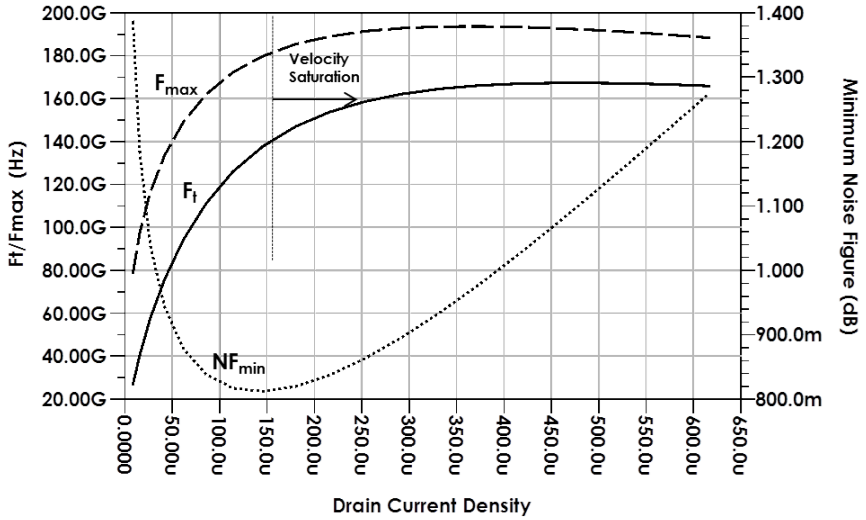


Figure 2.13: f_T, f_{max} and NF_{min} at 20GHz for TSMC 65 nm CMOS technology

The interstage matching network provides conjugate matching between the output of the first stage and input of the second stage. The output matching interfaces with a 50Ω output load.
The design is required to meet a $-30\,dBm$ input compression point. Stage 2 will be biased at higher current density (for higher gain) and higher drain current (increased linearity).

2.3.2 Schematic Level Design

A simplified schematic of the LNA is shown in Figure 2.15 utilizing the cascode topology for both stages. Allocating $2.8\,mA$ as the drain current for the first stage, the common-source transistor is sized at $70\,\mu m$ and degenerated with a $50\,pH$ source. This results in a $40\,uA/\mu m$ current density and an input quality factor of ≈ 3. The very low input quality factor reduces inductance required for matching. The common-gate transistor size is determined by plotting the width against the minimum noise figure (Figure 2.16), from which $60\,\mu m$ is chosen after compensating for parasitic effects.
The second stage transistor is biased with $3\,mA$ drain current, a little higher than the first stage to meet linearity requirements. The width is chosen for a $60uA/\mu m$ current density with a $G_{max} > 16\,dB$ at $20\,GHz$. The interstage-matching network is designed to provide conjugate impedance between the two stages stage, where the $0.6\,nH$ inductor increases the matching bandwidth.

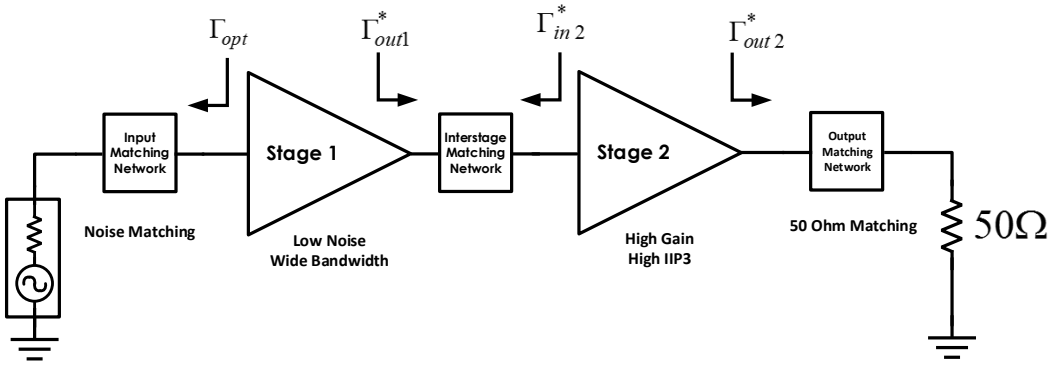


Figure 2.14: Two-stage LNA block diagram

2.3.3 Stability Considerations

Two Port Stability Analysis

Rigorous stability analysis would involve studying all the feedback loops and determining the negative resistance nodes for *all load and source impedances*. However it is sufficient to ensure that each stage of the amplifier is unconditionally stable under all operating conditions. In microwave analysis, the Rollet Stability Factor, K, is used[24]:

$$\begin{aligned} K &= \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \\ \Delta &= S_{11}S_{22} - S_{12}S_{21} \end{aligned} \tag{2.24}$$

A necessary and sufficient condition for unconditionally stable devices is:

$$\begin{aligned} K &\geq 1 \\ \Delta &< 1 \end{aligned} \tag{2.25}$$

The shortcoming of this analysis is that it assumes that all feedback loops are at the input and output terminals. As such, the effect of internal feedback loops in the circuits are not accounted for. This analysis is best suited to single-stage analysis. For multi-stage designs, each stage can be analysed for unconditional stability separately, ensuring that the loading between stages does not cause instability. Stability analysis for the common-source amplifier(see Appendix B) shows that high-Q loads and large transconductance, coupled

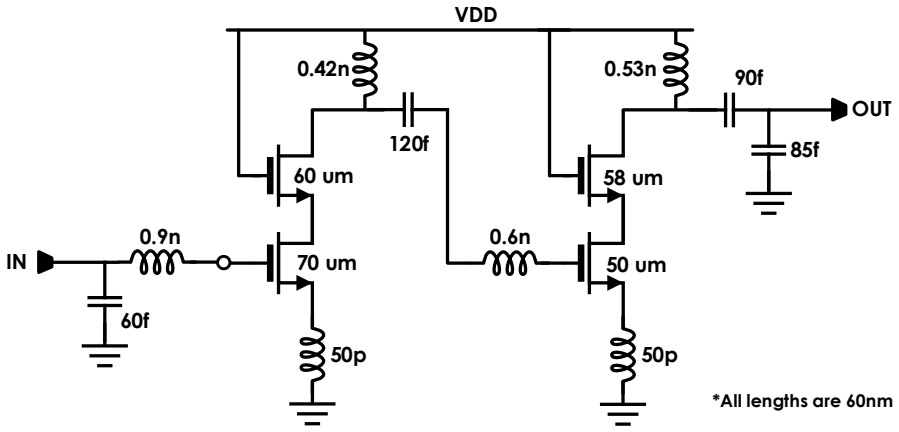


Figure 2.15: Simple two-stage LNA schematic

with feedback leads to potential instability. Although detrimental, parasitic resistances in the passive network (especially at the gate and drain) help de-Q the load and improve the stability factor. Stability analysis is performed over process, voltage and temperature variation throughout the design process.

Common-Gate Transistor Stability

The common-gate transistor has two potential sources of instability. If the gate terminal sees a parasitic inductance the wiring and the supply network Figure 2.17a), L_{Gp}, considering only the gate-source capacitance, the admittance looking into the source terminal is given as:

$$Y_{in} = \frac{g_m}{1 - \omega C_{gs} L_{Gp}} + j \frac{\omega C_{gs}}{1 - \omega C_{gs} L_{Gp}} \tag{2.26}$$

The denominator term creates negative conductance at high frequencies. Also, looking into the gate terminal, the source terminal is terminated by parasitic capacitances (from the common-source drain) and the drain-to-source resistance, ro(Figure 2.17b). Taking the case of $ro \to \infty$, the impedance looking into the gate terminal is:

$$Z_{in} = \frac{-g_m}{\omega^2 C_{Sp} C_{gs}} - j\Big(\frac{1}{\omega C_{gs}} + \frac{1}{\omega C_{Sp}}\Big) \tag{2.27}$$

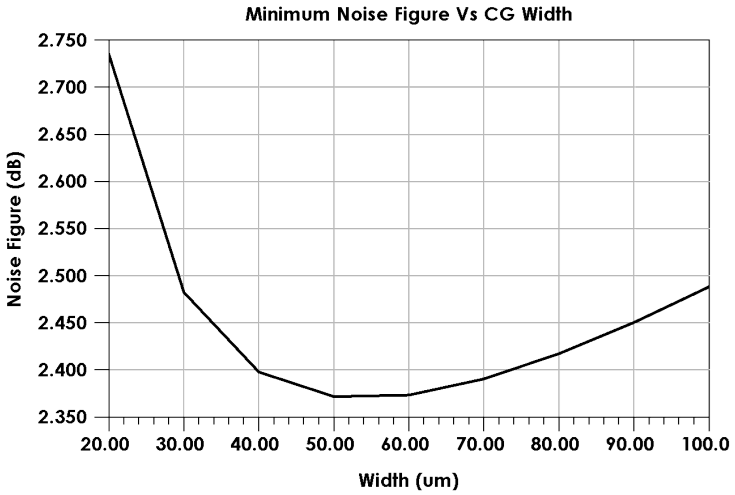
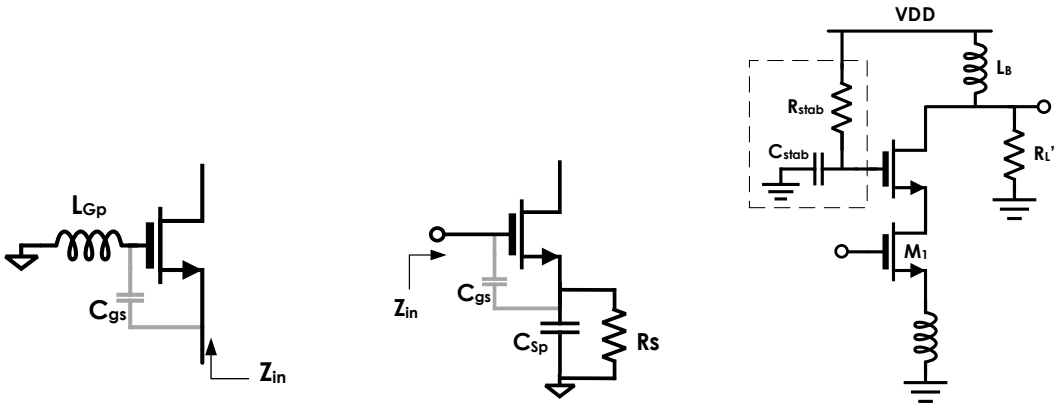


Figure 2.16: Noise figure at 20GHz with varying common gate transistor width

Which shows a negative resistance at all frequencies. Generally, ro is small enough to damp the negative resistance, but there can be cases where this node sees a high impedance(for example during turn-on), in which case noise from the supply could push the circuit into oscillation. The schematic in Figure 2.17c is a modification to correct both sources of instability. R_{stab} is a large resistor that negates the negative conductance due to parasitic inductance along the gate terminal. It also dampens any noise from the supply. C_{stab} is used to provide an AC-ground as well as supply filtering.

2.3.4 Inductors and Interconnects

All passives are implemented on-chip. Large inductors are implemented with metal (spirals). The process development kit contains inductor models measured and validated up to $40\,GHz$. The back-end features 9 metal layers with a thick $3.4\,\mu m$ top metal layer for interconnects. The inductor's width, turn and spacing are chosen to maximize the quality factor. The $50\,pH$ source inductance is implemented with a high-Q microstrip line. Microstrip lines with very small electrical lengths ($\beta l << \frac{\lambda_g}{4}$), can be approximated as a *quasi-lumped element*[26]. Consider the equivalent short circuit representation in Figure



(a) (b) (c)

Figure 2.17: Unstable common-gate Ccnfiguration (a) and (b). Nullifying the inductance and feedthrough (c).

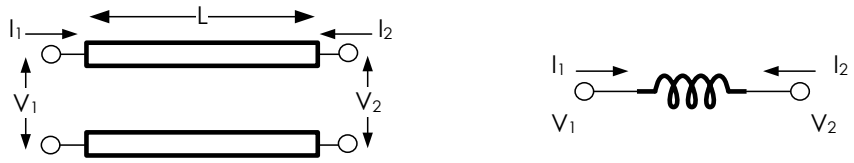
2.18b. From transmission line theory:

$$Y_{11} = \frac{1}{Z_{in}}\bigg|_{S.C.port2} = \frac{1}{jZ_0 tan(\beta l)} \approx \frac{1}{jZ_0\beta l} \tag{2.28}$$

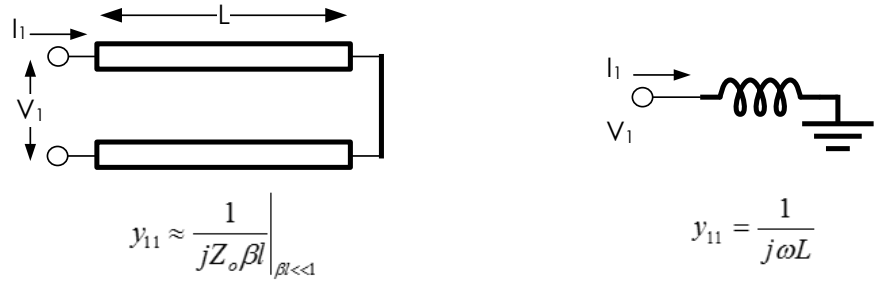
The equivalent inductance per unit length is given as:

$$L'_{eq} = \frac{Z_0}{v_p} \tag{2.29}$$

The quasi-lumped microstrip inductance is ideally constant with frequency. In reality, $Z_0 \approx \sqrt{\frac{R}{j2\pi fC}}$, and decreases with frequency until it approaches the corner frequency where $Z_0 = \sqrt{\frac{R+j2\pi fL}{G+j2\pi fC}}$. The microstrip line inductor is illustrated in Figure 2.19. The top metal (Metal 9) in the process is used as the signal, while the bottom metal (Metal 1) is used as the ground plane which is patterned to suppress *eddy currents*[27]. Microstrip lines of different widths and length were simulated and extracted. A $2\mu m$ line has an inductance per unit length of $0.5\,pH/\mu m$. A $95\mu m$ stripline was implemented as the source inductor for both stages with a Q of 4.5.

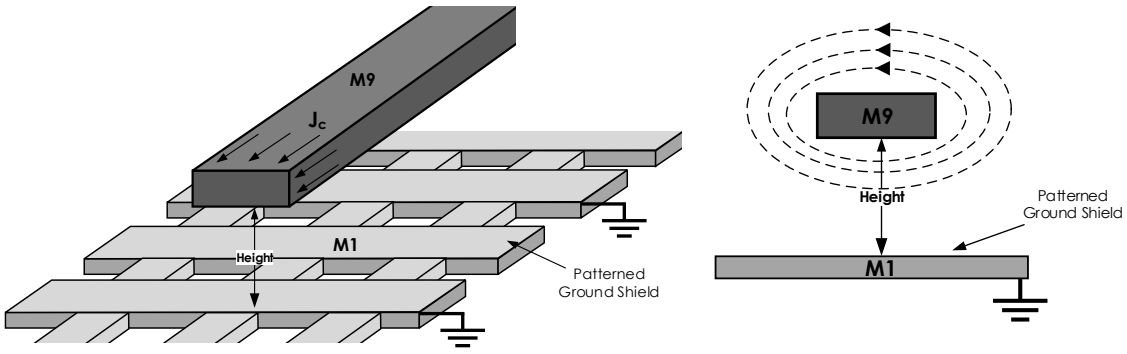


(a) Transmission Line Element



(b) Shorted Transmission Line for y_{11} calculations

Figure 2.18: Equivalent quasi-lumped inductor element



(a) (b)

Figure 2.19: Stripline inductor element

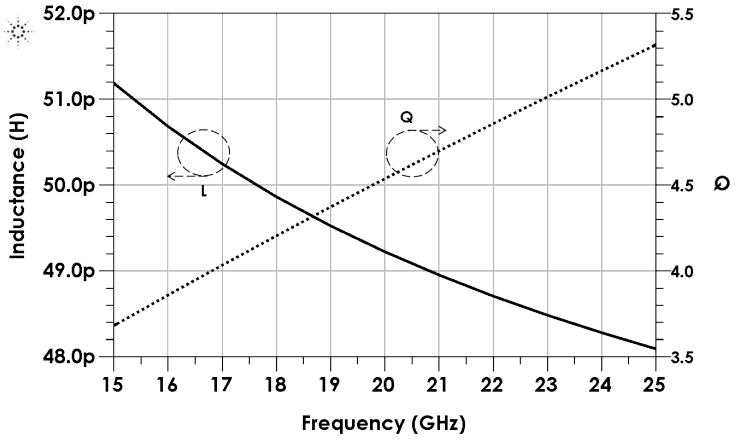


Figure 2.20: Inductance and quality factor of the microstrip line.

2.3.5 Simulation and Measurements

The complete $20\,GHz$ LNA schematic is shown in Figure 2.21. The bias circuit uses a $100\mu A$ reference current to set the gate voltage. Thin ($0.4\,\mu m$) p-type poly-silicon resistors are used to feed the gate bias voltage. Input and output matching capacitors are absorbed along with the pad capacitor. All RF pads and interconnects were EM-simulated in the ADS® Momentum simulator with grounding and shielding. The active die area occupies $600 \times 400\,\mu m^2$ without pads and $700 \times 550\,\mu m^2$ including pads.
The fabricated circuit was measured with on-wafer probing (illustrated in Figure 2.22). Figure 2.23a-2.23b are the measured and simulated S-parameters from $15\,GHz$ to $25\,GHz$. The LNA has $> 27\,dB$ gain from $19 - 21\,GHz$. The input return loss suffered a $1\,GHz$ frequency shift due to diodes added at the last minute to meet antenna rules. The Noise Figure has not been measured, but the simulated noise figure is plotted in Figure 2.23e achieving $2.6\,dB$ at $20\,GHz$. The measured input-referred 1dB compression point is $-28\,dBm$.

Table 2.1: Design and performance summary of the $20\,GHz$ LNA

Parameters		**Results**
Design Summary	Technology	65nm CMOS
	Stages	2
	Die Area	$700 \times 550\,\mu m^2$ (with pads)
Power	Voltage	$1.2\,V$
	Current	$5.8\,mA$ ($2.8\,mA$ Stage 1, $3\,mA$ stage 2)
	Power Consumption	$7\,mW$
Small-Signal	Center Frequency	$20\,GHz$
	Frequency Range	$19 - 21\,GHz$
	Gain	$29\,dB$
	Input Return Loss	$10\,dB$
	Output Return Loss	$12\,dB$
	Reverse Isolation	$> 40\,dB$
	Noise Figure	$2.6\,dB$
Large Signal	Input $P - 1dB$	$-29\,dBm$

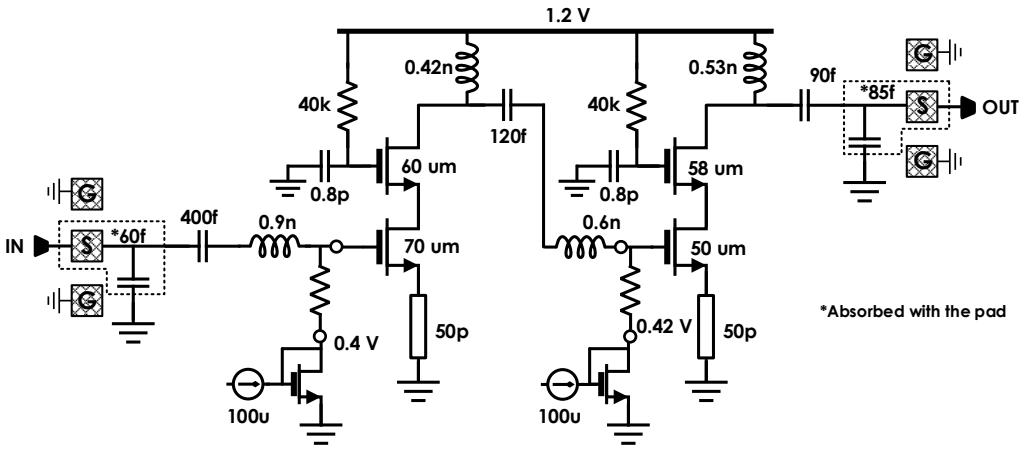
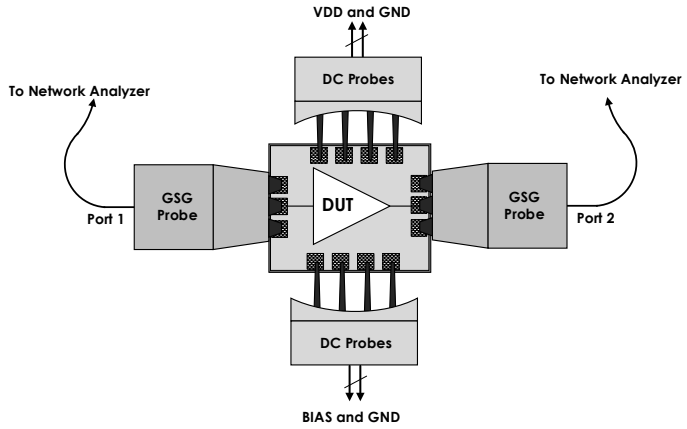
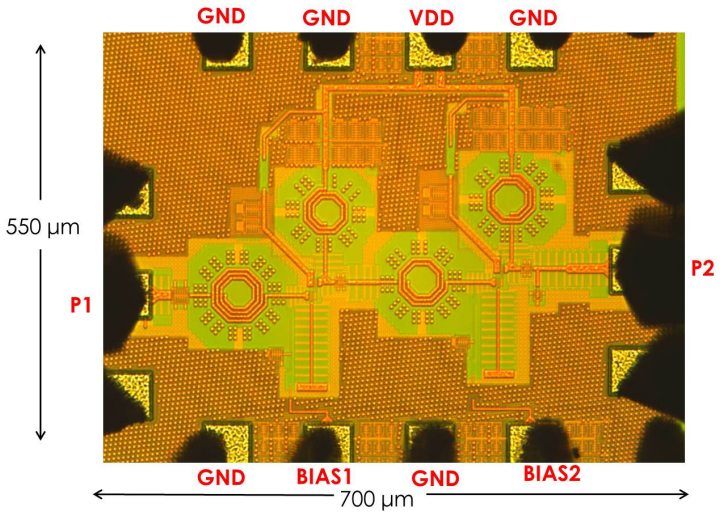


Figure 2.21: Complete $20GHz$ LNA schematic

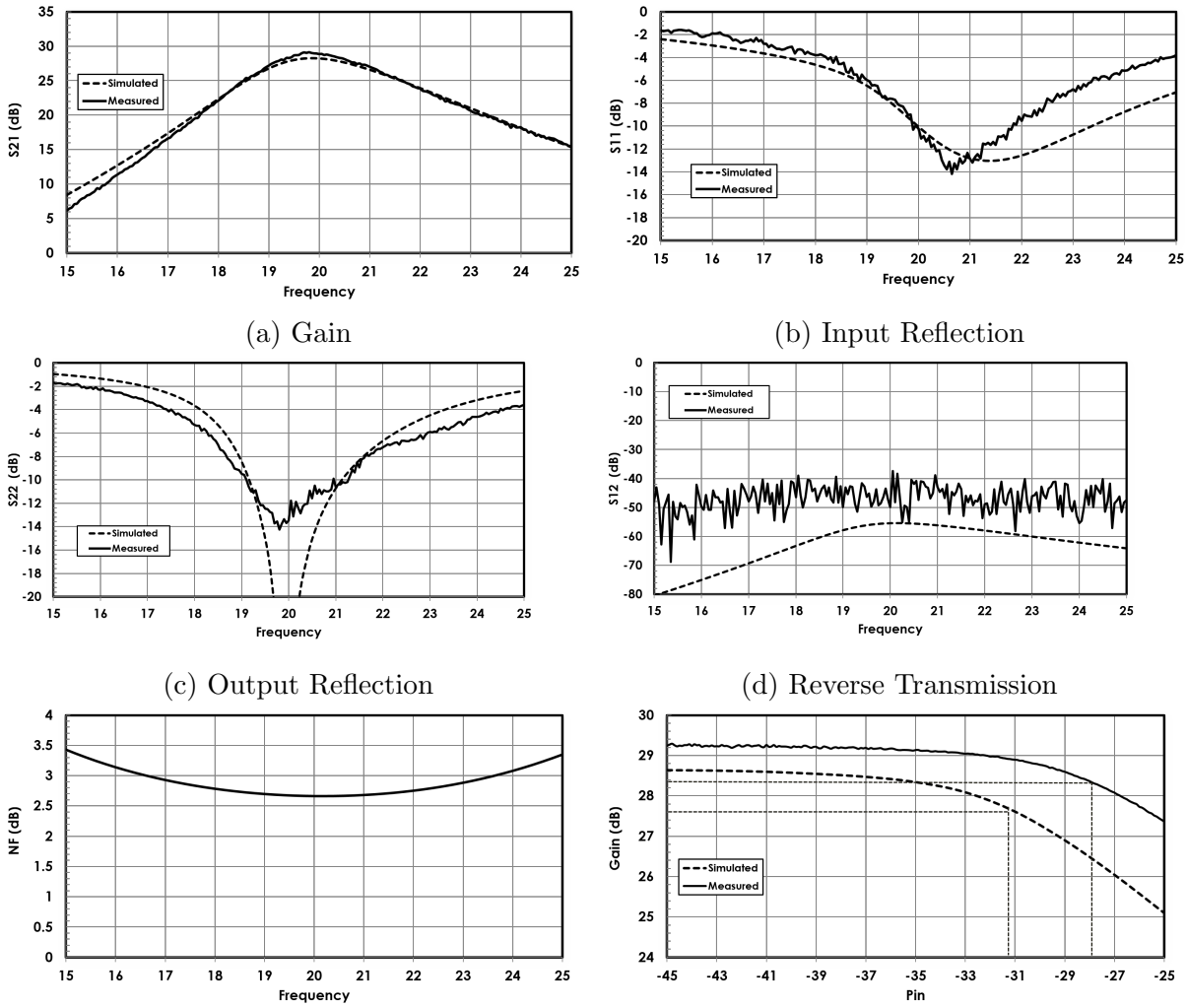


(a) Probe setup



(b) Micrograph

Figure 2.22: Measurement setup and chip micrograph



(a) Gain

(b) Input Reflection

(c) Output Reflection

(d) Reverse Transmission

(e) Noise Figure

(f) Gain Vs Input Power

Figure 2.23: Simulated and Measured results for the $20\,GHz$ Low Noise Amplifier

Chapter 3

Phase Shifters

3.1 Phase Shifter Requirements

3.1.1 Digital and Continuous Phase Shifters

By applying a progressive phase-shift, $\Delta\phi$, between array elements, it is possible to steer the main beam in a direction, θ_0, away from the antenna *bore-sight* (0°). This is known as beam-steering, and the relation is given by the equation:

$$\Delta\phi = \frac{2\pi}{\lambda} d\, sin(\theta_0) \tag{3.1}$$

where d is the distance between elements, and λ is the wavelength. The progressive phase shift is applied using a phase shifter as part of the beam-forming network. Phase shifters are implemented in one of two ways:

1. Continuous phase shifters
2. Digital phase shifters

Continuous phase shifters, such as [28, 29, 30], can be configured to provide a continuous phase shift value using an analog input control signal (like a DC voltage). They are capable of phase shift and pattern beam-steering with infinite precision. Thus, the array pattern does not suffer from the effects of phase quantization errors, which will be discussed later. Some analog phase shifters however, exhibit non-linear responses to the voltage control signal making it difficult to implement in a control loop. In addition, some implementations (like the BST based phase shifter[30]) require a large control voltage range ($> 20\,V$), which

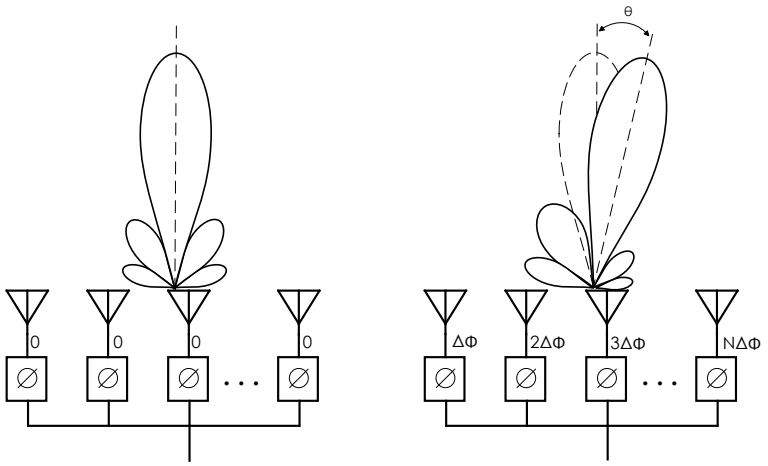


Figure 3.1: Illustration of beam-steering using elements excited by a progressive phase

is undesirable for integration and low-voltage applications.
Digital phase shifters [31, 32, 33] are capable of providing quantized phase shift values from a digital word input. An N_b-bit digital phase shifter has 2^{N_b} phase states with a progressive phase step:

$$\Delta\phi_s = \frac{2\pi}{2^{N_b}} \tag{3.2}$$

Digital phase shifters are designed for fixed phase shift values with $< \frac{1}{2}\Delta\phi_s$ uncertainty. Unlike continuous phase shifters, they are not subject to phase errors due to non-linearity between the phase shift and the control signal. They are easier to integrate with mixed-signal integrated systems, and in a lot of cases, can work in very low voltage applications. The adverse effect of digital phase shifter implementations are that they lead to quantization errors in the progressive phase. In the next section, it will be shown that this generates parasitic quantization lobes.

3.1.2 Effect of Phase Quantization

Consider an N-element linear array with a required progressive phase shift, $\Delta\phi$, between elements. This phase shift generates a main beam pointing in the $u_0 = sin(\theta_0)$ direction.

Ideally, the normalised far-field pattern is given as:

$$F(u) = \frac{1}{N} \sum_{n=-\frac{N-1}{2}}^{\frac{N-1}{2}} e^{jn(\frac{2\pi}{\lambda} d\, u_0 - \Delta\phi)}. \tag{3.3}$$

Assume digital phase shifters with phase steps $\Delta\phi_s$ are implemented at the transmitter. If the required progressive phase shift is equal to the phase step of the phase shifter(i.e., $\Delta\phi = \Delta\phi_s$), then the field pattern will be the same as (3.3). In a case where $\Delta\phi \leq \Delta\phi_s$, the actual phase shift applied to each element will be rounded off to the nearest phase state. Mailloux [34] showed that the result is an equivalent field pattern generated by m sub-arrays with M elements each, where $N = m \cdot M$. These unwanted *sub-arrays* are groups of elements that have a phase progression equal to the quantized phase shift, $\Delta\phi_s$ and are spaced, $(M \times d)$ apart. Since $(M \times d)$ is likely to be several wavelengths long, the sub-arrays will generate a number of *quantization lobes* in a direction, θ_q, set by:

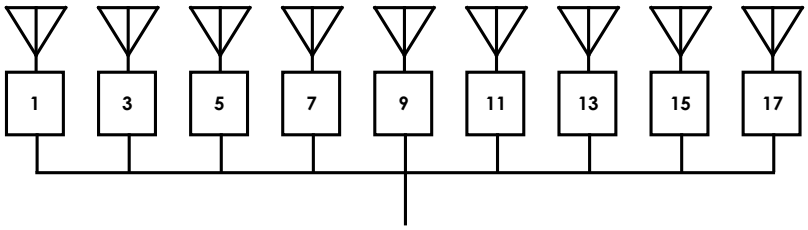
$$\theta_q = sin^{-1}\left(\frac{\Delta\phi_s}{kMd}\right). \tag{3.4}$$

The quantization lobe level is the difference between the gain at the peak of the quantization lobe and the main beam. The overall antenna pattern can be represented as by the product of the gain pattern due to the M elements in the sub-array(F_{sa}), and the array factor of the m sub-arrays(AF_{sa}) which create these quantization lobes.

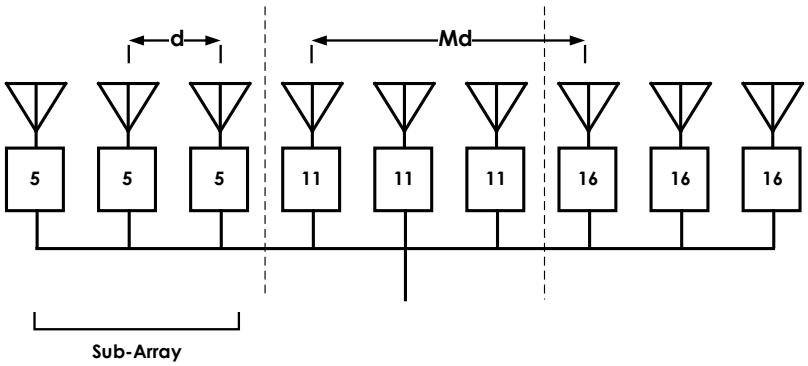
$$\begin{aligned} F(u) &= AF_{sa}(Z)F_{sa}(z) \\ F(u) &= \left\{\frac{1}{m} \sum_{p=-\frac{m-1}{2}}^{\frac{m-1}{2}} e^{jp(\frac{2\pi}{\lambda} Md\, u_0 - \Delta\phi)}\right\}\left\{\frac{1}{M} \sum_{q=-\frac{M-1}{2}}^{\frac{M-1}{2}} e^{jp(\frac{2\pi}{\lambda} d\, u_0 - \Delta\phi_s)}\right\} \end{aligned} \tag{3.5}$$

To illustrate this, consider a 3-bit phase shifter which can provide progressive phase shifts with 45° phase steps. Assuming that this phased shifter is used in an application that requires a progressive phase of 15°, as shown in Figure 3.2b, sub-arrays of size $M = 3$ will be formed due to quantization. The effect on the intensity pattern for a linear array consisting of $N = 30$ elements is shown in Figure 3.2c. The main quantization lobes generated from the second term of (3.5) are at $U = -0.5, 0.85$. Such a system, if used as a transmitter, will violate side-lobe level requirements, and if used as a receiver, will introduce noise and interference into the channel.

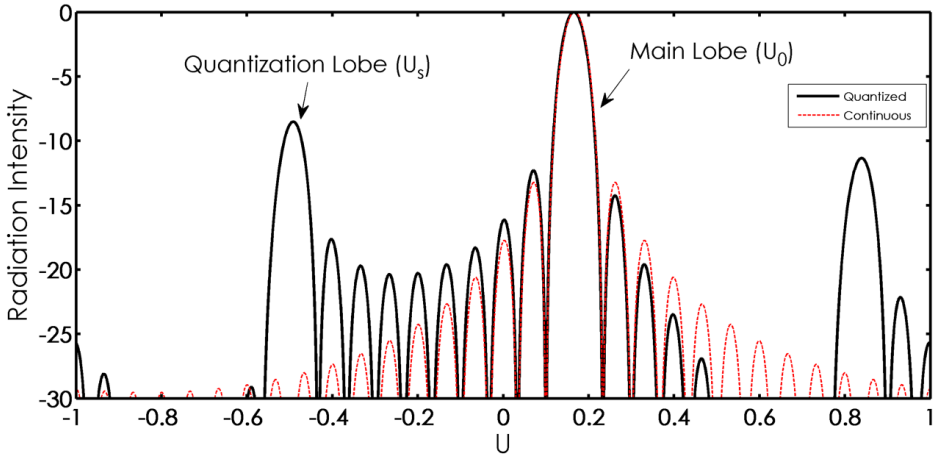
It turns out that this example presents a worst-case quantization lobe level, since the sub-arrays generated from the quantization error are correlated. This occurs when the desired phase shift is an integer multiple of the phase shifter's phase step.



(a) continuous phase progression



(b) 3-bit quantized phase progression



(c) beam intensity pattern in the u-space

Figure 3.2: Effect of phase quantization on the intensity pattern

So for the worst case, the sub-arrays are formed from $M = \frac{\Delta\Phi_s}{\Delta\Phi_0}$ uniform elements spaced d apart, and the sub-arrays are spaced Md apart. Work done initially by Miller[35] and then followed by Mailloux[34] used this assumption to derive the quantization lobe level:

$$QL(dB) = -20log\left[\frac{1}{Msin((p+\frac{1}{2^{N_b}})\frac{\pi}{M})}\right] + 9.94 - 6.02N_b \tag{3.6}$$

where N_b is the number of bits of the digital phase shifter and $p = \pm1, \pm2, ...$ is the index of the quantization lobes in the visible region of the radiation pattern. The lobe will point in the direction corresponding the $\Delta\phi_s$ phase in u space:

$$u_{QL} = sin(\theta_{QL}) = \frac{\lambda}{2\pi d}\Delta\phi_s \tag{3.7}$$

Figure 3.3 shows that the quantization lobes can be as high as $-4\,dB$ for small values of M. Thus, for satellite communication systems, it is important to have beamforming algorithms which can maximize the number of sub-array elements by applying uncorrelated phase shift values to the elements. For large values of M, the *upperbound* for the quantization lobe level is estimated as:

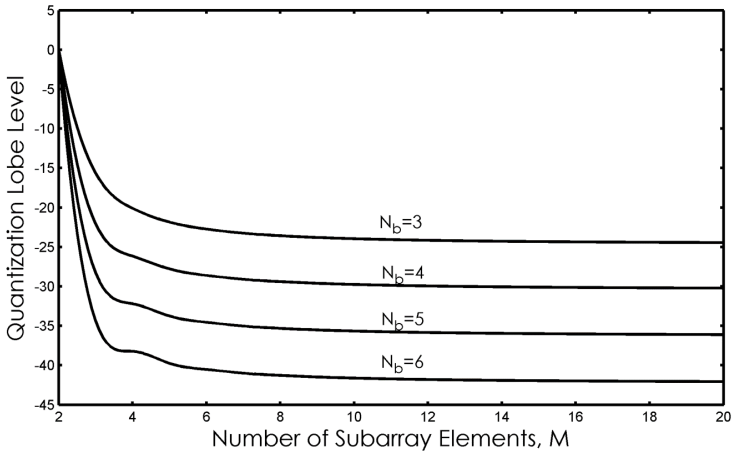


Figure 3.3: Quantization lobe level

$$QL(dB) < -20logM + 9.94 - 6.02N_b \tag{3.8}$$

Using Figure 3.3, the number of bits for the phase shifter can be chosen based on transceiver requirements. To meet $> 30\,dB$ side-lobe level (SLL), a 5-bit phase shifter is required.

3.2 Vector-Sum Active Phase Shifter

3.2.1 Theory of Operation

Vector-sum phase shifters are a popular implementation of digital phase shifters in integrated circuits[36, 37, 38]. The vector-sum phase shifter creates phase variation by combining an in-phase and quadrature-phase version with varying weights. Figure 3.4 is a block diagram illustration. Given an input signal, V_i, the quadrature generator will generate an in-phase (V_{iI}) and quadrature-phase (V_{iQ}) version of the original signal, where:

$$\begin{aligned} V_{iI} &= \frac{1}{\sqrt{2}} V_i \; e^{j\theta_0} \\ V_{iQ} &= \frac{1}{\sqrt{2}} V_i \; e^{j(\theta_0 + 90^\circ)} \end{aligned} \tag{3.9}$$

It should be noted that it is only required that V_{iQ} be 90° out of phase with V_{iI}, and thus, the phase with respect to the input (θ_0) can be arbitrary.

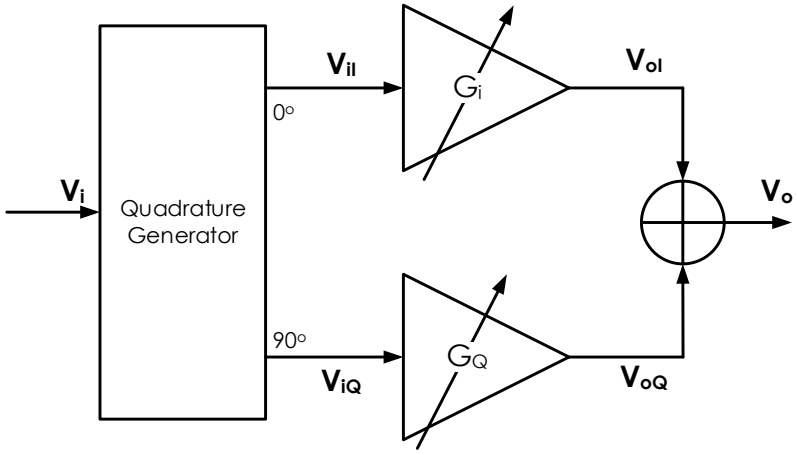


Figure 3.4: Vector-sum phase shifter block diagram

Each signal is amplified by variable gain amplifiers, G_I and G_Q, to produce V_{oI} and

V_{oQ} respectively. The two signals are summed to produce a final output signal, V_o:

$$\begin{aligned} V_o &= V_{oI} + V_{oQ} \\ V_o &= G_I V_{iI} + G_Q V_{iQ} \\ V_o &= \left(\frac{1}{\sqrt{2}} G_I \; e^{j\theta_0} + \frac{1}{\sqrt{2}} G_Q \; e^{j(\theta_0 + 90^\circ)} \right) V_i \end{aligned} \tag{3.10}$$

(3.10) can be written in matrix form as:

$$V_o = \begin{bmatrix} \frac{1}{\sqrt{2}} G_I \; e^{j\theta_0} \\ \frac{1}{\sqrt{2}} G_Q \; e^{j(\theta_0 + 90^\circ)} \end{bmatrix} Vi \tag{3.11}$$

The magnitude of the output is the vector sum of the in-phase and quadrature-phase components,

$$\begin{aligned} |V_o| &= \sqrt{\left(\frac{1}{\sqrt{2}} G_I \; e^{j\theta_0} \right)^2 + \left(\frac{1}{\sqrt{2}} G_Q \; e^{j\theta_0} \right)^2} \, |V_i| \\ |V_o| &= \frac{1}{\sqrt{2}} \left[\sqrt{G_I^2 + G_Q^2} \right] |V_i| \end{aligned} \tag{3.12}$$

Similarly, the phase is:

$$\begin{aligned} \angle V_o &= tan^{-1} \left(\frac{\frac{1}{\sqrt{2}} G_Q}{\frac{1}{\sqrt{2}} G_I} \right) + \theta_0 + \angle V_i \\ &= tan^{-1} \left(\frac{G_Q}{G_I} \right) + \theta_0 + \angle V_i \end{aligned} \tag{3.13}$$

From (3.13), the relative phase of the output can be controlled by varying the gains, G_I and G_Q:

$$\phi = tan^{-1} \left(\frac{G_Q}{G_I} \right) \tag{3.14}$$

However, (3.12) shows that there is a relative gain dependency with G_I and G_Q. For a constant gain, the choice of G_I and G_Q must be restricted such that the vector-sum traverses a *unit circle*.

From the unit circle properties, to produce a given output phase, ϕ, the required gains are:

$$\begin{aligned} G_I &= G_o cos(\phi) \\ G_Q &= G_o sin(\phi) \end{aligned} \tag{3.15}$$

where G_o is an arbitrary constant gain factor.

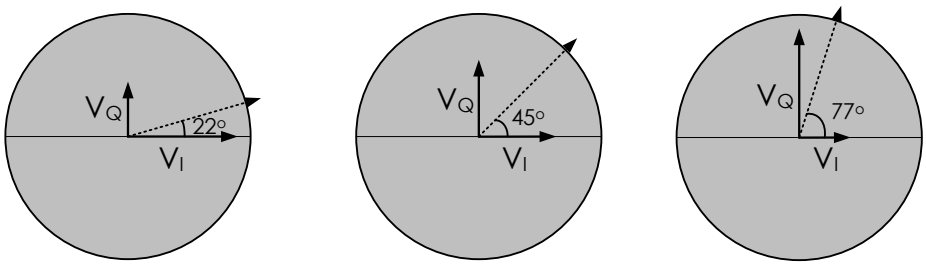


Figure 3.5: Unit circle illustation of the vector-sum magnitude/phase control

3.2.2 Error in the Quadrature Generator

The quadrature generator is required to generate equal magnitude terms, V_{iI} and V_{iQ} which are 90° out of phase. Consider a quadrature generator with magnitude error, ΔG_q and phase error, $\Delta\phi_q$. Using V_{iI} as a reference, from (3.9), the output of the quadrature generator is:

$$\begin{aligned} V_{iI} &= \frac{1}{\sqrt{2}} V_i \; e^{j\theta_0} \\ V_{iQ} &= \frac{1}{\sqrt{2}} \Delta G_q V_i \; e^{j(\theta_0 + 90^\circ + \Delta\phi_q)} \end{aligned} \tag{3.16}$$

Substituting (3.16) into (3.10), the output of the phase shifter is:

$$V_o = \left(\frac{1}{\sqrt{2}} G_I \; e^{j\theta_0} + \frac{1}{\sqrt{2}} G_Q \Delta G_q \; e^{j(\theta_0 + 90^\circ + \Delta\phi_q)} \right) V_i \tag{3.17}$$

The Gain Error is found by dividing the magnitude of (3.17) with (3.12):

$$\Delta G_o = \sqrt{\frac{|G_I^2 + G_Q^2 \Delta G_q^2 e^{2\Delta\phi_q}|}{G_I^2 + G_Q^2}} \tag{3.18}$$

Assuming that G_I and G_Q are chosen to provide constant gain (the *unit circle condition* in (3.15)), then the overall gain error is:

$$\Delta G_o = \sqrt{|cos^2(\phi) + sin^2(\phi) \Delta G_q^2 e^{2\Delta\phi_q}|} \tag{3.19}$$

which varies depending on the desired phase angle. The Phase Error is found by first expanding the exponential term in (3.17) as:

$$V_o = \left(G_I - G_Q \Delta G_q sin(\Delta\phi_q) + jG_Q \Delta G_q cos(\Delta\phi_q) \right) \frac{1}{\sqrt{2}} V_i \, e^{j\theta_0} \tag{3.20}$$

which is written as:

$$\Delta\phi_o = tan^{-1} \left(\frac{G_Q \Delta G_q cos(\Delta\phi_q)}{G_I - G_Q \Delta G_q sin(\Delta\phi_q)} \right) - \phi \tag{3.21}$$

Applying the unit circle condition (3.15):

$$\Delta\phi_o = tan^{-1} \left(\frac{sin(\phi) \Delta G_q cos(\Delta\phi_q)}{cos(\phi) - sin(\phi) \Delta G_q sin(\Delta\phi_q)} \right) - \phi \tag{3.22}$$

where ϕ is the desired phase. In implementation, the quadrature generator will have a limited bandwidth over which it can provide a tolerable gain and phase error. For $< \frac{1}{2} LSB$ error in phase, the overall phase error of the phase shifter should be $< 11^\circ$ phase error in the case of a 4-bit phase shifter and $< 5^\circ$ phase error in the case of a 5-bit phase shifter over the entire bandwidth of interest. Figure 3.6 shows contours of the maximum phase error in (3.22), as a function of the quadrature generator phase and gain error. For example, in a 5-bit phase shifter, 1 dB of gain error can be tolerated if the phase error remains $\leq 2^\circ$.

3.2.3 Generating 360° Phase Shift

The simplified architecture used thus far is only capable of 90° phase shift. To traverse the whole unit circle, a simple modification is made by adding two more amplifiers in opposite phase (Figure 3.7a). The added amplifiers are implemented as two additional sign bits to select the quadrant in the unit circle. The gain and phase error analysis for the quadrature generator remains the same in this configuration.
To minimize gain/phase errors between quadrants, it is desirable to implement all amplifiers using the same architecture. Different configurations have been employed in past work to implement the negative gain amplifiers, two of which were compared in [39]. In the fully differential implementation(Figure 3.7b), the same amplifier is used, but the polarity of the inputs are reversed.

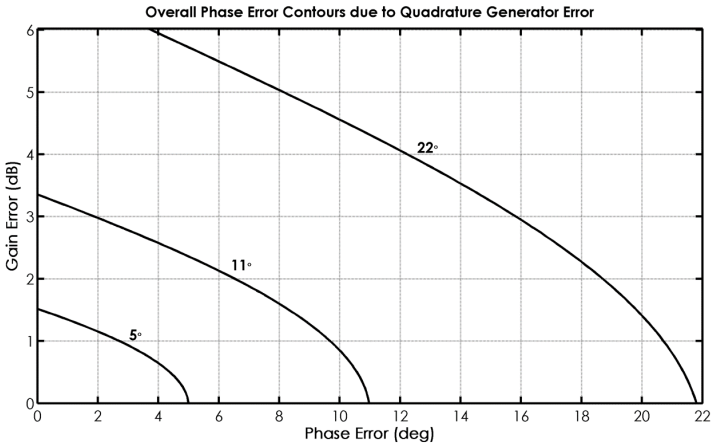


Figure 3.6: Maximum phase error contours as a function of the quadrature generator gain error and phase error

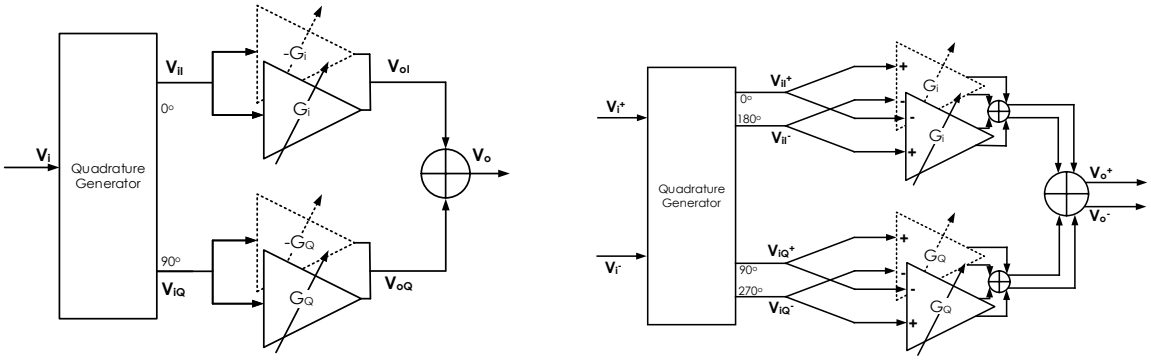
3.3 20GHz 5-bit Vector-Sum Active Phase Shifter in CMOS

In this section, a 20GHz 5-bit vector-sum phase shifter is designed in 65nm CMOS, using the fully differential architecture described in Figure 3.7b. The phase shifter is required to function with a 10% operating bandwidth. As with other components of the phased array, power consumption is a crucial design factor. The 5-bit of phase shift is required to meet $< 30dB$ side lobe level (from (3.8)). Since the LNA has been designed to compensate over $15\,dB$ of loss from the beam-forming network, power gain is not required, permitting very low power design.

3.3.1 Quadrature Generator

RC Polyphase Filters

The quadrature generator is required to generate two pairs of differential quadrature outputs from a differential input. Two general implementations of the quadrature generators are RC-polyphase filters (PPF) and RLC-quadrature all-pass (QAF) Filters. The polyphase filter has found extensive use in image reject receiver architectures[40].
The polyphase filter is built from RC-CR networks which outputs two voltages with phases



(a) Negative gain amplifiers

(b) Fully differential

Figure 3.7: 360° Vector-Sum Phase Shifter Implementation

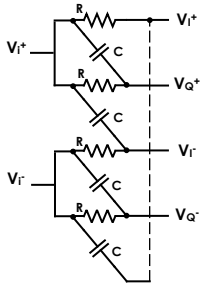
45° and −45° apart at a center frequency [**?**]:

$$\omega_c = \frac{1}{RC} \tag{3.23}$$

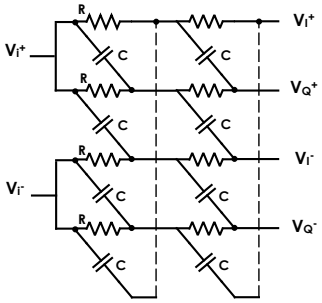
The schematic of the first-order polyphase filter is shown in (Figure 3.8a). This was designed and simulated for $f_c = 20\,GHz$. The quadrature phase error is plotted against the operating frequency in Figure 3.8c which shows a very narrow operating bandwidth. There is 3° of phase error at $1\,GHz$ offset, which, according to Figure 3.6, leaves very little room for tolerance (in both phase and gain error). To increase the bandwidth, higher-order polyphase filters can be implemented by cascading the first order networks. The second order polyphase filter (Figure 3.8b) is simulated for $20\,GHz$. The phase error plot in Figure 3.8d displays a larger operating bandwidth and less phase error.
The drawback with using higher order polyphase filter networks is the insertion loss that comes with the cascaded resistors. Figure 3.8e and 3.8f show the insertion loss for the 1^{st} and 2^{nd} order network, when terminated with 100Ω matched loads. The second order PPF adds an additional $3\,dB$ loss to the first order. Compensating this loss in the sub-VGA stage may lead to an increase in the power consumption.

Quadrature All-Pass Filters

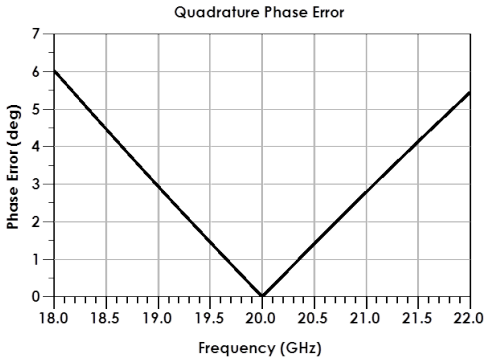
An alternative to the polyphase filter is the RLC quadrature all-pass filter (QAF)[36]. The QAF schematic is drawn in Figure 3.9a and redrawn in Figure 3.9b to show the I and



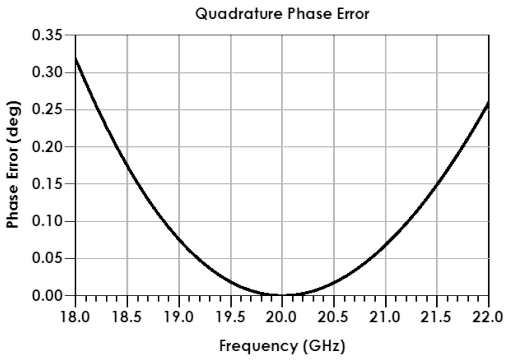
(a) First Order Polyphase Filter



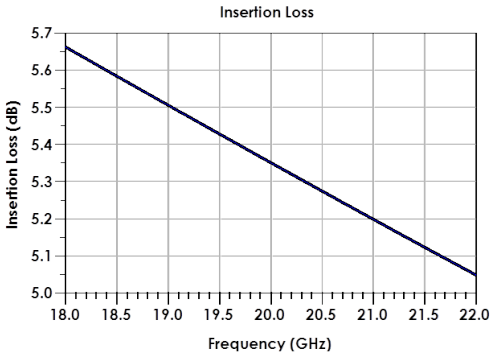
(b) Second Order Polyphase Filter



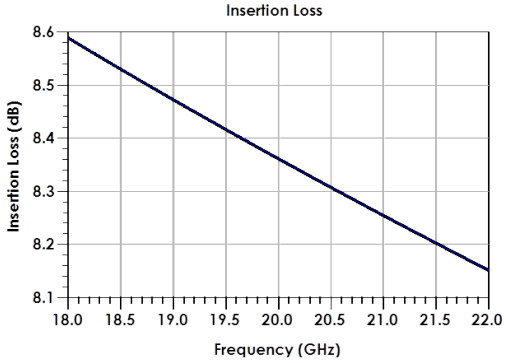
(c) First-order PPF phase error (R=71 Ω, $C = 112\,fF$)



(d) Second-order PPF phase error (R=71 Ω, $C = 112\,fF$)

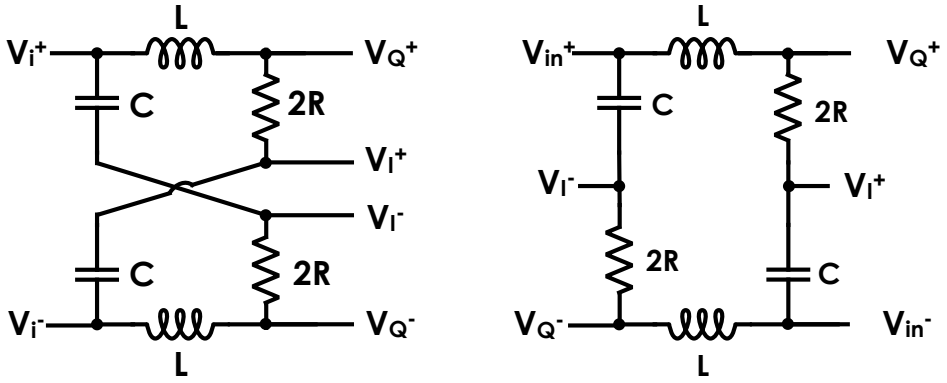


(e) First-order PPF insertion loss (R=71 Ω, $C = 112\,fF$)



(f) Second-order PPF insertion loss (R=71 Ω, $C = 112\,fF$)

Figure 3.8: Polyphase filter networks and frequency response



(a) Schematic (b) Redrawn

Figure 3.9: Quadrature All-Pass Filter

Q differential network. To analyse this filter, consider the single-ended versions shown in Figure 3.10a and 3.10b.

The open circuit voltage transfer function of the I network (Figure 3.10a) can be computed as:

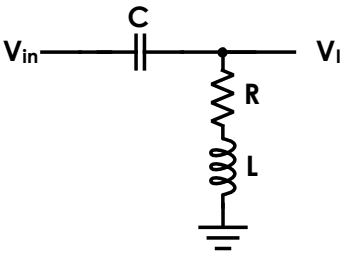
$$\frac{V_{oI}^{-}}{V_{in}} = s\left[\frac{s+\frac{R}{L}}{s+\frac{R}{2L}\left(1\pm\sqrt{1-\frac{4L}{R^2C}}\right)}\right] \tag{3.24}$$

Similarly for the Q network (Figure 3.10b):

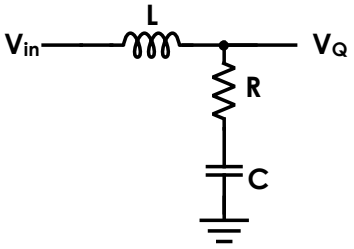
$$\frac{V_{oQ}^{+}}{V_{in}} = \frac{R}{L}\left[\frac{s+\frac{1}{CR}}{s+\frac{R}{2L}\left(1\pm\sqrt{1-\frac{4L}{R^2C}}\right)}\right] \tag{3.25}$$

To obtain the condition over which there is a quadrature phase shift between Q and I the overall transfer function between the outputs can be derived using (3.24) and (3.25):

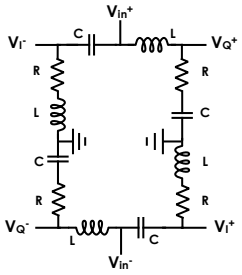
$$\begin{aligned}\frac{V_{oQ}^{+}}{V_{oI}^{-}} &= \frac{V_{oQ}}{V_{in}}\frac{V_{in}}{V_{oI}} \\ &= \frac{R}{sL}\left[\frac{s+\frac{1}{CR}}{s+\frac{R}{L}}\right]\end{aligned} \tag{3.26}$$



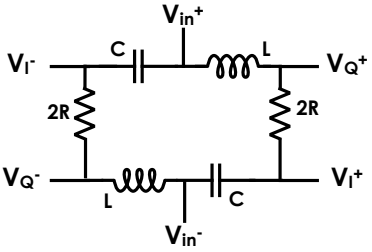
(a) Single-ended Q network



(b) Single-ended I network

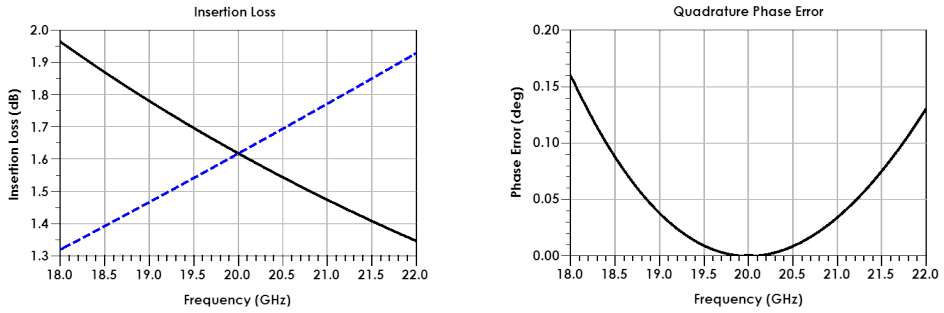


(c) Differential quadrature network



(d) Reduced quadrature network

Figure 3.10: Quadrature all-pass filter network single-ended and differential schematic



(a) Insertion loss (b) Phase error

Figure 3.11: Quadrature All-Pass Filter Frequency Response

The transfer function has one zero and two poles at the Left Half Plane and the origin. Evaluating the angle of the transfer function:

$$\theta_{Q^+,I^-} = tan^{-1}(\omega RC) - tan^{-1}\left(\omega\frac{R}{L}\right) - 90^\circ \tag{3.27}$$

If the pole and zero are placed together and generate 45° at $\omega = \omega_c$, the outputs will be in phase quadrature. The two conditions are thus:

$$\begin{aligned} R &= \sqrt{\frac{L}{C}} \\ \omega_c &= \frac{1}{\sqrt{LC}} \end{aligned} \tag{3.28}$$

Combining the single ended networks into a differential network, as shown in Figure 3.10c provides the outputs V_I^+, V_I^-, V_Q^+ and V_Q^-. However, if L and C are chosen as (3.28), then at ω_c the impedances of the inductor and capacitor are equal, i.e., $X_C = -X_L$. The L and C in Figure 3.10c are thus redundant[36] and can be removed to form the reduced schematic in Figure 3.10d.
The frequency response of a $20\,GHz$ quadrature all-pass filter is shown in Figure 3.11a-3.11b using L=$280\,pH$, C = $226\,fF$ and R = 35Ω. It has half the phase error of the second order polyphase filter at $2\,GHz$ bandwidth and more then $6\,dB$ improvement in the insertion loss. The drawback is in the quadrature gain error (between V_I and V_Q) which was not present in the polyphase filter case.

Load Capacitance Effect

The quadrature generator is connected to a set of variable gain amplifiers (sub-VGAs) which, as will be shown in the next section, are implemented using common-source differential-pair transistors. As a result, the quadrature filter sees a load capacitance, C_L, from the gate-source capacitance (C_{gs}) and Miller capacitance ($C_{gd}(1 - A_v)$) (Figure 3.12).

The impact of C_L on the filter response depends on it's value relative to C, which is

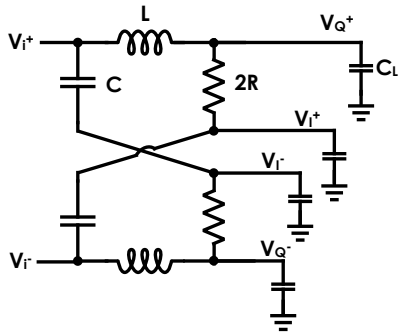
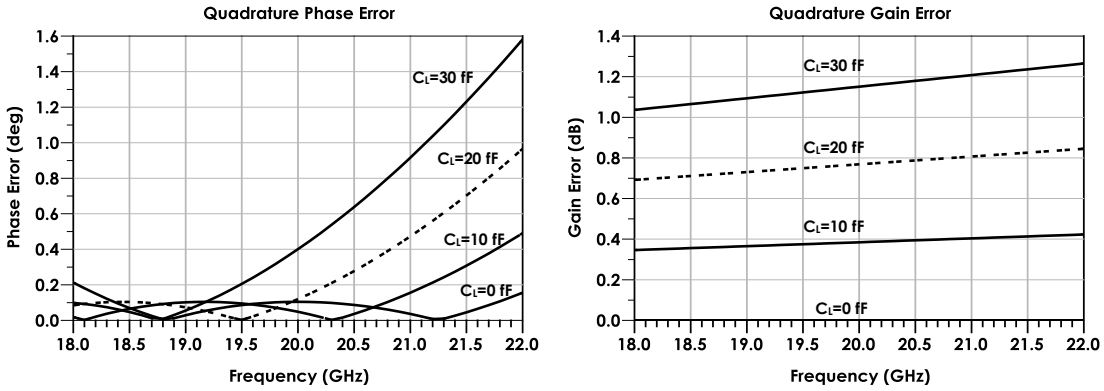


Figure 3.12: Quadrature filter with load capacitance

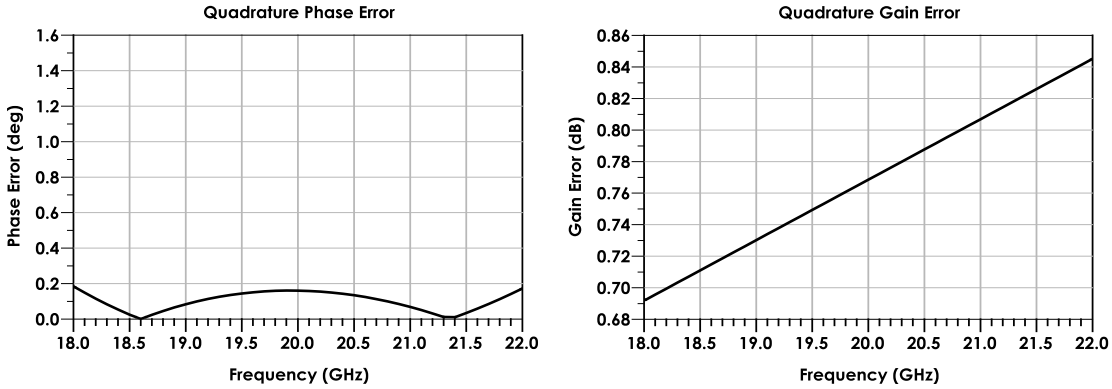
significant at $20\,GHz$. It adds an additional pole in the frequency response [36], shifting the filter's response to lower frequencies and increasing the phase error at the required band. This can be corrected by modifying the value of L and C to corrected the frequency offset. As an example, when the filter is terminated by a $20\,fF$ load, Figure 3.13a shows that the center frequency of the response shifts to $18.5\,GHz$. Thus, the load capacitance causes a $1.5\,GHz$ shift in the centre frequency. To correct this, the filter center frequency is adjusted to $\omega_c' = \omega_c + 1.5GHz = 21.5GHz$. The adjusted values, L' and C', are $257\,pH$ and $208\,fF$ respectively. The phase-corrected filter response is now re-centred as shown in Figure 3.14).

The gain error occurs because the load capacitance increases the loaded quality factor (loaded-Q) of the I-network (in parallel with the R-C branch) and dampens the Quality factor of the Q network (in parallel with the R-L branch). To rebalance the gain between both branches, the final quadrature filter in Figure 3.15 is used. A resistor is added in series with the inductor as shown, to dampen the loaded-Q of the I network without affecting the Q network. The plots in Figure 3.16 are the corrected phase and gain error of the filter when a 6Ω resistor is added in series with the inductor.



(a) Phase Error (b) Gain Error

Figure 3.13: Effect of Load Capacitance on the Filter Gain and Phase error [$L = 280\,pH$, $C = 220\,fF$, $R = 35\Omega$]



(a) Phase error (b) Gain error

Figure 3.14: Filter gain and phase error after phase error correction with $C_{load} = 20fF$ [$L' = 257\,pH$, $C' = 213\,fF$, $R = 35\Omega$]

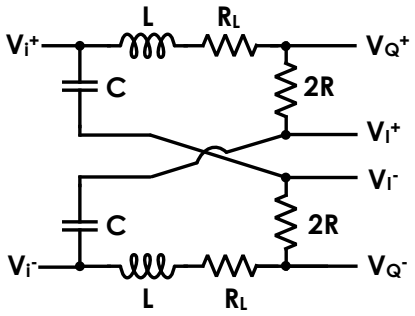
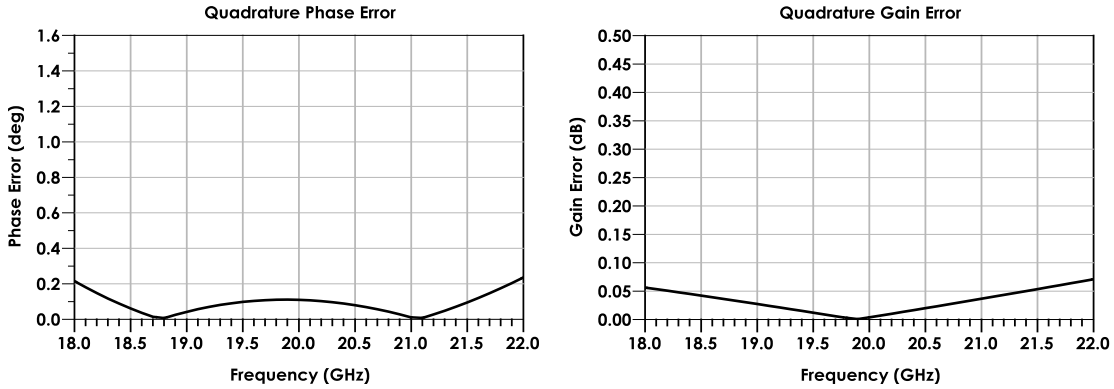


Figure 3.15: Complete quadrature filter

3.3.2 Amplifier and Combiner Network

Using the model in Figure 3.7b, two pairs of identical differential variable gain amplifiers are required for the I and Q network following the quadrature generator. Only one amplifier in each pair is required to operate at any one time, depending on what quadrant of the unit circle is required. The outputs from all four amplifiers are combined to one differential signal. Figure 3.17 shows the implemented amplifier and combiner network. M_{1-2}, M_{3-4}, M_{5-6} and M_{7-8} form four pairs of Gilbert amplifiers which employ current-mode combining at the drains. M_{1-2} and M_{3-4} are the in-phase amplifiers, while M_{5-6} and M_{7-8} are the quadrature-phase amplifiers. As illustrated in Figure 3.7b, the negative gain amplifiers are implemented by connecting M_{3-4} and M_{7-8} pair in reverse.

To access all 4 quadrants of the unit circle, only one of the differential pairs is enabled at a time. This is implemented by a switch at the tail source of each amplifier. B_I controls the switch at the tail source of the in-phase amplifiers (M_9/M_{10}) and B_Q controls the quadrature-phase (M_{11}/M_{12}). As an example, to access the first quadrant, the positive amplifiers are switched *on*, thus M_9 and M_{11} are connected to a bias voltage, $V_{DAC,I}$ and $V_{DAC,Q}$, while the negative amplifiers are switched off by grounding M_{10} and M_{12}.
The gain of each amplifier is controlled by varying the bias voltages, $V_{DAC,I}$ and $V_{DAC,Q}$.
All the amplifiers are current combined in a Gilbert cell topology at the source of M_{13-14}, which acts as a current buffer. M_{15-16} implements a single to differential current combiner which combines at the drain of M_{14} to a matching circuit at the output. To analyse the circuit, consider the simplified model in Figure 3.18 where the other differential pairs are removed and the current buffer is replaced by an output resistive network. The current-



(a) Phase error (b) Gain error

Figure 3.16: Filter gain and phase error after gain and phase error correction ($C_{load} = 20fF$) [$L' = 257\,pH$, $C' = 213\,fF$, $R = 35\Omega$, $R_c = 6\Omega$]

voltage relationship for the M_1 MOSFET in saturation is given as:

$$I_{D,1} = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 - \lambda(V_{DS} - V_{D,sat})) \tag{3.29}$$

The small signal transconductance as a function of a fixed drain current is computed as:

$$gm_1 = \sqrt{\mu_n c_{ox}\frac{W}{L}(1 - \lambda(V_{DS} - V_{D,sat}))I_{tail,I}} \tag{3.30}$$

which is also equal to the differential transconductance of the M_{1-2} pair. (3.30) shows that the transconductance of a single differential pair can be regulated by varying the tail bias current source.

Since the gilbert amplifier is a current combiner, the half-circuit current flowing into the buffer pair is:

$$I_{D,buf} = I_{D,1} + I_{D,5} \tag{3.31}$$

The overall transconductance of the combined amplifier is:

$$\begin{aligned} Gm &= \frac{\partial(I_{D,1} + I_{D,2})}{\partial V_{GS,1}} \\ &= gm_1 + gm_5 \\ &= \sqrt{\mu_n c_{ox}\frac{W}{L}(1 - \lambda(V_{DS} - V_{D,sat}))}\left(\sqrt{I_{tail,I}} + \sqrt{I_{tail,Q}}\right) \end{aligned} \tag{3.32}$$

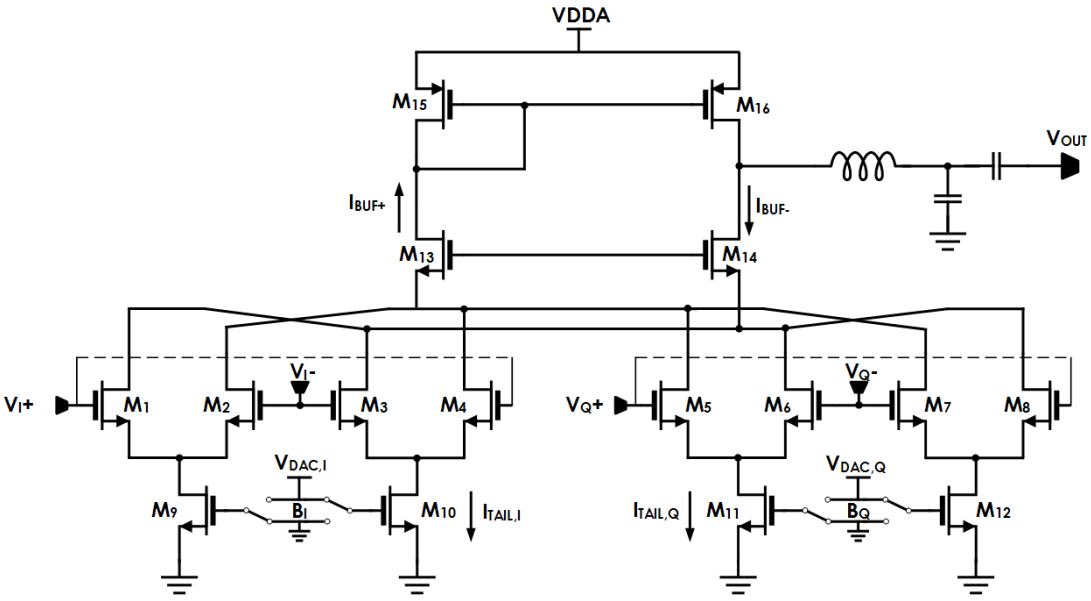


Figure 3.17: Variable gain amplifier network

Using (3.32), the small signal output voltage at the amplifier load is:

$$v_o = \sqrt{k_{eff}}\left(v_{i,I}\sqrt{I_{tail,I}} + v_{i,Q}\sqrt{I_{tail,Q}}\right)Z_L \tag{3.33}$$

where $k_{eff} = \sqrt{\mu_n c_{ox}\frac{W}{L}(1-\lambda(V_{DS}-V_{D,sat}))}$ and $v_{i,I}$ and $v_{i,Q}$ are the outputs of the quadrature filter. Assuming that $v_{i,Q} = v_{i,I}e^{j90^\circ}$, the output can be expressed as

$$v_o = v_i\sqrt{k_{eff}}\left(\sqrt{I_{tail,I}} + e^{j90^\circ}\sqrt{I_{tail,Q}}\right)Z_L \tag{3.34}$$

The small signal voltage gain is computed as:

$$A_v = \sqrt{k_{eff}}\left(\sqrt{I_{tail,I}} + e^{j90^\circ}\sqrt{I_{tail,Q}}\right)Z_L \tag{3.35}$$

From (3.35), the gain magnitude is equal to:

$$|A_v| = \sqrt{k_{eff}}Z_L\sqrt{I_{tail,I} + I_{tail,Q}} \tag{3.36}$$

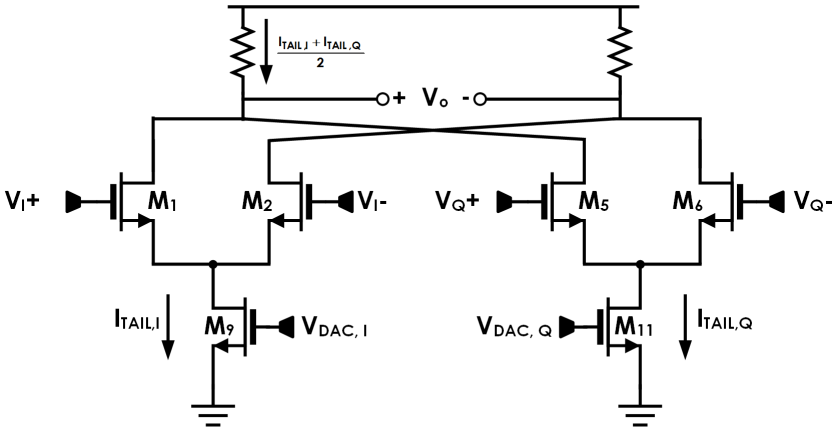


Figure 3.18: Simplified variable gain amplifier network

and the phase is:

$$\angle A_v = tan^{-1}\left(\sqrt{\frac{I_{tail,I}}{I_{tail,Q}}}\right) \tag{3.37}$$

The following conclusions can be made from (3.36) and (3.37):

1. The magnitude is proportional to the square root of the sum of the in-phase and quadrature-phase tail current sources.

2. The magnitude is constant if $I_{tail,T}(= I_{tail,I} + I_{tail,Q})$ is constant.

3. The phase varies as the inverse tangent of the square root of the current ratios. The phase has a very non-linear variation with currents and will have to be corrected to realise 5-bit accuracy.

The currents in the I and Q Gilbert networks are controlled by the voltages, $V_{DAC,I}$ and $V_{DAC,Q}$ which are driven by current based digital-to-analog converts (current DACs). The overall gain of the phase shifter can be increased by increasing the bias current (I_{tail}) or increasing the transistor W/L ratio. On the other hand, to minimize power consumption, a low tail current is used, but this will have a direct impact on gain. A large $\frac{W}{L}$ ratio can be used to increase the overall gain, but this will increase the capacitive loading effect at the output of the quadrature generator.

3.3.3 Current DAC

The current DAC is designed to enable 5-bit digital control of the phase shifts. It acts as a current mirror to the Gilbert network, as such, the control bits need to be sized according to the constraints in (3.36) and (3.37). A simplified schematic of the current DAC is shown in Figure 3.19.

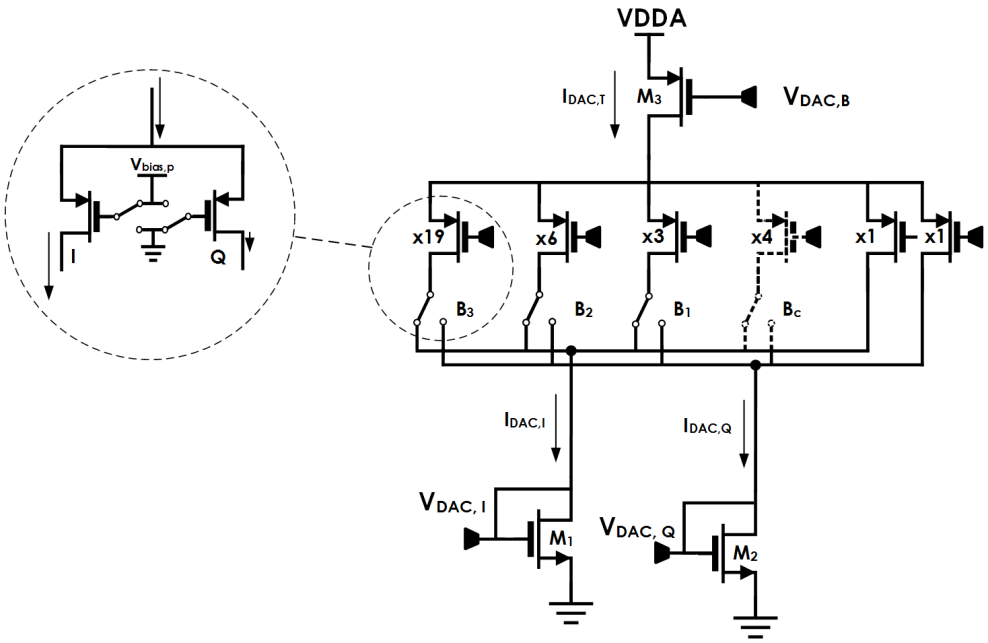


Figure 3.19: Current DAC (simplified schematic)

The PMOS current source, M_3 generates a constant tail current source, $I_{DAC,T}$. This is split between the in-phase and quadrature-phase paths by an array of digitally controlled PMOS transistors. Including the sign control, the function of the 6 control signals are summarised:

1. B_I and B_Q are the sign control bits which selects the unit circle quadrant. They also set the least significant phase setting within the quadrant of interest. This will be explained in detail.
2. B_1, B_2, and B_3 select the phase within any unit-circle quadrant with 3-bit precision
3. B_C is a bit to correct the 1-bit phase. This will also be explained in detail.

The topology ensures that $I_{tail,T}$, which mirrors to the Gilbert Amplifier, is constant, keeping the gain after the buffer constant.

Figure 3.20 is a graphical illustration of the digital control logic. The plot on the right is the phase for the normalised in-phase tail current based on (3.37), where

$$I_{tail,I}^{normalised} = \frac{I_{tail,I}}{I_{tail,T}} \tag{3.38}$$

The root-arc-tan function creates a non-linear mapping of the phase and DAC currents as shown in Figure 3.20. The digital control logic is implemented to compensate for this non-linearity.

A constant bias current is applied on both I and Q networks such that the minimum phase shift on any quadrant is $\frac{\Delta\phi_s}{2} = 5.6°$ as opposed to 0°. Thus, when switching between adjacent quadrants using B_I and B_Q, there is also a $\Delta\phi_s = 11.2°$ shift in phase. Figure 3.20 illustrates this by showing the effect of switching B_I from 0 to 1, which creates a phase shift from 354.4° to 5.6°

The transistor corresponding to the least significant bit is sized such that switching from

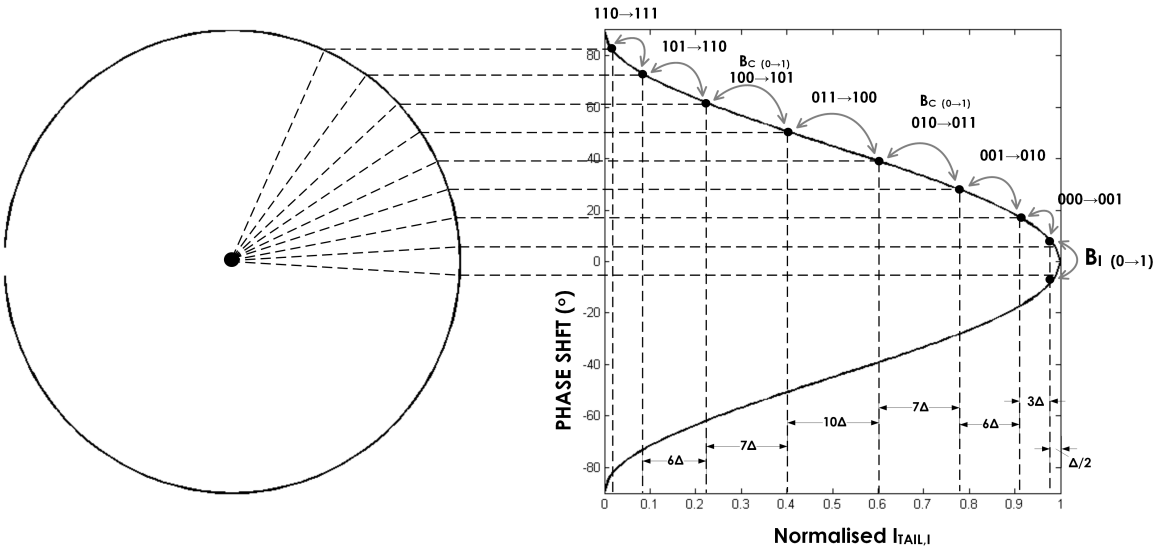


Figure 3.20: Current DAC digital phase control

the 000 state to 001 creates a phase shift from 5.6° to 16.9°. However, the least significant change in current required to create a phase shift from the 010 state to the 011 (28.1° → 39.4°) state is much higher than the current required at the 000 state. For this additional phase shift, a correction bit, B_C, is added to B_1, and is enabled at the 011 and 101 states. The combinatorial logic is thus written as:

$$B_C = B_3' B_2 B_1 + B_3 B_2' B_1 \tag{3.39}$$

which can also be implemented in AND-OR-INVERT (AOI) logic:

$$B_C = (B_3' B_2' + B_3 B_2 + B_1')' \tag{3.40}$$

The schematic of the combinatorial logic is shown in Figure 3.21.

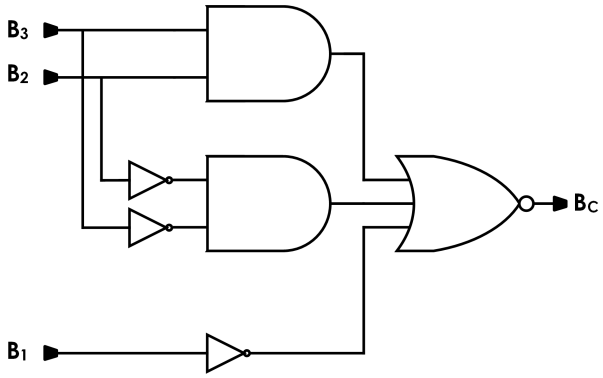


Figure 3.21: AND-OR-INVERT implementation of B_C

3.3.4 Complete Schematic, Simulation and Measurements

The schematic of the 20GHz active phase shifter is shown in Figure 3.22 (without the biasing network). The circuit was realised on a TSMC 65nm CMOS process, and operates on a 1.4V analog supply and a 1V digital supply. The phase shifter input is fully differential input signal and has a single-ended output. An input balun was not designed. A differential-to-single-ended converter was implemented using a PMOS active load topology which required a higher drain voltage. Other alternatives would have been a passive balun, which requires more area, or an active balun, which increases the overall power consumption.

The input and buffer transistors are implemented with $24 \times 0.06\,\mu m$ transistors as a compromise between the gain and capacitive loading. There is a $21\,fF$ input capacitance at the gate of each transistor, which loads each branch of the quadrature filter with $42fF$. The amplifiers are biased with $1.6\,mA$ for very low power with a g_m of $15\,mA/V$. The quadrature filter is designed with $L = 277\,pH$, $R = 107\,\Omega$, $C = 135\,fF$ and $R_L = 15\,\Omega$. All biasing circuits and current-DAC uses $0.8\,mA$.

The chip was tested by on-wafer probing using the measurement configuration illustrated in Figure 3.23. Assigning Port 1 and 2 as the differential input signal, and port 3

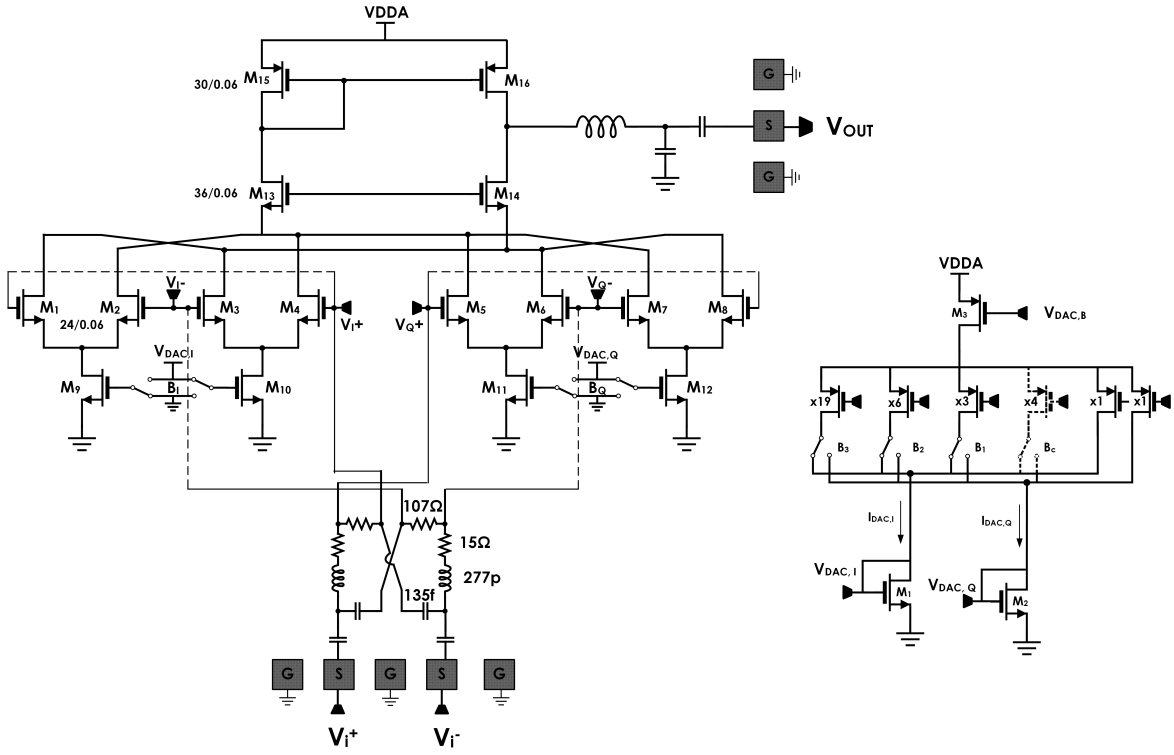


Figure 3.22: Phase shifter schematic

as a single-ended output. The 3-port scattering parameter (s-parameter) is converted to an equivalent 2-port mixed-mode s-parameter using the equations [41]:

$$S_{11,dd} = \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2} \qquad \text{differential-mode input reflection} \qquad (3.41)$$

$$S_{22,ss} = S_{33} \qquad \text{single ended output reflection} \qquad (3.42)$$

$$S_{21,sd} = \frac{S_{31} - S_{32}}{\sqrt{2}} \qquad \text{differential-mode to single-ended gain} \qquad (3.43)$$

$$S_{21,sc} = \frac{S_{31} + S_{32}}{\sqrt{2}} \qquad \text{common-mode to single-ended gain} \qquad (3.44)$$

The phase characteristics are obtained from the differential-to-single-mode gain:

$$\Phi_i = phase(S_{21,sd,i}) \qquad \text{For the i-th phase state} \qquad (3.45)$$

The phase performance is quantified using the rms-phase error defined as:

$$\Phi_{rms}^{error} = \frac{\sqrt{\sum_i^N (\Phi_i^{meas} - \Phi_i^{ideal})}}{N} \Bigg|_{N=32} \tag{3.46}$$

Finally, the Common-Mode Rejection ratio is calculated as:

$$CMRR = \frac{\text{Differential-Mode Gain}}{\text{Common-Mode Gain}} = \frac{S_{21,sd}}{S_{21,sc}} \tag{3.47}$$

The measured phase performance of the phase shifter is summarised in Figure 3.25 and is shown to achieve $< 5.5^\circ$ rms phase error between 19 and 21 GHz. The phase shifter has a 12 dB insertion loss (Figure 3.26a) as a consequence of low operating power and loss in the single-differential converter. There is 2 dB of gain variation (Figure 3.26b) over the 32 bit states. Although low, it shows some asymmetry in the circuit from mismatch. The input return loss is 10 dB on average and shows no variation with phase states. The Output Return Loss shows some variation but overall is 10dB between 17GHz and 21GHz. There is only 10dB of common-mode rejection which may need to be improved by redesigning the tail source and/or implementing a balun. The results are summarised in Table 3.1.

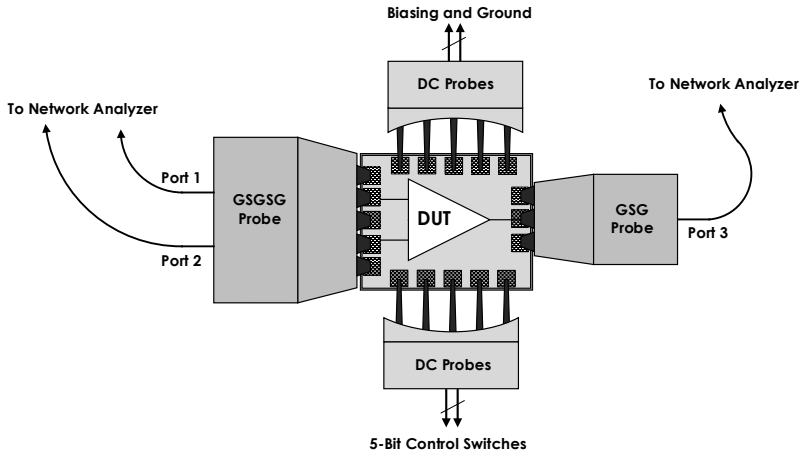


Figure 3.23: Differential to single-ended probe configuration

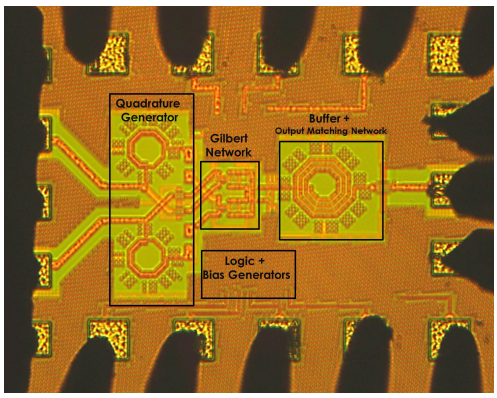
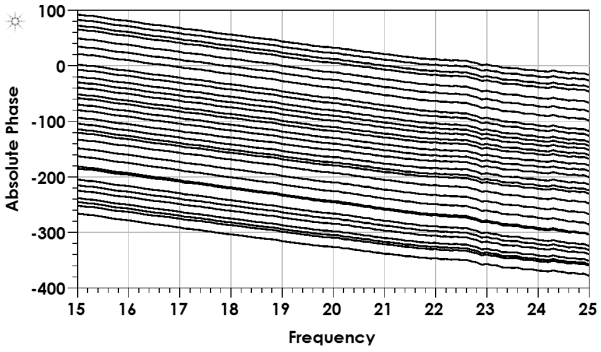
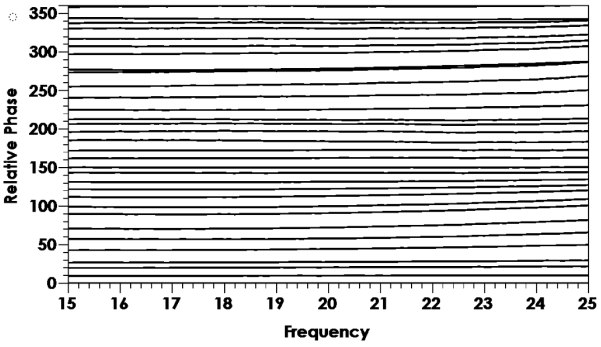


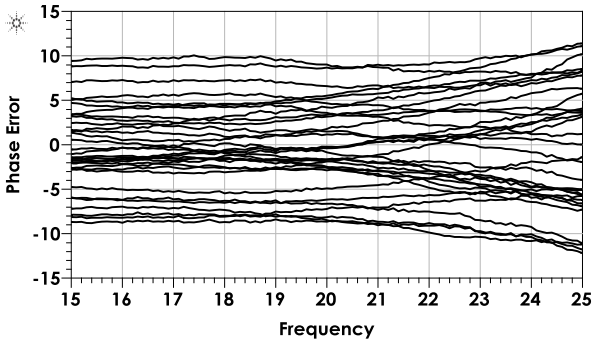
Figure 3.24: Phase shifter chip micrograph. $(0.6 \times 0.5\,mm^2)$



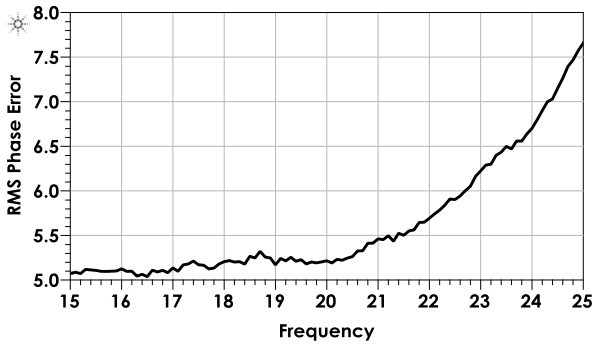
(a) Absolute phase response



(b) Relative phase

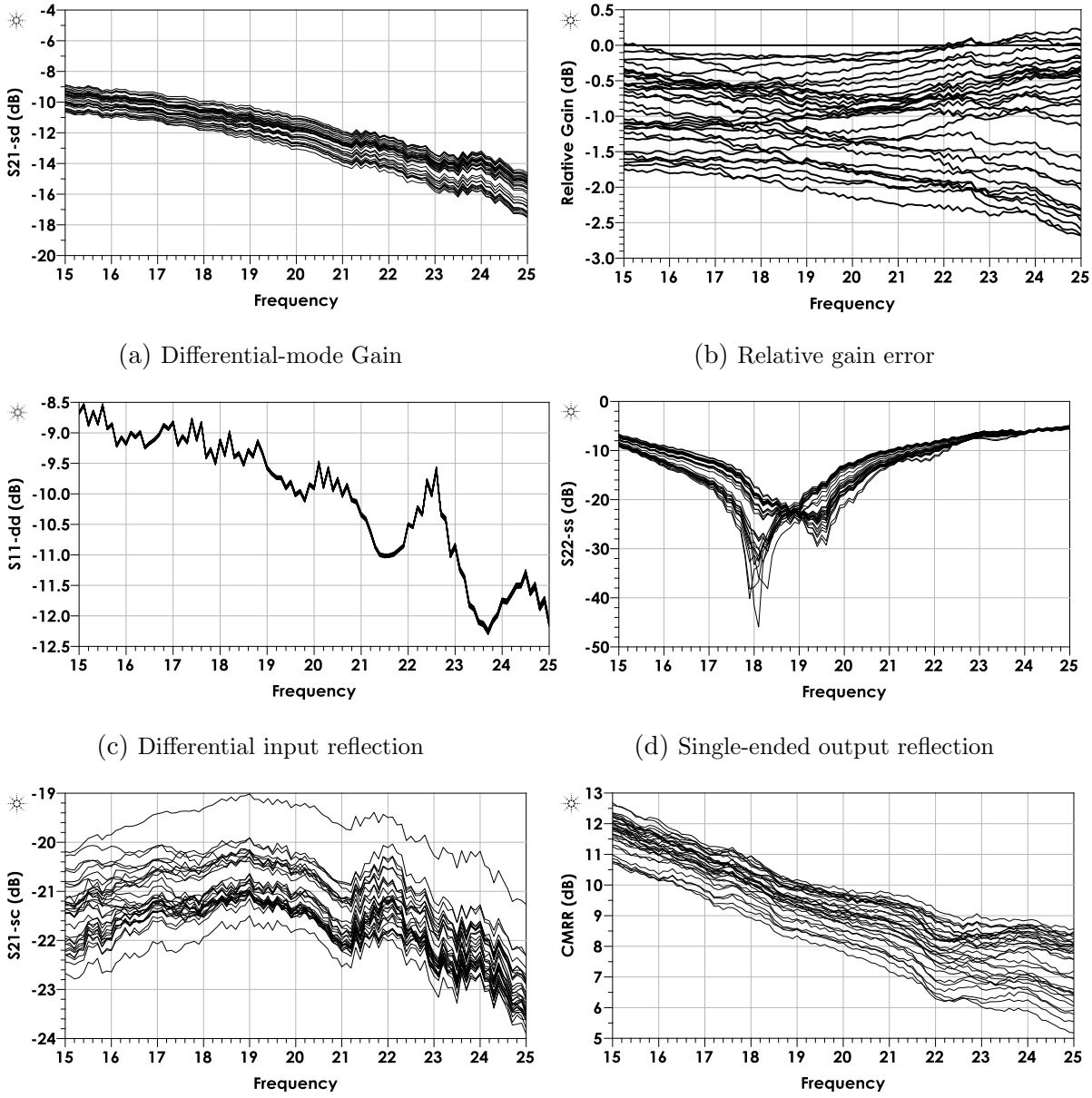


(c) Phase error



(d) RMS phase error

Figure 3.25: Phase shifter measured phase response for 32 States



(a) Differential-mode Gain

(b) Relative gain error

(c) Differential input reflection

(d) Single-ended output reflection

(e) Common-mode gain

(f) CMRR

Figure 3.26: Phase shifter gain and matching measurements for 32 states

Table 3.1: Design and performance summary of the $20\,GHz$ phase shifter

Parameters		**Results**
Design Summary	Technology	65nm CMOS
	Type	Vector-Sum based
	Die Area	$500 \times 600\,\mu m^2$ (including pads)
	Bits	5-bit (11.5° LSB)
Power	Voltage	$1.4\,V$
	Current	$4\,mA$ (including biasing and DAC)
	Power Consumption	$5.6\,mW$
Small-Signal	Center Frequency	$20\,GHz$
	Frequency Range	$19 - 21\,GHz$
	Differential Gain	$-12\,dB$ (at $20GHz$)
	Input Return Loss	$> 10\,dB$
	Output Return Loss	$> 10\,dB$
	RMS Phase Error	$< 5.5°$
	Gain Error	$< 2\,dB$

Chapter 4

Variable Gain Amplifiers

4.1 Variable Gain Amplifier Requirements

4.1.1 Pattern Synthesis

An N-element antenna array with each element having a radiation pattern, $f(\theta, \phi)$, generates a pattern which is the product of the elemental excitation and an array factor term, AF:

$$\begin{aligned} F(\theta, \phi) &= \frac{e^{-jkR}}{R} f(\theta, \phi) \sum_{i}^{N} a_i e^{jkr_i \cdot R} \\ &= \frac{e^{-jkR}}{R} f(\theta, \phi) AF(\theta, \phi) \end{aligned} \tag{4.1}$$

The array-factor and element excitation form a discrete fourier transform(DFT) pair between the u-space and k_x-space, where the element excitation coefficients are sampled versions of a continuous source distribution at sampling intervals, d_x. As long as the space between element samples is $< \lambda/2$(λ is the wavelength in free-space), there would be no grating lobes[6] and the pattern will be identical to the continuous distribution pattern. These grating lobes are the images that appear due to spatial aliasing.
In array synthesis, the continuous element distribution is first derived from a desired radiation pattern based on requirements such as the side-lobe level and beam-width. The excitation coefficients are obtained by sampling the continuous distribution at spatial intervals(ideally $< \lambda/2$). This section will briefly discuss pattern tapering and it's effects on the side-lobe level.

4.1.2 Tapering and Dynamic Range

In low noise satellite receivers, the side-lobes have a detrimental effect on the (G/T) because these lobes pick up environmental noise and radiation around the antenna. From the DFT relation, a uniformly distributed (rectangular) array (Figure 4.1a) has a sinc-squared radiation pattern with the first side-lobe $13.2\,dB$ below the main lobe [6].
"Window functions", as used in signal processing, can be applied to the rectangular distribution to obtain lower side-lobes, at the cost of increasing the main beam-width. The Dolph-Chebyshev array pattern (Figure 4.1c) uses an equi-ripple response, which yields the smallest beam-width for a given side-lobe level. The disadvantage of this is that it maintains a constant side-lobe level everywhere, making the antenna susceptible to noise and interference.

Taylor[42] introduced a distribution which compromises between the beam-width and side-lobe level offered by the Chebyshev distribution. It allows only a limited number of equi-ripple side-lobes and attenuates the rest at the cost of an increased beam-width. Figure 4.1c and 4.1e shows the radiation pattern for the 20-element array with a Chebyshev and Taylor distribution for a $20\,dB$ side-lobe level. Unlike the Chebyshev distribution, the side-lobes decay with the angle from the main lobe. Taylor distribution is determined first from the side-lobe level, R, which represents ratio of the main lobe and first side-lobe peaks, from which the factor, A, is obtained as [43]:

$$A = \frac{1}{\pi} cosh(R)^{-1} \tag{4.2}$$

The number of equi-ripple side-lobes, $\overline{n}$, is also specified. A smaller $\overline{n}$ means a faster side-lobe decay rate, but leads to larger beam-width. Very small values of $\overline{n}$ ($\overline{n} < 3$) could also lead to distortions in the side lobe pattern [10]. The normalised array coefficients required to generate the taylor distribution is given as:

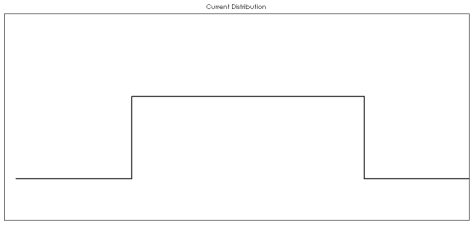
$$F(m, A, \overline{n}) = \frac{[(n-1)!]^2}{(\overline{n}-1+m)!(\overline{n}-1-m)!} \prod_{n=1}^{\overline{n}-1} (1 - \frac{m^2}{z_n^2}) \tag{4.3}$$

where, z_n are the zero location of the pattern:

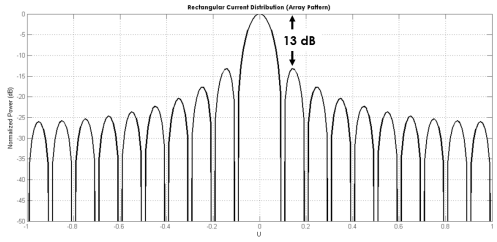
$$z_n = \pm\sigma(A^2 + (n - 1/2)^2)^{\frac{1}{2}} \tag{4.4}$$

and σ, known as the *dilation factor*, is given as:

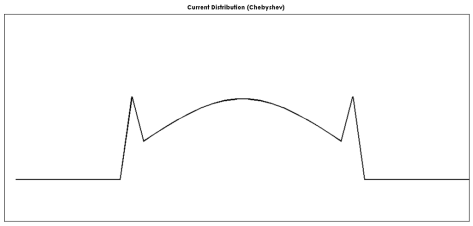
$$\sigma = \frac{\overline{n}}{[A^2 + (\overline{n} - 1/2)^2]^{\frac{1}{2}}} \tag{4.5}$$



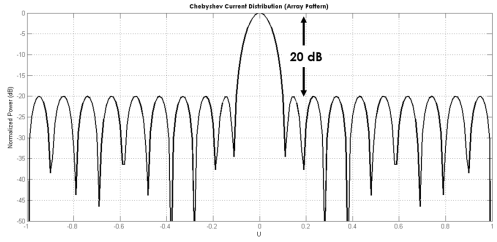
(a) Rectangular current distribution



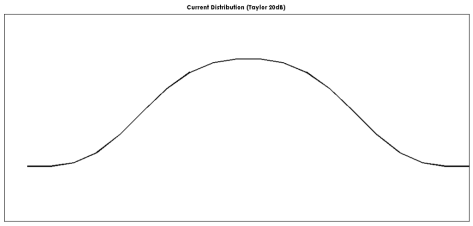
(b) Radiation pattern



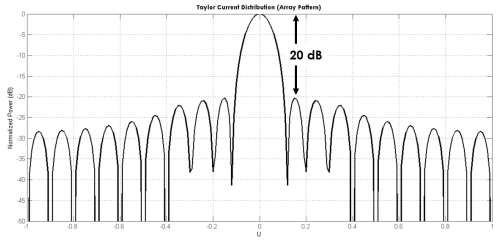
(c) Chebyshev current distribution



(d) Radiation pattern



(e) Taylor current distribution



(f) Radiation pattern

Figure 4.1: Tapered current distribution and the corresponding radiation pattern

The dilation factor is responsible for broadening the main lobe. $m = 0, \pm 1, \pm 2, ...$ are indexes of the sample location spaced d_x apart.
Tapering in the elemental excitation can be realized with variable gain amplifiers (VGA) or variable attenuators (VA). One criteria in the VA/VGA design is the gain/loss dynamic range. Figure 4.2 plots the normalised line source distribution required to realize radiation patterns with different side-lobe levels in a 41 element array with 5 equi-ripple side-lobes.

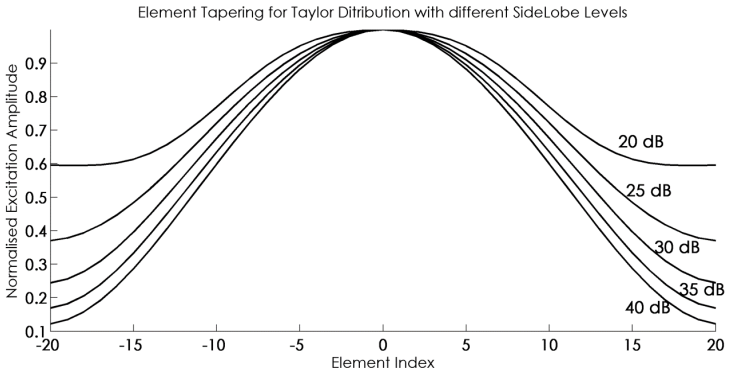


Figure 4.2: Line source distribution for various side-lobe levels

The dynamic range is obtained from the difference between the centre element and the edge element. For a $35\,dB$ side-lobe level, the edge element is tapered by a factor of 0.2 with reference to the centre element, thus a VGA/VA with $14\,dB$ dynamic range is required. Figure 4.3 plots the dynamic range against the required side-lobe level for a normalised taylor distribution with $\overline{n} = 5$.

4.2 Digitally Controlled Variable Gain Amplifiers

4.2.1 VGA Implementation in CMOS

Variable gain amplifiers can be implemented with either analog or digital gain control. Analog VGAs output a continuous range of gain control given an analog input voltage or current. Digital VGAs output quantized gain levels based on digital control bits. This amplitude quantization has an effect on the side-lobe level[34], but unlike phase quantization, it is harder to define a closed form relation for non-uniform tapering. Refer to Appendix C for more details on quantization effects. The digital gain control can be implemented

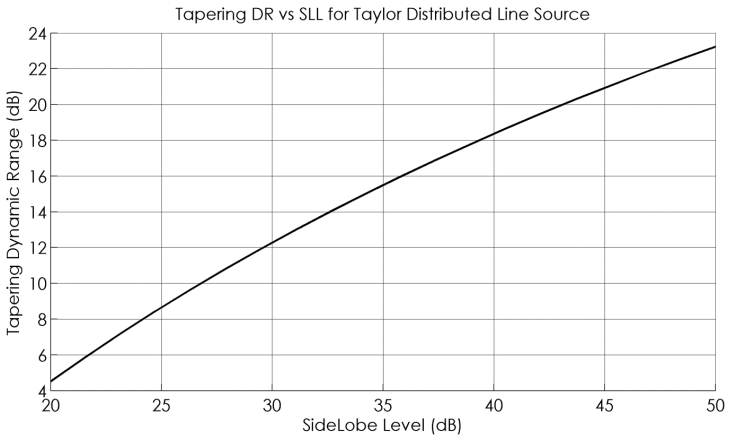


Figure 4.3: Tapering dynamic range vs side-lobe level

as either *linear-in-magnitude*, or *linear-in-decibels*. Since the elemental tapering is determined by a ratio to a normalised amplitude level, a VGA with linear-in-dB gain control will better utilize the full dynamic range.
The voltage gain of general amplifiers can be written as:

$$A_v = g_{m,eff} r_{out} \tag{4.6}$$

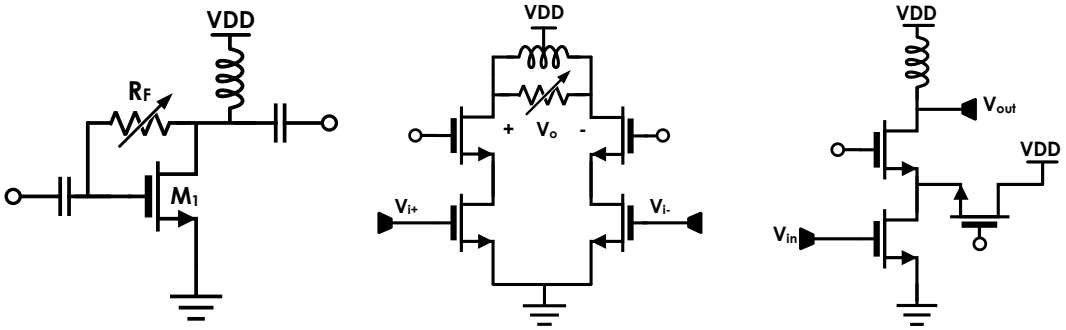
where $g_{m,eff}$ and r_{out} are the effective transconductance and intrinsic output resistance respectively. VGAs are typically designed by varying one of these two parameters. Common VGA topologies in CMOS include:

1. Variable load resistors[44] (Figure 4.4a)
2. Variable feedback factor (Figure 4.4b)
3. Current Steering / Current Bleeding topologies [45, 46] (Figure 4.4c)

Some important figure of merit depending on the topology used include:

1. Dynamic Range (Gain)
2. Bandwidth
3. Low phase variation
4. Low phase and group delay distortion

The current steering topology is very resistant to variations in phase and input return loss, but has limited dynamic range. It should be noted that while phase variation over a narrow bandwidth can be corrected by the phase shifter, it cannot correct phase errors that change *over the entire bandwidth*.



(a) (b) (c)

Figure 4.4: Typical VGA implementations

4.2.2 Current Steering VGA Analysis

Gain Variation

The current steering VGA is adapted from the cascode topology. Figure 4.5a is a simplified schematic of the basic current steering VGA. The common-source transistor, M_1 remains the same as the cascode, while the common-gate transistor, M_2, is paired with a current bleeding transistor, M_3. The total bias current flowing into the input transistor is the sum of the current through the common gate and the current bleed transistor:

$$I_{bias} = I_{cg} + I_{bleed} \tag{4.7}$$

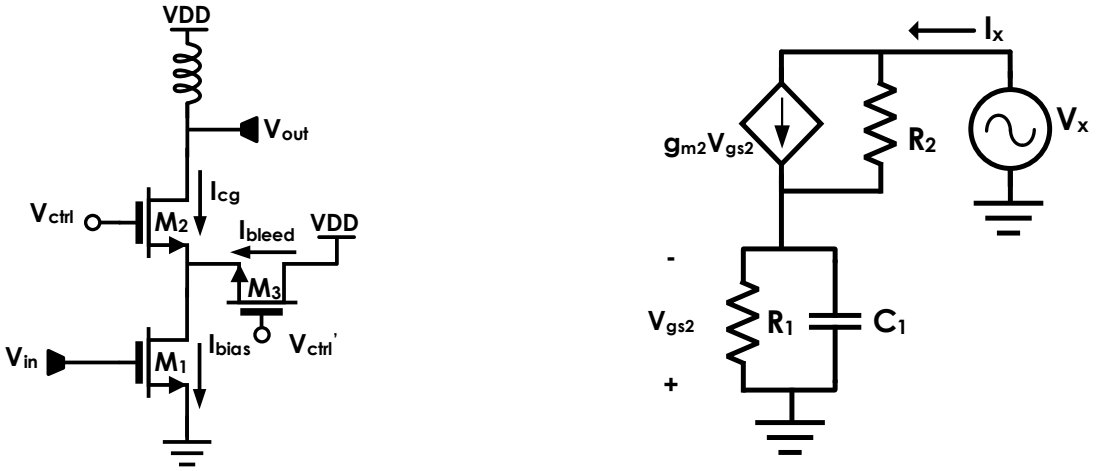
From the low noise amplifier chapter, the effective transconductance of the cascode is given as:

$$g_{m,casc} = g_{m1}\left(1 - \frac{1}{(g_{m2}ro_1 + \frac{ro_1}{ro_2})(\frac{1}{1+j\omega C_{gs2}ro_1})}\right) \tag{4.8}$$

The $(\frac{1}{1+j\omega C_{gs2}ro_1})$ term is approximately unity below ω_T. As an initial approximation, assume that $ro_1 = ro_2$:

$$g_{m,casc} = g_{m1}\left(1 - \frac{1}{(g_{m2}ro_1 + 1)}\right) = g_{m1}\left(1 - \frac{1}{\left(\sqrt{k_n(\frac{W}{L})_2 I_{cg}}ro_1 + 1\right)}\right) \tag{4.9}$$

If M_2 is switched off(i.e, $I_{cg} = 0$), then $g_{m2} = 0$ and from (4.9), $g_{m,casc} = 0$. If M_2 is in saturation, and $g_{m2}ro_1 >> 1$, then $g_{m,casc} \approx g_{m1}$. This simple analysis shows that



(a) Schematic

(b) Cascode Output resistance

Figure 4.5: Analog current steering VGA schematic

by varying the transconductance of common-gate transistor through current steering, the effective transconductance of the cascode can be controlled. The voltage gain is written as:

$$A_v = -g_{m,casc}(Z_{o,casc}||Z_L) \tag{4.10}$$

where $Z_{o,casc}$ is the intrinsic output impedance of the cascode given as:

$$Z_{o,casc} = \frac{V_x}{I_x} = g_{m2}Z_{o1}Z_{o2} + Z_{o1} + Z_{o2} \tag{4.11}$$

if $Z_{o,casc} >> Z_L$, then:

$$A_v \approx -g_{m,casc}Z_L \tag{4.12}$$

A variable gain amplifier with a constant input impedance can be realized by adjusting I_{cg} while keeping I_{bias} constant. This is implemented using the current bleeding transistor which is biased in complement with the common-gate transistor such that, $I_{cg} + I_{bleed}$, is constant.

Phase Variation

Although the input impedance remains constant, the phase variation in the current steering VGA is due to changes in the *complex impedance* seen at the output node of the cascode. The overall transconductance in (4.8) has little or no phase variation with g_{m2}, thus:

$$\begin{aligned} \phi &= \angle(-g_{m,casc}Z_{out}) \\ &= 180 + tan^{-1}(\frac{X_{out}}{R_{out}}) \end{aligned} \tag{4.13}$$

The loaded output impedance of the current steering topology is:

$$Z_{out} = Z_{o,casc}||Z_L \tag{4.14}$$

where Z_L is the impedance of the load and bias circuit. $Z_{o,casc}$ from (4.11) is given by substituting $Z_{o1} = R_{o1}||\frac{1}{j\omega C}$ and $Z_{o2} = R_{o2}$:

$$Z_{o,casc} = \frac{V_x}{I_x} = g_{m2}R_{o2}\big(R_{o1}||\frac{1}{j\omega C_1}\big) + \big(R_{o1}||\frac{1}{j\omega C_1}\big) + R_{o2} \tag{4.15}$$

(4.15) shows that $Z_{o,casc}$ will show variations in complex impedance with g_{m2}, leading to phase variations in Z_{out}. However, this can can be minimized if $Z_{o,casc} >> Z_L$,(making $Z_{out} \approx Z_L$) and using a purely resistive load.

4.2.3 10dB DR, 5-bit Digital VGA in 65nm CMOS

The design and sizing of the common-source and common-gate transistors follow a similar procedure to the low noise amplifier (LNA) design. However, since the VGA is placed after the LNA, the noise figure requirement is relaxed. Also recall that the LNA was designed to have the receiver tolerate $15\,dB$ noise figure from the beam-forming network. The VGA is required for a Taylor distributed line source with $> 25\,dB$ side-lobe level (First SLL requirement is $> 20\,dB$). This corresponds to a $10\,dB$ dynamic range. To achieve this dynamic range, with less than 6° phase error ($\frac{1}{2}LSB$ phase shift) over a 10% bandwidth, a resistive drain network is used to minimize the phase-frequency variation (Figure 4.6). Real resistors might be impractical as a results of the voltage drop (depending on the drain current used), hence, an active inductor is used to synthesize a resistive load.

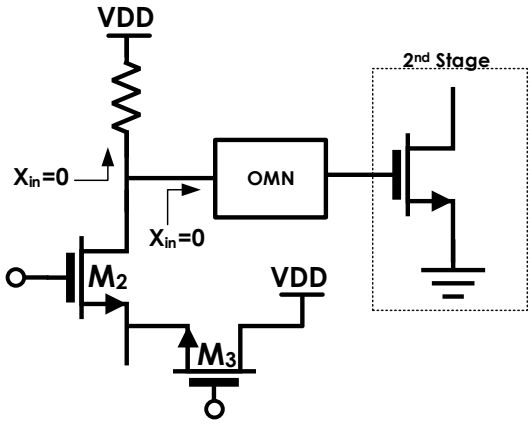


Figure 4.6: Resistive drain network for low VGA phase-frequency variation

Active Inductor Load

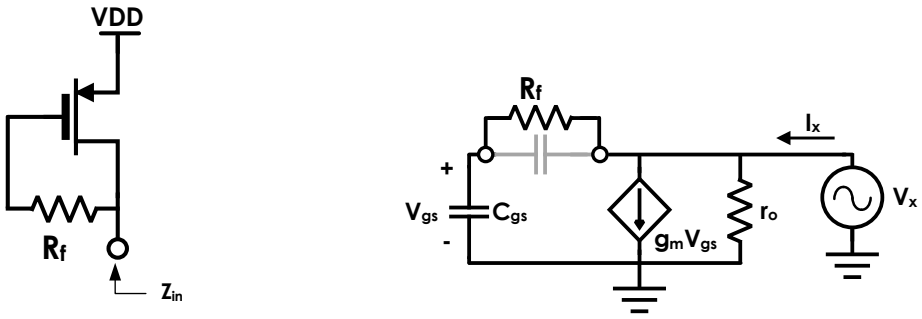
The active inductor is a means of realizing an equivalent inductance using transistors. The PMOS active inductor load is shown in Figure 4.7. The impedance can be written as (see Appendix D for derivation):

$$\begin{aligned} R_{in} &= R_f \frac{\omega^2}{\omega_T^2} + \frac{1}{g_{mp}} \\ X_{in} &= \frac{\omega}{\omega_T}\left(R_f - \frac{1}{g_{mp}}\right) \end{aligned} \tag{4.16}$$

which is purely resistive if $R_f = \frac{1}{g_{mp}}$. Also the active inductor is approximately real over a wide frequency range(Figure 4.8) and bias conditions(Figure 4.9).

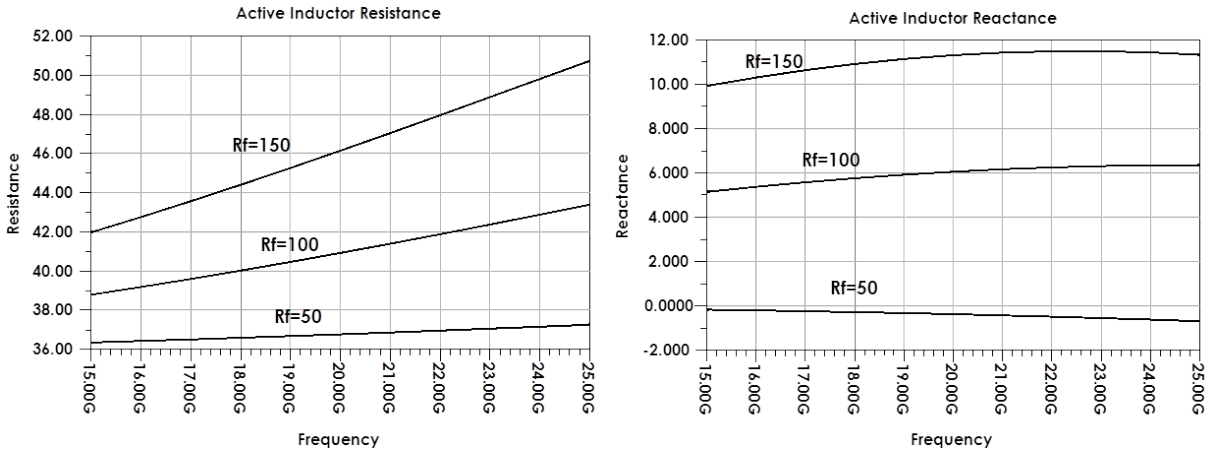
Linear-in-dB Digital Control Implementation

The digital control is implemented by using switched transistors to control the common-gate and current bleeding transistor. Figure 4.10 is a simplified circuit implementation. It consists of a constant bias transistor, M_2 and a number of binary controlled switched transistors with current bleeding complements. M_2 is sized to conduct the minimum I_{cg} determined from the dynamic range, which in-turn is limited by the phase error of the



(a) PMOS type (b) PMOS type (small signal)

Figure 4.7: Active inductor load and small signal model



(a) Resistance (b) Reactance

Figure 4.8: Impedance of active inductor with $\frac{1}{g_m} = 50\Omega$

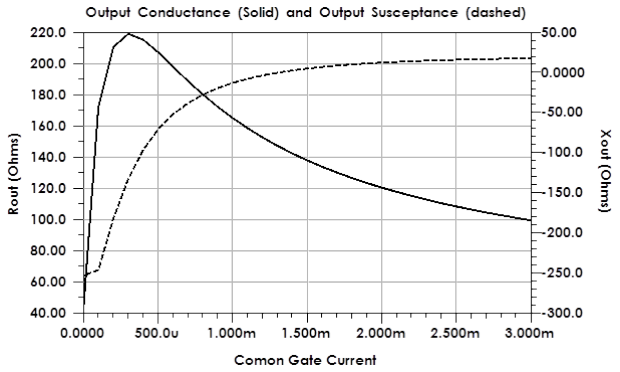


Figure 4.9: Active inductor R_{out}, X_{out} [$R_f = 400\Omega$, $W = 50\,\mu m$] at $20\,GHz$

circuit (with the active inductor). Transistor M_2 can be sized such that:

$$I_{cg,min} = \frac{W_{M2}}{W_{cg,T}} \times I_{bias} \tag{4.17}$$

where $W_{cg,T}$ is the total width of all common-gate transistors. The digital control is imple-

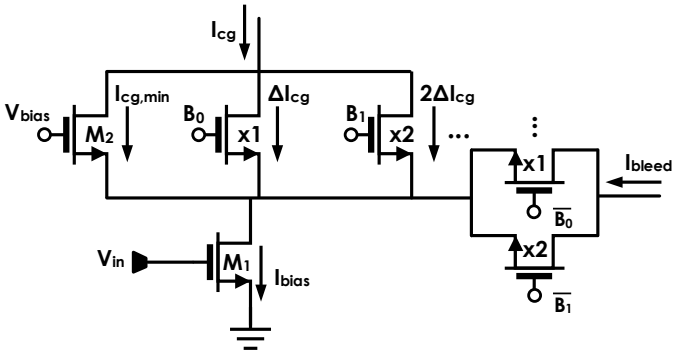


Figure 4.10: Switched transistor implementation of the current steering VGA

mentation by switching between conducting transistors. The overall g_m of the common-gate stage can be written as:

$$g_{m,cg} = g_{m2} + B_0 g_{m,b0} + B_1 g_{m,b1} + \cdots + B_N g_{m,bN} \tag{4.18}$$

where $B_0, \cdots, B_N$ are the binary control bits. By expanding the g_{m2} term in (4.9), (where $g_{m,cg} = g_{m2}$):

$$g_{m,vga} = g_{m1}\left(\frac{(g_{m2} + B_0 g_{m,b0} + B_1 g_{m,b1} + \cdots + B_N g_{m,bN}) ro_1}{[(g_{m2} + B_0 g_{m,b0} + B_1 g_{m,b1} + \cdots + B_N g_{m,bN}) ro_1 + 1]}\right) \tag{4.19}$$

Noting that the binary control sets $B_N = 0/1$, it is possible to decompose the terms in the parenthesis as an algebraic sum in the form:

$$g_{m,vga} = g_{m1}\Big(K(g_{m1}) + B_0 K(g_{m,b0}) + B_1 K(g_{m,b1}) + \cdots + B_N K(g_{m,bN})\Big) \tag{4.20}$$

where $K(g_{m1}) + K(g_{m,b0}) + \cdots + K(g_{m,bN}) \leq 1$. (4.20) presents the transconductance of the VGA as a magnitude variation set by the control bits. The overall gain is approximately:

$$A_v \approx -g_{m,vga} Z_L \qquad (Z_{o,vga} >> Z_L) \tag{4.21}$$

The transistors are sized such that each term, $K(g_{m,bN})$, is a linear-in-dB variation in gain.

4.2.4 Complete Design, Simulation and Results

Schematic and Layout

The complete 5-bit two-stage VGA schematic is shown in Figure 4.11. The $10\,dB$ dynamic range is split between two stages. The first stage controls the lower 4-bits of digital gain control with $5dB$ dynamic range, while the second stage controls the most significant bit with $5\,dB$ dynamic range. The unit cell transistor has a $2.1\,\mu m$ width and requires a $1\,V$ gate bias. Thus, the VGA is compatible with digital logic. A $1.4\,V$ drain bias is required, which is also compatible with the phase-shifter. The first stage is biased at a lower current density for low noise and the second stage is biased at a higher current density for linearity. The current bleeding transistors are terminated with a diode-connected PMOS transistor which is matched to the active inductor of the common-gate transistors. This ensures that the steered current matches the conducting current. Both stages use $4mA$ of bias current. The complete layout with pads is shown in Figure 4.12

Simulation

The result from s-parameter simulation after extraction are plotted in Figure 4.13. The two stage VGA has an overall voltage gain of $16\,dB$ with $10\,dB$ dynamic range and 5-bit control ($\Delta G = 0.3125\,dB$). There is $> 10\,dB$ return loss at the input over the 10%

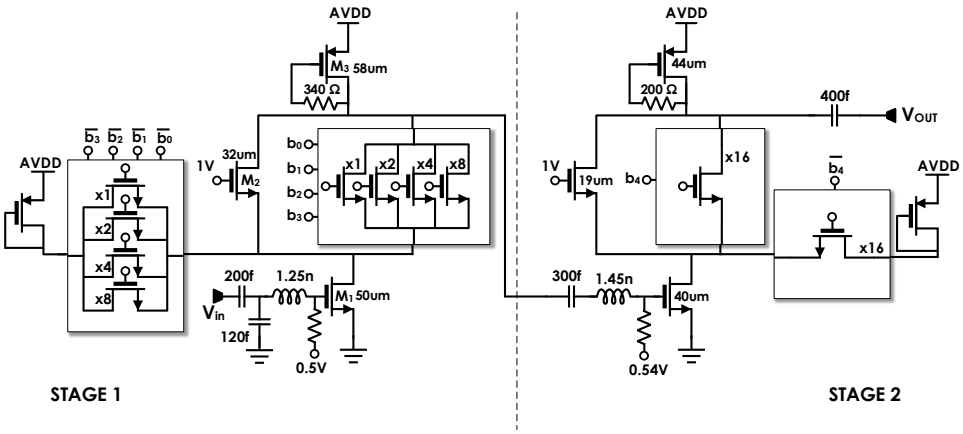


Figure 4.11: Two-stage current steering VGA schematic

bandwidth ($19\,GHz - 21\,GHz$), and the output shows $> 11\,dB$ over a wide range. The active inductor, shows very little frequency variation as an output impedance. The overall noise figure varies from $4.7\,dB$ to $7.5\,dB$ from the highest to the lowest gain setting.
The VGA achieves $< 3^{\circ}$ phase error over the required $2\,GHz$ bandwidth for the 32 phase states.

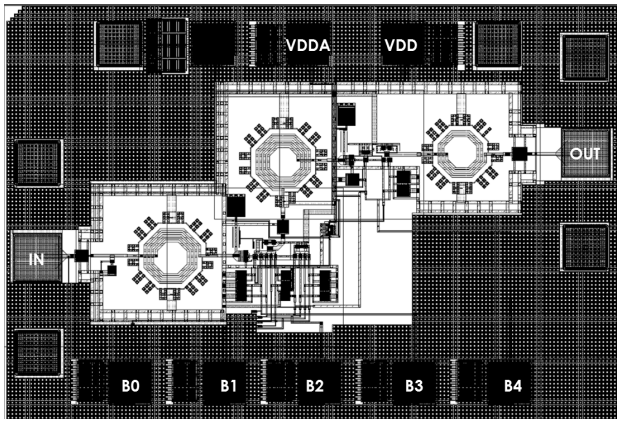
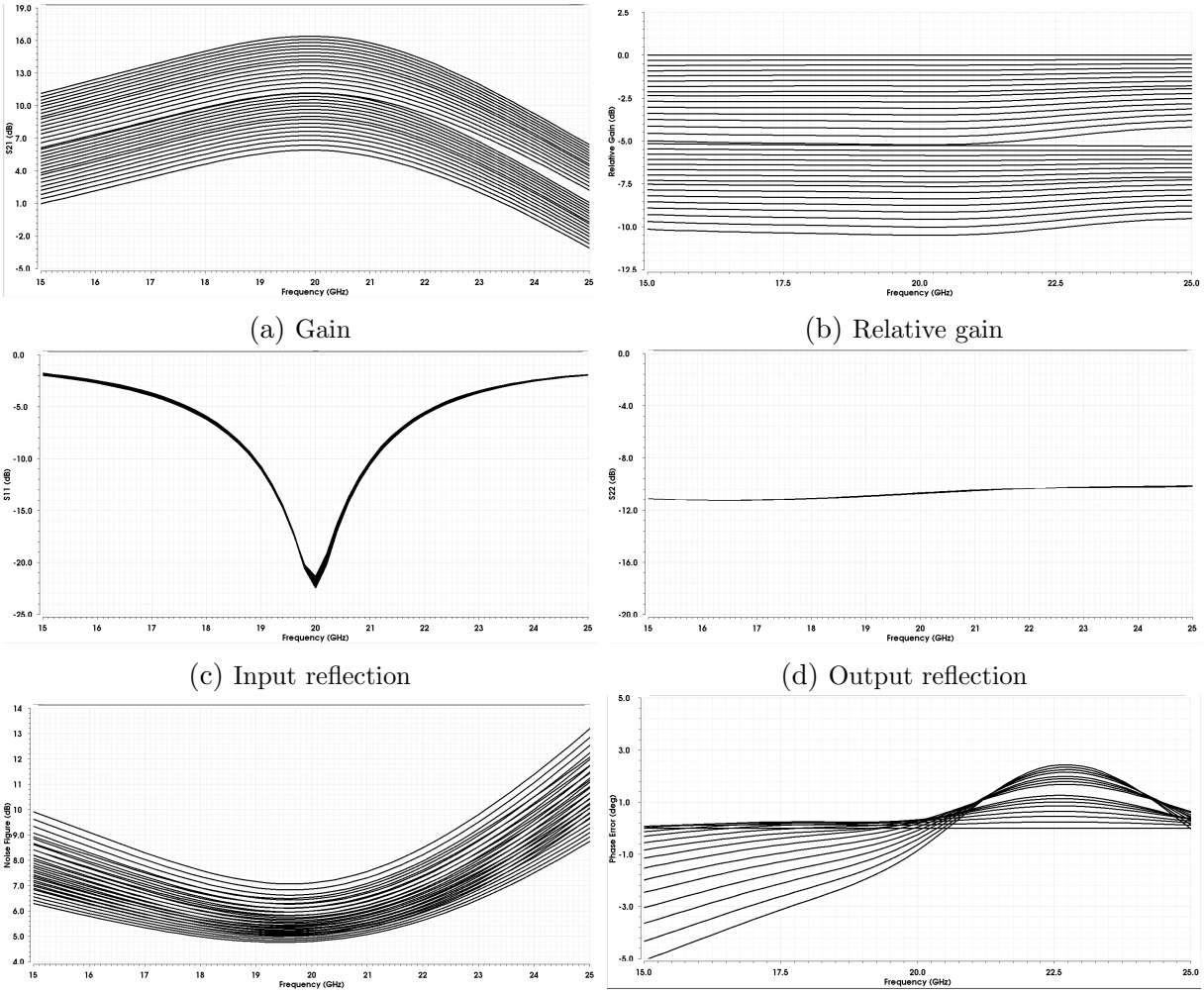


Figure 4.12: Current steering VGA layout

Table 4.1: VGA design and performance summary

Parameters		**Results**
Design Summary	Technology	65nm CMOS
	Stages	2
	Die Area	$750 \times 550\,\mu m^2$ (with pads)
	Bits	5-bit
Power	Voltage	$1.4\,V$
	Current	$8\,mA$ ($4\,mA$ Stage 1, $4\,mA$ stage 2)
	Power Consumption	$11.2\,mW$
Small-Signal	Center Frequency	$20\,GHz$
	Frequency Range	$19 - 21\,GHz$
	Gain	$6 - 16\,dB$
	Input Return Loss	$> 10\,dB$
	Output Return Loss	$> 11\,dB$
	Reverse Isolation	$> 50\,dB$
	Noise Figure	$4.8\,dB - 7.5\,dB$
	Phase Error	$< 3^{\circ}$



(a) Gain

(b) Relative gain

(c) Input reflection

(d) Output reflection

(e) Noise figure

(f) Phase error

Figure 4.13: Simulated performance of the 5-bit 20GHz VGA

Chapter 5

Single Channel System Analysis

5.1 System Overview

The single-channel receiver front-end module (FEM) is illustrated in Figure 5.1. It consists of a pair of *low noise amplifiers* connected to a *90° hybrid coupler*. A *switch* connects to one of the two outputs of the coupler to the *variable gain amplifier* and outputs to the *phase shifter*. To provide a fixed and stable bias, a bandgap voltage reference is also required.

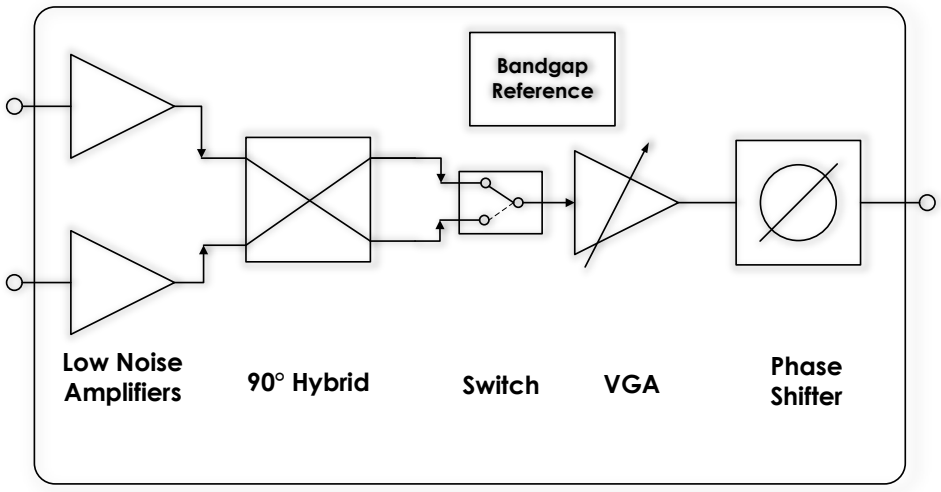
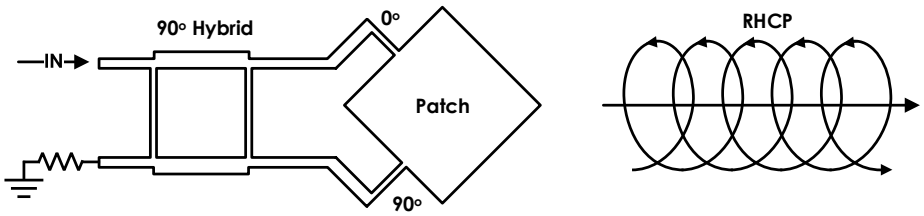
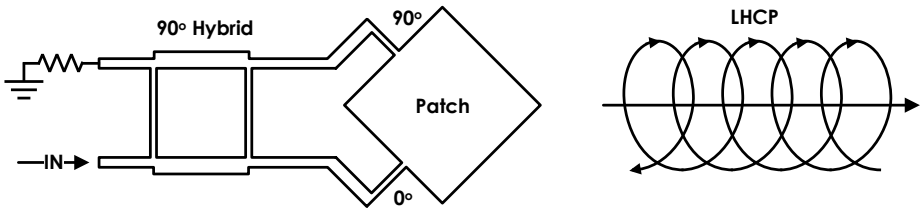


Figure 5.1: Illustration of the single channel receiver



(a) RHCP



(b) LHCP

Figure 5.2: Dual-fed circularly polarised patch element

The hybrid coupler and switch are required to implement both left and right-hand circular polarisation(CP). Circular polarisation is obtained by exciting two orthogonal modes in the current distribution of the antenna element [47]. In microstrip antennas, this can be achieved in two ways [47, 48]:

1. *Singly-fed circular polarisation*: The patch is perturbed to generate orthogonal eigenmodes.
2. *Dual-fed circular polarization*: The patch is fed on perpendicular ends with quadrature inputs.

The advantage of the singly-fed CP patch is the simplicity of the feed network, however, with the dual-fed patch, it is possible to change the *handedness* of the radiation pattern. The hybrid coupler implementation of the dual-fed CP patch in shown in Figure 5.2. By switching between the input ports of the hybrid coupler, the phase relation of the output fed to the patch can be reversed producing either a right-handed or left-handed circularly polarised radiation pattern. The next few sections summarise the additional circuits of the single channel receiver module.

5.2 Quadrature (90°) Hybrid Coupler

5.2.1 Branch Line Coupler

In microwave network theory, the quadrature hybrid coupler is a directional coupler which produces equal outputs with 90° phase difference. It is associated with the following s-parameter matrix [49]:

$$[S] = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{5.1}$$

where the output $S_{21} = \frac{-j}{\sqrt{2}}$ and $S_{31} = \frac{-1}{\sqrt{2}}$ are 90° out of phase with $3\,dB$ power split. The fourth port is the isolated port and $S_{41} = 0$ if all four ports are matched. The most common implementation of the quadrature hybrid is the branch-line coupler (Figure 5.3).

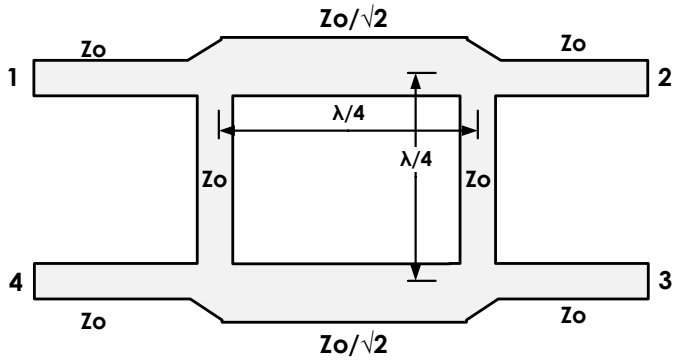


Figure 5.3: Branch-line coupler microwave network

The branch line coupler is designed from quarter-wavelength segments with characteristic impedances, Z_0 and $Z_0/\sqrt{2}$. All ports are impedance matched to the system impedance, Z_0 if terminated with Z_0 loads.

5.2.2 On-Chip Implementation of the Branch-Line Coupler

Theory and Implementation

Quadrature hybrids on IC's have been designed using LC-based[50] and transformer-based [51, 52] lumped element networks. A branch line coupler can be realised using π or *tee* lumped-element equivalent quarter-wave circuits[53](see Appendix E). As illustrated in Figure 5.4, if the π network is used, there will be redundant parallel elements which can be absorbed, reducing the component count by 4.

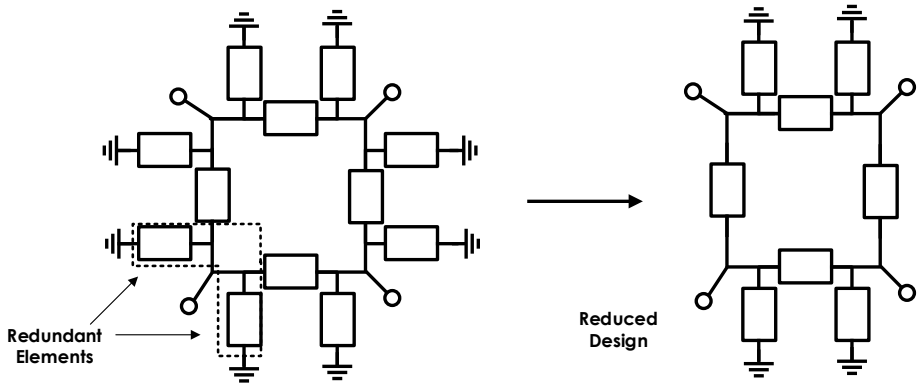


Figure 5.4: Branchline coupler based on lumped $\lambda/4$ networks and it's reduced equivalent circuit

The implementation can use either series inductors and parallel capacitors, or series capacitors and parallel inductors. As in the LNA matching network design, the quality factor of components plays into the overall gain performance when used as either series or parallel elements. For complex networks like these, the choice is best determined through simulations. However, one disadvantage of using the inductor as a parallel element is the possibility of coupling low frequency noise from the ground into the system. Considering the use of inductors are used as series elements, two possible configurations are shown in Figure 5.5a(type 1) and 5.5b (type 2). The s-parameter, gain imbalance and phase error performance of the type 1 and type 2 coupler are compared in Figure 5.5c-5.5h.

Type 1 uses 4 series inductors and 4 parallel capacitors. The component values derived from the quarter-wave elements (Appendix E) are computed as:

$$L_1 = \frac{Z_0}{\omega_0\sqrt{2}} \qquad L_2 = \frac{Z_0}{\omega_0} \qquad C_1 = \frac{\sqrt{2}+1}{Z_0\omega_0} \tag{5.2}$$

This coupler shows superior performance in both gain imbalance and phase error with bandwidth. The isolation and return loss have slightly narrower bandwidth compared to type 2. Type 2 uses two inductors and three capacitors. The component values are given as:

$$L_1 = \frac{Z_0}{\omega_0\sqrt{2}} \qquad C_1 = \frac{\sqrt{2}-1}{Z_0\omega_0} \qquad C_2 = \frac{1}{Z_0\omega_0} \tag{5.3}$$

The shunt capacitor has a value, $C_1 = \frac{\sqrt{2}-1}{\omega_0 Z_0}$, which is 6 time smaller than the Type 1 shunt capacitor. This type has very poor bandwidth performance in terms of gain imbalance, higher phase error, but maintains superior return loss over a wide bandwidth.

20GHz Branch Line Coupler Simulation in CMOS 65nm

The poor bandwidth performance of the type-2 hybrid makes it unsuitable in this application for circular polarisation . Type-1 is thus a preferred choice despite the larger footprint and added minor due to the extra 2 inductors. The calculated values are $L_1 = 281\,pH$, $L_2 = 398\,pH$ and $C = 384\,fF$. The branchline coupler schematic is shown in Figure 5.6a. The inductors use 1.5 turns for layout convenience and are optimized to maximize the quality factor. The values of the capacitors are changed to $400\,fF$ to correct the center frequency and bandwidth. The coupler was also designed on 130nm CMOS for the same frequency and bandwidth. The layout is shown in Figure 5.6b and occupies a $350\times500\,\mu m^2$ area.

The hybrid coupler simulation shows $< 1\,dB$ gain imbalance and $< 2^\circ$ phase error between $19\,GHz$ and $21\,GHz$.

5.3 High Isolation SPDT RF Switch

5.3.1 High Frequency CMOS Switches

In conjunction with the hybrid coupler, a single-pole double-throw (SPDT) switch is required to change the hand of polarisation. However, unlike power dividers, the hybrid coupler's ports are not isolated and requires *all 4 ports to be impedance matched*. This implies that the through and isolated port of the switched are simultaneously matched to 50Ω. Consider the hybrid/switch implementation illustrated in Figure 5.7, where port 1 of the switch is connected and Port 2 is isolated. The important metrics in the switch design are:

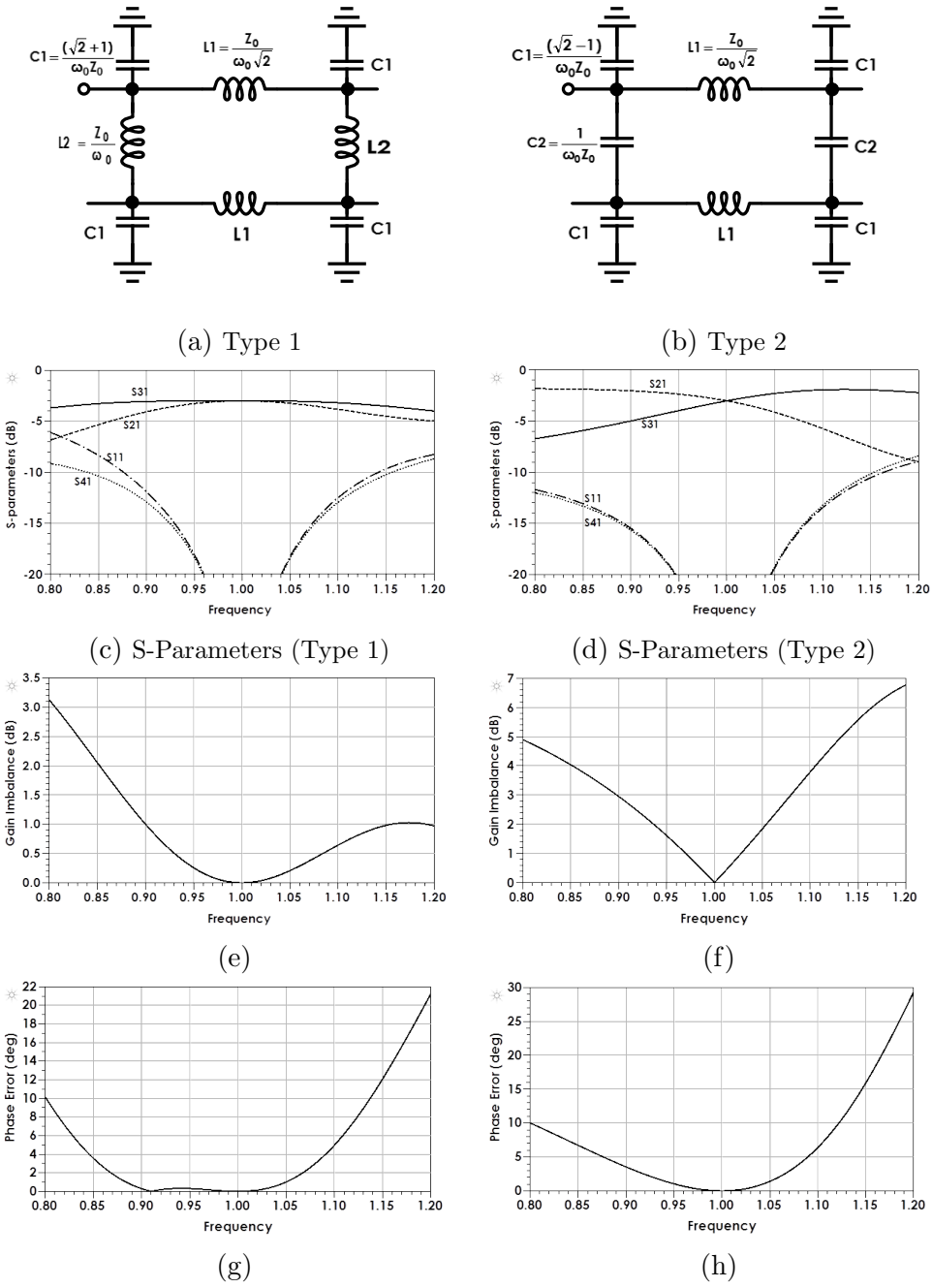
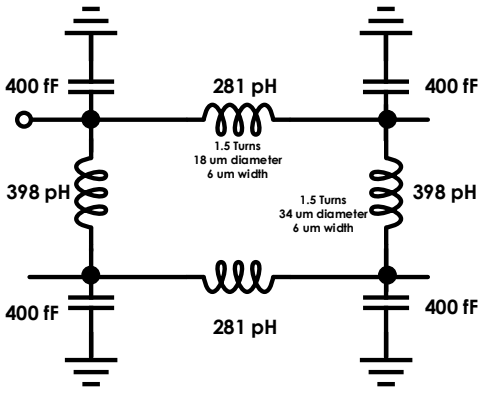
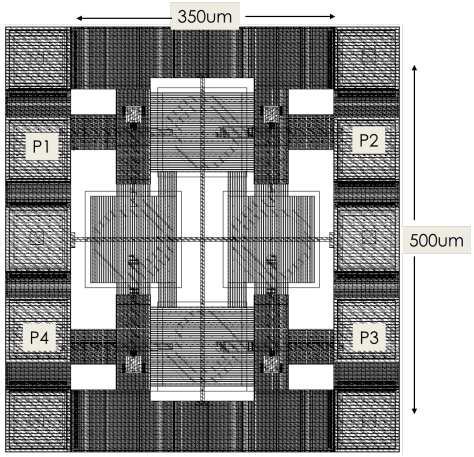


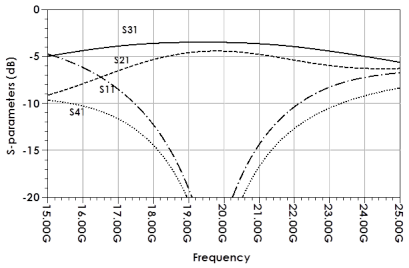
Figure 5.5: Type 1 and 2 gain and phase response on a normalised frequency axis



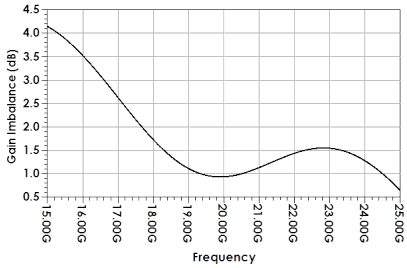
(a) Schematic



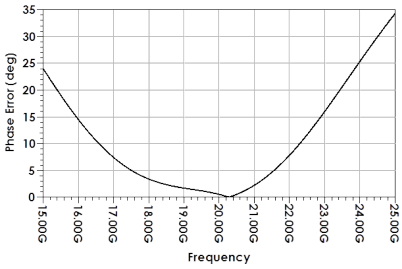
(b) Layout (130nm CMOS process)



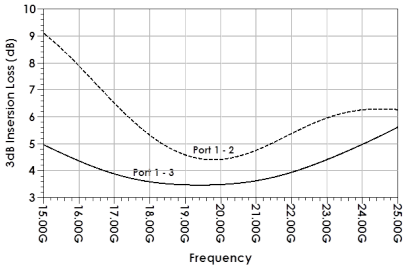
(c) Gain and Isolation



(d) Gain imbalance



(e) Phase Error



(f) Insersion loss

Figure 5.6: $20\,GHz$ hybrid coupler simulated performance on 65nm CMOS

1. Low insertion loss (S_{31})
2. High isolation ($-|S_{12}(dB)|$)
3. High input return loss($-|S_{11}(dB)|$)
4. High output return loss($-|S_{33}(dB)|$)
5. High isolated return loss($-|S_{22}(dB)|$)

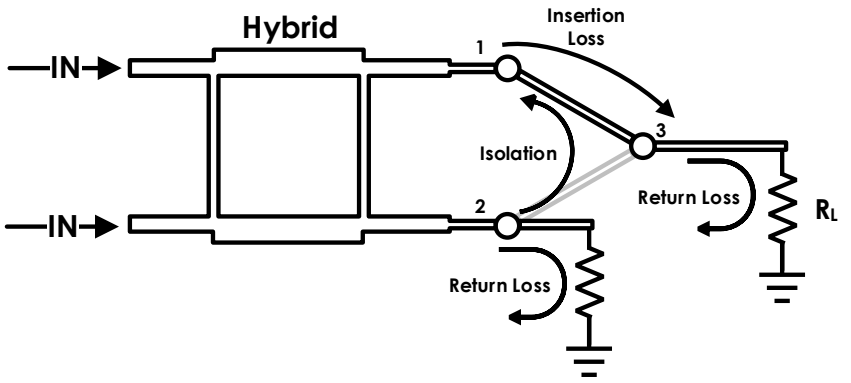
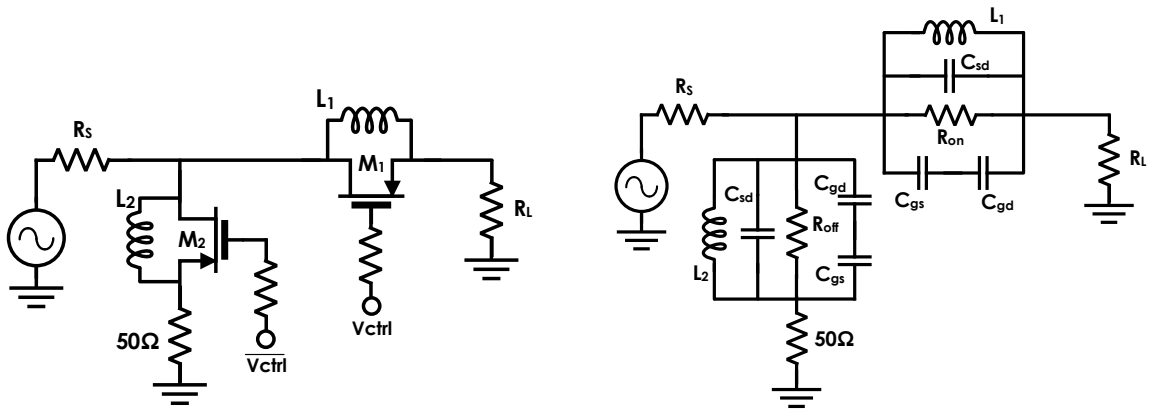


Figure 5.7: Illustration of the switch requirements

A high frequency (tuned) switch is shown in Figure 5.8a[22]. Large resistors are placed at the gate of the pass transistors to prevent the gate-to-source/drain capacitance from shunting to the ground as shown in the small signal model (Figure 5.8b). Inductors L_1 and L_2 are placed in parallel to resonate with the capacitance of the switches(in their *off* state) at the desired frequency given by:

$$L = \frac{1}{\omega_0^2 C_T} = \frac{1}{\omega_0^2 (C_{sd} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}})} \tag{5.4}$$

where C_T is the total source to drain capacitance. At the resonance frequency, when the transistor is *on*, the effect of the inductor and capacitor is negligible since it is in series with a small *on* resistance. But when the transistor is *off*, the inductor forms a resonant tank with the capacitor, creating a high impedance node and effectively isolating the input and output. The same applies to the shunt transistor. Increasing the width of the pass transistor will decrease the *on* resistance and decrease the inductance required for resonance (because C_T increases). Smaller inductance implies higher Q and smaller footprint. Since R_L loads the tank, ignoring the effect of R_{ON}, the bandwidth of the resonant switch is



(a) RF matched switch

(b) RF matched switch (small signal)

Figure 5.8: $20\,GHz$ Schematic RF Switch

estimated as:

$$F_{3dB} \approx \frac{1}{R_L C_T} = \omega_0^2 \frac{L}{R} \tag{5.5}$$

The minimum L (and maximum transistor size) is restricted by the bandwidth requirement. The 50Ω resistor placed across the shunt transistor provides impedance matching to the input when the switch is turned *off/isolated*.

5.3.2 20GHz Tuned SPDT Switch in 65nm-CMOS

Figure 5.9 is the schematic of the $20\,GHz$ switch designed in 65nm CMOS. All transistors have $180\mu m$ width and are of minimum length. The transistors are placed in isolated wells which is biased to ground with a high valued resistor to reduce body leakage. 3-turn inductors are used to tune the switch for isolation. The 50Ω resistors are implemented with large salicided p+ poly-silicon resistors, for low sheet resistance and to minimize mismatch.

The results of s-parameter simulations for the switch are shown in Figure 5.10a-5.10d. The simulations show $< 1.2\,dB$ insertion loss and $> 25\,dB$ isolation from $19-21\,GHz$. All three ports have $> 20\,dB$ return loss.

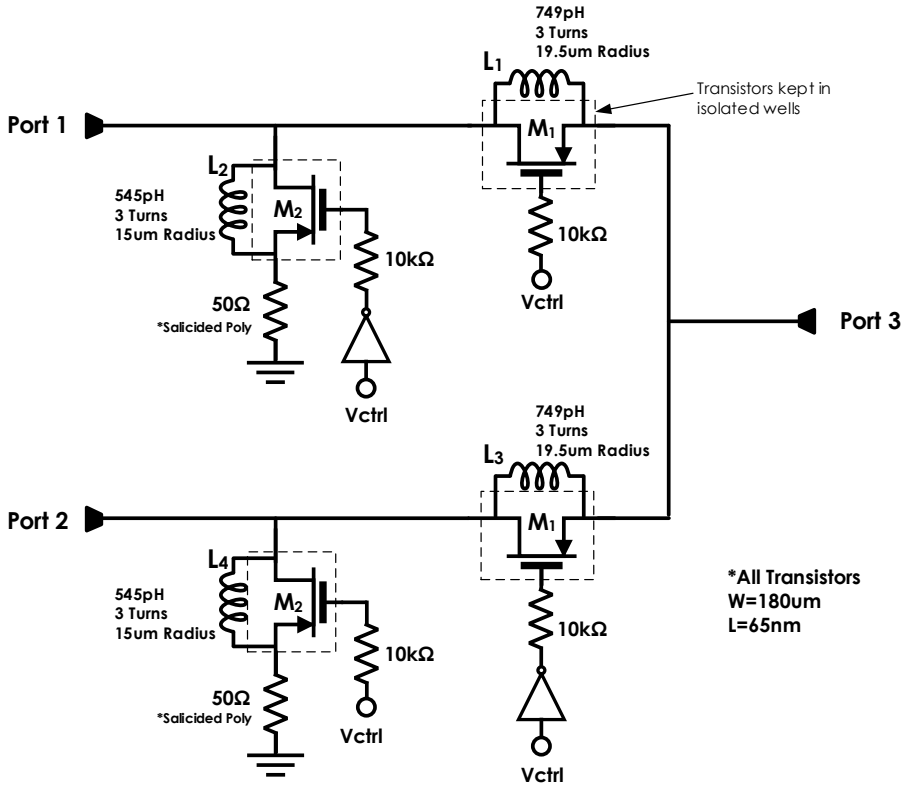
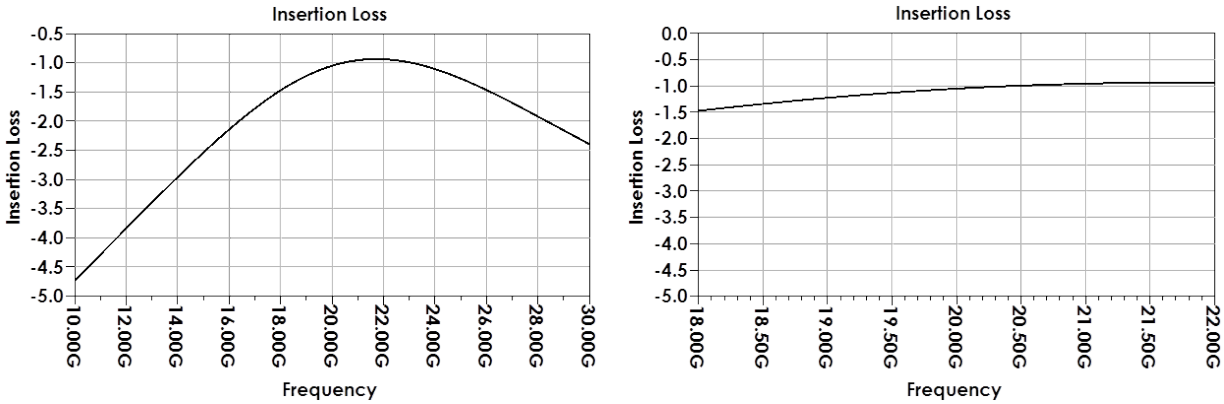


Figure 5.9: $20\,GHz$ RF switch schematic in 65nm CMOS

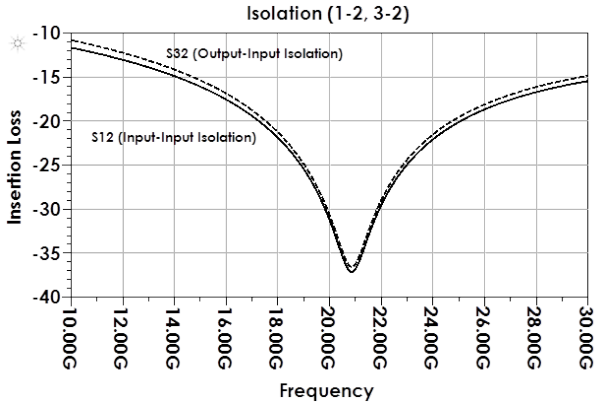
5.4 Low Voltage (1.2V) Bandgap Reference

A voltage reference is required to generate the bias necessary to establish the operating points of the circuits. The ideal bandgap reference can generate a fixed voltage/current reference insensitive to process, voltage and temperature (PVT) of the environment. A temperature independent reference is designed by combining the bias voltage/current of a *Proportional To Absolute Temperature Reference* (PTAT) with a *Complementary To Absolute Temperature Reference* (CTAT)[18].

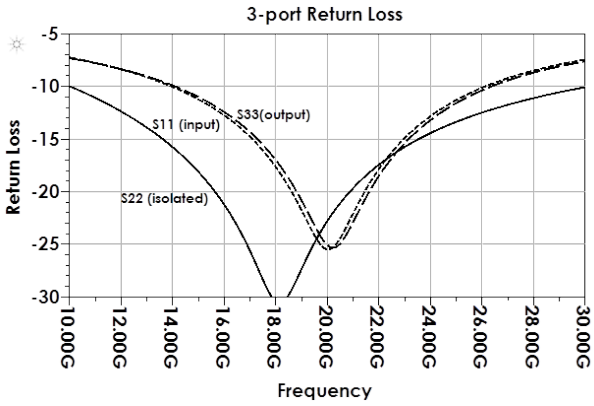


(a) Insertion Loss

(b) Insertion Loss $(18 - 22GHz)$



(c) Port 2-1/3-2 Isolation



(d) 3-port Return Loss

Figure 5.10: S-parameter analysis of the $20\,GHz$ tuned switch

5.4.1 Current Mode Bandgap Reference in CMOS

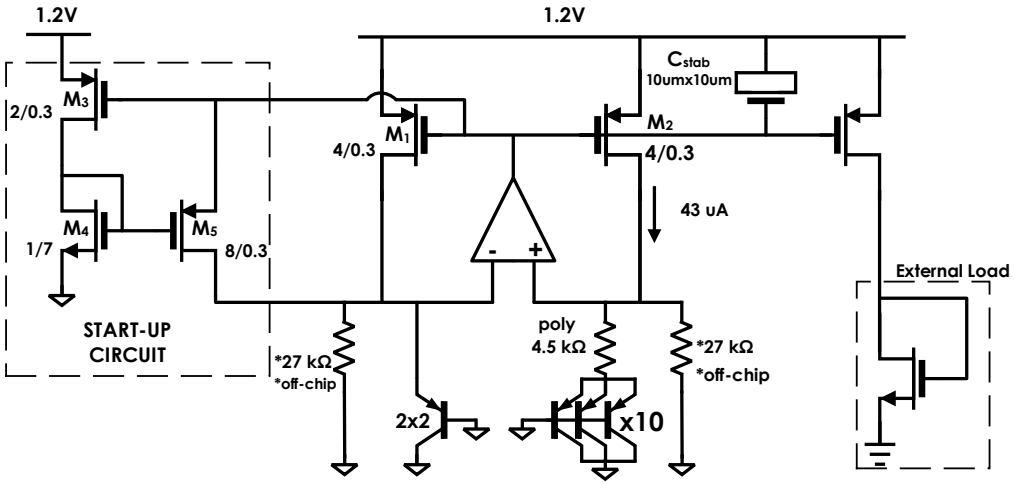
The standard voltage-mode bandgap reference generate an output voltage of $1.2V$[18] (bandgap voltage of silicon) to operate in CMOS technologies, which is equal to the technology limit in a 65nm process. It is however possible to synthesize a bandgap reference with lower voltage using current-mode operation[54, 55]. The total bias current generated at the output is the sum of a PTAT and CTAT reference[54]:

$$\begin{aligned} I_T &= I_{PTAT} + I_{CTAT} \\ &= \frac{1}{LR} V_{BE,1} + \frac{ln(K)}{R} V_T \end{aligned} \tag{5.6}$$

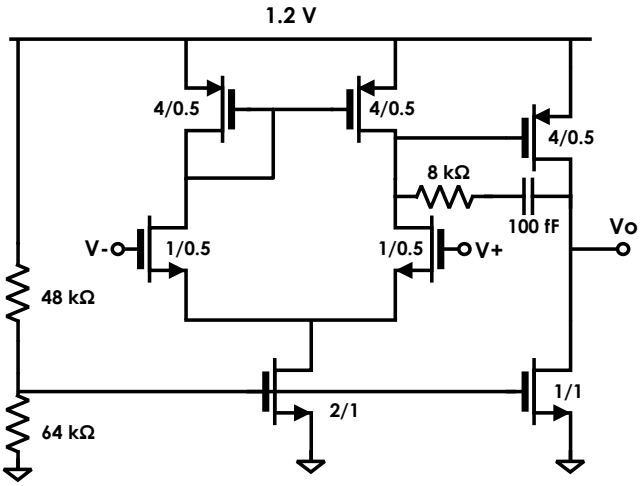
where R and K are chosen for zero temperature coefficient at T_0:

$$\left.\frac{dI_T}{dT}\right|_{T=T_0} = \frac{1}{LR} \left.\frac{dV_{BE,1}}{dT}\right|_{T=T_0} + \frac{ln(K)}{R} \left.\frac{dV_T}{dT}\right|_{T=T_0} = 0 \tag{5.7}$$

The schematic of the $1.2\,V$ bandgap reference is shown in Figure 5.11. It is designed to provide zero temperature coefficient at $40°C$. The required coefficients are $K = 10$ and $L = 6$. The circuit generates a nominal $43\,\mu A$ bias current. The $27\,K\Omega$ CTAT resistors need to have very low temperature coefficient and may require off-chip implementation.
The start-up circuit (M_3-M_5) uses the M_5 PMOS transistor to force a current through the resistor/BJT network. M_4 has a large $V_{GS,(on)}$ which turns off the M_5 transistor during normal operation. The Operational amplifier uses a simple two-stage self-biased topology. It uses $20\,uA$ of current and generates $60\,dB$ DC voltage gain.
The reference operates down to $1\,V$ (Figure 5.12a) and shows <0.1% variation up to $1.4\,V$.

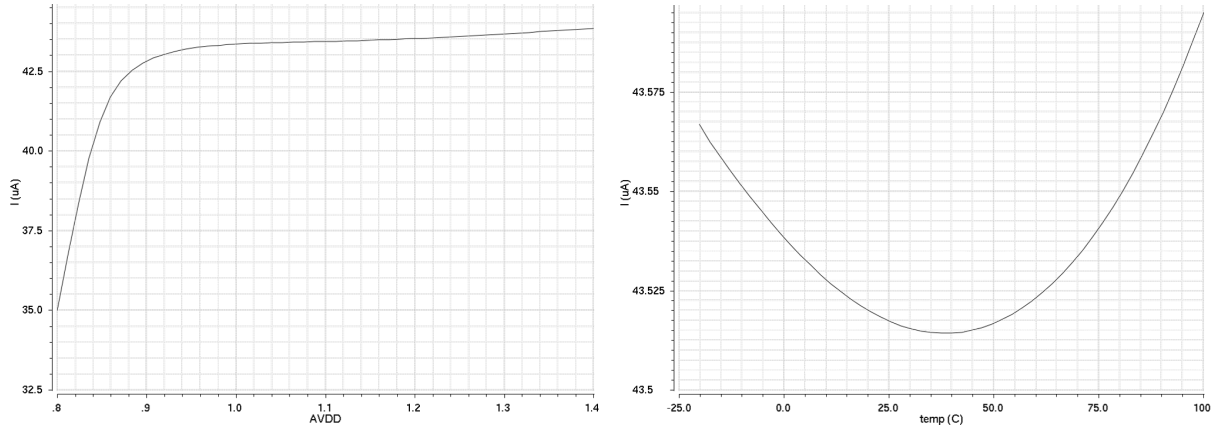


(a) Bandgap Reference



(b) Self-Biased Op-Amp

Figure 5.11: 1.2 V Bandgap reference circuit with self-biased Op-Amp



(a) I_{bias} vs supply voltage

(b) I_{bias} vs temperature

Figure 5.12: Bias current vs voltage and temperature

5.5 Single Channel Simulation and Performance

The frequency response, mismatch and phase variation of each component will affect the performance of the full receiver. To validate the receiver performance, the designed components need to be simulated and analysed as a complete system. The important metrics in the single-channel phased array receiver are:

1. Gain
2. Cross polarisation
3. Noise Figure
4. Phase variation
5. Gain variation
6. Phase and gain Error
7. Input/Output return loss

5.5.1 Gain, Cross Polarisation

As mentioned at the start of this section, the hybrid coupler and switch are required to generate circularly polarised radiation patterns. From reciprocity principle, the same applies to antennas in receiving mode (Figure 5.13). Consider a right-handed circularly

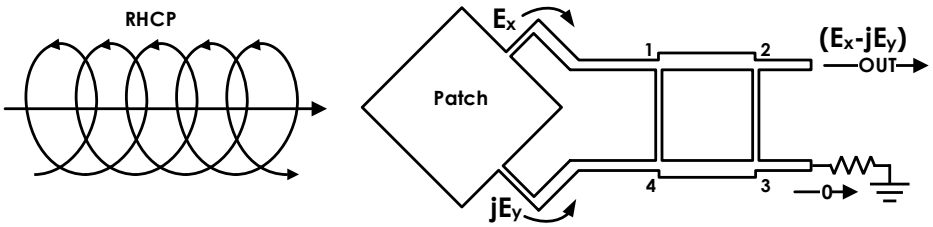


Figure 5.13: Dual-fed antenna (receiving mode)

polarised incident wave:

$$\mathbf{E_i} = \frac{(\hat{\mathbf{a}}_x + j\hat{\mathbf{a}}_y)}{\sqrt{2}} E_i \tag{5.8}$$

Assuming all ports of the coupler are perfectly matched and the receiver is configured to receive right handed circularly polarised signals, from (5.1), the voltage at Port 2 of the coupler is given as:

$$\begin{aligned} V_2 &= S_{21}V_1^+ + S_{31}V_4^+ \\ &= -j\frac{1}{\sqrt{2}}(V_1^+ - jV_4^+) \end{aligned} \tag{5.9}$$

The circularly polarised antenna, connected to ports 1 and 4, will receive two orthogonal signals such that:

$$\begin{aligned} V_1 &= \frac{\hat{\mathbf{a}}_x}{\sqrt{2}} E_i \cdot \hat{\mathbf{a}}_x l_e = E_i l_e \\ V_4 &= j\frac{\hat{\mathbf{a}}_y}{\sqrt{2}} E_i \cdot \hat{\mathbf{a}}_y l_e = jE_i l_e \end{aligned} \tag{5.10}$$

l_e is the *vector effective length* of the patch antenna at the orthogonal mode. Using (5.9) and (5.10), the output at port 2 is:

$$\begin{aligned} V_2 &= -j\frac{1}{2}(E_i l_e - j(jE_i l_e)) \\ &= -j(E_i \cdot l_e) \end{aligned} \tag{5.11}$$

If the same analysis is repeated at port 3:

$$\begin{aligned} V_3 &= -1\frac{1}{2}(E_i l_e + j(jE_i l_e)) \\ &= 0 \end{aligned} \tag{5.12}$$

Thus, with ideal components, no signal power is lost to port 3 and the polarisation loss ratio (PLR) will be $0\,dB$. However, for the receiver in consideration, various factors will affect the polarisation purity, mainly:

- Coupler Phase Error
- Coupler Gain Error
- Switch Isolation
- LNA/VGA Mismatch at Coupler and Switch Ports

It is possible to decompose the received signal into two orthogonal vectors. The signal vector received from the desired polarisation content is known as the *co-polarisation*(co-pol), while the orthogonal unwanted signal is the *cross-polarisation*(cross-pol) [6]. To verify the receiver's polarisation performance, the simulation test environment illustrated in Figure 5.14 uses an ideal quadrature coupler to generate two outputs 90° apart to represent an ideal circularly polarised signal. The receiver is configured for a particular hand of polarisation.

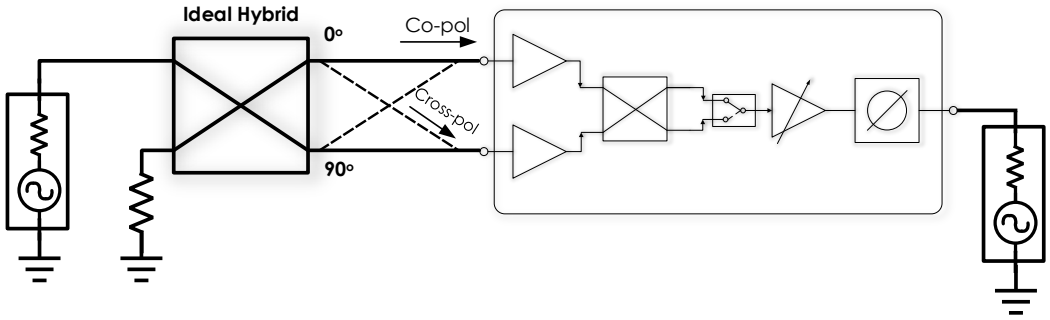


Figure 5.14: Co-polaristion and cross-polarisation gain simulation

The simulation is run with the coupler connected to the two LNA inputs to generate a right-hand polarised signal for the co-pol simulation. The leads are then switched to generate a left-hand polarised signal for the cross-pol simulation. The overall gain from each test will represent the co-pol gain and cross-pol gain respectively. The *cross-polarisation*

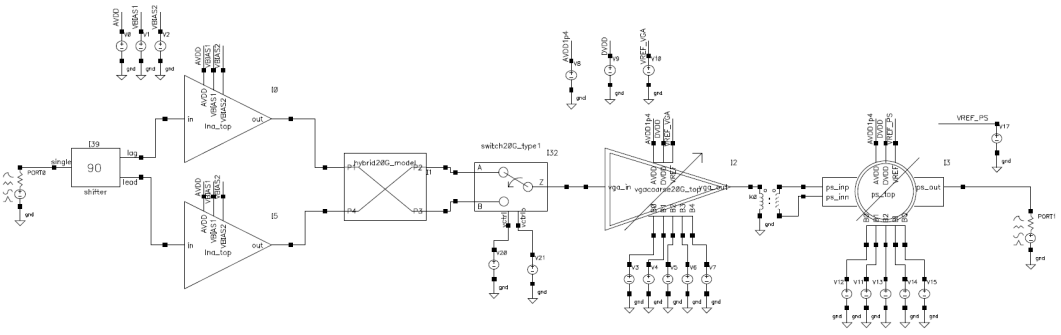


Figure 5.15: System analysis in Cadence® design environment

discrimination is defined as:

$$XPD(dB) = G_{co-pol}(dB) - G_{x-pol}(dB) \tag{5.13}$$

and is related to the axial ratio as:

$$XPD(dB) = 20log\left(\frac{AR+1}{AR-1}\right) \tag{5.14}$$

From Figure 5.16, the receiver shows $37\,dB$ gain for the co-pol and $12\,dB$ gain for cross-pol which is equal to $25\,dB$ cross-polarisation discrimination or $1\,dB$ axial ratio.

5.5.2 Gain, Noise Figure and Phase Error with Variable Gain Settings

The simulated system response to different VGA settings are shown in Figures 5.17. The receiver shows $10.5\,dB$ of gain variation for the 32 states and $< 5°$ of error from $19\,GHz$ to $21\,GHz$. The overall noise figure at the highest gain settings is $2.55\,dB$ and increases to only $2.62\,dB$ at the lowest gain settings. This shows that the effect of losses (and tapering) has been minimized due the low noise amplifier gain. The variable gain amplifier however, shows a large phase error when the second stage ($5\,dB$) is switched. This phase error is most likely due to the mismatch with the phase shifter input impedance. Thus, the VGA may require a buffer stage to mitigate this phase error.

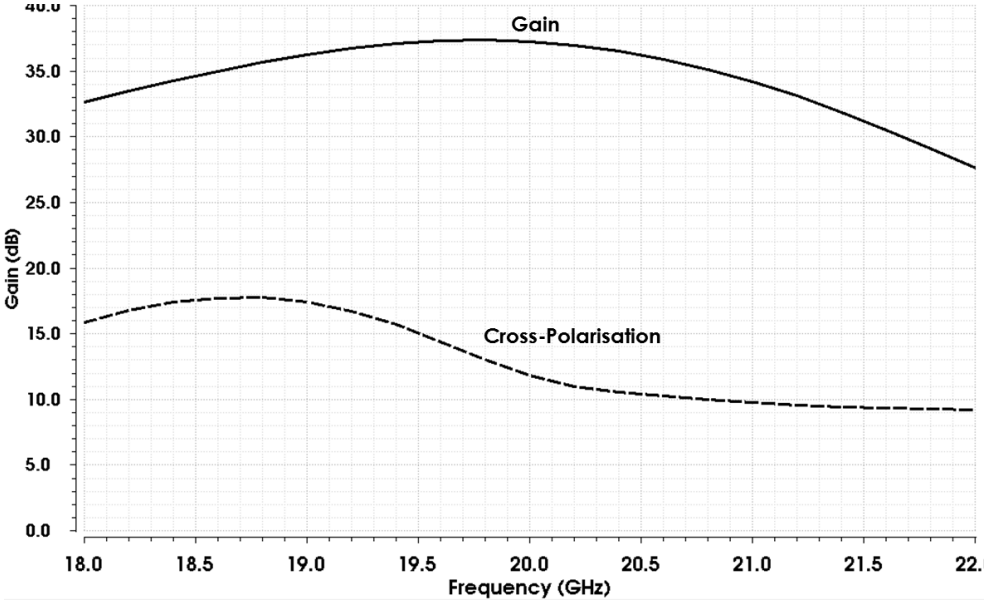


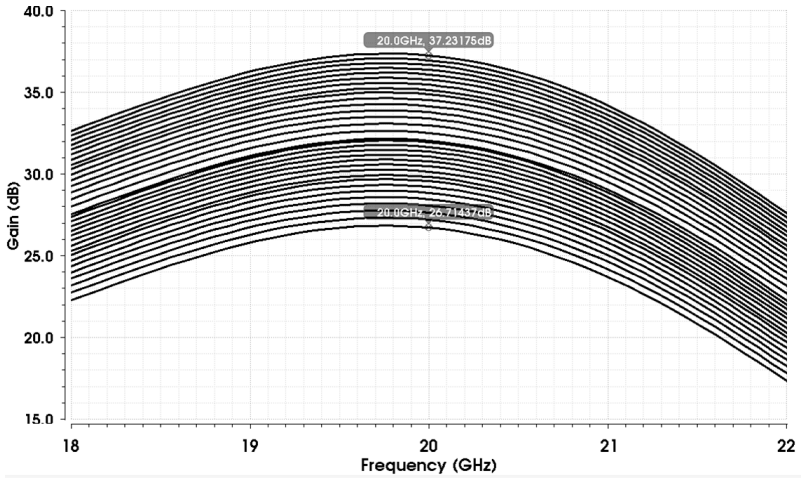
Figure 5.16: Co-polarisation and cross-polarisation gain

5.5.3 Gain, Phase Variation with Phase Shifter Settings

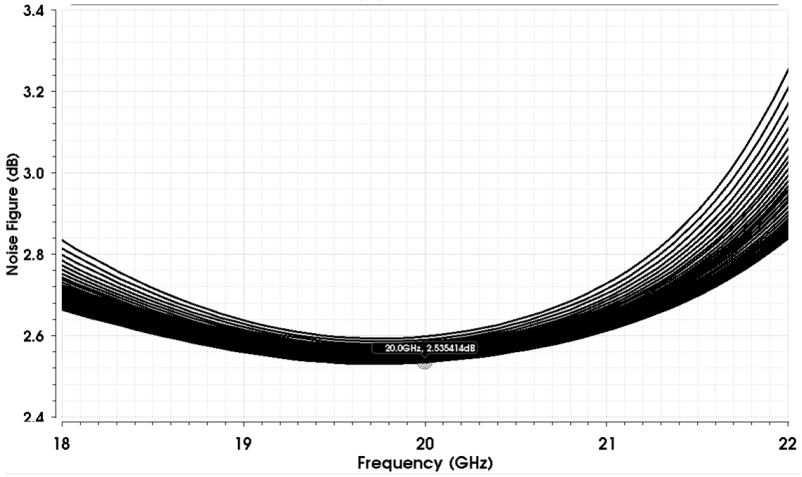
The simulated system response to different phase shifter settings are shown in Figures 5.17. There is $2.5\,dB$ gain variation with the 32 phase shifter settings which is a $0.5\,dB$ increase from the standalone measurement. This is also a possible effect of mismatch, and will require further study prior to the balun design.

5.6 Summary and Conclusion

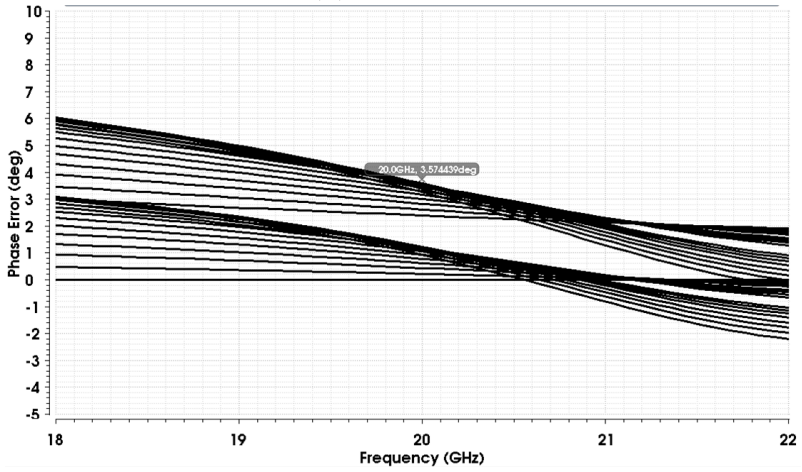
A single channel receiver was simulated in the Cadence® design environment. The receiver chain has two low noise amplifiers connected to a hybrid coupler and switch to generate a circularly polarised radiation pattern with two hands of polarisation. A 5-bit variable gain amplifier following the switch provides tapering to the array pattern and the 5-bit phase shifter enables beam-steering. The simulated receiver gain was $37\,dB$ with $< 2\,dB$ variation with phase within a $2\,GHz$ bandwidth. The hybrid coupler and switch enabled $27\,dB$ of cross-pol discrimination. The VGAs has a $10\,dB$ dynamic range and 5-bit resolution. An overall noise figure of $2.5\,dB$ was simulated at the highest gain setting and $2.7\,dB$ at the lowest gain setting. The phase shifter achieved full 360° digital phase variation with $< 5.5°$



(a) Gain

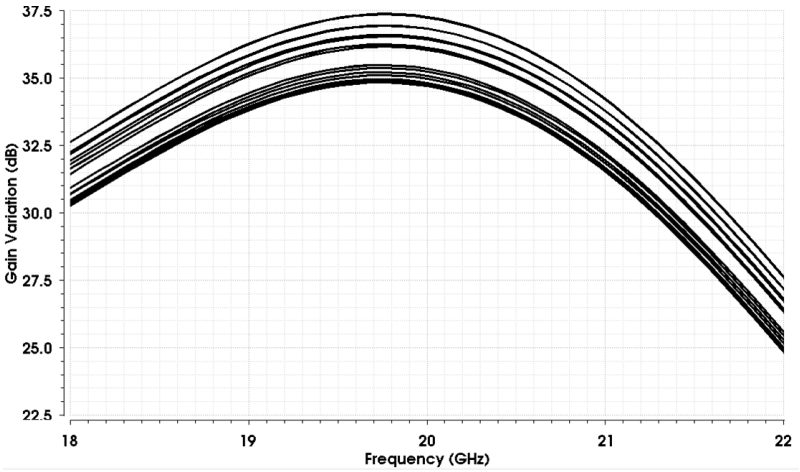


(b) Noise figure

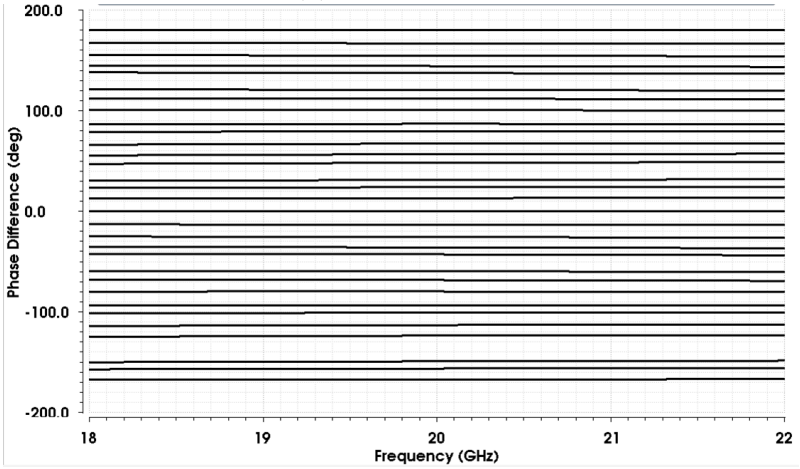


(c) Noise figure

Figure 5.17: Gain, noise figure and phase variation with 32 gain states



(a) Gain variation



(b) Relative phase shift

Figure 5.18: Gain and phase variation with 32 phase states

rms phase error, $< 2\,dB$ gain error with 5-Bit resolution.

The results are summarised in Table 5.1

Table 5.1: Summary of system simulation and performance

Parameters		**Results**
Design Summary	Technology	65nm CMOS
	Stages	2
	Voltage	$1.2\,V$(LNA), $1.4\,V$(VGA & PS)
	Power Consumption	$23.8\,mW$
Small-Signal	Center Frequency	$20\,GHz$
	Frequency Range	$19-21\,GHz$
	Gain (Co-pol)	$37\,dB$
	Cross-Pol Discrimination	$25\,dB$
	Axial Ratio	$1\,dB$
	Input Return Loss	$>10\,dB$
	Output Return Loss	$>15\,dB$
	Noise Figure	$2.5\,dB-2.7\,dB$
	Phase Resolution	5 bit
	RMS Phase Error (Phase Shifter)	$<5.5^{\circ}$
	Gain Resolution	5-Bit
	Dynamic Range	$10\,dB$
	Phase Error (Gain Variation)	$<5^{\circ}$
Large Signal	Input $P-1dB$	$-29\,dBm$

Chapter 6

Conclusion

6.1 Summary and Conclusion

The design of phased-array active antennas involves an intricate translation of antenna specifications to circuit requirements. Active antennas for satellite applications require 100s to 1000s of transmitter/receiver modules with independent phase shifting and tapering capabilities. Cost and power consumption are critical as a result of the large component count. This thesis demonstrated integrated circuit design principles that translate system level parameters and specifications to silicon level design. The thesis covered critical circuit blocks in a $20\,GHz$ receiver module which include a low-noise amplifier, phase shifter, variable-gain amplifier, hybrid coupler, switch and bandgap reference with a consistent focus on meeting the system level specification. All designs, simulations and fabricated samples were done on TSMC-65nm CMOS technology.

The two-stage low noise amplifiers designed showed a peak gain of $29\,dB$ and more than 10% bandwidth. Close agreement between simulation and measurement demonstrated the accuracy of the EM-simulated interconnects. The amplifier showed a simulated noise figure of $2.6\,dB$ and required only $7\,mW$ of power at $1.2\,V$ bias. The phase shifter was also designed and fabricated. It operates on the principle of vector modulation and uses current-DACs for digital control. A 5-bit digital control mechanism was developed which enables true 5-bit digital control. The measured device showed $2\,dB$ gain variation, $< 5.5^{\circ}$ rms phase error and requires $5.6\,mW$ of power. A digital control variable gain amplifier design was also demonstrated which uses an active load to achieve low phase error and wide band resistive matching. The digital VGA operates on the current steering principle

and implements switched transistors for digital gain control. It achieves $10\,dB$ dynamic range with a digital 5-bit resolution.

The hybrid coupler and switch were designed and simulated at the schematic level to implement right/left-hand circular polarisation. The simulation of the hybrid coupler showed $< 1.2\,dB$ gain imbalance between the output ports and $< 2^\circ$ phase error between $19\,GHz$ and $21\,GHz$. The switch simulation results also show $< 1.2\,dB$ insertion loss and $> 25\,dB$ port-port isolation between $19\,GHz$ and $21\,GHz$. A bandgap reference circuit design was finally investigated which can produce a temperature independent reference current with as low as $1\,V$ bias.

The single channel receiver module was finally simulated to study the single channel performance. An overall peak gain of $37\,dB$ was simulated with $25\,dB$ cross-pol discrimination, which would produce a radiation pattern with $1\,dB$ axial ratio if used with an ideal antenna. The lowest overall noise figure was $2.5\,dB$ which is less than the single-ended since two LNAs are combined in quadrature. The receiver has a gain variable from $27\,dB$ to $37\,dB$, with a 360° variable phase shift, both with 5-bit digital control.

Critical specifications were derived from the system-level requirements. This ensures that the individual components can be optimally designed to meet the system specifications.

6.2 Summary of Future Work

6.2.1 Complete Receiver MMIC

While major the receiver components were investigated, only the LNA and phase shifter have been fabricated. The future development of the phase array receiver will involve:

- Fabrication and testing of the variable-gain amplifier
- Layout, fabrication and testing of the hybrid coupler, switch and bandgap reference circuit
- Design, layout and fabrication of the complete single-channel receiver module.

The reciever MMIC is a single channel on-chip and will connect to multiple dual-fed circularly polarised antennas. The block diagram of the proposed receiver MMIC is shown in Figure 6.1.

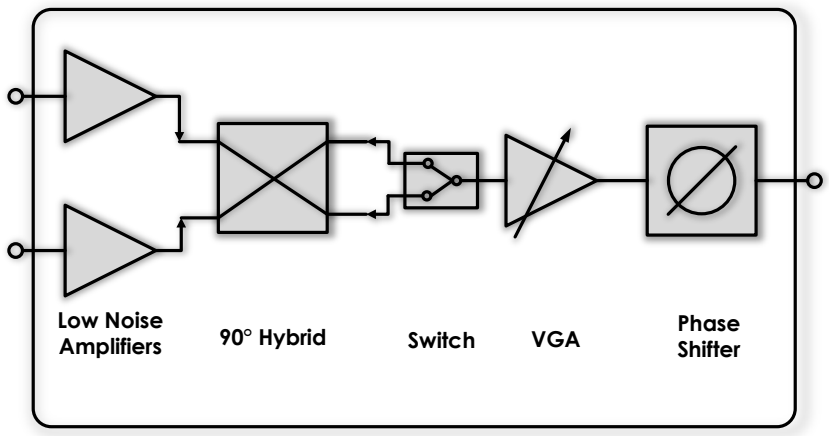


Figure 6.1: Receiver MMIC block diagram

6.2.2 Complete Transmitter MMIC

In conjunction with the receiver development, the transmitter is still under research and development. Required transmitter components are the:

- Power amplifier
- Driver
- Analog phase shifter
- Digital control variable-gain amplifier

The transmitter MMIC is a four-channel transmitter chain with independent analog phase shifters and gain control. Figure 6.2 illustrates the proposed four channel transmitter MMIC.

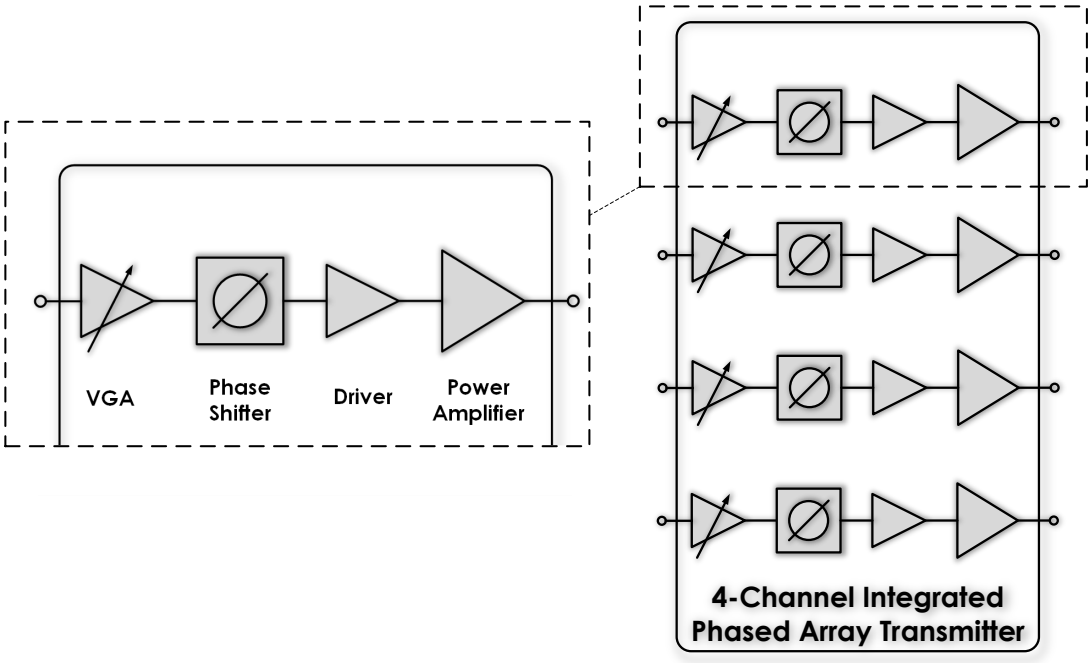


Figure 6.2: Transmitter MMIC block diagram

6.2.3 Antenna Module

The antenna module is a subarray antenna which will form part of a modular phased array antenna. The antenna will consist of a number of antenna modules connected together

by a feed network. The antenna modules incorporate the receiver/transmitter MMICs connected to patch antennas. A single module may have 4×4, 8×8 or 16×16 depending on the number of antennas required and the complexity of the feed-network. The antenna module is illustrated in Figure 6.3.

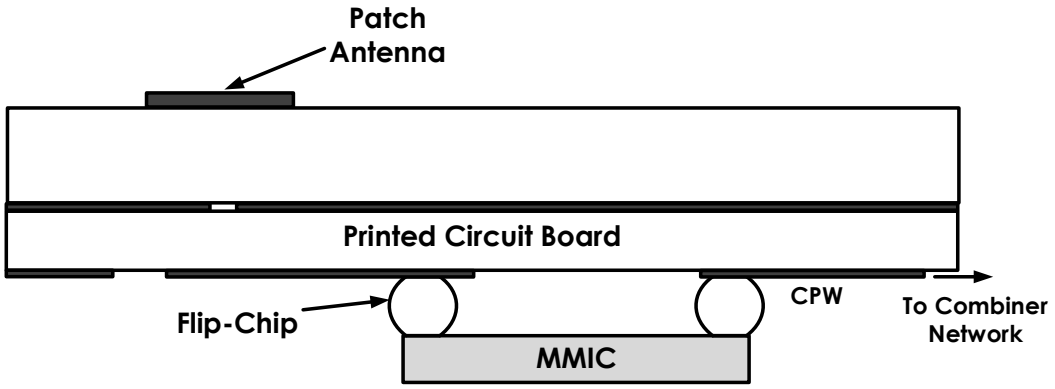


Figure 6.3: Single array module

APPENDICES

Appendix A

Noise and Power Specifications

A.0.4 Power Specification

Figure A.1 is a model for the satellite uplink. The transmitter/amplifier is usually com-

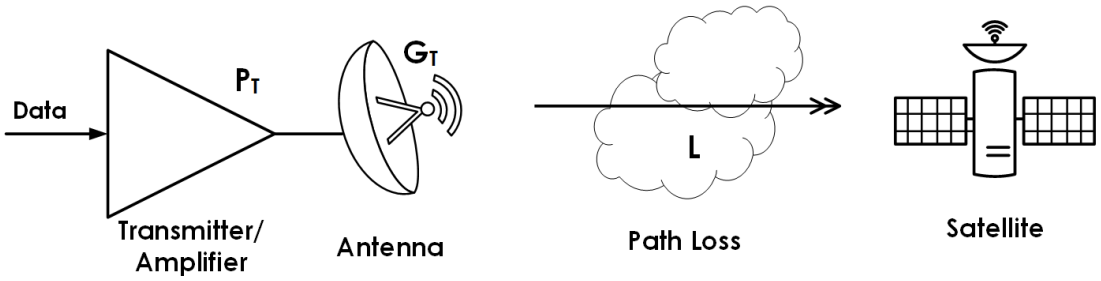


Figure A.1: Satellite Uplink Model

posed of a number of subcomponents such as modulators, mixers, oscillators and power amplifiers. For uplink budget analysis, it is modelled as a single signal amplifier. The power amplifier (usually the last component or placed before a filter), is designed to output the signal at a given output power level, P_T.
If the antenna is assumed to radiate the power radially in all directions (an isotropic radiator), then the power flux density is defined as the incident power per unit area at a distance, d, from the antenna surface, given as:

$$W_0 = \frac{P_T}{4\pi d^2} W/m^2 \tag{A.1}$$

Actual antennas are not isotropic, but radiate the same amount of power over a smaller area. Since the integrated power must remain the same, the transmitting antenna power flux density is higher and is given as:

$$W_t = \frac{P_T G_T}{4\pi d^2} W/m^2 \tag{A.2}$$

G_T is referred to as the Antenna Gain. It is a measure of the increased power density compared to an isotropic radiator. In the above calculation, the antenna gain is assumed to be constant over it's solid angle, but in reality, it is a function of the elevation and azimuth angle, described using the Gain function, $G(\theta, \phi)$.
The product of the output power and antenna gain is the effective isotropic radiated power:

$$EIRP = P_T \times G_T \tag{A.3}$$

It is the equivalent input power an isotropic antenna would need to achieve the same power density as the actual antenna with a gain, G_T. The flux density is the power radiated per unit area, expressed as:

$$W_t = \frac{EIRP}{4\pi d^2} W/m^2 \tag{A.4}$$

The receiving antenna of the satellite has an equivalent effective area or antenna aperture, A_{eff}. In antenna theory, the receiving mode aperture area, A_{eff} can be related to the antenna gain, G_R by the equation:

$$A_{eff} = \frac{\lambda^2}{4\pi} G_R \tag{A.5}$$

Given the flux density, the total received power at the satellite is written as:

$$P_R = W_t A_{eff} \tag{A.6}$$

Substituting Equation (A.4), (A.5) in (A.6), the received power at the satellite is:

$$P_R = G_R G_T P_T \left(\frac{\lambda}{4\pi d}\right)^2 \tag{A.7}$$

The last term in the (A.7), when inverted, is called the free-space path loss:

$$L_f = \left(\frac{4\pi d}{\lambda}\right)^2 \tag{A.8}$$

and it represents the power loss of the received signal solely due to the spherical wave nature of the transmitted signal in free-space. Other sources of path loss (rain fading, multipath,etc.) are added to the free-space path loss to give the path loss. It is common to represent the received power in *decibel Watts* (dBW):

$$P_R[dBW] = G_R[dB] + EIRP[dBW] - 20log_{10}\left(\frac{4\pi d}{\lambda}\right) \tag{A.9}$$

A.0.5 Noise Specification

Any signal propagating through a channel with a physical temperature, T_p, will be corrupted by thermal noise generated by random motions of charges in a medium. At radio frequency, thermal noise has a flat power spectral density, kTW/Hz, so the total noise power over a bandwidth, B, is given as:

$$P_N = kTB \ Watts \tag{A.10}$$

k, is Boltzmann's constant, $1.38 \times 10^{-23} \, J/K$, and T can either the physical temperature of the channel or an *equivalent Noise Temperature*. The equivalent noise temperature of a device is the physical temperature an equivalent resistor will require to generate the same noise power in (A.10) as the device. The downlink model in Figure A.2 illustrates important receiver components and their noise contributions. Antenna noise is associated with an

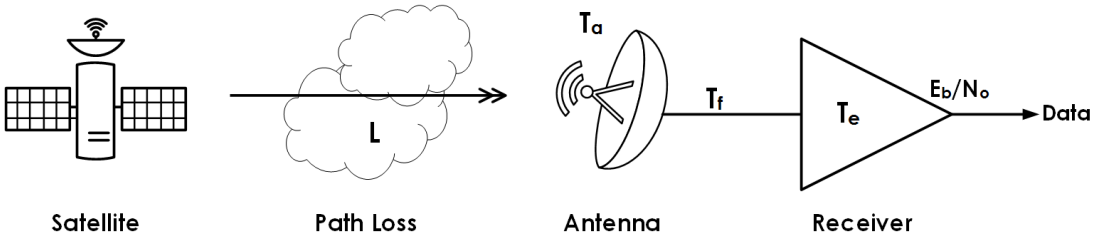


Figure A.2: Satellite Downlink Model

antenna temperature T_a, and characterizes the received signal noise from galactic and earth radiation in free space. The antenna is connected to a receiver by an antenna feed which has an equivalent temperature, T_f, due to transmission line loss ($\alpha \ Np/m$). The receiver is composed of a number of components (low noise amplifiers, mixers, modulators,...) and has an equivalent noise temperature, T_e, resulting from noise generated from passive losses, active components, and radiation.

It can be shown that the overall noise temperature or system noise temperature, in terms of noise temperature is equal to[3]:

$$T_s = \alpha T_a + (1 - \alpha) T_f + T_e \tag{A.11}$$

Using equation (A.10) and (A.11), the overall noise power at the output of the receiver is given as:

$$P_N = kT_sB \;\; W \tag{A.12}$$

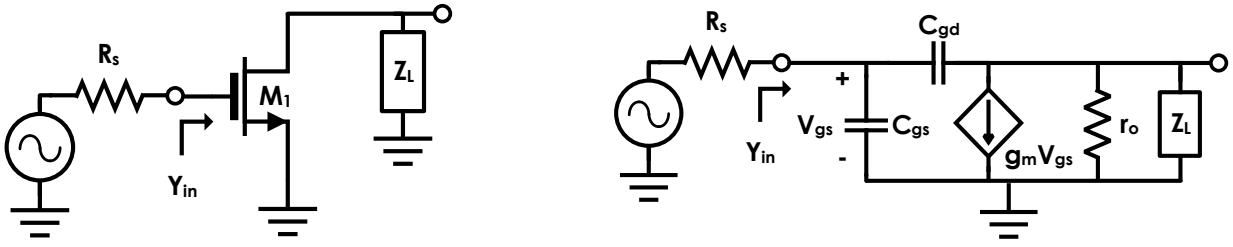
Appendix B

Common Source Amplifier Impedance

Consider the common-source amplifier in Figure B.1a, connected to an arbitrary load impedance, Z_L. The small signal equivalent circuit in Figure B.1b consists of a gate-source capacitance (C_{gs}) and gate-drain capacitance as dominant parasitic elements.

The input admittance is can be obtained by summing the admittances of the two current paths, i_{gs}, i_{ds}. The input admittance is given as:

$$Y_{in} = \omega C_{gd}(\omega C_{gd} R_L - X_L g_m) + j\omega C_{gs} + j\omega C_{gd}(1 + g_m R_L + \omega C_{gd} X_L) \tag{B.1}$$



(a) Schematic (b) Small Signal

Figure B.1: Common Source Amplifier

where $Z_L = R_L + jX_L$. Expressing (B.1) in terms of the Conductance:

$$\begin{aligned} G_{in} &= \omega^2 C_{gd}^2 R_L \left(1 - \frac{X_L}{R_L}\frac{g_m}{\omega C_{gd}}\right) \\ G_{in} &= \omega^2 C_{gd}^2 R_L \left(1 - Q_L \frac{g_m}{\omega C_{gd}}\right) \end{aligned} \tag{B.2}$$

and susceptance:

$$B_{in} = \omega C_{gs} + \omega C_{gd}(1 + g_m R_L + \omega C_{gd} X_L) \tag{B.3}$$

(B.2) shows that the input conductance becomes negative for loads that are predominantly inductive with high quality factor (Q_L). So how does this affect the common source amplifier? Consider the LNA configuration which uses the inductor, L_B, as a bias feed and drives a load, R'_L. Assuming $R_L = r_o || R'_L$:

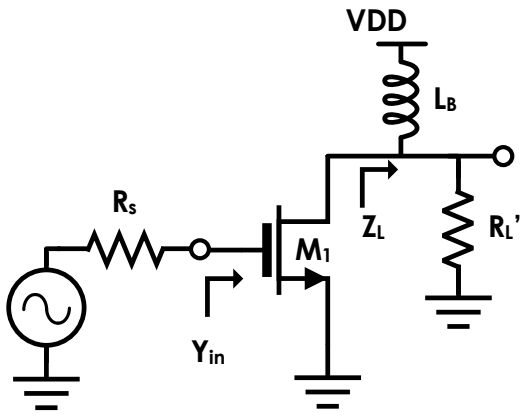


Figure B.2: Simple common-source LNA configuration

$$\begin{aligned} Z_L &= j\omega L_B || R_L \\ &= \frac{w^2 L_B R_L^2 + j\omega L_B R_L^2}{R^2 + \omega^2 L_B^2} \end{aligned} \tag{B.4}$$

Mapping the parallel load to series resistance and reactance; $R_L \rightarrow \frac{\omega^2 L_B^2 R_L}{R^2+\omega^2 L_B^2}$ and $X_L \rightarrow \frac{\omega L_B R^2}{R^2+\omega^2 L_B^2}$, the Quality Factor is obtained:

$$Q_L = \frac{X_L}{R_L} = \frac{R}{\omega L} \tag{B.5}$$

Substitute (B.5) into (B.2):

$$\begin{aligned} G_{in} &= \omega^2 C_{gd}^2 \frac{\omega^2 L_B^2 R_L}{R^2+\omega^2 L_B^2}\left(1 - \frac{R_L^2}{L_B}\frac{g_m}{\omega^2 C_{gd}}\right) \\ G_{in} &= C_{gd}^2 R_L \frac{\omega^2 L_B^2 R_L}{R^2+\omega^2 L_B^2}\left(\omega^2 - \frac{R_L^2}{L_B}\frac{g_m}{C_{gd}}\right) \end{aligned} \tag{B.6}$$

The scaling term outside the braces is positive for all frequencies, (B.6) reveals the stability problem with the common source configuration:

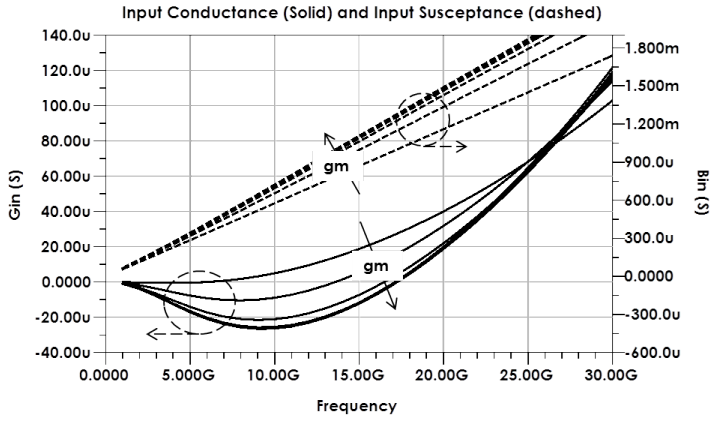
1. The amplifier becomes unstable (negative conductance) at frequencies below $\omega < \sqrt{\frac{R_L^2}{L_B}\omega_T}$.
2. Biasing at higher transconductance increases the frequency of instability.
3. Transistors with higher parasitic feedback (C_{gd}) are more stable.

Figure (B.3a) is a plot of the input and output conductance/susceptance for an $L_{bias} = 1\,nH$ and $R_L = 50\Omega$. As g_m increases the frequency of oscillation reaches $21\,GHz$. The output conductance and susceptance are also plotted in Figure B.3b which does not show negative impedance and has very wideband frequency response. The stability of the output can be understood by considering that the loopgain through the feedthrough capacitor, C_{gd}, is very small, so r_o *dominates.*

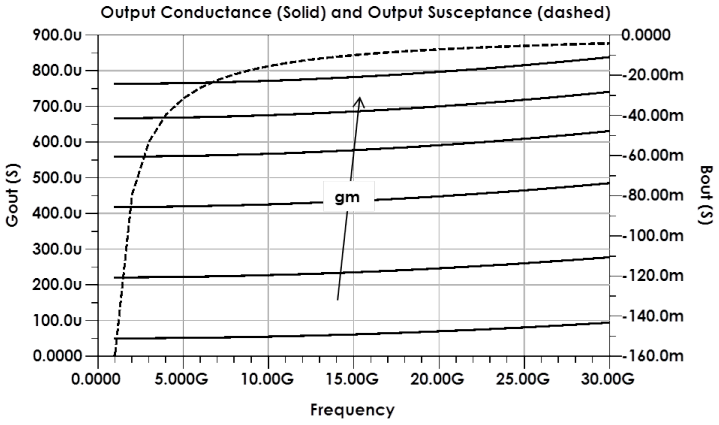
To conclude this stability study, we consider some ways to stabilize the common source configuration. Recall the expression for the input conductance, (B.2):

$$G_{in} = \omega^2 C_{gd}^2 R_L\left(1 - Q_L \frac{g_m}{\omega C_{gd}}\right) \tag{B.7}$$

It relates the frequency of instability to the series quality factor of the load (for inductive loads). More specifically, the device will oscillate for frequencies, $\omega < Q_L \frac{g_m}{C_{gd}}$. Without lowering the transconductance, one way to improve the stability may be to add a feedback capacitance, C_F(Figure B.4a . This will increase the effective gate to drain capacitor ($C_{gd} \rightarrow C_{gd} + C_F$) in B.7 and lower the unstable frequency band. The disadvantage is that it severely lowers the transistor f_T, and is commonly used in low frequency amplifiers.



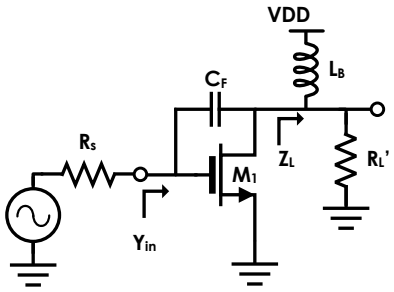
(a) Input



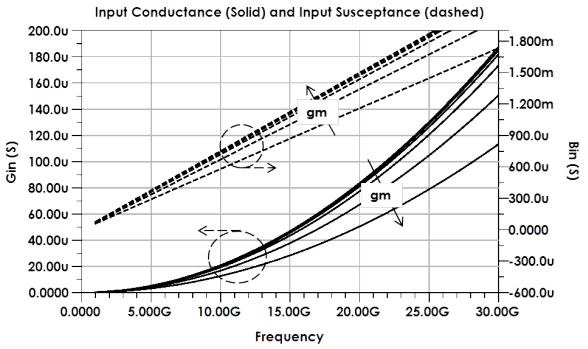
(b) Output

Figure B.3: Input and Output Conductance(Solid) / Susceptance(Dashed) of the Common Source Amplifier with $L_B = 1\,nH$ and $R'_L = 50\Omega$

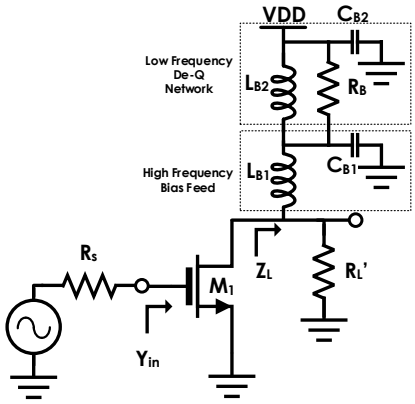
Another method is to add a low frequency de-Q-ing network. Figure B.4c is an implementation presented by Cripps[56] for stabilizing power amplifier bias networks. L_{B2} and R_B form a low Q bias feed and is added in series to the high frequency bias feed, L_{B1}. C_{B1} is large enough to create a short for high frequencies, but small enough to pass unstable low frequency components into the low-Q network and dampen the response. This method can be applied when operating devices at frequencies closer to the transistor's f_T. The cascode configuration (Figure B.4e) is the most widely used. The common-gate transistor acts as a buffer to the common-source, and increases it's isolation from the load. It also presents a resistive load which stabilizes the transistor. The drawback is the added noise presented by the common-gate transistor.



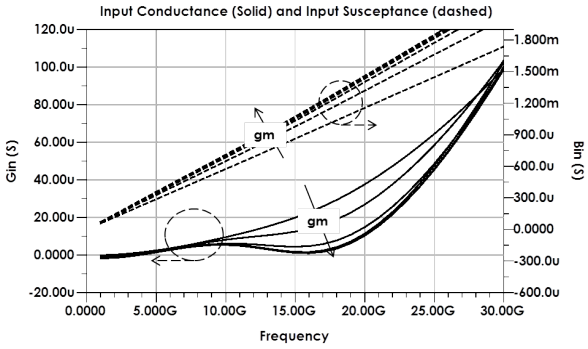
(a) Capacitor feed-back



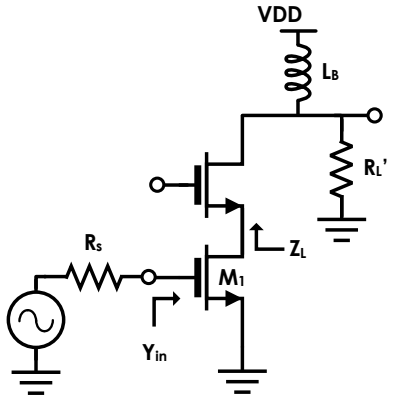
(b) Admittance [$L_B = 1\,nH$, $C_F = 40\,fF$]



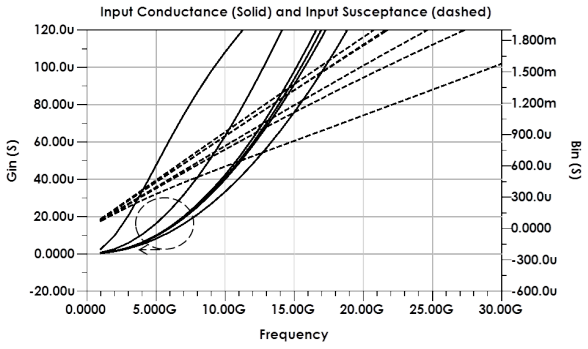
(c) Low frequency de-q network



(d) Admittance [$L_{B1} = 0.88\,nH$, $L_{B2} = 10\,nH$, $C_{B1} = 180\,fF$, $C_{B2} = 1\,pF$]



(e) Cascoding



(f) Admittance [$L_B = 1\,nH$]

Figure B.4: Common source load configurations

Appendix C

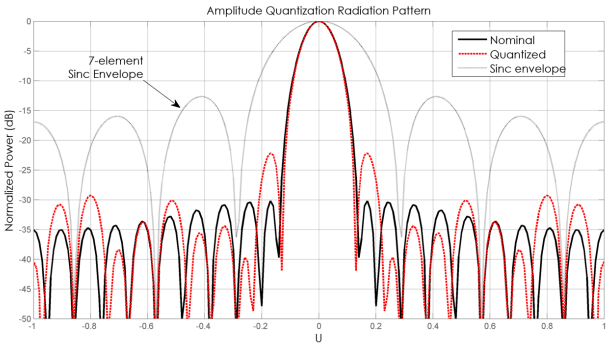
Effect of Amplitude Quantization

As in the case of phase shifters, VGAs and VAs can also be implemented with analog or digital control. The digitally controled VGAs/VAs will have quantized gain/loss levels determined over some dynamic range. Similar to phase quantization effects, tapering quantization and was shown to lead to "quantization lobes" in the visible band. Mailloux[34] analysed the effect of amplitude quantization as sub-arrays in the current distribution. He showed that the sub-arrays produce quantization lobes with a normalised power computed as:

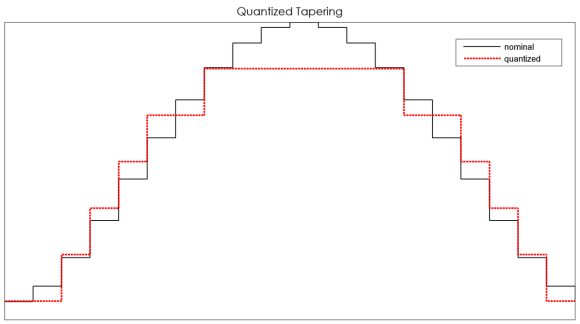
$$P_{QL} = \frac{B_b^2}{M^2 m^2 sin^2(\pi p/M)} \tag{C.1}$$

where M is the number of elements in the sub-array, m is the number of sub-arrays and B_b is the beam broadening factor defined as the ratio of the beamwidth of the tapered pattern to a uniform pattern. (C.1) assumes that the amplitude distribution has regular sub-arrays, which applies to triangular type distribution, but Chebyshev and Taylor type distribution have irregular sub-arrays and typically don't generate quantization lobes. The amplitude quantization in this case tends to create dominant sub-arrays at the centre with a quantized amplitude distribution which shapes the original pattern with a sinc distribution.

To illustrate this, Figure C.1b shows a 3-bit quantized element distribution for a 21-element array employing taylor distribution with $30\,dB$ sidelobe level. The quantized centre elements form a 7-element rectangular array which shapes the original radiation pattern with a sinc pattern as shown in Figure C.1a. The result is a radiation pattern with $22\,dB$ sidelobe level and spurious side-lobes in the visible region corresponding to the sidelobes of the 7-element sinc distribution. The irregularity of the sub-arrays makes it difficult to find an



(a) Nominal and quantized radiation pattern



(b) Nominal and quantized amplitude distribution

Figure C.1: Radiation Pattern and Element Tapering for a 21-element array, employing Taylor distributed tapering with $30\,dB$ sidelobe level

appropriate closed form bound to the number bits required and thus should be determined from array factor simulations.

Appendix D

Active Inductor

The PMOS and NMOS implementations of the active inductor load are shown in Figure D.1a and D.1b.

To see how the active inductor can be used to realise a wideband resistive load, consider the small signal representation in Figure D.1c where the effect of C_{gd} is ignored. To analyse the equivalent input impedance, ignore r_o and apply the test current and voltage:

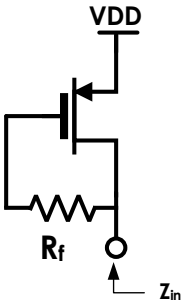
$$\begin{aligned} Z_{in} = \frac{V_x}{I_x} &= \frac{R_f + \frac{1}{j\omega C_{gs}}}{\frac{g_m}{j\omega C_{gs}} + 1} \\ &= \frac{R_f + \frac{1}{j\omega C_{gs}}}{\frac{\omega_T}{j\omega} + 1} \\ &= \frac{(R_f + \frac{\omega_T}{\omega^2 C_{gs}}) + j(\frac{R_f \omega_T}{\omega} - \frac{1}{\omega C_{gs}})}{\frac{\omega_T^2}{\omega^2} + 1} \end{aligned} \tag{D.1}$$

Assuming $\frac{\omega_T^2}{\omega^2} >> 1$:

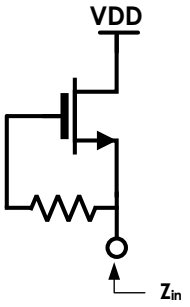
$$Z_{in} = \frac{V_x}{I_x} = \left(\frac{R_f \omega^2}{\omega_T^2} + \frac{1}{\omega_T C_{gs}}\right) + j\frac{\omega}{\omega_T}\left(R_f + \frac{1}{\omega_T C_{gs}}\right) \tag{D.2}$$

The real and imaginary part can be written as:

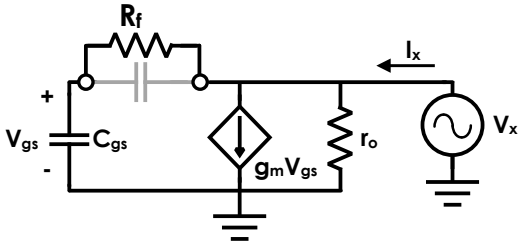
$$\begin{aligned} R_{in} &= R_f \frac{\omega^2}{\omega_T^2} + \frac{1}{g_m} \\ X_{in} &= \frac{\omega}{\omega_T}\left(R_f - \frac{1}{g_m}\right) \end{aligned} \tag{D.3}$$



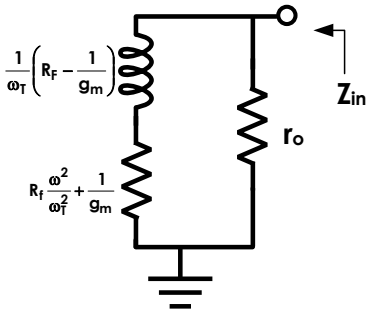
(a) PMOS type



(b) NMOS type



(c) PMOS Type (small signal)



(d) Input impedance

Figure D.1: Active inductor load implementation

The equivalent impedance circuit of the active inductor in Figure D.1d consists of a lossy R-L circuit provided $R_f > \frac{1}{g_m}$. If $R_f = \frac{1}{g_m}$, the active inductor becomes purely resistive over a wide frequency range (frequency independent L_{eff}).

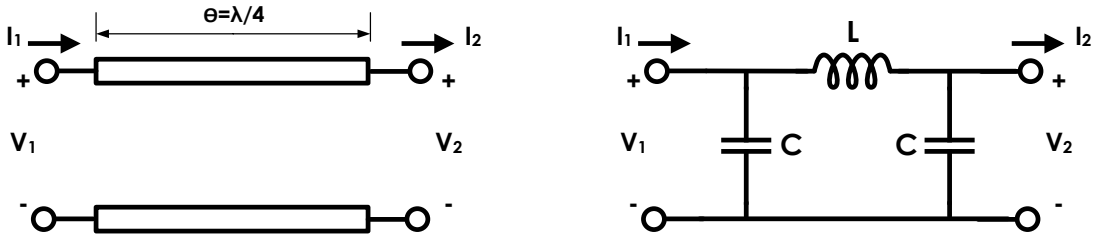
$$\begin{aligned} R_{in} &= \frac{1}{g_m}\left(1 + \frac{\omega^2}{\omega_T^2}\right)||r_o \approx \frac{1}{g_m}||r_o \\ X_{in} &= 0 \end{aligned} \tag{D.4}$$

Appendix E

Quarter-Wave Length Implementation

At the k and ka band of frequencies, Quarter-Wave length lines are between $2.5\,mm$ and $5\,mm$ in physical length, which is normally not feasible for on-chip implementations. However, the quarter-wave length line can be synthesized using lumped-element equivalent networks [53]. Consider the distributed and lumped circuit in Figure E.1. The ABCD parameters of the distributed circuit is given as [53]:

$$[ABCD]_{TL} = \begin{bmatrix} cos(\theta) & jZ_0 sin(\theta) \\ jsin(\theta)/Z_0 & cos(\theta) \end{bmatrix} \tag{E.1}$$



(a) Distributed (b) Lumped equivalent

Figure E.1: Quarter-wave length networks

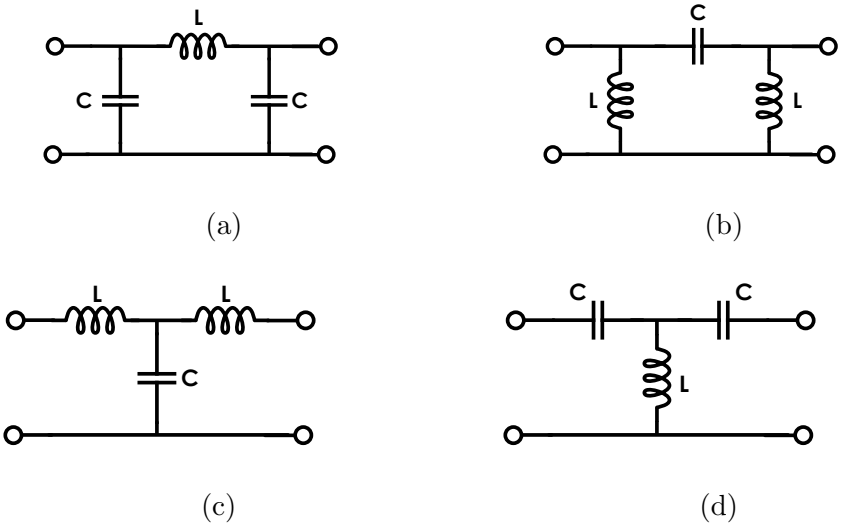


Figure E.2: Lumped element equivalent quarter-wave length networks

for the LC equivalent network:

$$[ABCD]_{LC} = \begin{bmatrix} 1-\omega^2 LC & j\omega L \\ j\omega C(2-\omega^2 LC) & 1-\omega^2 LC \end{bmatrix} \tag{E.2}$$

At a centre frequency, $\omega = \omega_0$, where $\theta = \pi/2$, the ABCD parameters of the distributed network is related to the lumped element equivalent as:

$$\begin{aligned} \omega_0 &= \frac{1}{\sqrt{LC}} \\ Z_0 &= \omega_0 L = \frac{1}{\omega_0 C} \end{aligned} \tag{E.3}$$

Using (E.3), it is possible to synthesize quarter-wave length lines with Lumped elements given the center frequency ω_0, and system impedance Z_0. The formulation is applicable to four LC configurations shown in Figure E.2

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