Current Contour Based Design Methodology for IMN Design of Doherty Power Amplifiers

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Carrier aggregation (CA) is used in modern communication schemes to increase communication bandwidth (BW) and reduce redundant equipment. This combined with the already high peak to average power ratio (PAPR) signals in use for complex modulation schemes results in stringent linearity requirements and degradation in the average drain efficiency (DE) in basic power amplifier (PA) topologies. This has led to research interests in highly efficient broadband PAs capable of addressing the bandwidth and multi-standard requirements. Several techniques have been developed to enhance the efficiency of PAs when driven by a modulated signal with high PAPR, but amongst them the Doherty power amplifier (DPA) has garnered considerable attention in research and commercial adoption.

In this work the importance of the current profiles at the drain of the main and peaking amplifier in the DPA is examined. By looking at the effect of the nonlinear capacitance at the input of the transistor, it is seen that choice of impedance presented at the fundamental and second harmonic have a drastic effect on the performance of the overall PA. To combat these issues, the constant current circle is introduced to aid in the design of the input matching network (IMN) of the main and peaking. By using the current contours the fundamental drain current can be carefully dictated by presenting the correct impedance at the gate of the transistor versus frequency and input drive. Using the current contours in conjunction with the design methodology outlined allows for the simple design of DPA IMN to extract the most performance out of the output combining node (OCN).

To validate the introduced material a 12-W 3.0-5.0GHz DPA was constructed using GaN HEMT transistors. The simulation results showed that the current profiles remained within range when using an iterative design approach along with current contours. Measurement results showed that the PA was able to achieve a gain of 8dB within the designed band. As well the efficiency at both peak and BO was greater than 37% across the band. To show the performance of the PA under modulated signal, the PA was tested with a 80MHz intra-band non-contguous signal at 3.3GHz. Before DPD the reported ACLR was 37dBc/Hz. Applying a DPD engine, the ACLR was brought down to 48dBc/Hz, or the noise floor of the equipment.

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Chapter 1

Introduction

1.1 Motivation

Wireless communication systems have become a critical component of our day-today lives over the past decade. With the introduction of smart-phones, the use of cellular communication systems has moved from voice-centric to more data-centric applications. This broader usage has brought along a need for higher throughput and bandwidth resulting in newer modulation schemes, such as Long Term Evolution (LTE) along with existing legacy systems, such as Wide-band Code Division Multiple Access (WCDMA). These new modulation schemes utilize carrier aggregation (CA) to utilize the available bandwidth (BW) efficiently. Fig.1.1 presents three use cases for Carrier Aggregation, (a) intra-band, contiguous, (b) intra-band, non-contiguous, and (c) inter-band, non-contiguous. This along with the need to reduce redundant equipment for base stations when supporting multiple modulation schemes at different frequencies has resulted in the need for wide-band Power Amplifiers (PA).

As well, to address this need and maximize spectral efficiency current wireless communications systems utilize signals with high peak to average power ratios (PAPR). An example of this signal can be seen along with its accompanying probability density function (PDF) in Fig.1.2. As seen the signal displays a wide range of amplitude values, with an average signal power significantly lower than the peak. This requires PAs which are highly linear and provide high efficiency at back-off (BO) power levels.
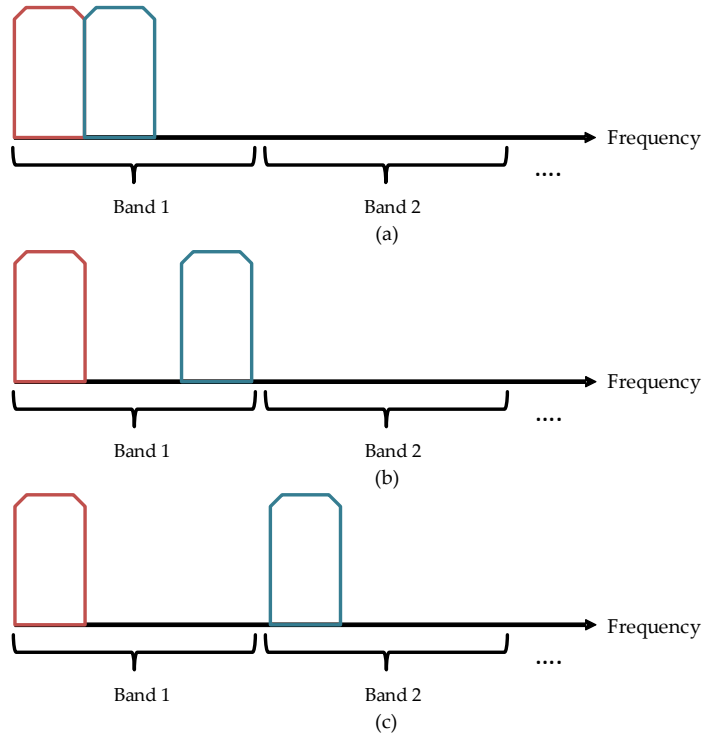
Figure 1.1: Three carrier aggregation scenarios, (a) intra-band, contiguous, (b) intra-band, non-contiguous, (c) inter-band, non-contiguous.

1.2 Problem Statement

In conventional power amplifier classes (e.g class-A, AB, B, C etc) the drain efficiency drops significantly as the power is backed off. Fig.1.3 shows an ideal efficiency versus output power plot for a conventional class-B amplifier. As can be seen the peak efficiency, 78.5%, is only achieved at one output power level, and the efficiency drops as this lowered, with 38% efficiency at 6dB BO. This is a significant problem for modulated signals where the majority of the signal lies within the BO region.

This brings forth a need for highly efficiency PAs for modulated signals. This has included topologies such as envelope tracking (ET), linear amplification using non-linear components (LINC), and Doherty. All these techniques try to address the low efficiency at
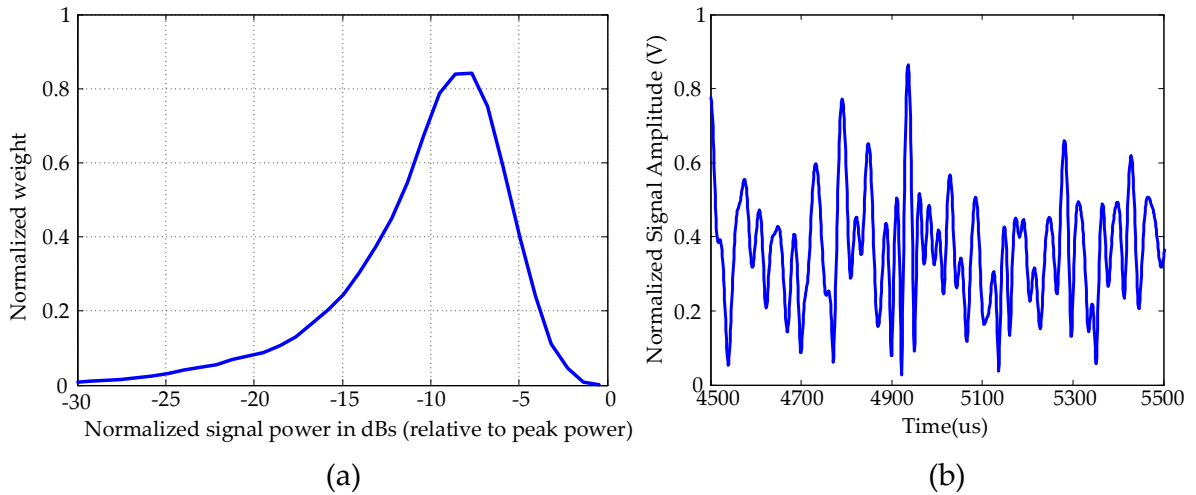
Figure 1.2: 7.1dB PAPR LTE Signal (a) probability distribution function (PDF) and (b) time domain signal.
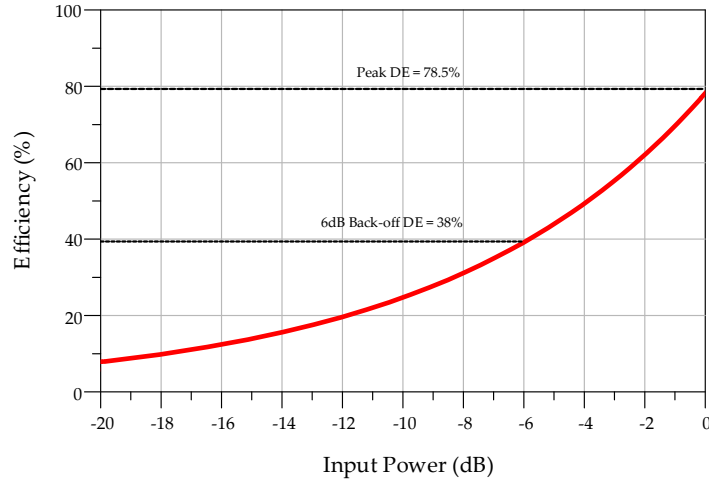
Figure 1.3: Ideal class-B PA efficiency.

BO in varying manners. From these techniques the Doherty Power Amplifier (DPA) has garnered significant interest in the research and industrial community due to its simple

implementation and and inherent benefits [1].

However, the conventional DPA has proved to be very narrowband due to its limiting output combining network (OCN). As such, much of the recent research has focused on extending the BW of the OCN without any consideration as to the effect of IMN on the overall BW. This has caused a significant degradation in achievable performance of the DPA, as the two driving factors in its operation are the load modulation, dictated by the OCN, and the current injection, dictated by the IMN.

In this thesis, a novel approach is presented whereby the IMN is designed using current contours to carefully dictate the fundamental drain current delivered to the OCN by presenting the correct impedances at the input. This along with a case study on the effects of the second harmonic for III-V semiconductor transistors, such as Gallium-Nitride (GaN) on the input allows for the formulation of a design methodology that can be used to create the IMN for the main and peaking transistors.

1.3 Thesis Organization

The organization of the thesis is as follows. Chapter 2 starts introduces the basic operation of a radio frequency (RF) power amplifier (PA) along with its limitations. This will continue on towards advanced wide-band power amplifier strategies such as waveform engineered classes. This includes class B/J. This will followed by information on the Doherty Power Amplifier (DPA), which is the underlying topic in this thesis. This chapter will conclude with a literature review where past research is presented along with results for the state of the art implementations of a DPA.

Chapter 3 presents a novel approach to the design of an input matching network (IMN) for a DPA and is the core of this thesis. IMN challenges are presented and how they relate to Gallium-Nitride (GaN) transistors specifically due to the effect of the second harmonic caused by the non-linear input capacitance. A new design tool, the current contour is introduced, along with a design methodology to create an IMN for the main and peaking transistors of the DPA. Chapter 4 presents the implementation and simulation results for a 3.0-4.8 GHz DPA designed using the methodology described in chapter 3. Chapter 4 also provides measurement results for the designed DPA. Finally, chapter 5 will conclude the work done in this thesis and provide some suggestions on future works.

Chapter 2

Power Amplifier Overview and Literature Review

In this chapter an overview of classical power amplifiers will be provided. This will be followed by more detail on advanced techniques to extend the bandwidth such as waveform engineered PAs, as well as efficiency enhancement modes such as the Doherty power amplifier along with the limitations of current topologies.

2.1   Overview of Classical Power Amplifiers

The PA is a critical component in any RF transmitting system. It takes a small signal which has been processed through the RF chain and enlarges it so that it can be transmitted through an antenna for large distances. The amount by which it is amplified is called the gain, and can be calculated using the following equation.

$$G = \frac{P_1}{P_{in}} \tag{2.1}$$

P_1, is the output power from the PA in watts at the fundamental frequency or carrier frequency (frequency of interest). P_{in} is the input power also in watts. The amplification takes place by converting DC power to RF power using an active device such as a transistor. Due to its high power consumption, the PA is generally the largest power consuming device in the transmit chain, and dictates the efficiency of the overall system. The drain efficiency of the PA is calculated using the following equation.

$$DrainEfficiency = \eta = \frac{P_1}{P_{dc}} \tag{2.2}$$

Here P_{dc} represents the DC power consumption of the transistor. Any lost power, or power not translated to RF power is lost as heat. This formulation however does not take into account the gain of the PA, which can be described using power added efficiency (PAE) as calculated below.

$$PAE = \frac{P_1 - P_{in}}{P_{dc}} \tag{2.3}$$

As well, since it is the last component before the antenna it also dictates the linearity of the system. The linearity of the PA along with the efficiency can be adjusted by using several factors in the design, such as the matching networks, biasing, and topology of use.

Classical power amplifiers consists of a single transistor, which is the active device in the circuit, along with the biasing and matching networks. The transistor, which is a voltage controlled current source (VCCS), converts an input voltage to an output current, based on its transfer characteristics. Fig.2.1 below shows the the transfer characteristics of an idealized transistor with abrupt turn-on and saturation points.
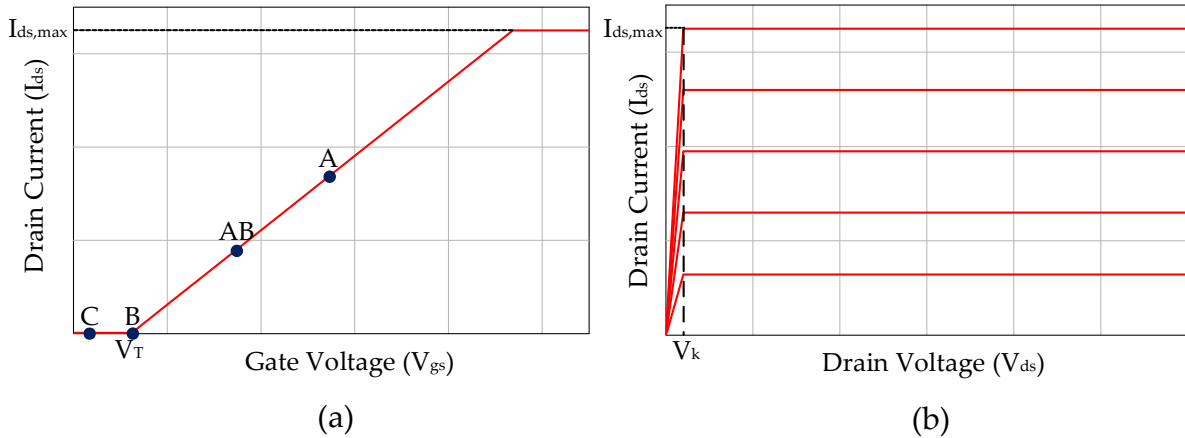
Figure 2.1: Ideal transistor (a) transfer and (b) output characteristics.

The DC biasing of the transistor at the input (gate) determines the class under which it operates. For instance in the class-A scenario the transistor is biased halfway between

the turn-on and cutoff point. To achieve the maximum gain at the output, the OMN transforms the load impedance to the PA's optimal impedance, R_{opt}. R_{opt} is determined by the maximizing the achievable power of the device. This means biasing the drain to allow for maximum swing ($V_{DS,max}/2$). R_{opt} can be calculated using the following formula.

$$R_{opt} = \frac{V_{DS,max}/2}{I_{max}/2} \tag{2.4}$$

Under this class-A configuration a PA is able to achieve a maximum DE of 50% which can be calculated based on current and voltage swings at the output. This efficiency is further degraded as the power is backed-off, as the DC consumption remains constant and RF power is decreased. As well, when non-idealities of the transistor is taken into account, such as the knee region. The possible efficiency is decreased by the appropriate amount.

Moving away from the class-A biasing towards the turn-on point, the efficiency can be increased, as the DC consumption is decreased. For instance in the class-B scenario the efficiency at peak is 78.5%. Anything between these two points, known as class-AB would be between the class-A and class-B. Further reduction below the threshold voltage results in class-C operation where efficiency can move towards 100%. The main disadvantage or trade-off for this increase in efficiency is gain. As the biasing is decreased, a larger input drive is needed to reach peak output power. Also, when operating outside of class-A the current waveform is clipped, introducing non-linearity to the system. A summary of the classical modes of operation of a PA is shown in Table.2.1.

Table 2.1: Summary of operation modes for classical power amplifiers.

Class of Operation	Efficiency	Gain	Linearity
A	Poor	Excellent	Excellent
AB	Satisfactory	Good	Satisfactory
B	Good	Satisfactory	Excellent
C	Excellent	Poor	Poor

2.2   Waveform Engineered Power Amplifiers

The main problem with classical amplifier topologies is the low efficiency and narrow design space. As mentioned the termination for classical amplifiers consists of R_{opt} and assumes that all the harmonics are shorted. To construct a wide-band amplifier, an OMN is needed to transform the load impedance to the desired R_{opt} across the operating frequency range. This however is difficult due to the narrow design space (single value). As well, in the classical cases all the harmonics are short circuited, which is difficult to achieve versus frequency and isn't always needed to achieve the best results.

In more advanced PA classes of operation, the harmonics can be tuned to modify the waveforms seen at the drain of the transistor. This is called waveform engineering. Two popular topologies utilizing waveform engineering are the class-F and class-B/J PAs which will be further discussed below.

2.2.1   High Efficiency Class-F/F^{-1} Power Amplifier

The class-F amplifier utilizes harmonic tuning to increase the effiency of the PA. A class-F PA topology is shown in Fig.2.2 along with its waveforms. As seen, the voltage waveform is now a perfect square wave. By reducing the overlap between the current and voltage waveforms, the efficiency can be extended to 100% in the ideal case by reducing the power dissipation in the transistor to zero. By writing the Fourier series expansion of the waveforms it can be shown that the square voltage waveform is achieved by presenting a short circuit to the even harmonics, while presenting an open circuit to the odd harmonics. The circuit for the class-F shown realizes this using a simple stub.

The equations governing the theoretical operation of the class-F amplifier are shown in Eq.(2.5)-(2.7). In real world implementations these requirements are relaxed to make the OMN more realizable. For instance by tuning upto just the third harmonic, the efficiency can be 90% in theory [2]. A dual of the class-F is the inverse class-F. By realizing the opposite load impedances, the current waveform can be squared and the voltage waveform can be left as a half-sine wave. This in theory also produces an ideal efficiency of 100%.

$$Z_L(f_o) = R_{opt} \tag{2.5}$$

$$Z_L(2nf_o) = 0 \tag{2.6}$$

$$Z_L(2(n+1)f_o) = \infty \tag{2.7}$$
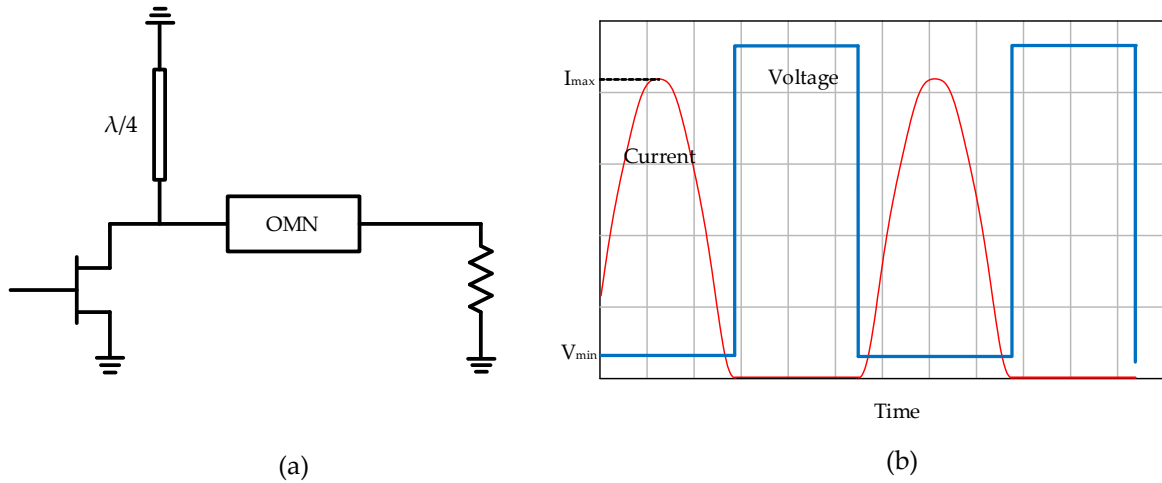
Figure 2.2: Class-F (a) circuit (b) waveforms.

In literature the class-F has shown to provide good performance in terms of efficiency but suffers from linearity issues since the transistor is operated in an over-driven mode. As well, the classical class-F formulation resulted in a very narrow design space due to the strict impedance requirements. This was solved through migrating away from class-F into another class or by designing dual-band networks for CA scenarios [3]. More recent work has allowed for a much more broad design space, called the continuous class-F [4]. This method of designing a class-F has shown to provide the ability to design wideband PAs resulting in over an octave in BW. However, as is the case with signal ended PAs the efficiency still significantly degrades as the input power is backed-off.

2.2.2 Class-B/J/J* Power Amplifier Design Space

Another waveform engineered topology very popular in research is the class-B/J amplifier. Similar to what the continuous class-F does for the class-F, the class-B/J amplifier increases the design space for the class-B PA. The theory shows that rather then one point on the Smith chart which produces class-B performance, there are multiple. These regions can be accessed by presenting various fundamental and second harmonic impedances (higher order harmonics are assumed to be shorted) to tune the waveform such that the resulting PA will have the same performance in terms of gain, efficiency, and linearity of that of a

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class-B. The equations that dictate this performance are derived in [5] and shown here in equation 2.8-2.9 where α is bounded between ± 1.

$$Z_L(f_o) = R_{opt} + j * \alpha * R_{opt} \tag{2.8}$$

$$Z_L(2f_o) = 0 - j * \alpha * \frac{3\pi}{8} * R_{opt} \tag{2.9}$$

Plotting the result on a Smith chart, the design space becomes more clear. In Fig.2.3 the class-B/J design space is plotted for an ideal transistor at the normalized current source plane. The blue dots represent the second harmonic terminations for various α values from -1 to 1. The red dots represent the corresponding fundamental impedances for the same range. As can be seen when α is equal to zero, the PA is operating in class-B (the reactive component is perfectly shorted). As α is increased towards 1 a corresponding negative reactance is required at the second harmonic, whereas when α moves towards -1 a corresponding positive reactance is required. When looking at the waveforms of the resulting drain current and voltage, a strong 2nd harmonic content can be seen. This results in the voltage swinging higher then peak in class-B, meaning for full power utilization a larger breakdown voltage transistor is required.

In literature the class-B/J design space has shown good results, with reported PAs having wideband operation with performance over an octave due to larger options when creating an OMN [6]. A larger design space can further be achieved when making small concessions on the efficiency and output power as shown in [7]. However, as mentioned since the PA provides the same performance as that of a class-B, the resulting PA suffers the same cons with the added pro of wider achievable BW.

2.3   Efficiency Enhancement Topologies

Efficiency enhancement mode topologies try to address the problem of low back-off efficiency by modifying the load impedance and biasing depending on the input signal to achieve high efficiency. Although various topologies do exist the three most popular include the linear amplification with nonlinear components (LINC), envelope tracking (ET), and the DPA.
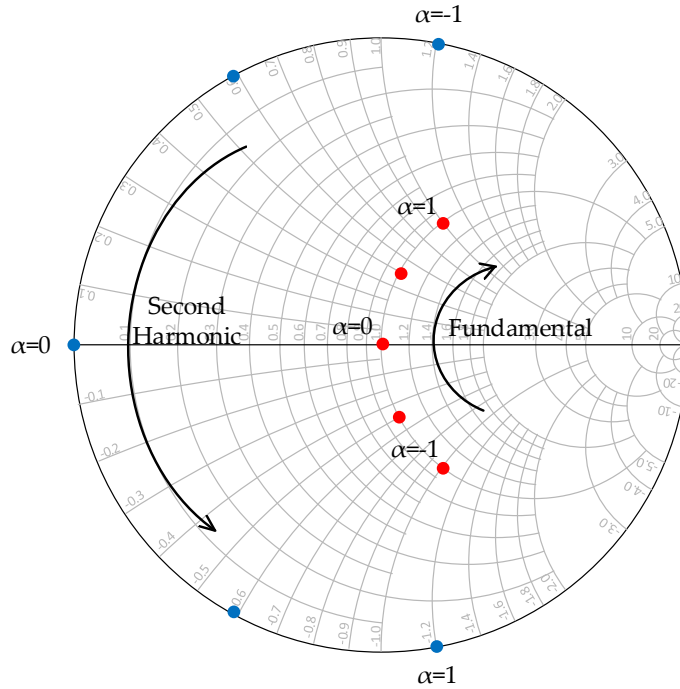
Figure 2.3: Class-B/J/J* design space for fundamental (red) and second harmonic (blue) at normalized current source.

2.3.1 Linear Amplification with Nonlinear Components

LINC was first introduced by Chireix in 1935 [8]. LINC tries to replace the linear, but inefficient amplifiers needed for AM signals with a non-linear highly efficient PA such as a class-F. A block diagram of a LINC PA is shown in Fig.2.4.

By taking an AM signal and decomposing it into two separate phase modulated signals, these signals can then be amplified using a non-linear PA which can have very high efficiency, but would otherwise distort the AM signal. A separate passive combining network would add the two signals coming out of the PAs together to reconstruct an amplified version of the original input signal. The decomposition of the signal is done by relating the amplitude of the original signal, $A(t)$ to a phase value as shown in equations 2.10-2.12 [9].
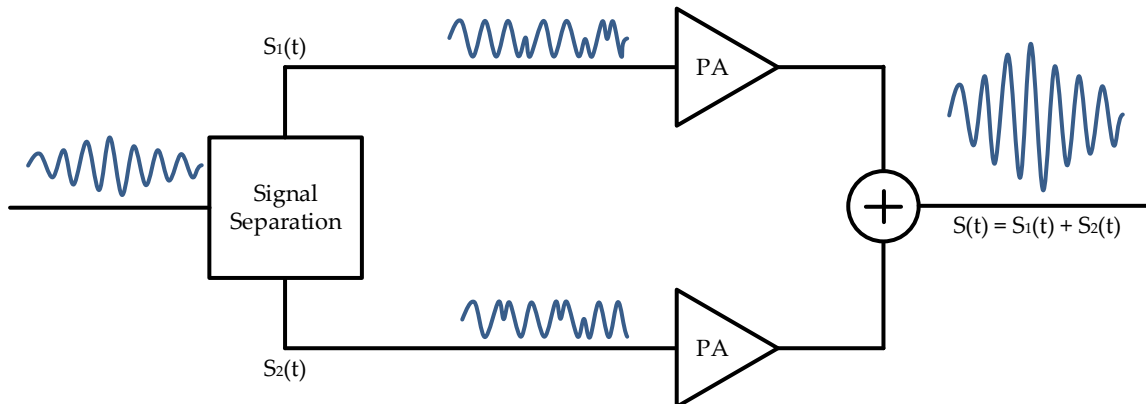
Figure 2.4: Simplified block diagram of a LINC system.

$$S_1(t) = 0.5cos(\omega_0(t) + \theta(t) + sin^{-1}(A(t))) \qquad (2.10)$$

$$S_2(t) = 0.5cos(\omega_0(t) + \theta(t) - sin^{-1}(A(t))) \qquad (2.11)$$

$$S(t) = S_1(t) + S_2(t) \qquad (2.12)$$

LINC PAs have in theory shown good performance, but the efficiency is significantly decreased by the output combiner. In general, two types of combiners exist, loss-less low isolation combiner, or lossy high isolation combiner. The former results in good efficiency but a significant degradation in linearity due to impedance presented to each transistor varying with the phase. The latter combiner results in poor efficiency of the overall system. These problems in literature have resulted in PAs with either poor efficiency when compared to conventional classes of operation or very narrow BW when compared to other efficiency enhancement techniques [10].

2.3.2 Envelope Tracking Power Amplifiers

ET PAs use the concept of drain modulation to increase the efficiency of a PA under modulated signal. As seen previously as the PA is backed off from peak power the efficiency decreases as the relationship between fundamental output power and dc power is increased. By modulating the DC drain voltage as a function of input voltage, the power consumed

by the transistor can be decreased at BO to increase the overall efficiency. This is done by reducing the DC voltage to maintain a maximum voltage swing at the output. A block diagram of an ET PA is seen in Fig.2.5.
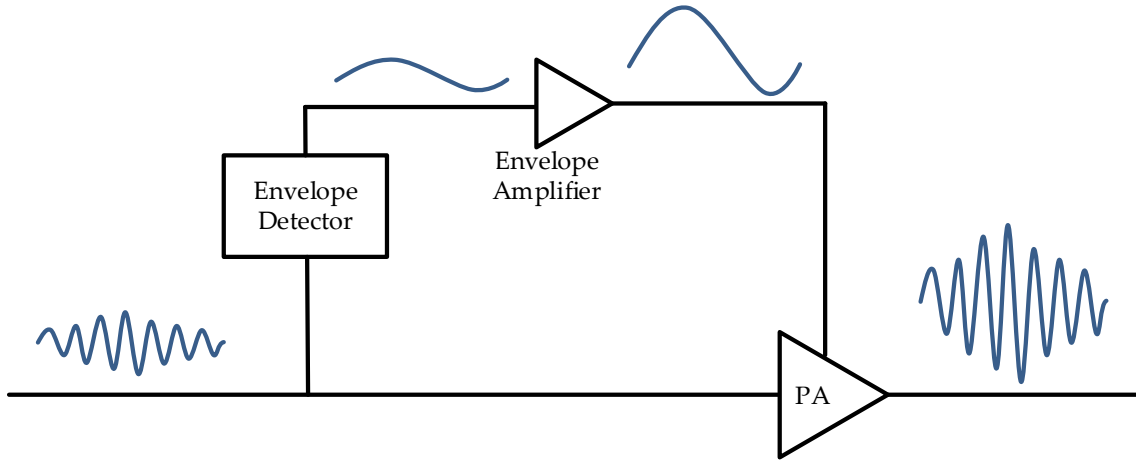
Figure 2.5: Simplified block diagram of a envelope tracking system.

The ET PA consists of three main components, the envelope detector, envelope amplifier, and the PA. The envelope detector tracks the input signal amplitude and passes it to the envelope amplifier which magnifies the signal and applies it to the drain of the PA. The PA in this system in contrast to LINC still needs to be highly linear as the linearity of the system is highly dependent on it, thus the PA is generally not a highly efficient PA such as a class-F. However, the envelope signal can be altered to to increase the linearity of the system digitally to allow for more efficient operation [11]. The major drawback with ET is the efficiency is highly dependent on that of the envelope amplifier, as the overall efficiency is dictated by equation 2.13.

$$\eta_{(overall)} = \eta_{PA} * \eta_{EA} \tag{2.13}$$

In recent literature, efforts have been made to increase the overall efficiency of the PA by either decreasing the power consumption of the envelope tracking PA or utilizing a combination of a linearization technique along with a nonlinear PA [12]. Other works have focused on increasing the BW of the ET PA which is limited by the envelope amplifier for

use with CA signals. This works however, are not able to achieve the combination of the efficiency and BW achieved by the next technique.

2.3.3 Doherty Power Amplifier

Conventional Doherty Power Amplifier

The Doherty power amplifier is an efficiency enhancement mode technique presented by W.H. Doherty in 1936 [13]. The use of the DPA was for vacuum tube based designs which dealt with high power amplitude modulated signals. Due to the amplitude modulation, high BO efficiency was required to reduce the operating cost of the equipment. More recently, the conventional DPA has become a very popular choice in the RFPA community due to its simple implementation and benefits when compared to other enhancement mode techniques discussed above. A basic schematic of a DPA can be seen in Fig.2.6 along with its ideal efficiency versus BO in Fig.2.7. As seen, the efficiency is drastically improved in BO in comparison to a regular class-B amplifier, allowing for a high efficiency region extending upto 6dB from BO. This aligns nicely with signals with high PAPR as the majority of the signal content is within the high efficiency range.
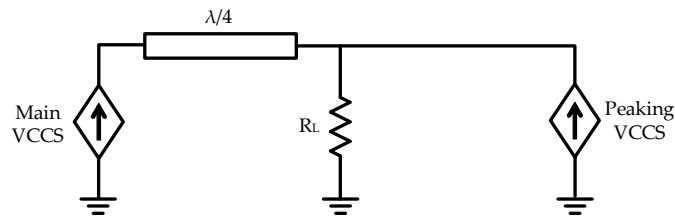
Figure 2.6: Simplified block diagram of a envelope tracking system.

The original or conventional DPA formulation, consists of two active devices, the main and peaking transistors, connected together through an output combing node (OCN). Both the devices are voltage controlled current sources (VCCS). Under this representation, ideal harmonic traps are placed at both the output and input of both transistors to short circuit the harmonic currents. The main device is connected to the OCN using a quarter wave impedance transformer. This allows the VCCS to be transformed to a voltage controlled voltage source (VCVS) at the center frequency. By doing so, the voltage at the output,
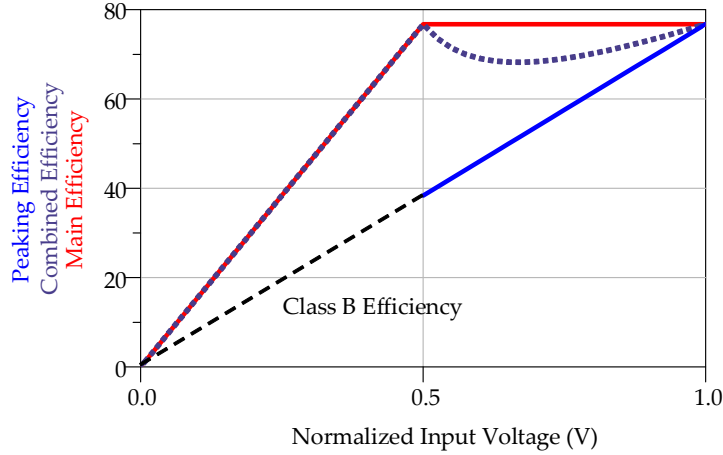
Figure 2.7: DPA efficiency for main (red), peaking (blue), and combined circuit(dotted purple) along with ideal class-B (black) efficiency for normalized input voltage.

across R_L, is strictly dictated by the main transistor. As such the linearity is determined by the that of the main transistor.

During the operation of the DPA, the peaking transistor is off during low input signals (anything beyond 6dB BO) by biasing it in a class-C mode. The main transistor which is biased in class-B (class-AB in real implementations) is providing all the output power, and the load seen by it is constant. During high input signals the peaking transistor turns on and injects current into the OCN. This current injection changes the impedance presented to intrinsic drain of the main, allowing for the voltage swing to be maximized for a larger range. By doing so the efficiency is increased versus power for a designated region under which this operation takes place while maintaining linearity. This variation in the impedance is called load modulation.

The overall operation of the DPA is dictated by two components, the OCN, or impedances presented to each transistor, and the currents injected by those transistors. In the conventional DPA, the current profiles are shown in Fig.2.8 along with the accompanying voltage profiles which are the result of the variation in impedance for the main. The OCN impedances can then be derived and results in the impedances presented to each transistor as shown in Fig.2.9.

The main limitations on the DPA occur from its narrow BW in the conventional case which is limited by various factors such as the quarter-wave impedance transformer. Pre-

Figure 2.8: Conventional DPA (a) current profiles and (b) voltage profiles for main (red) and peaking (blue) transistor versus normalized input voltage.
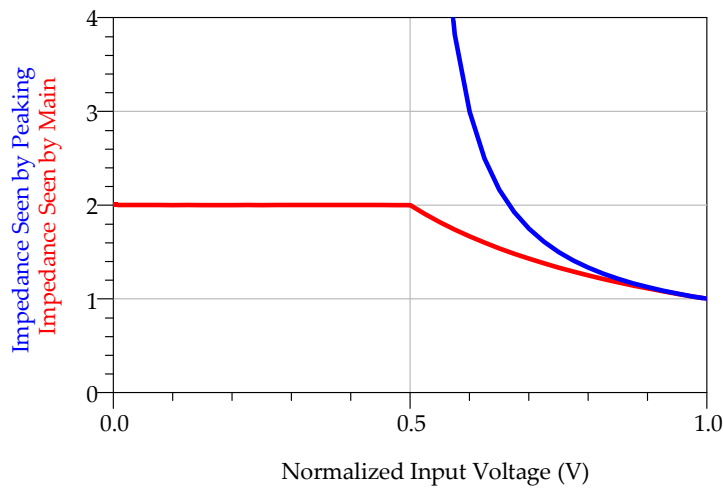
Figure 2.9: Normalized impedance seen by main (red) and peaking (peaking) transistor versus normalized input voltage.

vious studies on the impedance transformer have been conducted to show that the BW is limited to roughly 15% when taking into account a 10% degradation from peak efficiency

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[14]. This issue has led to solutions which try to address the problem by reducing the effective impedance transformation ratio by harnessing multiple sections tapered lines, off-set lines, and lumped components as shown in [15, 16, 17, 18]. However, the BW is still limited. Other works showed that by taking into account the parasitics of the DPA and absorbing them into the $\lambda/4$ line, the BW could be extended to harness the full capability of the conventional DPA [19]. Although all these results still use the original formulation and standard setup as depicted by Fig.2.10.
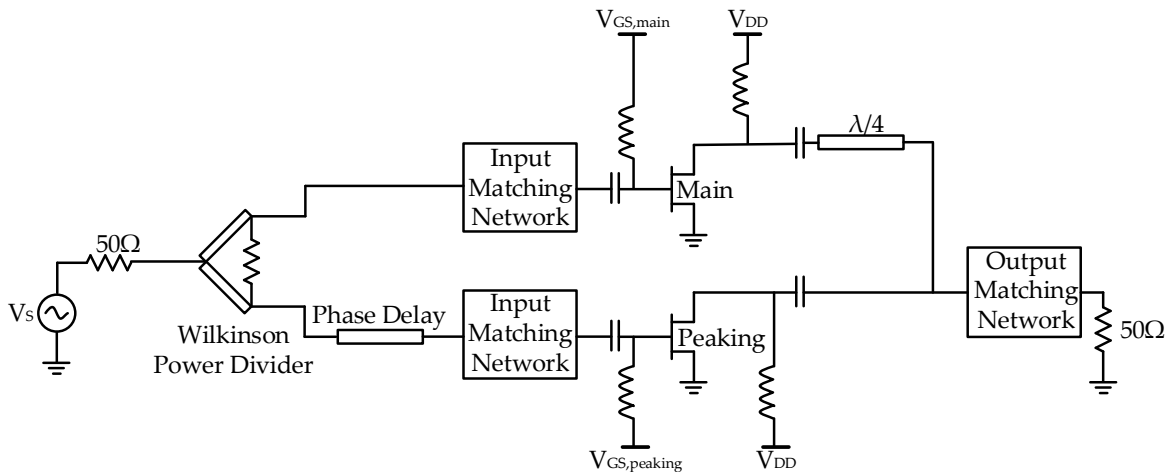
Figure 2.10: Simplified block diagram of a conventional DPA.

Advances in Doherty Power Amplifier

With the need to increase the BW of the DPA past its conventional threshold, more research has been conducted to move away from the original block diagram. For instance, some works have incorporated a mixed signal approach whereby the amplitude and phase of the input signal of the peaking transistor is controlled [20, 21, 22]. This allows for better performance to be achieved across frequency but with the added cost of complexity. As well, the mixed signal approach can only be used for single bands, and as such won't work for the inter-band non-contiguous signals CA.

Alternative works have moved away from the conventional DPA current profiles and circuit to yield much better results. The resulting DPA, known as the modified DPA, tackles the problem in reverse order, by first selecting the impedances of the circuit then

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deriving the required current profiles. By selecting the impedances, the BW at BO can be extended, while the peak is less susceptible to frequency dispersion [15]. The resulting current and voltage profiles are shown in Fig.2.11(a) and Fig.2.11(b) respectively with the overall block diagram remaining the same as the conventional DPA. This work showed good performance, achieving a BW of 35%. This work was further extended to show configurable back-off to extend the high efficiency range from the normal 6dB value to upwards of 10dB [23, 24]. However, the main drawback to this method is the need for asymmetrical biases for the main and peaking transistors. As a result, the peaking transistor needs to be biased much higher than that of the main, requiring transistors with high breakdown voltages. This can be made possible for transistors technologies such as GaN, but will result in poor power utilization factors for low breakdown technologies.
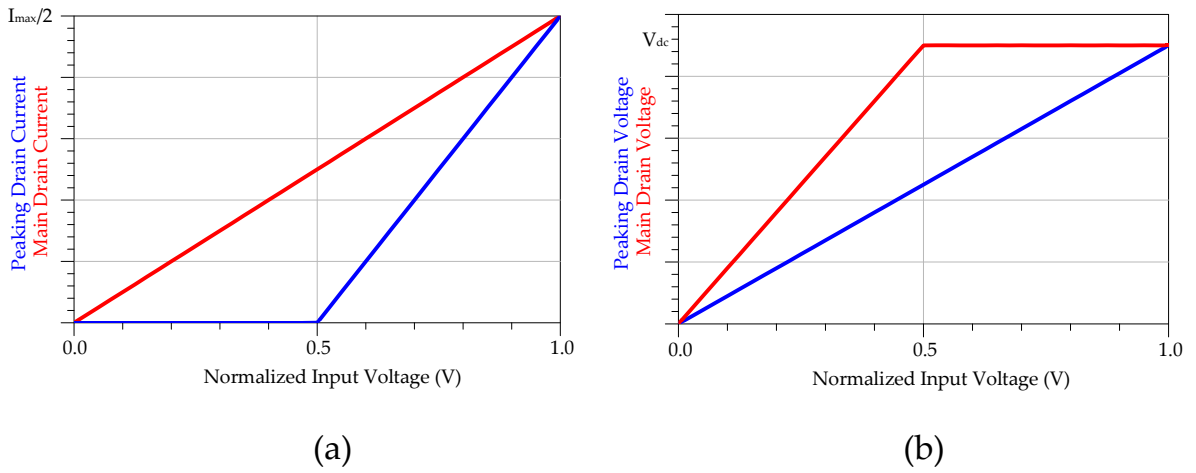

(a)   (b)
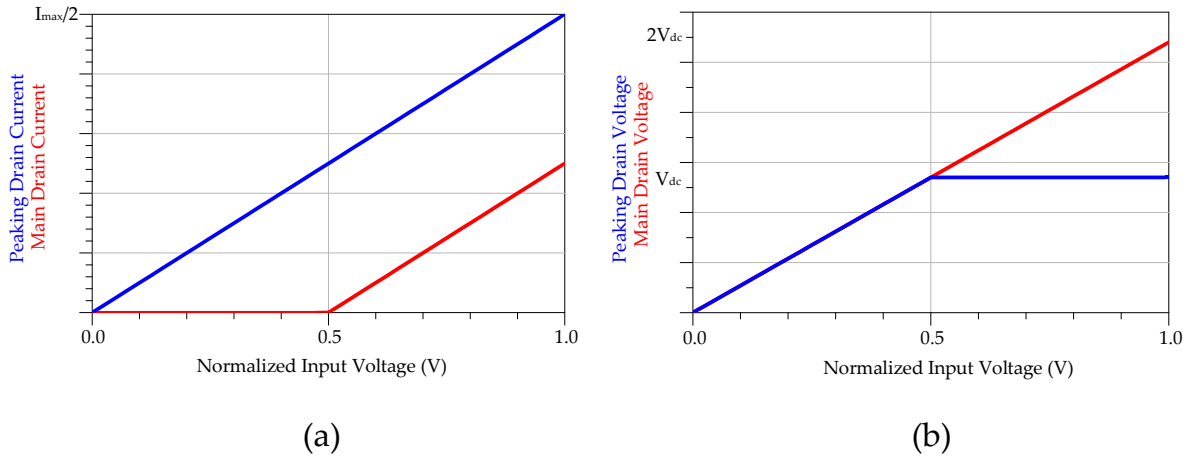
Figure 2.11: Modified DPA (a) current profiles and (b) voltage profiles for main (red) and peaking (blue) transistor versus normalized input voltage.

Alternatively, larger BO regions have been constructed using multiple peaking transistors, in a topology called N-way DPA [25]. However, most implementations run into similar problems that the 2-way DPA experience, such as the need for mixed signal input [26]. As well, the added complexity required for the input splitting, phase alignment, and load modulation results in sub-optimal results significantly degrading the achievable efficiency and linearity [27].

In recent work, the bandwidth of the DPA has been extended by modifying the configuration of the output combining network (OCN) to extend the load modulation bandwidth

and address the issues associated with the parasitics of the auxiliary device [28, 29, 30, 31]. An example of the new OCN is shown in Fig.2.12 where a $\lambda/2$ line is used and the phase delay is adjusted to the main amplifier. However, the loads presented to each transistor deviate significantly across the reported BW resulting in varying Doherty behavior.
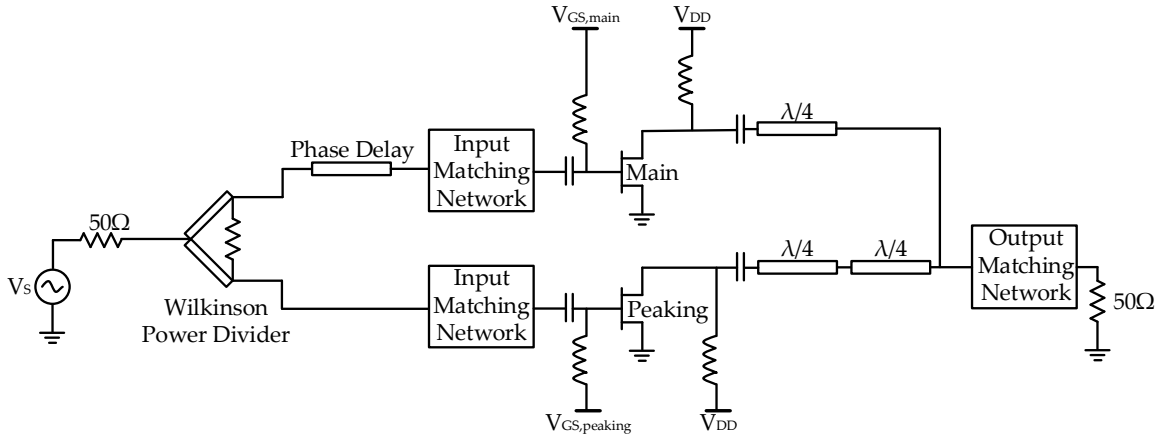
Figure 2.12: Simplified block diagram of a DPA with new $\lambda/2$ line in OCN.

More recent work has shown that replacing the preconceived notion and biasing of the transistors can drastically improve results if waveform engineered topologies are used in place of the main (class-AB) amplifier. However, these works have not addressed how the input can effect the performance of the DPA, and even limit the potential BW possible regardless of OCN topology, where it has been shown that the BW limitation has moved from the OCN to the input matching IMN.

Literature Review Summary

A summary of the of the works recently established for the DPA is presented below in Table.2.2.

Table 2.2: Summary of published DPA literature.

Year	Technique	Frequency (GHz)	Gain (dB)	P_{out} (dBm)	$\eta_{(6db)}$ min/max (%)
2010 [19]	Mixed-Signal	1.7-2.3	13	43	35/54
2012 [16]	Output Compensation	3-3.6	10	43	38/43
2012 [32]	TLLM	1.96-2.46	11	41	40/46
2012 [21]	Mixed-Signal	1.96-2.46	13	43	40/54
2012 [15]	Modified	0.7-1	15.3	49.9	48/57
2013 [24]	Modified	1.6-2.4	9	42	50/60
2014 [28]	OCN	0.79-0.96	20	55	48/50
2014 [31]	OCN	0.7-0.95	14	43	48/59
2014 [29]	OCN	0.47-0.8	15	58.5	38/47
2014 [30]	OCN	1.05-2.55	8	41	35/58

Chapter 3

Current Contour Based IMN Design Methodology for GaN Doherty Power Amplifiers

In this chapter the constraints on the IMN design for classical PAs will be demonstrated. Information will be presented on the nonlinear input capacitance of GaN devices and how it relates to the second harmonic's overall effect on the performance of the DPA. A case study will be presented outlining effects of a poor and good second harmonic termination at the input for two biasing conditions (main and peaking). Afterwards the novel concept of current contour based design will be introduced along with a design methodology to aid in the design of the IMN of a DPA.

3.1   Transistor Technology

In base station power amplifier design the transistor technology of choice has been dominated by the field effect transistors (FET)/ high electron mobility transistors (HEMT). RF transistors typically come packaged or in a bare form die. Die's exhibit less parasitics, which will be further discussed in a later section, in comparison to packaged transistors. This allows for much simpler designs due to less inherent non-linearites, as well as better performance overall in all three key metrics. However, a significant drawback is the reliability and assembly, which is much more complex in comparison to packaged devices. For this reason many real world applications and research activities prefer the use of packaged transistors.

Due to the need for high output power, base station transistors are chosen/optimized to give good efficiency, linearity, and impedance transformation ratios. The market itself consists of two competing technologies, laterally diffused metal oxide semiconductor (LD-MOS) FET and GaN HEMT. LDMOS currently is the dominant player in the industry for sub 2GHz applications due to its lower cost and high breakdown voltage. As well, LDMOS has shown to be much more linear in comparison to GaN, which exhibits a slow compression, when used in back-off or in linearization systems. Despite this and the higher cost, GaN has started to gain much more attention due to the benefits it offers. For instance the higher transition frequency, f_t, makes it attractive for potential future applications which will move towards high frequency. As well, GaN exhibits a much larger breakdown voltage and power density in comparison to LDMOS, which allows for greater reliability when the device is used in modern PA designs which use waveform engineering. These advantages make GaN an ideal candidate for this work where a higher frequency wideband DPA is the topic of conversation.

3.1.1   GaN Device and Package Characteristics

As mentioned in passing above, transistor packages add to the overall parasitics inherently present in a transistor. To understand the operation of a transistor more eloquently the transistor model and parameters need to be analyzed. In Fig.3.1 a simplified non-linear citcuit model of a transistor is shown. This model is suitable for both LDMOS and GaN, however, the effects of the parasitics and overall performance will be shown with examples of GaN parameters. It is important to note that real life models are much more complex, and consists of many more nodes, however, for the purposes of this study the simplified model will provide the same conclusions.

The parameters within the model can be divided into two components, the extrinsic and intrinsic parameters. The extrinsic parameters are outside the dotted area, and represent the linear and bias independent parts of the model. This includes all the components which connect the active area of the transistor to the external shell such as the bond wires and manifold. These parameters can be extracted using methods such as cold-FET. The intrinsic parameters, inside the dotted area, represents the active devices and non-linear components in the model such as the node capacitances and current source.

To a designer the intrinsic components are of the most interest as it consists of the power generating current source, and dictates the design of the matching networks. In GaN devices the capacitance at the gate, C_{gs}, and the feedback capacitance, C_{gd} cause the most problems as the drain capacitance, C_{ds}, is marginally non-linear. This translates to a
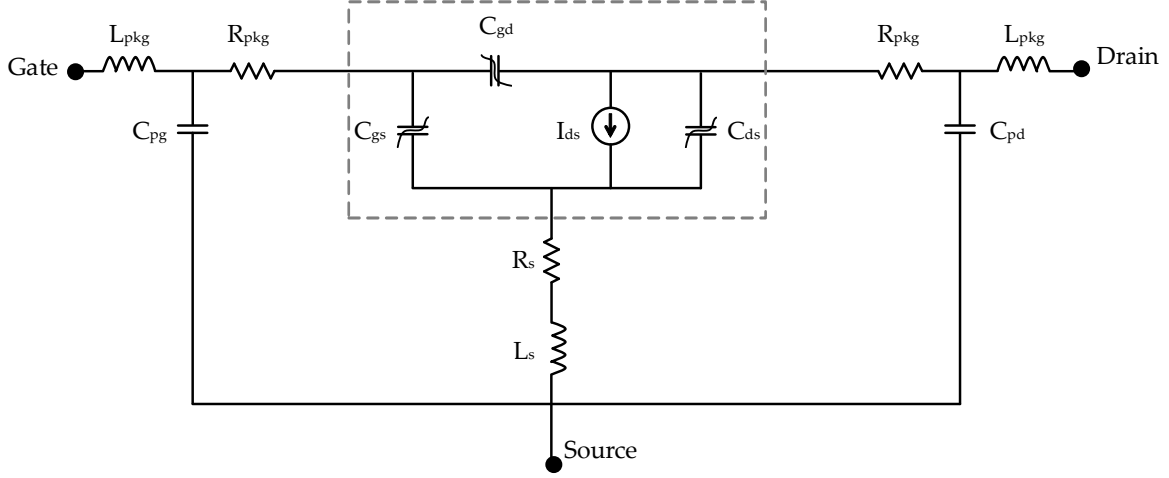
Figure 3.1: Simplified model of a packaged transistor

high variance in input capacitance of the transistor. For example the gate capacitance for a 6-W $0.25\mu m$ GaN packaged transistor is shown in Fig.3.2. Notice how the input capacitance varies significantly versus input drive, V_{gs}, almost doubling in the magnitude. This becomes even more significant for larger transistors where the value of the capacitance's are much larger. This in single ended designs causes significant issues for matching as the capacitance can only be resonated out at a single input power. A small way to combat this is by biasing the transistor more towards the upper region where it can operate closer to class-A/AB. However, this is not an option in the DPA. As noted in Chapter 2, the main and peaking amplifier are biased in class-B and class-C respectively. As shown in the Fig.3.2 this is in the most detrimental area in terms of input capacitance non-linearity. This leads to unwanted effects in the AM/AM and AM/PM of the transistor.

The AM/AM and AM/PM can be described by taking a simple model of a transistor IMN and nonlinear capacitance as shown in Fig.3.3 and finding the relationship between V_{gs} and V_S [33]. $Z_S(\omega)$ represents the impedances presented by the IMN versus frequency, and $Z_L(\omega)$ is the impedances presented by the OMN to the drain.

The nonlinear input capacitance can be modeled by equation (3.1) and can be approximated as a truncated second order power series for simplicity.

$$C_{in} = C_{in} + C_{in}tanh(V_{gs}) \tag{3.1}$$

Figure 3.2: Input capacitance (Cgs) of 6-W GaN device.

Figure 3.3: Input capacitance (Cgs) of 6-W GaN device.

$$C_{in} = C_0 + C_1 V_{gs} + C_2 V_{gs}^2 \tag{3.2}$$

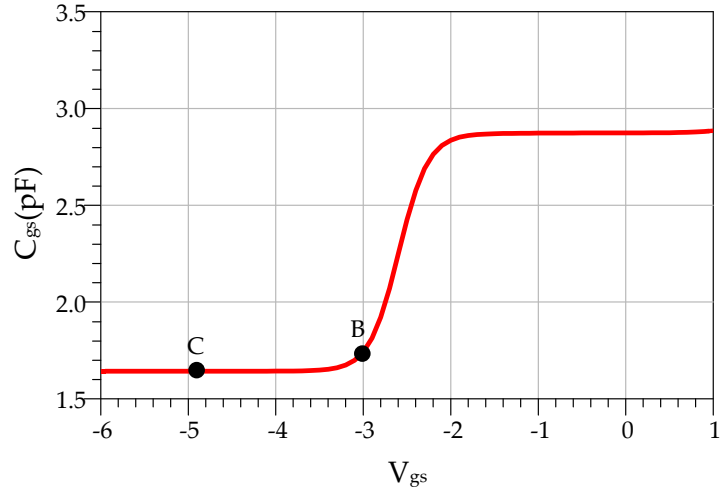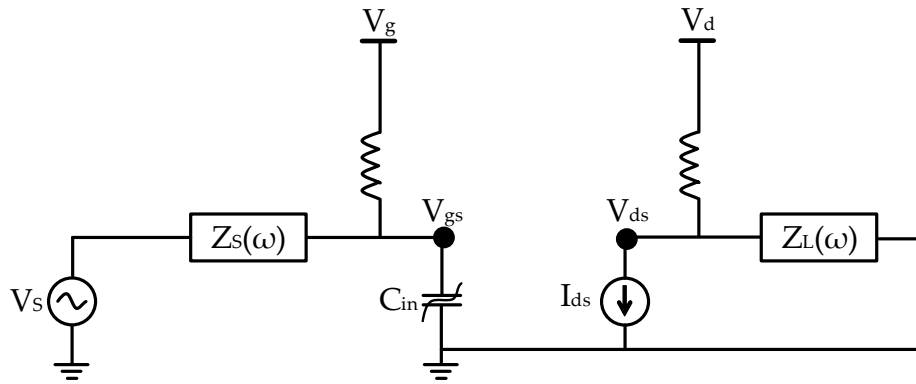By applying a single tone signal with an amplitude of V_S, the current through the capacitor can be found using the fundamental relationship of a capacitor in equation (3.3).

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$$i(t) = C_{in}\frac{dV_{gs}}{dt} \tag{3.3}$$

Substituting equation (3.2) into (3.3) yields (3.4).

$$i(t) = C_0\frac{dV_{gs}}{dt} + C_1 V_{gs}\frac{dV_{gs}}{dt} + C_1 V_{gs}^2\frac{dV_{gs}}{dt} \tag{3.4}$$

Assuming all harmonics are shorted by the IMN, the voltage at the gate is a magnitude/phase shifted version of the original input signal as represented by (3.5).

$$v_{gs} = V_0 + V_1 cos(\omega_0 t + \phi) \tag{3.5}$$

Substituting equation (3.5) into (3.4) and expanding, the fundamental current through the capacitor can be found as shown in (3.6).

$$\begin{aligned} i_1(t) = C_0\omega_0 V_1 sin(\omega_0 t + \phi) + C_1\omega_0 V_0 V_1 sin(\omega_0 t + \phi) \\ + C_2[\omega_0 V_0^2 V_1 sin(\omega_0 t + \phi) + 0.25\omega_0 V_1^3 sin(\omega_0 t + \phi)] \end{aligned} \tag{3.6}$$

The fundamental current in phasor notation can also be related to in the input voltage using equation (3.7).

$$I_1(\omega) = \frac{V_S(\omega) - V_1(\omega)}{Z_S(\omega)} \tag{3.7}$$

Transforming (3.6) into its phasor form and equating it to (3.7), the magnitude of the fundamental tone and phase can be found in terms of the input signal and the capacitance as shown in (3.8) - (3.9).

$$V_1 = V_S\sqrt{\frac{B_S^2(\omega_0) + G_S^2(\omega_0)}{C_0\omega_0 + C_1\omega_0 V_0 + C_2[\omega_0 V_0^2 + 0.25\omega_0 V_1^2] + B_S(\omega_0))^2 + G_S^2(\omega_0)}} \tag{3.8}$$

$$\phi = tan^{-1}\left(\frac{B_S(\omega_0)}{G_S(\omega_0)}\right) - tan^{-1}\left(\frac{C_0\omega_0 + C_1\omega_0 V_0 C_2[\omega_0 V_0^2 + 0.25\omega_0 V_1^2] + B_S(\omega_0)}{G(\omega_0)}\right) \tag{3.9}$$

As seen, the magnitude of the gate voltage is no longer just a function of the input voltage, but also of itself leading to a non-linear relationship. This is also the case with the phase of the voltage as well. This means that the gate voltage is significantly distorted version of the original due to the nonlinear capacitance, which can only be resonated out with a IMN for single frequency and bias point. This leads to unwanted AM/AM such as the slow compression exhibited in GaN transistors. In terms of AM/PM the non-linear capacitance also posses a much larger problem. Since the phase of the gate is already a distorted version of the input signal, the additional non-linearity caused by the current source and poor harmonic terminations exasperates the problem by the time a current is present at the drain. To combat this issue the the IMN network can be modified to sacrifice gain for better AM/PM. This AM/PM caused by the input capacitance also needs to be taken into account to a greater extent when talking about PA topologies which use multiple transistors such as the DPA. The DPA as mentioned in Chapter 2 uses current injection to modify the impedances presented to each transistor. Also at peak power the DPA can be considered a power combiner. This means that a significant AM/PM from either the main or peaking transistor will result in poor linearity or efficiency.

In general a good approach to make sure further or less dependence on the non-linear capacitance is seen is to short circuit the harmonics. However, as previously noted this becomes much more difficult when trying to be accomplished for wideband designs where a perfect short is not realizable over the BW. As well, with larger transistors it becomes more difficult to present a harmonic short at the intrisnic gate even over a narrowband due to the extrinsic parasitics present in the package and device. This leads to a significant impact on the design considerations of the IMN and power divider for the DPA which now need to be matched upto the second harmonic. This leads to the question of how and what impedances should be presented to the gate of the transistor if a harmonic short is not achievable, and how much this effects the overall operation of the PA.

3.2   Second Harmonic Case Study

In this section a case study will be presented to demonstrate the sensitivity of the main and peaking amplifier in the DPA to the 2nd harmonic termination presented at the input of the transistor.

3.2.1 Class-AB Power Amplifier Second Harmonic Sensitivity

To see the effects of the second harmonic source termination on the main transistor in the DPA, a 6-W GaN HEMT transistor is biased in class-AB with a source and load network. The output load network presents the ideal load impedance, R_{opt}, and the all output harmonics are perfectly shorted to see only the effect of the input non-linearity. On the input side the fundamental source impedance is also set to its ideal value. A schematic of this setup is shown in Fig.3.4.
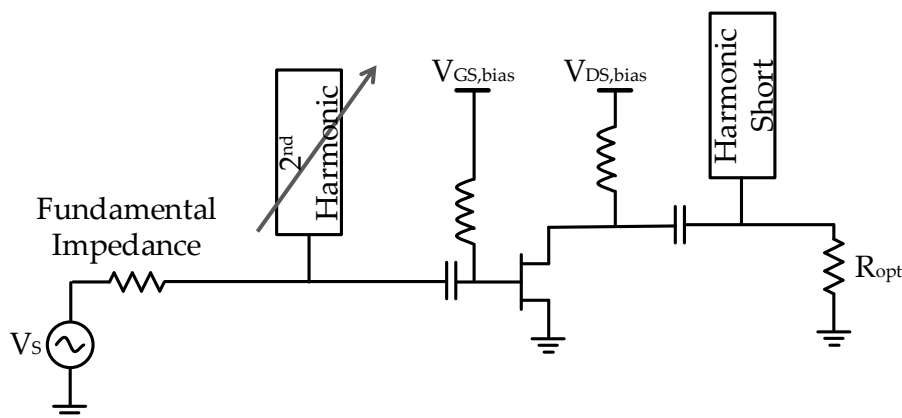
Figure 3.4: Second harmonic source pull setup.

Sweeping the second harmonic source impedance at 3GHz, the results are presented in Fig.3.5. The plot shows the PAE contours (red) in 4% increments and output power contours (blue) in 0.5dBm increments over the entire Smith. As is seen the second harmonic impedance varies the potential PAE significantly, with almost a 20% degradation over the entire Smith chart. However, the output power decreases very minimally, with only a variance of 0.5dBm across the Smith chart.

Looking at the voltage and current waveforms presented in Fig.3.6 at the intrinsic gate and drain respectively for two different 2nd harmonic terminations, a clearer picture is seen. The red curves represent a good 2nd harmonic termination whereas the blue curves represent a bad 2nd harmonic termination. The second harmonic content resulting from the improper termination at the intrinsic gate has changed the conduction angle and operating condition of the transistor. This has a direct impact on the efficiency and linearity of the Class-AB amplifier as shown in Fig.3.7. Fig.3.7(a) shows that the drain efficiency has
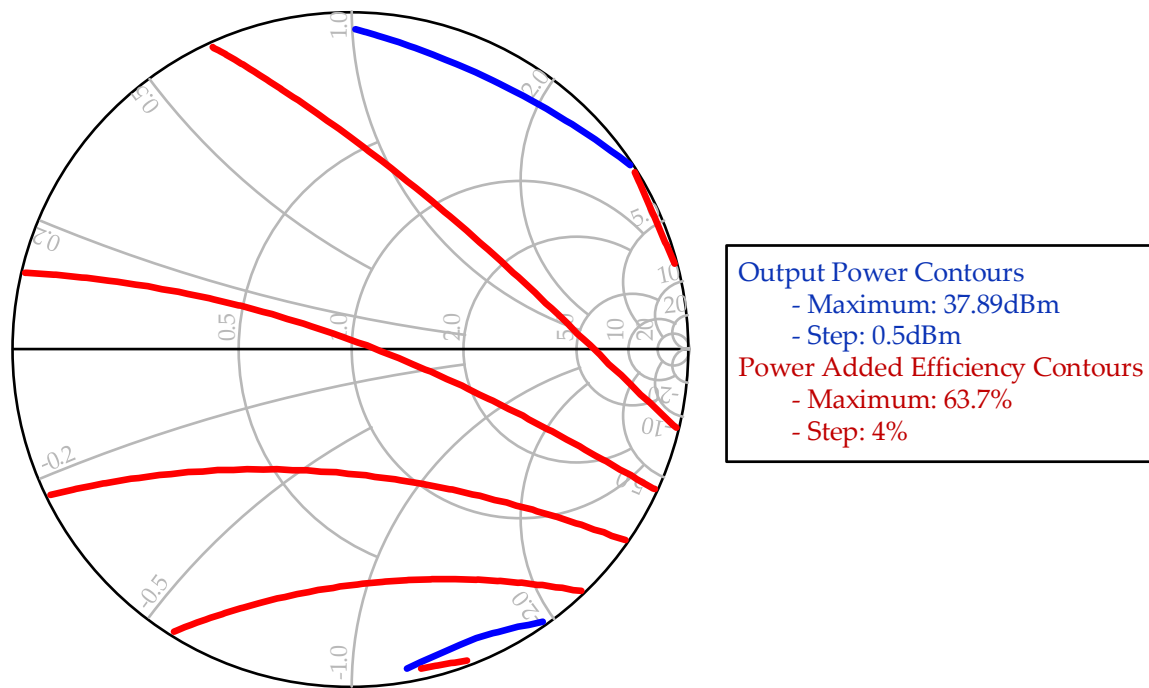
Figure 3.5: Second harmonic source pull on 6-W GaN transistor biased in class-AB at 3GHz.

decreased by over 10%. As well, Fig.3.7(b) shows that the AM/AM profile of the resulting PA has a been impacted as well, even though the small signal and large signal values remain the same. The plot shows that the compression in the AM/AM is much slower for the poor second harmonic termination. This is much harder to linearize using a standard digital pre-distortion (DPD) setup, since even as the PA is backed off from peak power, it is still operating non-linearly.

Conducting the same study at higher frequencies shows why it is much harder to design broadband amplifiers at higher frequencies. In Fig.3.8 a second harmonic source pull is conducted at 5GHz using the same setup. It shows that the PA is now even more sensitive to the second harmonic termination at the input. Again, the output power barely is effected, however, the PAE varies by over 20% across the Smith chart. Note that the concentration of the PAE curves around the optimal point at the edge of the Smith chart. This means a small mismatch can result in a large deviation in the efficiency of the PA, moving it
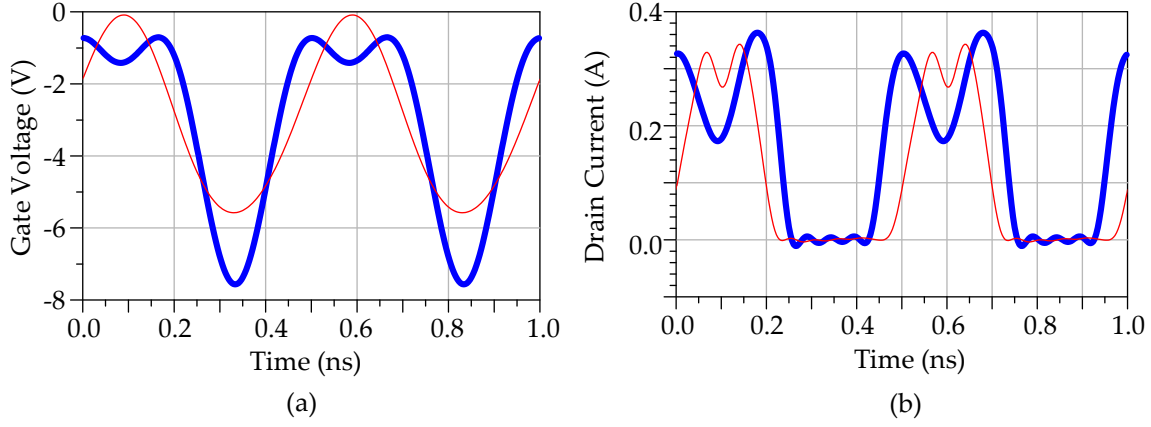
Figure 3.6: Waveforms of (a) gate voltage, and (b) drain current of class-AB amplifier for two different harmonic terminations, one good (red), and one bad (blue).
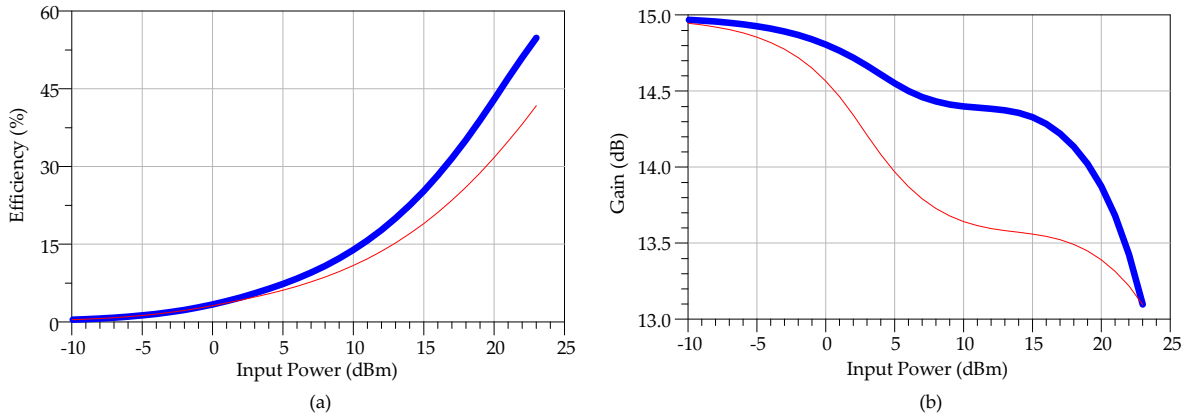
Figure 3.7: (a) Drain efficiency and (b) AM/AM versus input power for two different second harmonic terminations, one good (blue), one bad (red)

from a region of high efficiency to one of low. As well when thinking about designs that span an octave of BW, the second harmonic termination is of utmost importance as the second harmonic of the lower band is the fundamental of the higher band. Finally, it is

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important to note that these results are independent of the fundamental impedance at the input. Thus the second harmonic termination and fundamental impedance can be chosen independently in the design process.
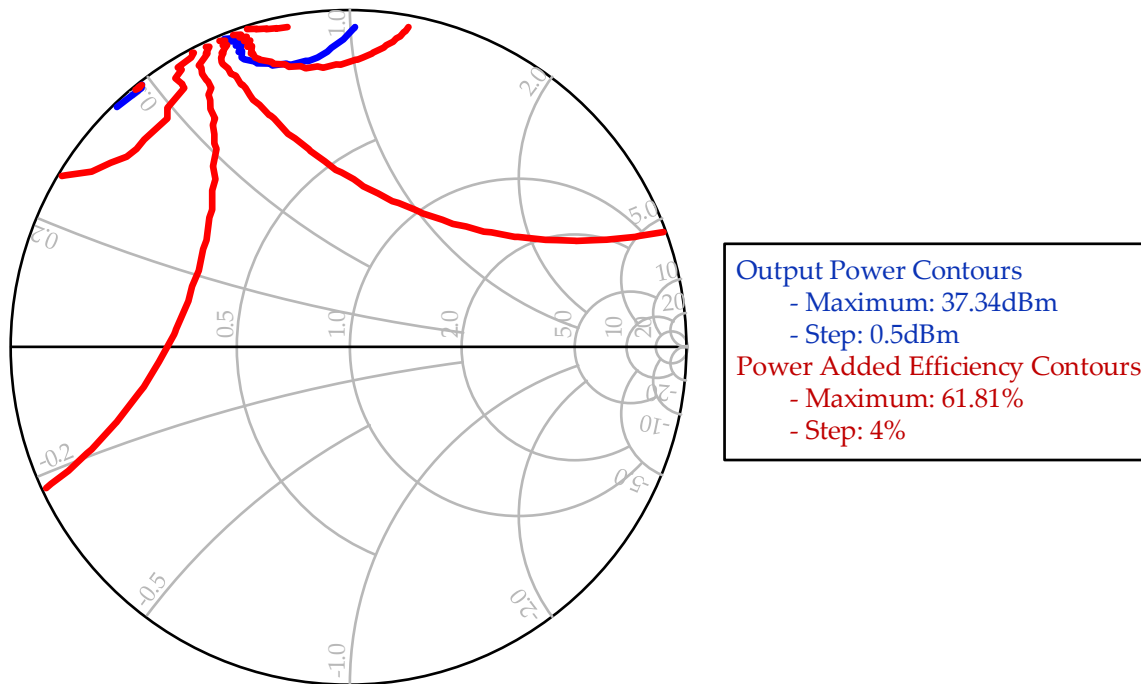
Figure 3.8: Second harmonic source pull on 6-W GaN transistor biased in class-AB at 5GHz.

3.2.2 Class-C Power Amplifier Second Harmonic Sensitivity

As was done the with main, transistor above, a harmonic study was conducted on a class-C amplifier, the exact operating point for an auxiliary transistor in the DPA. The study shows why Doherty operation isn't always achieved across the designed band when implementing an IMN for gain, which does not look at how the PA operates versus input power. In Fig.3.9 the same 2nd harmonic source pull conducted on the class-AB is conducted on the class-C at 3GHz. Notice, that as was seen with the class-AB, the PAE varies significantly across the entire Smith chart, losing upwards of 15%. However, now the power also varies

across the Smith chart, varying upwards of 1.5dB over the Smith chart. This however, only represents what is happening at peak power levels. Looking at Fig. 3.10 it is shown how the fundamental current varies versus input drive for two different second harmonic terminations. Notice how not only is the peak current different which is related to output power, but even the back-off current level varies for different terminations. This means that at back-off improper current injection can take place for the DPA leading to sub-optimal results. This is a noticeable problem when looking at design methodologies in place for DPA structures currently, which only take into account the gain of the class-C (peak output current) and biasing. The effects of this improper current injection are more thoroughly outlined in the next section and a new novel concept is introduced to help with the design of the IMN for a DPA to ensure that the proper current profiles are maintained across frequency.
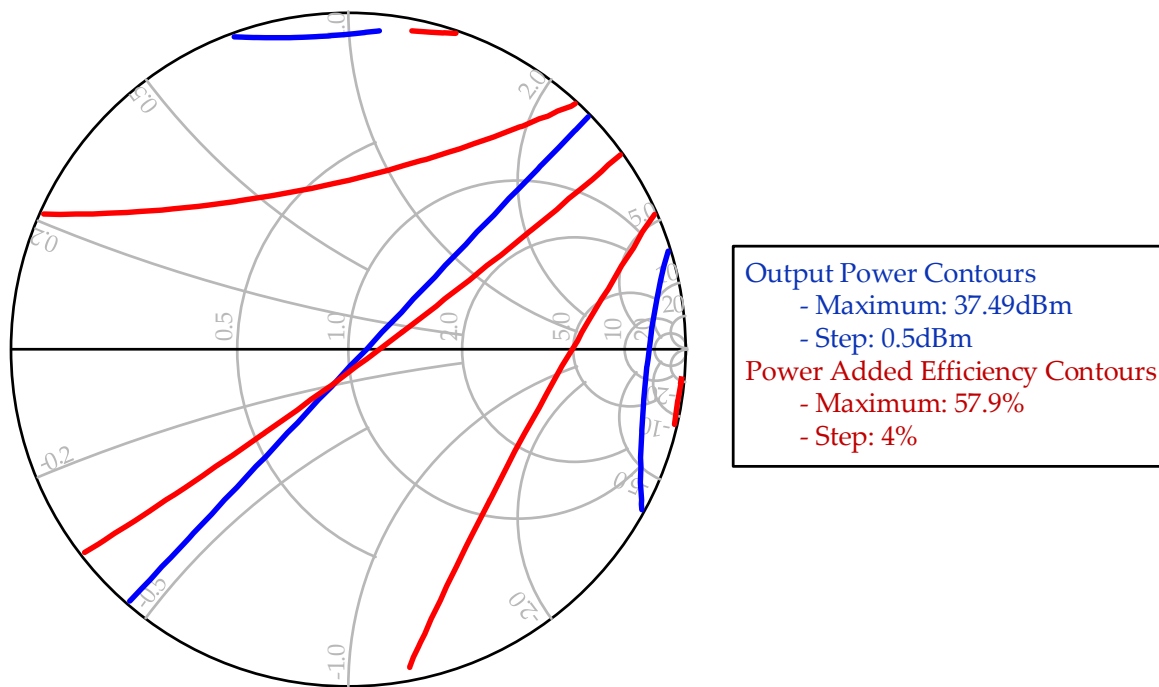

Figure 3.9: Second harmonic source pull on 6-W GaN transistor biased in class-C at 3GHz.
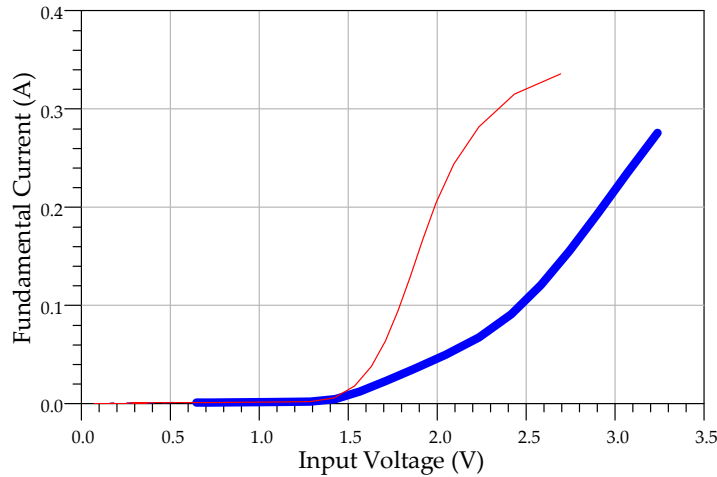
Figure 3.10: The fundamental current versus input drive for two different 2nd harmonic terminations.

3.3 Current Contours and Design Methodology

3.3.1 Doherty Power Amplifier Current Injection

As mentioned in Chapter 2, two key components dictate the operation of the DPA, the OCN which realizes the correct impedances, and the current injection which facilitates the load modulation. Deviating from these significantly alters the performance of the DPA. Fig.3.11 shows a series of current profiles for the main and peaking transistor, where the peaking transistor is turning on too late or too early and Fig.3.12 shows the corresponding results. In the case where the peaking amplifier turns on too early, the load presented to the main PA starts to decrease before the maximum swing is achieved. This causes the DPA efficiency to decrease at BO and peak output power. The linearity however remains unchanged since the transistor is not swinging into the knee region. When the transistor turns on to late the main transistor begins to saturate resulting in the gain starting to compress during the Doherty region.

Fig.3.13 shows the current profiles for the main and peaking transistor when they do not align at peak powers, with the corresponding efficiency and gain displayed in Fig.3.14. When the peaking transistor delivers to little current (or the main transistor too much), the linearity of the DPA is effected. The impedance presented to the main transistor is
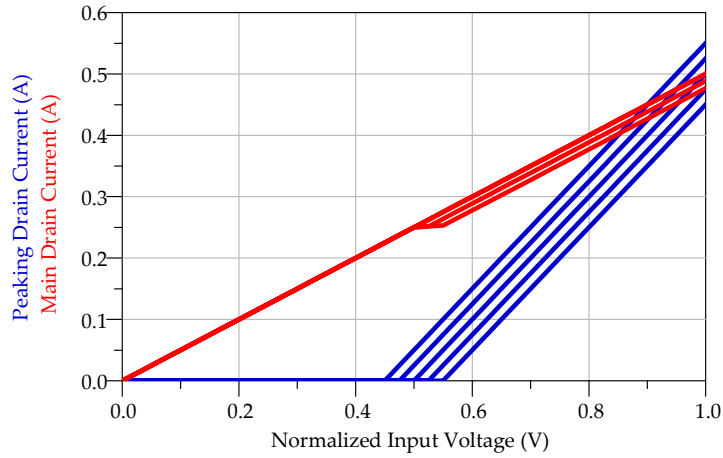
Figure 3.11: Main (red) and peaking (blue) drain currents for various turn on points of the peaking amplifier
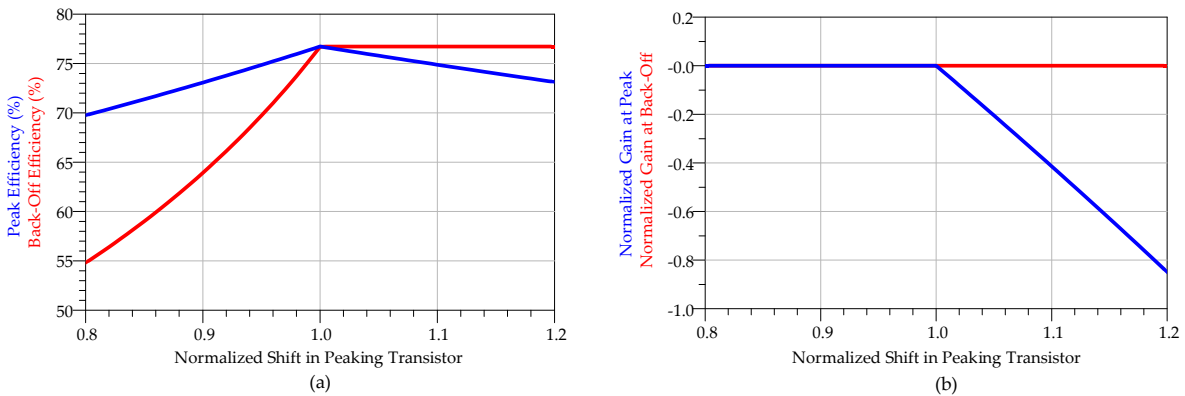
Figure 3.12: (a) Efficiency and (b) gain results at peak and 6dB-BO versus normalized shift in the turn-on point for the peaking transistor.

too high, causing the output voltage swing to go into the knee region. When the peaking transistor provides too much current at peak power (or the main transistor too little) the linearity remains in tact, however the efficiency decreases as shown.

All these results were presented with an ideal output matching network, such that the
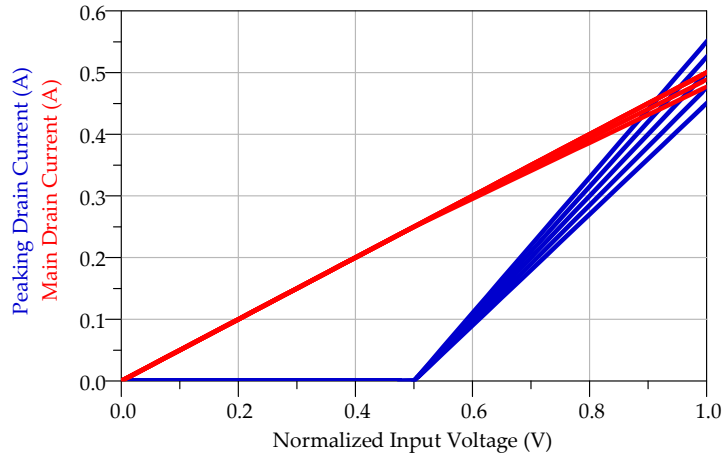
Figure 3.13: Main (red) and peaking (blue) drain currents for various peak values for the peaking amplifier.
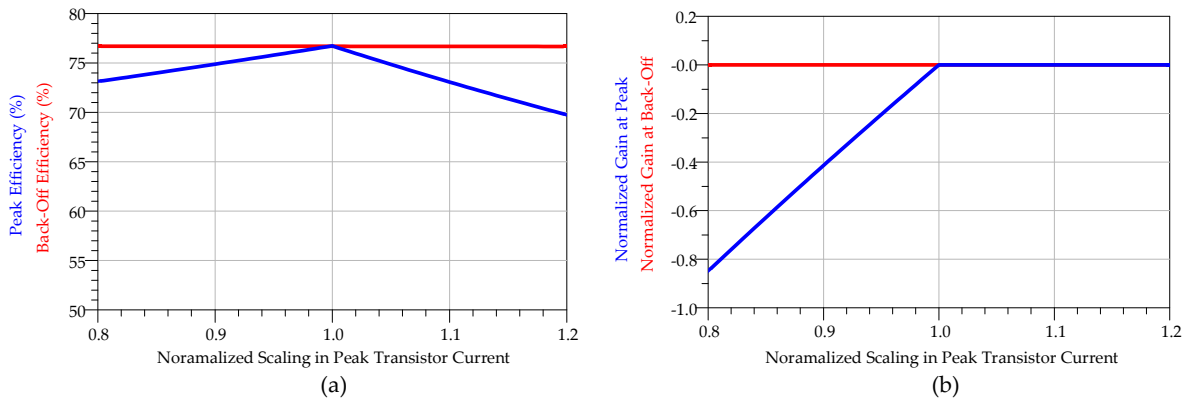
Figure 3.14: (a) Efficiency and (b) gain results at peak and 6dB-BO versus normalized scaling in the peaking transistor maximum current.

phase was always aligned and the ideal impedance values for the matching network was used. This shows that if the proper currents aren't supplied to the network, the DPA operation breaks down resulting in sub-optimal results. The currents however, can be controlled independently from the OCN in the ideal case by adjusting the IMN of each

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transistor. In the next section a method will be introduced to adjust the currents.

3.3.2   Constant Current Contours

As mentioned in the above sections the currents play an integral role in the operation of the DPA. The current profiles are strictly dictated by the input side, and can severely affect the operation of the DPA. As well, it was determined that the input second harmonic can severely affect the performance. For this reason a design methodology is needed to make sure that the proper currents are available and the proper harmonic impedances are presented.

The design methodology introduced here is the current contour. Current contours are very similar to other contours plotted during the design of a PA as part of a load pull or source pull measurement. In the classical case, source pull may be conducted and output power contours would be plotted for large signal operation. From here the proper input impedance can be determined for highest possible gain. This however, as noted above does not properly define the current needed for the DPA operation.

Current contours are the locus of points on the smith chart that create the same fundamental drain current at a given frequency for a power level. They allow the designer to carefully dictate the performance of the PA by mapping current presented by each transistor at the drain to the input impedance shown at the gate. In the simulation procedure a PA is first biased (although this can be varied to increase the range of operation) and terminated by its optimal impedance. This consists of R_{opt} for the fundamental and short circuit for the harmonics. The input harmonics can also be shorted for this scenario and can be dealt with later in the design process as detailed in the procedure provided in the next section.

An example of a current contour is shown in Fig. 3.15(a) along with its accompanying fundamental current plot versus input power in Fig. 3.15(b). The current contour displays the fundamental source impedances that will provide the designated fundamental drain current at the output for a specified input drive. In the DPA, for class-AB operation the designer is concerned with peak current, as the transistor will be on when RF power is applied. This resulting contour is refereed to as the high power constant current contour, or $I_{m,h}$ for the main amplifier. The $I_{m,h}$ contour shows the minimum acceptable current required at peak power. Any impedance inside the circle will provide more current, while outside the circle will provide less. In most cases a range is chosen, roughly within 10%-15% of peak current, to make the matching networks more realizable.
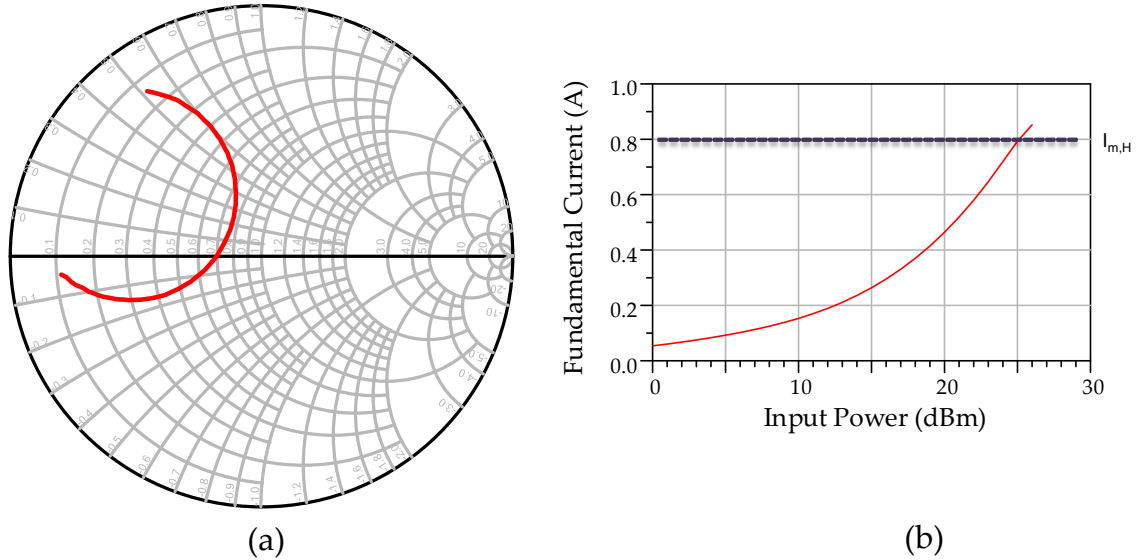
Figure 3.15: (a) High power current contour plot and (b) accompanying look at fundamental current versus input drive.

As mentioned the $I_{m,h}$ current contour can be used for peak power for the class-AB amplifier design in a DPA. Similarly, it can also be used for the design of the peak current for a class-C amplifier as well, in this case called the $I_{p,h}$ current contour. However, as mentioned, the turn on point for the class-C amplifier is also critical in the operation of the DPA to maintain correct load modulation. As such, a way to make sure the the transistor is turning on at the back-off point is required. For this reason in the design of the class-C amplifier the low power constant current contour is also needed, $I_{p,l}$. The $I_{p,l}$ current contour allows the designer to carefully dictate the operation of the class-C amplifier in back-off.

In Fig. 3.16 a typical Smith chart is shown displaying the two current contours for a class-C amplifier, along with the fundamental current versus input drive plot. The red contour represents the $I_{p,h}$ current contour, and the blue the $I_{p,l}$ current contour. The $I_{p,l}$ contour represents the maximum allowed current at back-off. Ideally this is zero, however over a large frequency band this is tough with realizable matching networks. As such, a suitable range is selected, this is roughly 10%-15% of the peak current. Looking at the Smith chart, anything inside the circle means too much current is present at the drain,

and any impedance on the outside of the blue circle represents the good region (less than the maximum amount of current). This forms an acceptable design space between the $I_{p,h}$ and $I_{p,l}$ contours as shown by the checkered region.
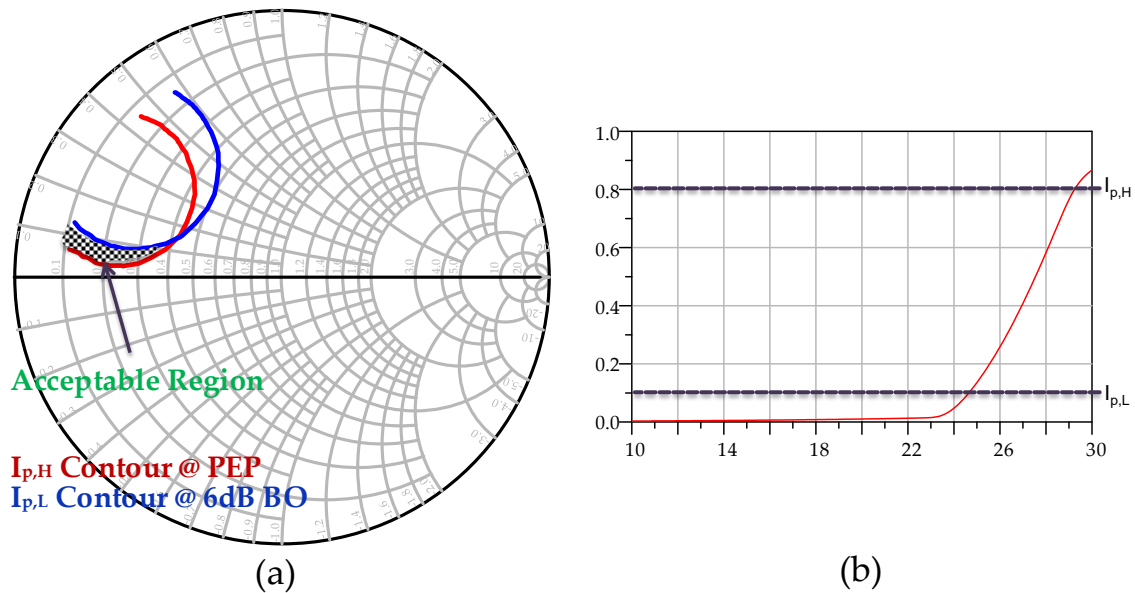
Figure 3.16: (a) High power and low power current contour plot and (b) accompanying look at fundamental current versus input drive for peaking transistor.

3.3.3 Application of Class-AB and Class-C Current Contour Based Design Methodology

Now having established a tool that can be used to carefully dictate the currents, and having knowledge of the effects of the second harmonic on the overall performance, a simple design methodology can be developed for the class-AB and class-C amplifier. The steps for the design of the class-AB amplifier are as follows.

1. Terminate the output with its ideal load. This includes shorting the harmonics at the output and input.

2. Using fundamental source-pull, plot constant $I_{m,h}$ contours (required current at full power) over the target frequency band. It's important to note that the circles usually shrink as the frequency increases. As well, the circles move in a counter-clockwise (CCW) direction. This means there is a limit on the gain of the PA beyond which no IMN is realizable over the target band.

3. With the current contours plotted, determine a realizable impedance profile (clockwise direction, etc.) for $Z_s(f_o)$ moving from the lower frequencies to higher frequencies.

4. Now overlaying the second harmonic source pull results on the same smith chart continue the impedance profile, extending it all the way upto the second harmonic frequency of the highest band, $Z_s(2f_o)$. By avoiding the sensitive regions or areas with low efficiency, the performance of the PA can be maintained close to peak.

5. Use circuit synthesis methods such as simple real frequency technique (SRFT), filter theory, etc. to realize the impedance profile.

Following this design methodology yields a class-AB amplifier with flat gain versus frequency which is equivalent to having a flat peak fundamental current. A similar design methodology can be followed for the class-C amplifier as well, with added need for the low power constant current contour for back-off operation. This procedure is detailed in the steps below.

1. Terminate the output with its ideal load. This includes shorting the harmonics at the output and input. At this point the designer can also start with an initial biasing for V_{GS}.

2. Using fundamental source-pull, plot constant $I_{p,h}$ contours (required current at full power) and the $I_{p,l}$ contours (maximum current allowed at BO) over the target frequency range.

3. Designate the areas where the $I_{p,h}$ and $I_{p,l}$ contours overlap. This design space can be increased by varying the biasing of the transistor depending on whether the low power or high power operation contours need to be adjusted. By biasing the transistor higher, the high power contour design space increases (larger gain for transistors operating closer to class-A). By decreasing the biasing, the low power contour design space is increased.

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4. Determine a realizable impedance profile for $Z_s(f_o)$ moving from the lower frequencies to higher frequencies through the designated overlapping areas.

5. Now overlaying the second harmonic source pull results on the same smith chart continue the impedance profile, extending it all the way upto the second harmonic frequency of the highest band, $Z_s(2f_o)$, while avoiding areas of low efficiency.

6. Use a circuit synthesis method such as SRFT or filter theory to realize the impedance profile.

Following this design methodology yields a class-C amplifier with flat gain versus frequency, and makes sure the current yields a linear profile. This design methodology also combats the frequency dependent turn-on seen in III-V semiconductor transistors such as GaN.

Chapter 4

Wideband Doherty Power Amplifier Design and Measurement Results

In this section the design of a broadband DPA is shown using current contours and the design methodology introduced in the previous Chapter. Details and simulation results are provided for the IMN and OCN of the DPA. At the end of the chapter measurement results are provided on the fabricated DPA.

4.1   Doherty Power Amplifier Implementation

In order to validate the proposed design methodology, a broadband DPA prototype was designed using two 6-W 0.25μm packaged GaN HEMT transistors from Cree for both the main and peaking transistors. Symmetrical devices were used to increase the PUF of the overall design as the proper sizing ratio was not available in the chosen offering. This in turn reduced the maximum gain of the overall PA by 3dB and proper splitting was accounted for by using the current contours so that a symmetric Wilkinson power divider can be used at the input, which can be designed to be much more broadband in comparison to a assymetric power divider. The targeted frequency band was $3.0 - 5.0$GHz to push the envelope for high power DPA designs in terms of frequency. As well, it was mentioned in passing in the previous sections that the design of the DPA becomes much harder when the frequency is increased, as the potential design space using current contours shrinks. By designing at higher frequencies the importance of current contours are more clearly outlined.

4.1.1 Input Matching Network

The IMN for both the main and peaking transistor was designed using the methodology proposed in the previous section. To obtain as high an efficiency as possible the transistor was biased in very deep class-AB. Plotting the current contours from 3.0 to 5.0GHz results in Fig.4.1. As can be seen the contours, red, move in the CCW direction and become smaller as the frequency is increased. An impedance profile is constructed and extended upto the second harmonic as seen by the black trace.
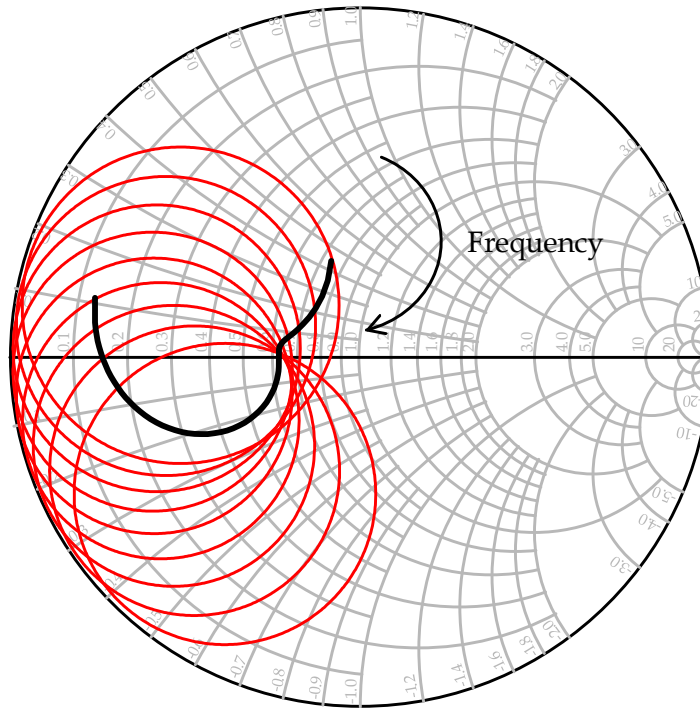

Figure 4.1: High power constant current contours (red) for main amplifier with accompanying impedance profile (black) needed upto $Z_s(2f_0)$.

The impedance versus frequency were tabulated and an IMN topology was constructed using SRFT. A final realization of this circuit was found using transmission lines (TL) and series capacitors by converting the SRFT lumped component model. The final results from the IMN are shown in Fig.4.2 and Fig.4.3. Fig.4.2 shows that currents line up nicely over

the enture frequency range, this results in good DE seen in Fig.4.3(a) and constant gain as seen in Fig.4.3(b).
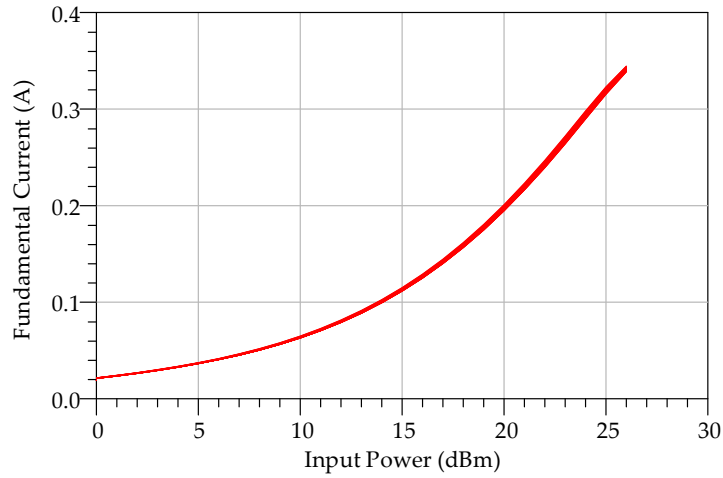

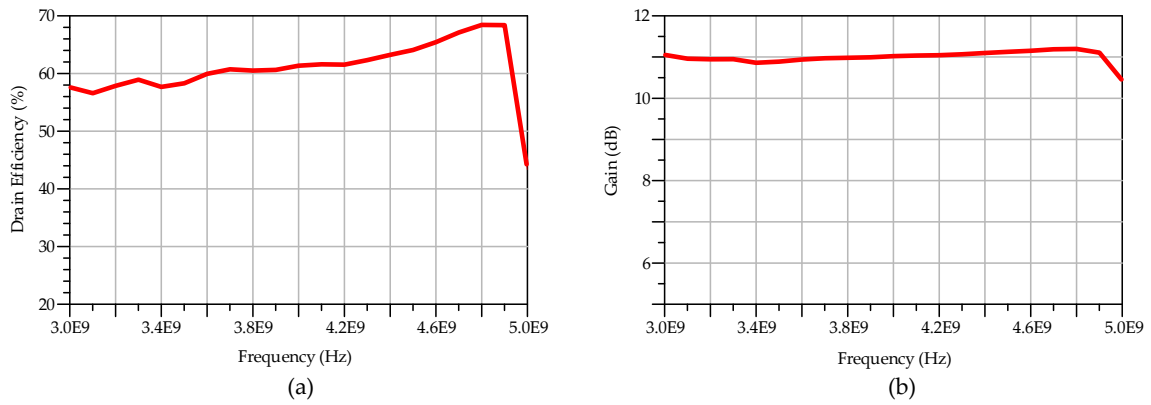Figure 4.2: Class-AB fundamental current versus input power after using design methodology.

Figure 4.3: Class-AB amplifier (a) DE and (b) gain after designing IMN using constant current contours.

For the peaking transistor, both the high and low power current contours were plotted as shown in Fig.4.4. To increase the low power current contour area, the transistor was biased further away from the turn-on point. As well, the stability network was added at the end of the design to allow for more a broader design space which was not needed for the class-AB. The Smith chart shows the overlap regions for three frequencies (3, 4, 5GHz) with the final resulting impedance profile highlighted in black. SRFT was used to realize the impedance profile and then transformed to a TL structure.
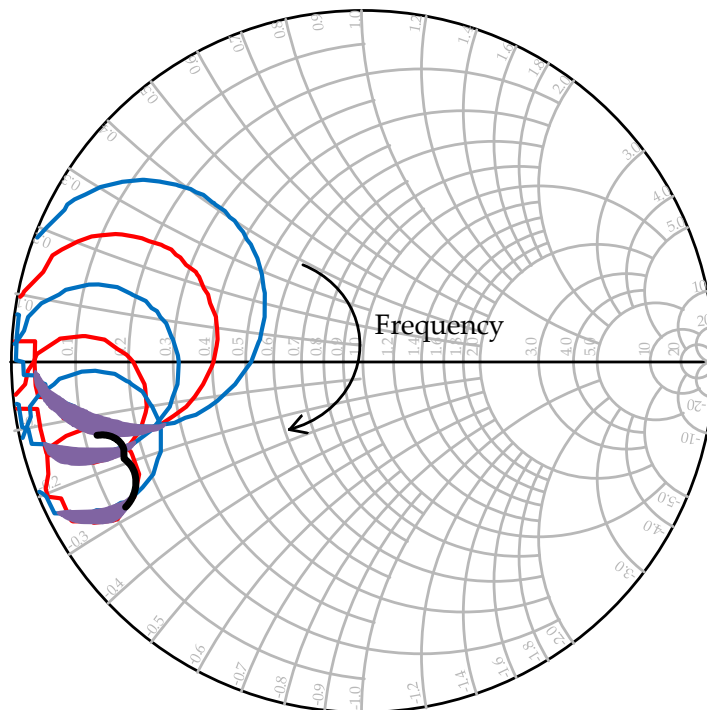
Figure 4.4: High power constant current contours (red) and low power constant current contours (blue) for peaking amplifier. The accompanying impedance profile (black) is shown going through the overlapping regions (purple).

The final results for the class-C current profile is shown in Fig.4.5 and the gain shown in Fig.4.6. As can be seen the peaking amplifier has a very similar turn-on point versus frequency and delivers a relatively flat current at peak resulting in a gain with only 0.5dB of deviation versus frequency.

Figure 4.5: Class-C fundamental current versus input power after using design methodology.
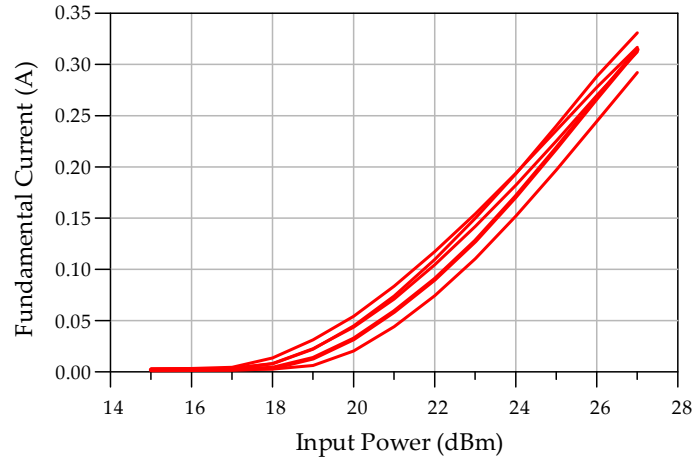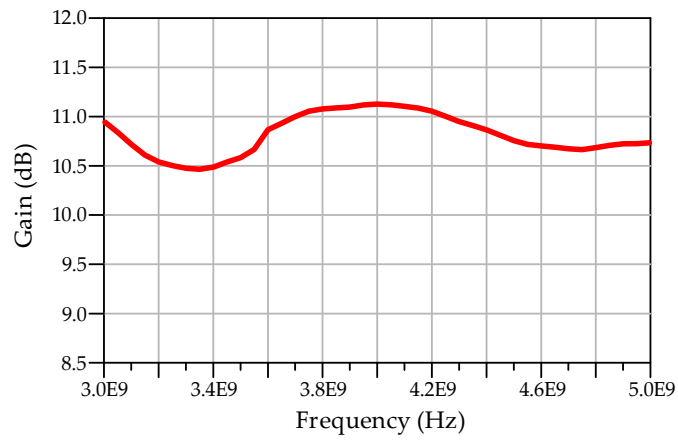

Figure 4.6: Class-C gain after designing IMN using constant current contours.

4.1.2 Output Matching Network

The OMN of the DPA was realized using transmission lines and load pull results. Conducting load pull, it was seen that the optimal characteristic impedance needed for the TL using conventional DPA theory would be 100Ω. This however is difficult to manufacture without moving to very high dielectric constant or thick substrates. This is a common problem for low power devices. To combat this issue, a transformation was used to convert the single stub line into a T-line as shown in Fig.4.7.
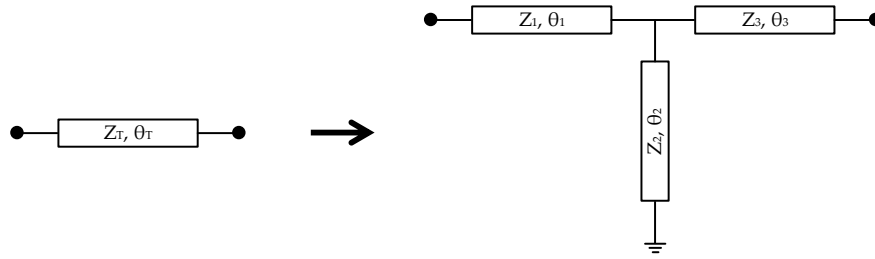
Figure 4.7: The transformation from a single TL to a T-line structure.

ABCD parameters of a single TL were matched to the T-Line to determine the new characteristic impedances and phases needed for each of the lines. The ABCD parameters can be seen in equations (4.1) - (4.5).

$$ABCD_T = \begin{bmatrix} cos(\theta_T) & jZ_T sin(\theta_T) \\ \frac{jsin(\theta_T)}{Z_T} & cos(\theta_T) \end{bmatrix} \tag{4.1}$$

$$ABCD_1 = \begin{bmatrix} cos(\theta_1) & jZ_1 sin(\theta_1) \\ \frac{jsin(\theta_1)}{Z_1} & cos(\theta_1) \end{bmatrix} \tag{4.2}$$

$$ABCD_2 = \begin{bmatrix} 1 & 0 \\ \frac{1}{jZ_2 tan(\theta_2)} & 1 \end{bmatrix} \tag{4.3}$$

$$ABCD_3 = \begin{bmatrix} cos(\theta_3) & jZ_3 sin(\theta_3) \\ \frac{jsin(\theta_3)}{Z_3} & cos(\theta_3) \end{bmatrix} \tag{4.4}$$

$$ABCD_T = ABCD_1 ABCD_2 ABCD_3 \tag{4.5}$$

By equating the ABCD parameters a design space is now available for the selection of the parameters in the T-line. By setting the characteristic impedances to much more realizable values depending on the chosen substrate the phases can be adjusted. This transformation also provides an added benefit for biasing. As can be seen in the Fig.4.7, the T-Line has a short circuited stub. This can be used as a DC feed. As well, by analyzing the design space, the characteristic impedance can be chosen to reduce the baseband impedance of the design. In many designs, a high impedance line is used for biasing close to the drain of the transistors to avoid disturbing the RF operation of the DPA. This line however along with the DC blocks creates a resonance at baseband which modulates the supply voltage when under CA signals.

4.1.3   Simulation Results

Once the IMN and OCN was completed, the system was connected together to form the DPA. However, it was seen that the currents had shifted significantly from the designed values with the resulting profiles shown in Fig.4.8. This is do to the non-negligible C_{gd} as designs move to higher frequencies. To take this into account an iterative approach needs to be taken whereby the input and output are designed in conjunction. By doing so the current profiles can be properly maintained in the design resulting in good load modulation and proper DPA operation. The current profiles from the resulting design are shown in Fig.4.9. Note that over the frequency band 3.0-4.8GHz the current profiles are maintained within the required limits. At the upper and lower edges the profiles start to falter limiting the potential BW.

Fig. 4.10 shows the simulated results of the designed DPA for efficiency (both back-off and peak) and peak power versus frequency. Note that good performance is achieved from 3.0-4.8GHz, or 46% BW. Over this range a peak and BO efficiency of over 40% was achieved over the entire operating range. As well, the output power was greater than 39.7dBm. The gain and efficiency versus input power is shown in Fig.4.11. The gain is greater than 9dB and shows a minimal amount of compression at peak power across the band. Looking at efficiency note that the BO efficiency is close to the peak power efficiency. This shows that DPA behavior is maintained over the BW, with a near flat efficiency seen over the Doherty operation.
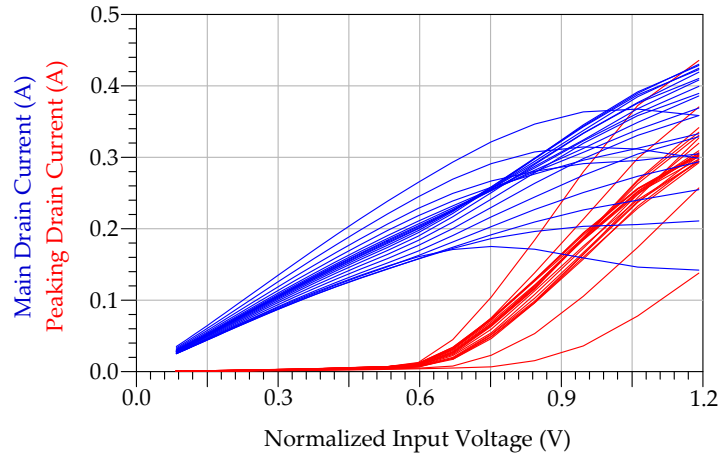
Figure 4.8: DPA current profiles after connecting the two PAs togeather. The blue profile represents the fundamental current for the main over the frequency range, while the red presents the fundamental current of the peaking.
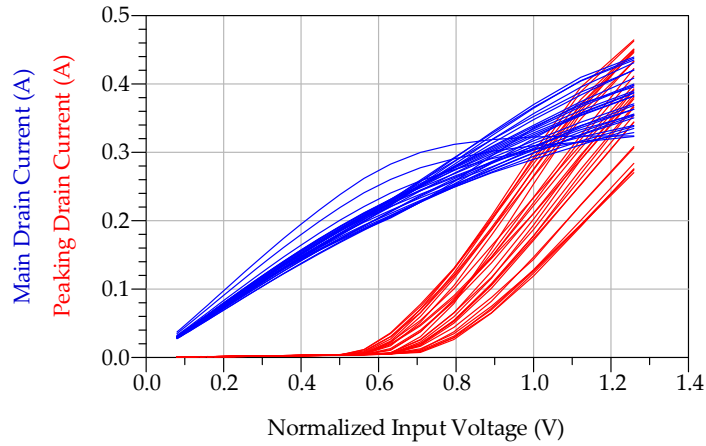

Figure 4.9: DPA current profiles after designing using an iterative approach. The blue profile represents the fundamental current for the main over the frequency range, while the red presents the fundamental current of the peaking.
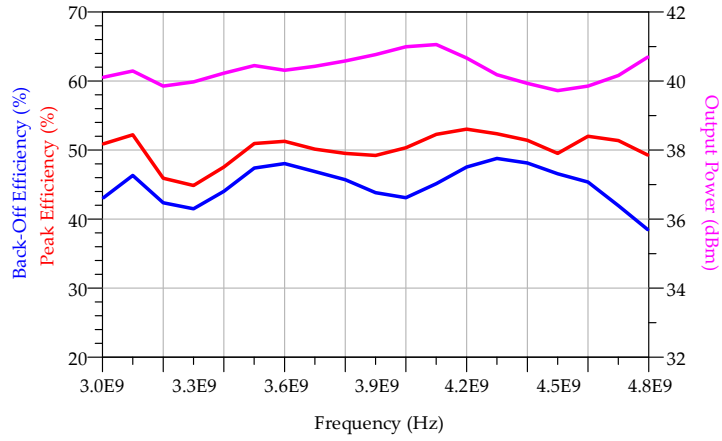
Figure 4.10: Simulated efficiency and output power versus frequency.
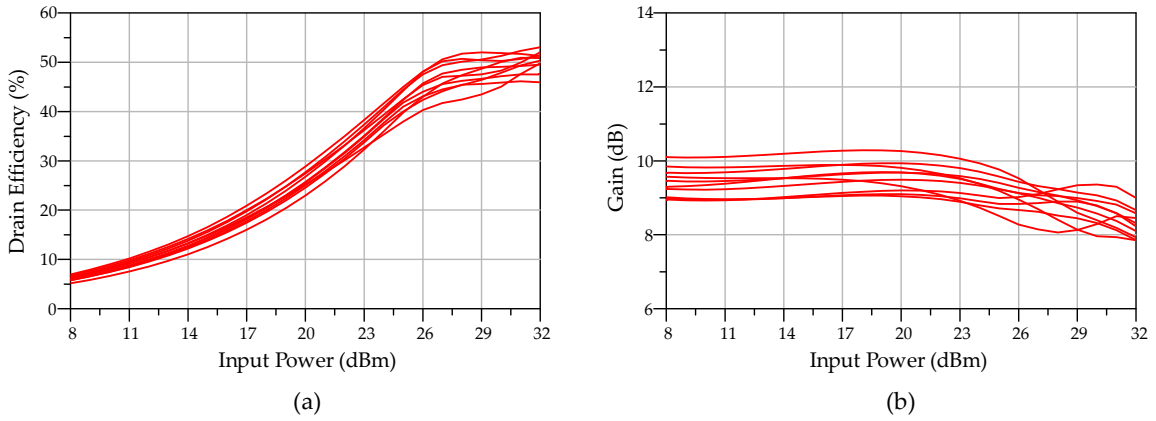

Figure 4.11: Simulated (a) DE and (b) gain versus input power for the DPA.

4.2 Measurement Results

To validate the simulation results the DPA was fabricated on a Rogers RT/Duroid 6006 75mil thick substrate and assembled in house. A picture of the assembled prototype is shown in Fig.4.12. The short circuit stubs as mentioned above have been used as access

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points to bias the transistor, with a single supply needed for both the main and peaking.
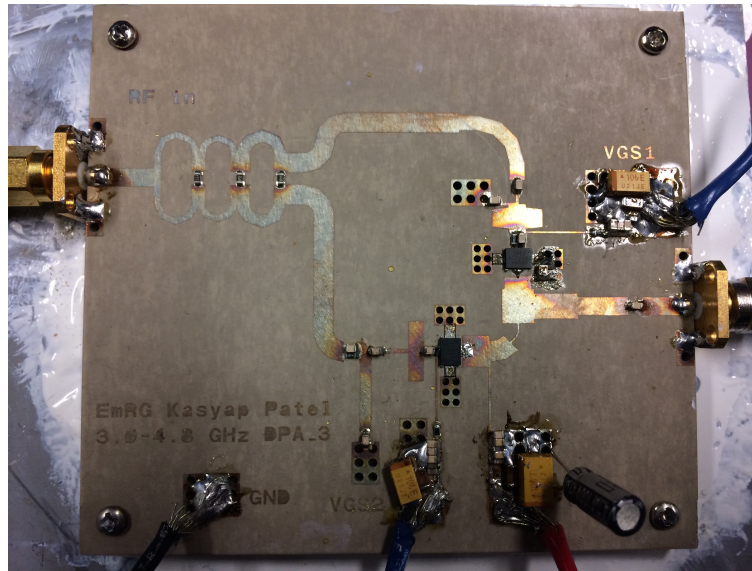

Figure 4.12: Fabricated DPA using proposed design methodology.

The performance of the DPA was measured under two setups, a continuous wave (CW) and modulated signal. Fig.4.13 shows the measured AM/AM for the DPA while Fig.4.14 shows the efficiency versus input drive at various frequencies. As can be seen, the DPA shows significant compression at certain frequencies in comparison to the simulated data and the efficiency has dropped by roughly 6%. This is due to the nature of the package for the 0.25μm GaN device which utilizes a plastic package in comparison to conventional GaN devices which include a large flange at the source for thermal dissipation. To gain more accurate results, a pulsed measurement setup is being worked on to mitigate the thermal effects.

Fig.4.15 shows a clearer visual of the peak efficiency and efficiency at 6dB BO versus frequency. The DE in both cases remains greater than 37% from from 2.7-4.7GHz. Fig.4.16 shows the gain and peak output power versus frequency. The DPA maintains an output power greater than 39.7dBm and gain greater than 8dB within the band.

To validate the linearity and linearizability of the DPA modulated signal measurements were conducted using a single-band LTE and WCDMA signal. Fig.4.17 and Fig.4.18 shows the measured spectrum of the DPA before and after lineaization for a 20MHz 1001 WCDA signal with 7.2dB PAPR at 3.3GHz and 4.1GHz respectively. The amplifier was able to
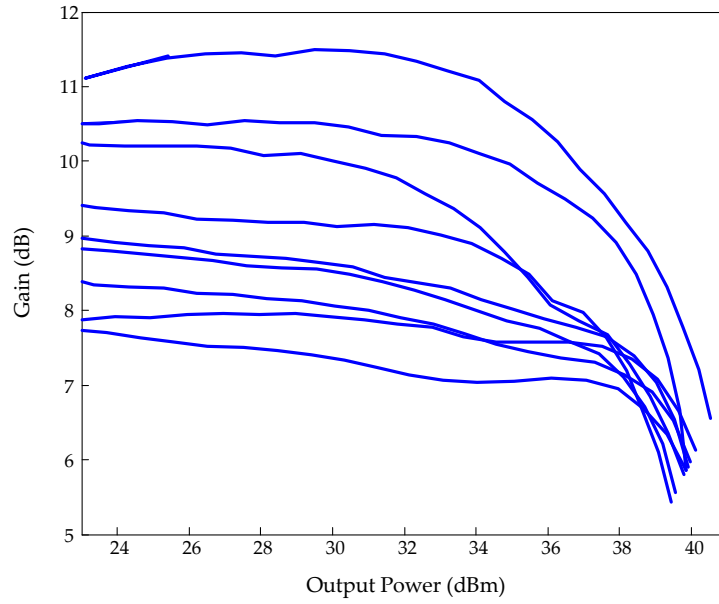
Figure 4.13: Measured CW gain of PA versus output power.

achieve a maximum adjacent channel leakage ratio (ACLR) of 33dBc/Hz before DPD and 51dBc/Hz after DPD. The average output power was 32.3dBm and DE was 34%.

In Fig.4.19 the output spectrum is shown when the PA is excited with a 80MHz signal at 3.3GHz with a PAPR of 9.4dB. The average output power was 30.4dBm and average DE was 24The ACLR before DPD was 37dBc/Hz and 48dBc/Hz after DPD.
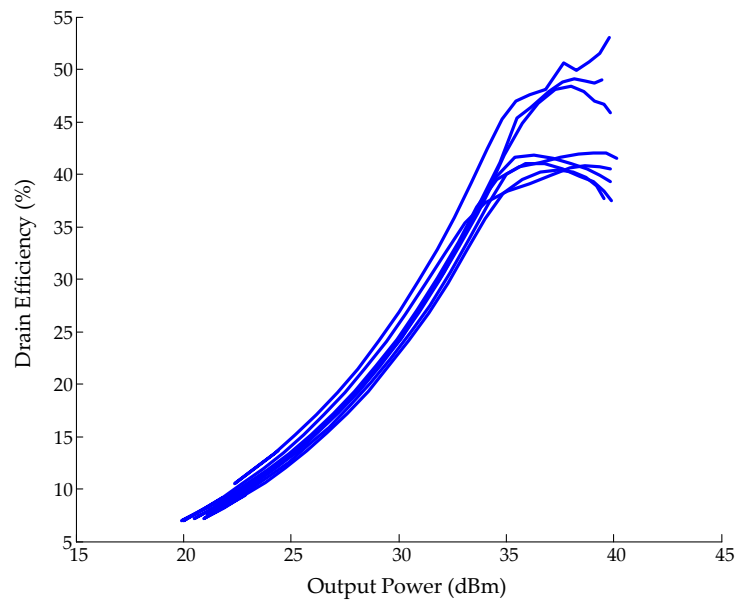
Figure 4.14: Measured CW efficiency of PA versus output power.
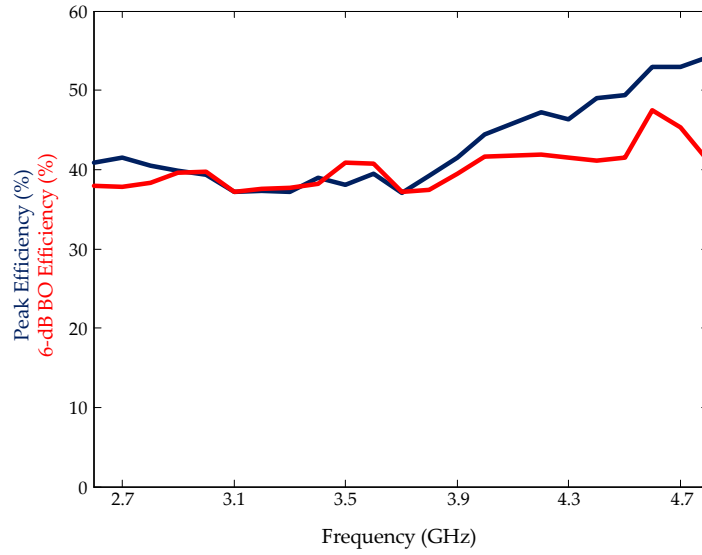
Figure 4.15: Measured efficiency at peak (blue) and 6-dB BO (red) of the PA under CW signal.
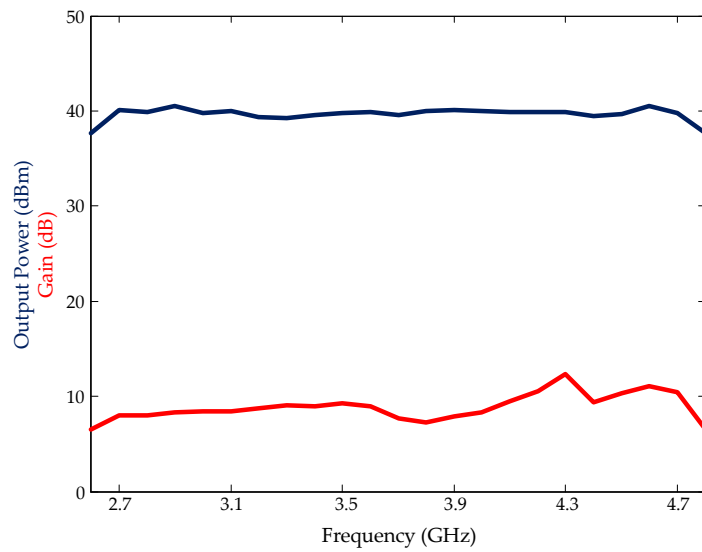
Figure 4.16: Measured output power (blue) and gain (red) of the PA under CW signal.
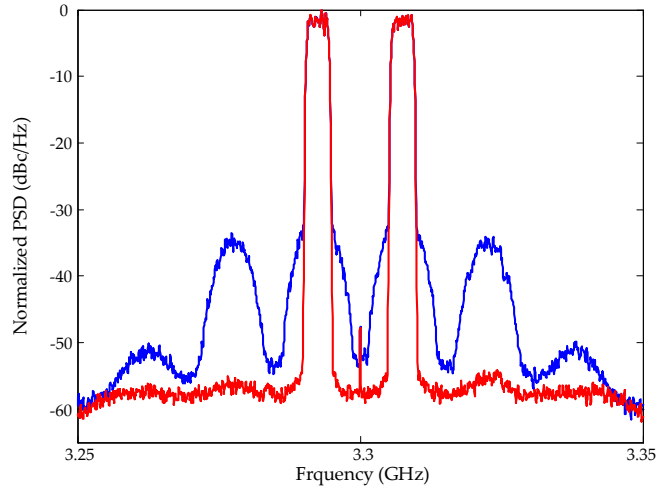
Figure 4.17: Measured spectrum of the output of proposed DPA before (blue) and after (red) linearization when driven with 20 MHz modulated signal.
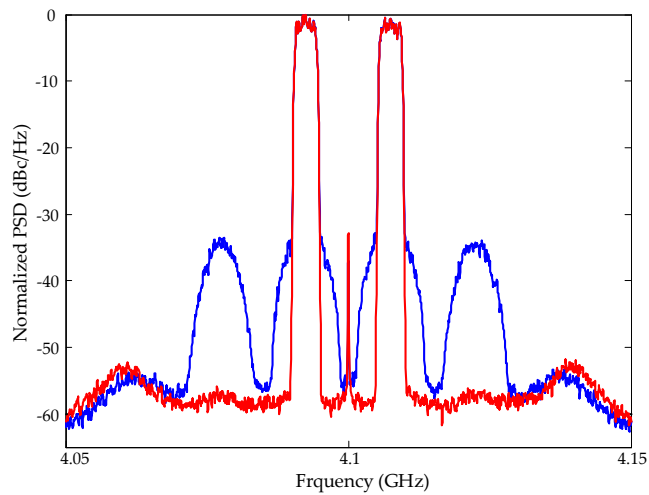
Figure 4.18: Measured spectrum of the output of proposed DPA before (blue) and after (red) linearization when driven with 20 MHz modulated signal.
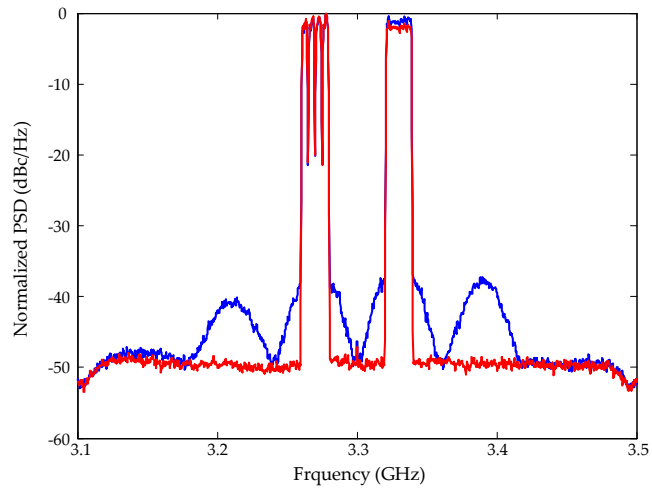
Figure 4.19: Measured spectrum of the output of proposed DPA before (blue) and after (red) linearization when driven with 80 MHz modulated signal.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

This thesis addresses the lack of information on the IMN of the DPA. In Chapter 1 it was shown that with the movement towards future communication systems that more importance is put on spectrum efficiency with the utilization of carrier aggregated signals and signals with high PAPR. As well a natural progression is made to higher frequencies where more empty bands are available for use.

Chapter 2 showed that classical PA topologies do not provide the needed efficiency at BO to efficiently amplify these signals. More complex single ended topologies suffer from restricted BWs. Hence a need is present for efficiency enhancement topologies that provide good BO efficiency and wideband operation. As such the DPA is the most popular in research currently providing adequate results in both these areas for base station applications. The problem or missing link in most research publications is when talking about the input for the DPA. The DPA has two driving factors that are key to its operation, the OCN, and the current profiles provided at the drain. One can not function without the other, but a recent trend has focused on extending the BW of the OCN. This work bridges the gap by providing information on the IMN design to make sure the correct current is provided to the input of the OCN.

Chapter 3 focused on how presenting the proper impedances at the input of the transistor can vary the performance significantly versus input drive. It was shown that the non-linear input capacitance, C_{gs} distorts the signal at the gate of the transistor. This distortion causes AM/AM and AM/PM deterioration. As well, the matching to the second

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harmonic becomes more cumbersome. For the class-AB amplifier it is seen that second harmonic impedance has a direct impact on the efficiency and AM/AM profile of the resulting PA. Moving to higher frequencies it was shown that sensitive regions on the Smith chart are formed where a small mismatch will move the PA from a region of high efficiency to one of low. For the class-C amplifier it was shown that a similar effect occurs but this time also the output power is effected causing varying current profiles depending on input termination.

To combat these issues Chapter 4 introduces a design methodology along with a tool, constant current contours, to aid in the design of the IMN for a DPA. By using constant current contours the drain current can be linked to impedance values at the input for varying drive levels. By doing so the current profiles can be carefully dictated versus frequency and input drive.

Using the described design methodology a 12-W GaN DPA was designed from 3.0-4.8GHz. The simulated results for the main and peaking amplifiers showed good performance as the current profiles across frequency and input drive matched those of the requirements. The overall DPA showed a gain of over 9dB across the band and an efficiency higher then 40% at both peak and BO. To validate the performance, the PA was fabricated and assembled. The PA showed thermal effects due to small package and under CW measurements provided a small signal gain greater than 8dB and BO efficiency greater than 37% across the band. Under modulated signal the PA was linearized under a 80MHz CA, intra-band non-contiguous signal with an ACLR before DPD of 37dBc/Hz and 48dBc/Hz after DPD.

5.2 Future Work

Several areas are worth further investigation at the conclusion of this project. As was mentioned in Chapter 4 the PA experienced significant thermal effects. The measurements can be greatly improved under a pulsed measurement setup where the PA experiences less stress. As well, currently good progress has been made to utilize the design methodology for GaN transistors due to there inherent input non-linearity. For future work the proposed topology can be used to design an LDMOS based DPA where the non-linear capacitance is more detrimental at the output to validate the proposed approach. Finally, as designs move towards higher frequencies the effect of the C_{gs} becomes more pronounced resulting in a bilateral transistor. The design methodology needs to be revised to accommodate this to move beyond the iterative approach presented here to make the IMN design much simpler and quicker.

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